An efficient implementation of BCI EEG net architecture

Project Name

An efficient implementation of BCI EEG net architecture

Objective

The objective is to detect the digit thought by a subject through an efficient implementation of EEG-net in Hardware. You can give the BCI data through UART

Dataset

Following is the suggested dataset; you could use any other dataset.

- http://mindbigdata.com/opendb/index.html

Suggested Resources

- https://iopscience.iop.org/article/10.1088/1741-2552/aace8c/pdf
- https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9925579

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Additional Resources

- https://pages.ucsd.edu/~desa/desaPubs/ieeetransbme.pdf
- https://e-tarjome.com/storage/btn_uploaded/2020-03-11/1583927128_10503-etarjome%20English.pdf
- http://learn.neurotechedu.com/preprocessing/
- https://press.rebus.community/programmingfundamentals/chapter/modular-programming/

Project Submission

Each Project submission should include

- A project report *(in the form ppt slides)* that includes the following details – Motivation, Introduction, Objective, dataset, model selection/implementation, hardware implementation, results, conclusions, and references. Your presentation should not be more than 6 slides
- Project Source Code (Written in a modular manner with appropriate comments) must be uploaded to GitHub and shared with the TA.
- A "Read me" document with instructions on installation and usage must be submitted.
- Demo of the working project.

You are encouraged to try out different model architectures in tensor flow and hardware. You should also try out different optimization techniques on both software and hardware. All your experiment's output should be put in the slides. These will carry extra marks.

For any other details and instructions, contact

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