

# DIGITAL

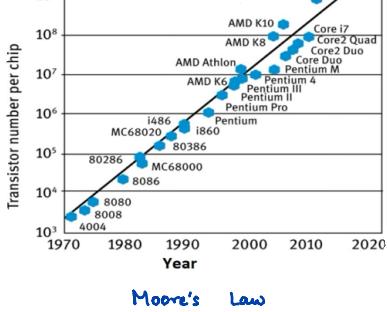
# VLSI

(Very Large Scale Integration)

# UE23EC252B

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# Unit-1 Introduction to MOS Inverters



→ The number of transistors per chip would grow exponentially (doubles every 18 months)

## Synthesis Process

→ Converting HDL Code to optimised gate level design using Standard Library

## Levels of Design Abstraction

Design Level	System Design	Logic Design	Circuit Design	Layout Design
Graphical Representation				
Elements	Blocks, Sub-blocks	Logic Gates	Logic Gates	Geometric Structure

## Design - Style Trade-offs (PPAs)

- Power Consumption
- Performance
- Design Time
- Unit Cost
- NRE Cost (Non-Recurring Engineering) (R&D)

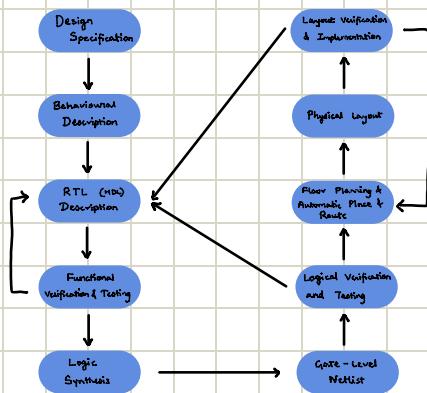
## EDA Tools

- Cadence (Encounter RTL Compiler, Genius, Virtuoso)
- Mentor Graphics (Questa sim, Leonardo Spectrum, Tanner)
- Synopsys (Design Compiler, Genesys)
- Xilinx (ISim, Vivado, Xilinx Synthesis)

IRDS: International Roadmap  
for device & system

ASIC: Application Specific IC's

## VLSI ASIC Design Flow



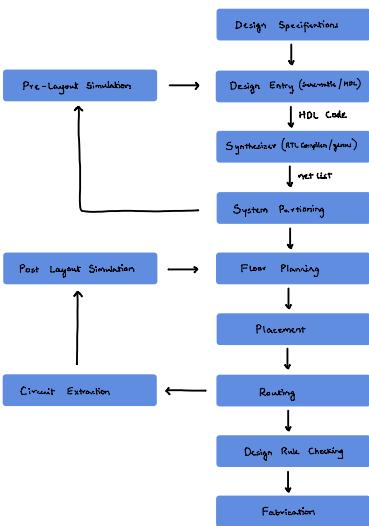
## Challenges

- Big Data Analytics
- Feature Recognition
- IOT Applications
- Logic Device Scaling
- 3D NAND Flash Memory
- Cyber Physical Systems

### Overview of Design Methodology

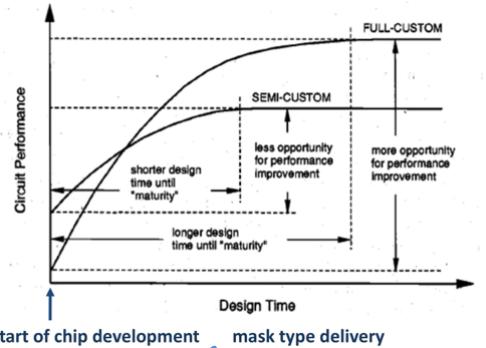
- Design complexity of logic chip increases almost exponentially with number of transistors to be integrated, this is translated into an increase into design cycle time
  - **Design Cycle Time** is the time period from start of chip development until the mask type delivery. Most time is used to achieve desired level of performance at an acceptable cost
  - Design cycle time & achievable circuit performance depends on VLSI design style
- There are 2 types :
- 1) Full Custom Design Style
  - 2) Semi Custom Design Style

### Design Methodology



#### Full Custom

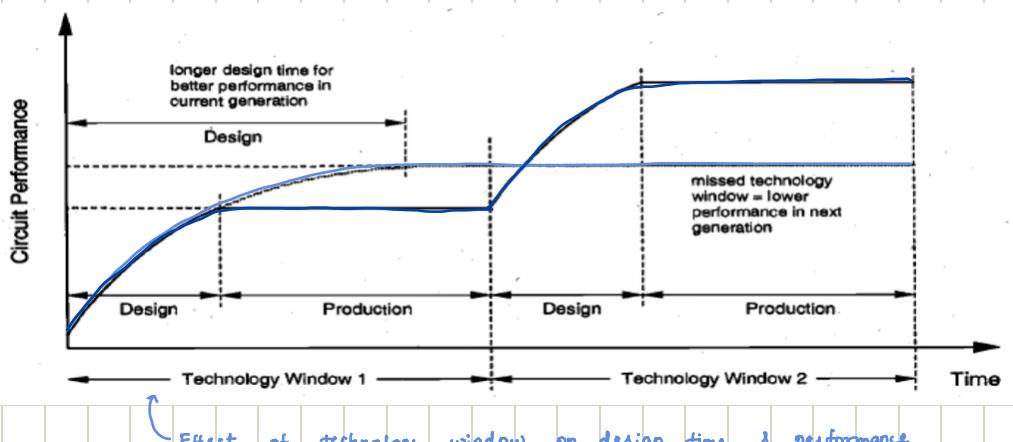
- It requires longer time until the design maturity is reached
- The flexibility in geometry & placement allows more opportunity for performance improvement
- Final product has higher level of performance
- Silicon area is relatively small because of better area utilization



Effect of design style on design cycle time & performance

#### Semi Custom

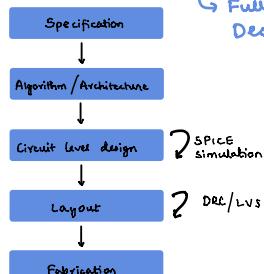
- Less design time & less opportunity for performance improvement
- Design performance is Higher than Full custom



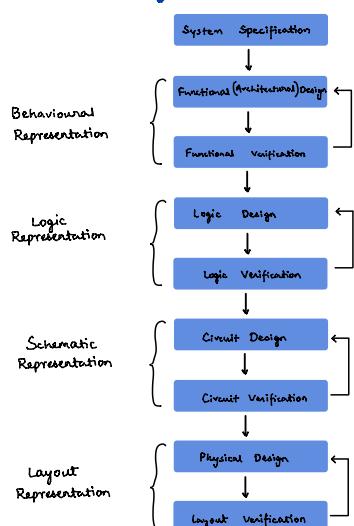
Effect of technology window on design time & performance

### MOS Inverters (Static Characteristics)

↳ Full Custom Design



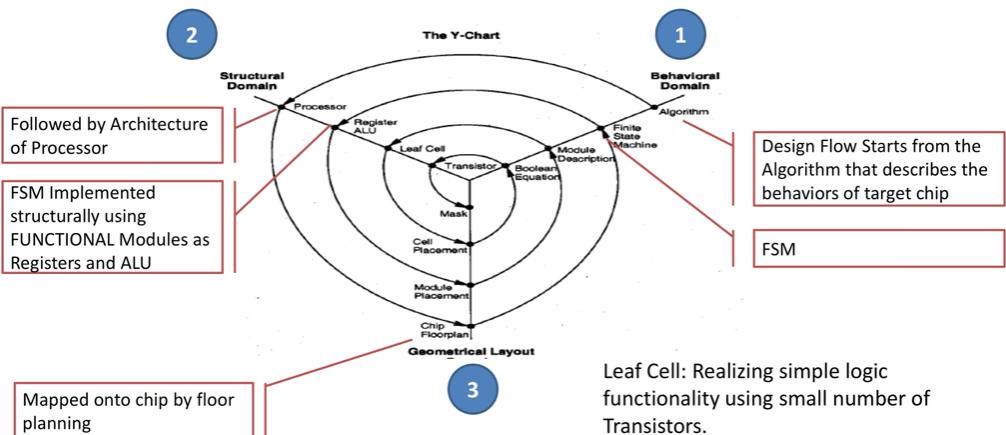
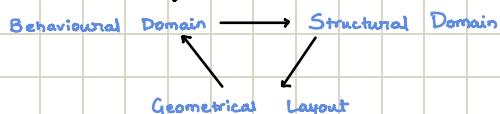
## ASIC Design Flow ★



	Full Custom	Semi Custom
	<ul style="list-style-type: none"> <li>1) Complete design, implementation placement is done from transistor level</li> <li>2) High Cost</li> <li>3) More design time required</li> <li>4) High circuit performance</li> <li>5) Less dependency on existing technology</li> <li>6) Can be used for mass production</li> <li>7) Very high speed</li> <li>8) Complex Circuit Layout</li> </ul> <p>ex: High performance processes, FPGAs &amp; memory chips</p>	<ul style="list-style-type: none"> <li>1) We use pre-design &amp; pre-tested module for designing</li> <li>2) Low Cost</li> <li>3) Less design time required</li> <li>4) Low circuit performance</li> <li>5) More dependency on existing technology</li> <li>6) Can't be used for mass production</li> <li>7) Less speed compared to Full Custom</li> <li>8) Simplified Circuit Layout</li> </ul> <p>ex: STD Cell based, gate arrays etc.,</p>

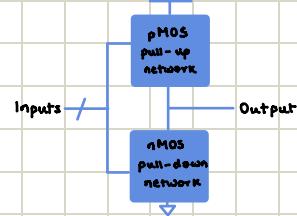
## Y-Chart / Gajski Chart

→ It is a 3-part graphic organizer that is used for describing 3 aspects of a topic



General logic gate using pull-up and pull-down networks

ex: CMOS Circuit

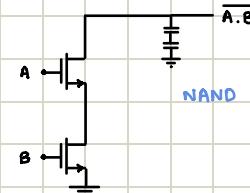


NOTE :

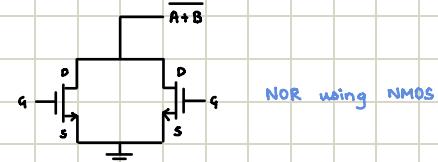
NMOS is a good transfer of logic 0  
PMOS is a good transfer of logic 1

$\rightarrow$  PUN  
pull-up  $\Rightarrow$  pulling to logic 1  
pull-down  $\Rightarrow$  pulling to logic 0  
 $\rightarrow$  PDN

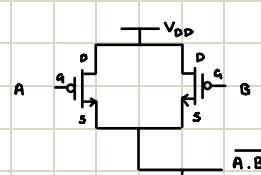
NAND and NOR Gates using Pull Down Network and Pull Up Network



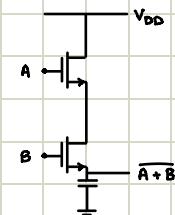
NAND using NMOS



NOR using NMOS



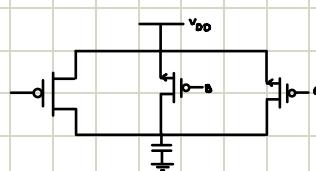
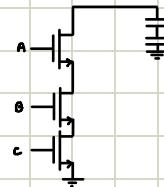
NAND using PMOS



NOR using PMOS

Q. Find CMOS for  $Y = \overline{A \cdot B \cdot C}$

A.

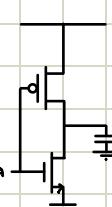


Inverter

$V_{Th}$  - Inverter Threshold Voltage

$V_{T,n}$  - NMOS  $V_{Th}$

$V_{T,p}$  - PMOS  $V_{Th}$

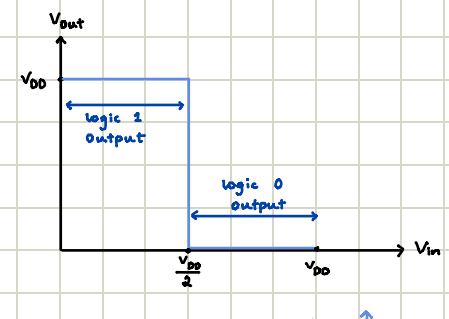


$A \rightarrow \overline{B} = \bar{A}$

Symbol

A	B
0	1
1	0

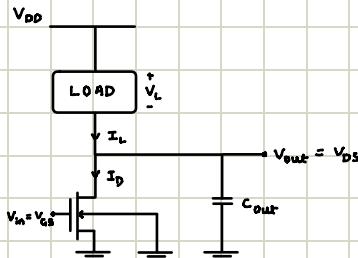
Truth Table



### MOS Inverter Gate

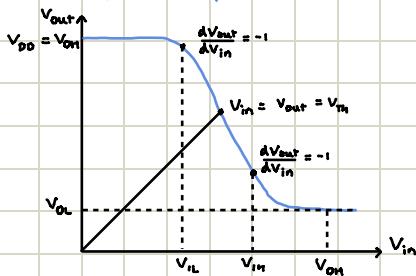
#### NMOS Inverter

- tve load inverter
- nMOSFET load inverter
- Depletion Load inverter
- Enhancement Load inverter
- CMOS inverter

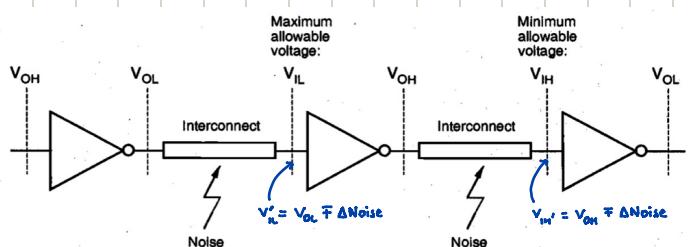
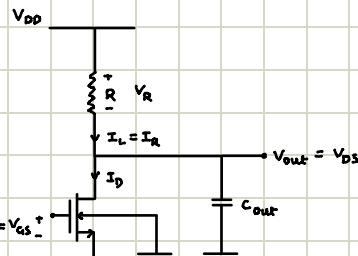


The load for inverter is considered as 2 circuit element in which 1 terminal is connected to  $V_{DD}$  & other to output. NMOS transistor is used as pull-down network in which drain is connected to  $V_{out}$  & source to ground. This is also called as driver transistor. Current entering the node  $V_{out}$  ( $I_L$ ) = current leaving the node ( $I_D$ )

#### → Voltage Transfer Characteristics



- $V_{OH}$ : Max output voltage when output level is '1'
- $V_{OL}$ : Min output voltage when output level is '0'
- $V_{IL}$ : Max input voltage which can be interpreted as '0'
- $V_{IH}$ : Min input voltage which can be interpreted as '1'



#### Noise Margin of MOS Inverter

$$N_{ML} = V_{IL} - V_{OL} \quad (\text{Noise Margin Low})$$

$$N_{MH} = V_{OH} - V_{IH} \quad (\text{Noise Margin High})$$

→ In general

$$\Rightarrow V_{out} = f(V_{in})$$

→ With Noise

$$\Rightarrow V'_{out} = f(V_{in} + \Delta V_{noise})$$

→ Using Taylor Expansion  $\Rightarrow V'_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise}$   
+ higher order terms  
↳ neglected

→ Ideally, The slope of VTC should be very large between  $V_{IL}$  &  $V_{IH}$  because a narrow uncertain (transition) region allows for large noise margin.

Reducing the width of the uncertain region is one of the important design objective

$$\text{Perturbed o/p} = \text{Nominal o/p} + (\text{gain} \times \text{External Perturbation})$$

### Types of Inverters

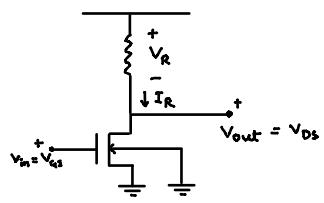
i) Resistive Load

ii) nMOS Load

→ Enhancement → Saturation  
→ Depletion

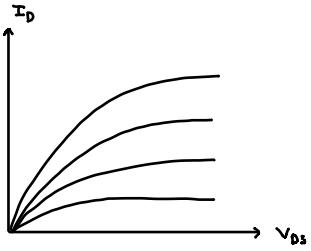
iii) CMOS Load

iv) BiCMOS Load



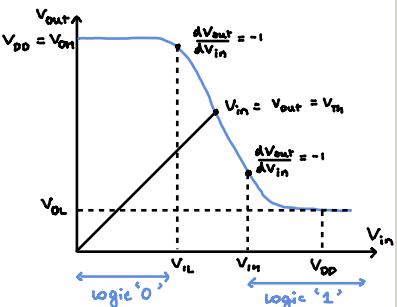
### Resistive Load Inverter

- Enhancement type nMOS is driver device
- Load is simple linear resistance ( $R_L$ )
- Power supply  $V_{DD}$
- $I_D$  of driver MOS =  $I_L$  in DC s state
- $V_{SG} = 0$  (No CLM)
- $V_{Th}$  is always equal to  $V_{To}$



$$K' = \mu_n C_{ox}$$

$$K_n = K' \frac{W}{L}$$



$$\text{Saturation} \Rightarrow V_{GS} > V_{Th}, \quad V_{DS} > V_{GS} - V_{Th}, \quad I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2$$

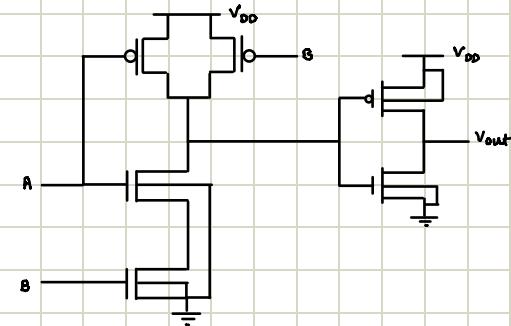
$$= \frac{K_n}{2} (V_{in} - V_{Th})^2$$

Input Voltage Range	Operating Mode
$V_{in} < V_{To}$	Cutoff
$V_{To} \leq V_{in} < V_{out} + V_{Ton}$	Saturation
$V_{in} \geq V_{out} + V_{To}$	Linear

$$\begin{aligned} \text{Cutoff} &\Rightarrow V_{GS} < V_{Th}, \quad I_D = 0 \\ \text{Linear} &\Rightarrow V_{GS} > V_{Th}, \quad V_{DS} < V_{GS} - V_{Th}, \quad I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \\ &= \frac{K_n}{2} \left[ 2(V_{GS} - V_{Th}) V_{DS} - V_{DS}^2 \right] \\ &= \frac{K_n}{2} \left[ 2(V_{in} - V_{Th}) V_{out} - V_{out}^2 \right] \end{aligned}$$

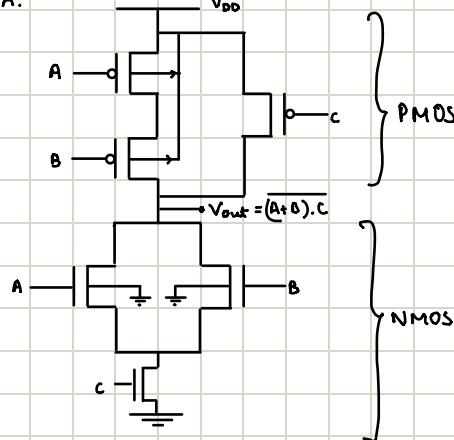
Q. 2 input AND Gate using CMOS Technology

A.



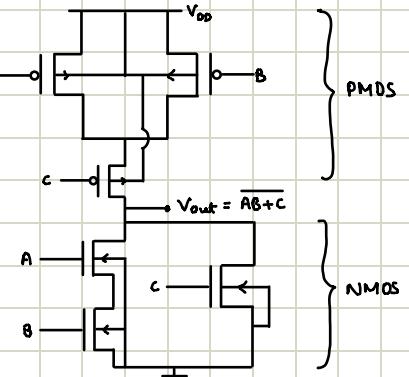
$$Q. \quad Y = (A+B).C$$

A.



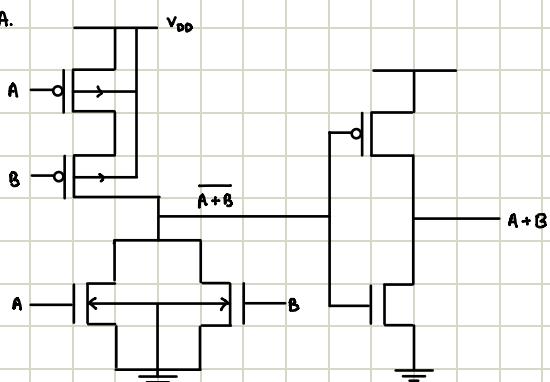
$$Q. \quad Y = \overline{AB} + C$$

A.



$$Q. \quad \overline{\overline{A+B}}$$

A.

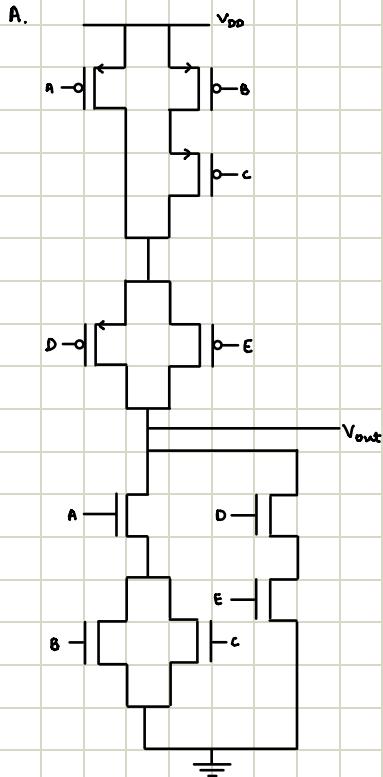


Note :

All Substrate to ground in NMOS

All Substrate to V<sub>DD</sub> in PMOS

Q.  $A(B+C) + DE$



### Power & Area Consideration

#### Power

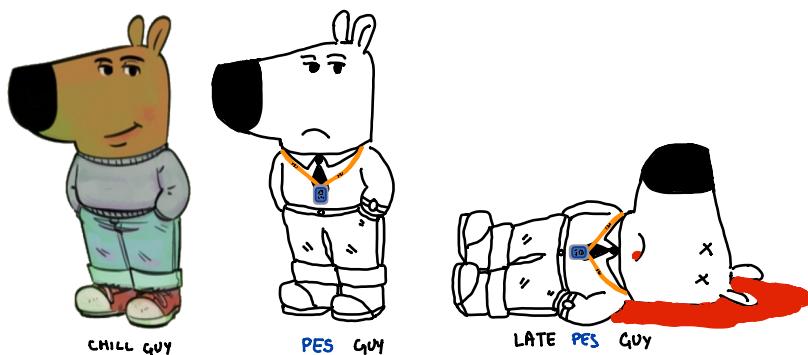
$$\rightarrow P_{dc} = V_{DD} \times I_{dc}$$

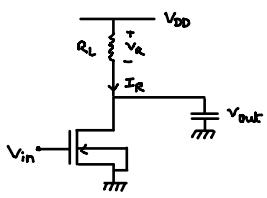
$\rightarrow$  The DC power dissipation of inverter circuit is the product of power supply voltage & amount of current drawn from supply

$$\rightarrow P_{dc} = \frac{V_{DD}}{2} [I_{dc}(v_{in=low}) + I_{dc}(v_{in=high})]$$

#### Area

$\rightarrow \frac{W}{L}$  should be near unity in order to optimise the area but as it contradicts the other design criteria like noise margin, dynamic switching speed & driving capability





### Calculating Critical Voltages

#### 1) $V_{OM}$ :

$$V_{DD} - V_R - V_{out} = 0$$

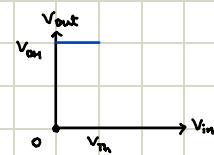
$$V_{out} = V_{DD} - I_R R_L$$

For  $V_{in} < V_{TH}$ , NMOS off  $\Rightarrow I_D = 0$

$$WKT, \quad I_D = I_R = 0$$

$$V_{out} = V_{DD} = V_{OM}$$

$V_{OM} = V_{DD}$  irrespective of resistive load value



#### 2) $V_{OL}$ :

Consider  $V_{in} = V_{OM} = V_{DD}$ , device is in linear region of operation

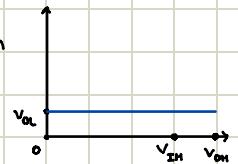
$$V_{out} = V_{OL} = V_{DS}$$

$$I_D = I_R$$

$$I_R = \frac{V_{DD} - V_{out}}{R_L} = \frac{V_{DD} - V_{OL}}{R_L}$$

$$V_{GS} = V_{DD} > V_{TH} \quad (\text{ON})$$

$$V_{DS} = V_{OL} < V_{DD} - V_{TH} \quad (\text{linear})$$



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( 2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2 \right)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[ 2(V_{DD} - V_{TH})V_{OL} - V_{OL}^2 \right]$$

$$= \frac{K_n}{2} \left[ 2(V_{DD} - V_{TH})V_{OL} - V_{OL}^2 \right]$$

$$\Rightarrow \frac{V_{DD} - V_{OL}}{R_L} = K_n (V_{DD} - V_{TH})V_{OL} - \frac{K_n V_{OL}^2}{2}$$

$$\frac{K_n V_{OL}^2}{2} - K_n (V_{DD} - V_{TH}) - \frac{V_{OL}}{R_L} + \frac{V_{DD}}{R_L} = 0$$

$$\frac{K_n V_{OL}^2}{2} - \left( K_n (V_{DD} - V_{TH}) + \frac{1}{R_L} \right) V_{OL} + \frac{V_{DD}}{R_L} = 0$$

$$V_{OL}^2 - 2 \left( V_{DD} - V_{TH} + \frac{1}{K_n R_L} \right) V_{OL} + \frac{2V_{DD}}{K_n R_L} = 0$$

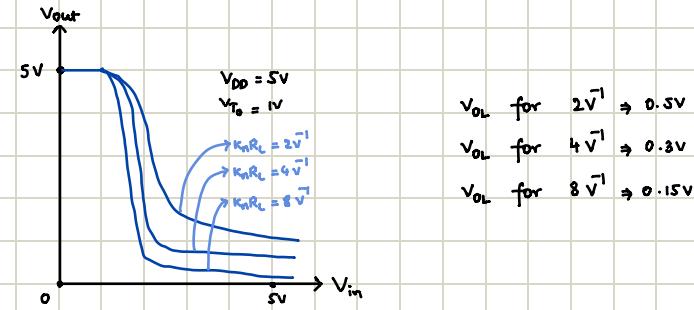
$$V_{OL} = \frac{2 \left( V_{DD} - V_{TH} + \frac{1}{K_n R_L} \right) - \sqrt{4 \left( V_{DD} - V_{TH} + \frac{1}{K_n R_L} \right)^2 - \frac{8V_{DD}}{K_n R_L}}}{2}$$

$$= V_{DD} - V_{TH} + \frac{1}{K_n R_L} - \sqrt{\left( V_{DD} - V_{TH} + \frac{1}{K_n R_L} \right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$V_{DD} \propto K_n R_L$$

- The value of output low voltage must be between 0 &  $V_{DD}$
- Out of the 2 possible solutions, the one which is physically correct for output low is chosen
- The product  $\frac{1}{K_n R_L}$  is one of the important design parameter that determines value of  $V_{OL}$

- VTC for different value of parameter ( $K_n R_L$ )



### 3) $V_{IL}$

$V_{in} = V_{IL}$  because  $V_{DS} > V_{GS} - V_{th} \Rightarrow$  NMOS in saturation

$V_{IL}$  is smaller of the 2 input voltages at which slope VTC becomes  $-1$   $\left( \frac{dV_{out}}{dV_{in}} = -1 \right)$

$$I_R = \frac{V_{DD} - V_{out}}{R_L}$$

$$I_D = \frac{K_n}{2} (V_{in} - V_{T_0})^2$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} (V_{in} - V_{T_0})^2$$

$$\text{Differentiate wrt } V_{in} \Rightarrow 0 - \frac{dV_{out}}{dV_{in}} = \frac{K_n (V_{in} - V_{T_0})}{R_L}$$

$$\text{When } \frac{dV_{out}}{dV_{in}} = -1, \quad V_{in} = V_{IL}$$

$$\frac{1}{R_L} = K_n (V_{IL} - V_{T_0})$$

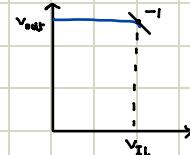
$$V_{IL} = V_{T_0} + \frac{1}{K_n R_L}$$

- To determine output voltage when  $V_{in} = V_{IL}$ ,

$$I_R = I_D \Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} (V_{in} - V_{T_0})^2$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left( V_{T_0} + \frac{1}{K_n R_L} - V_{T_0} \right)^2 = \frac{1}{2 K_n R_L^2}$$

$$V_{DD} - V_{out} = \frac{1}{2 K_n R_L} \Rightarrow V_{out} = V_{DD} - \frac{1}{2 K_n R_L}$$



Q. For  $K_n R_L = 2/4/8$ ,  $V_{DD} = 5V$ ,  $V_{TO} = 1V$ , Find  $V_{IL}$

$$A. V_{IL} = V_{TO} + \frac{1}{K_n R_L}$$

$$(V_{IL})_{2V} = 1 + \frac{1}{2} = 1.5V \Rightarrow V_{out} = 5 - \frac{1}{4} = 4.75V$$

$$(V_{IL})_{4V} = 1 + \frac{1}{4} = 1.25V \Rightarrow V_{out} = 5 - \frac{1}{8} = 4.875V$$

$$(V_{IL})_{8V} = 1 + \frac{1}{8} = 1.125V \Rightarrow V_{out} = 5 - \frac{1}{16} = 4.9375V$$

4)  $V_{IH}$

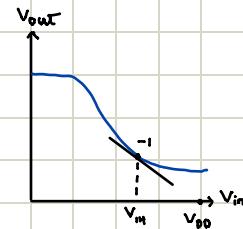
$$\rightarrow \text{When } \frac{dV_{out}}{dV_{in}} = -1, \quad V_{in} = V_{IH}$$

$\rightarrow$  NMOS in linear region

$\rightarrow$  From KCL,

$$I_{RL} = I_D \quad (\text{linear})$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left[ 2(V_{in} - V_{TO}) V_{out} - V_{out}^2 \right]$$



Differentiate wrt  $V_{in}$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{K_n}{2} \left[ 2(V_{in} - V_{TO}) \frac{dV_{out}}{dV_{in}} + 2V_{out} - 2V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$\text{Substitute } \frac{dV_{out}}{dV_{in}} = -1 \quad \& \quad V_{in} = V_{IH}$$

$$\frac{1}{K_n R_L} = -V_{IH} + V_{TO} + 2V_{out}$$

$\rightarrow$  To find  $V_{out}$  when  $V_{in} = V_{IH}$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left[ 2 \left( V_{TO} + 2V_{out} - \frac{1}{K_n R_L} - V_{TO} \right) V_{out} - V_{out}^2 \right] = \frac{K_n}{2} \left[ 2 \left( 2V_{out} - \frac{1}{K_n R_L} \right) V_{out} - V_{out}^2 \right]$$

$$V_{DD} - V_{out} = \frac{K_n R_L}{2} \left[ 2V_{out}^2 - \frac{2V_{out}}{K_n R_L} - \frac{V_{out}^2}{2} \right] = K_n R_L \left[ \frac{3}{2} V_{out}^2 - \frac{V_{out}}{K_n R_L} \right]$$

$$V_{out} \left( \frac{3}{2} K_n R_L \right) - V_{out} - V_{DD} = 0 \Rightarrow V_{out} = \sqrt{\frac{2 \cdot V_{DD}}{3 K_n R_L}}$$

$$V_{IH} = V_{TO} + 2 \sqrt{\frac{2 V_{DD}}{3 K_n R_L}} - \frac{1}{K_n R_L}$$

Observation:

$$\rightarrow V_{IH} \propto \frac{1}{K_n R_L}$$

$\rightarrow$  If  $K_n R_L$  increased,  $V_{IH}$  decreases

## Note :

1) Higher the value of  $K_n R_L$ , smaller is the  $V_{IH}$  (logic 1 : larger range)

2) Higher the value of  $K_n R_L$ ,

Smaller the  $V_{OL}$ .

(For ideal value of  $V_{OL}$  of inverter,  $K_n R_L$  should be longer)

3)  $V_{IL}, V_{IH}, V_{OL}$  are inversely proportional to  $K_n R_L$

## Summary

$$V_{OH} = V_{DD}$$

$$V_{OL} = (V_{DD} - V_{TO} + \frac{1}{K_n R_L}) - \sqrt{(V_{DD} - V_{TO} + \frac{1}{K_n R_L})^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$V_{IL} = V_{TO} + \frac{1}{K_n R_L}$$

$$V_{IH} = V_{TO} + \sqrt{\frac{2 V_{DD}}{3 K_n R_L}} - \frac{1}{K_n R_L}$$

Q. Consider the following inverter design problem:  $V_{DD} = 5V$ ,  $K_n = 30\text{mA}/V^2$  &  $V_{TO} = 1V$ . Design a resistive load inverter circuit with  $V_{OL} = 0.2V$ . Specifically, determine  $W/L$  ratio of the driver transistor and the value of load resistor that achieve required  $V_{OL}$ .

A.  $V_{OL} = 0.2V = V_{out}$

$$V_{OH} = V_{DD} = 5V = V_{in} = V_{GS}$$

$$K' = \mu n C_{ox}$$

$$K_n = \frac{K'W}{L}$$

$$V_{DS} = 0.2V < (V_{GS} - V_{TH}) \Rightarrow \text{Linear region}$$

$$I_R = I_D(\text{linear})$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{K_n'}{2} \frac{W}{L} [2(V_{GS} - V_{TO})V_{OL} - V_{OL}^2]$$

$$\frac{4.8}{R_L} = \frac{30 \times 10^{-6}}{2} \cdot \frac{W}{L} [2(4)(0.2) - (0.2)^2]$$

$$\frac{L}{WR_L} = 4.875 \times 10^{-6}$$

$$\frac{WR_L}{L} = 2.051 \times 10^5 R_L = 205.1 \text{ k}\Omega$$

W/L Ratio	$R_L (\text{k}\Omega)$	Power (mW) $P_{DC, \text{avg}}$
1	205	0.0585
2	102.5	0.117
3	68.33	0.175
4	51.25	0.234
5	41	0.2926
6	34.16	0.3512

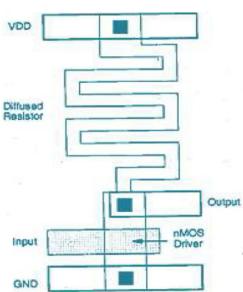
$$P_{DC} = \frac{V_{DD}}{2} \left[ I_{DC} (V_{in} = \text{low}) + I_D (V_{in} = \text{high}) \right]$$

$$= \frac{V_{DD}}{2} \left[ \frac{V_{DD} - V_{OL}}{R_L} \right]$$

→ Power consumption increases as  $R_L$  decreases &  $\frac{W}{L}$  increases

→ If power consumption is the concern,  $\frac{W}{L}$  is kept low &  $R_L$  is large

### Chip Area

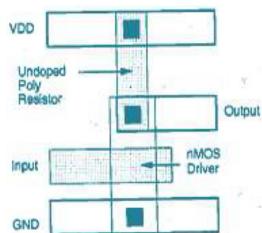


→ Chip area occupied by resistive load inverter depends on ( $\frac{W}{L}$ ) ratio of NMOS driver transistor &  $R_L$  value

→ 2 Methods of resistor fabrication :

#### Diffused Resistor

- Isolated n-type / p-type diffusion region with one contact on each end
- The resistance is determined by density of diffusion region & the dimension ( $\frac{L}{W}$  ratio)
- Diffusion range, sheet resistance  $\Rightarrow 20 - 100 \Omega/\text{square}$
- Large  $\frac{L}{W}$  required to get resistor of  $(10-100) \Omega$



#### Undoped Polysilicon Resistor

- Polysilicon layers are heavily doped in order to reduce resistivity. The sheet resistivity of doped polysilicon interconnect & gate is  $20 - 40 \Omega/\text{square}$
- Drawback:  $R$  value of this can't be controlled very accurately which results in large variation in VTC

Q. Consider a resistive load inverter circuit with  $V_{DD} = 5V$ ,  $k_n' = 20 \mu\text{A}/\text{V}^2$ ,  $V_{TO} = 0.8V$

$R_L = 200 \Omega$ ,  $\frac{W}{L} = 2$ . Calculate  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$  on the VTC & find noise margins

$$A. K_n R_L = k_n' R_L \times \frac{W}{L} = 4 \times 2 = 8$$

$$V_{OH} = V_{DD}$$

$$= 5V$$

$$V_{OL} = \left( V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right) - \sqrt{\left( V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right)^2 - \frac{2 V_{DD}}{K_n R_L}}$$

$$= \left( 5 - 0.8 + \frac{1}{8} \right) - \sqrt{\left( 5 - 0.8 + \frac{1}{8} \right)^2 - \frac{2 \times 5}{8}}$$

$$= 4.325 - 4.18$$

$$= 0.147V$$

$$V_{IL} = V_{TO} + \frac{1}{K_n R_L}$$

$$= 0.8 + 0.125$$

$$= 0.925V$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8 V_{DD}}{3 K_n R_L}} - \frac{1}{K_n R_L}$$

$$= 0.8 + \sqrt{\frac{8 \times 5}{3 \times 8}} - \frac{1}{8} = 1.966V$$

$$\text{Noise Margin High} \Rightarrow NM_H = V_{DD} - V_{IH} = 5 - 1.966 = 3.034V$$

$$\text{Noise Margin Low} \Rightarrow NM_L = V_{IL} - V_{OL} = 0.925 - 0.147 = 0.778V$$

For better noise immunity, noise margin for low signals should be 25% of  $V_{DD}$

Q. Design resistive load inverter with  $R = 1\text{ k}\Omega$  such that  $V_{OL} = 0.6\text{ V}$ .

The enhancement-type NMOS driver transistor has the following parameters:

$$V_{DD} = 5\text{ V}, \quad V_{TO} = 1\text{ V}, \quad \mu_nC_{ox} = 22\text{ mA/V}^2$$

a) Determine required  $W/L$  ratio

b) Determine  $V_{IL}$  &  $V_{IH}$

c) Determine  $NM_L$  &  $NM_H$

$$A. a) V_{OL} = \left( V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right) - \sqrt{\left( V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$0.6 = \left( 5 - 1 + \frac{1}{\frac{W}{L} \times 22 \times 10^{-6} \times 10^3} \right) - \sqrt{\left( 5 - 1 + \frac{1}{\frac{W}{L} \times 22 \times 10^{-6} \times 10^3} \right)^2 - \frac{2 \times 5}{\frac{W}{L} \times 22 \times 10^{-6} \times 10^3}}$$

$$= \left( 4 + \frac{500}{\frac{W}{L}} \right) - \sqrt{\left( 4 + \frac{500}{\frac{W}{L}} \right)^2 - \left( \frac{5000}{\frac{W}{L}} \right)}$$

$$\left( 3.4 + \frac{500}{\frac{W}{L}} \right)^2 = \left( 4 + \frac{500}{\frac{W}{L}} \right)^2 - \left( \frac{5000}{\frac{W}{L}} \right)$$

$$\frac{5000}{\frac{W}{L}} = \left( 4 + \frac{500}{\frac{W}{L}} + 3.4 + \frac{500}{\frac{W}{L}} \right) \left( 4 + \frac{500}{\frac{W}{L}} - 3.4 - \frac{500}{\frac{W}{L}} \right)$$

$$(a^2 - b^2 = (a+b)(a-b))$$

$$\frac{5000}{11 \times 0.6 \frac{W}{L}} = 7.4 + \frac{1000}{\frac{W}{L}}$$

$$\frac{1000}{\frac{W}{L}} \left( \frac{5}{0.6} - 1 \right) = 7.4 \Rightarrow \frac{W}{L} = \frac{1000}{11 \times 7.4} \left( \frac{5}{0.6} - 1 \right) = 90.1$$

$$b) V_{IL} = V_{TO} + \frac{1}{K_n R_L} = 1 + \frac{1}{90.1 \times 22 \times 10^{-6} \times 10^3} = 1.504\text{ V}$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8V_{DD}}{3K_n R_L}} - \frac{1}{K_n R_L}$$

$$= 1 + \sqrt{\frac{8 \times 5}{3} \times 0.504} - 0.504 \approx 2\text{ V}$$

$$c) NM_L = V_{IL} - V_{OL}$$

$$= 1.504 - 0.6 = 0.904\text{ V}$$

$$NM_H = V_{OH} - V_{IH}$$

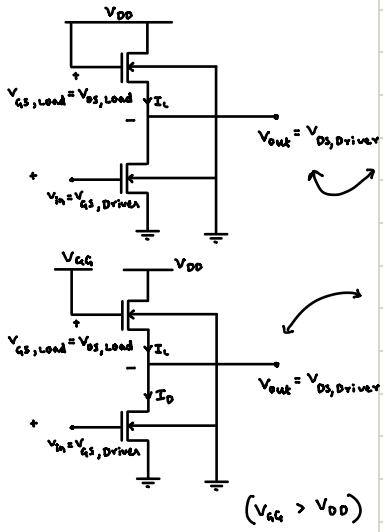
$$= 5 - 2 = 3\text{ V}$$

### Area

→  $W/L$  should be near unity in order to optimize the area but as it contradicts the other design criteria like noise margin, dynamic switching speed & driving capability (trade off)

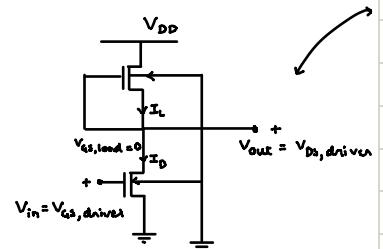
### NMOS Load Inverters

- Large area occupied by load resistor inverter, hence not suitable for digital circuits
- nMOS transistor as active load device
- Main advantage of using MOSFET as load device is that the silicon area occupied by transistor is usually smaller than that occupied by resistive load
- 2 Types :
  - i) Enhancement - load NMOS Inverter
  - ii) Depletion - load NMOS Inverter



#### Enhancement - Load nMOS Inverter (no channel)

- Depending on bias voltage applied to its gate terminal, the load transistor can be operated either in saturation or linear region
- Saturated enhancement type nMOS Load
  - Required single voltage supply & relatively simple fabrication process, yet  $V_{OH}$  level is limited to  $V_{DD} - V_{T,load}$  ( $V_{DS} = V_{GS}$ )
- Linear enhancement type nMOS Load
  - $V_{DS} = V_{DD} \Rightarrow$  higher noise margins compared to saturated load inverter ( $V_{GS} \gg V_{DS}$ )
  - Drawback is that it uses 2 power supply voltages
- Both suffer from relatively high stand-by (DC) power dissipation



#### Depletion - Load nMOS Inverter (channel pre-fabricated)

- Fabrication process is slightly complicated in depletion load inverter channel implant to adjust threshold voltage of load device
- Advantages of Depletion load nMOS inverter
  - i) Sharp VTC transition & better noise margins
  - ii) Single power supply
  - iii) Smaller overall layout area
- $V_{T,load} = -ve$ ,  $V_{T,driver} = +ve$
- Single p-substrate (both driver & load)
- Channel is already present
- $V_{GS} = 0$ , NMOS is already ON
- $V_{SB}$  of depletion load is  $V_{out}$
- $V_{T,load}$  is a function of  $V_{out}$
- $V_{SB,driver} = 0$

$$\rightarrow V_{T,load} = V_{TO,load} + \gamma (\sqrt{2\phi_F(1+v_{out})} - \sqrt{2\phi_F})$$

$$\rightarrow \text{Device in saturation : } I_D = \frac{k_n}{2} (V_{GS} - V_{TH})^2$$

$$I_{D,load} = \frac{k_n,load}{2} [-V_{T,load}(v_{out})]^2$$

$$= \frac{k_n,load}{2} |V_{T,load}(v_{out})|^2$$

$$\text{Device in linear : } I_D = \frac{k_n}{2} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

$$I_{D,load} = \frac{k_n,load}{2} [2|V_{T,load}(v_{out})|(V_{DD} - v_{out}) - (V_{DD} - v_{out})^2]$$

For Depletion Load ,

$$V_{GS} = 0V$$

$$V_{DS} = V_{DD} - v_{out} \quad V_{T,load} \rightarrow \text{function of } v_{out}$$

$$V_{SB} = v_{out} \quad \text{channel already formed}$$

$$V_T = -V_E \quad \text{always ON } (V_{GS} = 0)$$

Enhancement driver ,

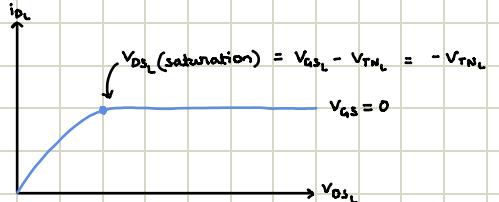
$$V_{GS} = V_{in}$$

$$V_{DS} = v_{out}$$

$$V_{T,driver} = V_{TO}$$

$$V_{SB} = 0V$$

$$V_T = +V_E$$



$$\rightarrow \text{Average DC Power} \Rightarrow P_{DC} = V_{DD} \times I_{DC}$$

$$= \frac{V_{DD}}{2} [I_{DC}(V_{in}=0) + I_{DC}(V_{in}=V_{on})]$$

For input high, load  $\rightarrow$  saturation ( $I_{DC_L}$ )

driver  $\rightarrow$  linear ( $I_{DC_N}$ )

$$\rightarrow P_{DC} = \frac{V_{DD}}{2} [I_{DC_L}(\text{sat})]$$

$$\begin{cases} V_{GS} = 0 \\ V_T = V_{T,load} (v_{out}) \end{cases}$$

$$P_{DC} = \frac{V_{DD}}{2} [I_{DC_N}(\text{lin})]$$

$$\begin{cases} V_{GS} = V_{in} = V_{on} \\ V_T = V_{TH} \end{cases}$$

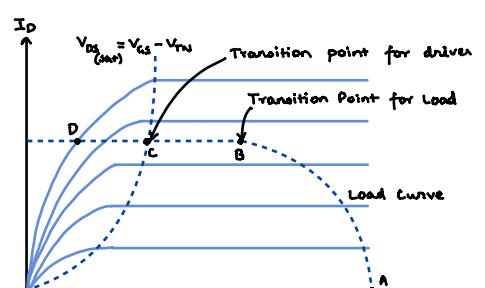
$$P_{DC} = \frac{V_{DD}}{2} \left[ \frac{k_n,load}{2} |V_{T,load}(v_{out})|^2 \right]$$

$$= \frac{1}{4} \cdot V_{DD} \cdot k_n,load |V_{T,load}(v_{out})|^2$$

$$P_{DC} = \frac{V_{DD}}{4} k_n,load |V_{T,load}(v_{out})|^2$$

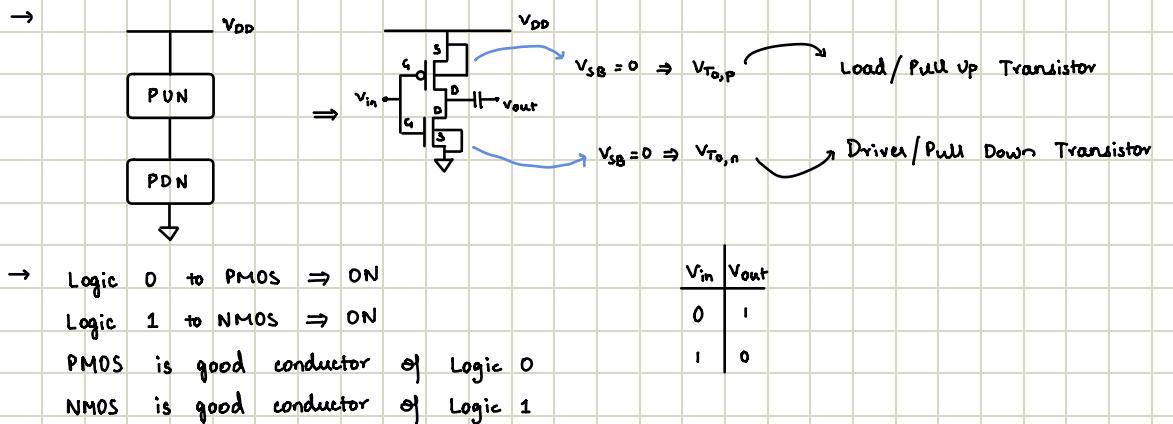
$$P_{DC} = \frac{V_{DD}}{2} \left[ \frac{k_n}{2} [2(v_{on} - V_{TH}) - V_{DS}] \right] = \frac{V_{DD} k_n}{4} [2(v_{on} - V_{TH}) V_{DS} - V_{DS}^2]$$

$V_{in}$	$V_{out}$	Driver	Load
$V_{OL}$	$V_{on}$	cutoff	linear
$V_{IL}$	$\approx V_{on}$	saturation	linear
$V_{on}$	$V_{on}$	linear	saturation
$V_{IH}$	$\approx$ small	linear	saturation



Merging the two transistor output characteristics when input  $V_{in}$  changes from  $V_{OL}$  to  $V_{on}$

### CMOS Inverter



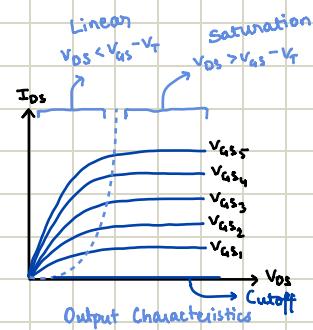
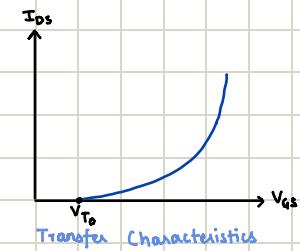
$\rightarrow$  Case (i) ( $V_{in} = 0$ , PMOS ON, NMOS OFF)

$$V_{in} = 0, V_{out} = V_{DD}$$

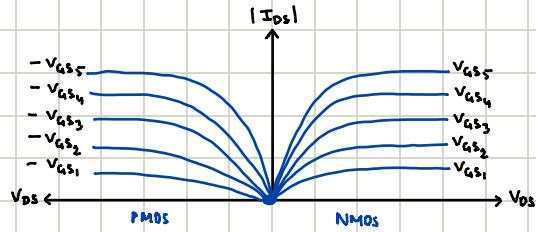
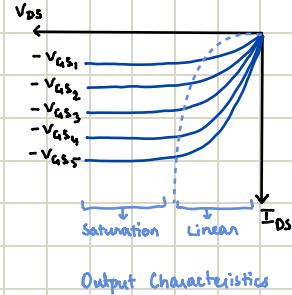
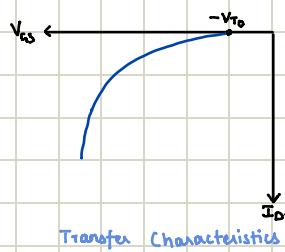
Case (ii) ( $V_{in} = 1$ , PMOS OFF, NMOS ON)

$$V_{in} = V_{DD}, V_{out} = 0$$

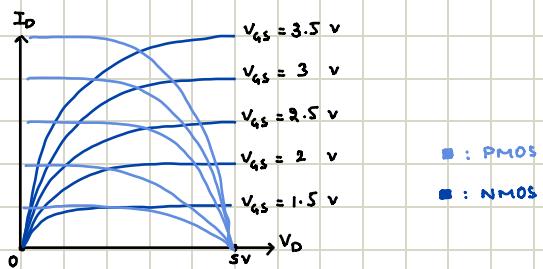
$\rightarrow$  For NMOS,



$\rightarrow$  For PMOS,

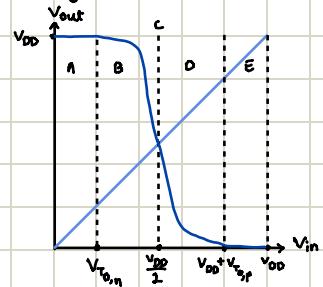


→ Take CMOS Inverter,  
 $V_{DD} = 5V$   
 $V_{TO,n} = 1V$   
 $V_{TO,p} = -1V$   
 $V_{TO,n} = |V_{TO,p}| = 1V$



Superimposed NMOS & PMOS

Using this we draw



VTC

Region	Input ( $V_{in}$ )	Output ( $V_{out}$ )	PMOS	NMOS
I	$V_{OL}$	$V_{OH}$	Linear	OFF
II	$\approx V_{OL}$	$< V_{OH}$	Linear	Saturation
III	$V_{DD}/2$	$V_{DD}/2$	Saturation	Saturation
IV	$\approx V_{OH}$	$> V_{OH}$	Saturation	Linear
V	$V_{OH}$	$V_{OL}$	OFF	Linear

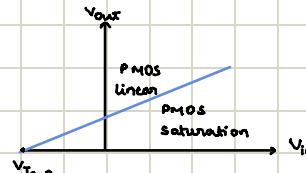
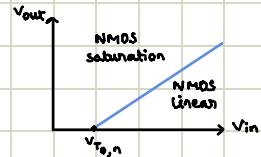
### Advantages

- Steady state power dissipation of CMOS inverter is virtually negligible, except for small power dissipation due to leakage current
- VTC exhibits a full output voltage swing between 0 &  $V_{DD}$  and that the VTC transition is usually very sharp

### Disadvantages

- 2 separate substrate is required

- More Area



Case (i) : ( $V_{in} < V_{Ton}$ )

→ nMOS OFF

→ pMOS ON (linear region)

→  $I_{D,in} = I_{D,p} = 0$

The D to S voltage of pMOS is 0,  $V_{out} = V_{DS} = V_{DD}$

Case (ii) : ( $V_{in} > V_{DD} + V_{Top}$ )

→ pMOS OFF

→ nMOS ON Linear region

→  $V_{DS,n} = 0V$

$V_{out} = V_{DL} = 0V$

Case (iii) : ( $V_{in} = V_{IL}$ )

→ nMOS ON saturation

→ pMOS ON linear

→ Since  $I_{D,n} = I_{D,p}$ ,

$$\frac{K_n}{2} (V_{in} - V_{Ton})^2 = \frac{K_p}{2} [2(V_{GSp} - V_{Top}) V_{DS,p} - V_{DS,p}^2]$$

$$K_n (V_{in} - V_{Ton})^2 = K_p [2(V_{in} - V_{DD} - V_{Top})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

Differentiating wrt  $V_{in}$

$$2K_n (V_{in} - V_{Ton}) = K_p \left[ 2(V_{in} - V_{DD} - V_{Top}) \frac{\partial V_{out}}{\partial V_{in}} + 2(V_{out} - V_{DD}) - 2(V_{out} - V_{DD}) \frac{\partial V_{out}}{\partial V_{in}} \right]$$

$$K_n (V_{IL} - V_{Ton}) = K_p [-V_{IL} + V_{DD} + V_{Top} + V_{out} - V_{DD} + V_{out} - V_{DD}]$$

$$\frac{K_n}{K_p} (V_{IL} - V_{Ton}) + V_{IL} - V_{Top} + V_{DD} = 2V_{out} \Rightarrow \frac{K_p(2V_{out} + V_{Top} - V_{DD})}{K_n + K_p} + K_n V_{Ton} = V_{IL}$$

$$V_{IL} = \frac{(2V_{out} + V_{Top} - V_{DD}) + \frac{K_p}{K_n} V_{Ton}}{1 + \frac{K_n}{K_p}}$$

$$V_{IL} = \frac{(2V_{out} + V_{Top} - V_{DD}) + K_r V_{Ton}}{1 + K_r}$$

$$\left( \frac{\partial V_{out}}{\partial V_{in}} = -1 \Rightarrow V_{in} = V_{IL} \right)$$



Case (iv): ( $V_{in} = V_{IH}$ )

$\rightarrow nMOS \text{ ON linear}$

$pMOS \text{ ON saturation}$

$\rightarrow I_{Dn} (\text{linear}) = I_{Dp} (\text{saturation})$

$$\frac{K_n}{2} [2(V_{GSn} - V_{Th})V_{DS} - V_{DS}^2] = \frac{K_p}{2} [V_{GSp} - V_{ToP}]^2$$

$$\frac{K_n}{2} [2(V_{in} - V_{Ton})V_{out} - V_{out}^2] = \frac{K_p}{2} [(V_{in} - V_{DD}) - V_{ToP}]^2$$

$$\frac{K_n}{K_p} \left[ 2(V_{in} - V_{Ton}) \frac{\partial V_{out}}{\partial V_{in}} + 2V_{out} - 2V_{out} \frac{\partial V_{out}}{\partial V_{in}} \right] = \frac{K_p}{K_n} \times \left( V_{in} - V_{DD} - V_{ToP} \right)$$

$$K_n \left[ -V_{IH} + V_{Ton} + V_{out} + V_{out} \right] = K_p (V_{IH} - V_{DD} - V_{ToP})$$

$$\left( \frac{\partial V_{out}}{\partial V_{in}} = -1 \Rightarrow V_{in} = V_{IH} \right)$$

$$\frac{K_n}{K_p} \left[ 2V_{out} - V_{IH} + V_{Ton} \right] = V_{IH} - V_{DD} - V_{ToP}$$

$$\frac{K_n}{K_p} \left[ 2V_{out} + V_{Ton} \right] + V_{DD} + V_{ToP} = \left( 1 + \frac{K_n}{K_p} \right) V_{IH}$$

$$V_{IH} = \frac{K_p (2V_{out} + V_{Ton}) + V_{DD} + V_{ToP}}{1 + K_p}$$

Case (v): Region C,  $V_{in} = V_{Th}$

$\rightarrow$  Both  $nMOS \& pMOS$  in saturation

$I_{Dn} (\text{saturation}) = I_{Dp} (\text{saturation})$

$$\frac{K_n}{2} [V_{GSn} - V_{Ton}]^2 = \frac{K_p}{2} [V_{GSp} - V_{ToP}]^2$$

$$K_n (V_{in} - V_{Ton})^2 = K_p (V_{in} - V_{DD} - V_{ToP})^2$$

$$(V_{in} - V_{Ton}) = \pm \sqrt{\frac{K_p}{K_n} (V_{in} - V_{DD} - V_{ToP})^2}$$

-ve is valid, +ve gives denominator as 0

$$V_{in} - V_{Ton} = -\sqrt{\frac{1}{K_p}} V_{in} + \sqrt{\frac{1}{K_p} (V_{DD} + V_{ToP})}$$

$$V_{in} = V_{Th} = \frac{V_{Ton} + \sqrt{\frac{1}{K_p} (V_{DD} + V_{ToP})}}{1 + \sqrt{\frac{1}{K_p}}}$$

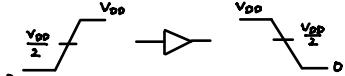
$\rightarrow$  For ideal CMOS inverter,  $V_{Ton} = 1V$ ,  $V_{ToP} = -1V$ ,  $\frac{K_p}{K_n} = 1$

$$V_{Th} = \frac{1 + (V_{DD} - 1)}{1 + 1} = \frac{V_{DD}}{2}$$

$\rightarrow$  For symmetric CMOS inverter

$$K_p = \frac{K_n}{K_p} = 1 \Rightarrow \frac{M_n(\frac{w}{L})_n}{M_p(\frac{w}{L})_p} = 1$$

$$\text{And typically, } 1 = \frac{580 (\frac{w}{L})_n}{230 (\frac{w}{L})_p} \Rightarrow (\frac{w}{L})_p \approx 2.5 (\frac{w}{L})_n$$



Summary,

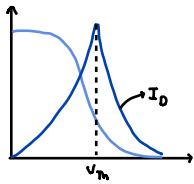
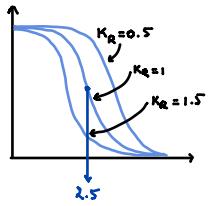
$$\rightarrow V_{DL} = 0V \quad [I_{Dn} = I_{Dp} = 0]$$

$$\rightarrow V_{DM} = V_{DD}$$

$$\rightarrow V_{IL} = \frac{(2V_{out} + V_{ToP} - V_{DD}) + K_p V_{Ton}}{1 + K_p} \quad [I_{Dn} (\text{saturation}) = I_{Dp} (\text{linear})]$$

$$\rightarrow V_{IH} = \frac{K_p (2V_{out} + V_{Ton}) + V_{DD} + V_{ToP}}{1 + K_p} \quad [I_{Dn} (\text{linear}) = I_{Dp} (\text{saturation})]$$

$$\rightarrow V_{Th} = \frac{V_{Ton} + \sqrt{\frac{1}{K_p} (V_{DD} + V_{ToP})}}{1 + \sqrt{\frac{1}{K_p}}} \quad [I_{Dn} (\text{saturation}) = I_{Dp} (\text{saturation})]$$



Q. Assume  $V_{DD} = 5V$ ,  $V_{T_{on}} = 1V$ ,  $V_{Top} = -1V$

$K_R = 0.5, 1, 1.5$ . Determine  $V_{Th}$

$$A. \text{ at } K_R = 0.5, \quad V_{Th} = \frac{1 + \sqrt{\frac{1}{0.5}(5-1)}}{1 + \sqrt{\frac{1}{0.5}}} = 2.757$$

$$\text{at } K_R = 1, \quad V_{Th} = \frac{1 + \sqrt{\frac{1}{1}(5-1)}}{1 + \sqrt{\frac{1}{1}}} = 2.5$$

$$\text{at } K_R = 1.5, \quad V_{Th} = \frac{1 + \sqrt{\frac{1}{1.5}(5-1)}}{1 + \sqrt{\frac{1}{1.5}}} = 2.348$$

→ As size of pMOS is increased greater than 2.5 times, the VTC curve shifts towards right

→ As size of pMOS is decreased lesser than 2.5 times, the VTC curve shifts towards left

→  $I_D$  max at  $V_m$

→ Increase in  $K_R > 1$ ,  $V_{Th}$  decreases less than  $\frac{V_{DD}}{2}$

→ Decrease in  $K_R < 1$ ,  $V_{Th}$  increases more than  $\frac{V_{DD}}{2}$

Q.  $V_{DD} = 3V$      $V_{T_{on}} = 0.7V$      $V_{Top} = -0.7V$

$K_R = 1, 4, 0.25$ .  $V_{Th} = ?$

$$A. K_R = 1, \quad V_{Th} = \frac{0.7 + \sqrt{\frac{1}{1}(3-0.7)}}{1 + \sqrt{\frac{1}{1}}} = 1.5$$

$$K_R = 4, \quad V_{Th} = \frac{0.7 + \sqrt{\frac{1}{4}(3-0.7)}}{1 + \sqrt{\frac{1}{4}}} = 1.23V$$

$$K_R = 0.25, \quad V_{Th} = \frac{0.7 + \sqrt{\frac{1}{0.25}(3-0.7)}}{1 + \sqrt{\frac{1}{0.25}}} = 1.77V$$

Q. Consider a CMOS inverter circuit with following parameters:

$V_{DD} = 3.3V$ ,  $V_{T_{on}} = 0.6V$ ,  $V_{Top} = -0.7V$ ,  $K_n = 200\mu A/V^2$ ,  $K_p = 80\mu A/V^2$ . Calculate Noise Margins

A.  $V_{OH} = V_{DD} = 3.3V$ ;  $V_{OL} = 0V$

$$V_{IL} = \frac{(2V_{out} + V_{Top} - V_{DD}) + K_R V_{Thn}}{1 + K_R} = \frac{(2V_{out} - 0.7 - 3.3) + 0.6 \left(\frac{200}{80}\right)}{1 + \frac{200}{80}} = \frac{2V_{out} - 2.5}{3.5}$$

at  $V_{in} = V_{IL}$ ,  $I_{Dn}(\text{sat}) = I_{Dp}(V_{in})$

$$\frac{K_n(V_{in} - V_{T_{on}})^2}{2} = \frac{K_p[2(V_{in} - V_{DD} - V_{Top})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]}{2}$$

$$2.5 \left( \frac{2V_{out} - 2.5}{3.5} - 0.6 \right)^2 = \left[ 2 \left( \frac{2V_{out} - 2.5}{3.5} - 3.3 + 0.7 \right) (V_{out} - 3.3) - (V_{out} - 3.3)^2 \right] \Rightarrow 0.672 V_{out}^2 + 0.03 V_{out} - 6.66 = 0$$

By solving quadratic eqn,  $V_{out} = 3.14$  or  $-3.14$

$$V_{IL} = \frac{2V_{out}}{3.5} - \frac{2.5}{3.5} = 1.08V$$

$$V_{IH} = \frac{K_p(2V_{out} + V_{T_{on}}) + V_{DD} + V_{Top}}{1 + K_R} = \frac{2.5(2V_{out} + 0.6) + 3.3 - 0.7}{1 + 2.5} = 1.42V_{out} + 1.17V$$

At  $V_{IH}$ ,  $I_{Dn}(V_{in}) = I_{Dp}(\text{sat})$

$$K_n [2(V_{in} - V_{T_{on}}) V_{out} - V_{out}^2] = K_p [V_{in} - V_{DD} - V_{Top}]^2$$

$$2.5 [2(1.42V_{out} + 1.17 - 0.6) V_{out} - V_{out}^2] = (1.42V_{out} + 1.17 - 3.3 + 0.7)^2$$

$$2.59 V_{out}^2 + 6.91 V_{out} - 2.044 = 0$$

$$V_{out} = 0.268 \text{ or } -3.14$$

$$V_{in} = 1.42(0.268) + 1.17 = 1.55V$$

$$NM_L = V_{IL} - V_{OL} = 1.08 - 0 = 1.08V$$

$$NM_H = V_{OH} - V_{in} = 3.3 - 1.55 = 1.75V$$

$K_R > 1 \Rightarrow$  Not symmetric,  $\frac{V_{DD}}{2} > V_{Th}$ , which is true ( $1.65 > 1.37$ )

Q. Consider CMOS inverter

$$nMOS \rightarrow V_{T_{on}} = 0.6V \quad M_n C_{ox} = 60 \mu A/V^2$$

$$pMOS \rightarrow V_{T_{off}} = -0.7V \quad M_p C_{ox} = 25 \mu A/V^2$$

$$(W/L)_n = 8$$

$$(W/L)_p = 12$$

Calculate Noise margin & Switching Threshold.

$$V_{DD} = 3.3V$$

$$A. K_T = \frac{60 \times 8}{25 \times 12} = 1.6$$

$$V_{OL} = 0V, \quad V_{OH} = 3.3V$$

$$V_{IL} = \frac{(2V_{out} + V_{top} - V_{DD}) + K_T V_{T_{on}}}{1 + K_T} = \frac{(2V_{out} - 0.7 - 3.3) + (1.6 \times 0.6)}{1 + 1.6} = \frac{(2V_{out} - 3.04)}{2.6}$$

$$V_{in} = V_{IL} \Rightarrow I_{Dn}(\text{sat}) = I_{Dp}(\text{lin})$$

$$\frac{K_n}{K_p} (V_{in} - V_{T_{on}}) = \frac{K_p}{K_n} \left[ 2(V_{in} - V_{DD} - V_{top})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2 \right]$$

$$1.6 \left( \frac{2V_{out} - 3.04}{2.6} \right) = \left[ 2 \left( \frac{2V_{out} - 3.04}{2.6} - 3.3 + 0.7 \right) (V_{out} - 3.3) - (V_{out} - 3.3)^2 \right]$$

$$0.54 V_{out}^2 - 7.25 V_{out} + 15.66 = 0$$

$$V_{out} = 1.92 \text{ or } 2.7$$

$$V_{IL} = \frac{2(2.7) - 3.04}{2.6} = 0.907$$

$$V_{IH} = \frac{K_T (2V_{out} + V_{top}) + V_{DD} + V_{top}}{1 + K_T} = \frac{1.6 (2V_{out} + 0.6) + 3.3 - 0.7}{1 + 1.6} = \frac{3.2V_{out} + 3.56}{2.6} = 1.23V_{out} + 1.37$$

$$At \quad V_{IH}, \quad I_{Dn}(\text{lin}) = I_{Dp}(\text{sat})$$

$$K_n [2(V_{in} - V_{T_{on}}) V_{out} - V_{out}^2] = K_p [V_{in} - V_{DD} - V_{top}]^2$$

$$1.6 [2(1.23V_{out} + 1.37 - 0.6)V_{out} - V_{out}^2] = [1.23V_{out} - 1.37 - 3.3 + 0.7]^2$$

$$0.54V_{out}^2 - 6.16V_{out} - 1 = 0$$

$$V_{out} = 0.16 \text{ or } -1.48$$

$$V_{IH} = 1.23V_{out} + 1.37 = 1.57V$$

$$V_{TH} = \frac{V_{T_{on}} + \sqrt{\frac{1}{K_T} (V_{DD} + V_{top})}}{1 + \sqrt{\frac{1}{K_T}}} = \frac{0.6 + \sqrt{\frac{1}{1.6} (3.3 - 0.7)}}{1 + \sqrt{\frac{1}{1.6}}} = 1.48V$$

$$NM_L = V_{IL} - V_{OL} = 0.907V$$

$$NM_H = V_{OH} - V_{IH} = 1.73V$$

Q. Design resistive-load inverter with  $R = 1k\Omega$ ,  $V_{OL} = 0.6V$ ,  $V_{DD} = 5V$ ,  $Y = 0.2V^{-1/2}$ ,  $M_n C_{ox} = 22 \mu A/V^2$

$$V_{T_0} = 1V, \lambda = 0. Find \quad a) W_L \quad b) V_{IL} \& V_{IH} \quad c) NM_L \& NM_H$$

$$A. a) I_R = I_{Dn}(\text{lin}) \Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{1}{2} M_n C_{ox} \frac{W}{L} [2(V_{in} - V_{T_0}) V_{out} - V_{out}^2] \Rightarrow 400 = \frac{W}{L} [2(5-1)(0.6) - (0.6)^2] \Rightarrow \frac{W}{L} = 90.1$$

$$b) V_{IL} = 1 + \frac{1}{1000 \times 1.98} = 1.5V, \quad V_{IH} = 3.09V \quad \left( V_{IH} = V_{T_0} + \frac{\sqrt{8V_{DD}}}{\sqrt{3} k_n R_L} - \frac{1}{k_n R_L} \right) \left( V_{IL} = V_{T_0} + \frac{1}{k_n R_L} \right)$$

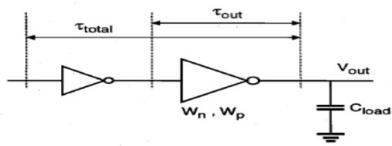
$$c) NM_L = 1.5 - 0.6 = 0.9V ; NM_H = 5 - 3.09 = 1.92V$$

$$P_{DC} = \frac{V_{DD} I_{DC}}{5 \times 4.4mV} \quad (I_{DC} = \frac{5 - 0.6}{1000} = 4.4mA)$$

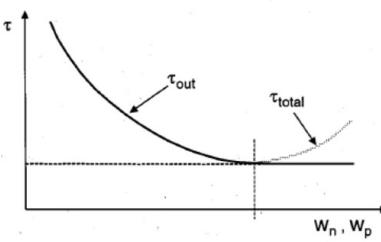
$$= 22mW$$

### BiCMOS Circuit

- Signal propagation delay due to large interconnected capacitances is major factor that limits the performance of CMOS digital integrated circuits
- System speed is restricted by current - driving capacity of CMOS gates



2nd inverter is larger to increase the I to increase performance



### Major Drawback of CMOS inverter

- Low Driving capability for large capacitance loads
- For driving large capacitive loads if scaled buffer chain is used, then larger amounts of Si required

### Advantages of CMOS inverter

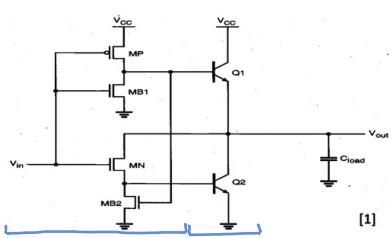
- Low static power dissipation
- Bidirectional Capability (Source & Drain interchangeable)
- Full swing output ( $V_{on} = V_{DD}$  &  $V_{off} = 0V$ )

**BJTs:** Have large driving capability but have more power dissipation

**MOS:** Have low power dissipation

**BiCMOS:** Use driving capability of BJT and low power dissipation of MOS to drive large capacitive load

### BiCMOS Inverter (with resistive base pull-down)

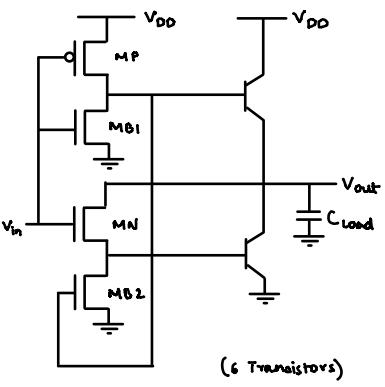


Totem Pole Configuration

MP - ON - Charges

MN - ON - Capacitor Discharges

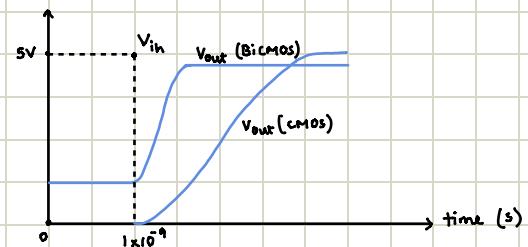
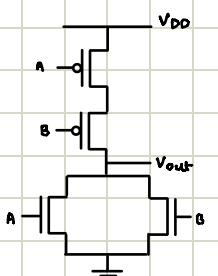
- For small base current, switch is closed. Large current flows
- The complementary pMOS & nMOS transistor  $M_p$  &  $M_n$  supply base currents to BJT & thus act as trigger devices for bipolar output stage
- $Q_1$  can efficiently pull up output voltage in presence of large output capacitance
- $Q_2$  pulls down output voltage
- Depending on  $V_{in}$ , either  $M_n$  or  $M_p$  can be ON in steady state, ensuring push pull operation for BJT
- Resistors are used to remove the base charge of BJT when they are in cut-off mode



BiCMOS inverter with active base pull-down

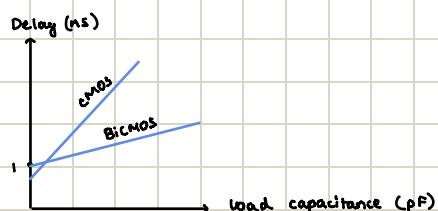
- Easy to fabricate nMOS than resistor
- The superiority of BiCMOS lies in the high current drive capability of BJT output.
- 0 static power dissipation, high input impedance provided by MOS
- To reduce the turn off times of BJT during switching & minimum sized NMOS are added to provide the necessary base discharge path instead of resistor

→ 2 Input NOR gate CMOS

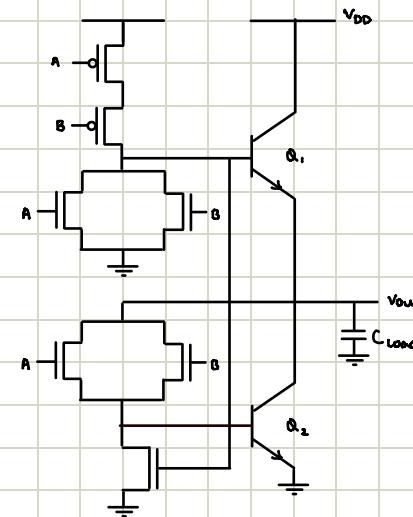


Simulated output voltage waveform of CMOS & BiCMOS for 5pF  
Both the circuits occupy approximately same amount of Si area

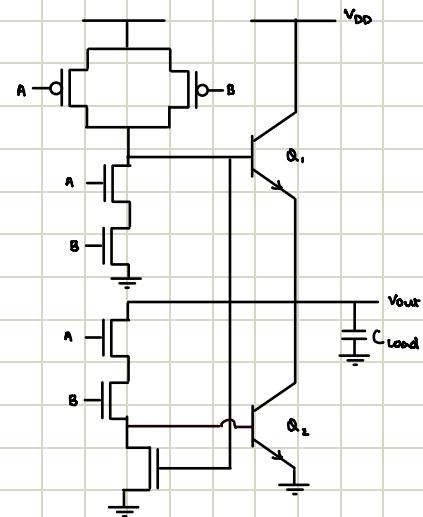
VTC curve of BiCMOS inverter



Q. 2 Input BiCMOS NOR gate



Q. 2 Input BiCMOS NAND gate

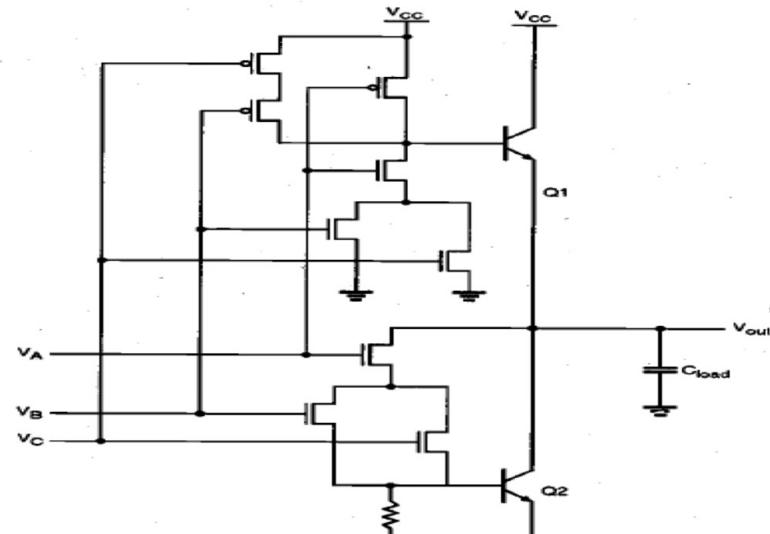


→ In BiCMOS circuit when pull-up PMOS devices are ON, it charges capacitor to  $V_{DD}$  ( $V_{out}$  is charged to  $V_{DD}$ ), meanwhile base charge of  $Q_2$  has to be removed by  $M_{B2}$  NMOS

→ When pull-down NMOS are ON, it discharges load capacitance to 0 by turning  $Q_2$ . Meanwhile base charge of  $Q_1$  will be discharged through NMOS transistors

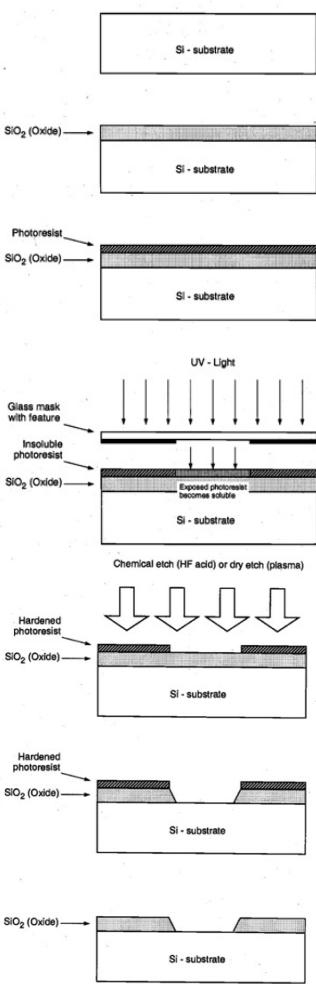
Q.  $y = [(B+C) \cdot A]'$

A.



# Unit -2

Process steps required for patterning of Silicon Dioxide



## Introduction

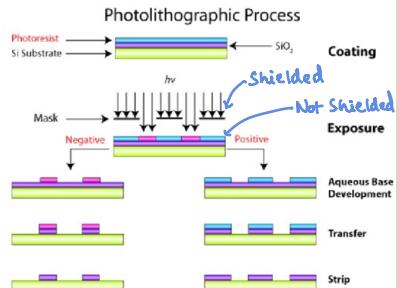
- We discuss here about CMOS fabrication which requires NMOS & PMOS transistors be built on same chip substrate.
- To accomodate nMOS & pMOS devices, special regions called wells are used for which semiconductor type is opposite to substrate type  
(n-well created in p-type substrate)  
(P-well created in n-type substrate)

## Fabrication Process Flow

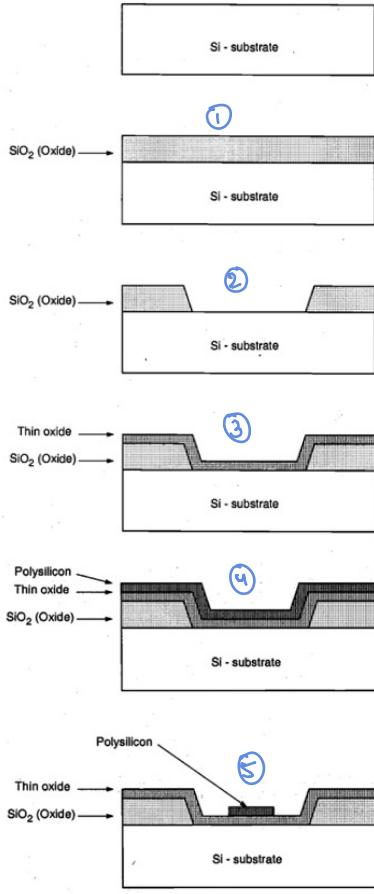
- Fabrication is a process of creating an IC by sequence of photo-lithographic and chemical processing steps

## Patterning

- IC may be viewed as a set of patterned layers of doped silicon, polysilicon, metal & insulating  $\text{SiO}_2$ .
- A layer must be patterned before next layer of material is applied on the chip and the process of transferring a pattern to a layer on the chip is called lithography
- Each layer has its own requirements and lithographic process is repeated for every step using different mask
- The entire oxide surface is covered with a light-sensitive, acid-resistant organic polymer, initially insoluble which is called photoresist. They become soluble upon exposure to UV light
- To selectively expose the photoresist, we have to cover some of the areas on the surface with a mask during exposure
- There are 2 types of photorests :
  - Positive Photoresist - Initially insoluble, soluble upon exposure to UV light
  - Negative Photoresist - Initially soluble, insoluble upon exposure to UV light  
(Negative photorests are more sensitive to light but photolithographic resolution is not as high as that of positive photorests)



### Fabrication of nMOS Transistor



- Step 1: Process starts with oxidation of Silicon substrate on which relatively thick  $\text{SiO}_2$  layer (Field Oxide) is created on surface
- Step 2: Field Oxide is selectively etched to expose Silicon surface on which MOS transistor will be created
- Step 3: Surface is covered with thin, high quality oxide layer, which eventually form gate oxide of MOS transistor
- Step 4: On top of this, layer of polysilicon is deposited. (Undoped polysilicon has high resistivity which can be reduced by doping with impurity atoms)
- Step 5: Polysilicon layer is patterned & etched to form interconnects & MOS Transistor gates
- Step 6: The thin gate which is exposed also gets etched, exposing bare silicon surface on which Source & Drain junctions are formed
- Step 7: Entire Silicon surface is doped with high concentration impurities, by diffusion or ion implantation (Donor atoms produce n-type doping)
- Step 8: Doping penetrates exposed areas, creating 2 n-type regions in p-type substrate which is again covered with an insulating layer of  $\text{SiO}_2$
- Step 9: Insulating oxide layer is patterned in order to provide contact windows for drain & source junctions
- Step 10: Surface is covered with evaporated aluminium which will form interconnects
- Step 11: Finally, metal layer is patterned & etched completing interconnection of MOS

### Device Isolation Techniques

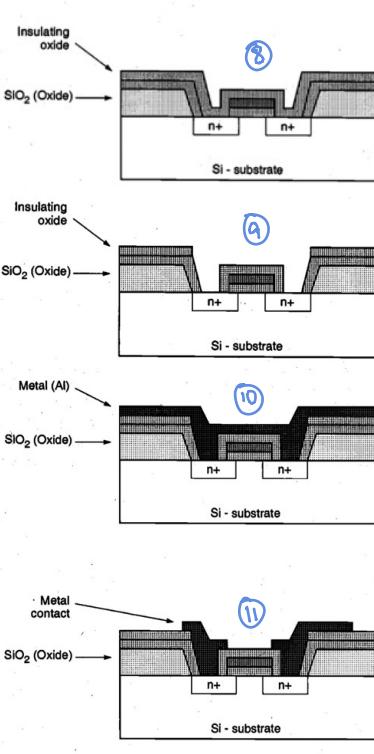
- MOS Transistors consisting an IC must be electrically isolated from each other during fabrication to prevent unwanted conduction path between devices, avoiding creation of inversion layers outside channel region of transistors on a chip surface (called active area)
- For NMOS Fabrication,
  - Silicon wafer → 75 to 150 mm. in diameter & 0.4mm thick
  - Impurity concentrations →  $10^{15} \text{ cm}^{-3}$  (P-type impurities : Boron)
  - Resistivity → 2-25  $\Omega\text{cm}$

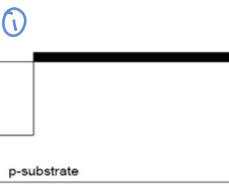
### Diffusion Implantation (Implantation of impurities to change resistivity)

- In high temperature, dopant atoms move from high conc. to low conc. region
- Disadvantage: sideways diffusion is difficult because small geometric

### Ion Implantation

- Dopant atoms implanted vertically into surface of silicon by high energy ion beam (ev), leading to less lateral diffusion





### Fabrication of n-Well CMOS

- Step 1: Moderately doped p-type substrate is prepared and lithographic mask is used to define N-well region which is formed by diffusion (or) ion implantation
- Step 2: Active regions for NMOS & PMOS are defined using another lithographic mask which are used to determine where transistors will be built
- Step 3: A thin  $\text{SiO}_2$  layer is grown on wafer's surface which insulates gate & polysilicon layer is patterned using photolithography to form gate electrodes
- Step 4: n-diffusions created in P-substrate for NMOS  
p-diffusions created in N-well for PMOS
- Step 5: Contact cuts are made to access diffusion regions & polysilicon layers
- Step 6: Thin Aluminium layer is deposited & patterned to form interconnections
- Step 7: Passivation layer is added for protection & Bonding pads for external connections

### Layout Design Rules

- Layout design is a schematic of the IC which describes the actual placement of devices / components on IC for fabrication
- Layout design rules are the constraints to be followed to manufacture the physical mask layout of any circuit
- The rules are:
  - Information of dimensions of layers (metal, diffusion, polysilicon)
  - How closely they can be placed (minimum width & minimum spacing constraints)
- Objective:  
IC should have high overall yield in smallest possible area

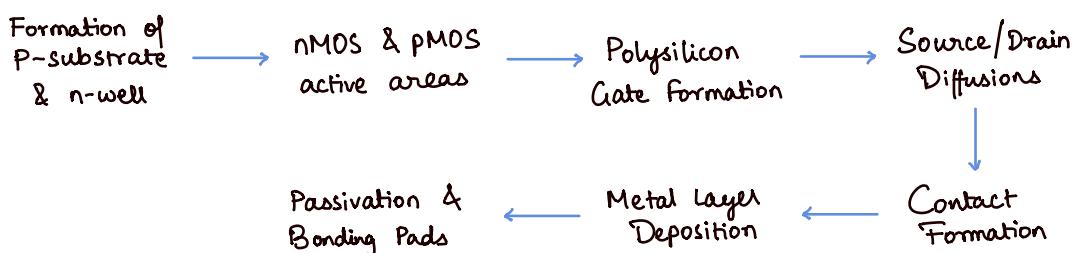
### Manufacturing Problems

- Variation in  $V_m$ : Variation in ion-implantation & poly-layer
- Diffusion, Poly, Metal: Variation in doping leading to variation in R & C
- Shorts (2 lines placed too close) & Opens (Too small metal line may break)
- Via/contact cuts problems: Consists of minimum-width & minimum spacing constraints & requirements b/w objects on same/ different layers
- Design rules are described in 2 ways:
  - i) Micron rules: Constraints are stated in terms of absolute dimensions in  $\mu\text{m}$
  - ii) Lambda rules: Constraints are stated in terms of single parameter ( $\lambda$ )

### Lambda Rules

- $\lambda$  is half of min. channel length ( $L = 2\lambda$ )
- Industry layout design rules are generally in  $\mu\text{m}$
- All widths, spacing & distance are written in terms of  $m\lambda$  form ( $m$ : multiplier)
- Change in  $\lambda$  can produce new mask

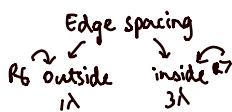
### Summary of CMOS Fabrication



## Summary

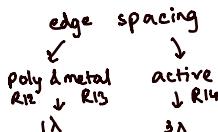
$$AA \Rightarrow 1, 2 \Rightarrow 3\lambda$$

$$P.S \Rightarrow 3-7 \Rightarrow \text{Mostly } 2\lambda$$

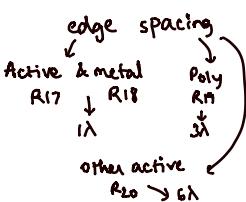


$$\text{Metal} \Rightarrow 8, 9 \Rightarrow 3\lambda$$

$$P.C \Rightarrow 10-14 \Rightarrow \text{Mostly } 2\lambda$$



$$A.C \Rightarrow 15-20 \Rightarrow \text{Mostly } 2\lambda$$



## Active area rules

### Rule No

### Description

### $\lambda$ -Rule

R 1 Min. active area width

$3\lambda$

R 2 Min. active area spacing

$3\lambda$

## Polysilicon rules

R 3 Min. poly width

$2\lambda$

R 4 Min. poly spacing

$2\lambda$

R 5 Min. gate extension of poly over active

$2\lambda$

R 6 Min. poly-active edge spacing (poly outside active area)

$1\lambda$

R 7 Min. poly-active edge spacing (poly inside active area)

$3\lambda$

## Metal Rules

R 8 Min. metal width

$3\lambda$

R 9 Min. metal spacing

$3\lambda$

## Metal 1 to polysilicon or to diffusion

- $2 \times 2 \lambda$  contact cut indicates an area in which oxide is to be removed down to the underlying polysilicon or diffusion surface
- Deposition of metal layer takes place the metal is deposited through contact cut areas onto underlying area so that contact is made between the layers

## Polycontact Rules

### Rule No

### Description

### $\lambda$ -Rule

R 10 Poly contact size

$2\lambda$

R 11 Minimum poly contact spacing

$2\lambda$

R 12 Minimum poly contact to poly edge spacing

$1\lambda$

R 13 Minimum poly contact to metal edge spacing

$1\lambda$

R 14 Minimum poly contact to active edge spacing

$3\lambda$

## Active contact Rules

### Rule No

### Description

### $\lambda$ -Rule

R 15 Active contact size

$2\lambda$

R 16 Min. active contact spacing (on same active region)

$2\lambda$

R 17 Min. active contact to active edge spacing

$1\lambda$

R 18 Min. active contact to metal edge spacing

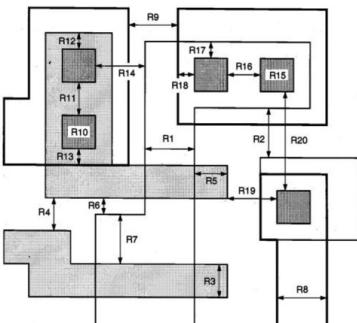
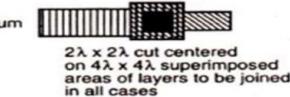
$1\lambda$

R 19 Min. active contact to poly edge spacing

$3\lambda$

R 20 Min. active contact spacing (on diff. active region)

$6\lambda$



Minimum Width

Thionix

n-diffusion

p-diffusion

3λ



3λ



2λ



2λ



Min. separal  
(where specified)

$3\lambda^*$

$1\lambda$

$2\lambda$

Polysilicon



$3\lambda^*$



$3\lambda^*$

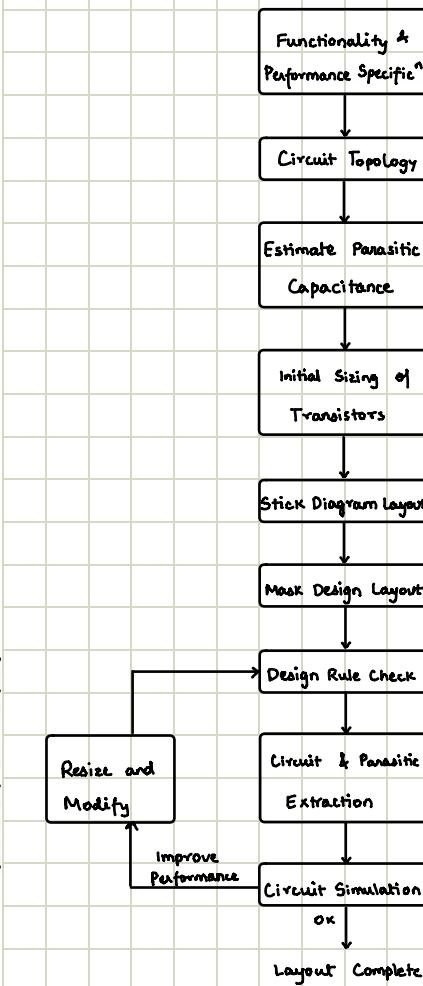
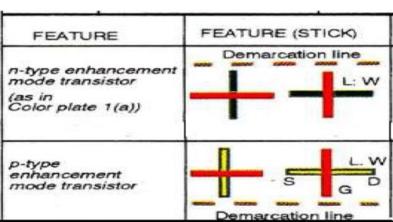


$4\lambda$



$4\lambda$

## Design Flow for production of a physical mask layout



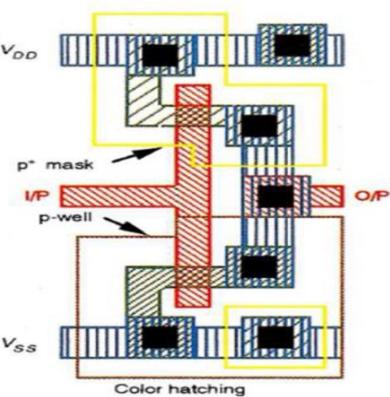
### Rules

- N/P diffusions should not cross the demarcation lines
- N & P diffusions are interconnected through metal
- Polysilicon & metal can cross the demarcation lines
- Crosses on V<sub>DD</sub>/Gnd power supply rails indicate Substrate/p-well connections
- Diffusion paths are run parallel to V<sub>DD</sub> & Ground

### Additional Rules

R25	Minimum Active Overlap over contact	1.5λ
R26	Minimum Metal1 Overlap over contact	1λ
R27	Minimum Poly Overlap over contact	1.5λ
R28	Minimum spacing to gate	1λ

## CMOS Inverter Layout



Via Rules (Via connects 2 metals)

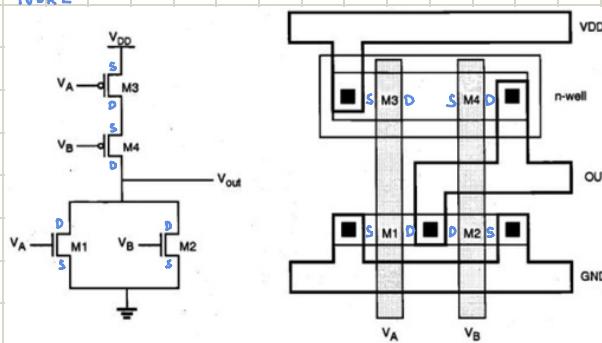
R29	Exact Size	2h
R30	Minimum Spacing	3h
R31	Minimum Overlap by Metal 2	1h
R32	Minimum Spacing to contact	2h
R33	Minimum Spacing to poly or active edge	2h

### Generic Combination Logic Circuit

- OR operations performed by parallel-connected drivers
- AND operations performed by series-connected drivers
- Inversion is provided by nature of MOS Circuit
- Each input variable is assigned to only 1 driver

### Complex Logic Circuits

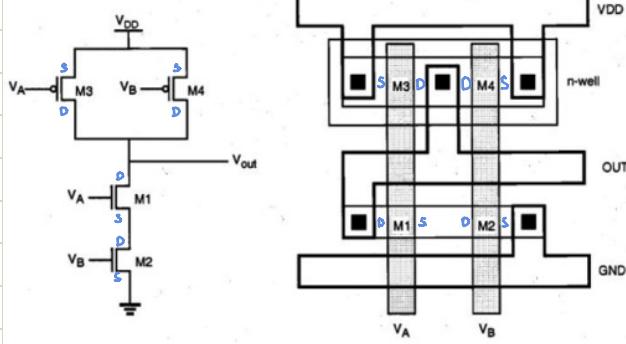
→ NOR2



Layout Diagram

Stick Diagram

→ NAND2



Layout Diagram

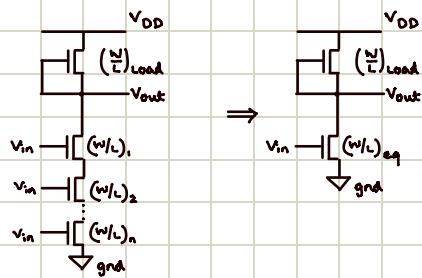
Stick Diagram

(+) operation  
PMOS - Parallel  
NMOS - Series

(+) Operation  
PMOS - Series  
NMOS - Parallel

### Generalized Structure & inverter equivalent

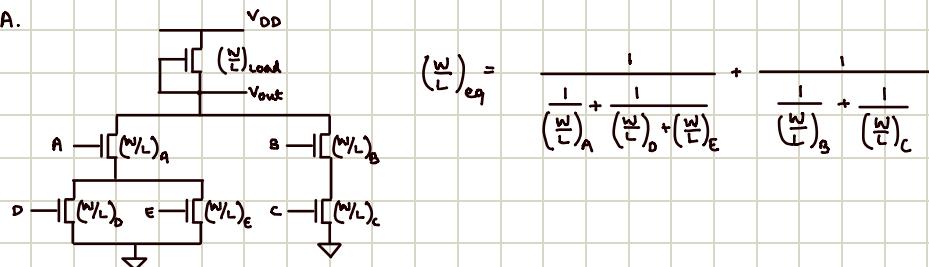
→ If we take a NAND Structure



$$I_D = \frac{MnC_{ox}}{2} \left( \frac{1}{\frac{\kappa(m)}{(W/L)_A}} + \frac{1}{\frac{\kappa(m)}{(W/L)_B}} + \dots + \frac{1}{\frac{\kappa(m)}{(W/L)_n}} \right), \begin{cases} [2(V_{in} - V_{T_0})V_{out} - V_{out}] \\ (V_{in} - V_{T_0})^2 \end{cases}, \begin{cases} \text{linear} \\ \text{saturation} \end{cases}$$

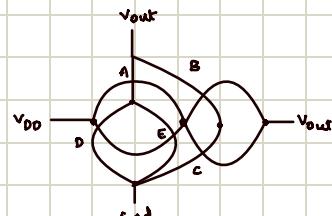
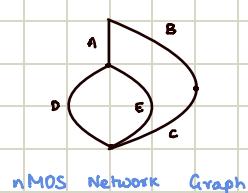
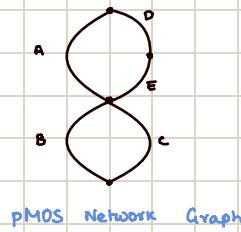
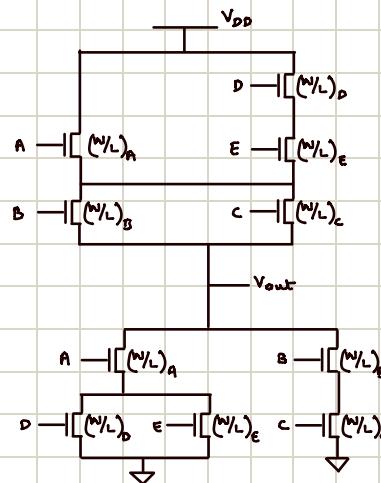
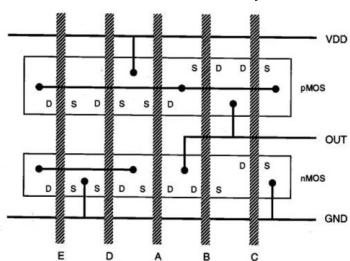
Q.  $Z = \overline{A(D+E)} + BC$

A.

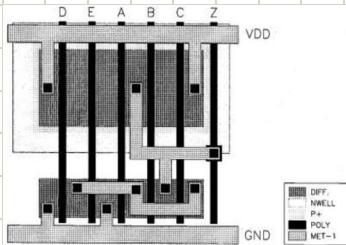


### Euler Path for Graph

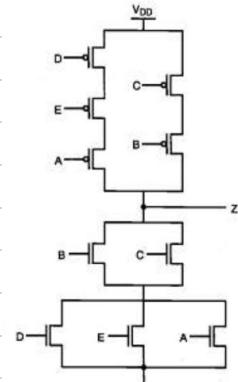
#### Optimized Stick Diagram



Q. Simplified layout of CMOS complex logic circuit is given. Draw corresponding circuit diagram & find equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming  $(\frac{w}{l})_p = 15$  &  $(\frac{w}{l})_n = 10$



A.

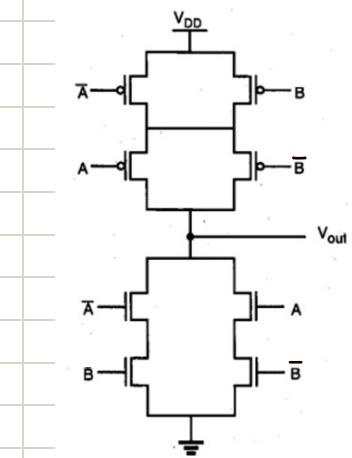


$$Z = \overline{(D+E+A)(B+C)}$$

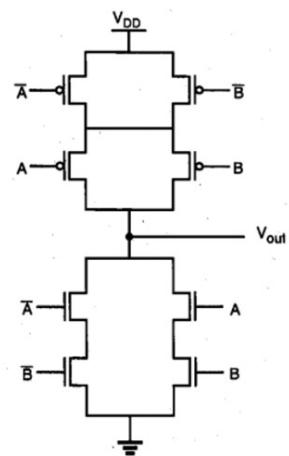
$$\begin{aligned} (\frac{w}{l})_{p,eq} &= \frac{1}{(\frac{w}{l})_D + (\frac{w}{l})_E + (\frac{w}{l})_A} + \frac{1}{(\frac{w}{l})_B + (\frac{w}{l})_C} \\ &= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 5 + 7.5 = 12.5 \\ (\frac{w}{l})_{n,eq} &= \frac{1}{(\frac{w}{l})_B + (\frac{w}{l})_C} + \frac{1}{(\frac{w}{l})_D + (\frac{w}{l})_E + (\frac{w}{l})_A} \\ &= \frac{1}{\frac{1}{10} + \frac{1}{10}} + \frac{1}{\frac{1}{10} + \frac{1}{10} + \frac{1}{10}} = \frac{600}{50} = 12 \end{aligned}$$

### CMOS XOR & XNOR

$$A \text{ XOR } B = \overline{AB} + AB$$



$$A \text{ XNOR } B = \overline{AB} + AB$$



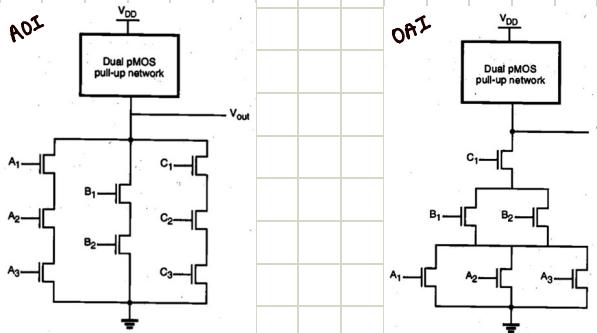
### AOI and OAI Gates

→ There are no strict limitations on topology of PUN & PDN but we have

2 types of gates :

i) AOI (AND-OR-INVERT)  $\Rightarrow$  Sum of products

ii) OAI (OR-AND-INVERT)  $\Rightarrow$  Product of sums

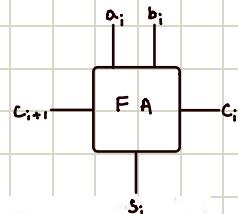


### Pseudo NMOS Gates

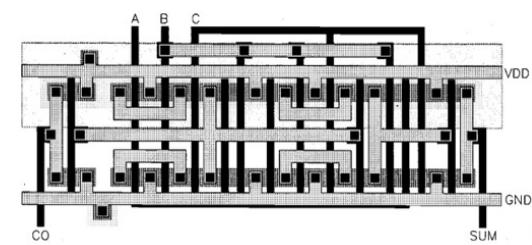
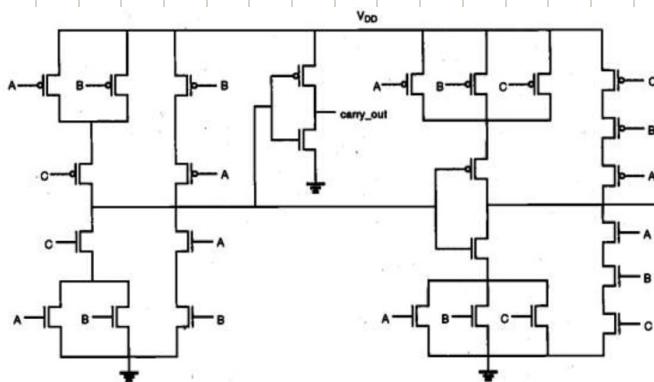
- A possible alternative to reduce number of transistors is to use single PMOS with gate connected to ground as load device
- This provides a simple pull-up arrangement, complex gate is implemented with fewer transistors
- Disadvantage: Non-zero static power dissipation because of the always-ON PMOS load, which affects V<sub>OL</sub> & noise margins based on transconductance ratio

### CMOS Full-Adder

$$\begin{aligned} \text{sum\_out} &= A \oplus B \oplus C \\ &= ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} \\ \text{carry\_out} &= AB + BC + AC \end{aligned}$$



a <sub>i</sub>	b <sub>i</sub>	c <sub>i</sub>	s <sub>i</sub>	c <sub>i+1</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Mask Layout of CMOS FA using min. size transistors

## MOSFET Scaling & Small - Geometry Effects

- Requirement to pack as many MOSFETs as possible in limited space (High Density)
- The reduction of size is termed as scaling, which causes change in operational characteristics
- Physical limitations limits the possibilities achievable by scaling
- Scaling improves density, speed, power
- We have 2 basic types of size-reduction strategies:
  - Full Scaling / Constant-field scaling
  - Constant-Voltage Scaling
- We use a constant called Scaling factor 's' ( $s > 1$ ) to describe scaling

### Constant - Field Scaling

- Preserves magnitude of internal electric fields

#### i) Oxide Capacitance

$$C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}'} = s \cdot \frac{\epsilon_{ox}}{t_{ox}} = s C_{ox}$$

#### ii) Drain Current

$$\begin{aligned} I_D' (\text{linear}) &= \frac{1}{2} \mu_n C_{ox}' \frac{W}{L} \left( 2(V_{GS}' - V_T') V_{DS}' - V_{DS}'^2 \right) \\ &= \frac{1}{2} \mu_n s C_{ox} \frac{W}{L} \frac{s}{s} \left( 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right) \cdot \frac{1}{s^2} = \frac{I_D}{s} (\text{linear}) \end{aligned}$$

$$\text{Similarly } I_D' (\text{saturation}) = \frac{I_D}{s} (\text{saturation})$$

#### iii) Power Dissipation

$$P' = I_D' \cdot V_{DS} = \frac{1}{s^2} \cdot I_D V_{DS} = \frac{P}{s^2}$$

#### iv) Power Density

$$P_D' = \frac{P'}{A'} = \frac{P/s^2}{A/s^2} = \frac{P}{A} = P_D \quad (\text{unchanged})$$

### Constant - Voltage Scaling

- Usually preferred over full scaling

Preferred

Quantity	Constant - field Scaling	Constant - Voltage Scaling
1) Dimensions ( $L, W, t_{ox}, z_j$ )	Reduced by $s$	Reduced by $s$
2) Voltages ( $V_{DD}, V_T$ )	Reduced by $s$	Unaffected
3) Doping Densities ( $N_A, N_D$ )	Increased by $s$	Increased by $s^2$
4) Drain Current ( $I_D$ )	Reduced by $s$	Increased by $s$
5) Power Dissipation ( $P$ )	Reduced by $s^2$	Increased by $s$
6) Power Density ( $P_D = P/A$ )	Unaffected	Increased by $s^3$
7) Oxide Capacitance ( $C_{ox}$ )	Increased by $s$	Increased by $s$

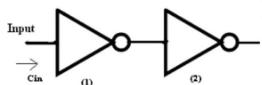
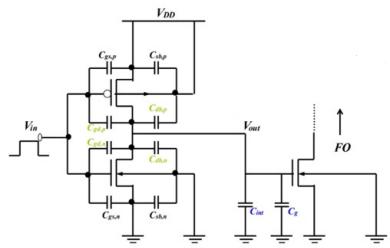
Year	Technology node	Shrink factor
1997	350 nm	$250/350 = 0.7142$
1999	250 nm	$180/250 = 0.72$
2001	180 nm	$130/180 = 0.7222$
2003	130 nm	$90/130 = 0.6923$
2006	90 nm	$65/90 = 0.7222$
2008	65 nm	$45/65 = 0.6923$
2010	45 nm	$32/45 = 0.7111$
2012	32 nm	$22/32 = 0.6875$

### Advantages of Scaling

- More capability
- speed improvement
- Increase in current
- Improved throughput

### Disadvantages of Scaling

- Short channel effects
- Complex process technology
- Parasitic effects dominate transistor effects



### Cascaded CMOS Inverter Stage

→ Consider a cascode connection of 2 CMOS inverters

→ Capacitances

$C_{gd,p}$  &  $C_{gd,n}$  are primarily due to gate overlap with diffusion

$C_{db,p}$  &  $C_{db,n}$  are voltage dependant junction capacitances

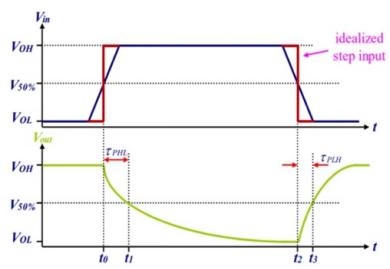
$C_g$  is due to thin-oxide capacitance over gate area

→ pulse waveform is applied to input of first stage inverter  
For the circuit  $C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$

→ Ineffective parasitic capacitances

$C_{sb,n}$  &  $C_{sb,p}$  because source-substrate voltage = 0

$C_{gs,n}$  &  $C_{gs,p}$  because they are connected b/w input node & ground



### Delay Definitions

#### i) Propagation Delay

$\tau_{PHL}$ : Time delay b/w  $V_{50\%}$  transition of rising input to  $V_{50\%}$  of falling output

$\tau_{PLH}$ : Time delay b/w  $V_{50\%}$  transition of falling input to  $V_{50\%}$  of rising output

$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

Avg. Propagation Delay: Avg. time required by input signal to propagate through inverter

$$\tau = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

#### ii) Rise time and Fall time

$\tau_r$ : Time required by output voltage to rise from 10% to 90%

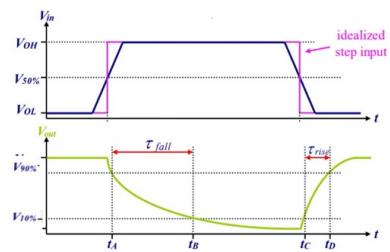
$\tau_f$ : Time required by output voltage to fall from 90% to 10%

$$V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL})$$

$$V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL})$$

$$\tau_r = t_B - t_A$$

$$\tau_f = t_D - t_C$$



## Delay Time Calculations

→ There are 2 methods

i) Average Current Method

ii) Differential Equation Method

→ Average Current Method

→ It is calculated during high-to-low transition of output by taking current values at beginning

$$i_c = C \frac{dv}{dt}$$

$$\tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg, HL}} = \frac{C_{load} (V_{OH} - V_{SOH})}{I_{avg, HL}} \Rightarrow I_{avg, HL} = \frac{1}{2} [i_c (V_{in} = V_{OH}, V_{out} = V_{OH}) + i_c (V_{in} = V_{OL}, V_{out} = V_{SOH})]$$

$$\tau_{PLH} = \frac{C_{load} \cdot \Delta V_{LH}}{I_{avg, LH}} = \frac{C_{load} (V_{SOH} - V_{OL})}{I_{avg, LH}} \Rightarrow I_{avg, LH} = \frac{1}{2} [i_c (V_{in} = V_{OL}, V_{out} = V_{SOH}) + i_c (V_{in} = V_{OL}, V_{out} = V_{OL})]$$

→ Differential Equation Method

→ KCL at Output node,

$$C_{load} \frac{dV_{out}}{dt} = i_c = i_{D,p} - i_{D,n}$$

$$= -i_{D,n} \quad (\text{PMOS OFF}, i_{Dp} = 0)$$

→ Consider NMOS in saturation from  $t_0$  to  $t'$

$$V_{OH} - V_{T,n} < V_{out} \leq V_{OH}$$

$$i_{D,n} = \frac{k_n}{2} (V_{in} - V_{T,n})^2 = \frac{k_n}{2} (V_{OH} - V_{T,n})^2 \quad \rightarrow ①$$

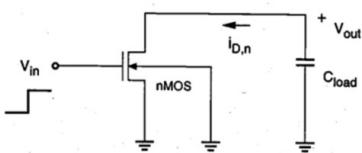
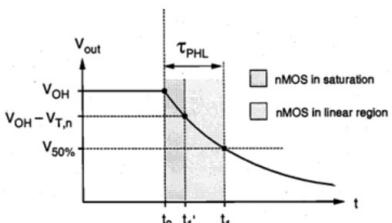
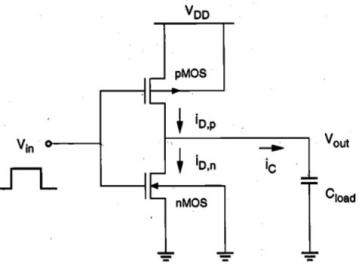
$$-i_{Dn} = C_{load} \frac{dV_{out}}{dt} \quad \rightarrow ②$$

Solving ① & ②,  $\frac{k_n}{2} (V_{OH} - V_{T,n})^2 = -C_{load} \frac{dV_{out}}{dt}$

$$\int_{t=t_0}^{t'=t'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{SOH}} \frac{dV_{out}}{i_{D,n}}$$

$$t'_1 - t_0 = \frac{-2C_{load}}{k_n (V_{OH} - V_{T,n})^2} (V_{OH} - V_{T,n} - V_{SOH})$$

$$t'_1 - t_0 = \frac{2(V_{T,n} C_{load})}{k_n (V_{OH} - V_{T,n})^2}$$



→ Consider NMOS in saturation from  $t_1'$  to  $t_1$

$$\text{in a similar way, } \int_{t=t_1'}^{t_1} dt = -2C_{load} \int_{V_{out}=V_{on}-V_{T,n}}^{V_{50\%}} \left( \frac{1}{K_n (2(V_{on}-V_{T,n})V_{out} - V_{out}^2)} \right) dV_{out}$$

$$t_1 - t_1' = \frac{-2C_{load}}{K_n} \int_{V_{on}-V_{T,n}}^{V_{50\%}} \frac{dV_{out}}{2(V_{on}-V_{T,n})V_{out} - V_{out}^2}$$

$$= -\frac{C_{load}}{K_n} \cdot \frac{1}{(V_{on}-V_{T,n})} \left[ \ln \left( \frac{V_{out}}{2(V_{on}-V_{T,n}) - V_{out}} \right) \right]_{V_{on}-V_{T,n}}^{V_{50\%}}$$

$$= -\frac{C_{load}}{K_n (V_{on}-V_{T,n})} \left[ \ln \left( \frac{V_{50\%}}{2(V_{on}-V_{T,n}) - V_{50\%}} \right) - \ln \left( \frac{V_{on}-V_{T,n}}{2(V_{on}-V_{T,n}) - (V_{on}-V_{T,n})} \right) \right]$$

$$= \frac{C_{load}}{K_n (V_{on}-V_{T,n})} \left[ \ln \left( \frac{2(V_{on}-V_{T,n}) - V_{50\%}}{V_{50\%}} \right) \right]$$

$$= \frac{C_{load}}{K_n (V_{on}-V_{T,n})} \left[ \ln \left( \frac{2V_{on} - 2V_{T,n} - \frac{V_{on}}{2} - \frac{V_{on}}{2}}{\frac{V_{on} + V_{ol}}{2}} \right) \right]$$

$$= \frac{C_{load}}{K_n (V_{on}-V_{T,n})} \left[ \ln \left( \frac{4(V_{on}-V_{T,n})}{V_{on}+V_{ol}} - 1 \right) \right]$$

→ Now,  $t_{PLH} = (t_1' - t_0) + (t_1 - t_1')$

$$= \left[ \frac{2C_{load}V_{T,n}}{K_n(V_{on}-V_{T,n})^2} \right] + \frac{C_{load}}{K_n(V_{on}-V_{T,n})} \left[ \ln \left( \frac{4(V_{on}-V_{T,n})}{V_{on}+V_{T,n}} - 1 \right) \right]$$

$$= \frac{C_{load}}{K_n(V_{on}-V_{T,n})} \left( \frac{2V_{T,n}}{V_{on}-V_{T,n}} + \ln \left( \frac{4(V_{on}-V_{T,n})}{V_{on}+V_{T,n}} - 1 \right) \right)$$

→ We can consider the same way for  $t_{PLH}$ ,

$$t_{PLH} = C_{load} \left[ \int_{V_{out}=V_{ol}}^{V_{DD}-|V_{T,load}|} \frac{dV_{out}}{I_{D,load}(\text{sat})} + \int_{V_{out}=V_{DD}-|V_{T,load}|}^{V_{50\%}} \frac{dV_{out}}{I_{D,load}(\text{linear})} \right]$$

$$= \frac{C_{load}}{K_p(V_{DD}-|V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD}-|V_{T,p}|} + \ln \left( \frac{4(V_{DD}-|V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

→ Actual time delay is calculated by considering Step input as well

$$t_{PLH}(\text{actual}) = \sqrt{t_{PLH}^2 + \left( \frac{t_f}{2} \right)^2}$$

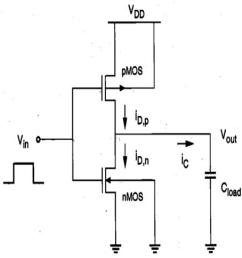
$$t_{PLH}(\text{actual}) = \sqrt{t_{PLH}^2 + \left( \frac{t_r}{2} \right)^2}$$

$t_r$ : rise time

$t_f$ : fall time

Q.

Consider the CMOS inverter circuit shown in Fig. 6.2, with  $V_{DD} = 3.3$  V. The  $I-V$  characteristics of the nMOS transistor are specified as follows: when  $V_{GS} = 3.3$  V, the drain current reaches its saturation level  $I_{d,sat} = 2$  mA for  $V_{DS} \geq 2.5$  V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0 V to 3.3 V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3 V to 1.65 V, assuming an output load capacitance of 300 fF.



$$A. t_{PHL} = t_{PHL}(t_i' \rightarrow t_0) + t_{PHL}(t_1 \rightarrow t_i)$$

$$I_{d,sat} = 2 \text{ mA} \quad \text{for} \quad V_{DS} \geq 2.5 \text{ V}$$

$$V_{GS} - V_{Tn} = 2.5$$

$$V_{Tn} = 3.3 - 2.5 = 0.8 \text{ V}$$

$$I_{d,sat} = \frac{k_n}{2} (V_{on} - V_{Tn})^2 \Rightarrow k_n = \frac{2 \times 2 \times 10^{-3}}{(3.3 - 0.8)^2} = 0.64 \text{ mA/V}^2$$

$$\begin{aligned} t_{PHL} &= t_{PHL}(t_i' \rightarrow t_0) + t_{PHL}(t_1 \rightarrow t_i') = \left( \frac{2 C_{load} \cdot V_{Tn}}{k_n (V_{on} - V_{Tn})^2} \right) \left( \ln \left( \frac{4(V_{on} - V_{Tn})}{(V_{on} + V_{Tn})} - 1 \right) \right) \\ &= \frac{2 \times 300f \times 0.8}{0.64m \times (2.5)^2} + \frac{300f}{0.64m \times (2.5)} \ln \left( \frac{4(2.5)}{3.3} - 1 \right) \\ &= 120p + 132p = 252p \end{aligned}$$

Q. For the CMOS inverter shown in Fig. 6.2 with a power supply voltage of  $V_{DD} = 5$  V, determine the fall time  $\tau_{fall}$ , which is defined as the time elapsed between the time point at which  $V_{out} = V_{90\%} = 4.5$  V and the time point at which  $V_{out} = V_{10\%} = 0.5$  V. Use both the average-current method and the differential equation method for calculating  $\tau_{fall}$ . The output load capacitance is 1 pF. The nMOS transistor parameters are given as

A. Avg-current method,

$$\begin{aligned} I_{avg} &= \frac{1}{2} [I(V_{in}=5, V_{out}=4.5) + I(V_{in}=5, V_{out}=0.5)] \\ &= \frac{1}{2} \left[ \frac{1}{2} k_n (V_{in} - V_{Tn})^2 + \frac{1}{2} k_n (2(V_{in} - V_{Tn})V_{out} - V_{out}^2) \right] \\ &= \frac{1}{2} \times \frac{1}{2} \times 20 \times 10^{-6} \times 10 \left[ (5-1)^2 + (2(5-1)0.5 - 0.5^2) \right] = 0.9875 \text{ mA} \\ \tau_{fall} &= \frac{C \Delta V}{I_{avg}} = \frac{1 \times 10^{-12} (4.5 - 0.5)}{0.9875 \times 10^{-3}} = 4.05 \text{ ns} \end{aligned}$$

Differential equation method,

$$C \frac{dV_{out}}{dt} = -\frac{1}{2} k_n (V_{in} - V_{Tn})^2 \quad (k_n = \mu_n C_{ox} \left( \frac{w}{l} \right)_n)$$

$$\frac{dV_{out}}{dt} = -\frac{20 \times 10^{-6} \times 10 (5-1)^2}{2 \times 1 \times 10^{-12}} = -1.6 \times 10^9 \text{ V/s}$$

$$t_{sat} = \frac{-1}{1.6 \times 10^9} \int_{4.5}^0 dV_{out} = 0.3125 \text{ ns}$$

$$C \frac{dV_{out}}{dt} = -\frac{1}{2} k_n (2(V_{in} - V_{Tn})V_{out} - V_{out}^2) \Rightarrow t_{fall} - t_{sat} = -2C \int_4^{0.5} \frac{dV_{out}}{k_n (2(V_{in} - V_{Tn})V_{out} - V_{out}^2)}$$

$$t_{linear} = \frac{C}{k_n} \cdot \frac{1}{(V_{in} - V_{Tn})} \left( \frac{2(V_{in} - V_{Tn}) - V_{sat}}{V_{sat}} \right)^{0.5} = \frac{10^{-12}}{20 \times 10^{-6} \times 10 \times 4} \left( \ln \left( \frac{8-0.5}{0.5} \right) - \ln \left( \frac{8-4}{4} \right) \right) = 3.385 \text{ ns}$$

$$t_{fall} = t_{linear} + t_{sat} = 3.385 + 0.3125 = 3.6975 \text{ ns}$$

$$\mu_n C_{ox} = 20 \text{ mA/V}^2$$

$$\left( \frac{w}{l} \right)_n = 10$$

$$V_{Tn} = 1 \text{ V}$$

### Symmetric CMOS Inverter

→ We know,

$$V_{TH} = \frac{V_{T_{ON}} + \sqrt{\frac{1}{K_R} (V_{DD} + V_{T_{OFF}})}}{1 + \sqrt{\frac{1}{K_R}}}$$

$$\sqrt{\frac{1}{K_R}} = \frac{V_{TH} - V_{T_{ON}}}{V_{DD} + V_{T_{OFF}} - V_{TH}}$$

$$K_R = \left( \frac{K_n}{K_p} \right) = \left( \frac{V_{DD} + V_{T_{OFF}} - V_{TH}}{V_{TH} - V_{T_{ON}}} \right)^2$$

$$\left( \frac{K_n}{K_p} \right)_{ideal} = \left( \frac{0.5V_{DD} + V_{T_{OFF}}}{0.5V_{DD} - V_{T_{ON}}} \right)^2 \quad (V_{TH,ideal} = 0.5V_{DD})$$

$$\text{For Symmetric CMOS, } \left( \frac{K_n}{K_p} \right) = 1 \quad (|V_{T_{OFF}}| = V_{T_{ON}} = V_T)$$

$$\rightarrow V_{IL} = \frac{3V_{DD} + 2V_{T_{ON}}}{8} \quad (V_{IL} = \frac{2V_{out} + V_{T_{OFF}} - V_{DD} + K_R V_{T_{ON}}}{1 + K_R})$$

$$V_{IM} = \frac{5V_{DD} - 2V_{T_{ON}}}{8}$$

$$V_{IL} + V_{IM} = V_{DD}$$

### Ring Oscillator

can be any odd no.

- The cascade connection of 3 identical CMOS inverters and output node of 3rd inverter is connected to input node of first forming a feedback loop
- The circuit oscillates once any input or output voltage deviates from unstable operating point  $V_{TH}$
- 3 Stage oscillation period  $T$

$$T = T_{PHL_1} + T_{PLH_1} + T_{PHL_2} + T_{PLH_2} + T_{PHL_3} + T_{PLH_3}$$

$$= 2T_p + 2T_p + 2T_p = 6T_p$$

$$f = \frac{1}{2nT_p}$$

- Ring oscillator can be used as very simple pulse generator  
Output waveform is utilized as simple master CLOCK signal generated on chip

