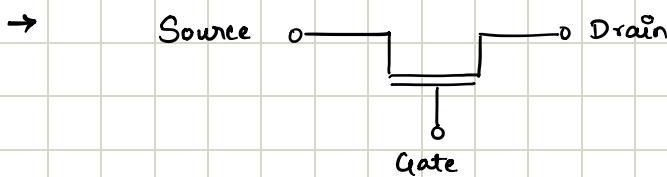


— ACD — Unit - 1 —

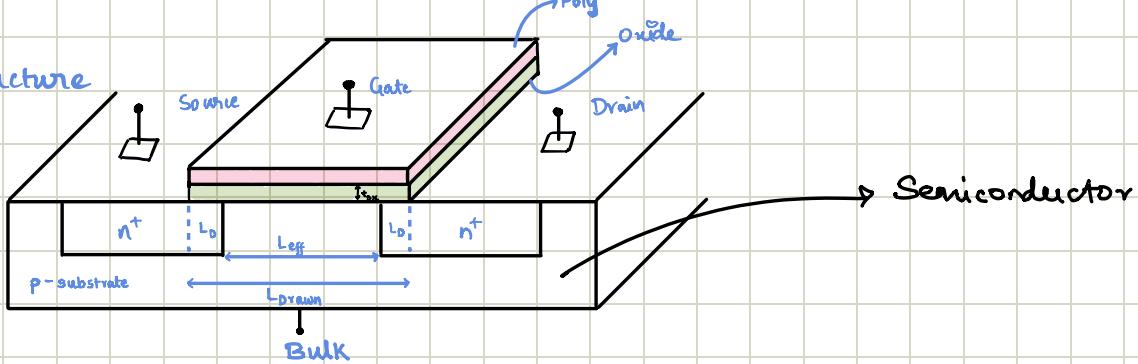
MOSFET - Metal Oxide Semiconductor Field effect Transistor



→ Because of symmetry, Source & Drain are interchangeable

→ When V_g is high, MOS acts as short circuit connecting Source & Drain
When V_g is low, MOS isolates Source & Drain

MOSFET Structure



→ Has 4 Terminals : B, S, G, D

$$L_{eff} = L_{drawn} - 2L_d$$

↳ usually 10 nm

$$t_{ox} = 15 \text{ Å} \quad (\text{less thickness, more capacitance}) \quad (Q = CV)$$

Since MOSFET is symmetric, battery is connected such that higher potential is connected to drain while lower to source

→ Source is the terminal providing charge carriers (e^- for NMOS)
Drain collects them

→ Source-Drain diodes must be reverse biased

→ Threshold voltage

→ For NFET, The gate voltage for which interface is as much n-type as substrate is p-type

→ It is adjusted by implantation of dopants into channel area during device fabrication

$$V_{Th} = \Phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}} \rightarrow \text{Charge in depletion region}$$

Work function difference
b/w polysilicon gate &
Silicon substrate

Fermi-potential

$$\Phi_F = \frac{kT}{q} \ln \frac{N_{sub}}{n_i}$$

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

$$= \sqrt{4Q\epsilon_s N_{sub} 10^{-12}}$$

Electrical Permittivity of Si

$$= 1.05 \times 10^{-12} \text{ F/m}$$

Gate-Oxide
Capacitance per unit area

$$= 1.5 \times 10^{-9} \text{ C/m}^2$$

Work function difference
b/w polysilicon gate &
Silicon substrate

MOSFET Operation

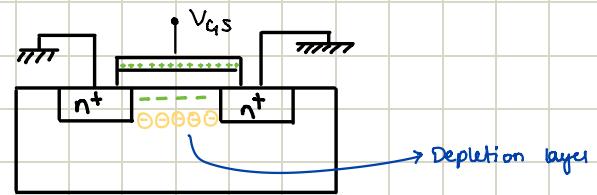
Case	V_{GS}	V_{DS}	Remarks
1	0	0	MOS is in OFF State
2	+ve	0	Positive holes get repelled & enter deep inside body leaving ions at that region & creating depletion layer MOS is still OFF
3	$\geq V_{TH}$	0	e^- from n^+ /source move to region A and e^- from p-substrate try to jump depletion layer MOS is turned ON
			$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$
4	$\geq V_{TH}$	+ve	I_D exists and flows from drain to source
5	$\geq V_{TH}$	More +ve	Assume the channel of e^- as a resistor If we measure potential at different points on channel, we get different values
			This causes tapering effect because channel isn't uniform, causing channel to close up right before drain causing pinch-off effect
			At this region, Q tends to 0, and we know $V_D = \frac{I}{Q}$, So drift velocity is large enough to penetrate through & finally reaching drain
			As V_{DS} keeps increasing, pinch off point moves towards source, creating a short circuit, also known as punch-off effect

I/V Characteristics Derivation

→ Case 1: When $V_{GS} \geq V_{TH}$ & $V_{DS} = 0$,
Device is ON & channel exists

$$Q = C \cdot V = WLC_{Ox} (V_{GS} - V_{TH})$$

$C = \frac{WLC_{Ox}}{\text{width} \times \text{length}}$ Capacitance per unit area



→ Case 2: When $V_{GS} \geq V_{TH}$ & $V_{DS} > 0$

$$Q = WLC_{Ox} (V_{GS} - V_{TH} - V(x))$$

$$Q_D = WC_{Ox} (V_{GS} - V_{TH} - V(x)) \quad (Q_D = Q/L)$$

$$\begin{aligned} I_D &= WC_{Ox} (V_{GS} - V_{TH} - V(x)) V_D \quad (V_D = I/Q) \\ &= WC_{Ox} (V_{GS} - V_{TH} - V(x)) \mu_n E \quad (V_D = \mu_n E) \rightarrow \text{Electric field} \\ &= WC_{Ox} (V_{GS} - V_{TH} - V(x)) \mu_n \frac{dV(x)}{dx} \quad (E = -\frac{dV(x)}{dx}) \end{aligned}$$

Current per length

$$I_D dx = +WC_{Ox} \mu_n (V_{GS} - V_{TH} - V(x)) dV$$

Now current is supplied by e^- (flow of e^-) and current will be -ve (opposite direction), hence cancelling to give +ve

Integrating on B.S.,

$$\int I_D dx = \int_0^{V_{DS}} WC_{Ox} \mu_n (V_{GS} - V_{TH} - V(x)) dV$$

$$I_D L = WC_{Ox} \mu_n \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$I_D = \frac{WC_{Ox} \mu_n}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Final Drain Current Equation (Triode/ Linear Region)

Region	Condition	Current eq ⁿ
Cut-off	$V_{GS} < V_{TH}$	$I_D = 0$
Deep Triode	$V_{GS} > V_{TH}$ $V_{DS} \ll 2(V_{GS} - V_{TH})$	$I_D = \mu_n C_{Ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$
Triode / Linear	$V_{GS} > V_{TH}$ $V_{DS} < (V_{GS} - V_{TH})$	$I_D = \mu_n C_{Ox} \frac{W}{L} \times V_{DS} \times (V_{GS} - V_{TH} - \frac{V_{DS}}{2})$
Saturation	$V_{GS} > V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = \mu_n C_{Ox} \frac{W}{L} \times (V_{GS} - V_{TH})^2$

→ For $I_{D\max}$, differentiate equation & equate to 0,

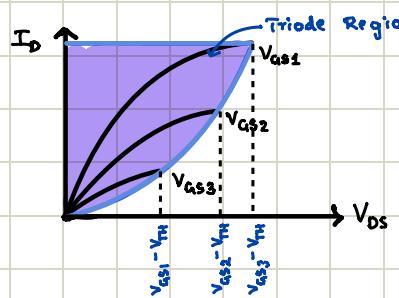
$$\frac{dI_D}{dV_{DS}} = \frac{W \mu_n C_{Ox}}{L} (V_{GS} - V_{TH} - V_{DS}) = 0$$

$$\Rightarrow V_{GS} - V_{TH} = V_{DS}$$

$$I_{D\max} = \frac{W \mu_n C_{Ox}}{L} \left(\frac{V_{GS} - V_{TH}}{2} \right)^2 \quad (W/L : \text{aspect ratio})$$

$V_{GS} - V_{TH}$: overdrive voltage

But at $V_{DS} = V_{GS} - V_{TH}$, there is pinch off & device prevents parabola thus $I_{D\max}$ is constant



Transconductance (g_m)

→ Ratio of current at output terminal to voltage at input terminal

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad | V_{DS}, \text{constant}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{Th})^2$$

$$g_m = \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{Th})$$

$$I_D = \frac{1}{2} \times g_m \times (V_{GS} - V_{Th})$$

$$\Rightarrow g_m = \frac{2I_D}{V_{GS} - V_{Th}}$$

$$V_{GS} - V_{Th} = \sqrt{\frac{2I_D L'}{2\mu_n C_{ox} W}}$$

$$\Rightarrow g_m = \mu_n C_{ox} \frac{W}{L'} \sqrt{\frac{2I_D L'}{2\mu_n C_{ox} W}}$$

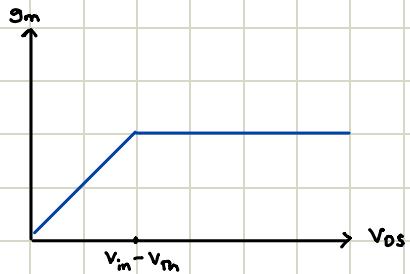
$$\Rightarrow g_m = \sqrt{\frac{2\mu_n C_{ox} W I_D}{L'}}$$

Transconductance - Triode Region

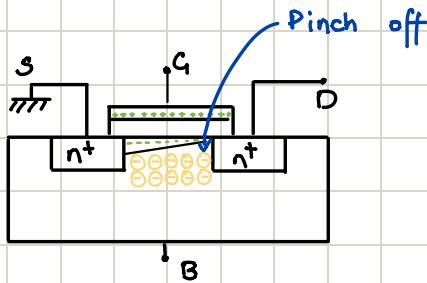
$$\rightarrow g_m = \frac{\partial}{\partial V_{GS}} \left(\mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \right)$$

$$= \mu_n C_{ox} \frac{W}{L} V_{DS}$$

g_m varies linearly with V_{DS}
in triode region



2nd Order Effect



- Once pinch off occurs in transistor, it enters saturation.
 Then effective channel length changes from L to L'
 As V_{DS} increases, pinch off point shifts towards source (L' decreases)
 This is known as **channel length modulation**

$$\rightarrow I_D = \frac{1}{2} M_n C_{ox} \frac{\omega}{L'} (V_{GS} - V_{TH})^2$$

$$\Rightarrow L' = L - \Delta L$$

$$\frac{1}{L'} = \frac{1}{L - \Delta L}$$

$$\frac{1}{L'} = \frac{L + \Delta L}{(L - \Delta L)(L + \Delta L)} = \frac{L + \Delta L}{L^2 - \Delta L^2}$$

$$\frac{1}{L'} = \frac{L + \Delta L}{L^2} = \frac{1 + \frac{\Delta L}{L}}{L} \quad (L^2 \gg \Delta L^2)$$

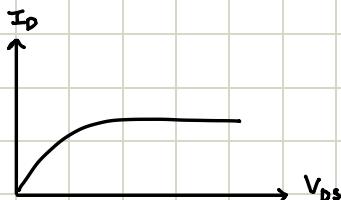
$$\frac{1}{L'} = \frac{1 + \lambda V_{DS}}{L} \quad (\frac{\Delta L}{L} \propto V_{DS})$$

λ : Channel modulation coefficient

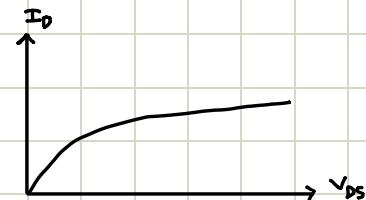
$$I_D = \frac{M_n C_{ox} \omega}{2} \left(\frac{1 + \lambda V_{DS}}{L} \right) (V_{GS} - V_{TH})^2 \Rightarrow I_D \propto \frac{\lambda V_{DS}}{L}$$

As V_{DS} increases, I_D also increases which results in non-zero slope

Theoretical



Practical



- Since I_D is no longer constant, MOSFET behaves like non-ideal current source in saturation region. This behaviour depends on larger value of λ & smaller value of L
 → C.L.M is seen mostly in short channel devices
 → I_D vs V_{DS} slope is negligible in long channel devices, so Ideal current source very high impedance

Q. Is there any C.L.M in triode region?

A. No! There is no pinch off in triode region. Only in saturation region

Transconductance (g_m)

$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS} = \text{const.}}$$

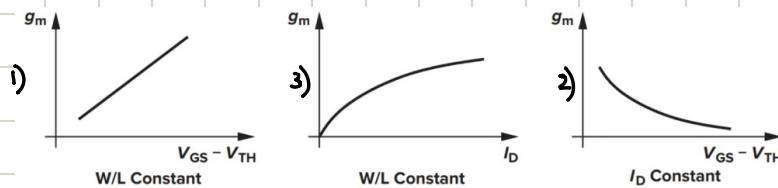
$$= MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right) (V_{GS} - V_{TH})$$

$$I_D = g_m \frac{(V_{GS} - V_{TH})}{2} \Rightarrow g_m = \frac{2 I_D}{V_{GS} - V_{TH}}$$

$$\rightarrow (V_{GS} - V_{TH}) = \sqrt{\frac{2 I_D}{MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right)}}$$

$$g_m = MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right) \sqrt{\frac{2 I_D}{MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right)}} \Rightarrow g_m = \sqrt{2 I_D MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right)}$$

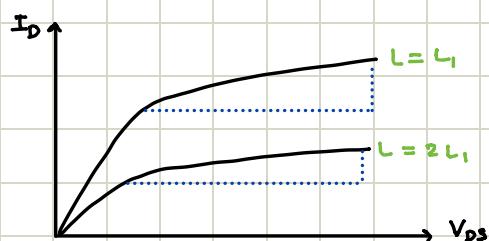
g_m with C.L.M	g_m without C.L.M
1) $g_m = MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right) (V_{GS} - V_{TH})$	1) $g_m = MnCox\omega \left(\frac{1}{L} \right) (V_{GS} - V_{TH})$
2) $g_m = \frac{2 I_D}{V_{GS} - V_{TH}}$	2) $g_m = \frac{2 I_D}{V_{GS} - V_{TH}}$
3) $g_m = \sqrt{2 I_D MnCox\omega \left(\frac{1 + \lambda V_{DS}}{L} \right)}$	3) $g_m = \sqrt{\frac{2 I_D MnCox\omega}{L'}}$



C.L.M I_D/V_{DS} Characteristics

$$\rightarrow I_D = \frac{MnCox\omega}{2L} (1 + \lambda V_{DS}) (V_{GS} - V_{TH})^2$$

$$\frac{\partial I_D}{\partial V_{DS}} \propto \frac{\lambda}{L} \Rightarrow \frac{\partial I_D}{\partial V_{DS}} \propto \frac{1}{L^2} \quad \left(\frac{\Delta L}{L} \propto V_{DS} \Rightarrow V_{DS} \propto \frac{1}{L} \right)$$



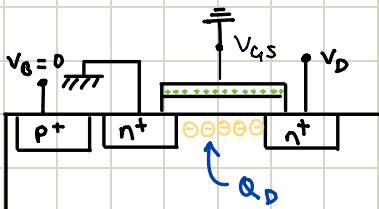
More L, less const. current (slope ↑)

Less L, more const. current (current source)

Body Effect

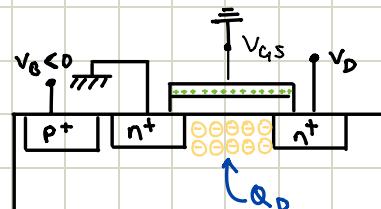
→ Till now we have seen Source & Body tied together & connected to ground in NMOS and V_{DD} in PMOS.

Now if they aren't connected to same potential, there is variation of Q_D



$$V_B = 0$$

$$V_G < V_{TH}$$



$$V_B < 0$$

$$V_G < V_{TH}$$

- As V_B becomes more negative, more holes are attracted to substrate connection, leaving large amount of negative immobile ions, & depletion layer widens
- Q_{dep} (Charge Density) also increases

$$V_{TH} = \phi_{ms} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

So, $Q_{dep} \propto V_{TH}$, Hence, V_{TH} increases

This phenomenon is called Body Effect or Back Gate Effect

- Increased V_{TH} , $V_{TH} = V_{Th_0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$

↳ Body Effect Coefficient

$$\gamma = \frac{\sqrt{2q\epsilon_s N_{sub}}}{C_{ox}}$$

- Bulk Potential V_B influences V_{TH} and hence I_D

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})$$

$$V_{BS} = -V_{SB}$$

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{Th})^2$$

Since there is a term V_{Th} in I_D we can find

$$\frac{\partial I_D}{\partial V_{BS}}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} 2(V_{GS} - V_{Th}) \left(-\frac{\partial V_{Th}}{\partial V_{BS}} \right)$$

Generally,

$$\gamma \Rightarrow 0.3 - 0.4 \sqrt{v}$$

$$\eta \Rightarrow 0.25$$

$$V_{Th} = V_{Th_0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

$$\frac{\partial V_{Th}}{\partial V_{BS}} = \frac{-\gamma}{\sqrt{2\phi_F + V_{SB}}} \quad \Rightarrow \quad \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th}) \cdot \frac{\gamma}{\sqrt{2\phi_F + V_{SB}}}$$

$$= g_m \gamma$$

$$\downarrow \eta$$

$$g_{mb} = g_m \gamma \quad \Rightarrow \quad \boxed{\gamma = \frac{g_{mb}}{g_m}}$$

Q. Calculate the total charge in NMOS if $C_{ox} = 10 \text{ fF}/\mu\text{m}^2$

$$w = 5 \mu\text{m}, L = 0.1 \mu\text{m}, V_{GS} - V_{Th} = 1 \text{ V}, V_{DS} = 0$$

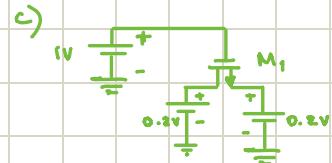
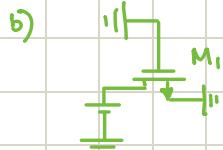
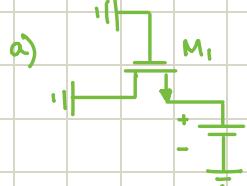
A. $Q_d = wL C_{ox} (V_{GS} - V_{Th})$

$$= 5 \times 10^{-6} \times 0.1 \times 10^{-6} \times 10 \times 10^{-15} \times (1)$$

$$= 5 \times 10^{-15} \text{ C}$$

$$= 5 \text{ fC}$$

Q. Identify the region of operation. $V_{Th} = 0.4 \text{ V}$ (NMOS) $C_{ox} = 100 \text{ fF}/\mu\text{m}^2$
 $= -0.4 \text{ V}$ (PMOS)



A. a) $V_{GS} = V_g - V_s$

$$= 0 - 1 = -1$$

Ground

$$V_{GS} < V_{Th} \Rightarrow \text{Cut-off region}$$

b) $V_{GS} = V_g - V_s < 0$

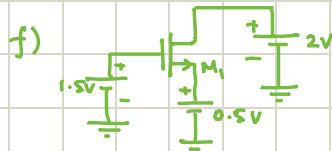
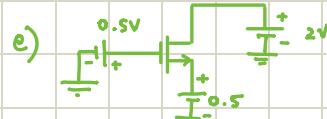
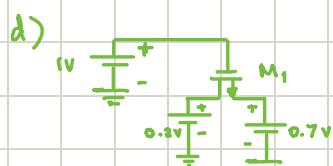
\Rightarrow Cut off region

c) $V_{DS} = 0$

$$V_{GS} - V_{Th} = 0.4 \text{ V}$$

$$V_{DS} < V_{GS} - V_{Th}$$

\hookrightarrow Deep Triode Region



d) $V_{GS} = 1 - 0.7$

$$= 0.3$$

$$V_{GS} < V_{Th} \Rightarrow \text{Cut-off}$$

e) $V_g = 0.5, V_s = 0.5$

$$V_{GS} = 0 < V_{Th}$$

\hookrightarrow Cut-off Region

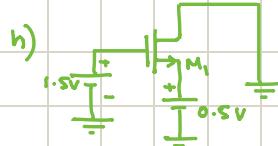
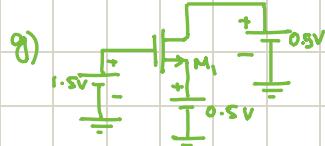
f) $V_g = 1.5, V_s = 0.5$

$$V_{GS} = 1 \text{ V}$$

$$V_{GS} - V_{Th} = 0.6 \text{ V}$$

$$V_{DS} = 2 - 0.5 = 1.5 \text{ V}$$

$V_{DS} > V_{GS} - V_{Th} \Rightarrow$ Saturation



g) $V_{GS} = 1.5 - 0.5 = 1 \text{ V}$

$$V_{DS} = 0.5 - 0.5 = 0 \text{ V}$$

$$V_{GS} - V_{Th} = 0.6 \text{ V}$$

$$V_{GS} - V_{Th} > V_{DS} \Rightarrow \text{Deep Triode}$$

h) $V_{GS} = 1.5 - 0.5 = 1 \text{ V}$

$$V_{DS} = 0 - 0.5 = -0.5 \text{ V}$$

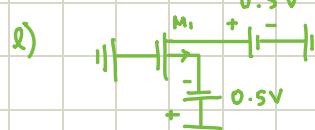
\hookrightarrow No region

i) $V_{GS} = 1.5 - 0 = 1.5 \text{ V}$

$$V_{DS} = 0.5 - 0 = 0.5 \text{ V}$$

$$V_{GS} - V_{Th} = 1.1 \text{ V}$$

$$V_{GS} - V_{Th} > V_{DS} \Rightarrow \text{Triode}$$



j) $V_{GS} = V_g - V_s = 0.5 \text{ V}$

$$V_{DS} = 0.5 \text{ V}$$

\hookrightarrow Saturation

k) $V_{GS} = V_g - V_s = 1 \text{ V}$

$$V_{DS} = 1 \text{ V}$$

\hookrightarrow Saturation

l) $V_{GS} = 0 - (-0.5) = 0.5 \text{ V}$

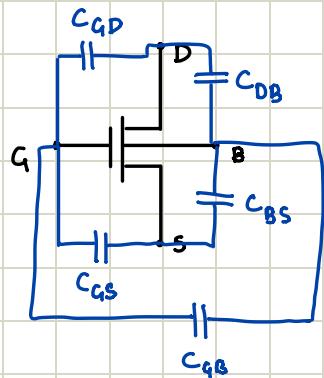
$$V_{DS} = 0.5 - (-0.5) = 1 \text{ V}$$

\hookrightarrow Saturation

MOS Device Capacitance

→ Exists b/w every 2 of the 4 terminals of MOSFET

→ Terminal



→ Physical Structure

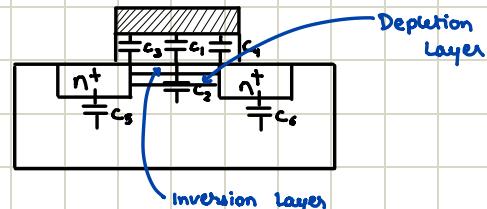
C_1 - Oxide Capacitance b/w Gate & Channel
= $WL C_{Ox}$

C_2 - Depletion capacitance b/w channel & substrate
= $WL \sqrt{(q\epsilon_{Si} N_{sub}) / 4\Phi_F}$

C_3, C_4 - Capacitance due to overlap of the gate poly with the source & drain
= $W C_{ov}$

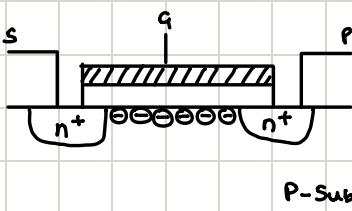
C_5, C_6 - Junction capacitance

↳ C_j - Bottom Plate Capacitance
↳ C_{jsw} - Sidewall Capacitance



→ Capacitance in different region

i) Cutoff Region → ($V_{GS} < V_{Th}$)



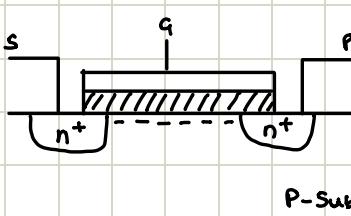
$$C_{GD} = W C_{Ox} \text{ series}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$= \frac{C_d (W L C_{Ox})}{C_d + W L C_{Ox}} \Rightarrow C_{GS} = C_{GD} = W C_{ov}$$

(C_{ov} = Overlap Capacitance)

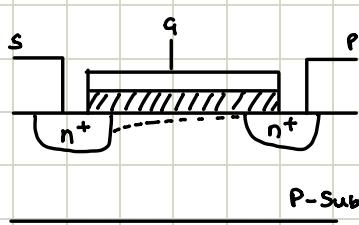
2) Triode Region → ($V_{GS} > V_{Th}$)



$$C_{GS} = C_{GD} = \frac{W L C_{Ox}}{2} + W C_{ov}$$

$$C_{GB} = \text{Neglect}$$

3) Saturation →

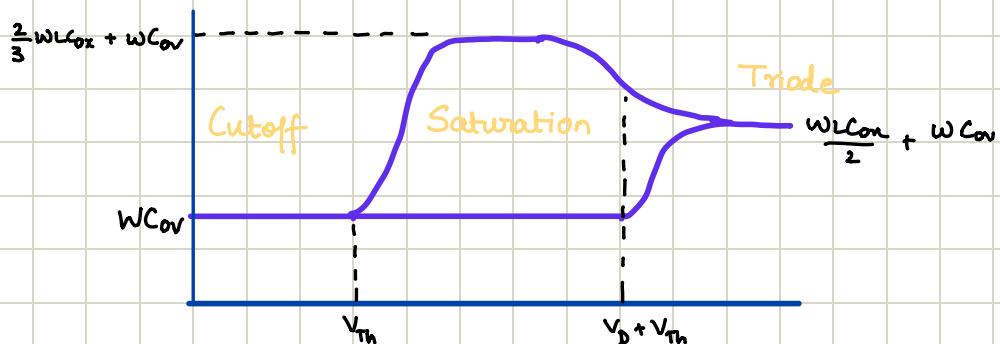


$$C_{GD} = W C_{ov}$$

$$C_{GS} = \frac{2 W L C_{Ox}}{3} + W C_{ov}$$

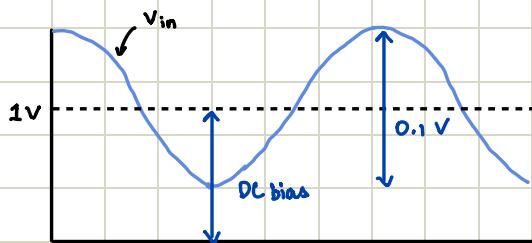
$$C_{GB} = \text{Neglect}$$

Behaviour of C_{GD} & C_{GS} in different region of operation



Small Signal Model

→ It's equivalent circuit used in an amplifier when the amplitude of AC circuit is small compared to DC bias voltage



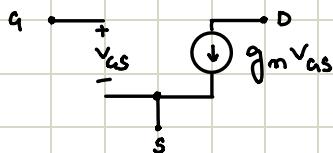
→ In saturation, I_D depends on V_{GS}

$$\Delta I_D \propto \Delta V_{GS}$$

$$\Delta I_D = g_m \Delta V_{GS}$$

$$i_D = g_m v_{GS}$$

It is represented as voltage-dependant current source b/w S & D terminals

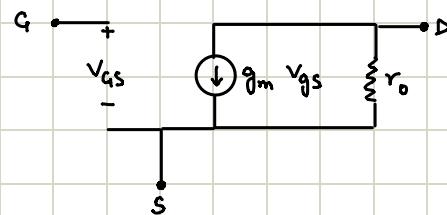


Small Signal model for short channel devices

→ Because of channel-length modulation effect, in saturation, I_D depends on $V_{DS}^2 V_{GS}$

→ Linear dependance of I_D on V_{DS} is represented by a resistor r_o b/w S & D

$$\begin{aligned} r_o &= \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}} \\ &= \frac{1}{\frac{1}{2} \mu n C_{ox} \frac{W}{L} (v_{GS} - v_{Th})^2} \\ &= \frac{1}{\lambda I_D} \end{aligned}$$



Small signal model considering body effect

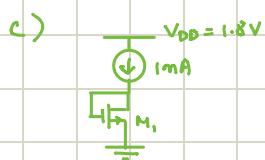
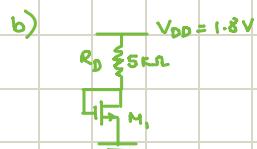
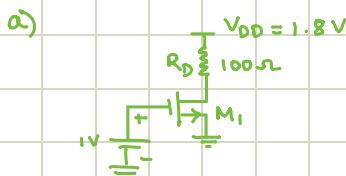
→ Body effect excess in devices where substrate & source aren't connected to same potential, as a result V_{Th} will increase

$$V_{Th} = V_{Th0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

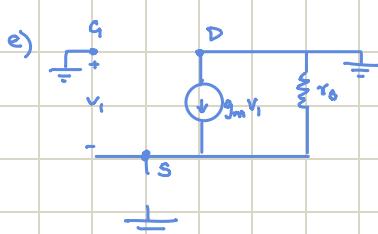
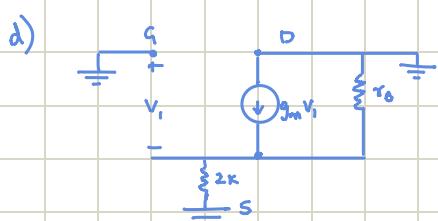
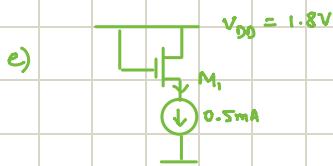
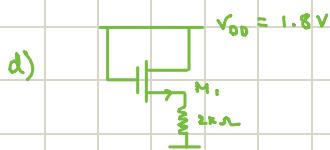
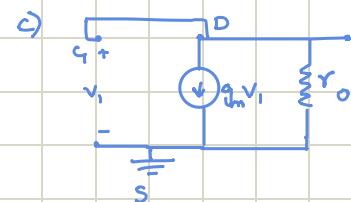
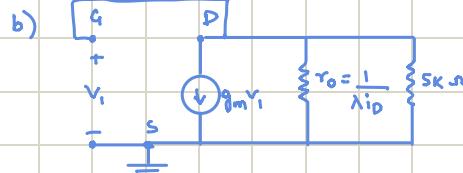
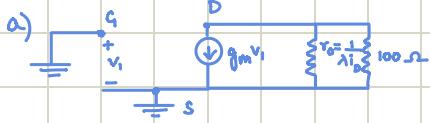
Now, I_D depends on V_{GS} , V_{DS} and V_{BS}

$$\frac{\partial I_D}{\partial V_{BS}} = g_{mb} \Rightarrow i_D = g_{mb} V_{BS}$$

Q. Construct small signal model for each of the following circuit where $\lambda = 0.1 \text{ V}^{-1}$



→ In order to construct SSM of the circuit, DC Voltage sources must be open



Q. Assume $\lambda = 0$, compute $\frac{W}{L}$ of M1 in Fig below such that the device operates at edge of saturation

A. $V_{DS} = V_{GS} - V_{Th}$

$$V_{GS} = V_G - V_S = 1 - 0 = 1 \text{ V}$$

$$V_{DS} = 1 - 0.4 = 0.6 \text{ V}$$

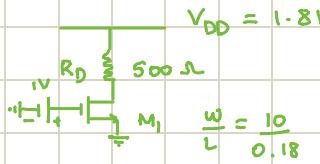
$$V_{DD} = I_D R_D + V_{DS} \Rightarrow I_D R_D = V_{DD} - V_{DS} = 1.8 - 0.6 = 1.2$$

$$I_D = \frac{1.2}{1000} = 1.2 \text{ mA}$$

$$I_D = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 = \frac{1}{2} \times 200 \times 10^{-6} \times \frac{W}{L} (1 - 0.4)^2 \Rightarrow \frac{W}{L} = \frac{100}{3}$$



Q. In the fig. below, what is min. allowable value of V_{DD} if M_1 must not enter triode region? Assume $\lambda = 0$



A. $V_{DS} = V_{GS} - V_{Th} = 1 - 0.4 = 0.6 \text{ V}$

$$V_{Th} = 0.4$$

$$M_n C_{ox} = 200 \times 10^{-6}$$

$$\begin{aligned} V_{DD} &= I_D \times 500 + V_{DS} \\ &= 2 \times 10^{-3} \times 500 + 0.6 \\ &= 1.6 \text{ V} \end{aligned}$$

$$I_D = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2$$

$$= \frac{1}{2} 200 \times 10^{-6} \times \frac{10}{0.18} (0.6)^2$$

$$= 2 \times 10^{-3}$$

MOSFET Operating Point Analysis

- Amplifier produces output that is magnified version of input
- Important aspects of Amplifier's Performance -

- i) Power dissipation
- ii) Speed
- iii) Noise
- iv) Operating Voltage
- v) Area
- vi) Linearity etc.,
- vii) I/O impedances

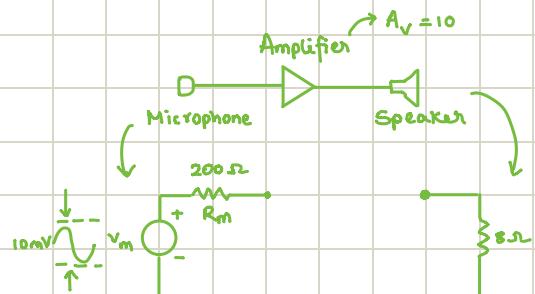
I/O of ideal voltage amplifier

- At input, circuit must operate as voltmeter
 - i) Ideal input impedance = ∞
 - ii) Input signal might not get attenuated / distorted
 - iii) No power loss & signal current used properly
- At output, circuit must behave as voltage source
 - i) Ideal Output impedance = 0
 - ii) Max possible output amplified signal w/o any attenuation

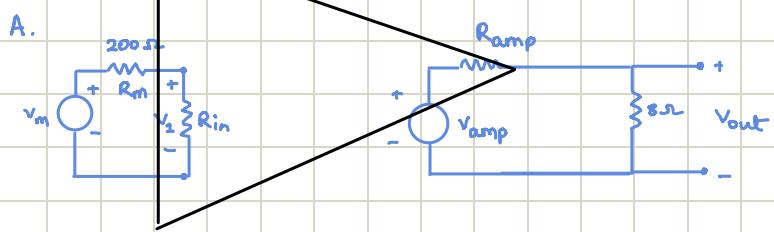
→ sense voltage w/o disturbing preceding stage

→ Delivers constant signal level to any load impedance

Q. Amplifier with voltage gain of 10, senses signal generated by microphone & applies amplified output to speaker. Assume microphone can be modeled with voltage source having a 10 mV peak-to-peak signal & series resistance of $200\ \Omega$. Assume speaker represented by $8\ \Omega$



- Determine signal level sensed by amplifier if circuit has input impedance of $2\text{k}\Omega$ or $500\ \Omega$
- Determine signal level sensed by amplifier if circuit has output impedance of $10\ \Omega$ or $2\ \Omega$



$$a) V_1 = \frac{R_{in} V_m}{R_{in} + R_m}$$

For $R_{in} = 2\text{k}\Omega$

$$V_1 = \frac{2000 V_m}{2200} \Rightarrow V_1 = 0.91 V_m$$

For $R_{in} = 500\ \Omega$

$$V_1 = \frac{500 V_m}{700} = 0.71 V_m$$

Only 9% less than microphone signal level | 30% less than microphone signal level

Therefore, desirable to maximize input impedance

$$b) V_{out} = \frac{R_L V_{amp}}{R_L + R_{amp}}$$

For $R_{amp} = 10\ \Omega$

$$V_{out} = \frac{8}{18} V_m \Rightarrow V_{out} = 0.44 V_{amp}$$

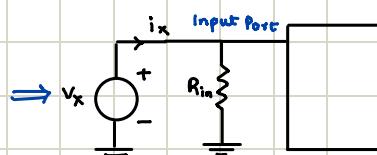
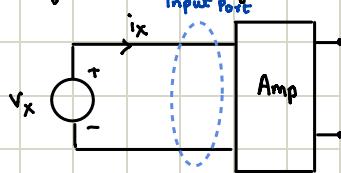
For $R_{amp} = 2\ \Omega$

$$V_{out} = \frac{8}{10} V_m \Rightarrow V_{out} = 0.8 V_{amp}$$

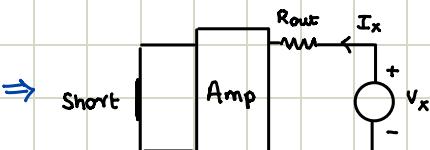
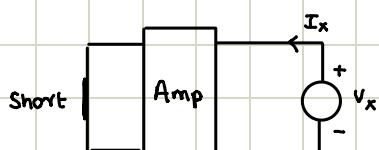
Therefore, desirable to minimize output impedance of amplifier

Measurement of Input & Output Impedance

- The I/O impedances measured b/w I/O nodes while all independant voltage & current sources are set to zero
- Voltage source with short connection
- Current source with open connection
- Then apply a voltage source v_x to the node of interest & measure resulting I_x

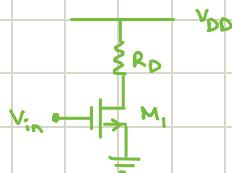


$$R_{in} = \frac{v_x}{I_x} = \frac{\text{Input Voltage}}{\text{Input Current}}$$



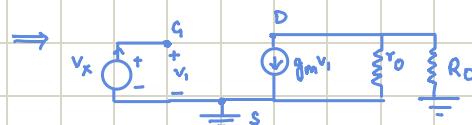
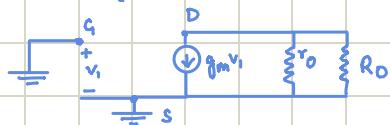
$$R_{out} = \frac{v_x}{I_x} = \frac{\text{Output Voltage}}{\text{Output Current}}$$

Q. Calculate I/O impedance of given circuit, where transistor is in saturation region & there is channel length modulation

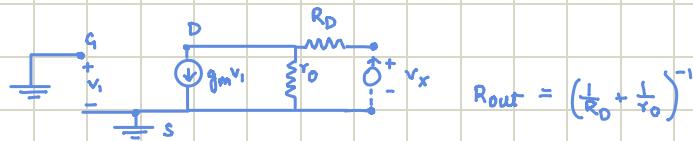


A.

Small Signal Model →

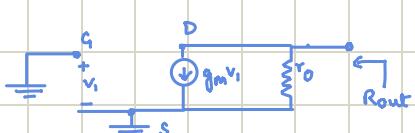


$$R_{in} = \frac{v_x}{I_x}$$



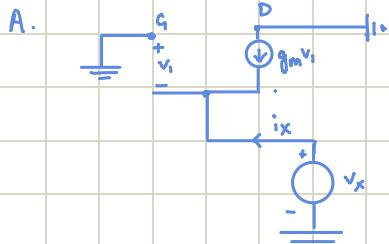
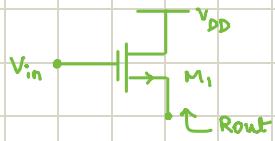
$$R_{out} = \left(\frac{1}{R_D} + \frac{1}{r_o} \right)^{-1}$$

Q. Calculate Output Impedance of circuit where channel length modulation is considered from drain end



$$R_{out} = r_o$$

Q. Calculate the impedance seen at the source of M₁. Neglect channel length modulation



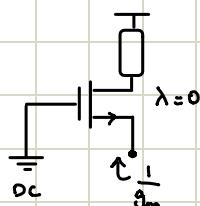
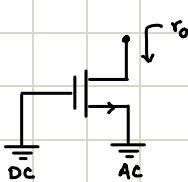
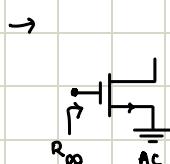
$$KVL, V_i + V_x = 0 \Rightarrow V_i = -V_x$$

$$g_m V_i = -i_x$$

$$\frac{1}{g_m} = \frac{V_x}{i_x}$$

$$R_{out} = \frac{1}{g_m}$$

→ 3 Important Rules



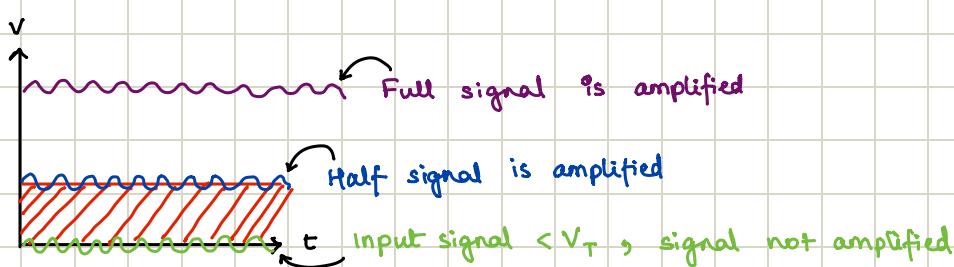
- Looking into the gate, we see ∞
- Looking into the drain, we see r_o if the source (ac) is grounded
- Looking into the source, we see $\frac{1}{g_m}$ if the gate (ac) is grounded and channel length modulation is neglected

Biasing

- Ensures transistor operates in correct region to amplify the signals
- DC & Small-Signal Analysis
 - Procedure for Amplifier Analysis
 - Compute the operating (quiescent) conditions (terminal voltages & currents) of each transistor in the absence of signals
 - Called the 'dc analysis' or 'bias analysis', this step determines both the region of operation (saturation or triode) & small-signal parameters of each device

Need for DC biasing

- If a signal of very small voltage is given to input of MOSFET, it can't be amplified because two conditions must be met
 - i) input voltage should exceed cut-in voltage for transistor to be ON
 - ii) MOSFET should be in saturation region to be operated as amplifier



Small Signal Analysis

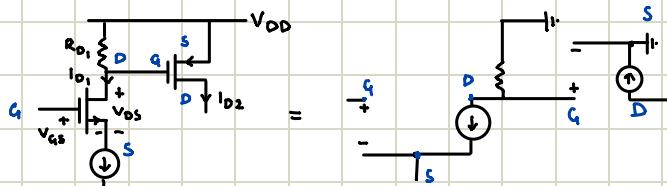
- Study of response of circuit to small signals and compute quantities like voltage gain & I/O impedances
- Small Signal analysis deals only with small changes in voltages & currents in a circuit around their quiescent values

Construction of Small Signal model

- Constant sources don't vary with time, so, all constant voltage sources are grounded & constant current sources are open

$$\begin{array}{c} + \\ \text{---} \\ - \end{array} = \text{short}$$

$$\begin{array}{c} \text{---} \\ \text{---} \end{array} = \text{open}$$



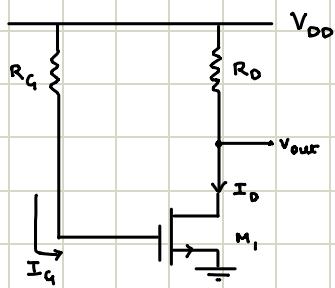
$$V_{GS} = \frac{R_1 V_{DD}}{R_1 + R_2}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{R_1 V_{DD}}{R_1 + R_2} - V_{th} \right)^2$$

$$V_{DD} = I_D R_D + V_{DS} \Rightarrow V_{DS} = V_{DD} - I_D R_D$$

Simple Biasing (using R_g)

- Uses a resistor connected to a base of transistor to establish bias current
- Not very stable as it depends on properties like current gain (β), which can vary



$$R_g I_g + V_{GS} = V_{DD}$$

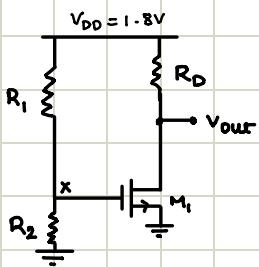
$$I_g = \frac{V_{DD} - V_{GS}}{R_g} \Rightarrow I_D = \beta \left(\frac{V_{DD} - V_{GS}}{R_g} \right)$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$= V_{DD} - \beta \left(\frac{V_{DD} - V_{GS}}{R_g} \right) \times R_D$$

Simple Biasing (Using Resistive Divider Network)

- More stable method where 2 resistors form voltage divider to set the base voltage, making bias less sensitive to β variations



$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

If M_1 in saturation region, $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{th} \right)^2$

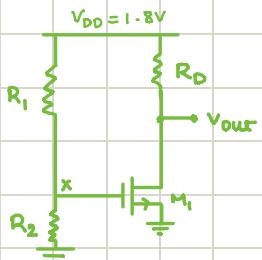
$$V_{DS} \geq V_{GS} - V_{th}$$

$$V_{DD} - R_D I_D \geq \frac{R_2 V_{DD}}{R_1 + R_2} - V_{th}$$

Q. Determine the bias current of M_1 in figure given below assuming $V_{Th} = 0.5V$

$$M_nC_{ox} = 100 \mu A/V^2, \frac{W}{L} = \frac{6}{0.18}, \lambda = 0, R_1 = 20k\Omega, R_2 = 15k\Omega$$

What is max allowed value of R_D for M_1 to remain in saturation?



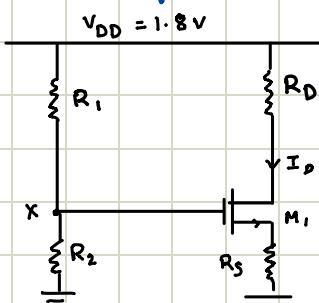
$$A. V_{GS} = \frac{V_{DD}R_2}{R_1+R_2} = \frac{1.8 \times 15}{20+15} = 0.77V$$

$$I_D = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 = \frac{1}{2} \times 100 \times 10^{-6} \times \frac{6}{0.18} \times (0.77 - 0.5)^2 = 102 \mu A$$

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{1.8 - 0.27}{102 \times 10^{-6}} = 15k\Omega$$

Biasing with Source Degeneration

→ Adds resistor to source to stabilize the operating point, making it less sensitive to variations in temperature or transistor properties, thereby providing source degeneration



→ Assume M_1 in saturation & $\lambda = 0$

$$V_X = \frac{R_2 V_{DD}}{R_1 + R_2}$$

and since, $V_X = V_{GS} + I_D R_S$

$$\frac{R_2 V_{DD}}{R_1 + R_2} = V_{GS} + I_D R_S \quad \text{--- (1)}$$

$$I_D = \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{GS} \right) \times \frac{1}{R_S}$$

$$\text{also, } I_D = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 = \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{GS} \right) \times \frac{1}{R_S} (V_{GS} + (V_i - V_{Th}))^2 = (V_i - V_{Th})^2 - V_{Th}^2 - \frac{2 R_2 V_{DD} V_i}{R_1 + R_2}$$

$$\text{We know } V_i = \frac{1}{M_n C_{ox} \frac{W}{L} R_S} \Rightarrow M_n C_{ox} \frac{W}{L} V_i = \frac{1}{R_S}$$

$$\frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 = \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{GS} \right) \times M_n C_{ox} \frac{W}{L} V_i$$

$$\frac{1}{2} (V_{GS} - V_{Th})^2 = \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{GS} \right) V_i$$

(Note: V_Y must exceed $V_X - V_{Th}$ to ensure operation in saturation region i.e., $V_D > V_g - V_{Th}$)

$$V_{GS}^2 + V_{Th}^2 - 2V_{GS}V_{Th} = \frac{2R_2 V_{DD}}{R_1 + R_2} - 2V_{GS}V_i$$

$$V_{GS}^2 + V_{Th}^2 + 2V_{GS}(V_i - V_{Th}) - \frac{2R_2 V_{DD}}{R_1 + R_2} = 0$$

and $(V_i - V_{Th})^2$ on B.S

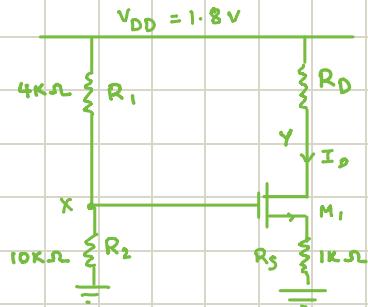
$$V_{GS}^2 + (V_i - V_{Th})^2 + 2V_{GS}(V_i - V_{Th}) = (V_i - V_{Th})^2 - V_{Th}^2 - \frac{2R_2 V_{DD} V_i}{R_1 + R_2}$$

$$V_{GS} = -(V_i - V_{Th}) + \sqrt{(V_i - V_{Th})^2 - V_{Th}^2 - \frac{2R_2 V_{DD} V_i}{R_1 + R_2}}$$

$$V_{GS} = -(V_i - V_{Th}) + \sqrt{V_i^2 + 2V_i \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{Th} \right)}$$

Put V_{GS} in (1) & find I_D

Q. Determine the bias current of M_1 in figure given below assuming $V_{Th} = 0.5V$
 $MnCox = 100 \mu A/V^2$, $\frac{W}{L} = \frac{5}{0.18}$, $\lambda = 0$. What is max allowable value of R_D for M_1 ?



$$A. \quad V_X = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{1.8 \times 10}{4 + 10} = 1.285V$$

$$V_X = V_{GS} + I_D R_S$$

$$V_I = \frac{1}{R_S MnCox \frac{W}{L}} = \frac{1}{10^3 \times 100 \times 10^{-6} \times \frac{5}{0.18}} = 0.36V$$

$$\begin{aligned} V_{GS} &= -(V_I - V_{Th}) + \sqrt{V_I^2 + 2V_I \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{Th} \right)} \\ &= -(0.36 - 0.5) + \sqrt{(0.36)^2 + (2 \times 0.36) \left(\frac{10 \times 1.8}{10 + 4} - 0.5 \right)} \\ &= 0.974V \end{aligned}$$

$$I_D = \frac{1.285 - 0.974}{10^3} = 0.311 \text{ mA}$$

$$V_{DD} = V_{DS} + I_D R_D + I_D R_S$$

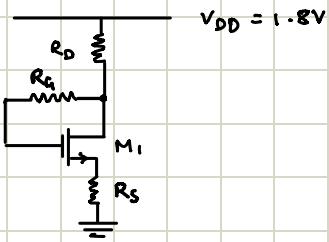
$$1.8 = V_{GS} - V_{Th} + I_D R_D + I_D R_S$$

$$1.8 - \frac{0.974 + 0.5}{0.311 \times 10^{-3}} - 0.311 = R_S$$

$$R_S = 3.263 \text{ k}\Omega$$

Self Biasing

- Commonly used in discrete & integrated circuits
- Gate voltage is provided from drain, hence, the name self-biasing



$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\text{Since } V_{DS} = V_{GS}$$

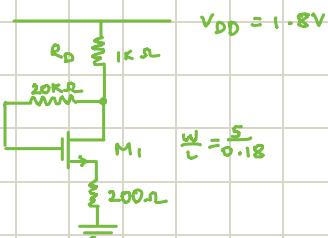
$$V_{DD} = I_D R_D + V_{GS} + I_D R_S$$

$$V_{GS} = V_{DD} - I_D (R_D + R_S)$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{DD} - I_D (R_D + R_S) - V_{th} \right)^2$$

- I_D can be obtained by solving the quadratic eqn
If I_D is known, V_{GS} can be calculated

Q. Calculate M₁ drain current if $\mu_n C_{ox} = 100 \mu A/V^2$, $V_{th} = 0.5V$, $\lambda = 0$
What value of R_D is necessary to reduce I_D by factor of 2?



A. $V_{DD} = I_D R_D + V_{DS} + I_D R_S$

$$V_{DS} = V_{GS}$$

$$V_{DD} = I_D (R_D + R_S) + V_{GS}$$

$$V_{GS} = V_{DD} - I_D (R_D + R_S)$$

$$= 1.8 - I_D (1000 + 200)$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$= \frac{1}{2} \times 100 \times \frac{5}{0.18} (1.8 - 1200 I_D - 0.5) \Rightarrow I_D = 556 \mu A$$

$$V_{DD} = I_D (R_D + R_S) + V_{GS}$$

$$1.8 = 278 \times 10^{-6} (R_D + 200) + 0.95$$

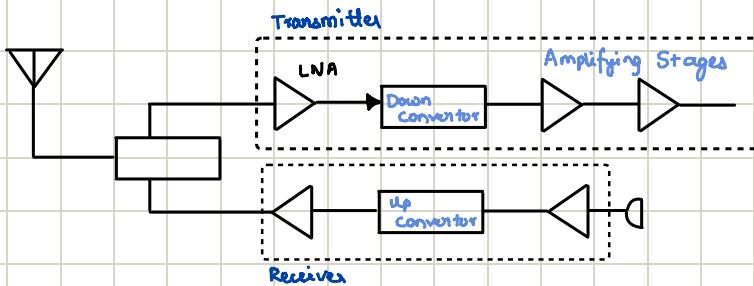
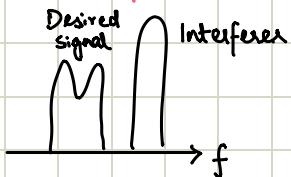
$$R_D = 2.867 k\Omega$$

Single

Stage

Amplifier

→ Role of an amplifier system



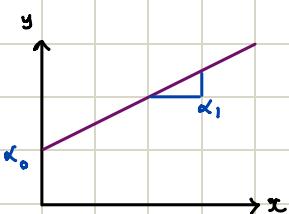
Ideal Amplifier

→ It generates the output $y(t)$ which is a linear replica of $x(t)$

$$y(t) = \alpha_1 x(t)$$

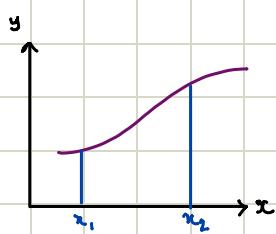
→ Since output signal is superimposed on a DC biased condition, we can write

$$y(t) = \underbrace{\alpha_0}_{\text{dc bias}} + \underbrace{\alpha_1}_{\text{gain}} x(t)$$



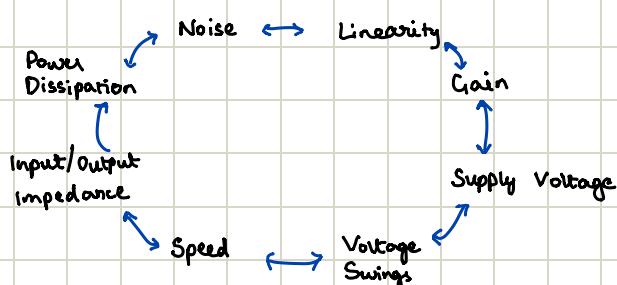
Non-ideal Amplifier

→ $\alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots$



(Distorts signal of interest or creates unwanted interactions among several signals that may coexist at the input)

Analog Design Octagon



Customer Specification

- Power Dissipation, Speed

Fabrication Related

- Supply Voltage

Design Specification

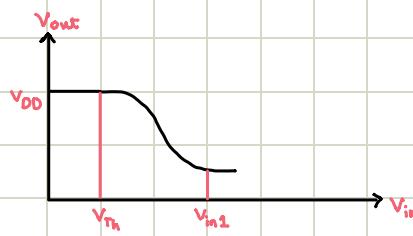
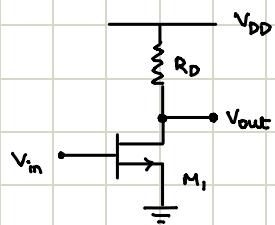
- I/O Impedance, Gain, Voltage Swings

Accuracy Specification

- Noise, Linearity

N L G V I/O S P S
A D F C

Common Source with Resistive Load



M_1 in cut-off region for $V_{in} < V_{Th}$
 M_1 in saturation for $V_{in} > V_{Th}$
 M_1 in linear region for $V_{in} - V_{Th} > V_{out}$

Output voltage,

$$V_{out} = V_{DD} - R_D I_D$$

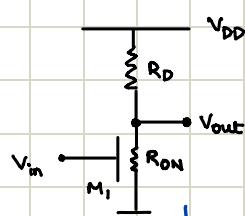
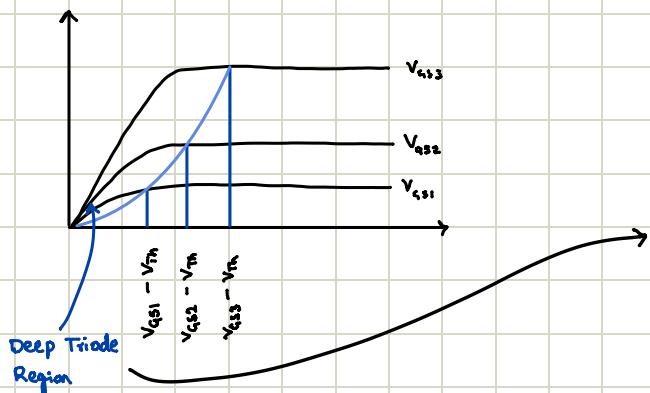
Input impedance high at low frequencies

We will study high frequencies at end of unit

$$\rightarrow \text{MOSFET in saturation} \Rightarrow V_{out} = V_{DD} - R_D \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{in} - V_{Th})^2$$

$$\rightarrow \text{MOSFET at edge of saturation} \Rightarrow V_{in2} - V_{Th} = V_{DD} - R_D \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{in2} - V_{Th})^2$$

$$\rightarrow M_1 \text{ in linear} \Rightarrow V_{out} = V_{DD} - R_D \frac{\mu_n C_{ox}}{2} \left[(V_{in} - V_{Th}) V_{out} - \frac{V_{out}^2}{2} \right]$$



equivalent circuit in deep triode region

$$\rightarrow V_{out} = \frac{V_{DD} R_{DS}}{R_{DS} + R_D} = \frac{V_{DD}}{1 + \frac{\mu_n C_{ox}}{2} \frac{W}{L} R_D (V_{in} - V_{Th})}$$

\rightarrow MOSFET in saturation

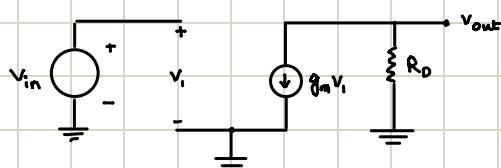
$$V_{out} = V_{DD} - R_D \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{in} - V_{Th})^2$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D \frac{\mu_n C_{ox}}{L} (V_{in} - V_{Th})$$

$$A_V = -g_m R_D$$

Gain

\hookrightarrow MOS Transconductance



\hookrightarrow Small Signal Model

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{X_i}$$

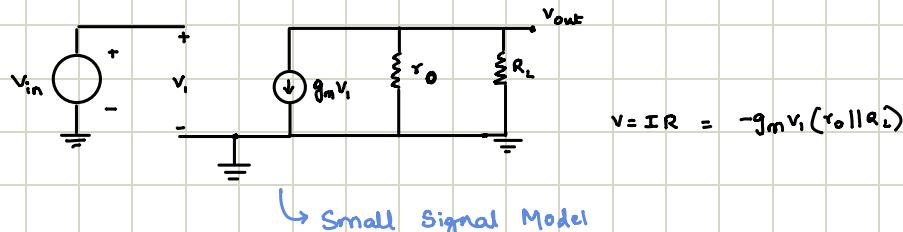
$$A_V = -\sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D \frac{V_{DD}}{I_D}}$$

$$A_V = -\sqrt{2 \mu_n C_{ox} \frac{W}{L} \cdot \frac{V_{DD}}{\sqrt{I_D}}}$$

\rightarrow Design Tradeoffs

- Increase $\frac{W}{L}$ \Rightarrow Greater Device capacitances
- Increase V_{DD} \Rightarrow Limits V_{out} swing
- Reduce I_D \Rightarrow Greater time constant

→ With Channel Length Modulation



$$A_V = \frac{V_{out}}{V_{in}}$$

$$V_{in} = V_i$$

$$V_{out} = -g_m V_i (r_o \parallel R_L)$$

$$A_V = -\frac{g_m V_i (r_o \parallel R_L)}{V_i} = -g_m (r_o \parallel R_L) = -g_m \frac{r_o R_L}{r_o + R_L}$$

From equation,

$$V_{out} = V_{DD} - I_D R_L$$

Saturation I_D with CLM

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{\omega}{L} (V_{in} - V_{th})^2 (1 + \lambda V_{out})$$

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{\omega}{L} R_L (V_{in} - V_{th})^2 (1 + \lambda V_{out})$$

$$A_V = \frac{\partial V_{out}}{\partial V_{in}} = 0 - \frac{1}{2} \mu_n C_{ox} \frac{\omega}{L} R_L (1 + \lambda V_{out}) \cancel{(V_{in} - V_{th})}$$

$$- \frac{1}{2} \mu_n C_{ox} \frac{\omega}{L} R_L (V_{in} - V_{th})^2 \left(0 + \lambda \frac{\partial V_{out}}{\partial V_{in}} \right)$$

$$= -\mu_n C_{ox} \frac{\omega}{L} R_L (V_{in} - V_{th}) (1 + \lambda V_{out}) - I_D \lambda \frac{\partial V_{out}}{\partial V_{in}} R_L$$

$$(g_m = \mu_n C_{ox} \frac{\omega}{L} (1 + \lambda V_{out}) (V_{in} - V_{th}))$$

$$\left(r_o = \frac{1}{\lambda I_D} \right)$$

$$A_V = -g_m R_L - \frac{A_V R_L}{r_o}$$

$$A_V \left(1 + \frac{R_L}{r_o} \right) = -g_m R_L \Rightarrow$$

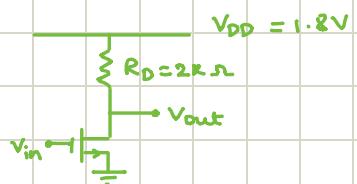
$$A_V = \frac{-g_m R_L}{\left(1 + \frac{R_L}{r_o} \right)}$$

$$A_V = -g_m (r_o \parallel R_L)$$

- Q. In CS stage, $w/l = 30/0.18$, $\lambda = 0$, $\mu nCox = 200 \mu A/V^2$
- What gate voltage yields drain current of 0.5mA (M1 in saturation)
 - With such drain bias current, calculate voltage gain of the stage.

A. a) $I_D = \frac{1}{2} \mu nCox \frac{w}{L} (V_{GS} - V_{TH})^2$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu nCox \frac{w}{L}}} + V_{TH} = \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{200 \times 10^{-6} \times \frac{30}{0.18}}} + 0.4 \\ = 0.573 \text{ V}$$



$$V_{DS} = V_{DD} - I_D R_D \\ = 1.8 - 0.5 \times 10^{-3} \times 2000 \\ = 0.8 \text{ V}$$

b) $A_v = -\sqrt{2\mu nCox \frac{w}{L}} \frac{V_{RD}}{\sqrt{I_D}} = -\sqrt{\frac{2\mu nCox w}{L}} \cdot \frac{I_D R_D}{\sqrt{I_D}}$
 $= -\sqrt{\frac{2 \times 200 \times 10^{-6} \times \frac{30}{0.18}}{0.18} \times 0.5 \times 10^{-3} \times 2 \times 10^3} = -11.54$

- Q. We wish to design a CS stage for $A_v = 5$, $\frac{w}{l} \leq \frac{20}{0.18}$

Determine required R_D if power dissipation mustn't exceed 1mW

A. $A_v = 5$

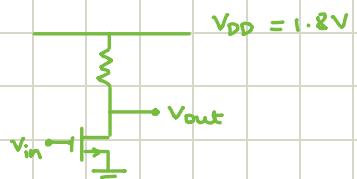
$$\frac{w}{l} \leq \frac{20}{0.18}$$

$$A_v = \sqrt{2\mu nCox \frac{w}{L} I_D \times R_D}$$

$$P_D = I_D V_{DD} \Rightarrow I_D = \frac{10^{-3}}{1.8} = 0.55 \text{ mA}$$

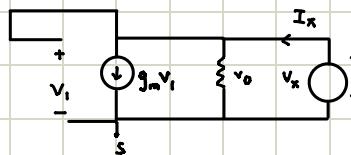
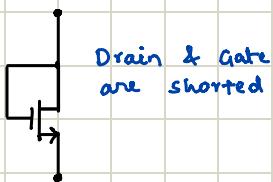
$$S = \sqrt{\frac{2 \times 200 \times 10^{-6} \times \frac{20}{0.18} \times 0.5 \times 10^{-3}}{0.18} \times R_D}$$

$$R_D = 1.011 \text{ k}\Omega$$



→ Common Source with diode connected load

→ In some CMOS technologies, it is difficult to fabricate resistors with controlled value, so it is desirable to replace R_D with MOS Transistor which is always in saturation & the configuration should exhibit small signal behaviour to 2 terminal resistor



$$v_i = v_x$$

$$I_x = \frac{v_x}{r_o} + g_m v_x$$

$$\frac{v_x}{I_x} = \frac{1}{g_m + \frac{1}{r_o}} = \frac{r_o}{g_m r_o + 1} = \frac{r_o}{g_m (r_o + \frac{1}{g_m})}$$

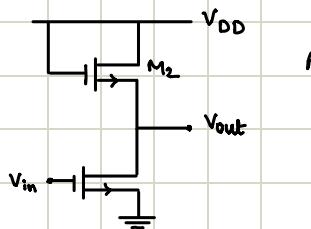
$$= \frac{r_o \times g_m}{(r_o + \frac{1}{g_m})} = \left(\frac{1}{g_m}\right) \parallel r_o$$

$$R_{out} = \frac{v_x}{I_x} = \frac{1}{g_m} \parallel r_o \approx \frac{1}{g_m}$$

→ Resistance b/w drain & source

$$I_x = (g_m + g_{mb}) v_x + \frac{v_x}{r_o}$$

$$\frac{v_x}{I_x} = \frac{1}{g_m + g_{mb} + \frac{1}{r_o}} = \frac{1}{g_m + g_{mb}} \parallel r_o \approx \frac{1}{g_m + g_{mb}}$$



$$A_v = \frac{-g_{m1}}{g_{m2} + g_{mb2}} = \frac{-g_{m1}}{g_{m2} (1 + \frac{g_{mb2}}{g_{mb}})} = \frac{-g_{m1}}{g_{m2}} \times \frac{1}{1 + \eta}$$

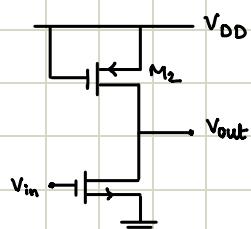
$$= -\frac{\sqrt{2\mu_n C_{ox} (\frac{w}{L})_1 I_{D1}}}{\sqrt{2\mu_n C_{ox} (\frac{w}{L})_2 I_{D2}}} \times \frac{1}{1 + \eta}$$

$$I_{D1} = I_{D2}$$

$$A_v = -\frac{\sqrt{(\frac{w}{L})_1}}{\sqrt{(\frac{w}{L})_2}} \times \frac{1}{1 + \eta}$$

→ if η is constant, the gain A_v is independant of I_D & voltages

→ When PMOS load is used as diode connected load



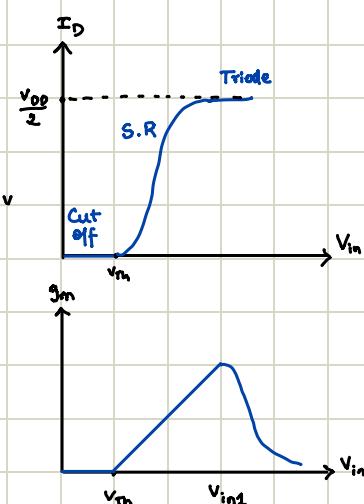
→ The effect of body effect is reduced, A_v increases

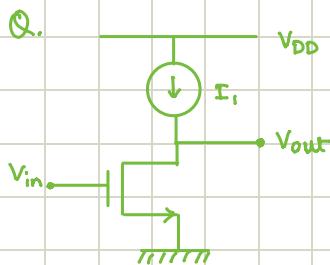
$$\rightarrow I_{D1} = I_{D2}$$

$$\mu_n \left(\frac{w}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \mu_p \left(\frac{w}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

$$A_v = \sqrt{\frac{\mu_n \left(\frac{w}{L}\right)_1}{\mu_p \left(\frac{w}{L}\right)_2}}$$

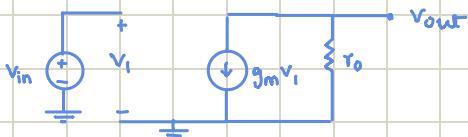
$$\Rightarrow \frac{|V_{GS2} - V_{TH2}|}{|V_{GS1} - V_{TH1}|} = A_v$$





Assume M_1 is biased in saturation region, calculate small signal voltage gain

A.



$$V_{in} = V_i$$

$$V_{out} = -g_m V_i r_o$$

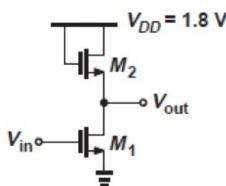
$$A_v = \frac{-g_m V_i r_o}{V_i} = -g_m r_o$$

Intrinsic Gain of Transistor

→ Intrinsic Gain of Transistor is the quantity representing maximum voltage gain that can be achieved using a single device

Q.

We wish to design the circuit shown in Fig. for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.



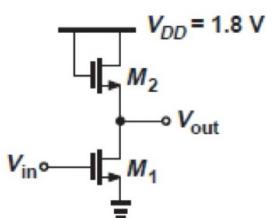
A. $A_v = 3$

$$\left(\frac{W}{L}\right)_1 = \frac{20}{0.18}$$

$$A_v = -\sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} \Rightarrow \left(\frac{W}{L}\right)_2 = \frac{\left(\frac{W}{L}\right)_1}{A_v^2} = \frac{20/0.18}{3^2} = 12.3$$

In the circuit of Fig. $(W/L)_1 = 10/0.18$ and $ID_1 = 0.5 \text{ mA}$.

- Q. (a) If $\lambda = 0$, determine $(W/L)_2$ such that M_1 operates at the edge of saturation.
 (b) Now calculate the voltage gain.
 (c) Explain why this choice of $(W/L)_2$ yields the maximum gain.



A. a) $I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2 \Rightarrow V_{GS1} = \sqrt{\frac{2ID}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} + V_{TH} = 0.3 + 0.4 = 0.7 \text{ V}$

at edge of saturation, $V_{DS1} = V_{GS1} - V_{TH} = 0.7 - 0.4 = 0.3 \text{ V}$

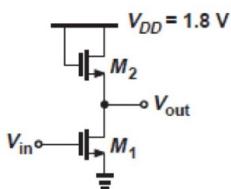
$$V_{DS1} = V_{D1} - V_{S1} \Rightarrow V_{D1} = 0.3 - 0 = 0.3 \text{ V}$$

$$V_{D1} = V_{S2} \Rightarrow V_{GS2} = V_{G2} - V_{S2} = 1.8 - 0.3 = 1.5 \text{ V} \Rightarrow \left(\frac{W}{L}\right)_2 = \frac{2ID}{\mu_n C_{ox} (V_{GS2} - V_{TH})^2} = 4.132$$

b) $A_v = \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} = 3.67$

c) minimum $\frac{W}{L}$ is req, cuz $A_v \propto \frac{1}{g_m}$. to get A_v max, we use a low $\left(\frac{W}{L}\right)_2$ value.

- Q** The CS stage of Fig. must achieve a voltage gain of 5. (a) If $(W/L)_2 = 2/0.18$, compute the required value of $(W/L)_1$.
 (b) What is the maximum allowable bias current if M_1 must operate in saturation?



$$A. \quad a) \quad \left(\frac{W}{L}\right)_2 = \frac{2}{0.18}$$

$$A_v = \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} \Rightarrow \left(\frac{W}{L}\right)_1 = A_v^2 \times \left(\frac{W}{L}\right)_2 = \frac{50}{0.18}$$

$$b) \quad I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2$$

$$= \frac{1}{2} \times 200 \times 10^{-6} \times \frac{2}{0.18} (1.8 - V_{S2} - 0.4)^2 = \frac{1}{900} (1.4 - V_{S2})^2 \rightarrow \textcircled{1}$$

$$\text{also, } I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2$$

$$= \frac{1}{2} \times 200 \times 10^{-6} \times \frac{50}{0.18} (V_{in} - 0.4)^2 = \frac{1}{36} (V_{in} - 0.4)^2 \rightarrow \textcircled{2}$$

$$\textcircled{1} = \textcircled{2}$$

$$\frac{1}{900} (1.4 - V_S)^2 = \frac{1}{36} (V_{in} - 0.4)^2 \Rightarrow (V_{in} - 0.4) = \frac{(1.4 - V_{S2})}{5}$$

$$V_{in} - V_{TH} = V_{DS1} \quad \text{and} \quad V_{S2} = V_{D1}$$

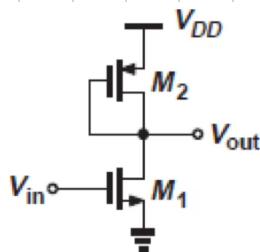
$$V_{DS1} = V_{D1} - V_{S1} = V_{D1}$$

$$\text{So, } 5 V_{DS1} = 1.4 - V_{DS1}$$

$$V_{DS1} = \frac{1.4}{6} = 0.233 \text{ V}$$

$$I_D = \frac{1}{900} (1.4 - 0.233)^2 = 1.51 \text{ mA}$$

Q. If $\lambda \neq 0$, Determine A_v



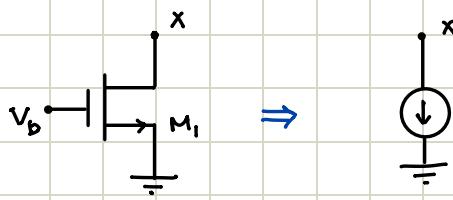
$$A. \quad A_v = -\frac{g_m_1}{g_m_2} = -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_1}{\mu_p \left(\frac{W}{L}\right)_2}}$$

$$I_D = \text{constant}, \quad \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

$$\Rightarrow \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} = \frac{|V_{GS2} - V_{TH2}|}{|V_{GS1} - V_{TH1}|} = A_v$$

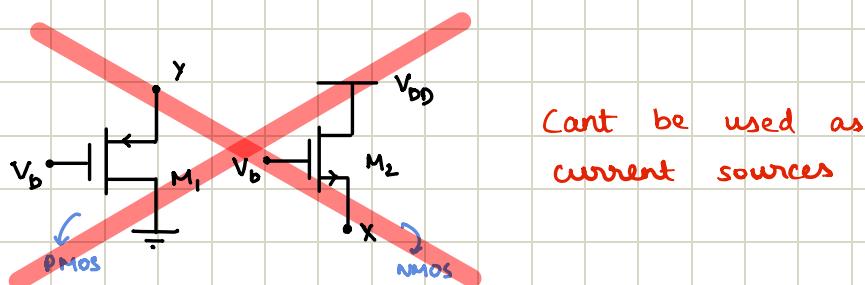
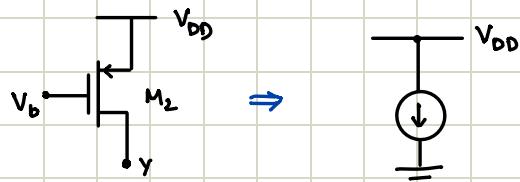
Realization of Current Sources

- MOSFETs in saturation act as current sources
- An NMOS serves as current source with i terminal grounded



→ A PMOS draws current from V_{DD} to y .

If $\lambda = 0$, currents remain independent of V_x or V_y



→ Common Source with current source load

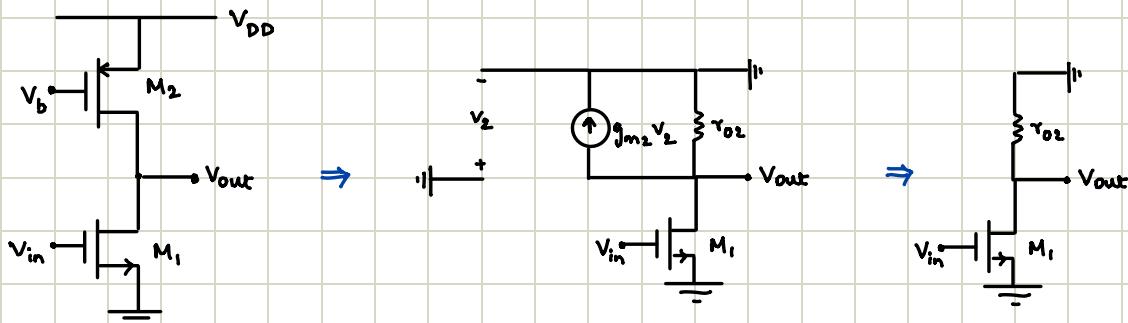
→ For large voltage gain in single stage,

$A_v = -g_m R_D \Rightarrow$ we must increase load impedance

→ With resistor or diode connected load, if we increase R_D ,

We have large voltage drop across the load, limiting the output voltage swing

→ Instead we replace load with a current source (Doesn't obey Ohm's law)

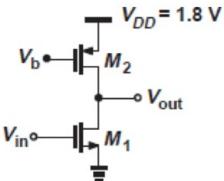


$$A_v = -g_m 1 (\tau_{o1} || \tau_{o2})$$

$$g_m 1 \tau_{o1} = \sqrt{2 \left(\frac{W}{L} \right)_1 M_n C_{ox} I_D} \times \frac{1}{\lambda I_D}$$

The CS stage of Fig. Must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1 \text{ V}^{-1}$, and $\lambda_2 = 0.15 \text{ V}^{-1}$. (a) Compute the required value of $(W/L)_1$. (b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_b .

Q.



A. a)

$$r_{o1} = \frac{1}{\lambda_1 I_D} = \frac{1}{0.1 \times 0.5 \times 10^{-3}} = 20 \text{ k}\Omega$$

$$r_{o2} = \frac{1}{\lambda_2 I_D} = \frac{1}{0.15 \times 0.5 \times 10^{-3}} = 13.33 \text{ k}\Omega$$

$$A_v = -g_m (r_{o1} || r_{o2}) \Rightarrow g_m = \frac{10}{8000} = 1.25 \times 10^{-3} \text{ S}$$

$$g_m = -\sqrt{2 \mu_n C_{ox} \left(\frac{w}{l}\right)_1 I_D} \Rightarrow \sqrt{2 \times 200 \times 10^{-6} \left(\frac{w}{l}\right)_1 \times 0.5 \times 10^{-3}} = 1.25 \times 10^{-3}$$

$$\left(\frac{w}{l}\right)_1 = 7.81$$

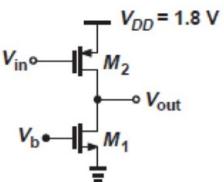
b) $V_{GS2} = V_{DD} - V_b$; $\left(\frac{w}{l}\right)_2 = \frac{20}{0.18}$

$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{w}{l}\right)_2 (V_{GS2} - V_{Th})^2 = \frac{1}{2} \mu_p C_{ox} \left(\frac{w}{l}\right)_2 (V_{DD} - V_b - V_{Th})^2$$

$$\begin{aligned} V_b &= V_{DD} - V_{Th} - \sqrt{\frac{2 I_D}{\mu_p C_{ox} \left(\frac{w}{l}\right)_2}} \\ &= 1.8 - 0.4 - \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{100 \times 10^{-6} \times \frac{20}{0.18}}} \\ &= 1.1 \text{ V} \end{aligned}$$

The CS stage depicted in Fig. Must achieve a voltage gain of 15 at a bias current of 0.5 mA. If $\lambda_1 = 0.15 \text{ V}^{-1}$ and $\lambda_2 = 0.05 \text{ V}^{-1}$, determine the required value of $(W/L)_2$.

Q.



A.

$$A_v = g_m (r_{o1} || r_{o2})$$

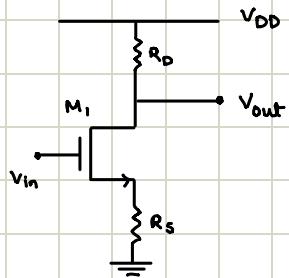
$$r_{o1} = \frac{1}{\lambda_1 I_D} = \frac{1}{0.15 \times 0.5 \times 10^{-3}} = 13.33 \text{ k}\Omega$$

$$r_{o2} = \frac{1}{\lambda_2 I_D} = \frac{1}{0.05 \times 0.5 \times 10^{-3}} = 40 \text{ k}\Omega$$

$$g_m = \frac{A_v}{r_{o1} || r_{o2}} = \frac{15}{10 \times 10^{-3}} = 1.5 \text{ ms}$$

$$g_m = -\sqrt{2 \mu_p C_{ox} \left(\frac{w}{l}\right)_2 I_D} \Rightarrow \left(\frac{w}{l}\right)_2 = \frac{g_m^2}{2 \mu_p C_{ox} I_D} = \frac{(1.5 \times 10^{-3})^2}{2 \times 100 \times 10^{-6} \times 0.5 \times 10^{-3}} = 22.5$$

→ Common Source Amplifier with source degeneration



$$V_{in} = V_{GS} + I_D R_S$$

$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

$$V_{DS} \geq V_{GS} - V_{TH}$$

$$V_{in} \uparrow \rightarrow V_{GS} \uparrow \rightarrow I_D \uparrow \rightarrow I_D R_S \uparrow \rightarrow V_{GS} \downarrow \rightarrow I_D \downarrow$$

→ As V_D increases, I_D increases, resulting more voltage drop across R_S & thus reduces V_{GS}

$$G_m = \left. \frac{I_{SC}}{V_{in}} \right|_{V_{out}=0} \Rightarrow \text{Therefore, } R_D = 0$$

→ We Know,

$$V_{out} = V_{DD} - I_D R_D$$

$$\text{and } \frac{\partial V_{out}}{\partial V_{in}} = 0 - \left(\frac{\partial I_D}{\partial V_{in}} \right) R_D$$

$$\text{We also know, } G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \cdot \frac{\partial V_{GS}}{\partial V_{in}}$$

$$\Rightarrow V_{GS} = V_{in} - I_D R_S$$

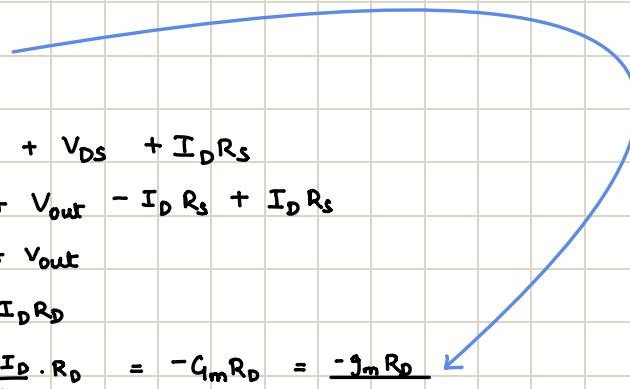
$$\frac{\partial V_{GS}}{\partial V_{in}} = 1 - \frac{\partial I_D}{\partial V_{in}} \cdot R_S \Rightarrow G_m = \frac{\partial f}{\partial V_{GS}} \left(1 - \frac{\partial I_D}{\partial V_{in}} R_S \right)$$

$$\text{So, } G_m = g_m - g_m G_m R_S \Rightarrow G_m (1 + g_m R_S) = g_m \Rightarrow G_m = \frac{g_m}{1 + g_m R_S}$$

$$\Rightarrow A_V = -g_m R_L$$

$$= -G_m R_D$$

$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$



$$\begin{aligned} \text{Also, } V_{DD} &= I_D R_D + V_{DS} + I_D R_S \\ &= I_D R_D + V_{out} - I_D R_S + I_D R_S \\ &= I_D R_D + V_{out} \end{aligned}$$

$$\Rightarrow V_{out} = V_{DD} - I_D R_D$$

$$\frac{\partial V_{out}}{\partial V_{in}} = 0 - \frac{\partial I_D}{\partial V_{in}} \cdot R_D = -G_m R_D = \frac{-g_m R_D}{1 + g_m R_S}$$

$$G_m = \frac{g_m}{1 + g_m R_S} = \frac{1}{\frac{1}{g_m} + R_S} \approx \frac{1}{R_S} \quad (R_S \gg \frac{1}{g_m})$$

Q. Prove that Input & Output current relation in common source amplifier with degeneration is linear.

A. $G_m = \frac{g_m}{1 + g_m R_s} = \frac{1}{\frac{1}{g_m} + R_s} \approx \frac{1}{R_s}$

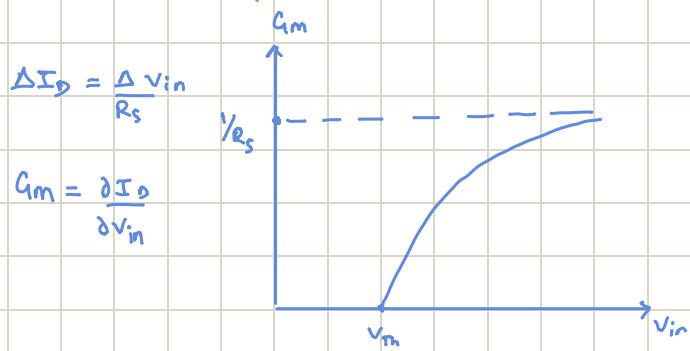
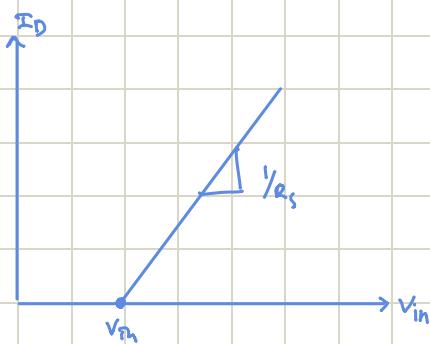
By keeping R_s high, compound to $\frac{1}{g_m}$, we get drain current as a linearised function of input voltage, but

$$A_v = \frac{-g_m R_D}{1 + g_m R_s} = \frac{-R_D}{\frac{1}{g_m} + R_s} \approx -\frac{R_D}{R_s}$$

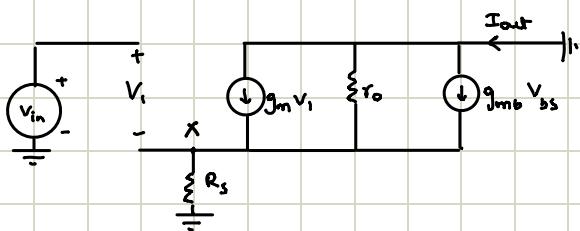
If $R_s \uparrow \Rightarrow A_v \uparrow$, so $A_v \propto g_m$

Q. Plot I_D v/s v_{in} and G_m v/s v_{in} for C.S Amplifier with Degeneration

A.



→ Small signal gain with Body effect & Channel Length Modulation



$$\begin{aligned} \Rightarrow I_{out} &= g_m v_i - g_{mb} v_x - \frac{I_{out} R_s}{R_o} \\ &= g_m (v_{in} - I_{out} R_s) + g_{mb} (-I_{out} R_s) - \frac{I_{out} R_s}{R_o} \end{aligned}$$

$$A_v = -G_m R_D$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m R_o}{R_s + [1 + (g_m + g_{mb}) R_s] R_o} = \frac{g_m}{1 + g_m R_s + g_{mb} R_s + \frac{R_s}{R_o}}$$

$$\Rightarrow I_x - (g_m + g_{mb}) v_i = I_x + (g_m + g_{mb}) R_s I_x$$

$$R_o [I_x + (g_m + g_{mb}) R_s I_x] + I_x R_s = v_x$$

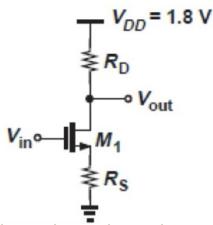
$$\begin{aligned} R_{out} &= [1 + (g_m + g_{mb}) R_s] R_o + R_s \\ &= [1 + (g_m + g_{mb}) R_s] R_o + R_o \end{aligned}$$

$$\text{If } (g_m + g_{mb}) R_o \gg 1$$

$$R_{out} = (g_m + g_{mb}) R_o + R_o$$

$$R_{out} = R_o [1 + (g_m + g_{mb}) R_s]$$

- Q.** In the circuit of Fig. determine the gate voltage such that M1 operates at the edge of saturation. Assume $\lambda = 0$. Bias current = 1mA. $V_{RS} = 200\text{mV}$
- If $R_D = 1\text{k}\Omega$ determine the required value of W/L . Does the transistor operate in saturation for this choice of W/L ?
 - If $W/L = 50/0.18$, determine the required value of R_D . Does the transistor operate in saturation for this choice of R_D ?



A. a) $|A_v| = \frac{g_m R_D}{1 + g_m R_S} \Rightarrow |A_v| = \frac{R_D}{\frac{1}{g_m} + R_S} \Rightarrow 4 = \frac{1000}{\frac{1}{g_m} + \frac{200 \times 10^{-3}}{1 \times 10^{-3}}} \Rightarrow g_m = \frac{1}{50} = 20\text{mS}$

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} \Rightarrow \frac{W}{L} = \frac{g_m^2}{2 I_D \mu_n C_{ox}} = \frac{(20 \times 10^{-3})^2}{2 \times 1 \times 10^{-3} \times 200 \times 10^{-6}} = 10^3$$

To check if in saturation or not,

$$V_{DS} = V_D - V_S = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2$$

$$= V_{DD} - I_D R_D - V_S$$

$$= 1.8 - (10^3 \times 10^3) - 0.2$$

$$= 0.6\text{ V}$$

$$V_{GS} - V_{Th} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}} = \sqrt{\frac{2 \times 10^{-3}}{200 \times 10^{-6} \times 10^3}} = 0.1$$

$$V_{DS} > V_{GS} - V_{Th} \Rightarrow \text{Saturation}$$

b) $\frac{W}{L} = \frac{50}{0.18}$

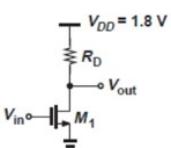
$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}} = \sqrt{2 \times 10^{-3} \times 200 \times 10^{-6} \times \frac{50}{0.18}} = 10.5\text{mS}$$

$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S} \Rightarrow 4 \left(\frac{1}{10.5 \times 10^{-3}} + 200 \right) = 1181\Omega$$

$$V_{DS} = V_D - V_S = (V_{DD} - I_D R_D) - V_{RS} = (1.8 - (10^3 \times 1181)) - 0.2 = 0.421$$

$$V_{DS} > V_{GS} - V_{Th} \Rightarrow \text{Saturation}$$

- The CS stage of Fig. carries a bias current of 1mA. If $R_D = 1\text{k}\Omega$ and $\lambda = 0.1\text{V}^{-1}$, Compute the required value of W/L for a gate voltage of 1V. What is the voltage gain of the circuit?



A. $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS})$

$$\frac{W}{L} = \frac{2 I_D}{\mu_n C_{ox} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS})} = \frac{2 \times 10^{-3}}{200 \times 10^{-6} (1 - 0.4)^2 (1 + 0.1 \times 0.8)} = 25.72$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th}) (1 + \lambda V_{DS}) = 200 \times 10^{-6} \times 25.72 \times (1 - 0.4) (1 + 0.1 \times 0.8) = 3.33\text{ mS}$$

$$A_v = -g_m R_D = -3.33$$

Q. The common-gate stage shown in Fig. must provide a voltage gain of 4 and an input impedance of 50 ohm. If $I_D = 0.5 \text{ mA}$, and $\lambda = 0$, determine the values of R_D and W/L .

A. $A_v = 4 \quad R_{in} = 50 \Omega \quad I_D = 0.5 \text{ mA}$

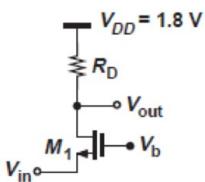
$$R_{in} = \frac{1}{g_m + g_{mb}} \quad \text{but since } \lambda = 0, g_{mb} = 0$$

$$R_{in} = \frac{1}{g_m} \Rightarrow g_m = \frac{1}{50} = 0.02 \text{ S}$$

$$A_v = g_m R_D \Rightarrow R_D = \frac{4}{0.02} = 200 \Omega$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \Rightarrow \frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = \frac{(0.02)^2}{2 \times 200 \times 10^{-6} \times 0.5 \times 10^{-3}} = 2000$$

Suppose in Fig. $I_D = 0.5 \text{ mA}$, $\lambda = 0$, and $V_b = 1 \text{ V}$. Determine the values of W/L and R_D for an input impedance of 50 ohm and maximum voltage gain (while M_1 remains in saturation).



A. $g_m = \frac{1}{R_{in}} = \frac{1}{50} = 0.02 \text{ S}$

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}} \Rightarrow \frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = \frac{(0.02)^2}{2 \times 200 \times 10^{-6} \times 0.5 \times 10^{-3}} = 2000$$

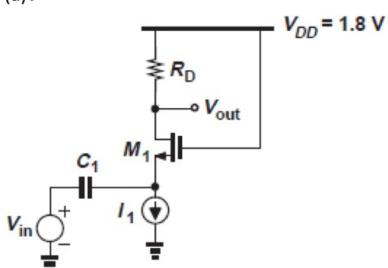
$$V_{Dmin} = V_g - V_{Th} = V_b - V_{Th} = 1 - 0.4 = 0.6 \text{ V}$$

$$R_{Dmax} = \frac{V_{DD} - I_D R_D}{I_D} = \frac{V_{DD} - V_{Dmin}}{I_D} = \frac{1.8 - 0.6}{0.5 \times 10^{-3}} = 2.4 \text{ k}\Omega$$

$$A_v = g_m R_D = 0.02 \times 2400 = 48$$

The CG amplifier shown in Fig. is biased by means of $I_1 = 1 \text{ mA}$. Assume $\lambda = 0$ and C_1 is very large.

- (a) What value of R_D places the transistor M_1 100 mV away from the triode region?
- (b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?

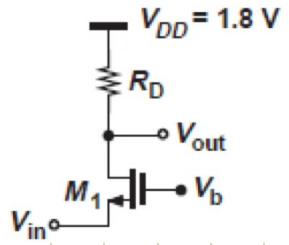


A. a) $V_D = V_g - V_{Th} + 100 \text{ mV} = 1.8 - 0.4 + 0.1 = 1.5 \text{ V}$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1.8 - 1.5}{1 \text{ mA}} = 300 \Omega$$

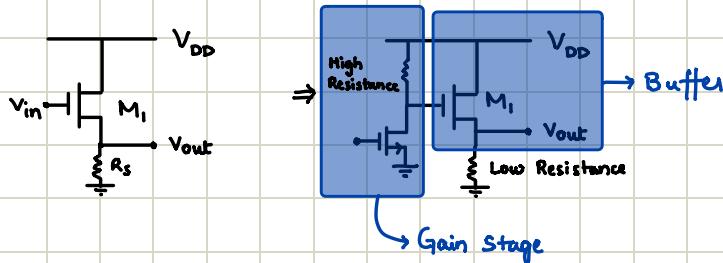
b) $A_v = g_m R_D \Rightarrow g_m = \frac{5}{300}$

$$\frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = \frac{25}{90000 \times 2 \times 200 \times 10^{-6} \times 10^{-3}} = 694.44$$



→ Common Drain Amplifier (Source Follower)

- Load Impedance should be as high as possible will violate the condition for Ideal amplifier. There will be reduction in voltage gain.
- To avoid this condition, connect voltage buffer after amplifier which is having output impedance. The Common Drain Amplifier acts as buffer.



$$\rightarrow V_{out} = \frac{1}{2} M_n C_{ox} \frac{W}{L} (V_{in} - V_{Th} - V_{out})^2 R_s$$

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \frac{1}{2} M_n C_{ox} \frac{W}{L} \times 2(V_{in} - V_{Th} - V_{out}) \left(1 - \frac{\partial V_{Th}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}} \right)$$

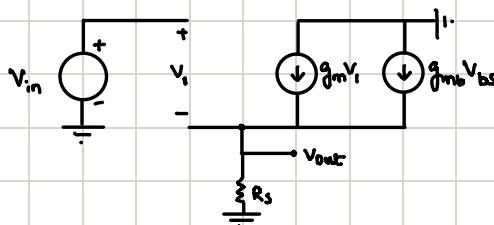
$$= M_n C_{ox} \frac{W}{L} (V_{in} - V_{out} - V_{Th}) \left(1 - \eta \frac{\partial V_{out}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}} \right)$$

$$= \frac{\partial V_{out}}{\partial V_{in}} \left(1 + M_n C_{ox} \frac{W}{L} R (V_{in} - V_{out} - V_{Th}) \right) + \eta M_n C_{ox} \frac{W}{L} R_s (V_{in} - V_{out} - V_{Th})$$

$$= \frac{\partial V_{out}}{\partial V_{in}} (1 + g_m R_s + \eta g_m R_s) = g_m R_s$$

$$\eta = \frac{g_{mb}}{g_m} \Rightarrow A_v = \frac{g_m R_s}{1 + g_m R_s (1 + \frac{g_{mb}}{g_m})} = \frac{g_m R_s}{1 + g_m R_s + g_{mb} R_s} = \frac{g_m R_s}{1 + (g_m + g_{mb}) R_s}$$

→ Small signal model ⇒



$$V_{out} = (g_m V_i + g_{mb} V_{bs}) R_s$$

$$V_{in} - V_{out} = V_i \quad ; \quad V_{bs} = -V_{out}$$

$$V_{out} = (g_m (V_{in} - V_{out}) + g_{mb} (-V_{out})) R_s$$

$$V_{out} (1 + (g_m + g_{mb}) R_s) = g_m V_{in} R_s$$

$$\text{So, } \frac{V_{out}}{V_{in}} = \frac{g_m R_s}{1 + (g_m + g_{mb}) R_s}$$

→ Output Resistance

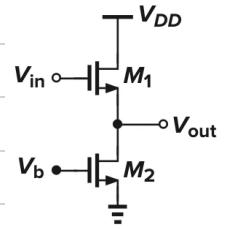
$$V_i = V_{bs} = -V_x$$

$$\text{by KCL at } X, \quad I_X - g_m V_x - g_{mb} V_x = 0 \Rightarrow R_{out} = \frac{V_x}{I_X} = \frac{1}{g_m + g_{mb}}$$

Q. Suppose that in the source follower of Fig. 3.37(a), $(W/L)_1 = 20/0.5$, $I_1 = 200 \mu\text{A}$, $V_{TH0} = 0.6 \text{ V}$, $2\Phi_F = 0.7 \text{ V}$, $V_{DD} = 1.2 \text{ V}$, $\mu_n C_{ox} = 50 \mu\text{A/V}^2$, and $\gamma = 0.4 \text{ V}^{1/2}$.

(a) Calculate V_{out} for $V_{in} = 1.2 \text{ V}$.

(b) If I_1 is implemented as M_2 in Fig. 3.37(b), find the minimum value of $(W/L)_2$ for which M_2 remains saturated when $V_{in} = 1.2 \text{ V}$.



$$A. a) I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Th})^2$$

$$V_{GS1} = V_{in} - V_{out}$$

$$\begin{aligned} V_{out} &= V_{in} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} - V_{Th} \\ &= 1.2 - \sqrt{\frac{2 \times 200 \times 10^{-6}}{50 \times 10^{-6} \times \frac{20}{0.5}}} - 0.6 = 0.153 \text{ V} \end{aligned}$$

$$\begin{aligned} V_{Th} &= V_{Th0} + \gamma \left(\sqrt{2\Phi_F + V_{GS}} - \sqrt{2\Phi_F} \right) \\ &= 0.6 + 0.4 \left(\sqrt{0.7 + 0.153} - \sqrt{0.7} \right) \\ &= 0.635 \text{ V} \end{aligned}$$

So, V_{out} is 35 mV less than calculated value $\Rightarrow V_{out} = 0.153 - 0.035$
 $= 0.118 \text{ V}$

$$b) V_{DS2} = 0.118 \text{ V}$$

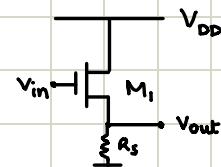
$$I_D = 200 \mu\text{A}$$

$$(V_{GS} - V_{Th})_2 \leq 0.118 \text{ V}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_{Th})_2^2$$

$$\left(\frac{W}{L}\right)_2 \geq \frac{2I_D}{\mu_n C_{ox} (V_{GS} - V_{Th})_2^2} = \frac{2 \times 200 \times 10^{-6}}{50 \times 10^{-6} \times (0.118)^2} = 574$$

Q. For the source follower with $(W/L) = 360$, $R_s = 50 \text{ ohm}$, power budget of 20mW. Find voltage gain ? assume $V_{DD} = 2 \text{ V}$ and $\gamma = 0$.



$$A. P = I_D V_{DD}$$

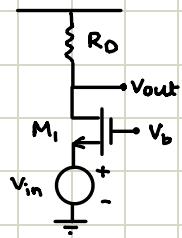
$$I_D = \frac{20 \times 10^{-3}}{2} = 0.01 \text{ A}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2$$

$$g_m = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} = \sqrt{2 \times 0.01 \times 200 \times 10^{-6} \times 360} = 0.038 \text{ s}$$

$$A_v = g_m R_s = 0.038 \times 50 = 1.9$$

→ Common Gate Amplifier



$$V_{out} = V_{DD} - I_D R_D$$

- A CG stage sense input at source & produces output at drain
- Gate is biased to establish proper operating conditions

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th})^2$$

$$V_{DD} - I_D R_D = V_b - V_{Th} \Rightarrow V_D - \frac{R_D}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th})^2 = V_b - V_{Th} = V_{out}$$

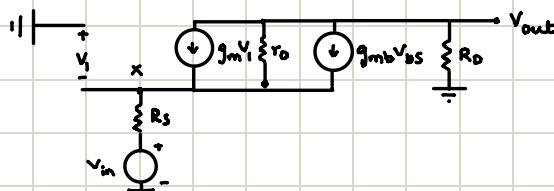
$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th}) \left(-1 - \frac{\partial V_{Th}}{\partial V_{in}} \right) R_D$$

Since $\frac{\partial V_{Th}}{\partial V_{in}} = \frac{\partial V_{Th}}{\partial V_{SB}} = \eta$,

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} R_D (V_b - V_{in} - V_{Th}) (1 + \eta)$$

$$A_v = g_m (1 + \eta) R_D$$

→ Small Signal Model ⇒



$$\text{Current through } R_s = -\frac{V_{out}}{R_D} \Rightarrow V_i - \frac{V_{out} R_s}{R_D} + V_{in} = 0$$

$$\begin{aligned} \text{Current through } r_o &= r_o \left(-\frac{V_{out}}{R_D} - g_m V_i - g_{mb} V_i \right) - \frac{V_{out} R_s}{R_D} + V_{in} = V_{out} \\ &\Rightarrow r_o \left[-\frac{V_{out}}{R_D} - (g_m + g_{mb}) \left(V_{out} \frac{R_s}{R_D} - V_{in} \right) \right] - \frac{V_{out} R_s}{R_D} + V_{in} = V_{out} \end{aligned}$$

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb}) r_o + 1}{r_o + (g_m + g_{mb}) r_o R_s + R_s + R_D} R_D$$

→ Input Impedance ⇒ We know $V_i = -V_x$

$$\begin{aligned} \text{Current through } r_o &\Rightarrow I_x + g_m V_i + g_{mb} V_i \\ &= I_x - (g_m + g_{mb}) V_x \end{aligned}$$

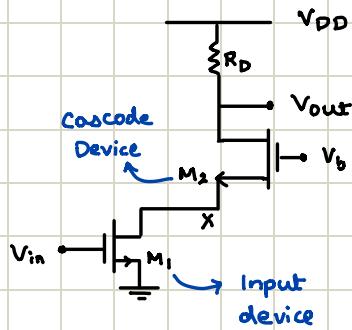
$$\text{Voltage across } r_o \& R_D \Rightarrow R_D I_x + r_o [I_x - (g_m + g_{mb}) V_x] = V_x$$

$$\frac{V_x}{I_x} = \frac{R_D + r_o}{1 + (g_m + g_{mb}) r_o} \approx \frac{R_D + r_o}{(g_{mb} + g_m) r_o}$$

→ Output Impedance ⇒ $R_{out} = \{ [1 + (g_m + g_{mb}) r_o] R_s + r_o \} || R_D$

Cascode Amplifier

- The cascade of CS stage & a CG stage is called 'cascode'
- In CS amplifier, transistor converts input voltage to a current signal & in CG amplifier, input signal drives the source current of the amplifier so we can cascade CS & CG



Cascode Stage : Bias Conditions

- i) For M_1 to be in saturation $\Rightarrow V_x \geq V_{in} - V_{Th2}$
- ii) If M_1 & M_2 both are in saturation, M_2 operates as source follower & V_x is primarily determined by V_b $\Rightarrow V_x = V_b - V_{GS2}$

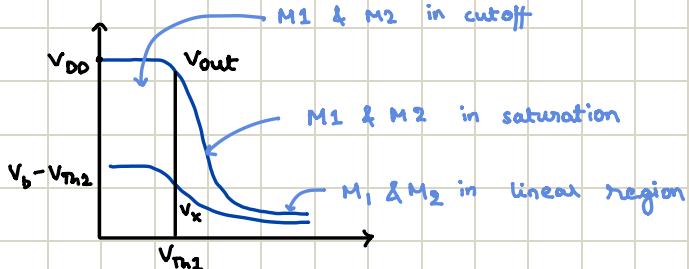
$$\text{So, } V_b - V_{GS2} \geq V_{in} - V_{Th2} \Rightarrow V_b > V_{in} + V_{GS2} - V_{Th2}$$

$$\text{For } M_2 \text{ to be saturated} \Rightarrow V_{out} \geq V_b - V_{Th2}$$

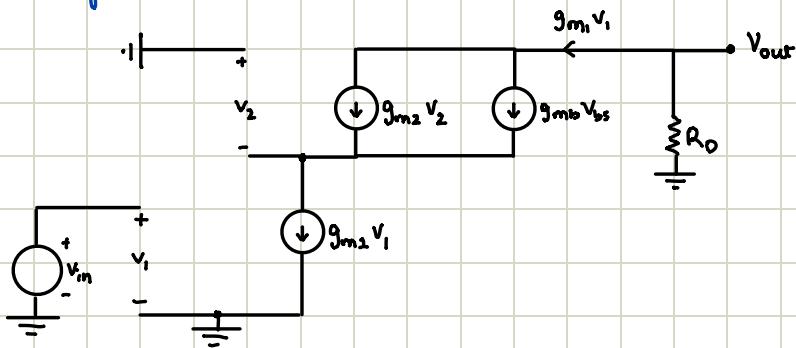
$$\begin{aligned} \text{So, } V_{out} &\geq V_{in} - V_{Th1} + V_{GS2} - V_{Th2} \\ &= (V_{GS2} - V_{Th2}) + (V_{GS2} - V_{Th2}) \end{aligned}$$

→ Minimum output level for both transistors in saturation = sum of overdrives of M_1 & M_2

Input Output Characteristics



→ Small signal characteristics



→ Assume both MOSFETs in saturation & $\lambda = 0$

$$A_v = \frac{V_{out}}{V_{in}}$$

$$V_{out} = -g_m V_1 (R'_D \parallel R_D)$$

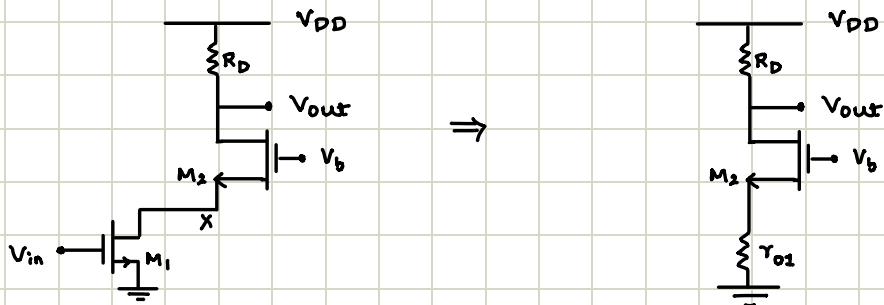
$$= -g_m V_{in} (R'_D \parallel R_D)$$

$$\frac{V_{out}}{V_{in}} = -g_m (R'_D \parallel R_D) = A_v$$

→ Independent of g_m & body effect of M_2

→ Output Impedance

→ Cascode Amplifier has high output impedance



→ Circuit can be viewed as common-source stage with degeneration resistor $= r_{o2}$ for calculating R_{out}

$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o2} + r_{o2}$$

Assuming $g_m r_o \gg 1$, $R_{out} = (g_{m2} + g_{mb2}) r_{o2} r_{o2}$

→ M_2 boosts output impedance of M_1 by factor of $(g_{m2} + g_{mb2}) r_{o2}$

Frequency Response of Amplifiers

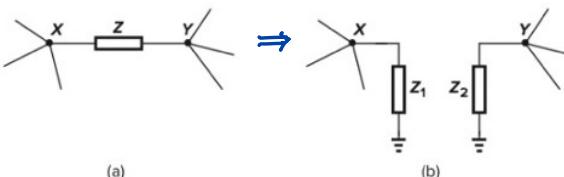
→ Miller's Effect

→ If a 2 terminal impedance is connected b/w 2 nodes, it can be splitted as input side & output side impedance

$$\hookrightarrow z_1 = \frac{z}{1 - A_v}$$

$$\hookrightarrow z_2 = \frac{z}{1 - \frac{1}{A_v}}$$

$$\text{where } A_v = \frac{V_y}{V_x}$$



Proof:

$$\text{Current through } z = \frac{V_x - V_y}{z}$$

For the 2 circuits to be equal, same current flows through z_1

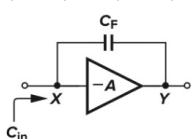
$$\text{So, } \frac{V_x - V_y}{z} = \frac{V_x}{z_1}$$

$$1 - \frac{V_y}{V_x} = \frac{z}{z_1} \Rightarrow z_1 = \frac{z}{1 - \frac{V_y}{V_x}} = \frac{z}{1 - A_v}$$

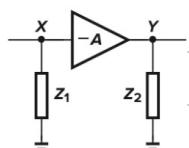
$$\text{Similarly, } \frac{V_y - V_x}{z} = \frac{V_y}{z_2}$$

$$1 - \frac{V_x}{V_y} = \frac{z}{z_2} \Rightarrow z_2 = \frac{z}{1 - \frac{V_x}{V_y}} = \frac{z}{1 - A_v^{-1}}$$

Q. Consider the following circuit, where voltage amplifier has negative gain = $-A$ & is otherwise ideal. $C_{in} = ?$



A. Upon applying miller's effect,



$$z = \frac{1}{C_F s}$$

$$z_1 = \frac{1/C_F s}{1 + A}$$

$$= \frac{1}{C_F s(1+A)}$$

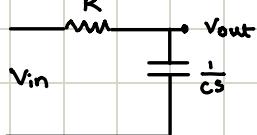
$$z = \frac{1}{C_s}$$

$$C_{in} = C_F (1+A)$$

$$z_2 = \frac{1/C_F s}{1 + \frac{1}{A}}$$

$$= \frac{1}{C_F s(1+\frac{1}{A})}$$

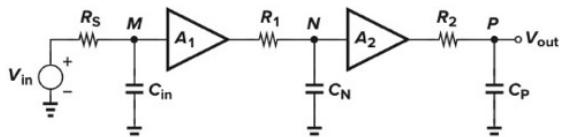
Transfer Function of RC Circuit



$$V_{out}(s) = \frac{V_{in}(s) \times \frac{1}{Cs}}{R + \frac{1}{Cs}}$$

$$\frac{V_{out}(s)}{V_{in}} = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{\frac{1}{Cs}}{\frac{R + \frac{1}{Cs}}{Cs}} = \frac{1}{1 + Rcs} = \frac{1}{1 + \frac{s}{\omega}}$$

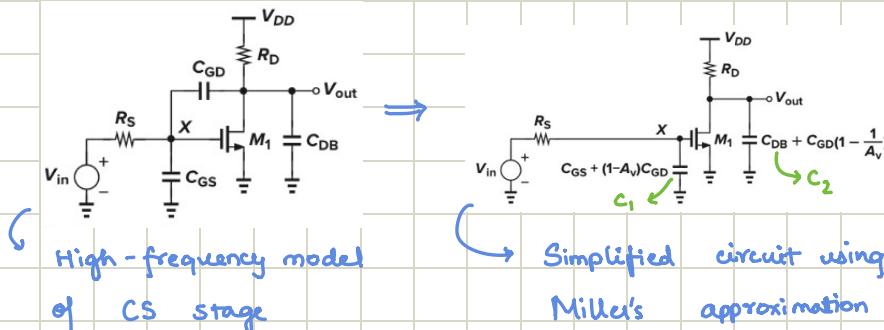
Association of Poles with nodes



$$\frac{V_{out}(s)}{V_{in}} = \frac{A_1}{1 + R_s C_{in}s} \cdot \frac{A_2}{1 + R_1 C_N s} \cdot \frac{1}{1 + R_2 C_P s}$$

Miller's Approximation

→ Assuming $\lambda=0$ & M1 operates in saturation



$$C_1 = C_{GS} + (1 - A_v) C_{GD}$$

$$C_2 = C_{DB} + (1 - \frac{1}{A_v}) C_{DO}$$

$$C_2 = C_{DB} + C_{GD}$$

$(A_v \gg 1)$

$$\omega = \frac{1}{RC}$$

$$\omega_{in} = \frac{1}{R_s C_1}$$

$$\omega_{out} = \frac{1}{R_D C_2}$$

$$\omega_{in} = \frac{1}{R_s [C_{GS} + (1 + g_m R_D) C_{GD}]}$$

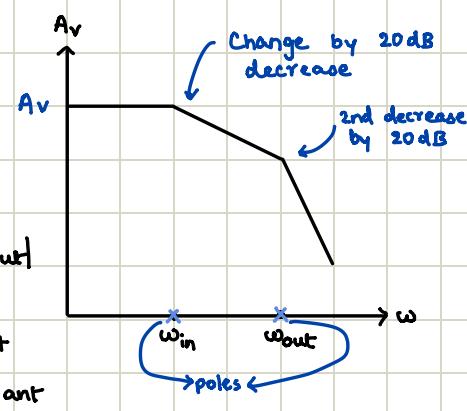
$$\& \omega_{out} = \frac{1}{R_D (C_{DB} + C_{GD})}$$

$$\frac{V_{out}(s)}{V_{in}} = \frac{-g_m R_D}{\left(1 + \frac{s}{\omega_{in}}\right)\left(1 + \frac{s}{\omega_{out}}\right)}$$

zeros = 0
poles = 2

$$\text{then } \Rightarrow 1 + \frac{s}{\omega_{in}} = 0 \Rightarrow s = -\omega_{in} \quad |-\omega_{in}| \& |-\omega_{out}|$$

$$1 + \frac{s}{\omega_{out}} = 0 \Rightarrow s = -\omega_{out} \quad \text{Consider the values to plot on 1st quadrant}$$



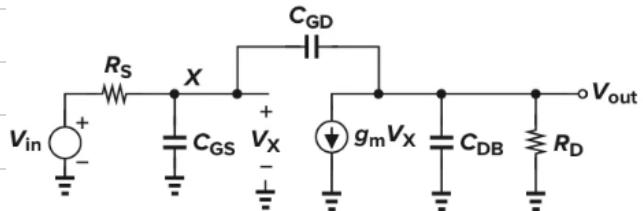
Problem of Miller Approximation

- The primary error is that we haven't considered existence of zeros in the circuit
- Another concern stems from approximating gain of amplifier by $-g_m R_D$
- But in reality, gain varies with frequency

Direct Analysis

- We obtain exact transfer function using small signal model

$$V_X = \frac{-V_{out} (C_{GD}s + \frac{1}{R_D} + C_{DB}s)}{g_m - C_{GD}s}$$



Apply KCL at input side, (Node X)

$$\frac{V_X - V_{in}}{R_s} + V_X C_{GS} + (V_X - V_{out}) C_{GD}s = 0 \quad \rightarrow ①$$

$$(V_{out} - V_X) C_{GD}s + \frac{V_{out}}{R_D} + V_{out} C_{DB}s + g_m V_X = 0$$

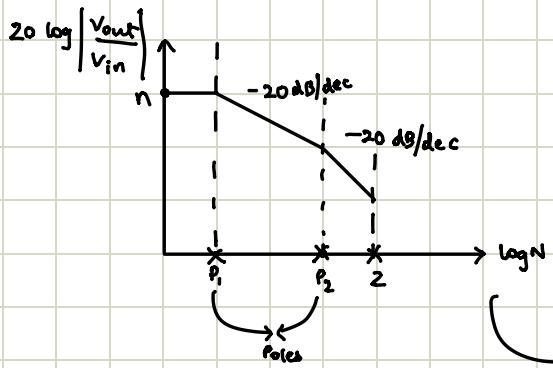
From this, $V_X = \frac{-V_{out} (C_{GD}s + C_{DS}s + \frac{1}{R_D})}{g_m - C_{GD}s}$

(Substitute in ①)

$$-V_{out} \left(\frac{R_s^{-1} + (C_{GS} + C_{GD})s}{g_m - C_{GD}s} \right) \left(\frac{R_D^{-1} + (C_{GD} + C_{DB})s}{g_m - C_{GD}s} \right) - V_{out} C_{GD}s = \frac{V_{in}}{R_s}$$

$$\frac{V_{out}(s)}{V_{in}} = \frac{(C_{GD}s - g_m) R_D}{R_s R_D s^2 + [R_s(1 + g_m R_D) C_{GD} + R_s C_{GS} + R_D(C_{GD} + C_{DB})]s + 1}$$

$$\epsilon = C_{GS} C_{GD} + C_{GS} C_{DB} + C_{GD} C_{DB}$$



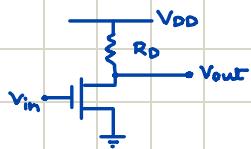
Bode plot is the plot b/w magnitude & phase wrt frequency

Cutoff Frequency

- Any frequency that changes the gain of the amplifier

Amplifier

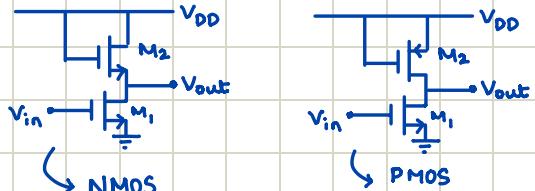
Common Source with resistive load



$$A_v = -g_m R_D \quad (\text{or}) \quad A_v = -g_m R_{out} = -g_m (r_o || R_D)$$

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -\sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} \cdot \frac{V_{DD}}{R_D}$$

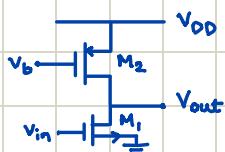
Common Source with Diode connected load



$$\text{NMOS, } A_v = \frac{-g_{m1}}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}} \left(\frac{1}{1 + \gamma} \right) = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cdot \frac{1}{1 + \gamma}$$

$$\text{PMOS, } A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} \quad (\text{no body effect for PMOS}) \\ = \frac{|V_{GS2} - V_{th2}|}{V_{GS1} - V_{th1}}$$

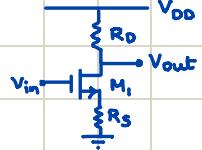
Common Source with Current Source Load



$$A_v = -g_{m1} (r_o || r_{o2})$$

$$g_{m1} r_{o1} = \sqrt{2 \left(\frac{W}{L} \right)_1 \mu_n C_{ox} \frac{I_D}{\lambda I_D}} \times \frac{1}{\lambda I_D}$$

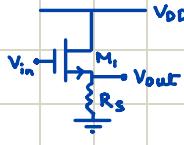
Common Source with Source Degeneration



$$g_m = \frac{g_m}{1 + g_m R_s}$$

$$A_v = -g_m R_D = \frac{-g_m R_D}{1 + g_m R_s} = \frac{-R_D}{g_m^{-1} + R_s}$$

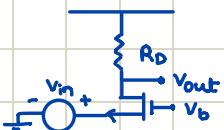
Source Follower (Common Drain)



$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th} - V_{out}) ; \quad R_{out} = \frac{1}{g_m} || \frac{1}{g_{mb}}$$

$$A_v = \frac{g_m R_s}{1 + (g_m + g_{mb}) R_s} ; \quad A_v = \frac{1}{\frac{1}{g_m} + \frac{1}{g_{mb}}} = \frac{g_m}{g_{mb} + g_m}$$

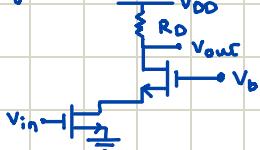
Common Gate Stage



$$A_v = g_m (1 + \gamma) R_D \quad (\text{higher than CS amplifier})$$

$$R_{in} = \frac{V_x}{I_x} = \frac{1}{\frac{1}{r_o} + g_m + g_{mb}} ; \quad R_{out} = \left\{ [1 + (g_m + g_{mb}) r_o] R_s + r_o \right\} || R_D$$

Cascode Stage



$$A_v = -g_m R_{out}$$

$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2} \\ \approx (g_{m2} + g_{mb2}) r_{o2} r_{o1} + r_{o2}$$