

# DIFFERENTIAL AMPLIFIERS AND CURRENT MIRRORS

## Current Mirrors

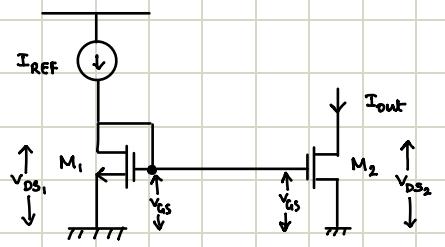
→  $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{V_{DD} R_i}{R_i + R_2} - V_{Th} \right)$  in a voltage divider bias circuit

$I_D$  depends on  $\mu_n$ ,  $V_{DD}$  &  $V_{Th}$  if temperature changes

To overcome this, we use **Current Mirror**!

→ We assume some  $I_{REF}$  which is constant current source (**Golden Reference**) and we copy this current

→ Normally, if the cause is  $V_{GS}$ , the effect is  $I_D$  (Change in  $V_{GS}$  causes change in  $I_D$ )  
But now, the cause is  $I_D$ , the effect is  $V_{GS}$  (Change in  $I_D$  causes change in  $V_{GS}$ )



Basic Current Mirror

$$V_{GS1} = V_{GS2}$$

$$I_{out} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{Th})^2$$

$$I_{REF} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{Th})^2$$

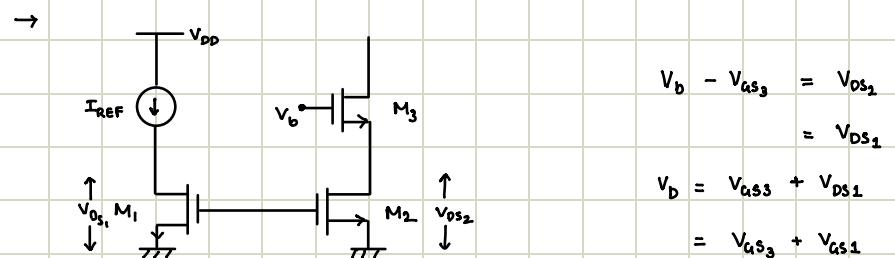
$$I_{out} = \frac{\left( \frac{W}{L} \right)_2}{\left( \frac{W}{L} \right)_1} \cdot I_{REF} \Rightarrow I_{out} \text{ only depends on } I_{REF} \text{ & } \left( \frac{W}{L} \right) \text{ ratios}$$

→ But this doesn't guarantee that  $I_{out} = \frac{\left( \frac{W}{L} \right)_2}{\left( \frac{W}{L} \right)_1} \cdot I_{REF}$  because,  $I_D$  depends on  $V_{DS}$  as well.

We only are sure  $V_{GS1} = V_{GS2}$  but not  $V_{DS1} = V_{DS2}$  and hence use only for simple applications.

→ To overcome this issue, we use **Cascade Current Mirror**

## Cascade Current Mirrors

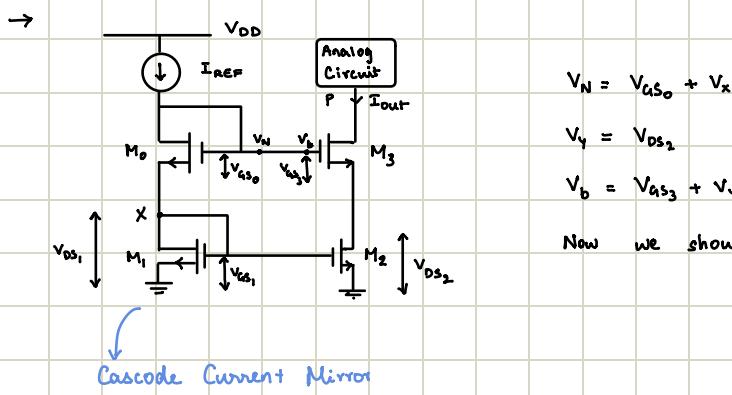


$$V_b - V_{GS3} = V_{DS2}$$

$= V_{DS1}$  ( $V_{DS1}$  should be equal to  $V_{DS2}$ )

$$V_b = V_{GS3} + V_{DS2}$$

$$= V_{GS3} + V_{DS1} \quad (V_{GS1} = V_{GS2})$$



$$V_N = V_{GS0} + V_x$$

$$V_y = V_{DS2}$$

$$V_b = V_{GS3} + V_y$$

Now we should make  $V_N = V_b$

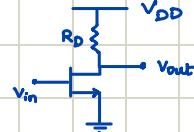
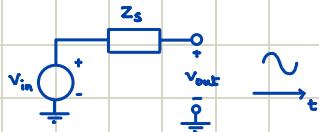
$$V_{GS0} + V_x = V_{GS3} + V_y$$

$$V_x = V_y \quad (V_{GS0} = V_{GS3})$$

Then  $V_{DS1} = V_{DS2} \quad (V_x = V_y)$

## Single Ended and Differential Operation

→ "Single ended signal" is one that is measured wrt fixed potential (usually ground)

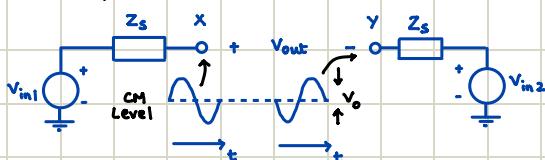


ex: CS Amplifier

⇒ If each single ended output has a peak amplitude voltage of  $V_0$ , then single ended peak-to-peak voltage is  $2V_0$

→ "Differential signal" is one that is measured b/w 2 nodes that have equal & opp. signal excursions around fixed potential

ex: Operational Amplifier



↳  $V_{in1}$  &  $V_{in2}$  are out of phase

→ If each single-ended output has peak amplitude of  $V_0$

Then, single-ended peak-to-peak swing is  $2V_0$

& differential peak-to-peak swing is  $4V_0$

→ The "center" potential in differential signaling is called **common mode**

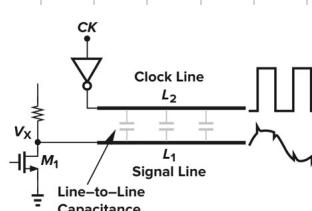
↳ Bias value

$$\begin{aligned} V_{out} &= V_x - V_y \\ V_{in1} &= V_0 \sin \omega t + V_{CM} \\ V_{in2} &= -V_0 \sin \omega t + V_{CM} \\ V_{out} &= V_{in2} - V_{in1} \\ &= 2V_0 \sin \omega t \\ V_{out} &= 2(2V_0 \sin \omega t) = 4V_0 \sin \omega t \\ \text{Max } V_{out} &= 4V_0 \end{aligned}$$

## Advantages of Differential Operation

→ Higher immunity to environmental noise

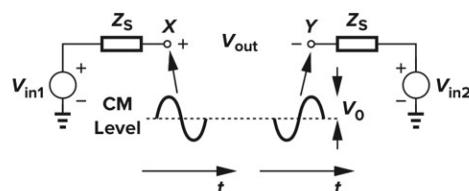
So for example, take a system where 2 adjacent lines in a circuit carry small sensitive signal & large clock waveform, & due to capacitive coupling b/w lines, transition on  $L_2$  corrupts signal on  $L_1$



$$\begin{aligned} V_{in1} &= V_{in1} + V_{noise} \\ V_{in2} &= V_{in2} + V_{noise} \\ V_d &= V_{in1} + V_{noise} - (V_{in2} + V_{noise}) \\ V_d &= V_{in1} - V_{in2} \end{aligned}$$

→ But in another case, sensitive signal is distributed as 2 equal & opposite phases so if clock line is placed at midway b/w the two, transitions disturb differential phases by equal amounts, leaving difference intact called **CM rejection**

Even though Common-mode level of 2 phases is disturbed, differential output isn't corrupted



→ CM rejection also occurs with noisy supply voltages

In CS Stage,

$\rightarrow V_{DD}$  varies by  $\Delta V$

$$V_{DD} = V_{DD} \pm \Delta V$$

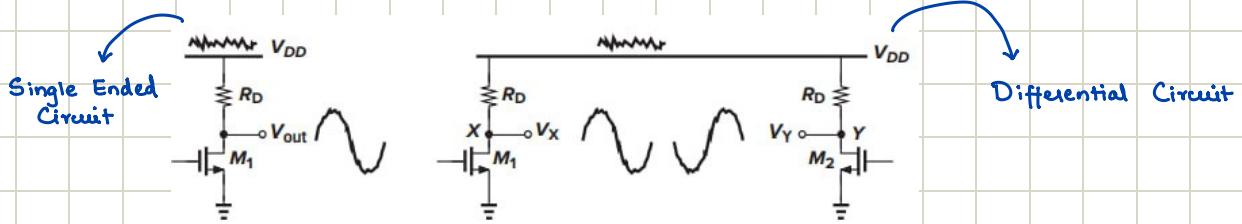
$$V_{out} = (V_{DD} \pm \Delta V) - I_D R_D$$

So, output is quite susceptible to noise on  $V_{DD}$

If circuit is symmetric,  $V_{DD}$  affects  $V_x$  &  $V_y$

but,  $V_x - V_y = V_{out}$  which doesn't change

So, Differential circuit's signal is more robust in dealing with supply noise

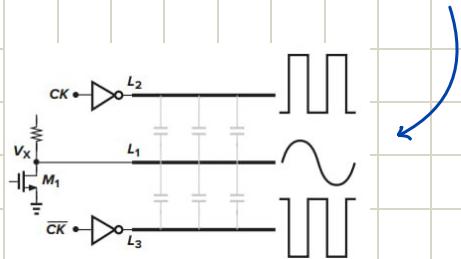


→ In Conclusion, we can employ differential path for sensitive signals & noisy signals

victims

aggressors

Suppose the clock signal is distributed in differential form on 2 lines, then with perfect symmetry, components coupled from CK &  $\overline{CK}$  to the signal line cancel each other



→ Differentiable signaling increase max achievable voltage swings

The max output swing at X or Y =  $V_{DD} - (V_{AS} - V_{TH})$

But peak to peak swing for  $V_x - V_y$  =  $2[V_{DD} - (V_{AS} - V_{TH})]$

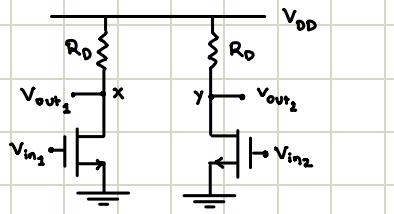
→ Simpler Biasing

→ Higher Linearity

### Disadvantage of Differential Operation

→ Occupies Twice the area of single-ended alternatives

## Basic Differential Pair



$V_{in1}, V_{in2} \Rightarrow$  Differential Input

$V_{out1}, V_{out2} \Rightarrow$  Differential Output

$V_{in,CM} \Rightarrow$  Bias Potential

$V_{out,CM} > V_{in,CM}$

$$\rightarrow A_v = \frac{V_{out}}{V_{in}} \Rightarrow V_{out} = A_v V_{in}$$

$$\rightarrow V_{out1} = -g_m R_D V_{in1} \quad \& \quad V_{out2} = -g_m R_D V_{in2}, \quad R_{D1} = R_{D2} = R_D$$

$$V_0 = V_{out2} - V_{out1}$$

$$= -g_m R_D (V_{in2} - V_{in1})$$

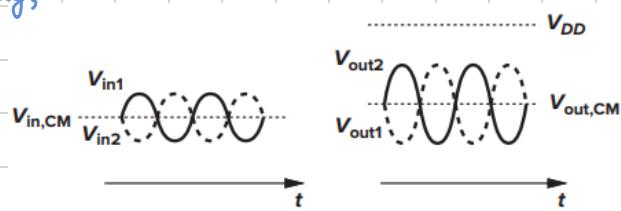
$$\Rightarrow \frac{V_0}{V_d} = -g_m R_D \quad (V_d = V_{in2} - V_{in1})$$

Circuit amplifies difference of input signal

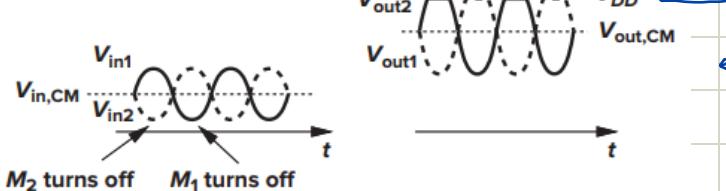
Q. What happens if  $V_{in2}$  &  $V_{in1}$  don't have a well defined CM dc level?

A. If any variation in  $V_{in,CM}$  occurs,  $I_D$  changes causing  $g_m$  and  $A_v$  to change. This causes  $V_{out,CM}$  to change.

Ideally,

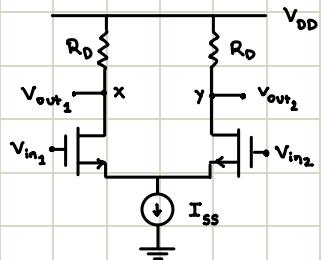


BUT, if input CM level is excessively low, then minimum value of  $V_{in1}$  &  $V_{in2}$  may turn off M1 & M2 leading to clipping of corresponding output



Avoiding clipping of output (current source)

→ At the tail end of basic differential pair, we include a current source  $I_{SS}$



$$I_{SS} = I_{D1} + I_{D2}$$

$$R_{D1} = R_{D2} = R_D$$

$$V_{in1} = V_{in2}$$

$$I_{SS} = 2 I_D$$

$$V_{out} = V_{DD} - I_D R_D \Rightarrow V_{out} = V_{DD} - \frac{I_{SS} R_D}{2}$$

Output depends on  $I_{SS}$  rather than  $I_D$

## Qualitative Analysis / Behaviour / Operation of Differential Amplifiers

→ Assume  $V_{in1} - V_{in2}$  varies from  $-\infty$  to  $\infty$

**Case 1 :** If  $V_{in1}$  is more negative than  $V_{in2}$ ,  $M_1$  is OFF,  $M_2$  is ON

Then  $I_{D2} = I_{SS}$

$$V_{out1} = V_{DD}$$

$$V_{out2} = V_{DD} - I_D R_D = V_{DD} - I_{SS} R_D$$

**Case 2 :** As  $V_{in1}$  is brought closer to  $V_{in2}$ ,

$M_1$  gradually turns ON

Partial amount of  $I_{SS}$  is drawn from  $R_{D2}$  &  $V_{out1}$  decreases

$I_{D1} \uparrow$      $I_{D2} \downarrow$

$$I_{D1} + I_{D2} = I_{SS} \Rightarrow V_{out1} \downarrow, V_{out2} \uparrow$$

**Case 3 :** When  $V_{in1} = V_{in2}$ , Both  $M_1$  &  $M_2$  are ON

$$V_{out1} = V_{out2} = V_{DD} - \frac{R_D I_{SS}}{2}$$

**Case 4 :** When  $V_{in1} > V_{in2}$ ,

$M_1$  is ON,  $M_2$  is OFF

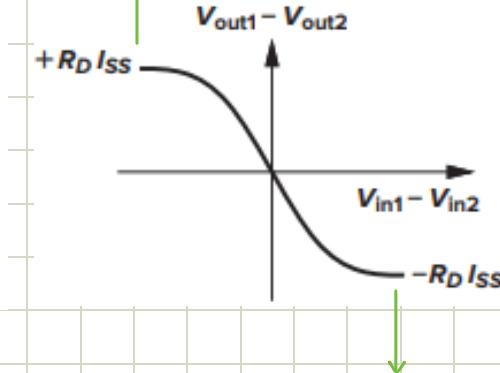
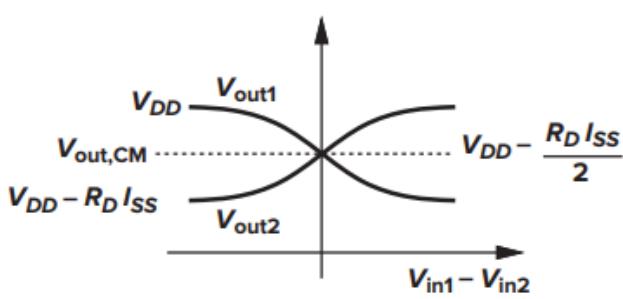
Then,  $I_{D1} = I_{SS}$  &  $I_{D2} = 0$

$$V_{out1} = V_{DD} - I_{SS} R_D$$

$$V_{out2} = V_{DD}$$

$$\begin{aligned} V_{out1} &= V_{DD} \\ V_{out2} &= V_{DD} - R_D I_{SS} \end{aligned}$$

I/O Char.  
of Differential  
Amplifier

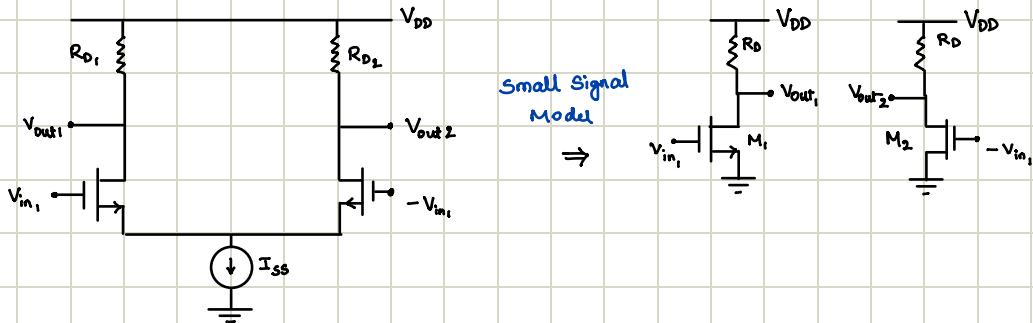


- Maximum & Minimum values at output are well defined & independent of input CM level
- Small signal gain (slope of  $V_{out1} - V_{out2}$  v/s  $V_{in1} - V_{in2}$ ) is max for  $V_{in1} = V_{in2}$  but reduces to zero as  $|V_{in1} - V_{in2}|$  increases

$$\begin{aligned} V_{out1} &= V_{DD} - R_D I_{SS} \\ V_{out2} &= V_{DD} \end{aligned}$$

## Small signal analysis of Differential Amplifier

→ Here we use "Half Circuit Concept"



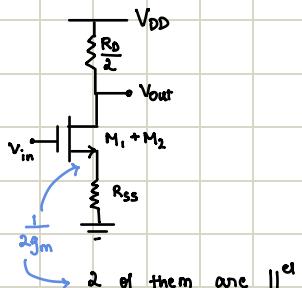
$$V_{out1} = -g_m R_d (v_{in1})$$

$$V_{out2} = -g_m R_d (-v_{in1})$$

$$\begin{aligned} V_{out1} - V_{out2} &= -g_m R_d (v_{in1}) - (-g_m R_d (-v_{in1})) \\ &= -2g_m R_d v_{in1} \end{aligned}$$

$$-g_m R_d = \frac{V_{out1} - V_{out2}}{-2v_{in1}}$$

## Common - Mode Response



$$A_{v, CM} = \frac{V_{out}}{V_{in, CM}} = \frac{-\frac{R_D}{2}}{\frac{1}{2g_m} + R_{SS}}$$

Resistance at drain  
Resistance at source

$$A_{v, CM} = \frac{-g_m R_D}{1 + 2g_m R_{SS}}$$

where  $g_m$  is transconductance of each of  $M_1$  &  $M_2$

AND  $\lambda = \gamma = 0$

Here, it is a symmetric circuit,

input CM variations disturb the bias points

altering small-signal gain and limiting output voltage swings

Q.

The circuit of Fig. 4.30 uses a resistor rather than a current source to define a tail current of 1 mA. Assume that  $(W/L)_{1,2} = 25/0.5$ ,  $\mu_n C_{ox} = 50 \mu A/V^2$ ,  $V_{TH} = 0.6$  V,  $\lambda = \gamma = 0$ , and  $V_{DD} = 3$  V.

(a) What is the required input CM voltage for which  $R_{SS}$  sustains 0.5 V?

(b) Calculate  $R_D$  for a differential gain of 5.

(c) What happens at the output if the input CM level is 50 mV higher than the value calculated in (a)?

A. a)  $V_{in, CM} = ?$

$$I_{SS} = 1 \text{ mA} \Rightarrow I_{D1} = I_{D2} = \frac{I_{SS}}{2} = 0.5 \text{ mA}$$

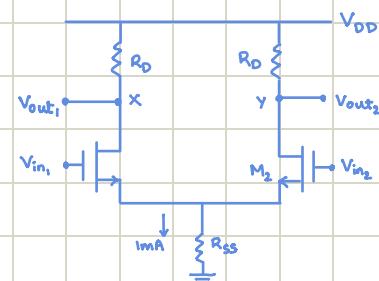
$$I_D = \mu n C_{ox} \frac{W}{L} \left( \frac{V_{GS} - V_{TH}}{2} \right)^2 \Rightarrow V_{GS} = \sqrt{\frac{2 I_D}{\mu n C_{ox} \frac{W}{L}}} + V_{TH} = V_{GS1} = V_{GS2}$$

$$= \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{50 \mu \cdot \frac{25}{0.5}}} + 0.6 = 1.23 \text{ V}$$

$$V_{in, CM} = V_{GS} + 0.5 = 1.23 + 0.5 = 1.73 \text{ V}$$

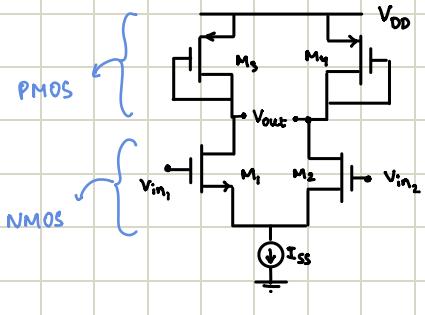
$$b) g_m = \sqrt{2 \mu n C_{ox} \frac{W}{L} I_{D1}} = \sqrt{2 \times 50 \mu \times \frac{25}{0.5} \times 0.5 \times 10^{-3}} = 1.58 \text{ mA} ; A_v = g_m R_D \Rightarrow R_D = \frac{5}{1.58 \times 10^{-3}} = 3162 \Omega$$

$$c) V_{in, CM} \text{ increases by } 50 \text{ mV} \Rightarrow |\Delta V_{x,y}| = \Delta V_{in}$$



## Differential Pair with MOS Loads

### i) Diode Connected



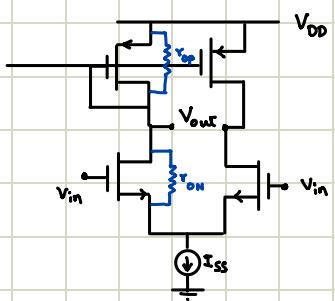
$$A_v = \frac{g_m 1}{g_m 2 + g_m b 2}$$

$$g_m b 2 = 0$$

$$A_v = \frac{g_m 1}{g_m 2} = -\frac{g_m N}{g_m P}$$

$$A_v = \sqrt{\frac{M_n(\frac{W}{L})_N}{M_p(\frac{W}{L})_P}}$$

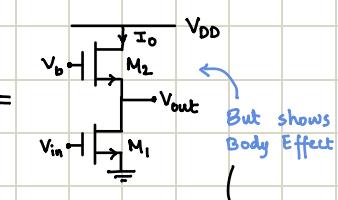
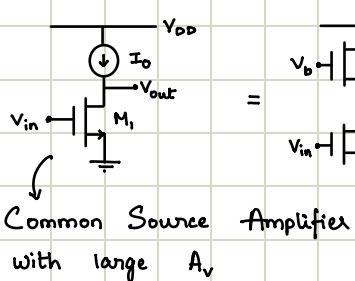
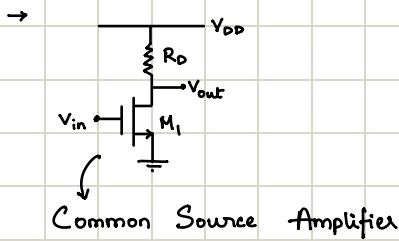
### ii) Current Source Load



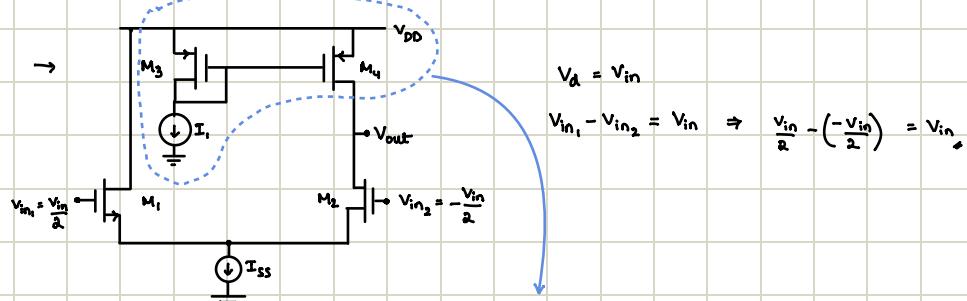
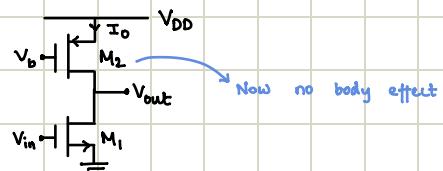
$$A_v = -g_m (R_{D1} || r_o)$$

$$= -g_m (\tau_{ON} || \tau_{OP})$$

## Differential Amplifier with Passive Load



To avoid it, we can use PMOS



$$V_{in1} - V_{in2} = V_{in} \Rightarrow \frac{V_{in}}{2} - \left( -\frac{V_{in}}{2} \right) = V_{in}$$

To generate single-ended output, Simply discard 1 output of differential pair

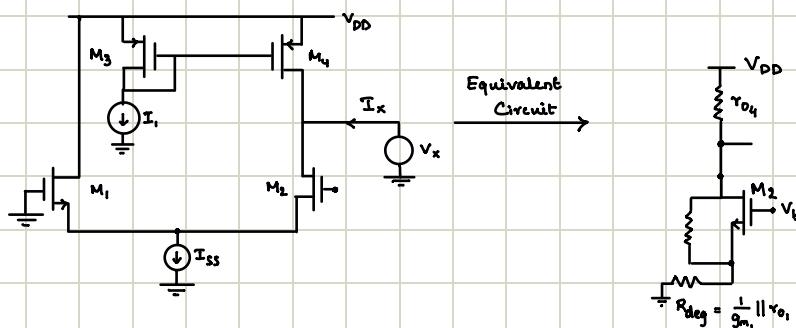
Current source in passive mirror serves as load

$$\text{we know, } A_v = \frac{V_{out}}{V_{in}}$$

$$\text{and to find } g_m = \frac{V_{out}}{V_{in} \times R_{out}} = \frac{I_{out}}{V_{in}} = \frac{g_m \cdot V_{in}/2}{V_{in}} = \frac{g_m}{2}$$

Half of  $I_0$  is wasted  
So  $g_m$  is reduced to half

→ For  $R_{out}$ , short input to zero & apply test voltage at output node



$$R_{out} \approx 2r_{o2} || r_{o4}$$

$$A_v = -G_m R_{out}$$

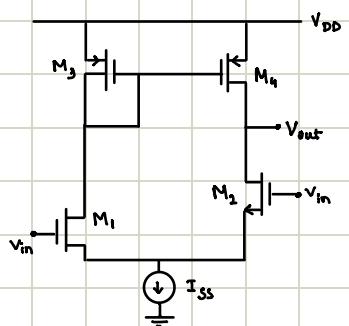
$$= -\left(\frac{g_m}{2}\right) (2r_{o2} || r_{o4})$$

If  $r_{o4} \rightarrow \infty$  then  $A_v \rightarrow -g_m r_{o2}$

### Differential Pair with Active Load (Active Current Mirror)

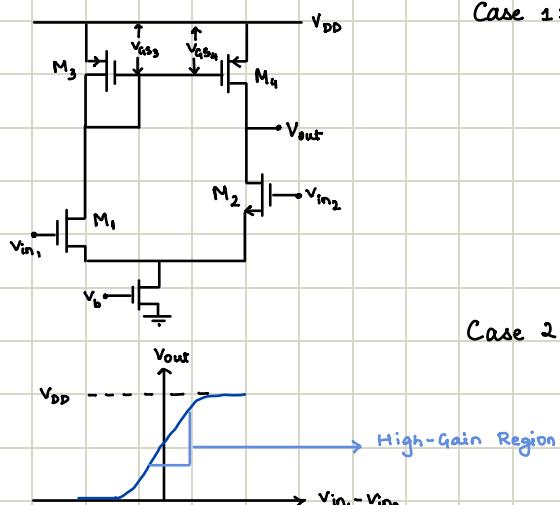
→ In passive load, small signal current of  $M_1$  is wasted and  $A_v$  is halved.

We want to utilize the current with proper polarity at output.



By maintaining  $M_3$  &  $M_4$  at same ( $\frac{W}{L}$ ) then we can mirror the current onto  $M_4$  therefore not wasting current

### Large Signal Analysis



Case 1:  $v_{in1} \gg v_{in2}$

$$v_{in1} - v_{in2} = +ve$$

$M_1$  is ON,  $M_2$  is OFF  $\Rightarrow I_2 = I_4 = 0$

$M_1$  is conducting which means  $V_{GS3} \neq 0$ , and  $V_{GS4}$  is across same points, so,  $V_{GS4} \neq 0$

$$V_{out} = V_{DD}$$

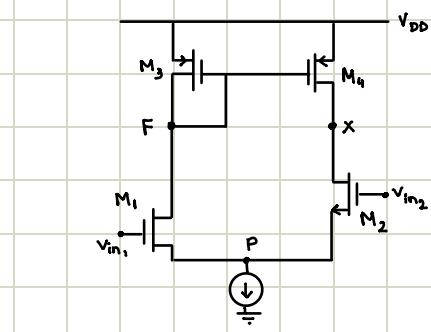
Case 2:  $v_{in1} \ll v_{in2}$

$$M_1 \text{ is OFF, } M_2 \text{ is ON } \Rightarrow I_1 = I_3 = 0 \Rightarrow V_{out} = 0$$

$$V_{out} = 0$$

High-Gain Region

## → Small Signal Analysis



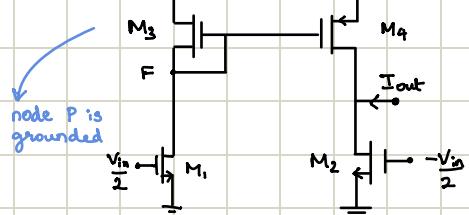
The impedances at F and X are different and so is voltage swing. This is because  $M_3$  is diode-connected & yields lower voltage gain from input to node F. Current returning from F to P through  $r_{o2}$  is negligible so then we can consider P as a virtual ground.

$$I_{D1} = |I_{D3}| = |I_{D4}| = g_{m_{1,2}} \frac{V_{in}}{2}$$

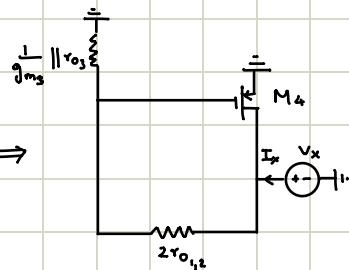
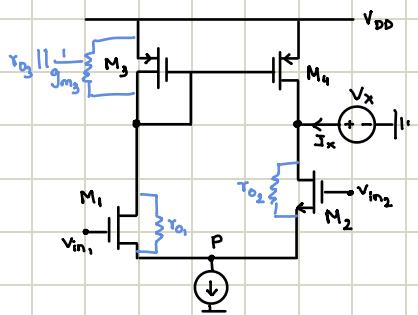
$$I_{D2} = -\frac{g_{m_{1,2}}}{2} V_{in}$$

$$A_v = G_m \cdot R_{out}$$

$$G_m = \frac{I_{out}}{V_{in}} = -\frac{g_{m_{1,2}}}{V_{in}} = -g_{m_{1,2}} \Rightarrow \text{Twice the value of passive load}$$



To find  $R_{out} \Rightarrow$



Current through  $M_4$  has 2 parts  
Mirror action from  $M_3$  to  $M_4$

$$I_x = 2 I_3 + I_4$$

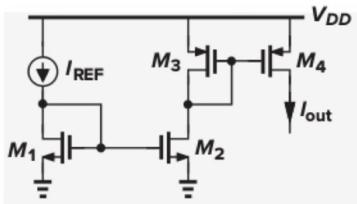
$$= \frac{2 V_x}{2 r_{o2} + (r_{o3} || \frac{1}{g_{m3}})} + \frac{V_x}{r_{o4}}$$

$$\frac{V_x}{I_x} = \frac{1}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = r_{out}$$

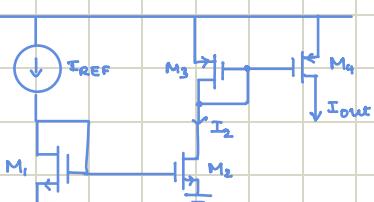
Which is higher than passive load

In the following circuit, find the drain current of  $M_4$  if all of the transistors are in saturation.

Q.



A.

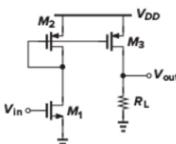


$$I_2 = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

$$|I_2| = |I_3|$$

$$I_4 = I_{out} = I_3 \times \frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(W/L)_4}{(W/L)_3} \cdot I_{REF}$$

Q. Calculate the small-signal voltage gain of the circuit shown below.



$$A. I_1 = g_m V_{in}$$

$$I_2 = I_1$$

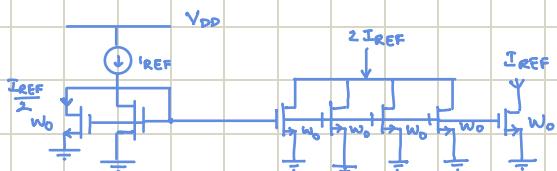
$$I_3 = I_2 \cdot \frac{\left(\frac{w}{L}\right)_3}{\left(\frac{w}{L}\right)_2} = g_m V_{in} \cdot \frac{\left(\frac{w}{L}\right)_3}{\left(\frac{w}{L}\right)_2}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_3 R_L}{V_{in}} = \frac{g_m V_{in} R_L \left(\frac{w}{L}\right)_3}{V_{in} \left(\frac{w}{L}\right)_2} = \frac{g_m R_L \left(\frac{w}{L}\right)_3}{\left(\frac{w}{L}\right)_2}$$

Q. If  $I_{REF}$  is given, generate  $\frac{I_{REF}}{2}$  &  $2 I_{REF}$ ?

Assume that all transistors will have same width

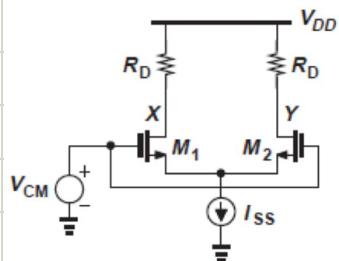
A. Initially  $\Rightarrow I_{REF}$



$2I_{REF}$  collectively because 4 of them receive  $\frac{I_{REF}}{2}$ .

Placing them parallelly finally adds up to give  $2 I_{REF}$

The MOS differential pair of Fig. must be designed for an equilibrium overdrive of 200 mV. If  $\mu nCox = 100 \mu A/V^2$  and  $W/L = 20/0.18$ , what is the required value of  $I_{SS}$ ?



$$A. V_{GS} - V_{TH} = 200 \text{ mV}$$

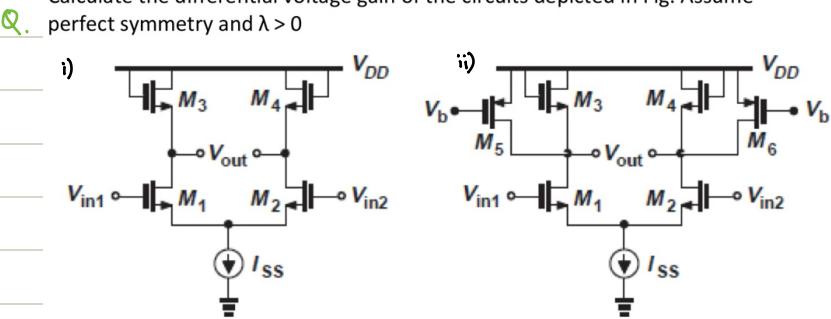
$$I_D = \frac{1}{2} \mu nCox \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$I_D = \frac{1}{2} \times 100 \times 10^{-6} \times \frac{20}{0.18} \times (200 \times 10^{-3})^2$$

$$= 0.22 \text{ mA}$$

$$I_D = \frac{I_{SS}}{2} \Rightarrow I_{SS} = 2 I_D \Rightarrow I_{SS} = 0.44 \text{ mA}$$

Calculate the differential voltage gain of the circuits depicted in Fig. Assume perfect symmetry and  $\lambda > 0$



A. i) Using half Circuit concept,

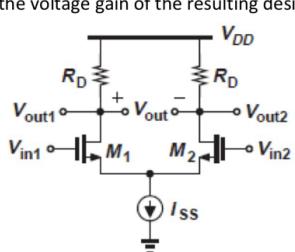
$$A_v = -g_{m_1} \left( r_o \parallel \left( r_{o3} \parallel \frac{1}{g_{m_3}} \right) \right)$$

$\downarrow$   
also parallel to  $\frac{1}{g_{m_3}}$   
if Gate & Drain  
shorted to same  
potential

ii) Using half Circuit concept,

$$A_v = -g_{m_1} \left( r_o \parallel \left( r_{o3} \parallel \frac{1}{g_{m_3}} \right) \parallel r_{o5} \right)$$

Q. Design the MOS differential pair of Fig. for an equilibrium overdrive voltage of 100 mV and a power budget of 2 mW. Select the value of RD to place the transistor at the edge of triode region for an input common-mode level of 1 V. Assume  $\lambda = 0$ ,  $\mu nCox = 100 \mu A/V^2$ ,  $VTH,n = 0.5 V$ , and  $VDD = 1.8 V$ . What is the voltage gain of the resulting design?



$$P = I_{ss} V_{DD}$$

$$I_{ss} = \frac{2 \times 10^{-3}}{1.8} = 1.11 \text{ mA}$$

$$V_{GS} - V_{Th} = 100 \text{ mV}$$

$$I_D = \frac{I_{ss}}{2} = \frac{1}{2} \mu nCox \frac{W}{L} (V_{GS} - V_{Th})^2$$

$$\frac{1.11 \times 10^{-3}}{100 \times 10^{-6} \times (100 \times 10^{-3})^2} = \frac{W}{L} \Rightarrow \frac{W}{L} = 1111.11$$

$$g_m = \sqrt{\mu nCox \frac{W}{L} \cdot I_{ss}} = \sqrt{100 \times 10^{-6} \times 1111.11 \times 1.1 \times 10^{-3}} = 0.011 \text{ S}$$

To place transistor at edge of triode region

$$V_{DS} = V_{GS} - V_{Th}$$

$$\text{and } V_{out} = V_{in,CM} - V_{Th}$$

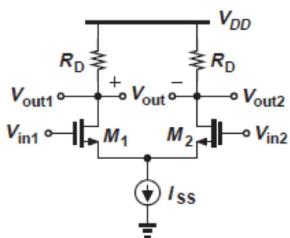
$$V_{DD} - R_D I_D = V_{in,CM} - V_{Th} \quad (V_{out} = V_{DD} - I_D R_D)$$

$$V_{DD} - \frac{R_D I_{ss}}{2} = V_{in,CM} - V_{Th}$$

$$R_D = \frac{(1.8 - 1 + 0.5) \times 2}{1.11 \times 10^{-3}} \Rightarrow R_D = 2.34 \text{ k}\Omega$$

$$A_v = -g_m R_D = -0.011 \times 2.34 \times 10^3 = -25.76$$

Design the MOS differential pair of Fig. for a voltage gain of 5 and a power dissipation of 1 mW if the equilibrium overdrive must be at least 150 mV. Assume  $\lambda = 0$ ,  $\mu nC_{ox} = 100 \mu A/V^2$ , and  $V_{DD} = 1.8V$



$$A_v = 5 \quad ; \quad P = 1 \text{ mW}$$

$$V_{GS} - V_{Th} \geq 150 \text{ mV}$$

$$\mu nC_{ox} = 100 \mu A/V^2 \quad ; \quad V_{DD} = 1.8V$$

$$P = I_{SS} V_D \Rightarrow I_{SS} = \frac{1 \text{ m}}{1.8} = 0.55 \text{ mA}$$

$$A_v = -g_m R_D$$

$$g_m = \frac{2 I_D}{(V_{GS} - V_{Th})} = \frac{I_{SS}}{V_{GS} - V_{Th}} = \frac{0.55 \text{ mA}}{150 \text{ mV}} = 3.67 \text{ mS}$$

$$R_D = \frac{5}{3.67 \text{ m}} = 1.363 \text{ k}\Omega$$

$$I_{SS} = \mu nC_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{Th})^2 \Rightarrow \left(\frac{W}{L}\right)_1 = \frac{0.55 \times 10^{-3}}{100 \times 10^6 \times (150 \times 10^{-3})^2} = 244.45$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 244.45$$