## **8-bit Processor Specification**

## **8-bit Instruction format**

|        | opcode |   |          | rd | 1        | rs |
|--------|--------|---|----------|----|----------|----|
| opcode |        |   |          | rd | imm[1:0] |    |
| opcode |        |   | imm[3:0] |    |          |    |
| 7      |        | 4 | 3        | 2  | 1        | 0  |

## <u>Instructions</u>

| opcode | reg/val | reg/val | Machine code |
|--------|---------|---------|--------------|
| LD     | ir      | nm      | 0000         |
| ST     | ir      | nm      | 0001         |
| MR     | rd      | rs      | 0011         |
| MI     | rd      | imm     | 0010         |
| SUM    | rd      | rs      | 0100         |
| SMI    | rd      | imm     | 1100         |
| SB     | rd      | rs      | 0101         |
| SBI    | rd      | imm     | 1101         |
| CM     | rd      | rs      | 0111         |
| CMI    | rd      | imm     | 1111         |
| ANR    | rd      | rs      | 0110         |
| ANI    | rd      | imm     | 1110         |
| ORR    | rd      | rs      | 1000         |
| ORI    | rd      | imm     | 1001         |
| XRR    | rd      | rs      | 1010         |
| XRI    | rd      | imm     | 1011         |

## <u> Note</u>:

- → 2-bit line for register address representation
- → Each register can hold value of 8-bit width, there are total 4-registers
- → 4-bit msb of instructions represent opcode
- → There is total 16 instructions
- → Immediate value is extended by 4-bit sign extended at msb in load/store mode instructions and 6-bit sign extended in immediate addressing mode instructions