IMPORTANT TOPICS

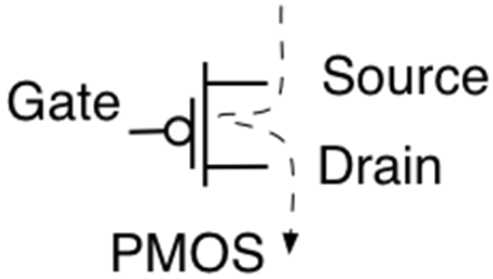
- Introduction to CMOS scaling
- It's History
- It's Application
- It's Working
- It's limitation
- Fin-FET {application ,working, adv and dis-adv, compare with CMOS}
- Technology mode {180nm, 90nm, …}
- Difference b/w long and short channel
- LT spice software
- Spice Modelling

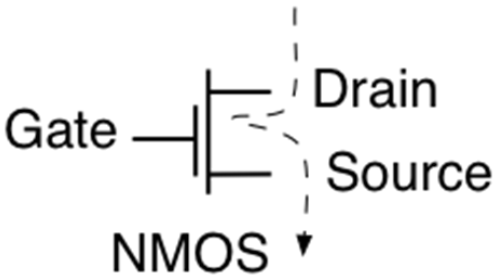
INTRODUCTION TO CMOS

❖CMOS (Complementary Metal-Oxide-Semiconductor) technology has been the backbone of the semiconductor industry.

❖It behaves as logic gate.

❖It's components are pmos & nmos.





❖In pmos when Gate= 0V, then pmos will short circuit, act as ON,
while when Gate= 1V, then pmos will open circuit, act as OFF.

❖ In nmos when Gate= 0V, then nmos will open circuit, act as OFF,
while when Gate= 1V, then nmos will short circuit, act as ON.

CMOS SCALING

- Defines as **reduction of the dimension** of different **parameters** of MOSFET.
- Why Scaling ???

1) Increase device packing density.

2) Improve speed or frequency response (1/L).

3) Improve current drive (Transconductance Gm).

4) Decrease Power consumption

TYPES OF SCALING

1) Constant Field Scaling or Full Scaling:

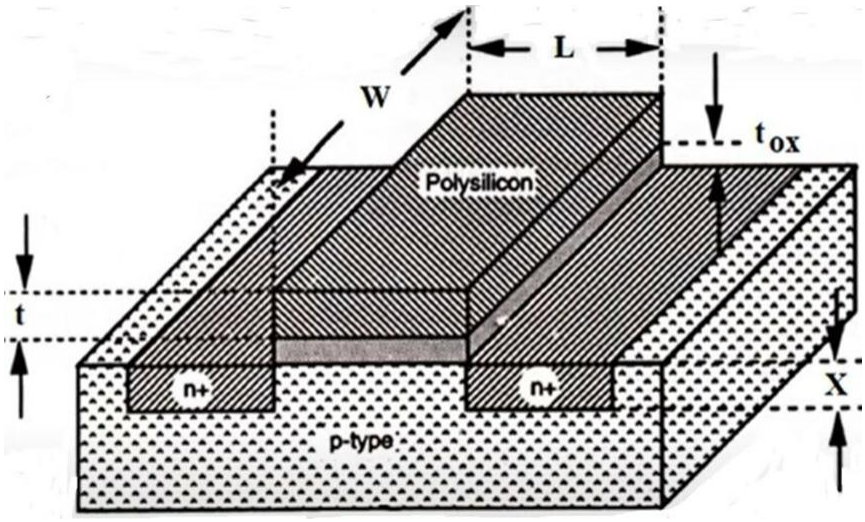
In this, all the parameter of the MOSFET is scaled to understand it in a better way we will consider a case, suppose the scaling factor is "S" who's values greater than 1 (S>1) now consider all the parameters of MOSFET is scaled by scaling factor "S" then it's all parameter will get changed to a new value.
For example, if the original gate length is "L" then after scaling it will become L' = L/S
In a similar way, all parameters of the MOSFET will get changed to their new value hence this type of scaling is known as the Full Scaling.

2) Constant Voltage Scaling:

In this only, the physical parameters of the MOSFET are Scaled-down such as the Gate length of the MOSFET is decreased, and this result In a **Short Channel Effect** which will directly affect the Drain Current, therefore the drain Current is Inversely proportional to gate length. And electrical Parameters are kept constant, such as the terminal voltage of the MOSFET is kept constant.

3) Lateral Scaling:

In this type of scaling only the width of the gate channel is scaled. It's commonly called a **gate shrink.** This type of scaling is used only in specific applications. the disadvantage associate with this type is the high electric field through the channel and hence it also causes a **short channel effect.**



PARAMETER	BEFORE SCALING	AFTER SCALING	
		FULL SCALING	VOLTAGE CONSTANT SCALING
Channel length	L	$L' = L/s$	$L' = L/s$
Channel width	W	$W' = W/s$	$W' = W/s$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/s$	$t_{ox}' = t_{ox}/s$
Junction depth	X_j	$X_j' = X_j/s$	$X_j' = X_j/s$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/s$	$V_{DD}' = V_{DD}$
Threshold voltage	V_{TO}	$V_{TO}' = V_{TO}/s$	$V_{TO}' = V_{TO}$
Doping density	N_A, N_D	N_A', $N_D' = sN_A$, sN_D	N_A', $N_D' = s^2N_A$, s^2N_D
Oxide capacitance	C_{OX}	$C_{OX}' = C_{OX}/s$	$C_{OX}' = C_{OX}/S$
Drain current	I_D	$I_D' = s.I_D$	$I_D' = s.I_D$
Power dissipation	P_D	$P_D' = P_D/s^2$	$P_D' = S.P_D$
Power density	P_D/Area	P_D/Area' $= P_D$/Area	P_D/Area' $= s^3.P_D$/Area

HISTORY OF CMOS

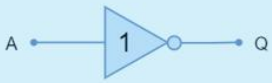
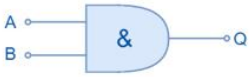
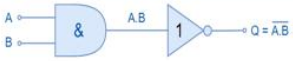
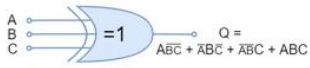
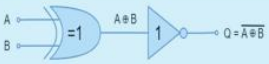
- ✓1963: Invention by Frank Wanlass at Fairchild Semiconductor.
- ✓1970s: Commercial adoption for low-power devices.
- ✓1980s: Dominance in microprocessors and memory.
- ✓1990s: Key to the rise of personal computing.
- ✓2000s: Central to the mobile device revolution.
- ✓2010s: Advanced techniques like FinFETs and high-k/metal gates.
- ✓2020s: Innovations in materials, 3D integration, and quantum computing.

WORKING OF CMOS

- CMOS works on the **principle** of:

  CMOS operates using **complementary pairs** of MOSFETs for low-power, noise-immune digital logic.

- In CMOS logic gates a collection of n-type MOSFETs is arranged in a **pull-down network** between the output and the low voltage (Vss or ground).
- Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a **pull-up network** between the output and the higher-voltage (Vdd).
- Furthermore, for better understanding of CMOS working principle, we need to discuss various logic gates(which discuss bellow).

NAME	SYMBOL	BOOLEAN
NOT		$Y=\overline{a}$
AND		$Y=a.b$
OR		$Y=a+b$
NAND		$Y=\overline{(ab)}$
NOR		$Y=\overline{(a+b)}$
XOR		$Y=(a \oplus b)$
XNOR		$Y=\overline{(a \oplus b)}$

CMOS STRUCTURE OF INVERTER

NMOS Transistor (Pull-down Network):

1. The NMOS transistor is connected between the output and ground.
2. When the input is high (logic 1), the NMOS transistor conducts, providing a path to ground and pulling the output low (logic 0).

PMOS Transistor (Pull-up Network):

1. The PMOS transistor is connected between the output and the supply voltage (Vdd).
2. When the input is low (logic 0), the PMOS transistor conducts, providing a path to Vdd and pulling the output high (logic 1).

Fin-FET

- It is Type of **Multi Gate** MOSFET.
- It is widely use over **planar CMOS FET**.
- Fin is the channel in between **S**ource and **D**rain.
- FinFET can have two or four or more Fin in same structure.
- It gives following advantages over FET
  - Area of performance
  - Lower Power Leakage
  - Low Voltage operation
  - Low Retention Voltage for SRAM
  - Better control over Current