UBC Department of Electrical and Computer Engineering
CPEN 211: Introduction to Microcomputers (2021W)
Course Syllabus

Calendar Description: Boolean algebra; combinational and sequential circuits; organization and operation of microcomputers, memory addressing modes, representation of information, instruction sets, machine and assembly language programming, systems programs, I/O structures, I/O interfacing and I/O programming, introduction to digital system design using microcomputers. Credit will be granted for only one of CPEN 211, CPEN 312, EECE 256, EECE 259 or EECE 355. Prerequisites: APSC 160.

Contact Information

Instructor: Prof. Tor Aamodt (aamodt@ece.ubc.ca;check weekly announcements for office hour times)
Teaching Assistants (TAs): Contact information available at https://cpen211.ece.ubc.ca

Course Structure

Lectures:	Tues., Thur.	1530-1730 (Tues. online on Zoom; Thur. in person in IRC 2)
Tutorial:	Wed.	1700-1900 (in person ESB 1013)
Lab marking:	See SSC for times and locations.	
Office hours:	See schedule in weekly announcements on Piazza.	

Required Materials

DE1-SoC Board: In the labs you will make use of an FPGA prototyping board called the DE1-SoC. If you have not already ordered a DE1-SoC, you can order one from http://ubc.terasic.com

Second Year Tools and Parts Kit: For Lab 2, you will need parts from the 2nd Year Tools and Parts kit that you must order. Order from https://rpelectronics-edustore.com/password using the password CPEN.ELEC21

Textbooks and References:
1. Digital Design: A Systems Approach, W.J. Dally, C.R. Harting, 2012 (used heavily weeks 1-8 of course)
2. Computer Organization & Design, ARM Edition, Patterson and Hennessy, 2016 (eBook OK; used weeks 8-13)

Course Content: Topics to be covered include: Effect of noise in circuits; representing information; Boolean algebra; CMOS logic gates, standard cell design; Verilog syntax, semantics and synthesis rules; combinational logic design and building blocks; finite state machine (FSM) design; field programmable gate array (FPGA) architecture; testbenchs & debugging; read-only and read-write memory; addition in binary, 2's complement; datapath FSMs; design of arbitrary digital circuits; assembly coding in ARM; loops, function calls; fixed- and floating-point numbers; computer system organization: performance, pipelining.

Learning Objectives: By the end of CPEN 211 you will be able explain how a computer works from the bottom up; from the operation of individual complementary metal oxide semiconductor (CMOS) transistors up to C programming constructs. You will be able to design and optimize combinational and sequential digital logic circuits both manually using the principles of Boolean algebra and automatically with the assistance of modern computer aided design (CAD) tools using a language called Verilog. You will be able to describe rules for using Verilog to ensure it can be synthesized into hardware that behaves correctly. You will be able to construct larger circuits by combining smaller circuits. You will be able to identify design errors in a circuit by creating testbenches. You will be able to describe the von Neumann computing model and design a simple computer implementing this model in Verilog. You will be able to explain how software is represented in 1's and 0's at the machine level and to write programs in ARM assembly corresponding to C programs.

Course Activities and Assessment: Your mark is based upon assessment of lab assignments, lab proficiency tests, online preparation work for flipped lectures, a midterm and a final exam. See course schedule on last page for dates and times. The weight of each component on your final grade will be:

Lab assignments:	21% (7 labs in total, each lab contributes 3% to your final grade)
Lab proficiency tests:	15% (3 tests, using laptop during tutorials; **you *must* get ≥ 3/15 to pass CPEN 211**)
Flip lecture prep:	4% (for answering questions on edge.edx.org *before* flipped lectures)
Midterm exam:	20% (closed book)
Final exam:	40% (closed book; **you must pass the final exam to pass CPEN 211**)

Webpages: CPEN 211 makes use of the following online resources:

- Piazza (sign up via http://canvas.ubc.ca): Slides, lab handouts, announcements, online discussion and Q&A.
- Flipped lecture exercises will use edge.edx.org (follow sign-up instructions to be distributed later)
- Lab partners sign up, lab TA lookup, lab proficiency tests, auto grader: https://cpen211.ece.ubc.ca
- Grades: http://canvas.ubc.ca

Announcements: Important information will be communicated via weekly announcements posted every Sunday evening on Piazza. You will likely lose marks somewhere if you do not read the weekly announcements.

Slides/Video/Notes: The lectures slides are not a complete record of the course. You should take notes while attending lectures or watching CPEN 211 2021W lecture videos online. Updates to slides may be posted after lectures. Lecture videos will be recorded using the built-in recording system in IRC 2 (Thu.) and Zoom (Tue.)

Problem Sets: Problem sets emphasize concepts. They are not marked but solutions will be posted and your learning will be assessment via related questions on the midterm, lab proficiency tests and final exam.

Lab Assignments: CPEN 211 emphasizes practical engineering skills through weekly labs. Even if you don't usually enjoy labs you should view labs as an opportunity to grow your capabilities. Expect to spend 6 *or more* hours per week on completing labs for CPEN 211. Part marks are given for partially completed labs. To balance CPEN 211 with other courses set a limit on how much time you are able to invest into these labs. For Lab 3 to 7 you **MUST** submit your code via a program called "handin" by the time noted on the lab handout by **9:59 PM (Pacific Time)** the night before your lab section. A portion of your marks for some later labs will be assigned using an auto grader that performs automated tests to check for errors. While the difficulty of labs varies, all labs are given equal weight in terms of your final grade (3% each).

To reduce congestion in the lab, sessions are split into two, one hour marking sessions. You and your lab partner will be assigned to one of these The TA who marks you and your partner will typically change from one week to the next. Lookup your marking session and TA https://cpen211.ece.ubc.ca/cwl/ta_lookup.php the evening before your lab session.

The first lab is the week of September 27. You will need an ECE account to submit your code for Lab 3 to 7. To get an ECE account, go to: https://help.ece.ubc.ca/How_To_Get_An_Account. Due to the National Day for Truth and Reconciliation, Thursday sections (L1D, L1E) for Lab 1 will be held on Oct 7. Due to Thanksgiving, Tuesday sections (L1A, L1B) for Lab 2 will be held on Oct 19. Lab 3 will be Oct 25 to 29 for all sections.

Lab Proficiency Tests: The ability to design complex systems that work is a skill prized by employers. The labs in CPEN 211 are an opportunity to develop this skill. To assess this aspect of learning there are three Lab Proficiency Tests (LPTs) held during tutorials on Nov 3, 17, and Dec 1. To complete the LPTs you need a computer with ModelSim and Quartus installed (see Lab 3).

Each LPT is worth 5%. The first LPT (Nov 3) will cover Lab 3. The second LPT (Nov 18) will cover Lab 4. The last LPT (Dec 1) will cover Lab 5 and 6.

At the start of the proficiency test you download the proficiency test questions to your computer from https://cpen211.ece.ubc.ca. Each student must complete the proficiency test *individually*. When you are done you will submit your solution code via Canvas. Each question solution will be auto-graded and often either be marked as passing and get full marks or else get zero marks. We will endeavor to provide results within one week. To avoid losing marks carefully test your code before submission.

Exams: The midterm is Oct. 20 during tutorial. The final exam date is TBD. The objective is to assess competence in and mastery of course material. They include questions of varying difficulty. Rough guide: Competency questions (~½ of marks for questions in this category), mild questions (~¼), "challenge" questions (~1/8), and "hard" questions (~1/8). Midterm and exam cover lectures, problem sets and labs.

Course Policies

Lab Grades: Due to limited number of TA hours you are permitted to attend **ONLY** the lab marking session you are assigned to. The TAs will email a lab demonstration record to you when you receive a mark in the lab.

They will enter your grade online within one week of the lab. If you do not see a grade you must notify the TA within two weeks of the lab demonstration date via email. Requests for "missing grades" received more than two weeks after a lab demonstration may not be considered. For Lab 3 to 7 you **MUST** submit your code via a program called "handin" by **9:59 PM** the night before your lab section (see Lab 3 handout for details). **There is a one-hour grace period that ends at 10:59 PM. If you submit during the grace period 3 marks will be deducted by your TA. After the grace period, your mark for the lab will be zero.** If you earn bonus marks on a lab these can be carried over to other portions of the course (e.g., you can earn more than 21% of your final course grade from the labs if you do well on the required portion and earn bonus marks).

Academic Integrity: Sharing of lab solution code or providing a description of your solution to another student who has not finished their lab are forbidden. Use of code written by anyone but an authorized lab partner is forbidden. Code from assigned textbooks can be used if the source is cited. Students repeating CPEN 211 are not permitted to submit any portion of code they wrote while taking the course previously. Additional lab policies are described in "CPEN 211 Lab Academic Integrity Policy". All students must sign and upload a signed copy of this handout on https://cpen211.ece.ubc.ca prior to Lab 1. This document can be found on Piazza under "Lab Handouts". Lab marks given by a TA before a signed copy of the academic integrity policy is returned will not be counted towards your final grade. Use of a compiler to generate ARM code for Lab 4 or during Lab Proficiency Tests is forbidden.

Lab Partners: For Lab 1 and 2 each student *must* work individually. For Labs 3 through 7 you may work with a partner using "paired programming" if the rules below are followed. Your partner must be registered in the same lab section as you. **BEFORE** beginning to work together as partners you **MUST** formally sign up as partners on https://cpen211.ece.ubc.ca The deadline to sign up is 96 hours (4 days) before the start of the lab. Pair programming means both partners meet and work on the lab together and both partners are active participants in the development process of the entire lab solution. Specifically, each partner must contribute at least one third to every lab. It may be considered "unauthorized collaboration" if you write less than one third of the code submitted for any lab and do not acknowledge this fact both during your demo and in a CONTRIBUTIONS.txt file submitted via Handin for Lab 3 to 7.

Select a lab partner that wishes to invest the same amount of time per week for labs in CPEN 211 as you do and who has a schedule that enables you to meet to work together of scheduled lab sessions. To change partners, you **MUST** notify your current partner by email at least seven days before the submission deadline and before you provide them any solution code or receive any solution code for the lab in which the change will take effect. In case of any concerns around academic integrity a copy of this email **MUST** be retained until the end of term and in addition the email **MUST** be written in English. You MUST also register your new partner using the https://cpen211.ece.ubc.ca website at least 96 hours before the start of the lab.

Requests for Academic Concessions (In-term): To request concession for missed work you must submit a request using: https://academicservices.engineering.ubc.ca/form-request-for-academic-concession-in-term-work/

Midterm and Final Exam: Both midterm and exam are expected to take place in person. For the midterm one single sided 8.5" x 11" handwritten (not photocopied) aid sheet is allowed. For the final exam you can bring two such sheets (or use both sides of one sheet). You must pass the final exam to pass the course.

Regrade requests: Regrade requests for the midterm must be submitted within two weeks after midterms are returned. Requests for corrections to lab marks must be sent by email to your lab TA within two weeks of your lab session. You can look up your TAs email address online here: https://cpen211.ece.ubc.ca/cwl/ta_lookup.php. Requests for regrading autograder marks must be made within two weeks of their release by submitting an "concern" from the autograder results page linked from here: https://cpen211.ece.ubc.ca/cwl/check.php As per UBC policy [http://www.calendar.ubc.ca/vancouver/?tree=3,41,93,0], final exam viewing requests **must** be received by January 31. Such requests **must** acknowledge it is UBC's policy that "The purpose of this exercise is purely pedagogic and distinct from the Review of Assigned Standing." Requests for Review of Assigned Standing (i.e., if you think your grade is incorrect) follow the policy outlined in the UBC calendar [http://www.calendar.ubc.ca/vancouver/index.cfm?tree=3,49,0,0#25149].

2021 CPEN 211 Lecture, Lab, Quiz, Proficiency Test and Reading Schedule

NOTE: lecture topic and reading dates are a rough guide only; timing will vary depending upon pace of lectures [Version 1; 7 Sep 2021]

		Lecture topics / slides; Quizzes	Readings	Lab
Week 1	9/8/21	*tutorial -- no meeting*		
	9/9/21	Introduction to CPEN 211; Effect of noise; representing information.	Dally 1.1-1.4, 10.1	
Week 2	9/14/21	Combinational vs sequential logic; Boolean algebra	Dally 3, 6.1 - 6.3	
	9/16/21	CMOS Logic Gates	Dally 4.1 - 4.3	
Week 3	9/21/21	Logic Gates Diagrams; Bubble rule	Dally 3.5	
	9/22/21	*tutorial -- problem set #1*		
	9/23/21	**F1: KMAPs**	Dally 6.3 - 6.10	
Week 4	9/28/21	Comb. logic building blocks (1) - decoder, mux, encoder	Dally 8.1 - 8.4	Lab 1: Breadboard Comb Logic
	9/30/21	**F2: Finite State Machine (FSM) design**	Dally 14.1 - 14.5	(L1A,L1B,L1C,L1F - Tue/Wed/Fri)
Week 5	10/5/21	What is verilog? Verilog module syntax	Dally 1.5, 7	Lab 1: Breadboard Comb Logic
	10/6/21	*tutorial -- ModelSim and Quartus Introduction*		(L1D,L1E - Thu)
	10/7/21	Busses, instantiation, parameters, named association		
Week 6	10/12/21	Standard cell design; What's in an FPGA? I/O Pins; Testbenchs & Debugging		Lab 2: Breadboard FSM
	10/14/21	Always block; Synthesis rule #1; Ambiguous else		(L1C,L1D,L1E,L1F - Wed/Thu/Fri)
Week 7	10/19/21	FSMs in Verilog, synthesis rule #2, non-blocking	Dally 14.6	Lab 2: Breadboard FSM
	10/20/21	*tutorial -- Midterm*		(L1A,L1B - Tue)
	10/21/21	**F3: ARM assembly coding flipped lecture #1 - ALU, loads+stores**	COD4e (PDF) 2.1-6	
Week 8	10/26/21	**F4: ARM assembly coding flipped lecture #2 - branches**	COD4e (PDF) 2.7	Lab 3: Comb. and FSM in Verilog
	10/28/21	Function calls, ARM examples	Dally 8.5 - 8.7	
Week 9	11/2/21	Hex; Addition in binary, 2's Complement		Lab 4: ARM Assembly
	11/3/21	*tutorial -- Lab Proficiency Test #1 (Lab 3)*		
	11/4/21	Iterative circuit design; arbiters, comparators; factoring, priority encoder	Dally 10.1-10.3	
Week 10		***break week***		
Week 11	11/16/21	Casex; Datapath FSMs; RAM		Lab 5: Datapath of the "Simple
	11/17/21	*tutorial -- Lab Proficiency Test #2 (Lab 4)*		RISC Machine"
	11/18/21	Computer system performance; pipelining	COD 1, 4	
Week 12	11/23/21	Fixed- vs. Floating-point numbers	Dally 11	Lab 6: FSM Controller for the
	11/25/21	Designing arbitrary digital circuits		"Simple RISC Machine"
Week 13	11/30/21	Designing arbitrary digital circuits		Lab 7: Adding Memory to the
	12/1/21	*tutorial -- Lab Proficiency Test #3 (Lab 5 and 6)*		"Simple RISC Machine"
	12/2/21	Designing arbitrary digital circuits		