Table of Contents

1. **Scope of the Project**

2. **Functional Requirements**

3. **Block Diagram**

4. **Bill of Materials (BOM)**

5. **Methodology**

SRS Document

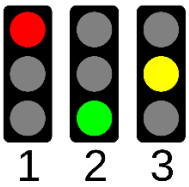
Scope of the project:

Main objective of this project is to automate traffic lights for a four-way intersection road. Normally the traffic lights turn on and off based on the amount of traffic sensed by the in-road sensors and the overall traffic situation in the nearby vicinity, which determines how long will the specific lights (red, green and yellow) stay on. In this project however, a fixed interval for all the four sets of traffic lights has been set since using sensors and other strategies is out of scope of this project.

The project is going to be implemented on a FPGA, and the code will be written in Verilog using the behavioral model. Four sets of three LEDs each will be connected to the FPGA in order to count for all the traffic lights. They will be connected to the Nexys-2 via the boards I/O header pins. Internal clock on the board will be used for timing the traffic lights.

Functional Requirements:

1. Fully functional Verilog code synthesizable on the Nexys-2 FPGA.
2. International order for the sequence of traffic lights will be used, which is as follows:

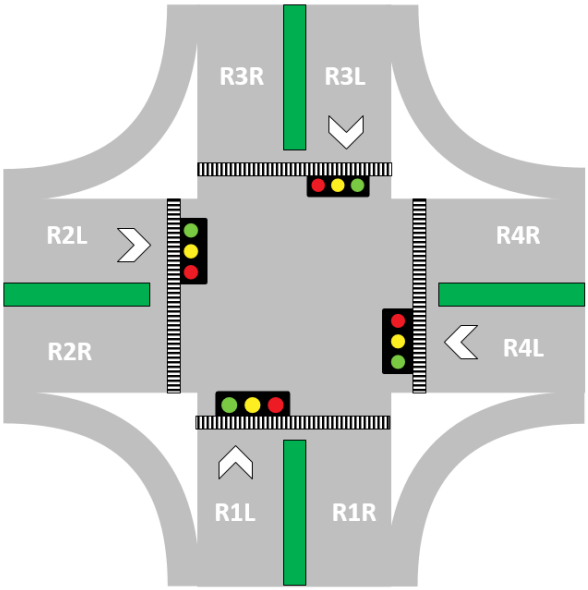


3. Proper timing between the traffic lights as set in the Verilog code.
4. The traffic LEDs and other components can be easily be managed on a single breadboard.
5. No extra power required for turning on the LEDs. Nexys-2 board's I/O header pins provide adequate voltage (3.3V) for powering all 12 the traffic lights.

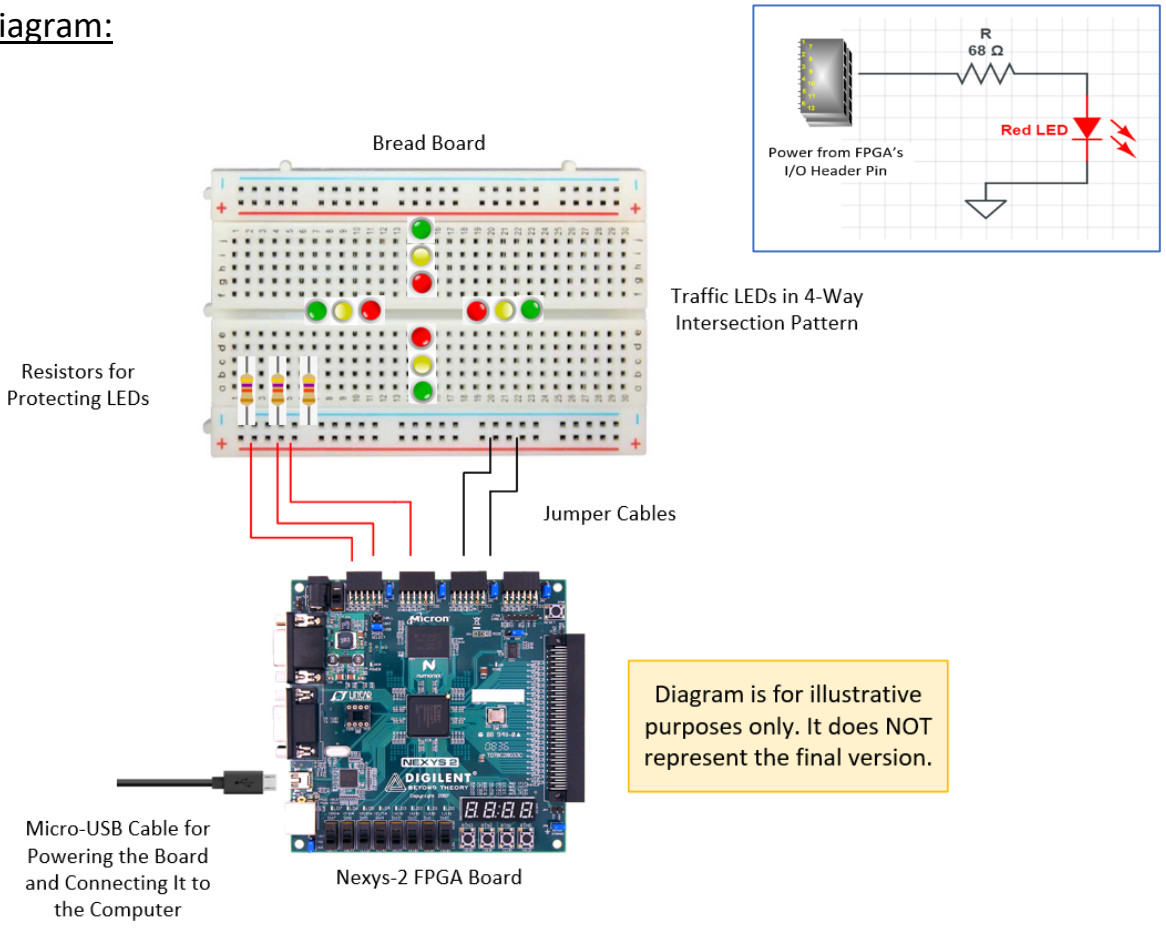
Optional Features:

Pedestrian lights can also be implemented concurrently with the traffic lights which will provide indications for pedestrians crossing the road either automatically or when an input is received from the pedestrian. Another feature will be adding a 7-segment display to the traffic lights system which will show the countdown time for each traffic light respectively while the lights change from one sequence to another.

Four-Way Intersection Diagram:



Project Block Diagram:



Bill of Materials (BOM):

S. No.	Description	Qty.
01	Nexys-2 FPGA Board	01
02	Bread Board	01
03	Jumpers/Wires	Many
04	Red LEDS	04
05	Green LEDs	04
06	Yellow LEDs	04
07	68 Ohms Resisters	12
08	Micro-USB Cable for Powering FPGA	01

Software Used:

1. Xilinx ISE 14.7
2. Proteus 8 Professional
3. Microsoft Visio
4. Microsoft Excel

Project Methodology:

At the selection/design stage of this project, I am not completely equipped with knowledge required to accomplish this project. Therefore, I would prefer to adopt the *Agile* methodology for this project. As a project management methodology, Agile is highly interactive, allowing for quick changes and modifications throughout the project. Due to no previous experience of such a project, this methodology will allow me to respond to unpredictability through iterative work processes.

END