

Digital Design and Synthesis

COEN 6501

Lecture_1

In this lecture we will review:

The Digital Design process

Introduce and review Adders

- a) The Carry Ripple Through Adder**
- b) The Carry Look Ahead Adder**

System Design Description

Systems are described in terms of three domains:

Behavioural domain

Structural domain

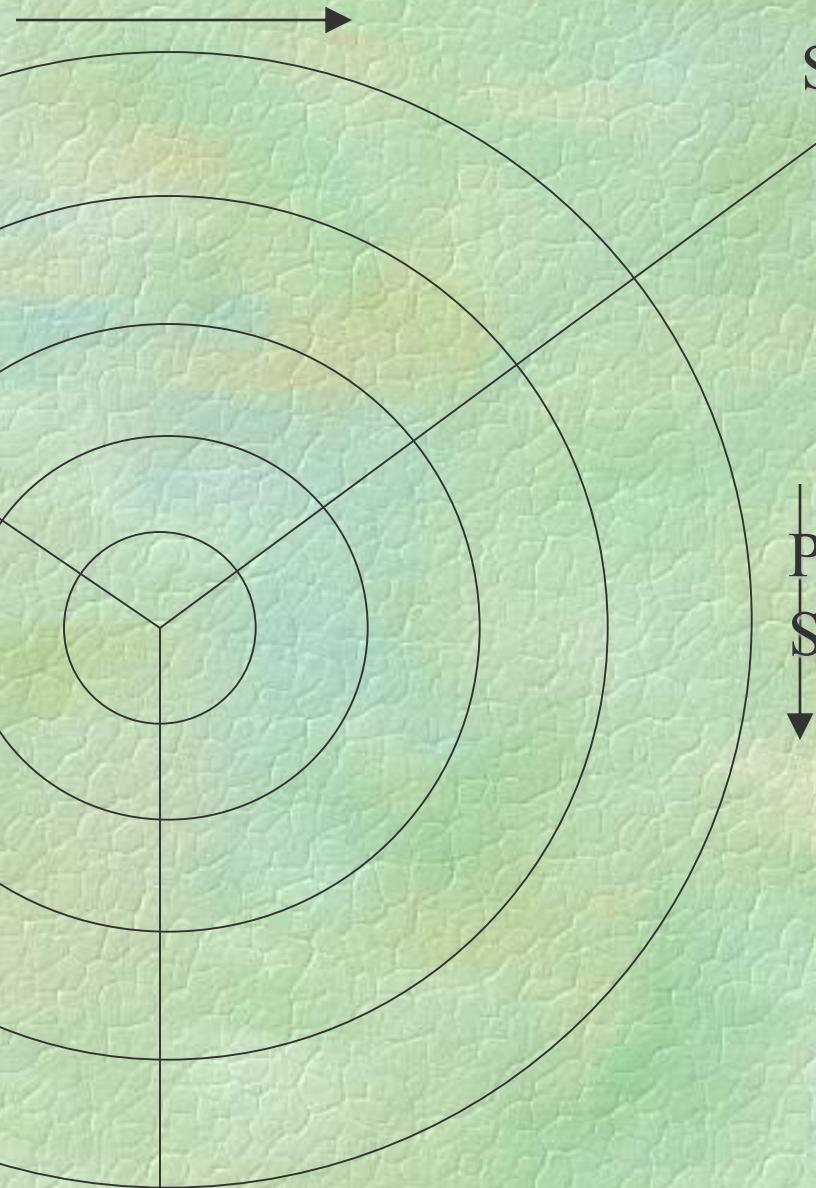
Physical domain

Logic Synthesis

Behavioural

Structural

Physical



Logic synthesis

Behavioural

Structural

Systems

Algorithms

Register transfer

Logic Equations

Transfer function

Algorithmic

Micro architecture

Logic

Circuit

Transistors

Rectangles

Cells

Macro-cells

Modules

Chips, boards...

Processor

Hardware modules

ALU, registers

Gates, F/Fs

Physical
synthesis

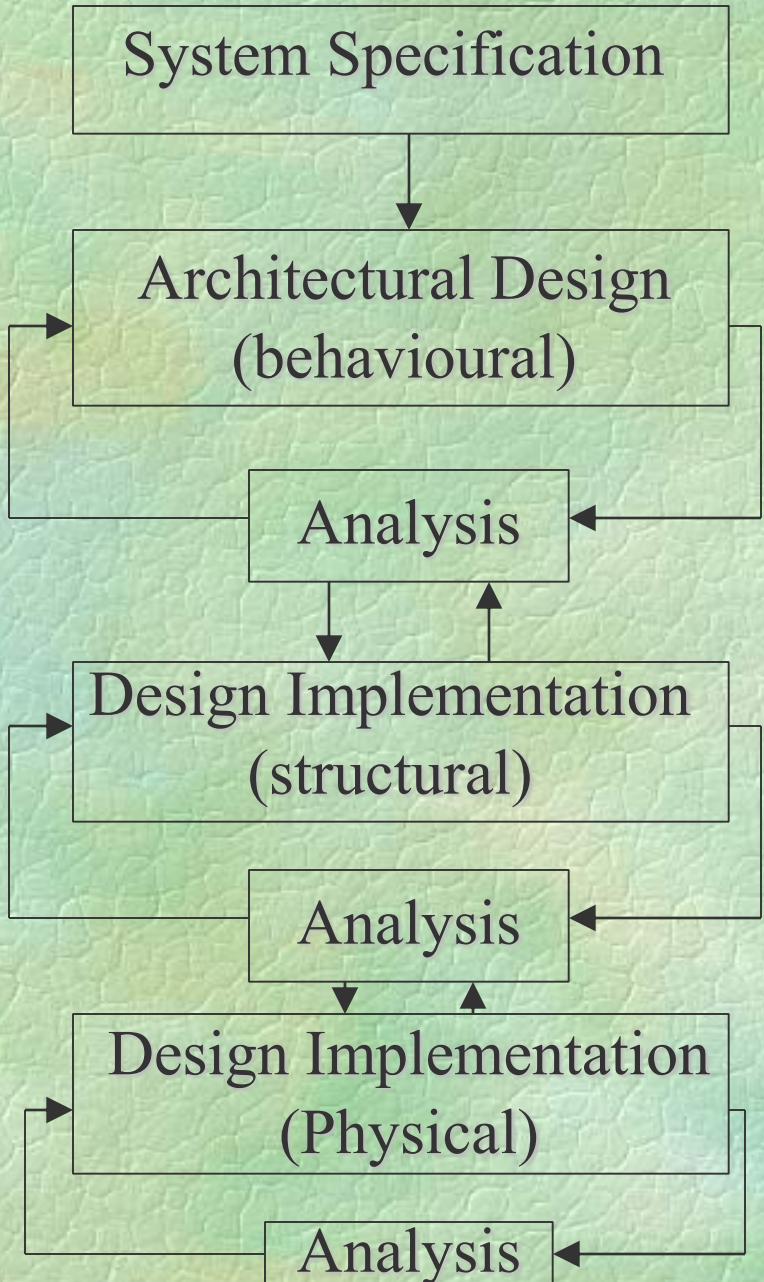
Physical

Optimization Levels

Level	Transformation	Expected Power Saving
Algorithmic	Algorithm selection	Orders of magnitude
Behavioural	Concurrency	Several times
Register Transfer Level	Structural transformations	~10 - 15%
	Clock control	~10 - 90%
Data/signal encoding		~20%
Technology independent	Extraction/decomposition	~15%
Technology dependant	Technology mapping	~20%
	Gate sizing	~20%
Layout	Placement	20%

Design Process:

It starts with behavioural description, decomposing the high level of constructs into more precise functional units, then mapping these units into physical elements.



Design Strategies

Hierarchy

- | A repeated process of dividing large modules into smaller sub-modules until the complexity of sub-modules are at an appropriately comprehensible level of detail.
- | Parallel hierarchy is implemented in all domains.

A Structured Design

Ô Regularity

- | Divide the hierarchy in to similar building blocks whenever possible.
- | Some programmability could be added to achieve regularity.

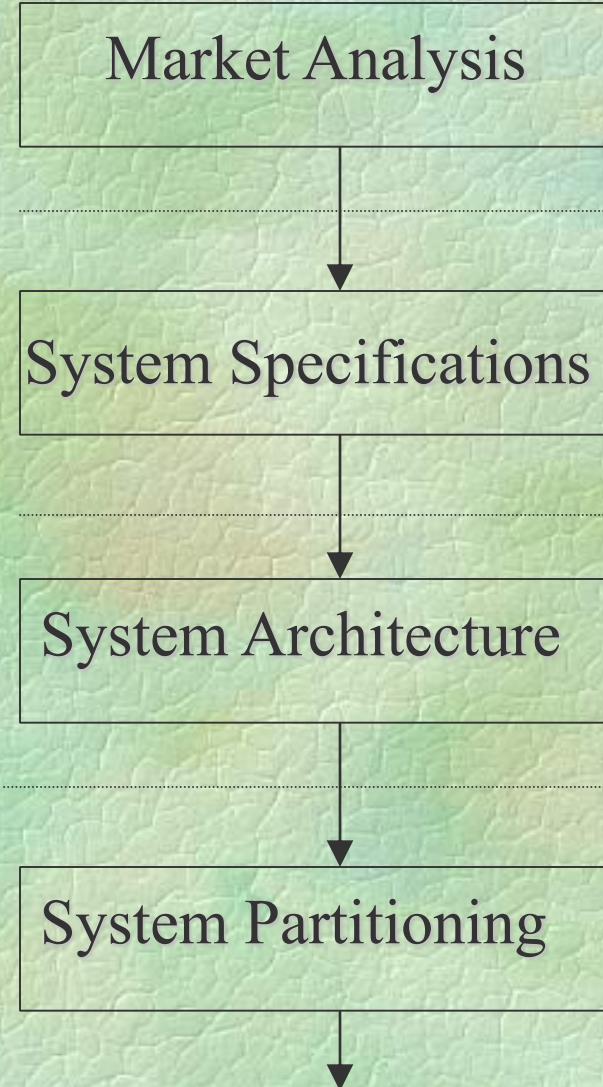
Ô Modularity

- | Well defined behavioural, structural and physical interface.
- | Helps: divide tasks into well defined modules, design integration, aids in team design.

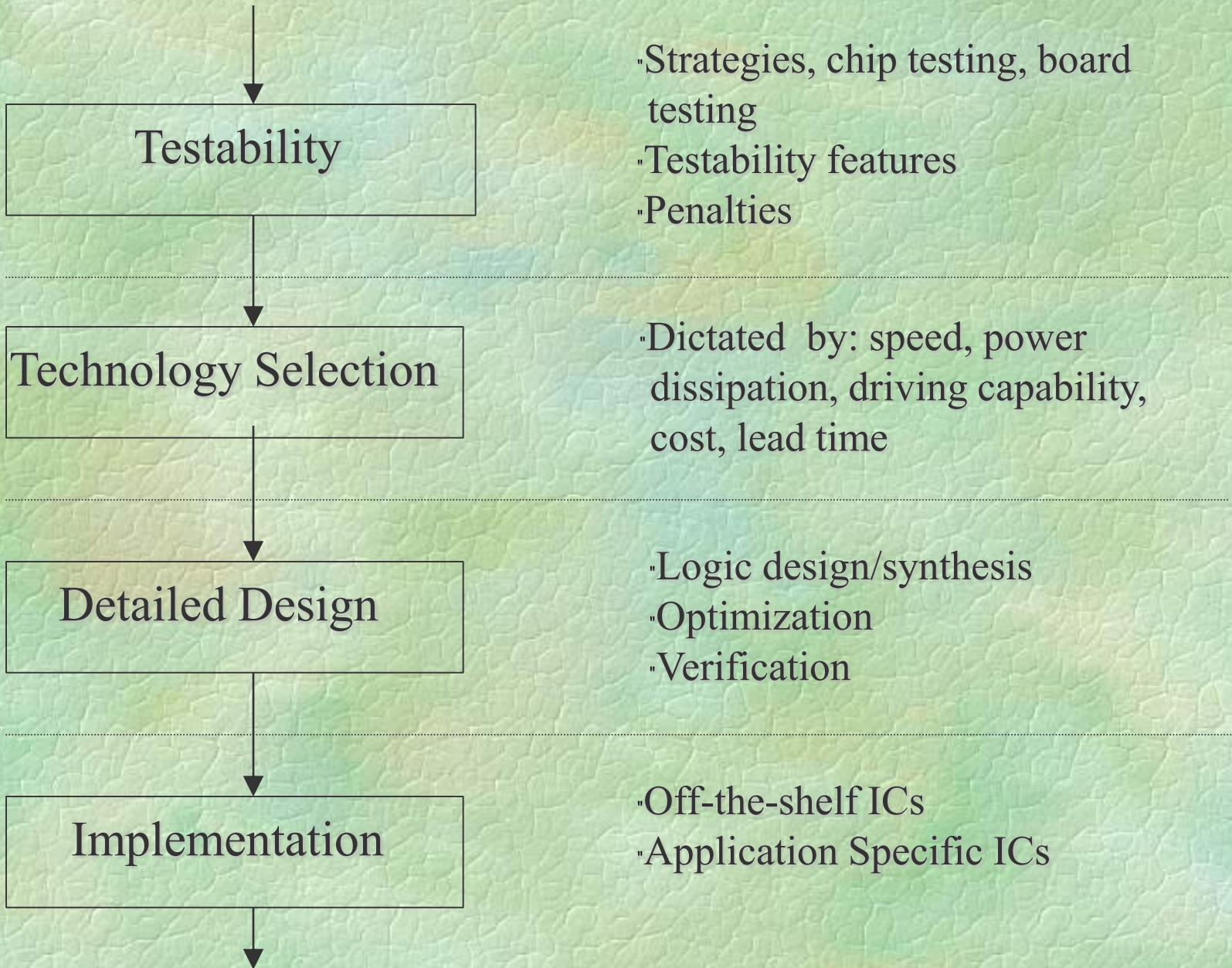
Ô Locality

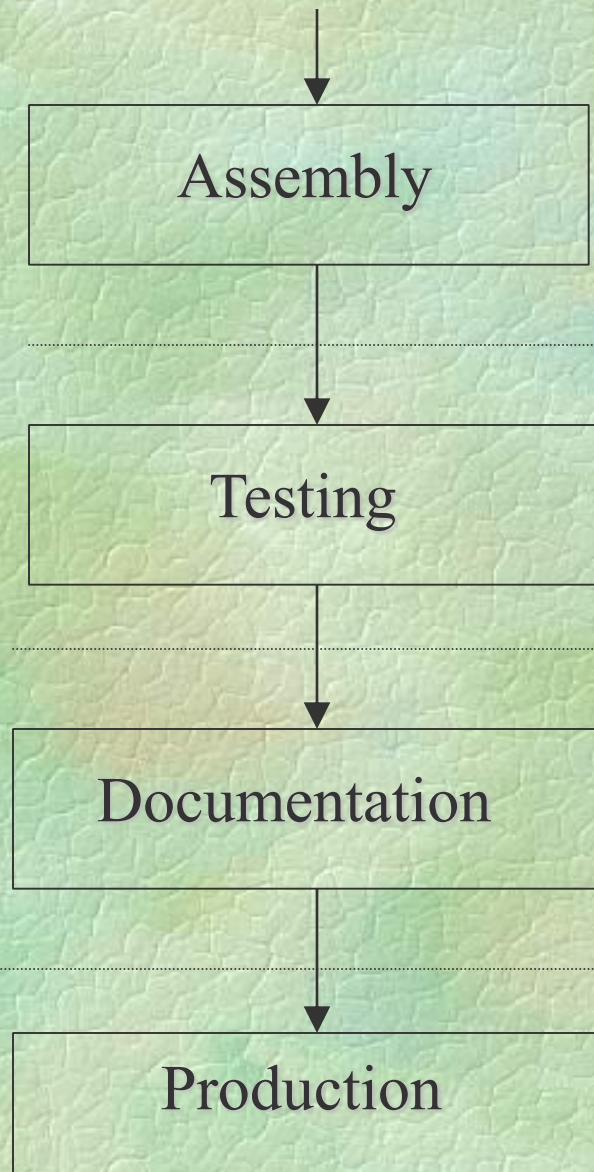
- | Internals of the modules are unimportant to any exterior interface.

System Design Methodology



- Market windows
- System features & requirements
- Standards
- Functional
- Electrical
- Mechanical
- Environmental
- Strategies
- Modelling
- Verification
- Dictated by complexity, I/O pins, off-the-shelf components, special requirements
- Partitioning guidelines
- Partitioning approaches: vertical, horizontal, functional, performance



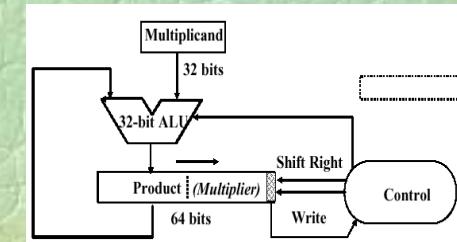
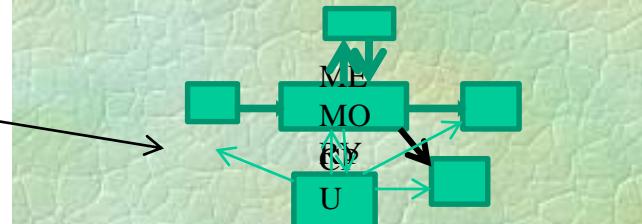
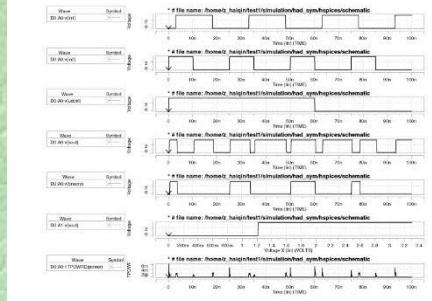


- Decide on packaging technical components
- Design/manufacture
- Components
- Electrical/mechanical assembly
- Mechanical assembly & components sales

- Functional
- DC test
- AC test
- Burn-in

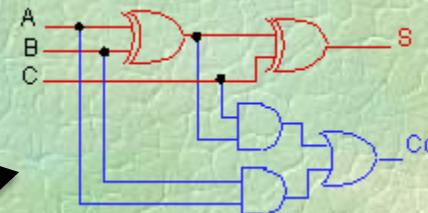
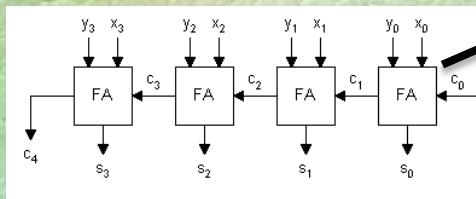
- Technical documents
- H/W & S/W & mechanical
- User manual
- Test document

Verify at every step

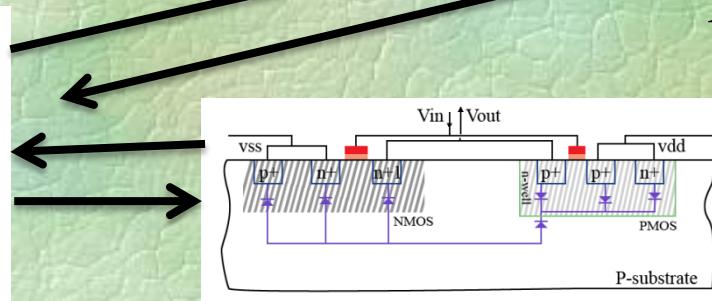
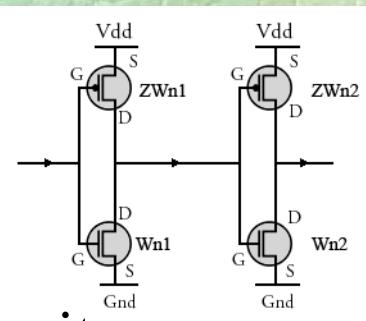


Functional

Structural



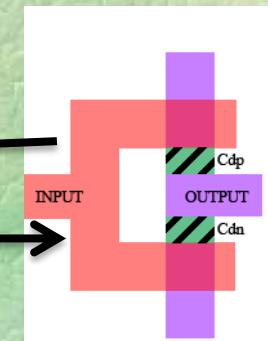
Logic



Circuit

Device

Layout
13



IC Design Methodology

Requirement specification

- | most important function which impacts the ultimate success of an IC relates to how firm and clear the device specifications are.
- | Device specification may be updated throughout the design cycle.
- | Main items in the specifications are:
 - functional intent: brief description of the device, the technology and the task it performs.
 - Packaging specification
 - device port number
 - package type, dimension, material

Functional Description

| Functional description

- high-level block diagram: all major blocks including intra block connections and connections to pin-outs indicating direction and signal flow.
- Intra block signal function: description of how blocks interact with each other supported with timing diagram where necessary.
- Internal block description of internal operation of each block. Where necessary, the following to be included: timing diagram, state diagram, truth table.

Specifications

- | I/O specifications
 - pin-out diagram
 - I/O functional description
 - loading
 - ESD requirements
 - latch-up protection
- | D.C. specifications
 - absolute maximum ratings for: supply voltage, pin voltages
 - main parameters: VIL and VIH for each input, VOL and VOH for each output, input loading, output drive, leakage current for tri-state operation, quiescent current, power-down current (if applicable)

Specification, continued

- | AC specifications
 - inputs: set-up and hold times, rise and fall times
 - outputs: propagation delays, rise and fall times, relative timing
 - critical thinking
- | Environmental requirements
 - operating temperature, storage temperature, humidity condition (if applicable)
- | Testing

Device Specification

-] Functional intent: briefly describe the device, the technology, and the circuits it will replace as well as the task it will perform.
- ^ Design concept
 - † pin-out diagram: describe the device using a block diagram of the external view of the chip - basically, a box with all the I/O pins labelled and numbered
 - † I/O description: use a chart to define the I/O signals shown in the pin-out diagram

Example:

Pin #	Pin Name	I/O Type	Function
P1	V _{DD}	Power Supply	Power Supply, +5V dc with respect to V _{SS}
P2	TXCLK	Input	Transmit Clock, 5.12 MHz rate
P3	TXP1	Output	Transmit output – channel 1, +ve polarity

Functional Specification

- internal block diagram: draw blocks for major functions, show all connections including: connection to all pin-outs, connections between blocks, and direction of signal flow
- Inter-block signal function: describe how the blocks interact with each other and support this with timing diagrams where necessary
- internal block description: describe the internal operation of each block. When necessary, include: timing diagrams, state diagrams, and truth table
- Logic description: circuit schematic or logic diagram using standard cell library components
- Package description: device port number, package type, dimensions, materials

Operating characteristics

Absolute maximum stress ratings.

Example:

Parameter	Symbol	Min.	Max.	Unit
Storage T	T_s	-65	+150	°C
Operating T	T_A	-40	+85	°C
Supply V	V_{DD}	-0.5	7	V
Input V	V_I	-0.3	$V_{DD} + 3$	V
Supply I	I_{DD}		5	mA

Requirements

- | Operating power and environmental requirement:
 - power supply voltage
 - operating supply current (specify conditions, e.g., power up, power down, frequency, output conditions)
 - storage temperature
 - operating temperature
 - humidity conditions (if applicable)

Input characteristics. Example chart:
 (V reference is VSS = 0, temperature range is 0oC to 70oC)

Pins	Symbol	Para- meter	Min	nom	Max	Units	Comments
TXDAT2	VIL	Input low V	-0.3	0.4	0.8	V	
TXCK	VIH	Input high V	2.0	2.4	VCC + 0.3	V	
ENB1	CI	Input C to V _{ss}			10	pF	Inputs protected against static damage
ENB2	IIL	Input low I			+/- 10	A	
ICK	IIH	Input high I			+/- 10	A	
LFPM	VIP	Input peak V			VDD + 0.3	V	
CSBL							
RX1N1							
RX1N2							

Output Interface Characteristics

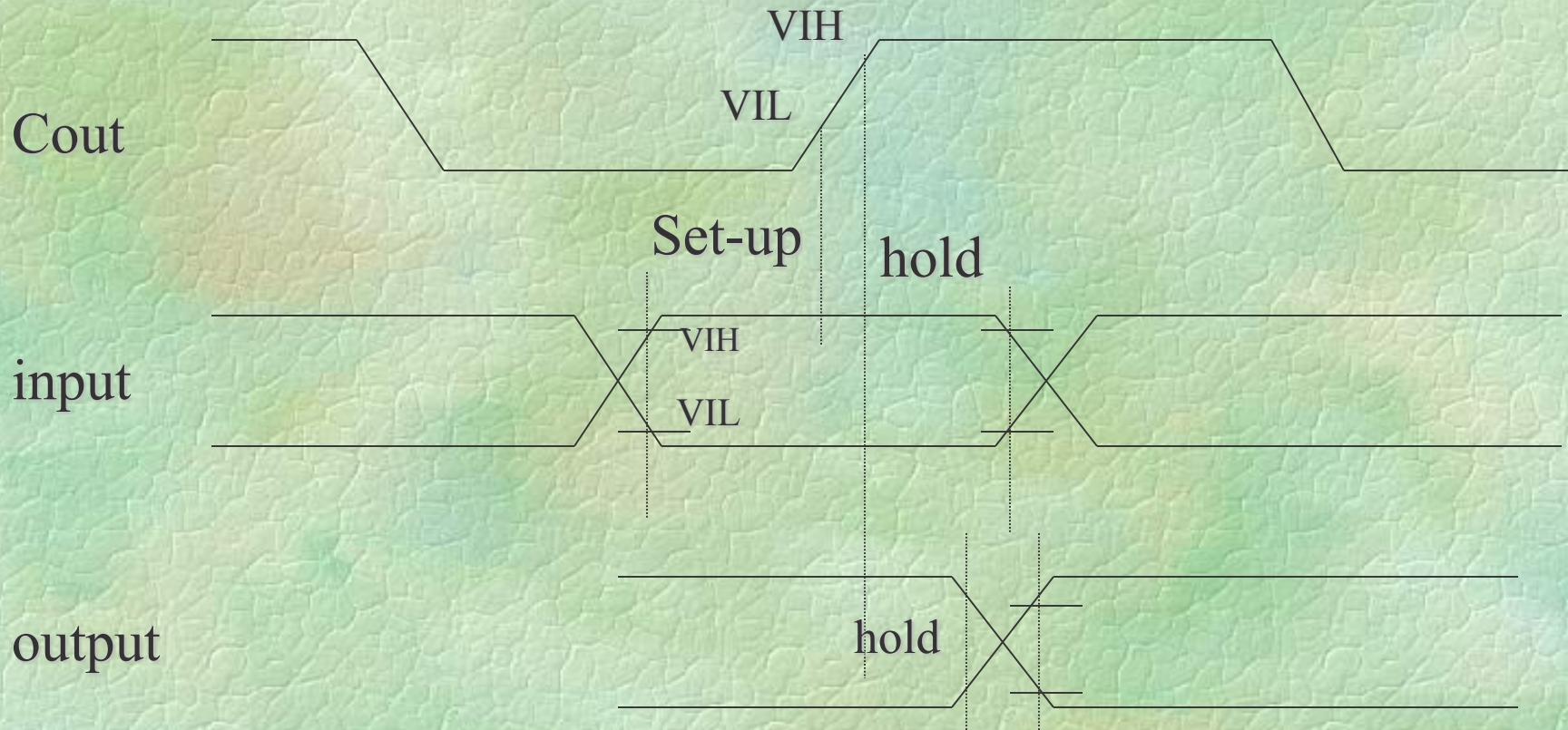
Example chart: (VSS = 0, T range 0oC to 70oC)

Pin names	Parameter	Symbol	min	max	units	Test condns
LABUS <0..15>,	High level Vout	VOH	$V_{DD} - 0.1$		volt	IO<= 1microA
RABUS <0..15>	Low level Vout	VOL		0.1	volt	IO<= 1microA
	High level Iout	IOH	0.25		mA	$V_O = 4.6V$
			1.6		mA	$V_O = 2.5V$
	Low level Iout	IOL	1.6		mA	$V_O = 0.4V$
			3.4		mA	$V_O = 2.5V$
	High level tristate Iout leakage	IOIH		10	microA	$V_O = V_{DD}$
	Low level tristate Iout leakage	IOIL		10	microA	$V_O = 0V$
	Cout	C_O		10	pF	

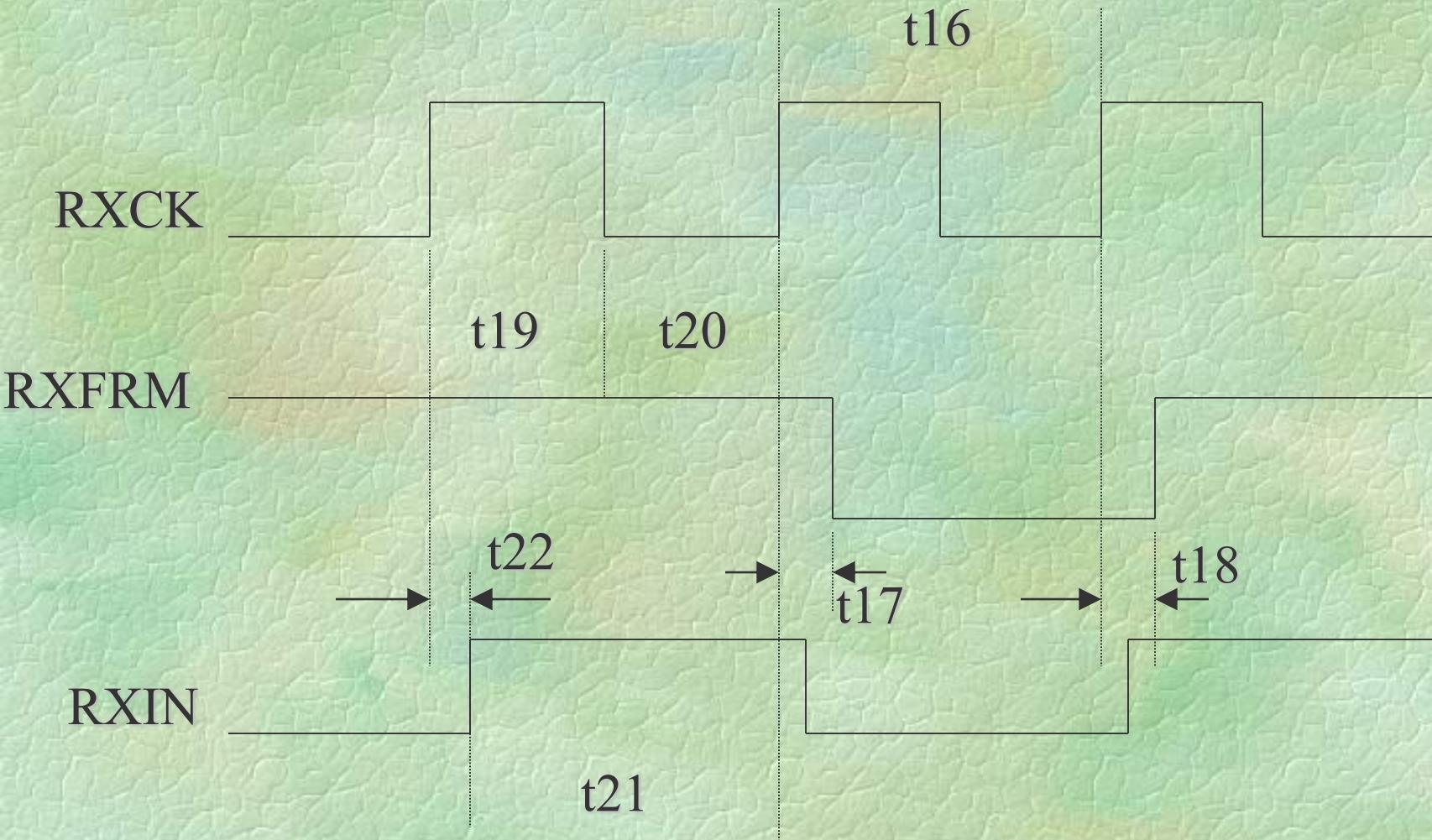
AC description

Timing diagram: include well-labelled signal drawings of all significant input and output relationships, rise and fall times, data set-up and hold times. Indicate the voltage range over which timing must be guaranteed

Definitions:



Example: timing diagram and chart



Specs (continued)

pins	symbol	Param eter	min	nom	max	units
RXCK	t19	Clock high	68		110	ns
	t20	Clock low	68		110	ns
	t16	Period		195.3125		ns
	t16	Period	194		197	ns
	t22	RXIN to RXCK delay		90		ns
	t17	Frame delay				ns
RXFRM	t18	Frame hold				ns

Critical Path

- Ô Signal paths with ‘tight’ timings (if applicable)
- Ô potential ‘race’ conditions (if applicable)
- Ô any set of paths with the same source and destination such as a clock signal and its complement (if applicable)

Test Description

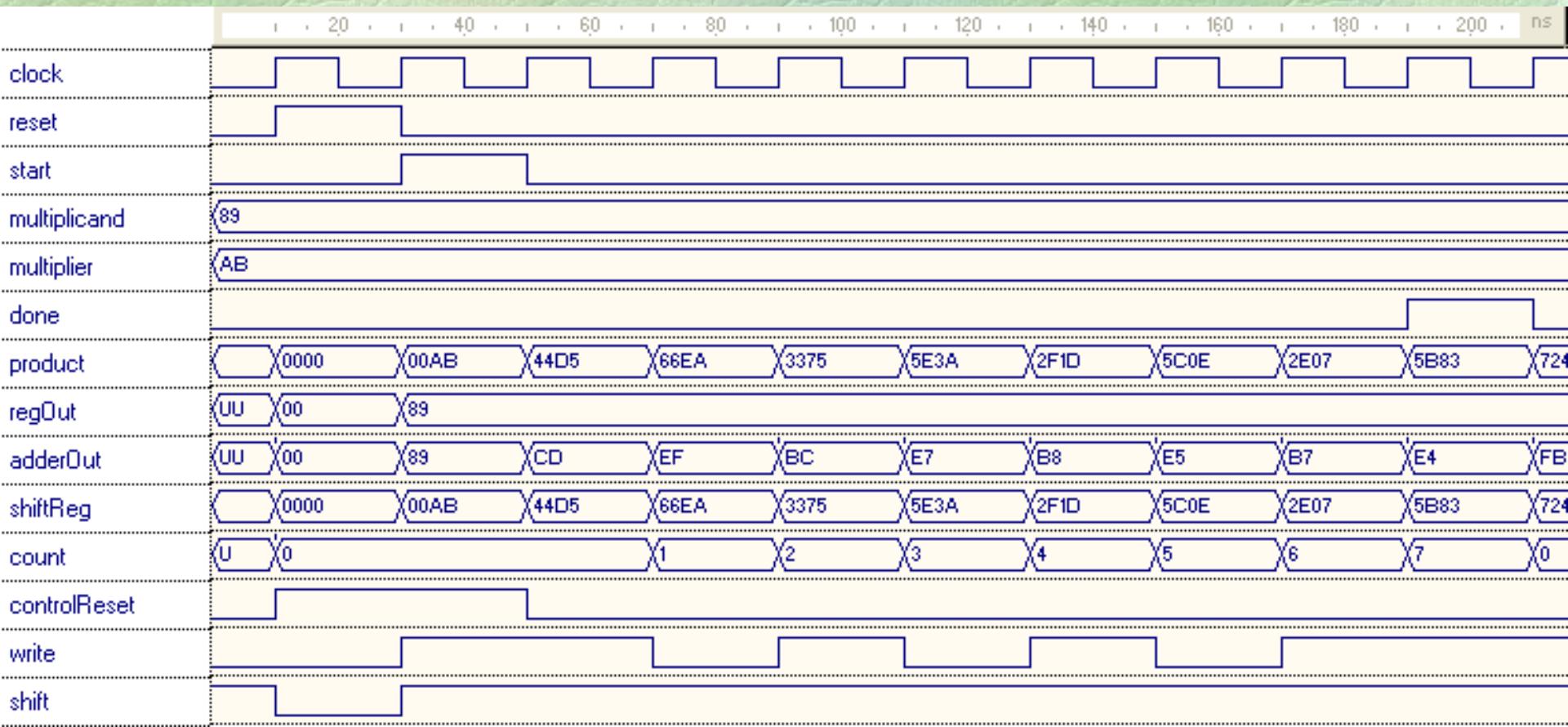
- Ô Test strategy: written description of functions to be tested. This section is a guide for determining and explaining simulation patterns
- Ô simulation input/output patterns: timing diagrams which include stimulus to be applied to input pins and the expected response on the output pins

Example :

$$\text{Multiplicand} = 10001001_2 = 89_{16}$$

$$\text{Multiplier} = 10101011_2 = AB_{16}$$

$$\text{Expected Result} = 101101110000011_2 = 5B83_{16}$$



System Level Design

- Ô Top down approach
- Ô Using behavioural constructs, top level architecture is defined
- Ô Design validation is technology independent
- Ô Use HDL to model the design (e.g., VHDL and Verilog)
- Ô RTL is efficient for describing data flow

System Level design (Continued)

- Ô Timing verification is difficult unless structure logic is defined
- Ô VHDL representation can be changed into structural logic through - manual design, design synthesis: automated process which involves the conversion of VHDL/RTL into a set of registers and combinational circuits

Synthesis report

```
File Edit Search Preferences Shell Macro Windows Help
I ****
Report : fpga
Design : SQUARER_8
Version: V-2004.06-SPI
Date   : Tue Mar  7 21:00:01 2006
****

Xilinx FPGA Design Statistics
-----
FG Function Generators:          203
H Function Generators:           0
Number of CLB cells:             232
Number of Hard Macros and
    Other Cells:                 0
Number of CLBs in
    Other Cells:                 0
Total Number of CLBs:            232

Number of Ports:                  28
Number of Clock Pads:             1
Number of IOBs:                   27

Number of Flip Flops:              29
Number of 3-State Buffers:         0

Total Number of Cells:            260
```

Area report after Synthesis

File Edit Search Preferences Shell Macro Windows

Help

I

Report : area
Design : SQUARER_8
Version: V-2004.06-SPI
Date : Tue Mar 7 21:00:01 2006

Library(s) Used:

xfga_4000e-3 (File: /CMC/tools/xilinx vM3. li/synopsys/libraries/syn/xfga_4000e-3. db)
xprim_4010e-3 (File: /CMC/tools/xilinx vM3. li/synopsys/libraries/syn/xprim_4010e-3. db)

Number of ports: 28
Number of nets: 117
Number of cells: 46
Number of references: 20

Combinational area: 0.000000
Noncombinational area: 259.000000
Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: 259.000000
Total area: undefined

Power report after Synthesis

File Edit Search Preferences Shell Macro Windows

Help

```
*****
Report : power
    -analysis_effort low
Design : SQUARER_8
Version: V-2004.06-SPl
Date   : Tue Mar  7 21:00:03 2006
*****
```

Library(s) Used:

```
xfgpa_4000e-3 { File: /CMC/tools/xilinx vM3.li/synopsys/libraries/syn/xfgpa_4000e-3.db}
xprim_4010e-3 { File: /CMC/tools/xilinx vM3.li/synopsys/libraries/syn/xprim_4010e-3.db}
```

Warning: The library cells used by your design are not characterized for internal power. (PWR-2)

Operating Conditions: WCCOM Library: xprim_4010e-3
Wire Load Model Mode: top

Design	Wire Load Model	Library
SQUARER_8	4010e-3_avg	xprim_4010e-3

Global Operating Voltage = 4.75
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, C, T units)
Leakage Power Units = Unitless

Cell Internal Power = 0.0000 mW (0%)
Net Switching Power = 22.6160 mW (100%)

Total Dynamic Power = 22.6160 mW (100%)

Cell Leakage Power = 0.0000

File Edit Search Preferences Shell Macro Windows Help

I*****

Report : timing
 -path full
 -delay max
 -max_paths 1
 Design : SQUARER_8
 Version: V-2004.06-SPI
 Date : Tue Mar 7 21:00:01 2006

Operating Conditions: WCCOM Library: xprim_4010e-3
 Wire Load Model Mode: top

Startpoint: SPREG8_1/SPREG2/DFF4/Q_INSIDE_reg
 (rising edge-triggered flip-flop clocked by CLK)
 Endpoint: DFF1/Q_INSIDE_reg
 (rising edge-triggered flip-flop clocked by CLK)
 Path Group: CLK
 Path Type: max

Des/Clust/Port	Wire Load Model	Library
SQUARER_8	4010e-3_avg	xprim_4010e-3

Point	Incr	Path
clock CLK {rise edge}	0.00	0.00
clock network delay {ideal}	0.00	0.00
SPREG8_1/SPREG2/DFF4/Q_INSIDE_reg/K {clb_4000}	0.00	0.00 r
SPREG8_1/SPREG2/DFF4/Q_INSIDE_reg/XQ {clb_4000}	4.50	4.50 r
SPREG8_1/SPREG2/DFF4/Q {DFF_0}	0.00	4.50 r
SPREG8_1/SPREG2/Z {SP_REG_4_0}	0.00	4.50 r
SPREG8_1/Z {SP_REG_8}	0.00	4.50 r
U4/PAD {iob_4000}	8.50	13.00 r
MUX1/S {MUX_2tol_5}	0.00	13.00 r
MUX1/NOT1/A {NOT_2_37}	0.00	13.00 r
MUX1/NOT1/U7/X {clb_4000}	3.15	16.15 f
MUX1/NOT1/A_NOT {NOT_2_37}	0.00	16.15 f
MUX1/AND2/B {AND_2_26}	0.00	16.15 f

File Edit Search Preferences Shell Macro Windows Help

CSA8BIT_1/RCA1/FADD4/HADD2/NAND1/B {NAND_2_16}	0.00	66.05 f
CSA8BIT_1/RCA1/FADD4/HADD2/NAND1/U8/X {clb_4000}	3.15	69.20 f
CSA8BIT_1/RCA1/FADD4/HADD2/NAND1/U7/X {clb_4000}	3.15	72.35 r
CSA8BIT_1/RCA1/FADD4/HADD2/NAND1/Z {NAND_2_16}	0.00	72.35 r
CSA8BIT_1/RCA1/FADD4/HADD2/NOT1/A {NOT_2_29}	0.00	72.35 r
CSA8BIT_1/RCA1/FADD4/HADD2/NOT1/U7/X {clb_4000}	3.15	75.50 f
CSA8BIT_1/RCA1/FADD4/HADD2/NOT1/A_NOT {NOT_2_29}	0.00	75.50 f
CSA8BIT_1/RCA1/FADD4/HADD2/C {HADDER_16}	0.00	75.50 f
CSA8BIT_1/RCA1/FADD4/OR1/B {OR_2_21}	0.00	75.50 f
CSA8BIT_1/RCA1/FADD4/OR1/U7/X {clb_4000}	7.85	83.35 f
CSA8BIT_1/RCA1/FADD4/OR1/Z {OR_2_21}	0.00	83.35 f
CSA8BIT_1/RCA1/FADD4/Cout {FADDER_8}	0.00	83.35 f
CSA8BIT_1/RCA1/Cout {RCA_4BIT_1}	0.00	83.35 f
CSA8BIT_1/MUX5/S {MUX_2tol_0}	0.00	83.35 f
CSA8BIT_1/MUX5/NOT1/A {NOT_2_8}	0.00	83.35 f
CSA8BIT_1/MUX5/NOT1/U7/X {clb_4000}	3.15	86.50 r
CSA8BIT_1/MUX5/NOT1/A_NOT {NOT_2_8}	0.00	86.50 r
CSA8BIT_1/MUX5/AND2/B {AND_2_16}	0.00	86.50 r
CSA8BIT_1/MUX5/AND2/U7/X {clb_4000}	3.15	89.65 r
CSA8BIT_1/MUX5/AND2/Z {AND_2_16}	0.00	89.65 r
CSA8BIT_1/MUX5/OR1/B {OR_2_8}	0.00	89.65 r
CSA8BIT_1/MUX5/OR1/U7/X {clb_4000}	3.15	92.80 r
CSA8BIT_1/MUX5/OR1/Z {OR_2_8}	0.00	92.80 r
CSA8BIT_1/MUX5/Z {MUX_2tol_0}	0.00	92.80 r
CSA8BIT_1/Sum<8> {CSA_8BIT}	0.00	92.80 r
DFF1/D {DFF_8}	0.00	92.80 r
DFF1/Q_INSIDE_reg/C1 {clb_4000}	0.00	92.80 r
data arrival time		92.80
clock CLK {rise edge}	96.00	96.00
clock network delay {ideal}	0.00	96.00
clock uncertainty	-0.05	95.95
DFF1/Q_INSIDE_reg/K {clb_4000}	0.00	95.95 r
library setup time	-2.42	93.53
data required time		93.53

Timing Report After Synthesis

AIMs

Ô What the CUSTOMER wants

- Ô High Quality
- Ô Low Cost
- Ô Small Size/Weight

Ô What the EMPLOYER wants

- Ô Design the:
- Ô Best
- Ô Cheapest
- Ô In shortest time
- Ô Follow the Spec or better.

Ô What you CHIP DESIGNER should do:

- Ô Design a chip with:
- Ô High speed
- Ô Small area
- Ô Low power
- Ô Testable and reliable
- Ô Delivered in a short time

Logic Design

- Ô Evaluation of library constructs (basic & macro) function, timing, area
- Ô Logic minimization
- Ô NAND/NOR transformation
- Ô Buffering
- Ô Fan-out reduction
- Ô Fan-in reduction

Logic Level design (Continued)

- Ô Critical timing
- Ô Priority routing
- Ô I/O compatibility
- Ô Logic optimization
- Ô Cost function: area, speed, power, or a combination

Logic Simulation

- Ô Simulation is the process of exercising a theoretical model of the design as a function of time for some applied input sequence
- Ô Logic simulation is to aid in verification of a digital system

Logic Simulation (Continued)

Ô Components

- | models: functional, timing
- | connectivity: a description of how the basic components are connected together
- | stimulus: 1's and 0's that are applied at specific times to the primary inputs of the design
- | simulation control

Ô States: basic (0, 1, X), strength could be combined with basic; strong (S), resistive (R), high impedance (Z), indeterminate (I)

Simulation model

- logical

```
*****  
** Library: ACME  
** Technology: 2u CMOS  
** Part: fdrc  
**  
** Description: D flip-flop with rising edge, async. Clear  
*****
```

```
model fdrc: table  
input d, rn;  
edge_sense input cp;  
output q, qn;
```

State_table

```

rn,      cp,      d,      q      ::      q,      qn;
*****
-----
```

0,	(??),	?,	?	::	0,	1,
1,	(01),	?,	?	::	(d),	!(d);
1,	(?0),	?,	?	::	N,	!(q);
1,	(1?),	?,	?	::	N,	!(q);

end (fdrc: table);

Timing Verification

- Ô Process of making accurate delay prediction and to detect timing violation in the design. These violations include set-up time, hold time, races and spikes.
- Ô Delay through the circuit is a function of:
 - | intrinsic delay
 - | number of loads connected to each net
 - | temperature
 - | voltage
 - | process variation, layout
- Ô Typically, best and worst case scenarios should be considered.

Simulator uses a set of equations to calculate exact delays

Ô Fan-out

- | $td = t(int) + K * L$
- | $t(int)$ = intrinsic delay
- | K = drive factor
- | L = sum of equivalent loads

Timing Verification (Continued)

- Ô temperature
 - M
 - td = td/FT
 - FT = (T2/T1)
- Ô voltage
 - t'd = td/[VDDr(1 + 0.0f)]
- Ô process
 - factor
 - t'd = td(1 + 0.01Fp), Fp =
= processing variation
- Ô layout information is normally supplied in two forms:
 - | pre-layout estimation
 - | post-layout: back annotation

Timing

Ô hazards

- | spikes: inertial and transport delays



$t_{PLH} = 2$

$t_{PHL} = 1$



inertial

transport



- | set-up time/hold time/minimum pulse width

Timing

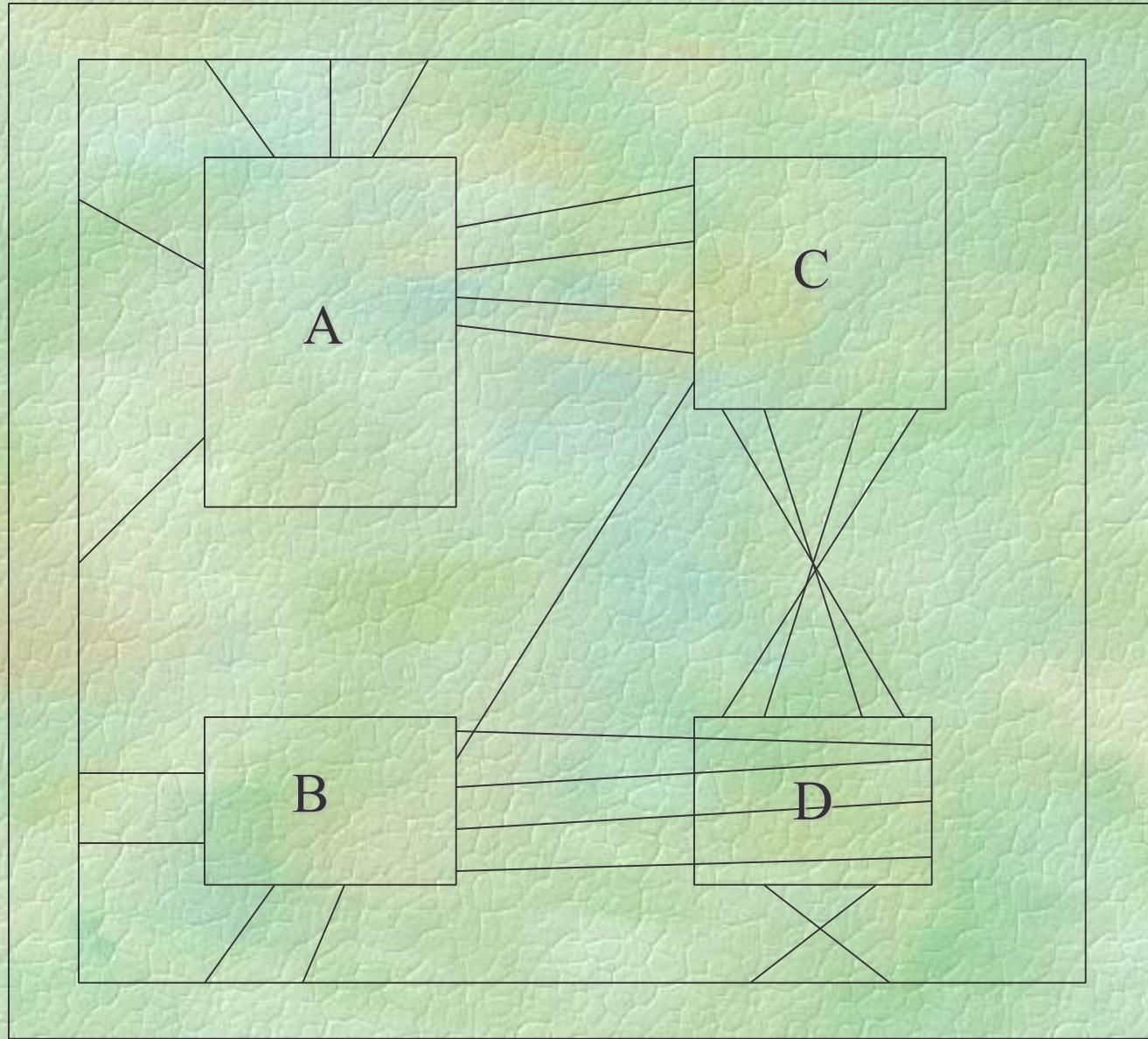
Ô Critical path analysis

- | detection of timing violation for data path structure
- | the process is simply adding up path delays and compute the result with the period of the clock at the destination (F/F)
- | path analysis is not simulation and does not utilize information about the functionality of the device
- | look for two parameters
 - hold slack = clock period - hold path time
 - set up slack = clock period - set up path time
 - slack ≥ 0
 - paths are chosen to provide the least amount of available set up or hold times

Structural layout synthesis

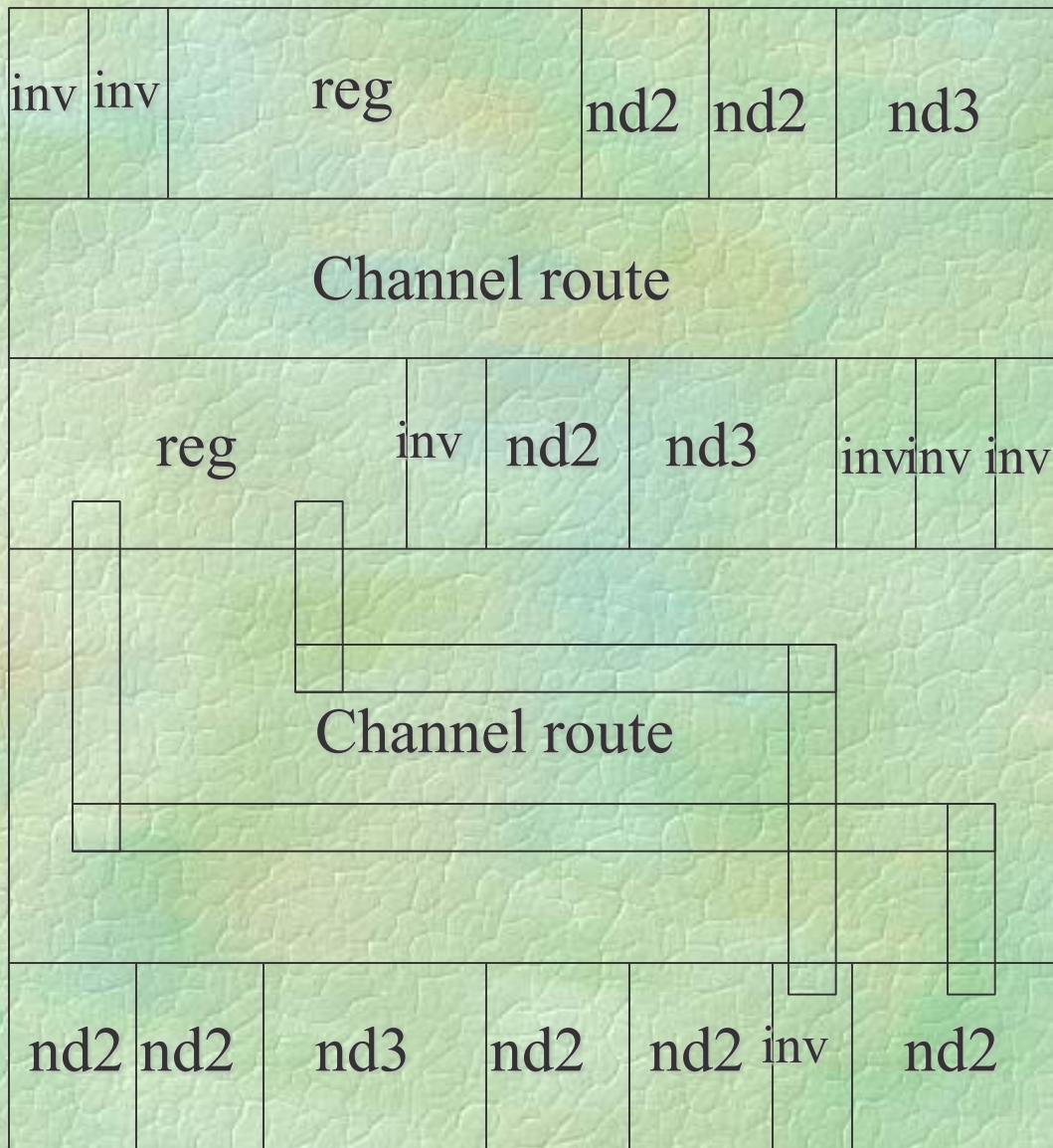
Ô Floor planning

- | it is the exercise of arranging blocks of layout within a chip to minimize area or to maximize speed
- | floor plan editors provide graphical feedback about the size and placement of modules (without showing details), also the connectivity information between the modules in the form rat's-not
- | floor planning could be done manually, or automatically with manual intervention
- | factors influencing floor planning (core & I/Os)



Placement and routing

- Ô Placement: is the task of placing modules adjacent to each other to minimize area or cycle time
- Ô two algorithms: min-cut, simulated annealing
- Ô routing: a router takes a module placement and a list of connections, connects the modules with wires
- Ô types of routers: channel, switch box, maze



Layout

Ô Other layout tools

- | synthesis
- | compaction

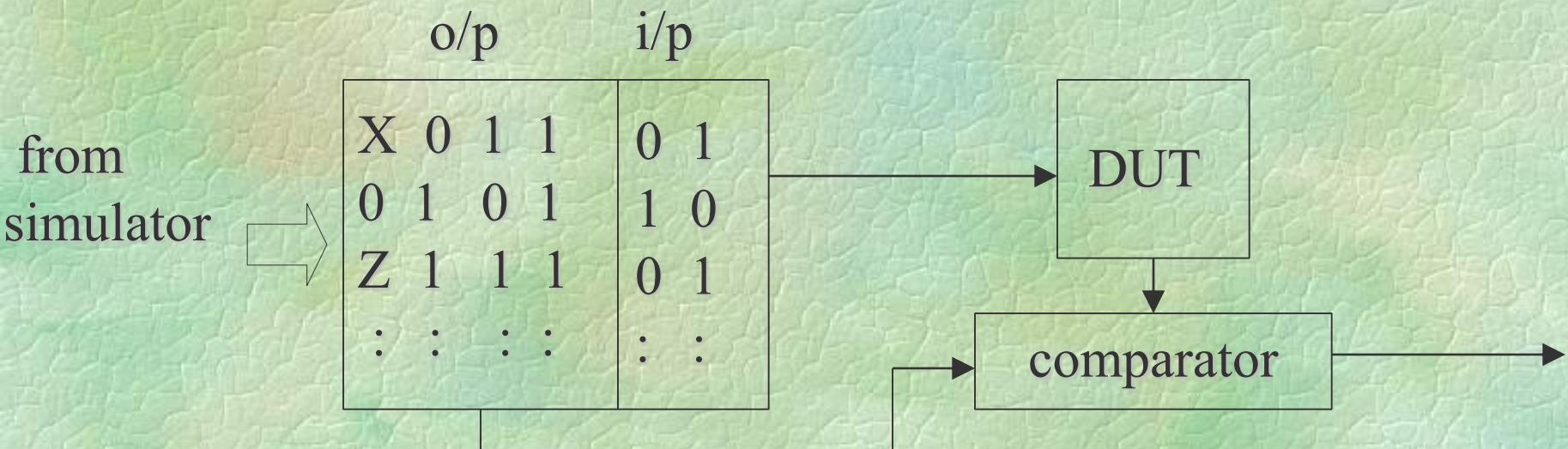
Ô Layout verification

- | design rule checking
- | layout extraction
- | layout vs. schematic

Ô Back annotation of post layout simulation

Testing

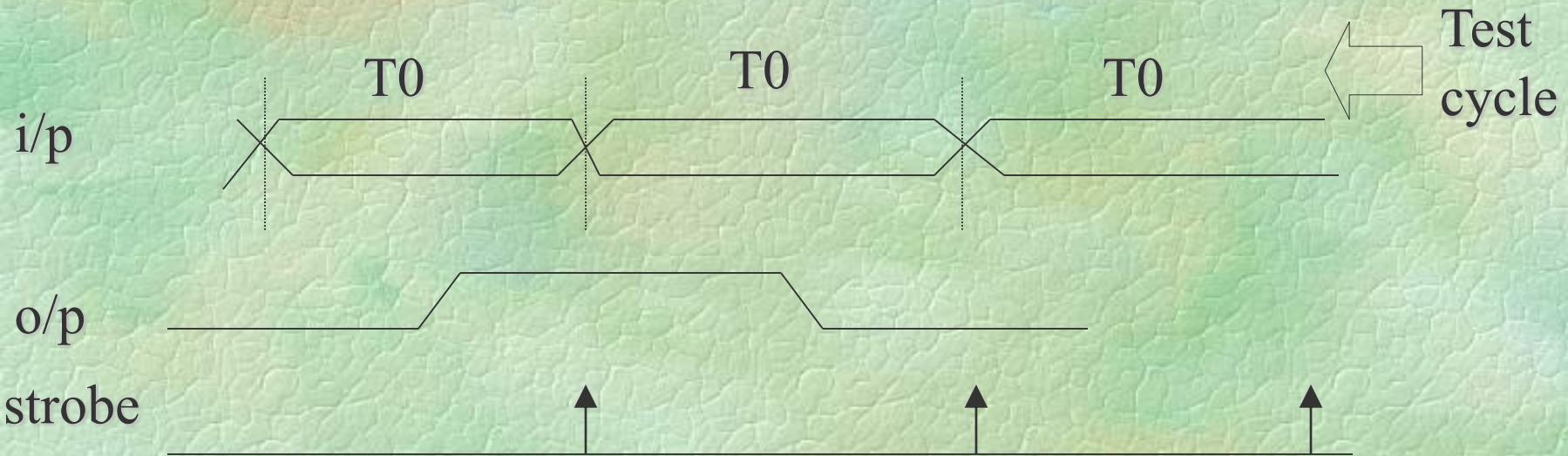
- | to verify the correct operation of the device by exercising it by a set of test patterns, and then to check the output patterns to see whether they are identical to the ones predicted by the simulator



- | tester also verifies DC and AC parameters on the pins of the device

Timing Analysis

- | Tester operates in a periodic fashion
- | input signals change states at the beginning of the test period
- | output signals are strobed at the end of the period to determine whether the measured values matches the simulated values..



Types of Testing

Functional (mostly at lower speeds)

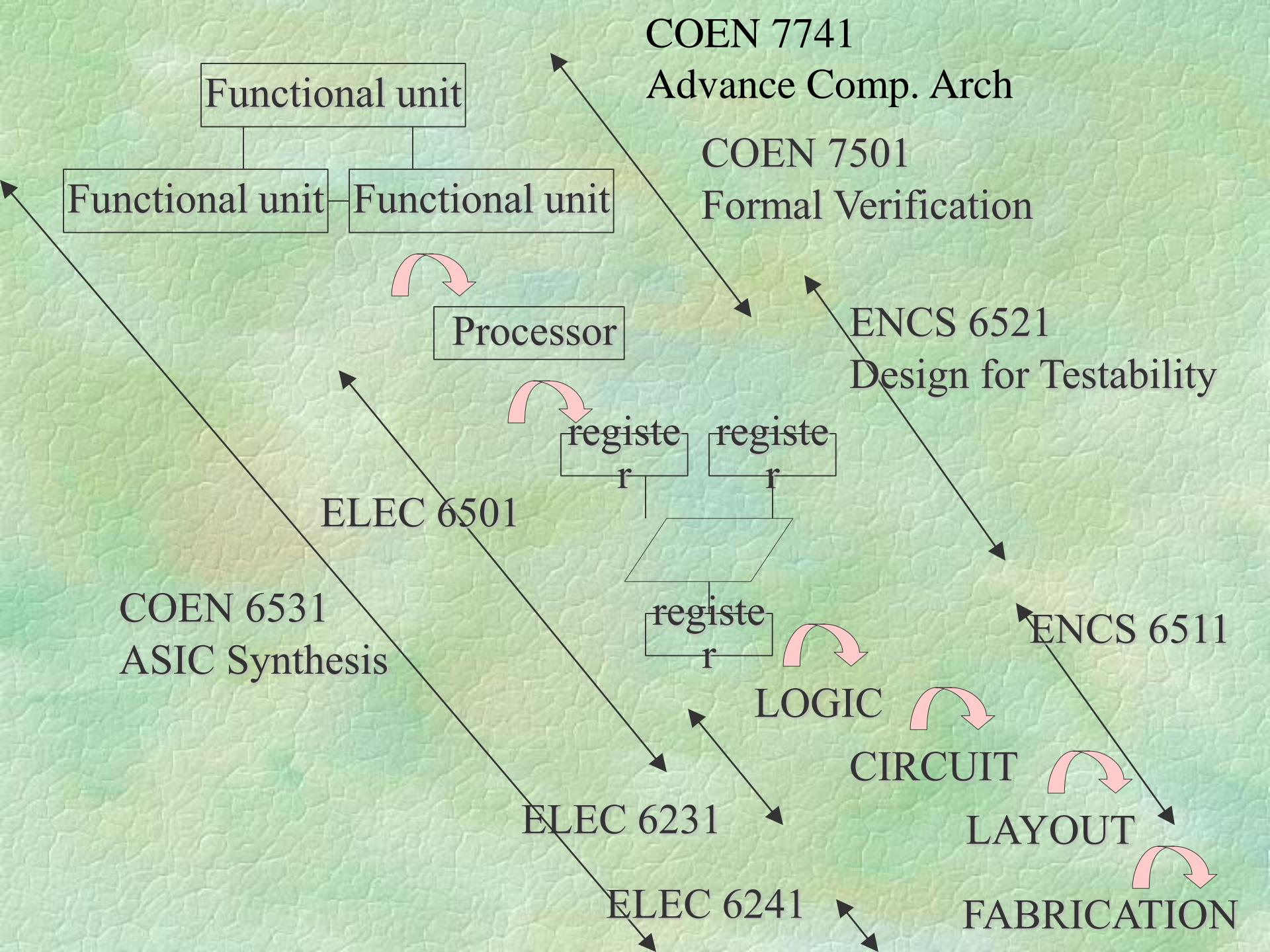
- | static
- | dynamic (refresh if required)

DC test

- | continuity
- | leakage, power consumption
- | high/low voltage levels, drive capability

AC test

- | rise/fall times, propagation delays
- | set-up and hold times, access times



Binary Arithmetic

operation	unsigned	Signed magnitude	One's complement	Two's complement
	No change	If +ve then MSB = 0 else MSB = 1	If –ve then flip bits	If –ve then flip bits, add 1
3 =	0011	0011	0011	0011
-3 =	NA	1011	1100	1101
Zero =	0000	0000 or 1000	1111 or 0000	0000
Max. +ve =	1111 = 15	0111 = 7	0111 = 7	0111 = 7

$$\text{Max. - ve} = 0000 = 0 \quad 1111 = -7 \quad 1000 = -7 \quad 1000 = -8$$

Addition = S = S = A + B
A + B =
addend +
augend SG(A)
= sign of A

Addition result : OR =
OV = overflow,
OR = out of
range COUT(MSB)
COUT is
CARRY OUT

SG(S) = NA
sign of S, S
= A + B

If SG(A) = SG(B) then S = A + B else {if B < A then S = A - B else S = B - A}

If SG(A) = SG(B) then OV = XOR{COUT(MSB), COUT(MSB - 1)}, COUT(MSB - 1)}
OV = 0 (impossible)

If SG(A) = SG(B) then SG(S) = SG(A) else {if B < A then SG(S) = SG(A) else SG(S) = SG(B)}

S = A + B + COUT(MSB)
COUT IS CARRY OUT

S = A + B
Ov = XOR{COUT(MSB), COUT(MSB - 1)}

NA

Subtraction =	$D = A - B$	$SG(B) =$ $NOT(SG(B));$ $D = A + B$	$Z = -B$ (negate); $D = A + Z$	$Z = -B$ (negate); $D = A + Z$
$D = A - B =$ minuend - subtrahend				
Subtraction result : OV = overflow, OR = out of range	OR = $BOUT(MSB)$ $BOUT$ is borrow out	As in addition	As in addition	As in addition
Negation : Z $= -A$ (negate)	NA	$Z = A;$ $SG(Z) =$ $NOT(SG(A))$	$Z = NOT(A)$	$Z = NOT(A)$ + 1

Example: design an addition overflow circuit, in accordance with the following specification:



- Ô When the operation is addition and both addend and augend are +ve, overflow is indicated by a carry from the most significant digit (MSD)
- Ô when the operation is addition and both addend and augend are -ve, overflow is indicated by the absence of carry from the MSD
- Ô when the operation is subtraction and the minuend is +ve and the subtrahend -ve, overflow is indicated by a carry from the MSD
- Ô when the operation is subtraction and the minuend is -ve and subtrahend is +ve, overflow is indicated by absence of a carry from the MSD

**THE
END**