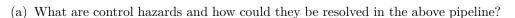
1. What advantage does a single virtual address space design offer over traditional unixstyle multiple virtual address spaces?

2. 1 2004 Paper 6 Question 2

the ARM processor allows the second operand to be shifted by an arbitrary amount. In order to improve the performance, a six-shage pipeline is proposed with the following stages:

instruction	decode and	shift	execute	memory	register
fetch	register fetch	operand 2		access	write back



- (b) What are data hazards and how could they be resolved in the above pipeline?
- (c) What are feed-forward paths and where could they be added to the above pipeline to improve performance?
- (d) Why might a branch instruction result in pipeline bubbles and how many bubbles will appear in the above pipeline as a result of taking a branch instruction?
- 3. Using your summer work as a starting point, describe what each of the following terms mean and why it is important to CPU cache design (hint: for each principle of cache design, give an example use case when it is very appropriate and when it is very inappropriate)
 - (a) A write-back policy
 - (b) A write-through policy
 - (c) A write-around policy
 - (d) A victim buffer
 - (e) write-merging/combining/collapsing/coalescing
 - (f) A virtually-addressed cache
 - (g) A physically addressed cache
 - (h) Cache coherency
 - (i) A cacheline dirty bit
 - (j) Direct-mapped caching
 - (k) Set-associative caching



https://www.cl.cam.ac.uk/ teaching/exams/pastpapers/ y2004p6q2.pdf