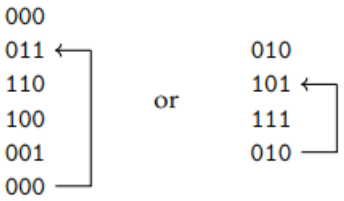
1. A sequential circuit has been built using D-type flip flops. It behaves slightly erratically. When switched on, it produces on its three output wires one of the following patterns:



Deduce the circuit details by drawing the next-state table and working out a minimised sum-of-products expression for the input to each of the three state registers (CBA). Propose a modification that ensures that in due course the circuit will always settle into the cycle shown in the first pattern. Show a Karnaugh map for each flip-flop input before and after your modification, and use them to highlight the change.

The patterns show that this circuit is non-self starting – and the task is to find the circuit which resulted in these two patterns and modify it so that the circuit IS self-starting.

Let the state be CBA and the next state as $C'B'A'$. Combining the next state results for both diagrams gives the following three Karnaugh maps for the flip flops.

C'

		CB			
		00	01	11	10
A	0	0	1	0	1
	1	1	0	1	0

From the Karnaugh map:

$$\begin{aligned} C' &= CBA + CB\bar{A} + C\bar{B}A + \bar{C}BA \\ C' &= C \oplus B \oplus A \end{aligned} \tag{1}$$

B'

		CB			
		00	01	11	10
A	0	0	1	1	1
	1	0	0	0	1

From the Karnaugh map:

$$B' = C\bar{B} + B\bar{A} \tag{2}$$

A'

		CB			
		00	01	11	10
A	0	1	1	1	0
	1	0	0	1	0

From the Karnaugh map:

$$A' = CB + \bar{C}\bar{A} \tag{3}$$

I noticed that if FF B only goes to 1 when it is in a state in the first loop, then the second loop will go into the first loop and hence the circuit will self-start. I chose to

modify B because it gave the expression which required the least modification to the previous expression. This would make it the easiest change. It was also one of the few modifications that actually reduced the number of gates in the expression.

A simple modification that would make the circuit self-start (and hence prevent the second, unintended loop) would be changing the expression for B' (2) to

$$B'' = C\bar{A} \tag{4}$$

This does not affect the first loop, however the circuit now self-starts:

$$\begin{aligned} &010 \to 000 \\ &101 \to 000 \\ &111 \to 101 \to 000 \end{aligned} \tag{5}$$

So the new equation for the next states ($C''B''A''$) is:

$$\begin{aligned} C'' &= C \oplus B \oplus A \\ B'' &= C\bar{A} \\ A'' &= CB + \bar{C}\bar{A} \end{aligned} \tag{6}$$

C''

		CB			
		00	01	11	10
A	0	0	1	0	1
	1	1	0	1	0

B''

		CB			
		00	01	11	10
A	0	0	0	1	1
	1	0	0	0	0

A''

		CB			
		00	01	11	10
A	0	1	1	1	0
	1	0	0	1	0

2. (a) Explain (in your own words, no diagrams, bullet points are fine) how to modify the simple single cycle processor to permit data memory access.

   Perform the current calculation. Take the result from the ALU and use it to address a location in data memory. Then put the result from the memory access into a multiplexer with the result straight from the ALU. The multiplexer then controlls whether the result stored in the register should be from memory or the result of the calculation.

   (b) Explain (in your own words, no diagrams, bullet points are fine) how to modify the simple single cycle processor to permit branching.

   When loading the next result into memory, there is an adder which will increment the current address in the program counter. Call this output (a). Put (a) into another adder which adds an offset (taken from an instruction decoder). Then put this into a MUX with (a) to give the option of branching.

(c) Change two words in order to correct the following sentence: *Instruction throughput is usually lower in a multicycle processor (compared to a single cycle processor) and multi-cycle processors make less effective use of available chip area.*

*Instruction throughput is usually **higher** in a multicycle processor (compared to a single cycle processor) and multi-cycle processors make **more** effective use of available chip area.*

(d) Change two words in order to correct the following sentence: *A pipelined processor reduces throughput (compared to a multicycle processor) and decreases per-instruction latency*

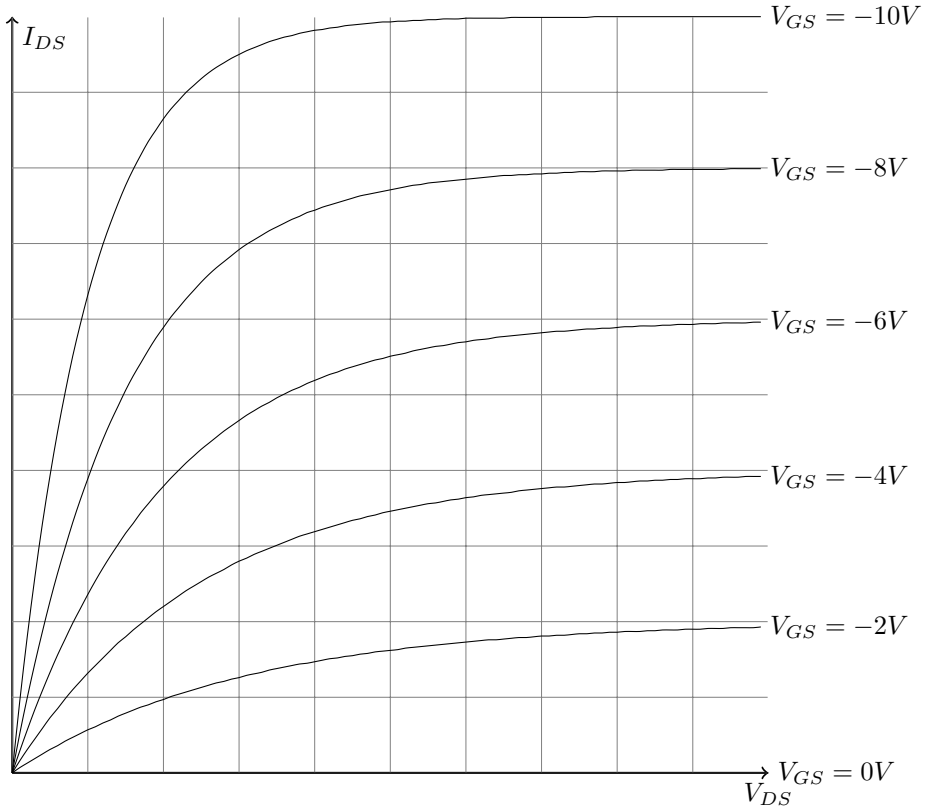
*A pipelined processor **increases** throughput (compared to a multicycle processor) and **increases** per-instruction latency*

3. 1 2012 Paper 2 Question 2

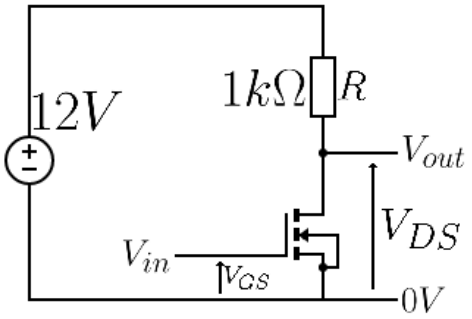
https://www.cl.cam.ac.uk/teaching/exams/pastpapers/y2012p2q2.pdf

(a) With the aid of appropriate diagrams, show how the Source–Drain current that flows in a p-channel MOSFET is controlled by the applied Gate–Source voltage.

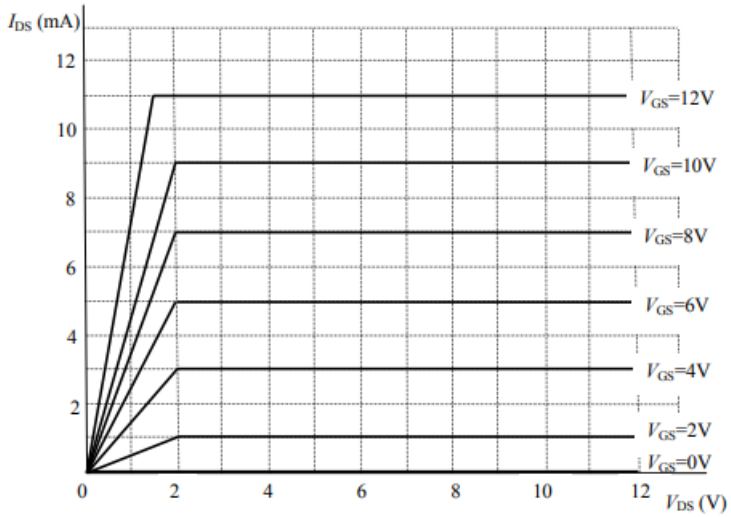
In a p-channel MOSFET, the Source has a positive voltage. Only if the Gate has a lower voltage than the source can current flow (and the transistor turn on). The transistor is off when the voltage of the gate with respect to the source is $0V$ (or positive).
When current is flowing, the transistor is on. This means that a lower voltage in the Gate than in the source turns the transistor on.



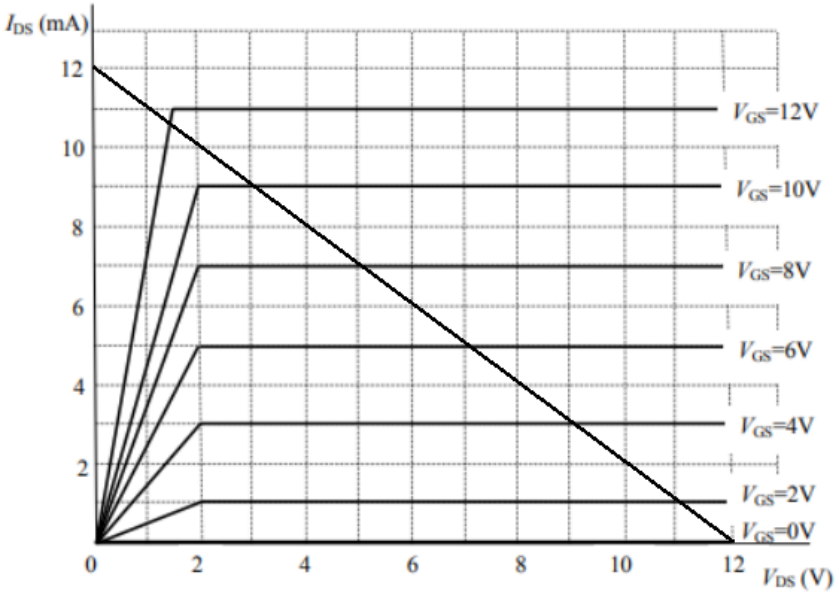
(b) (i) Draw the circuit diagram of a NOT gate that comprises an n-channel MOSFET and a resistor R.



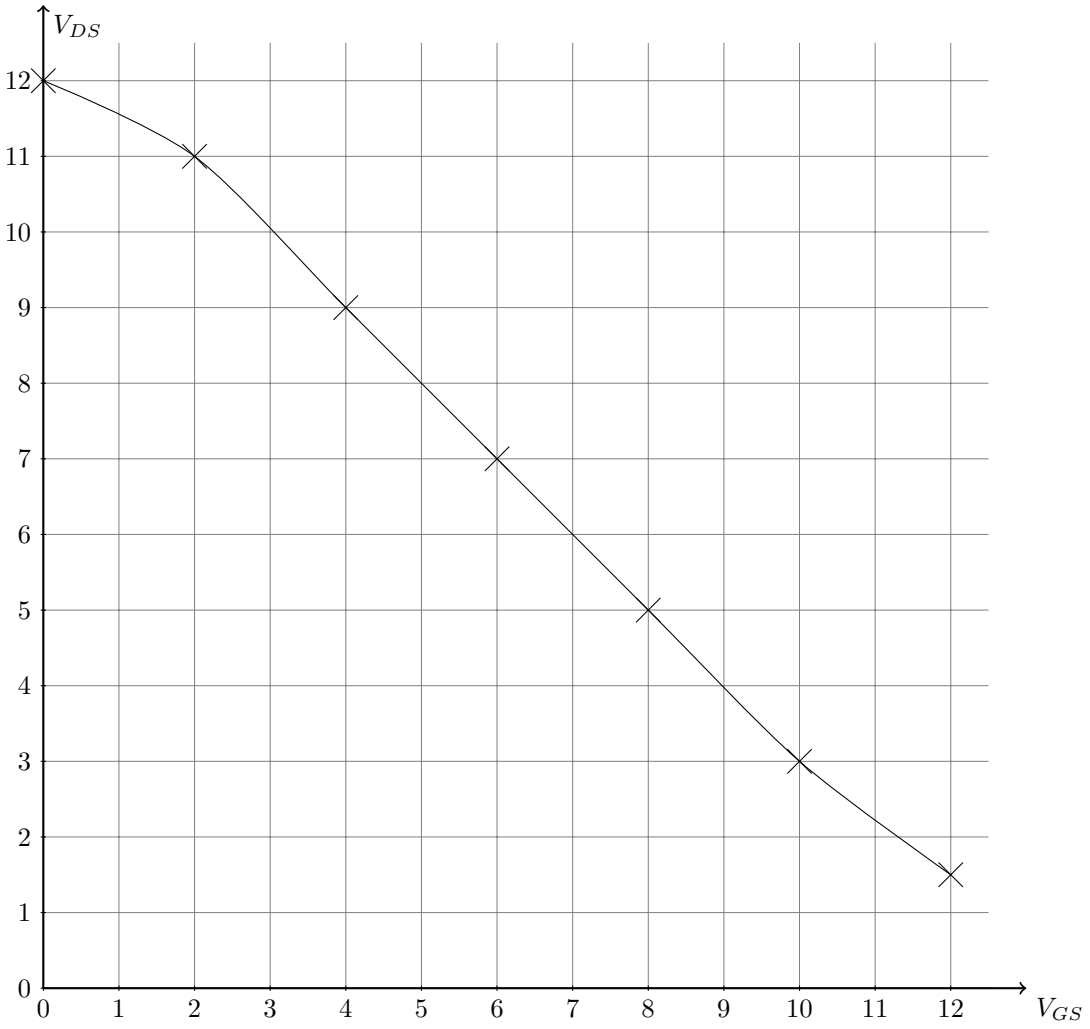
(ii) For the NOT gate in (b)(i), plot the relationship between the input voltage, Vin and the output voltage, V_{out}. Assume that the power supply voltage $V_{DD} = 12$ V, $R = 1$ $k\Omega$, and that the MOSFET has the characteristics given in the following figure.



Using the graphical method:



Plotting V_{out} of the intersections against V_{GS}.



(c) For the NOT gate in (b), calculate the power dissipated by the entire gate and that by resistor R alone, when $V_{in} = 12$ V.

When $V_{in} = 12V$; $V_{GS} = 12V$. Reading off the graph in 3.(b)(ii) gives $I_{DS} = 10.6mA$.

The voltage across the circuit is $12V$.
So using the equation $P = IV$ gives:

$$\begin{aligned} P_t &= I_{DS}V_{in} \\ &= 10.6mA \times 12V \\ &= 10.6 \times 10^{-3} \times 12 \\ &= 127.2 \times 10^{-3}W \\ &= 127.2mW \\ &\approx 127mW \text{to 3.S.F} \end{aligned} \tag{7}$$

So the total power dissipated in the circuit is $\approx 127mW$.

The current flowing through the resistor is $10.6mA$

Using the equation for power gives the power dissipated in the resistor is:

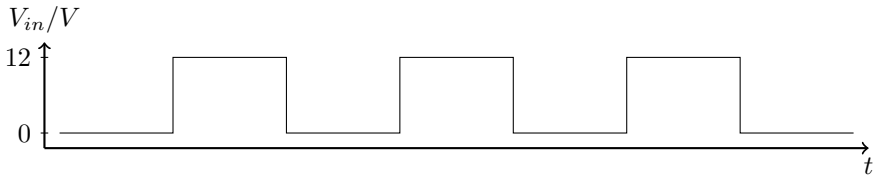
$$\begin{aligned} P_r &= I^2R \\ &= 10.6mA^2 \times 1k\Omega \\ &= 112.36 \times 10^{-6} \times 1 \times 10^3 \\ &= 112.36 \times 10^{-3}W \\ &= 112.36mW \\ &\approx 112mW \text{to 3.S.F} \end{aligned} \tag{8}$$

So the power dissipated by resistor R is $\approx 112mW$

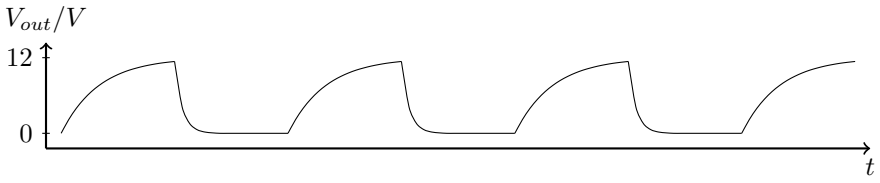
(d) The stray capacitance present at the output of the NOT gate in (b) can be represented by a capacitor, C = 100 nF connected between the gate output and 0 V. Also assume that the MOSFET has an ON resistance Ron = 100 Ω. The input signal, V_{in}, is a 1 kHz square wave with minimum and maximum amplitudes of 0 V and 12 V respectively.

(i) Sketch the output signal waveform, Vout, of the NOT gate being sure to include indicative rise and fall times and voltage levels.

Input signal waveform:



Output signal waveform:



(ii) How could the rise-time of V_{out} be reduced and what would be the impact of your proposed solution on the power dissipation of the circuit?

The rise-time of V_{out} could be reduced by decreasing the resistance of the resistor R. This would decrease the time constant RC and so V_{out} would rise quicker.
But it would increase the power dissipated in the circuit. Since $P = \frac{V^2}{R}$ and V is constant: $P \propto \frac{1}{R}$. So a decrease in R will increase the power dissipated in the circuit.

4. A CMOS inverter circuit is shown in part (a) of the figure below. The characteristic of the p-type MOSFET T1 is shown in part (b). The characteristic of the n-type MOSFET T2 is shown in part (c).

(a) Determine the output voltages V_o corresponding to input voltages V_i of 0 V and 10 V (low and high inputs).

When the input voltage, V_i is $0V$: V_{GS} for the PMOS is $-10V$ and V_{GS} for the NMOS is $0V$. V_{out} is $10V$.

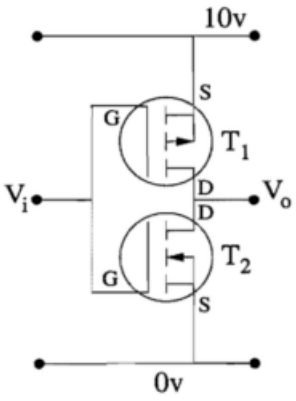
When the input voltage, V_i is $10V$: V_{GS} for the PMOS is $0V$ and V_{GS} for the NMOS is $10V$. V_{in} is $0V$.

(b) Check that the power dissipated in each transistor for high and low inputs is negligible.

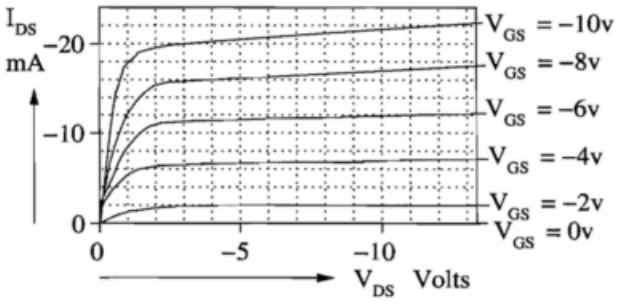
When V_i is low: the NMOS is off and the PMOS is on. This means that there is not a complete circuit. So current does not flow. Since $P = \frac{I^2}{R}$; and $I = 0$, the power dissipated is negligible.

When V_i is high: the PMOS is off and the NMOS is on. This means that there is not a complete circuit and so current cannot flow. Since $P = \frac{I^2}{R}$; and $I = 0$, the power dissipated is negligible.

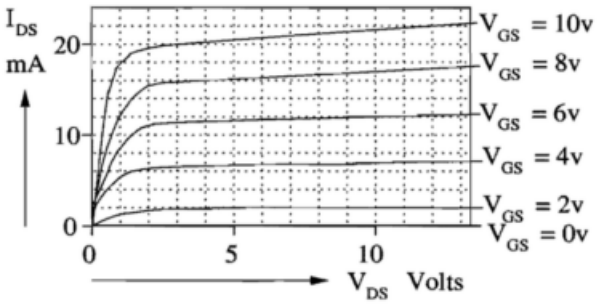
(c) If, due to a faulty lead, the input is floating at becomes +4 V, determine V_o, the power dissipated in each transistor, and the power taken from the supply.



(a)



(b) PMOS Characteristics



(c) NMOS Characteristics

If the input is $+4V$, then V_{GS} for the P-MOS is $-6V$ and V_{GS} for the N-MOS is $4V$.

So $V_o = 6V$. So V_{DS} for the N-MOS is $6V$. On the circuit diagram, this means that the current flowing through the N-MOS is $7mA$. So the power dissipated in the N-MOS is:

$$\begin{aligned} P_{nmos} &= I_{nmos} \times V_{nmos} \\ &= 7mA \times 6V \\ &= 42mW \end{aligned} \tag{9}$$

V_{DS} for the P-MOS is $10V - 6V = 4V$. Reading off the characteristic graph: at this V_{DS} with a V_{GS} of $-6V$: the current flowing through the P-MOS is $11.5mA$.

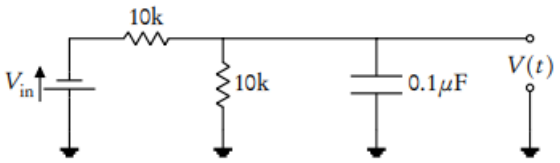
So the power dissipated in the P-MOS is:

$$\begin{aligned} P_{nmos} &= I_{pmos} \times V_{pmos} \\ &= 11.5mA \times 4V \\ &= 46mW \end{aligned} \tag{10}$$

The power taken from the supply is equal to the sum of the power dissipated across both of the transistors.

$$\begin{aligned} P_{supply} &= P_{nmos} + V_{pmos} \\ &= 42mW + 46mW \\ &= 88mW \end{aligned} \tag{11}$$

5. Find and sketch $V(t)$ in the following circuit (start from first principles, i.e. Kirchoff's laws, Ohm's law, the definition of capacitance, current, etc.):



V(t) measures the voltage across the $0.1\mu F$ capacitor.

Initially, the upper $10k\Omega$ resistor dominates the resistance in the circuit. So initially the voltage across the capacitor is $0V$. As the capacitor charges up, the voltage across it will increase. However, since there are two resistors and the capacitor is only in parallel with one of them: the voltage across the capacitor will never exceed the voltage across the second resistor.
Using the potential divider equation:

$$\begin{aligned} V_{max} &= V_{in} \times \frac{10k\Omega}{10k\Omega + 10k\Omega} \\ &= V_{in} \times \frac{1}{2} \\ &= \frac{V_{in}}{2} \end{aligned} \tag{12}$$

So the capacitor starts at $0V$ and charges to a maximum of $\frac{V_{in}}{2}$.

Using the equation for a charging capacitor:

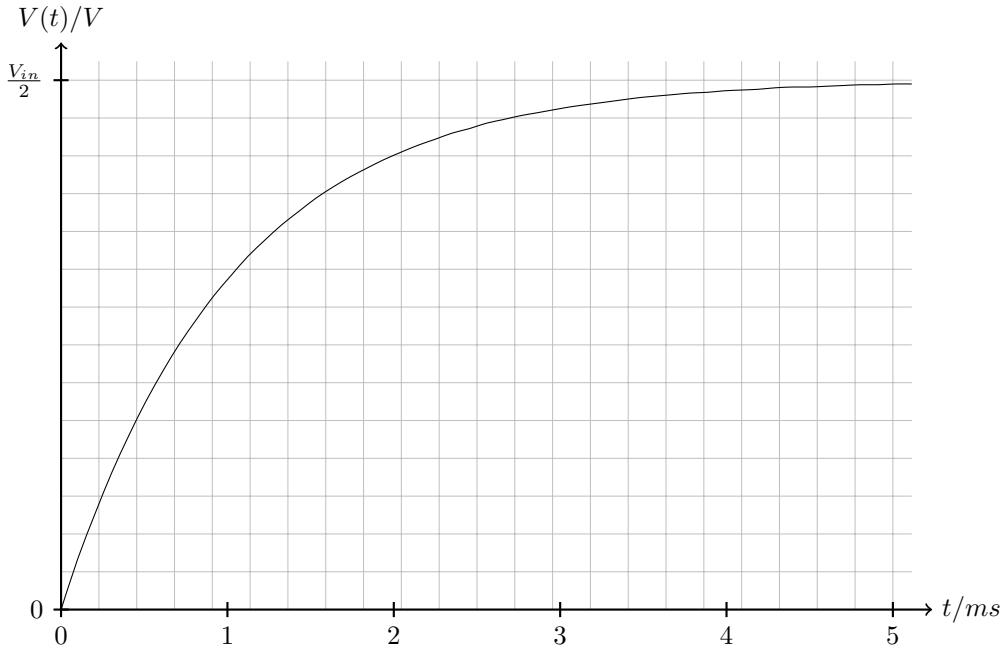
$$\begin{aligned} V &= V_0(1 - e^{-\frac{t}{\tau}}) \\ &= V_0(1 - e^{-\frac{t}{RC}}) \\ &= V_0(1 - e^{-\frac{t}{10k\Omega 0.1\mu F}}) \\ &= V_0(1 - e^{-\frac{t}{1ms}}) \end{aligned} \tag{13}$$

Substituting this into the previous equation gives:

$$V = \frac{V_{in}}{2}(1 - e^{-\frac{t}{1ms}})$$

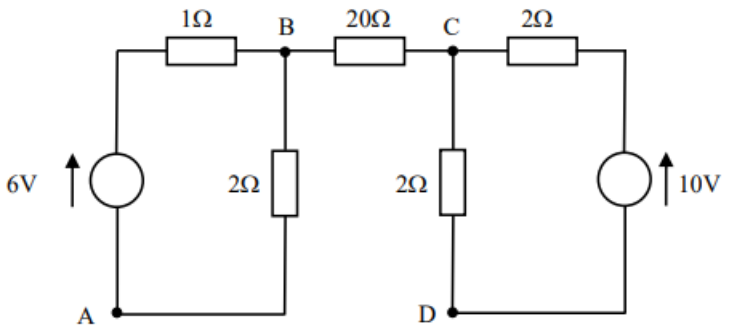
Add actual times onto this. You know RC so can do that.
This graph contains times up to 5RC.

V(t) is the voltagea across the capacitor. So the question is asking us to plot a graph of the voltage across the capacitor.



The two questions which were removed from the supervision work are included below.

1. For the following circuit



(a) What is the current flowing through the 20Ω resistor?

The current flowing through the 20Ω resistor is $0A$.
This is because although the two circuits are connected, they do not have a route back. So if there was a current flowing through the 20Ω resistor then one cell would have a greater current flowing out than in and the other cell would have a lower current flowing out than in. Which would violate Kirchoff's 1^{st} law.

(b) Find the voltage at nodes B, C, and D with respect to node A, i.e., V_{AB}, V_{AC} and V_{AD}.

(V_{AB}) Since there is no current flowing through the 20Ω resistor, we can consider the left hand circuit as a separate circuit when considering V_{AB}.

The total resistance of the left hand circuit is 3Ω ($1\Omega + 2\Omega$).
The voltage supplied to the left hand circuit is $6V$.

So using Ohm's Law:

$$\begin{aligned} V &= IR \\ I &= \frac{V}{R} \\ I &= \frac{6V}{3\Omega} \\ I &= 2A \end{aligned} \tag{14}$$

Since we are considering V_{AB}, we must consider the reverse voltage over the 2Ω resistor. So V_{AB} = - $V_{R_{2\Omega}}$.

$$\begin{aligned} V_{R_{2\Omega}} &= IR \\ &= 2A \times 2\Omega \\ &= 4V \\ V_{AB} &= -V_{R_{2\Omega}} \\ \therefore V_{AB} &= -4V \end{aligned} \tag{15}$$

(V_{AC}) There are no components between A and the LHS Cell. So the voltage at A is $0V$. The voltage V_{AC} is the voltage at A minus the voltage at C. This is equivalent to the negative of the voltage at C.

In the right-hand circuit:

$$\begin{aligned} V &= IR \\ I &= \frac{V}{R} \\ I &= \frac{10V}{2\Omega + 2\Omega} \\ I &= \frac{5}{2}A \\ V_{CD} &= IR \\ V_{CD} &= \frac{5}{2}A \times 2\Omega \\ V_{CD} &= 5V \\ V_{AC} &= -V_{CD} \\ \therefore V_{AC} &= -5V \end{aligned} \tag{16}$$

(V_{AD}) There are no components between D and the battery. So the voltage at D is $0V$. Since the voltage at A is also $0V$; The voltage at D with respect to A is $0V$.
$\therefore V_{AD} = 0V$.

2. The op-amp based amplifiers shown in Fig. 2 (a) and (b) are used to boost the +/- 100mV signal at the output of a transducer so that suits the +/- 5V input voltage range of an analogue to digital converter (ADC).

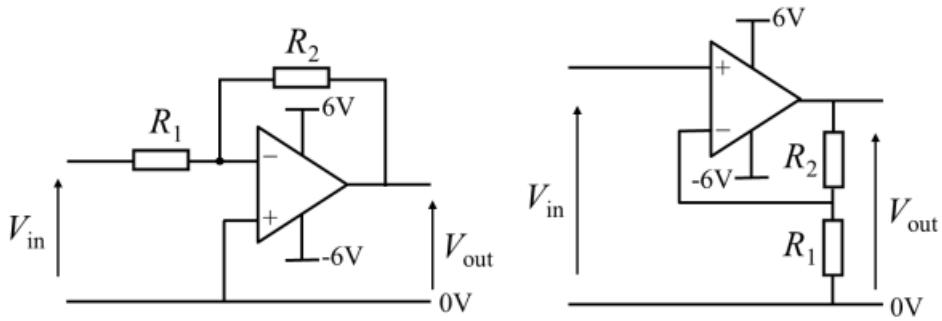


Figure 2 (a) (b)

(a) What voltage gain is required?

In the first circuit (Fig. 2 (a) – an inverting amplifier); the voltage gain needs to be $-5.1V$.
The second equation (Fig. 2 (b) – a non-inverting amplifier); the voltage gain required is $4.9V$.

(b) For the inverting and non-inverting amplifiers in Fig. 2 (a) and (b) respectively, select the value of R_2 if $R_1 = 1k\Omega$.

The formula for the output voltage from an inverting amplifier (such as in Fig. 2 (a)) is:

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \tag{17}$$

Given that $V_{out} = -5V$, $V_{in} = 100mV$ and $R_1 = 1k\Omega$:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= -\frac{R_2}{R_1} \\ \frac{-5V}{0.1V} &= -\frac{R_2}{1k\Omega} \\ -50 \times 1k\Omega &= -R_2 \\ 50k\Omega &= R_2 \end{aligned} \tag{18}$$

So the value of R_2 in Fig. 2 (a) is $50k\Omega$.

The formula for the output voltage from a non-inverting amplifier (such as in Fig. 2 (b)) is:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{19}$$

Given that $V_{out} = -5V$, $V_{in} = 100mV$ and $R_1 = 1k\Omega$:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= 1 + \frac{R_2}{R_1} \\ \frac{5V}{0.1V} &= 1 + \frac{R_2}{1k\Omega} \\ 50k\Omega &= 1k\Omega + R_2 \\ 49k\Omega &= R_2 \end{aligned} \tag{20}$$

So the value of R_2 in Fig. 2 (b) is $49k\Omega$.

(c) What problem arises if the transducer output voltage exceeds $+/-120mV$?

An op-amp scales up the input by a given factor.
For this specific op-amp, that factor is $50\times$. However, the maximum voltage which it can output is limited by the supply voltage. The supply voltage for this op-amp is $+/-6V$. So the maximum ouput voltage from these op-amps is $+/-6V$. If the transducer output voltage (which is the op-amps input) is greater than $+/-120mV$, then the voltage which the op-amp *should* output (the transducer output voltage $\times$ 50) is greater than $+/-6V$ so the op-amp cannot output that high a voltage. So the voltage output by the op-amp is not the right voltage.
IE if the transducer output voltage was $200mV$, then the op-amp output voltage should be $10V$. However, it will only output $6V$.

In short: if the transducer output voltage exceeds $+/-120mV$, the voltage of the power supply is too low and prevents the op-amp from outputting the appropriate voltage.