Everywhere you imagine. RENESAS

Introduction of

Renesas Technology Corp.

Mobile Sales & Marketing Division
Local Business Group

28th Aug, 2007

Renesas Confidential

070828 for Chinese customers

What is MIPI ?

MIPI - Mobile Industry Processor Interface
(移动通信行业处理器接口)

MIPI Alliance founded by ARM, Nokia, STMicroelectronics and Texas Instruments in July 2003

- **The number of member companies : ~150 companies now**
  - Management Board : 7 companies
    (Nokia, Motrola, Intel, Samsung, STMicro, TI, NXP)
  - Contributors : 50 companies
    (Renesas…)
  - Adopters : 89 companies
    (Himax, ILI…)

http://www.mipi.org

The Needs for Mobile Industry Standards

- Fragmentation in mobile industry
- Increasing complexity of system designs
- Limited engineering resources need to focus on delivering maximum ROI (Return On Investment)
- Accelerating time-to-market demands

MIPI Benefits the Entire Mobile Industry

Benefits to Component Suppliers

- Better industry alignment on physical interfaces among processors and peripheral devices
- Broader spectrum of hardware and software solutions to complement each vendor's products
- Rapid definition and adoption of new interfaces to meet evolving system requirements.

Benefits to Mobile Device Suppliers

- Rapid innovation & improved time to market by reducing system design complexity
- Maximum application software portability due to common hardware & software interfaces
- Wider availability of optimized peripheral devices like LCD's, Cameras, and Communications ICs

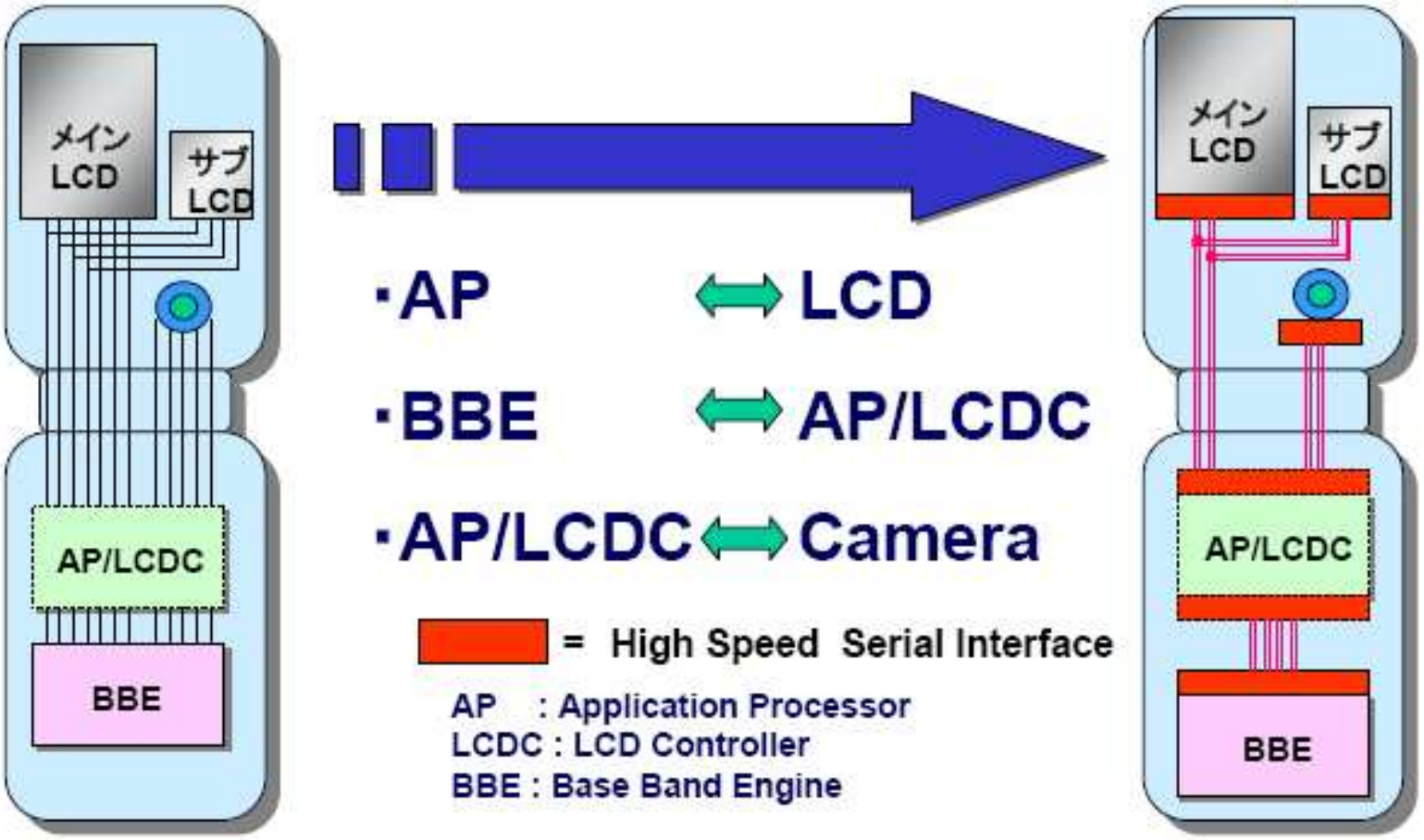
Benefits to OS Vendors

- Common hardware and software interfaces provide standard view toward the OS
- Maximum reuse & commonality in the OS port

Benefits to Consumers

- Advancements in mobile device technologies will reach the market sooner

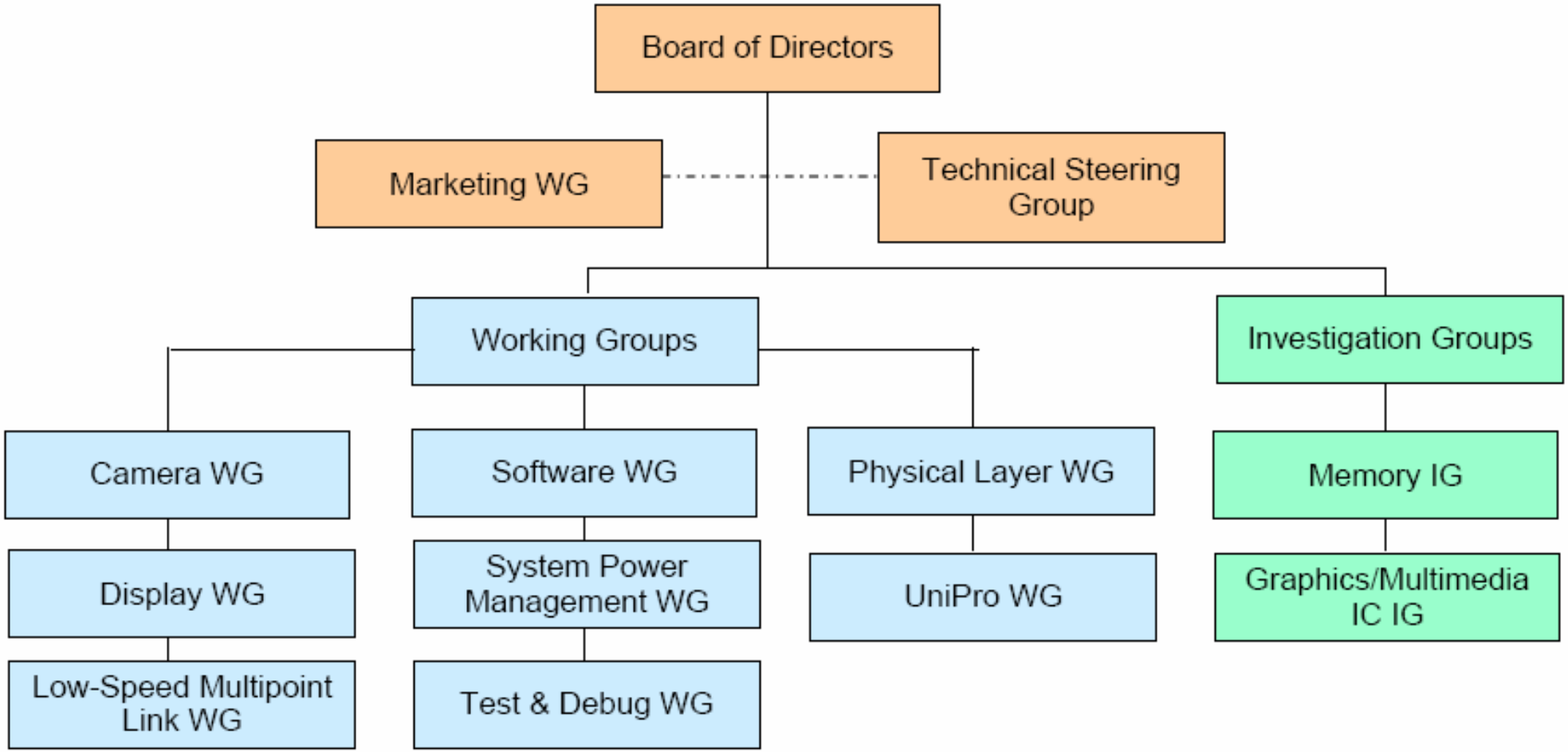
Conventional & High-speed



Conventional I/F

High-speed I/F

Organizational Structure



Working group

(~ for Display)

- **DWG–Display Working Group**
  - **DCS - Display Command Set**
  - **DBI - Display Bus Interface -> CPU BUS IF**
  - **DPI - Display Pixel Interface -> RGB IF**
  - **DSI - Display Serial Interface -> High Speed Serial IF**

- **PHY-WG**
  - **D-PHY : Points to Points, Up to 1Gbps**
  - **M-PHY : Multi-points, Over 1Gbps (Future Spec)**

DCS-Display Command Set

◆DCS – Display Command Set

The comparison for Command List between MIPI DCS and Nokia I/F – 1/2

MIPI DCS Command List			Nokia I/F Command List	
Command	Hex Code	Description	Operational Code	Function
nop	00h	No Operation	00h	No Operation
soft_reset	01h	Software Reset	01h	Software reset
-	-	-	04h	Read Display Identification
get_red_channel	06h	Get te red component of the pixel at (0,0).	-	-
get_green_channel	07h	Get the green component of the pixel at (0,0)	-	-
get_blue_channel	08h	Get the blue component of the pixel at (0,0)	-	-
-	-	-	09h	Read Display status
get_power_mode	0Ah	Get the current power mode	0Ah	Read Display Power mode
get_address_mode	0Bh	Get the frame memory to the display panel read order	0Bh	Read Display MADCTLR2
get_pixel_format	0Ch	Get the current pixel format	0Ch	Read Display Pixel Format
get_display_mode	0Dh	Get the current display mode from the peripheral	0Dh	Read Display Image Mode
get_signal_mode	0Eh	Get display module signaling mode	0Eh	Read Display Signal Mode
get_diagnostic_result	0Fh	Get Peripheral Self_Diagnostic Result	0Fh	Read Display Self
enter_sleep_mode	10h	Power for the display is off	10h	Sleep in
exit_sleep_mode	11h	Power for the display is on	11h	Sleep out
enter_partial_mode	12h	Part of the display area is used for image display	12h	Partial Mode On
enter_normal_mode	13h	The whole display area is used for image display	13h	Normal Display Mode On
exit_invert_mode	20h	Displayed image colors are not inverted	20h	Display Inversion off
enter_invert_mode	21h	Displayed image colors are inverted	21h	Display Inversion on
set_gamma_curve	26h	Selects the gamma curve used by the display device	26h	Gamma Set W format: 1byte for curve selection
set_display_off	28h	Blanks the display device	28h	Display off
set_display_on	29h	Show the image on the display device	29h	Display on
set_column_address	2Ah	Set the column extent	2Ah	Column Address Set
set_page_address	2Bh	Set the page extent	2Bh	Page Address Set
write_memory_start	2Ch	Transfer image data from the Host Process to the peripheral starting at the location provided by set_column_address and set_page_address	2Ch	Memory Write

◆DCS – Display Command Set

The comparison for Command List between MIPI DCS and Nokia I/F – 2/2

MIPI DCS Command List			Nokia I/F Command List	
Command	Hex Code	Description	Operational Code	Function
write_LUT	2Dh	Fills the peripheral look-up table with the provided data	2Dh	Colour set
read_memory_start	2Eh	Read image data from the peripheral to the Host Processor interface starting at the location provided by set_column_address and set_page_address	2Eh	Memory Read
set_partial_area	30h	Defines the partial display area on the dosplay device	30h	Partial area set
set_scroll_area	33h	Defines the vertical scrolling and fixed area on display device	33h	Verttical scrolling area set
set_tear_off	34h	Synchronization information is not sent from the display module to the host processor	34h	Tearing Effect Line Off
set_tear_on	35h	Synchronization information is sent from the display module to the host processor	35h	Tearing Effect Line On
set_address_mode	36h	Set the read order from frame memory to the display panel	36h	Set Memory Acess Control for memor scan direction
set_scroll_start	37h	Defines the vertical scrolling starting point	37h	Vertical scrolling start
exit_idle_mode	38h	Full color depth is used on the display panel	38h	Idle Mode off
enter_idle_mode	39h	Reduced color depth is used on the diplay panel	39h	Idle Mode on
set_pixel_format	3Ah	Defines how many bits per pixel are used in the interface	3Ah	Interface pixel format
write_memory_continue	3Ch	Transfer image information from the Host Processor interface to the peripheral from the last written location	-	-
read_memory_continue	3Eh	Read image data from the peripheral continuing after the last read_memory_continue or read_memory_start.	-	-
set_tear_scanline	44h	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the Provided scanline.	-	-
get_scanline	45h	Get the current scanline	-	-
Read_DDB_start	A1h	Read the DDB from the provided location	-	-
Read_DDB_continue	A8h	Continure reading the DDB from the last read location	-	-
-	-	-	DAh	Read ID1
-	-	-	DBh	Read ID2
-	-	-	DCh	Read ID3

Example

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- **User Command**
  1) Sleep in (10h) – No parameter
  2) Column Address Set(2Ah) – 4 parameters
  3) …….

- **Manufacturer Command**
  1) Entry mode(B4h) – 1 parameter
  2) Gamma set (E9h) – 16 parameters
  3) ……

DBI-Display Bus Interface
&
DPI-Display Pixel Interface

Display Architectures

Functions			Display Architectures			
			Type 1	Type 2	Type 3	Type 4
Display Device			○	○	○	○
Display Driver	Interface	Control Interface	○	○	○	
		Video Stream Interface		○	○	○
		Control Lines				○
	Memories & Registers	Full-frame memory	○			
		Partial memory		○		
		Non-volatile memory	○	○	○	
		Control Registers	○	○	○	
	Others	Display Driving Circuit	○	○	○	○
		Timing Controller	○	○	○	○
		Power Supply	○	○	○	○
Host Interface			DBI	DPI		

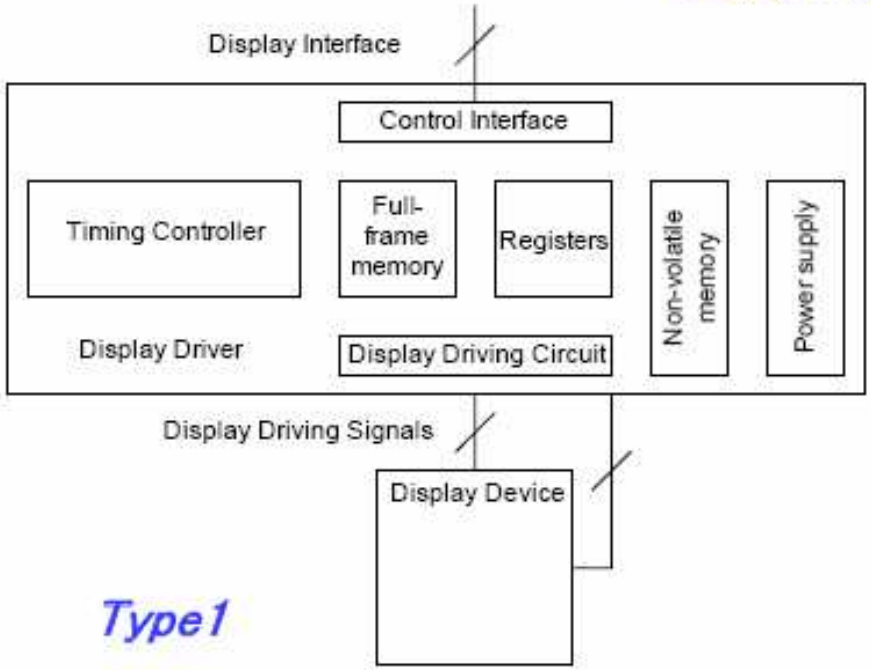
Display Bus Interface Constructions

- *Type A : 68 type Bus Interface*
- *Type B : 80 type Bus Interface*
- *Type C : Serial Communication Interface*

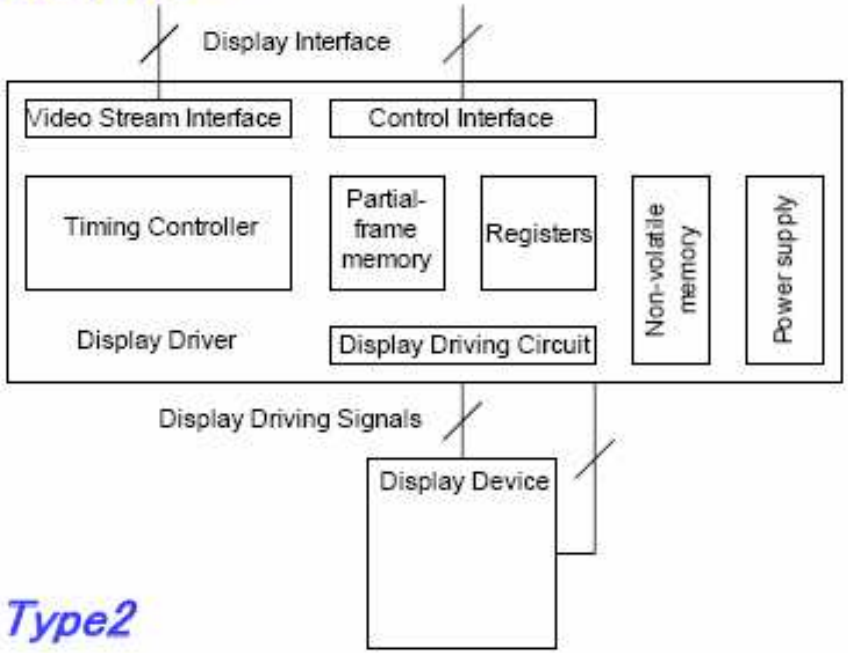
Display Pixel Interface Constructions

- *RGB data with timing signals, Vsync, Hsync, PixelClock*

~Display Architectures~



Type1



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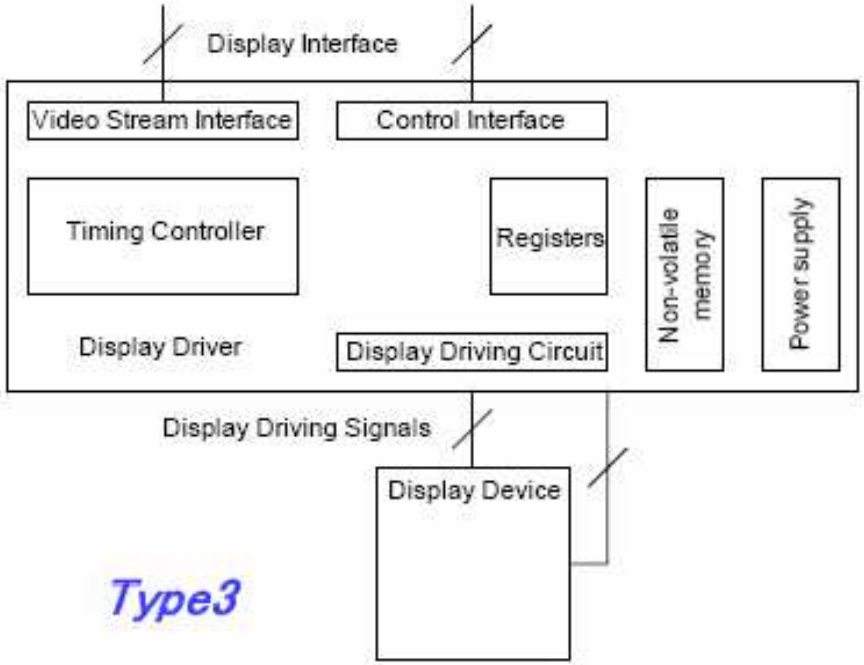
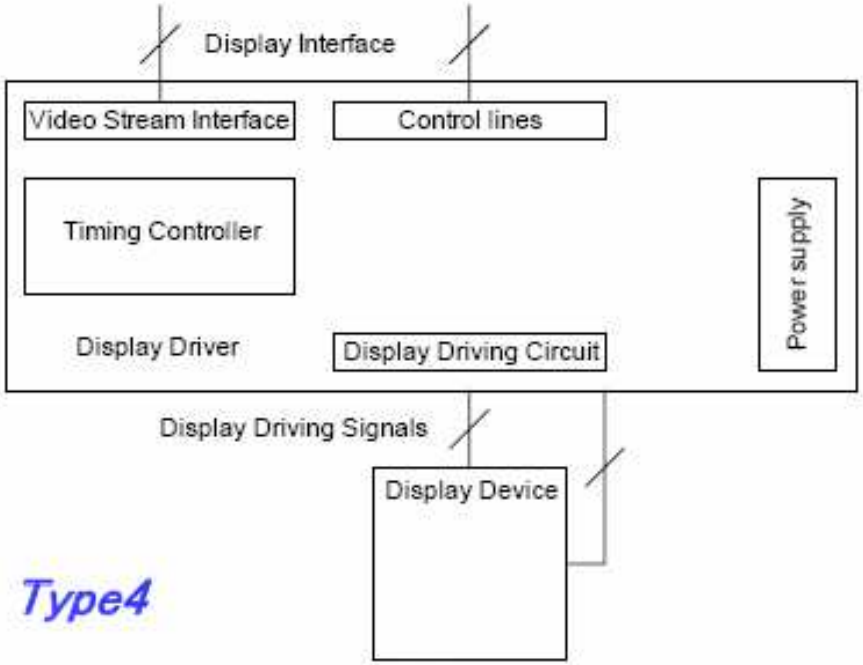


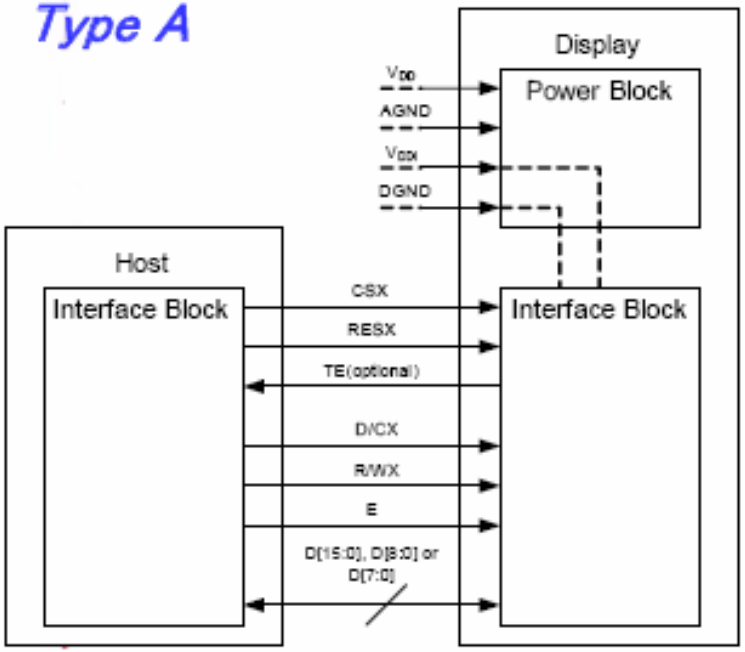
Type3



Type4

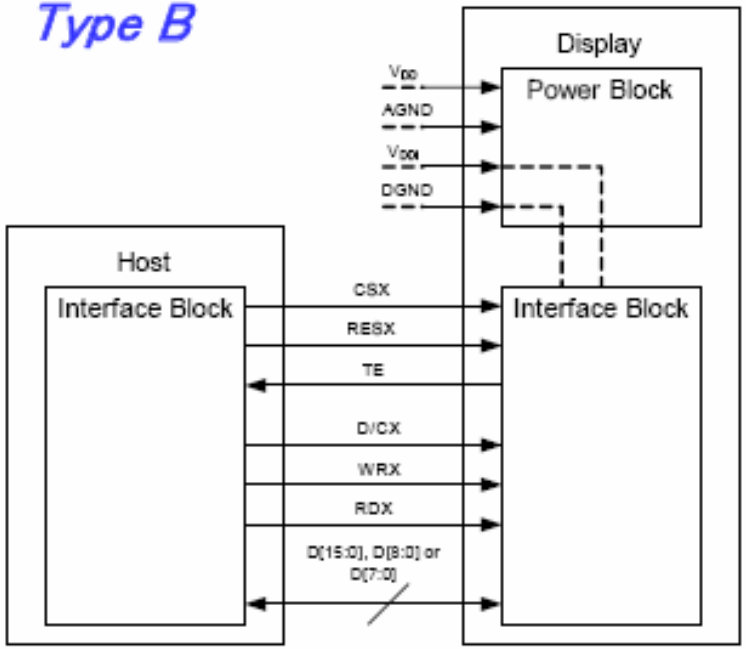
~Display Bus Interface Constructions~

Type A



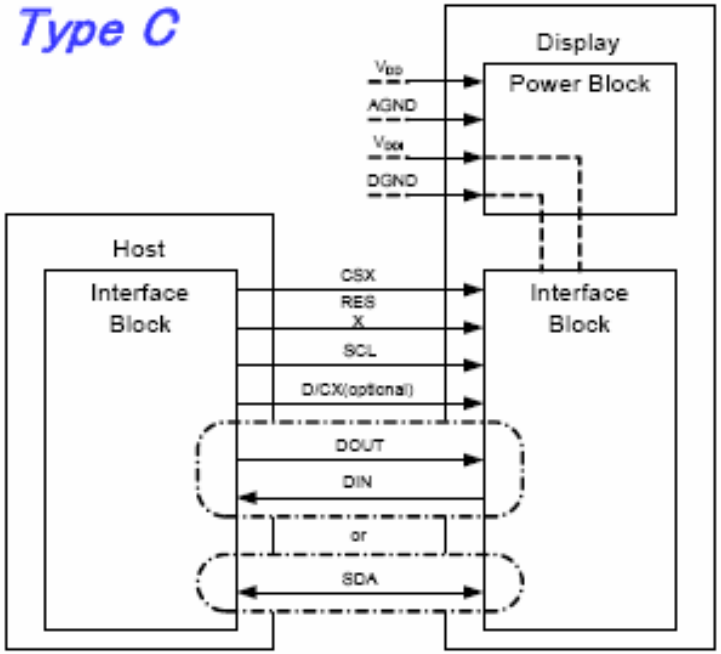
Symbol	Name	I/O
CSX	Chip Select	O
R/WX	Read/Write	O
E	E clock	O
D[15:0], D[8:0], or D[7:0]	Information	I/O
D/CX	Data/Command	O
RESX	Reset	O
TE	Tearing Effect	I

Type B



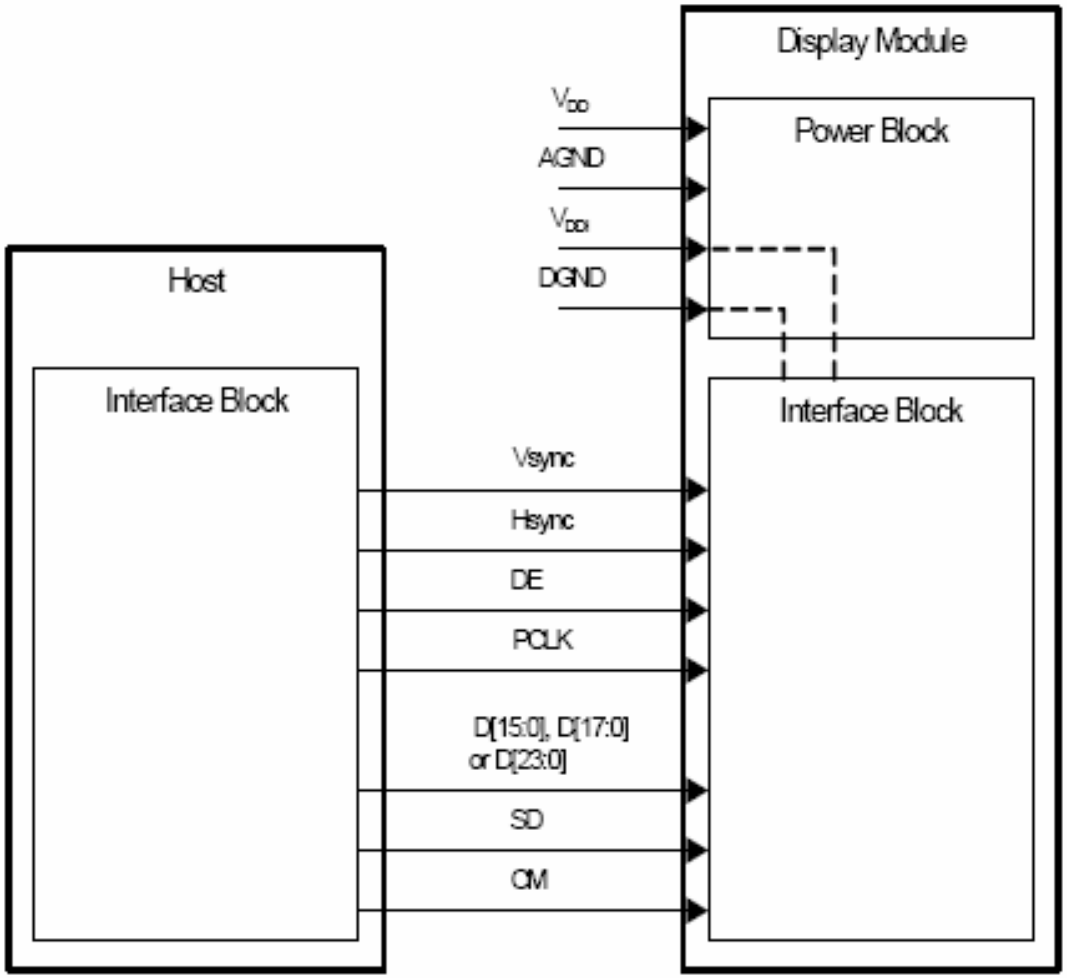
Symbol	Name	I/O
CSX	Chip Select	O
RDX	Read	O
WRX	Write	O
D[15:0], D[8:0] or D[7:0]	Information	I/O
D/CX	Data/Command	O
RESX	Reset	O
TE	Tearing Effect	I

Type C



Symbol	Name	I/O
CSX	Chip Select	O
SCL	Serial Clock	O
DOUT	Information Out	O
DIN	Information In	I
SDA	Information	I/O
D/CX	Data/Command	O
RESX	Reset	O

~Display Pixel Interface Constructions~



Symbol	Name	I/O
Vsync	Vertical sync	O
Hsync	Horizontal sync	O
DE	Data enable	O
PCLK	Pixel Clock	O
D[15:0], D[17:0] or D[23:0]	Pixel Data	O
SD	Shutdown	O
CM	Color Mode	O

Example

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- MIPI-DCS
- MIPI-DBI
- MIPI-DPI

DSI-Display Serial Interface

Motivation for Serial Solutions

Transforming traditional parallel interfaces to serial

- **Benefit:** low pin count, reduced power requirement, standardized I/F
- **Must support** both Command Mode and Video Mode architectures
- **Maintain all functionality** of legacy parallel interfaces

Physical Basis for High-Performance Low-Power Interfaces

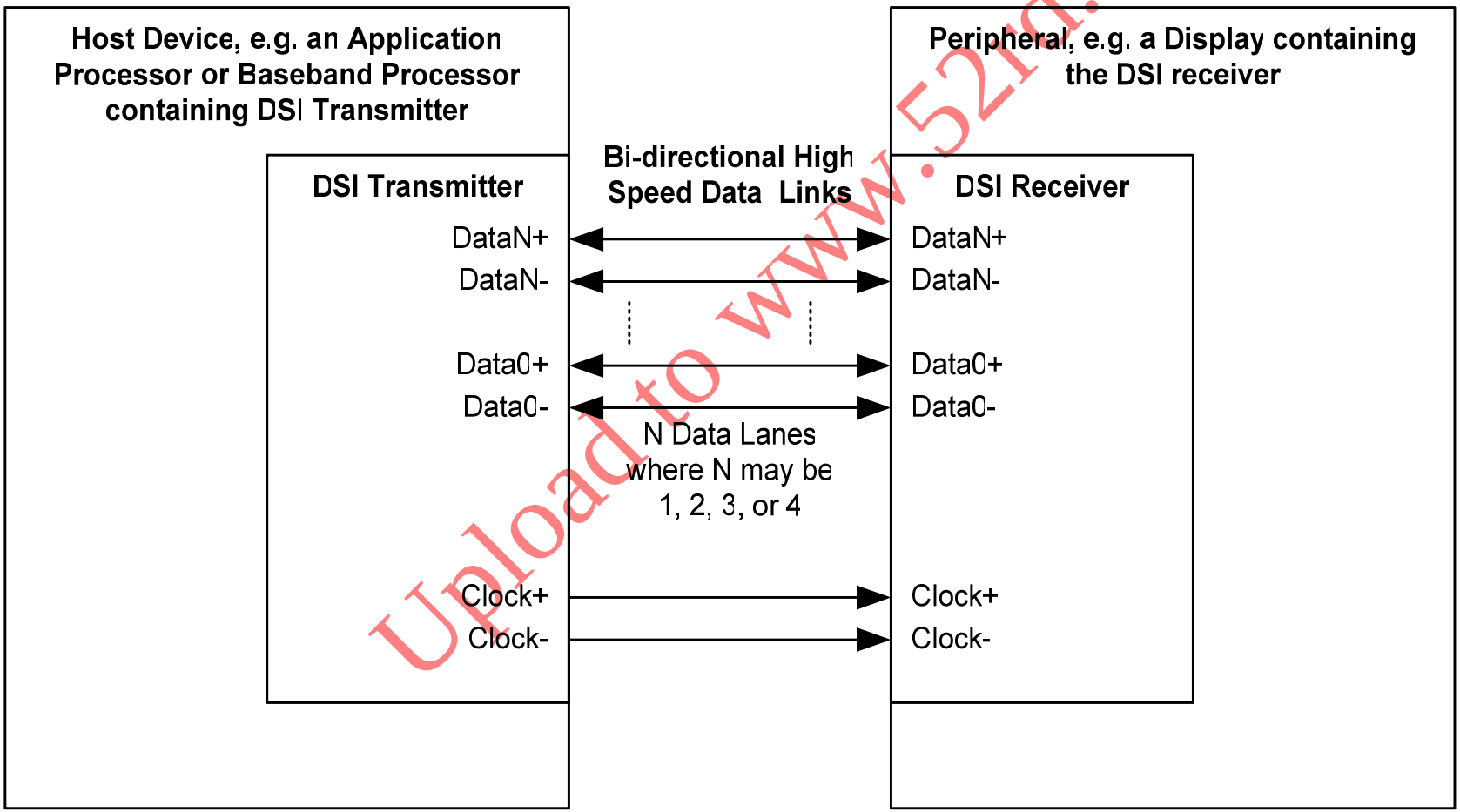
- See D-PHY specification for electrical and timing, low-level functions
- DSI selects and mandates specific configurations of documented D-PHY components:
  - Clock Lane
  - Data Lane(s)
  - Directionality
  - Low-power signaling support and directionality

Requirements for DSI

- **Standard display formats supported:**
  - Sub-displays QQVGA (180 x 120) and smaller on low end
  - Up to WVGA (800x480) and SVGA (800x600) on high end
  - 16, 18, and 24 bits per pixel
  - Bandwidth requirement range 20 to 850 Mbits / sec
- **Lane-Scalable, up to data 4 lanes**
- **Low operational power and very low standby power**
- **Bidirectional data capability, to support Command Mode**
  - Reverse-direction bandwidth requirement < 1 Mbit / sec
- **Up to 12cm conductor length, with connectors & flex cable**
- **Excellent EMI rejection and low emissions, low error rate**
- **Minimize pincount and cost – no exotic circuit design**
- **Protocol supports multiple displays**

Basic DSI System - Physical

- 1 Clock Lane, unidirectional
- 1 to 4 Data Lanes, *may be* unidirectional for Video Mode displays
- Mandates support for LP(Low Power) Signaling



Example

Standard IC? - Developing

- **MIPI-DCS**
- **MIPI-DBI**
- **MIPI-DPI**
- **MIPI-DSI**

Renesas Technology Corp.