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Preliminary Report II: Last Stage Amplifier

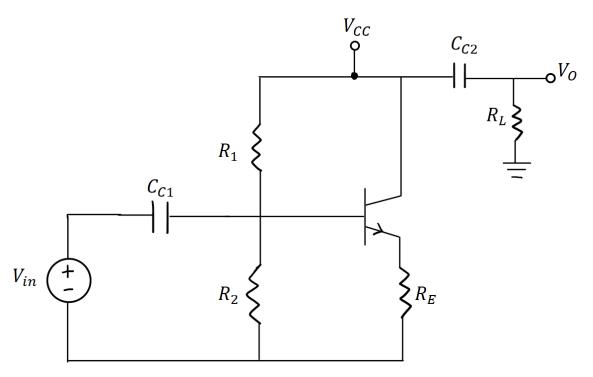


Figure 1: DC Circuit for Emitter Follower Stage

Our theoretically calculated DC circuit parameters are as follows:

$$V_{CC} = 9 V$$

$$V_{CEQ} = \frac{V_{CC}}{2} = 4.5 V$$
 $R_L = 10 \Omega, V_{L,max} > 200 \, mV, I_{L,max} \approx 20 \, mA$

$$I_{CQ} \approx 2I_{L,max} \approx 40 \, mA$$

$$I_{BQ} = 0.4 \, mA, I_{EQ} = 40.4 \, mA$$

$$R_E = \frac{(V_{CC} - V_{CE})}{I_{EQ}} \approx 100 \, \Omega$$

$$R_{TH} \approx 0.1(1 + \beta)R_E \approx 1010 \, \Omega$$

$$V_{TH} = R_{TH}I_{BQ} + V_{BE}(on) + R_EI_{EQ} = 5.144 \, V$$

$$R_1 = R_2 = 2.2 \, k\Omega$$

Our goal is to design an emitter follower amplifier to have sufficient current flowing through the load resistor (> 10 mA).

To find the small signal current gain, the process is as follows: