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DATE: 12/07/2024

SUBJECT: CMPE 314 Lab Project-Audio Amplifier

Objective and Outline

Our objective in this project is to design and implement an audio amplifier that can be used in an AM radio receiver. To achieve this, we will utilize RF input signal and an audio signal (both 100kHz) to drive a multi-stage amplifier that can amplify weak input signal (RF input) without distortion to drive an earphone, which will be represented as a load resistor. This document will discuss the design process and provide the results to the overall outcome of the designed audio amplifier.

Pre-Amp Stage Design

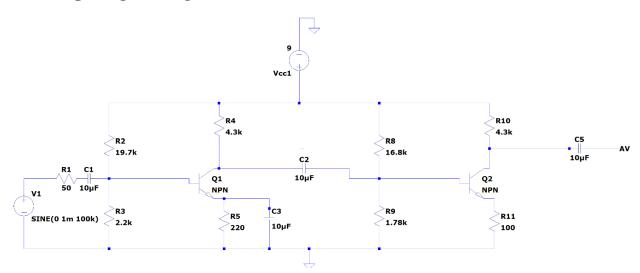


Figure 1: LTSpice Pre-Amp Stage Simulation

In our pre-amp stage, we used the constraints provided to theoretically solve the resistor values needed to create the system. We utilized a MATLAB script that allowed us to get closer to accurate values. From the values, we looked at what we had available and went from there. Our goal was to get a gain of around 500 in the pre-amp stage, so at the output of the second amplifier.

```
% Common Emitter Amplifier with Re
% Modifiers
k = 1000;
m = 10^-3;
u = 10^-6;

% Constraints
Vcc = 9;
B = 100;
Rs = 50;
Vce = 4.5;
Icq = 1 * m;
Ibq = 10 * u;
```

```
% Gain
A v = 120;
% RE and RC calculations
Re = (Vcc - Vce) / ((A_v + 1) * Icq);
Rc = A_v * Re;
% Thevenin values
Rth = 0.1 * (B + 1) * Re;
Vth = (Ibq * Rth) + 0.7 + ((B + 1) * Ibq * Re);
% R1 and R2 calculations
R1 = Rth * (Vcc / Vth);
R2 = Rth * (Vcc / (Vcc - Vth));
% Resistances
rpi = (B * 0.026) / Icq;
Rib = rpi + (1 + B) * Re;
Ri = (Rth * Rib) / (Rth + Rib);
% Actual gain
Af = (-B * Rc) / (rpi + (B + 1) * Re) * (Ri / (Ri + Rs));
% DISPLAY
fprintf('\nResistor w/ voltage gain A_v = %.1f:\n', A_v);
fprintf('R1 = %.2f Ohms\n', R1);
fprintf('R2 = %.2f Ohms\n', R2);
fprintf('RC = %.2f Ohms\n', Rc);
fprintf('RE = %.2f Ohms\n', Re);
fprintf('Ri = %.2f Ohms\n', Ri);
fprintf('Actual A_v gain = %.2f\n', Af);
% Practical Resistor Values(Utilize practical resistor values)
Rp1 = 16800;
Rp2 = 1780;
RpC = 4300;
RpE = 100;
Old_gain = Af;
% Practical RC calculation
Rpc = RpC; % Replace Rc with practical resistor value RpC
% Practical Thevenin values
RPth = 0.1 * (B + 1) * RpE;
VPth = (Ibq * RPth) + 0.7 + ((B + 1) * Ibq * RpE);
% Practical resistances
rPpi = (B * 0.026) / Icq;
RPib = rPpi + (1 + B) * RpE;
RpI = (RPth * RPib) / (RPth + RPib);
RL = 1428.44;
% Practical actual gain
APf = (-B * RpC) / (rPpi + (B + 1) * RpE) * (RpI / (RpI + Rs));
```

```
% DISPLAY
fprintf('\n Real Resistor w/ voltage gain A_v = %.1f:\n', Old_gain);
fprintf('Rp1 = %.2f Ohms\n', Rp1);
fprintf('Rp2 = %.2f Ohms\n', Rp2);
fprintf('RpC = %.2f Ohms\n', RpC);
fprintf('RpE = %.2f Ohms\n', RpE);
fprintf('Ri = %.2f Ohms\n', RpI);
fprintf('New A_v gain = %.2f\n', APf);
VPth = (Ibq * RPth) + 0.7 + ((B + 1) * Ibq * RpE);
```

Figure 2: MATLAB Script for Practical Values

This is what our theoretical part looks like for the first amplifier of the pre-amp stage. We updated some things from our preliminary report 1, specifically resistor values that would help us obtain a big gain. As seen in the theoretical, we got a gain of 134, which is a good start for the goal at hand.

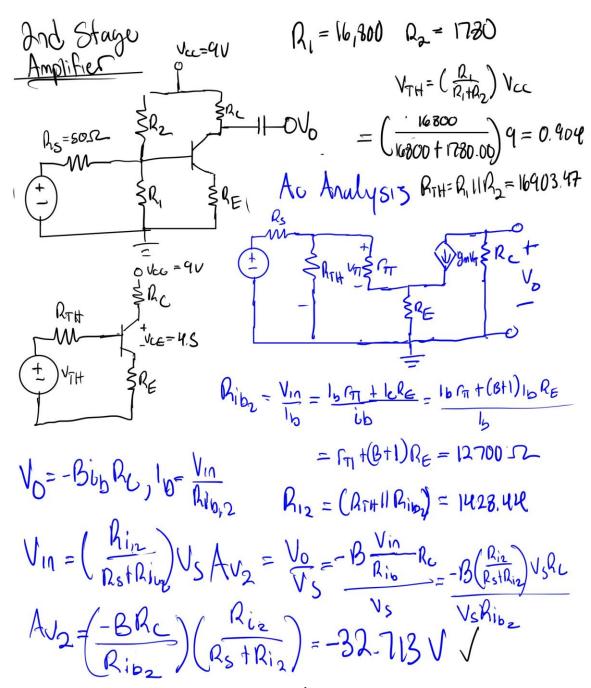


Figure 3: 2nd stage of Pre-Amp

These are the theoretical values of the 2^{nd} stage transistor in our pre-amp stage. Most changes to our pre-amp design went to our first stage because a needed re-work was needed to achieve a workable gain.

Results

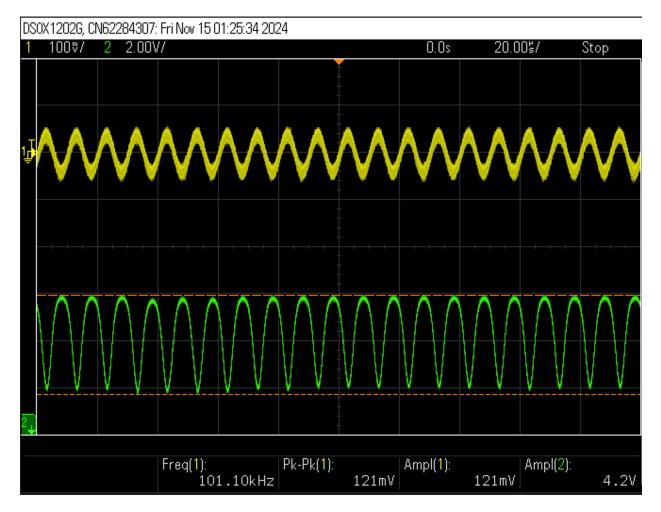


Figure 4: Output Gain

As seen in figure 4, based off the computed voltage gain from calculations of $A_v = -134 \times -32 = 4288$ V we see an exact amplitude of 4.2 V which is what we expected from our pre-amp stage calculations.

Discussion

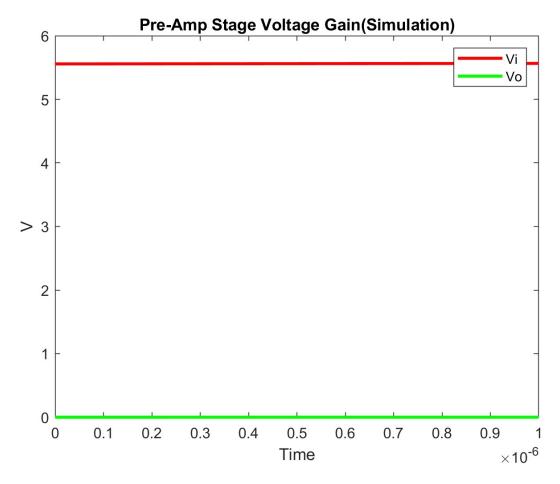


Figure 5: Pre-Amp Voltage Gain

Analyzing and comparing our experimental and simulated output, the experimental resulted in a lower voltage gain than anticipated. This could be due to an assortment of other factors during the experiment such as resistance values, real capacitance, and even equipment such as the oscilloscope.

Final Stage Design

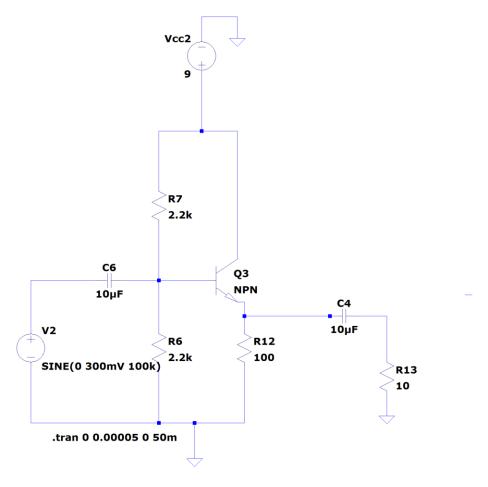


Figure 6: LTSpice Emitter Follower Output Stage Design

Our output stage design required that we use a 10 ohm resistor as the load. The goal in this stage was to be able to provide enough current to the load resistor or just get more than 200 mV as the output voltage. To test this stage, we used the input voltage from the waveform generator instead of the output of the 2nd amplifier from the pre-amp stage. The input voltage was an amplitude of 300 mV and a frequency of 100 kHz.

$$V_{CC} = 9 V$$

$$V_{CEQ} = \frac{V_{CC}}{2} = 4.5 V$$
 $R_L = 10 \Omega, V_{L,max} > 200 \text{ mV}, I_{L,max} \approx 20 \text{ mA}$

$$I_{CQ} \approx 2I_{L,max} \approx 40 \text{ mA}$$

$$I_{BQ} = 0.4 \text{ mA}, I_{EQ} = 40.4 \text{ mA}$$

$$R_E = \frac{(V_{CC} - V_{CE})}{I_{EQ}} \approx 100 \Omega$$

$$R_{TH} \approx 0.1(1 + \beta)R_E \approx 1010 \Omega$$

$$V_{TH} = R_{TH}I_{BQ} + V_{BE}(on) + R_EI_{EQ} = 5.144 V$$

$$R_1 = R_2 = 2.2 \text{ k}\Omega$$

This is the DC analysis part of our emitter follower circuit. Following the project guidelines, we were able to get the required values for the Q values. This part was in our preliminary report, so no update was required.

$$V_{i} \stackrel{ie}{=} V_{in} \stackrel{ie}{=} V_{in} \stackrel{ie}{=} V_{in} + (I+\beta)i_{b}(R_{E}||R_{L}) = 0$$

$$R_{ib} = \frac{V_{in}}{i_{b}} = \frac{V_{in}}{i_{b}} + \frac{(I+\beta)i_{b}(R_{E}||R_{L})}{i_{b}} \stackrel{R_{E}||R_{L}}{} \stackrel{R_{i}}{=} R_{TH}||R_{ib}} \stackrel{R_{ib}}{=} \Gamma_{\pi} + \frac{(I+\beta)(R_{E}||R_{L})}{i_{b}} = 74.09 \Omega$$

$$A_{V} = \frac{V_{0}}{V_{i}} = \frac{(I+\beta)i_{b}(R_{E}||R_{L})}{\frac{V_{0}}{V_{0}}(R_{E}||R_{L})} = 12.39$$

This is the AC analysis for the emitter follower stage. It makes sense that we're not getting a high voltage gain like we've been getting before, as this is the voltage buffer stage. The voltage buffer is responsible for maintaining an almost identical voltage as what was inputted, so it must have a high input impedance but low output impedance. The resistor values make sense, we have a much higher resistance at the input than we do at the output.

Results

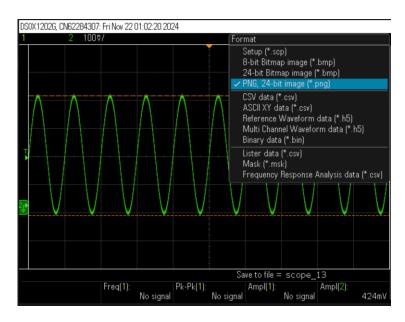


Figure 7: Final Stage Voltage Output

This image shows the result of our final stage implementation. The specification we expected to pass was 200mV open load voltage. Here this image shows an open load of 424 mV which is double what we need to drive the earphone.

Discussion

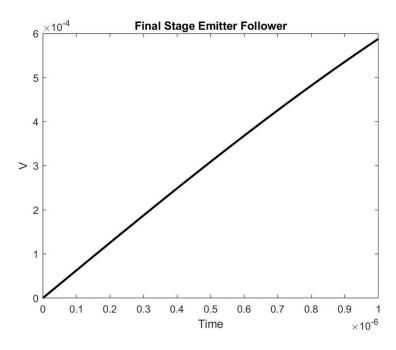


Figure 8: Simulated Final Stage Overall Voltage Output

In this simulation we see that the expected voltage output was around 600mV. This simulated value is around our experimental value considering all other factors that could affect this output. Both simulated and experimental results prove that that design can handle supplying load to the earphone (load resistor.

Overall System Performance

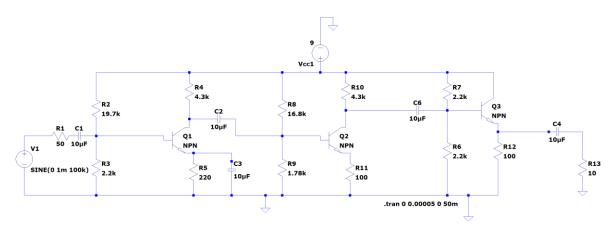


Figure 9: LTSpice Complete Design

Here figure 8 shows a completed implementation of what the final design of the implementation looks like. Everything is put together; we have the two common emitter amplifiers that served as voltage amplifiers up until the final stage, which is the emitter follower and serves as the voltage buffer.

Results

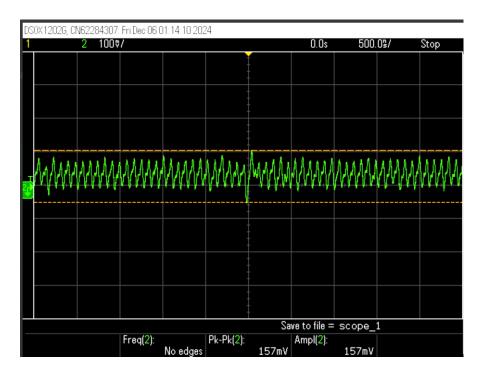


Figure 10: Oscilloscope Full Load Drive

In Figure 10, it is evident that the final stage driving the load exhibits signs of signal distortion. This can be attributed to the use of certain capacitors and the alteration of resistors in earlier stages, which contribute to this effect. The intended load voltage is below 200 mV. Moreover, impedance mismatching was anticipated to some extent but remained within the acceptable output range. Additionally, improper selection of interfacing capacitors could lead to such distortion. With careful adjustments, a better output without signal distortion can be expected.

Discussion

The corner frequencies of each of the required capacitors are as follows.

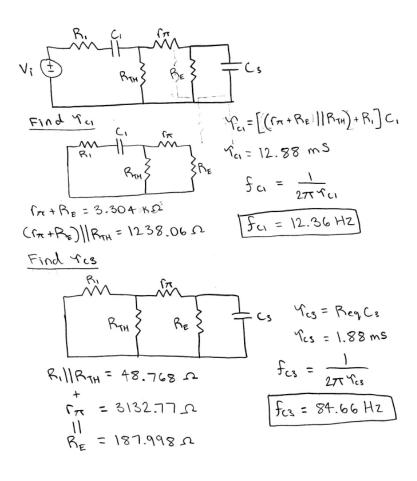


Figure 11: Frequency Response of 1st Stage Transistor (Pre-Amp)

Figure 12: Frequency Response of 2nd Stage Transistor (Pre Amp)

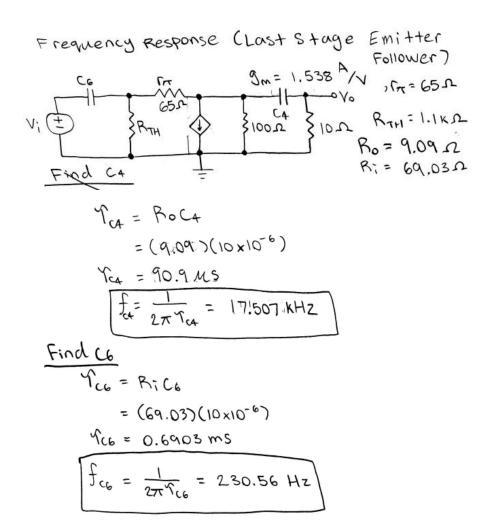


Figure 13: Frequency Response Final Stage

Final Stage voltage output

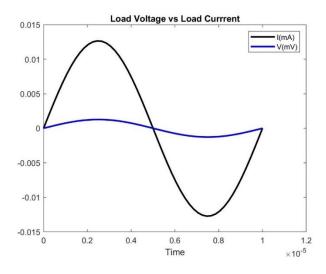


Figure 14: Simulated Frequency Response with Driven Load

In Figure 14, it is observed that the simulation generated a voltage and current significantly below expectations. Despite this discrepancy, even an ideal implementation would fail to provide the required current of at least 40mA to the load.

Conclusion and Final Takeaways

In conclusion, this project had some successful moments, but the overall output of the system is not what we wanted. Some of the successful moments came in our first common emitter amplifier (1st stage) when we got a significantly good gain, the second common emitter amplifier which also gave us a good gain, and testing the emitter follower independent of the previous stages gave us good results (output voltage > 200 mV). The end goal was to get the output voltage to be greater than 200 mV with the full system integration, but we did not manage to get that, we got around 157 mV as our amplitude. We learned a lot about how different types of amplifiers work, like the common emitter being a voltage amplifier while the emitter follower is a voltage buffer. Not only do we now know the theoretical aspect of these characteristics, but we also know through testing what these amplifiers do.