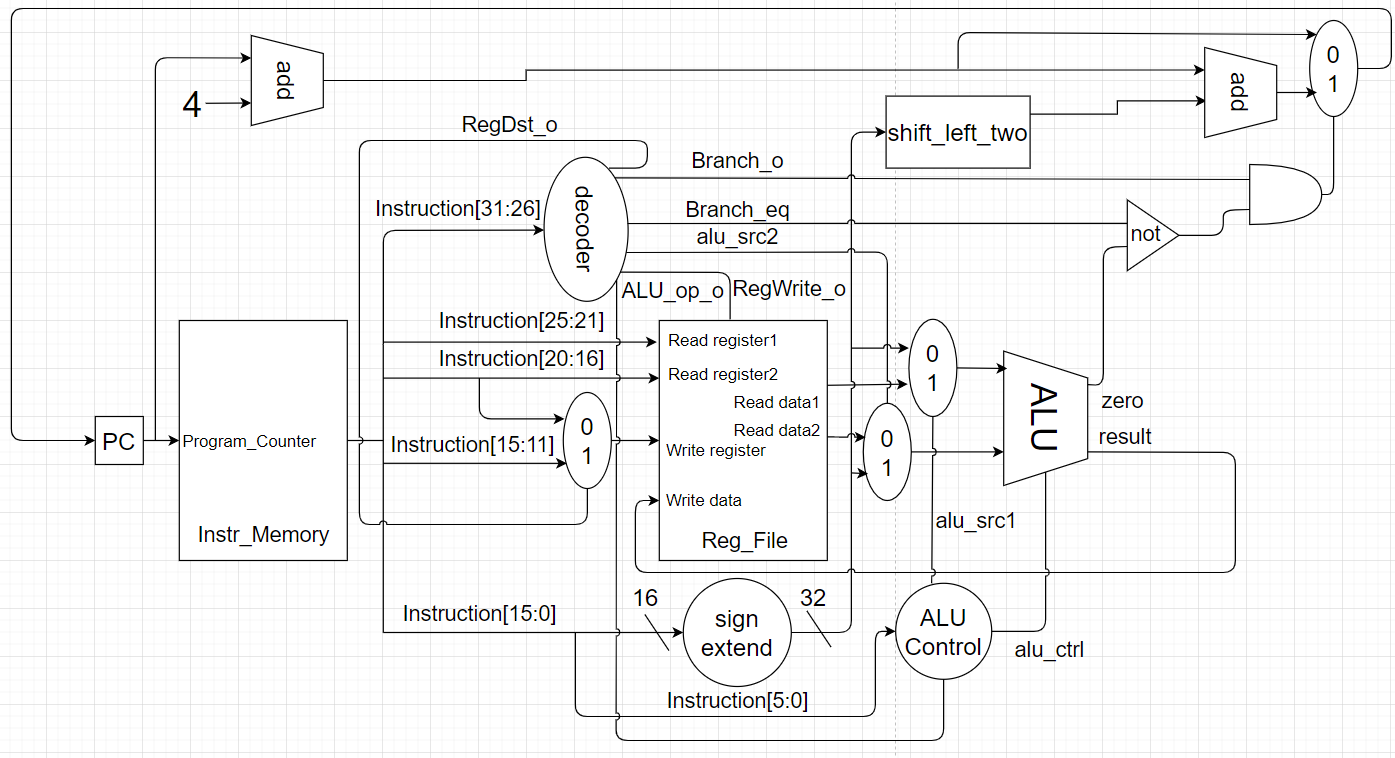
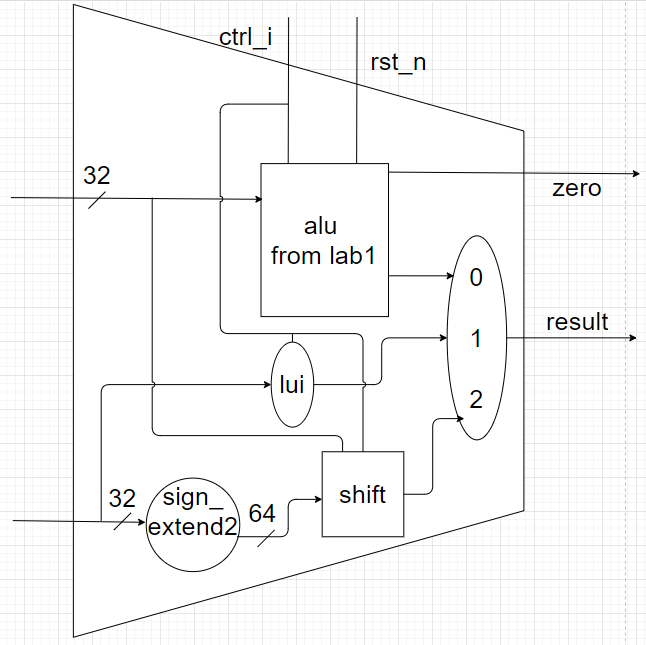
DIAGRAM



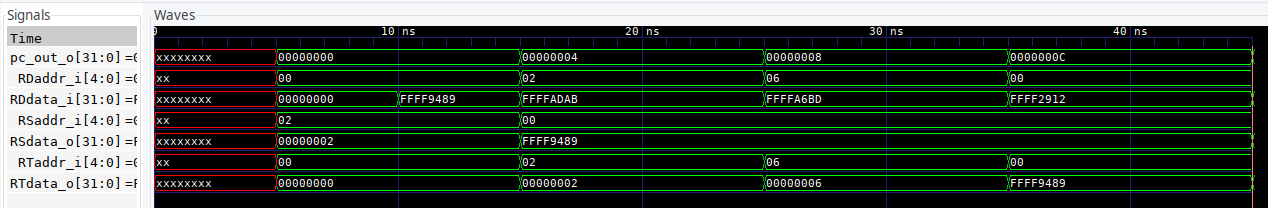
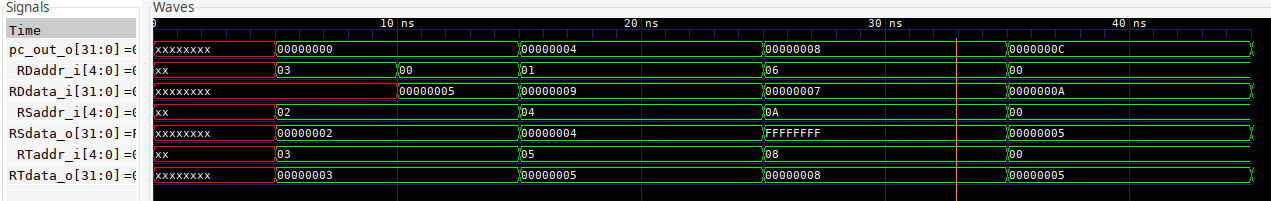
ALU

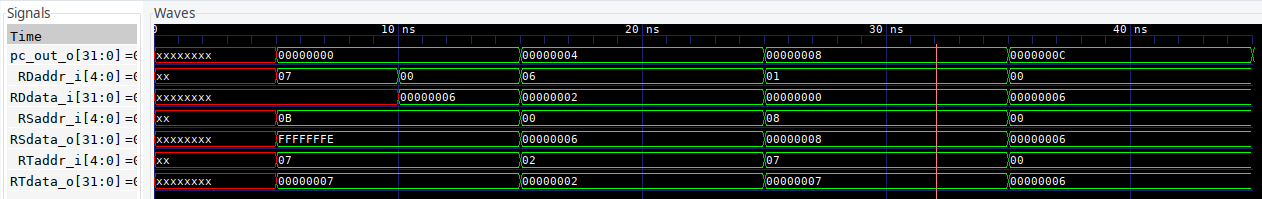


Description

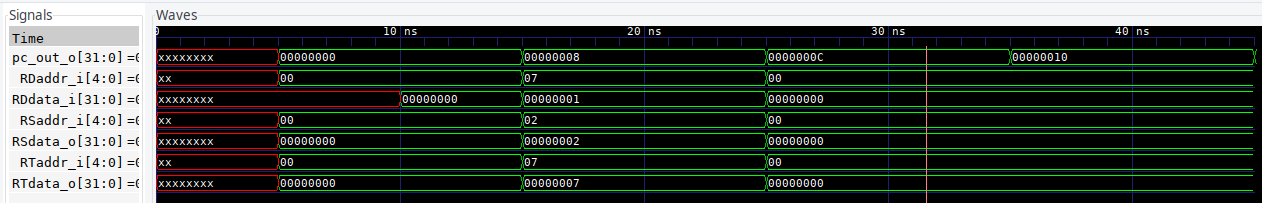
* Adder : add the two input up, calculate the address
* MUX\_2to1 : decide which of the should be output
* Alu\_Ctrl : decide the output control signal by the input instruction[5:0]
* Decoder : decide output the control signal of most of the module in the diagram
* Instr\_Memory : output the instruction of the current input PC address
* ProgramCounter : input the current PC address
* Reg\_File : output the data of the input address, or write the input register into the data memory
* Shift\_Left\_Two\_32 : turn the input address from byte into word
* Sign\_Extend : extend the 16-bit constant to 32-bit to satisfy the input of the after module, we also include the unsigned extend in this module by adding
* Sign\_Extend2 : extend the 32-bit constant to 64-bit to deal with the shift operation
* ALU\_Wrapper : the wrapper of the big ALU in the first diagram
* alu : the alu from lab1
* alu\_top : the first 31 block of alu
* alu\_bottom : the last block of alu
* simple\_add : the add function in alu

Waveform

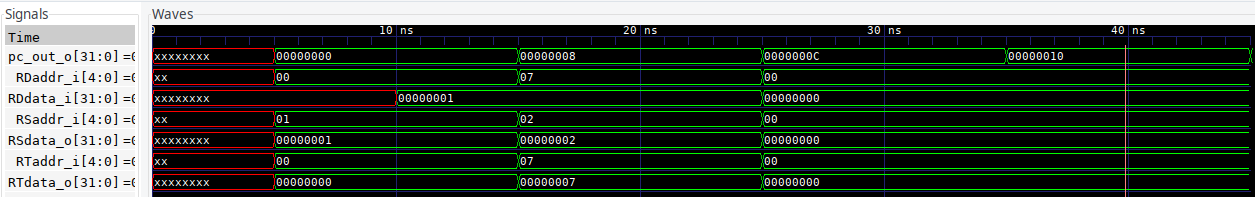
* **addi:**
* **addu:**
* **and:**

****

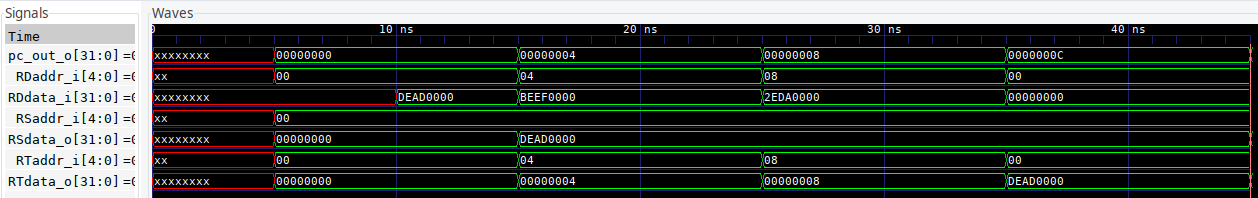
* **beq:**

****

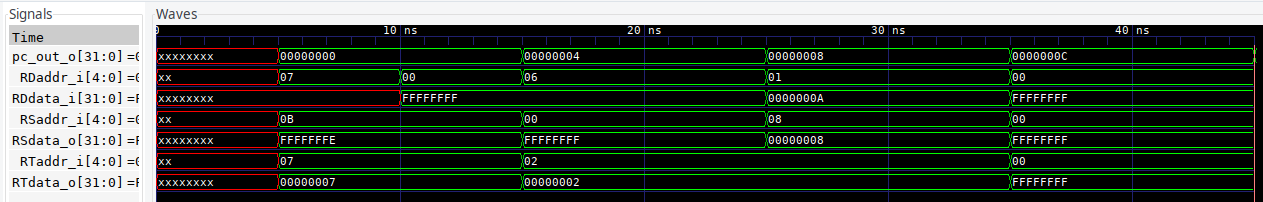
* **bne:**

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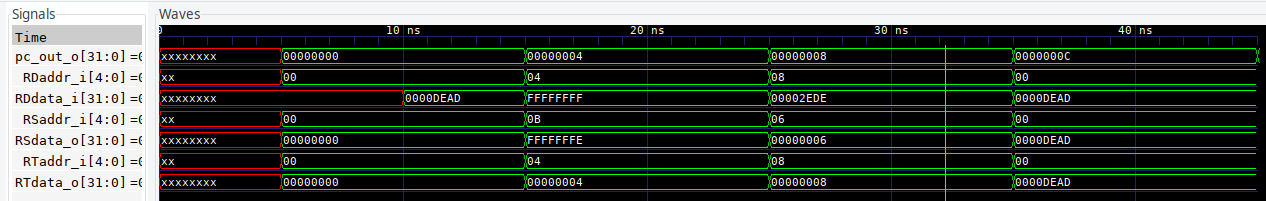
* **lui:**

****

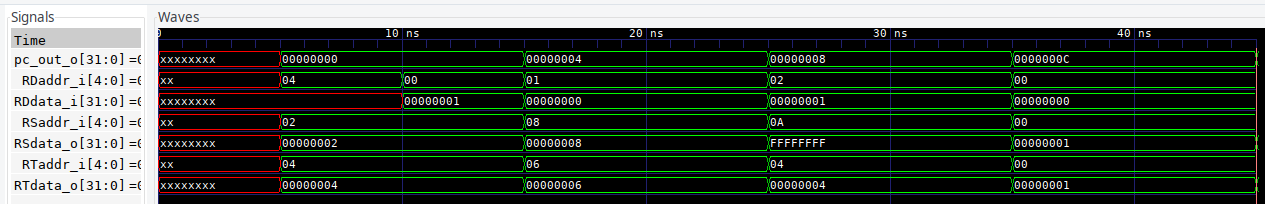
* **or:**

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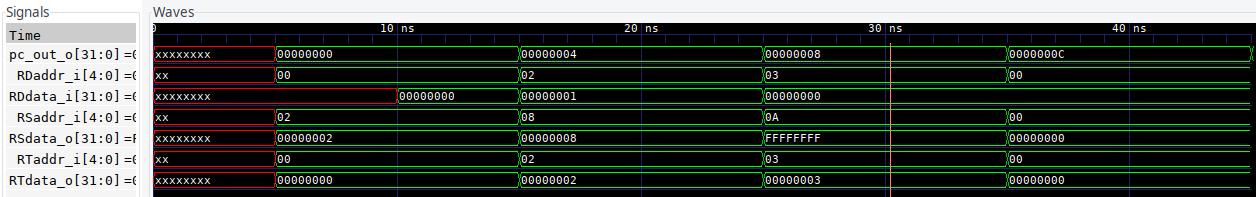
* **ori:**

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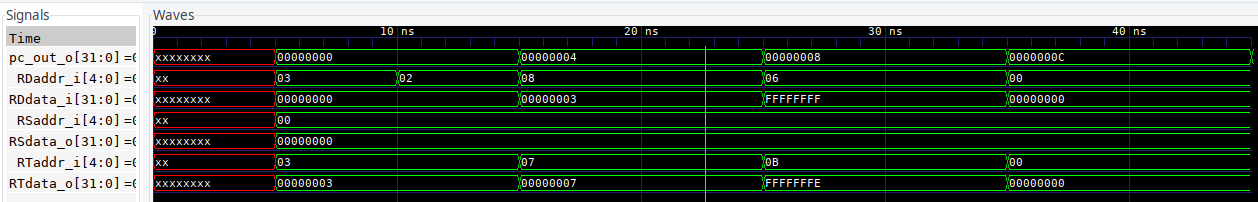
* **slt:**

****

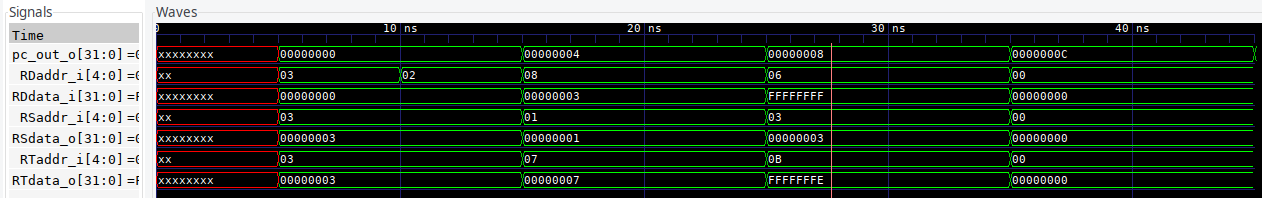
* **sltiu:**

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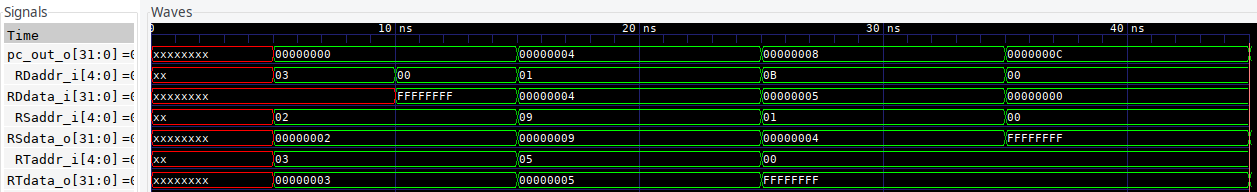
* **sra:**

****

* **srav:**

****

* **subu:**

****

Question

* the most significant bit of the two is on the different side, one count from left to right, one count from right left
* to operate the code within whenever the condition behind the “always” changes
* port connection by order can reduce the time typing the name of the module, but as one port is missed in the module, every port in the module will lose their track

port connection by name can change the order of the port whatsoever as long as every port in connect in the module, however, we need to type all of the name of the port of the module