Received: 15 August 2022 | Revised: 19 October 2022 | Accepted: 16 December 2022

IET Power Electronics

DOI: 10.1049/pel2.12443

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

A high step-up DC-DC converter based on three-winding coupled inductor and voltage multiplier for renewable energy applications

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Funding information
National Natural Science Foundation of China, Grant/Award Numbers: 61803136, 62272109; Undergraduate Teaching Quality and Teaching Reform Project of Guangdong Ocean University, Grant/Award Number: 010301112107

Abstract

A high step-up DC-DC converter for renewable energy applications is proposed. Based on a three-winding coupled inductor and two voltage multiplier cells, the proposed converter obtains a high voltage conversion ratio. Through the passive clamp circuit, the voltage stress of the main switch is suppressed and the leakage energy of the coupled inductor is recycled. This leads to utilize a low on-state power resistance and low voltage-rating power switch that decreases the conduction losses. Meanwhile, the current stress of the diodes is minimized and the reverse recovery problem is alleviated. Thus, high efficiency can be achieved. Under continuous conduction mode (CCM) and discontinuous conduction mode (DCM), different operating principles and the mathematical derivations of the proposed converter are described in detail. To validate the feasibility of the proposed converter, a 320 W prototype with 25–38 V input voltage and 400 V output voltage is implemented. The measured maximum and full load efficiencies are 95.83 % and 94.96 %, respectively.

1 | INTRODUCTION

Nowadays, the demands of high step-up converters are significantly increased due to the diversified utilization of sustainable energy source (SERs) [1]. Photovoltaic (PV), fuel cell (FC) and small wind turbine systems are important renewable energy resources [2–4]. However, one of the challenges to utilize these energies is their low output voltage. Converters with high transfer ratio are required for converting the energy between the dc bus and the energy source. Figure 1 depicts a general schematic of DC distribute generation system.

Among a variety of renewable energy sources, PV systems have the merit of being an unlimited and freely accessible resource [5]. Electric vehicles (EVs) using PV energy can decrease the reliance of petroleum, which reduce the emissions of greenhouse gases [6]. However, the terminal of the renewable power generating unit is usually fluctuant as the electricity of solar PV is highly sensitive to shading. When a small portion of a cell, module, or array is shaded, the output of solar PV electricity significantly decreases [7]. Therefore, high step-up converters with a wide input voltage range are necessary to generate the required dc bus voltage for the grid connection.

Isolated dc–dc converters is one of the solutions to improve voltage gain where high voltage gain can be achieved by raising the transformer turns ratio [8–10]. However, a huge proportion of components are required and the voltage spikes across the power switches increase due to the increase of leakage inductance. Therefore, if the isolation is not essential, non-isolated structure with high voltage gain are more competitive in terms of cost.

For non-isolated converters, traditional boost converter is the standard step-up converter most widely used as it can theoretically achieve unlimited gain with an excessively duty cycle. However, depending on the quality of the components and the output power, the voltage gain becomes maximum at a certain duty cycle. Moreover, the power switch suffers from high voltage stress equals to the output voltage and a high on-state power resistance switch is necessary. Consequently, the boost topology cannot be recommended for high voltage gain applications.

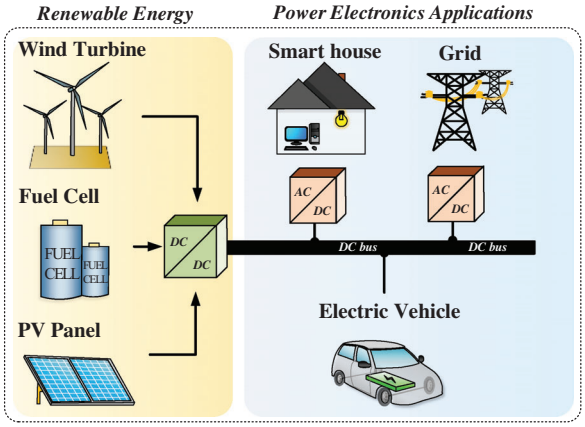

FIGURE 1 Typical building block of DC distributed generation system

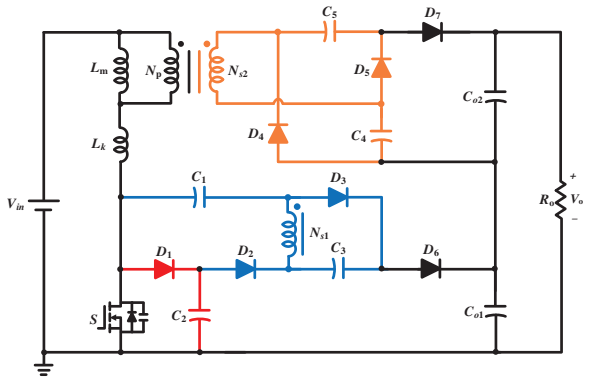

FIGURE 2 The structure of the circuit topology

To operate in a proper duty cycle, different approaches have been proposed [11–33]. Switched capacitor (SC) and switched inductor (SL) have been used. A symmetrical hybrid switch inductor converter (SH-SLC) and an asymmetrical hybrid switch inductor converter (AH-SLC) [11], and the combination of SL and SC cell [12–13] were proposed. Nevertheless, significant instantaneous current is generated, leading to extra power losses and electromagnetic noise. Also, the demand for SC cells and magnetic devices further increases when higher voltage gain is required.

Voltage lift (VL) [14–15] and cascade technique [16–18] are commonly used in step up applications. A cascade boost converter is proposed [16], by connected VL cells in series, the output voltage increases in geometric steps. However, this method requires more control circuit for each cell. By sharing the switches, a quadratic-boost converter and a cascade boost-SEPIC converter are proposed in [17–18], the control complexity is reduced with the single switch structure. However, when implementing three or more boost cells, many components are required. Applying the interleaved structure can also extend the voltage gain [19–21], but the size is bulky.

Compared with a variety of topologies, the topologies with coupled inductor (CL) are proved to have high boost capacity with fewer components. Converters using CL technique are proposed in [22–26]. Due to the two degrees of freedom, the conversion ratio can be attained by assigning turns ratio in addition to duty cycle. Thus, for some specific occasions, a smaller value of duty cycle can be considered. Multiple winding coupled inductors are proposed in [24–26]. Combining cascade and CL techniques, a flyback converter is stacked up on a boost converter in parallel using three-winding coupled inductor (3WCL) [27]. However, utilization of CL creates voltage spike on the power switch owning to the leakage energy. To mitigate this drawback, suppress voltage spikes and recycle leakage energy, different kinds of clamp circuits are adopted [28–30]. Voltage multiplier (VM) can also solve the problem of restricted gain. A combination of conventional boost converter and VM cell [31], and the combinations of 3WCL and VM cells [32–33] are proposed. High voltage gain is achieved while operating in a moderate duty cycle.

Selecting a suitable converter as the foundation for a new design is another essential point to improve performance. Z-source and quasi-Z source converters are proposed in [34, 35]. The main drawbacks of converter in [34] are the discontinuous current and uncommon ground structure. Although the quasi-Z source converter in [35] has a continuity input current, the maximum duty cycle is less than 0.5. The SEPIC and CUK converters provide continuous output current for the load and a common ground structure [36–38]. Nevertheless, their voltage gains are limited.

Recently, a topology based on active switched inductor (ASL), SC and 3WCL has been proposed [39]. High conversion ratio can be achieved with lower voltage stress and current stress on the power switch. However, using two synchronous switches complex the control and the non-common ground characteristics increase the cost of control due to the requirement of more isolated power supplies.

This paper presents a single switch high step-up DC-DC converter with 3WCL and VM techniques. The features of the proposed converter are summarized as follows:

1. The 3WCL technique is used to step up the static gain and the VM cells offer extra voltage gain. Therefore, high transfer ratio can be achieved.
2. With the clamp circuit, the voltage stress of the power switch is suppressed. Low voltage-rating power switch can be used to decrease the conduction loss.
3. The average currents of the diodes are the same as the output current. Therefore, lower the current stress of the diodes, alleviating the reverse recovery problem and improving the efficiency.
4. With the common ground and single switch structure, the control is simple.

Figure 2 shows the topology of the proposed converter. Secondary windings N_{s1} and N_{s2} are integrated with voltage multipliers. Two output capacitors C_{o1} and C_{o2} are in series to supply the load.

In order to properly explore the converter, this paper is organized as follows. Section 2 shows the analysis of operating principles under CCM and DCM. In Section 3, the steady-state analysis is demonstrated. In section 4, a prototype with input

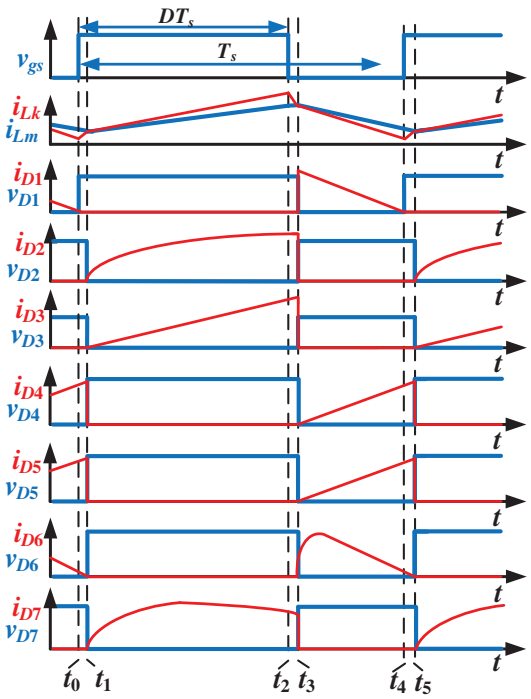

FIGURE 3 Key waveforms of the proposed converter in CCM

voltage of 30 V, output voltage of 400 V and output power of 320 W is constructed. The experimental results verified the feasibility of the proposed converter. Finally, Section 5 concludes this article.

2 | OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

To simplify the analysis of the topology, some conditions are assumed:

1. All power devices excluding output capacitance of the power switch are considered as ideal;
2. All capacitors are sufficiently large so that their voltages can be regarded as constants;
3. The coupled inductor is divided into three parts which includes the ideal transformer with magnetizing inductance L_m and leakage inductance L_k in the primary side.

The turns ratio N_p: N_{s1}: N_{s2} is defined as 1: n_1: n_2.

2.1 | CCM operation

Key waveforms of the proposed converter under CCM are shown in Figure 3. The equivalent circuits for each operating modes (Mode I~IV) are shown in Figure 4.

Mode I [t_0~t_1]: The power switch S is turned on. Diodes D_4, D_5 and D_6 are conducted and diodes D_1, D_2, D_3 and D_7 are reversed biased. Figure 4a shows the path of current flow. The magnetizing inductor L_m and the primary leakage inductor L_k receive energy from dc source V_{in}. Meanwhile, the energy stored in magnetizing inductor L_m is transferred to C_4 and C_5. Thus, current i_{Lm} decreases when current i_{Lk} increases linearly. Moreover, the energy stored in capacitors C_1 and C_3 are discharged to the output capacitor C_{o1}. Output capacitors C_{o1} and C_{o2} are in series to supply the load R_o. When i_{Lk} is equal to i_{Lm} at $t = t_1$, this mode ends.

Mode II [t_1~t_2]: In this transition interval, diodes D_2, D_3 and D_7 are turned on and the rest of other diodes D_1, D_4, D_5 and D_6 are turned off. The power switch S is remained on. Magnetizing inductor L_m and the leakage inductor L_k remain receiving energy from V_{in}. Hence, the currents i_{Lm} and i_{Lk} are upgrading linearly. The direction of current flow is shown in Figure 4b. The energy stored in secondary winding N_{s1} and capacitor C_2 are released to charge capacitor C_1. Meanwhile secondary winding N_{s1} also releases energy to C_3 through D_3. Capacitors C_4, C_5 and the winding N_{s2} are connected in series to charge capacitor C_{o2} through diode D_7. The energies stored in capacitors C_{o1} and C_{o2} discharge constantly to the load R_o. When the power switch S is turned off at $t = t_2$, this mode ends.

Mode III [t_2~t_3]: In this mode, the power switch S is turned off. Diodes D_2, D_3 and D_7 remain in conduction and diodes D_1, D_4, D_5 and D_6 are turned on. The equivalent circuit is shown in Figure 4(c). The magnetizing inductor L_m and the leakage inductor L_k still charged by the input power V_{in}. The leakage inductor L_k releases energy to the parasitic capacitance of the power switch S and the decreasing rate of i_{Lk} is faster than i_{Lm}. The capacitor C_2 and secondary windingN_{s1} remain releasing energies to capacitor C_1 and the secondary winding N_{s1} discharges to capacitor C_3. This mode ends when i_{Lm} is equal to i_{Lk} at $t = t_3$.

Mode IV [t_3~t_4]: In this mode, the power switch S is turned off. Diodes D_1, D_4, D_5 and D_6 are on and rest of the diodes D_2, D_3 and D_7 are off. Figure 4(d) shows the current flow paths. The inductor L_m starts to discharge, releases energy to secondary winding N_{s1} and N_{s2}, i_{Ns1} and i_{Ns2} change their following direction. Meanwhile, the winding N_{s2} charges the switched capacitors C_4 and C_5. The energy stored in leakage inductor L_k is released through D_1 and recovered by capacitor C_2, which also limits the voltage spike of S. Capacitors C_{o1} and C_{o2} together provide energy to the load R_o. This mode ends when v_{gs} is high at t_4.

2.2 | DCM operation

To simplify the analysis of the discontinuous conduction mode (DCM) operation, all assumptions are consistent with those of the CCM operation. Moreover, the description will not be repeated as Mode I–III in DCM are equal to the Mode II–IV in CCM operation. Figure 4 shows the equivalent current flow path of DCM operation. The theoretical waveforms of DCM operation are shown in Figure 5 and the analysis of Mode IV of DCM is shown below.

Mode IV [t_3~t_4]: During this interval, all the diodes and power switch are turned off. Magnetizing inductor L_m is no longer releasing energy, i_{Lm} drops to zero. Meanwhile, the input

FIGURE 4 The operation modes of the proposed converter in the CCM and DCM operation, (a) Mode I CCM; (b) Mode II CCM & Mode I DCM; (c) Mode III CCM & Mode II DCM; (d) Mode IV CCM & Mode III DCM; (e) Mode IV DCM

current i_{in} and output diode current i_{D7} are equal to zero. The energy stored in output capacitors C_{o1} and C_{o2} provides the energy for the load R_o. This mode ends when switch S is turned on at the beginning of the next cycle.

3 | STEADY-STATE CHARACTERISTIC ANALYSIS OF THE PROPOSED CONVERTER

3.1 | The voltage gain of CCM

To simplify the analysis of CCM operation, ignore the mode with extremely short occupancy time, only Mode II and Mode IV are taken into account. During $0\sim DT_s$, the following equations can be derived as

$$\begin{cases} V_{Lm} = V_{in} \\ V_{Ns1} = V_{C3} = n_1 V_{in} \\ V_{Ns2} = n_2 V_{in} \\ -V_{Ns1} + V_{C1} - V_{C2} = 0 \\ -n_2 V_{in} + V_{Co2} - V_{C4} - V_{C5} = 0 \end{cases}. \tag{1}$$

During $DT_s\sim T_s$, the following equations can be obtained.

$$\begin{cases} V_{Lm} = V_{in} - V_{C2} \\ V_{C1} = V_{D2} + n_1 V_{Lm} \\ V_{C4} = V_{C5} = -V_{Ns2} = -n_2 V_{Lm} \\ V_{Co1} = V_{D2} + V_{C3} + V_{C2} \end{cases}. \tag{2}$$

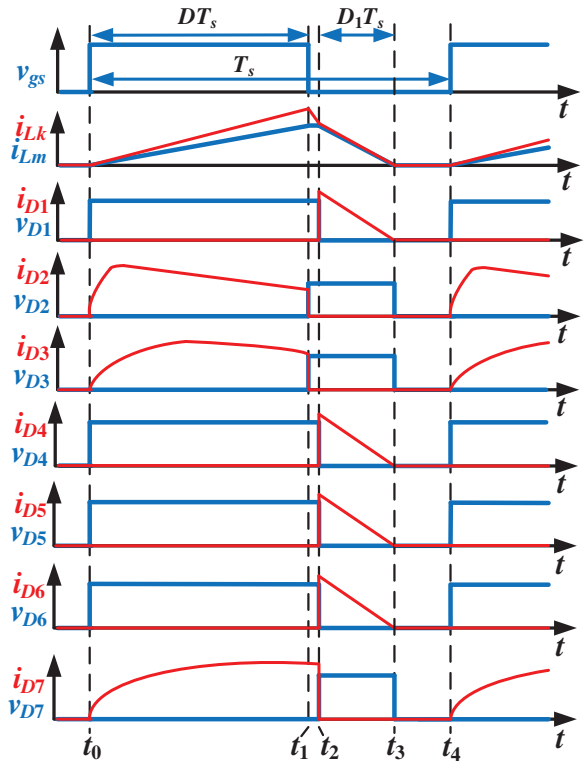

FIGURE 5 Key waveforms of the proposed converter in DCM

Using a volt-second balance on magnetizing inductor L_m, the following equation is obtained.

$$\int_0^{DT_s} V_{in}dt + \int_{DT_s}^{T_s} (V_{in} - V_{C2})\,dt = 0. \tag{3}$$

From (1), (2) and (3), the voltage stresses of C_1, C_2, C_4, and C_5 can be derived as follows.

$$V_{C2} = \frac{1}{1-D}V_{in}, \tag{4}$$

$$V_{C1} = \frac{n_1 + 1 - n_1 D}{1-D}V_{in}, \tag{5}$$

$$V_{C4} = V_{C5} = \frac{n_2 D}{1-D}V_{in}. \tag{6}$$

According to (2), (4) and (5), the voltage stress of D_2 can be calculated as

$$V_{D2} = \frac{n_1 + 1}{1-D}V_{in}. \tag{7}$$

From (1) and (6), the voltage of the output capacitor V_{Co2} can be obtained as

$$V_{Co2} = \frac{n_2 D + n_2}{1-D}V_{in}. \tag{8}$$

Referring to the Mode IV in CCM operation, V_{Co1} can be represented as follows.

$$V_{Co1} = \frac{2 + 2n_1 - n_1 D}{1-D}V_{in}. \tag{9}$$

Conspicuously, C_{o1} and C_{o2} are connected in series to power the load R_o.

$$V_o = V_{Co1} + V_{Co2}. \tag{10}$$

The voltage gain M_{CCM} in CCM operation can be derived from (7), (8) and (9).

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2 + 2n_1 + n_2 + (n_2 - n_1)\,D}{1-D}. \tag{11}$$

Thus, the three-dimensional diagram of the voltage gain of the proposed converter is shown in Figure 6. The voltage gain is related to the duty cycle D and turns ratio N where $N = N_{s1}/N_p = N_{s2}/N_p$. When $N = 1$ and the duty ratio D is 0.525/0.688, it can be capable of up to 10.53/16 times voltage gain.

3.2 | Voltage stress analysis

Referring to Figure 4(b) and (d), the voltage stresses of D_1, D_3, D_4, D_5, D_6, D_7 and S can be derived.

$$V_{D1} = V_{ds} = V_{C2} = \frac{1}{1-D}V_{in}, \tag{12}$$

$$V_{D3} = V_{C3} - n_1 V_{Lm} = \frac{n_1}{1-D}V_{in}, \tag{13}$$

$$V_{D4} = V_{D5} = V_{C5} + V_{Ns2} = \frac{n_2}{1-D}V_{in}, \tag{14}$$

$$V_{D6} = V_{Co1} - V_{C2} - V_{C3} = \frac{n_1 + 1}{1-D}V_{in}, \tag{15}$$

$$V_{D7} = V_{Co2} - V_{C4} = \frac{n_2}{1-D}V_{in}. \tag{16}$$

3.3 | Current stress analysis

From $0 \sim T_s$, by applying the ampere–second principle to all capacitors, the following current relationships can be deduced.

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_o, \tag{17}$$

$$I_{ns1} = I_{ns2} = -I_o, \tag{18}$$

$$I_{ds} = MI_o - I_{D1}. \tag{19}$$

According to KCL, the following expression can be obtained.

$$\int_{DT_s}^{T_s} \left(i_{Lm} - i_{Np}\right) = \int_{DT_s}^{T_s} (i_{D1} + i_{D6})\,dt, \tag{20}$$

where $i_{Np} = n_1 i_{Ns1} + n_2 i_{Ns2}$.

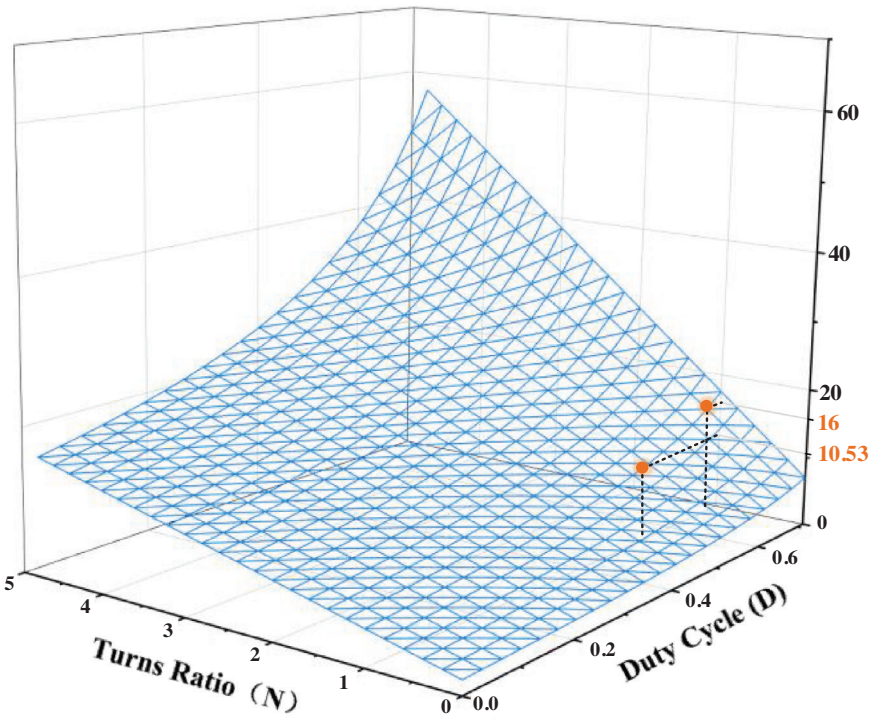

FIGURE 6 Three-dimensional diagram of voltage gain of the presented topology

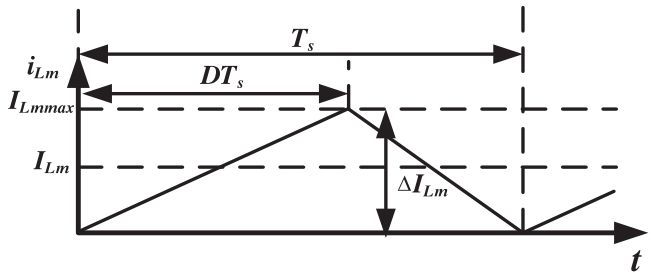

FIGURE 7 Key waveform of the proposed converter in BCM

The average current I_{Lm} is obtained as

$$I_{Lm} = \frac{2 + 2n_2 + n_1}{1 - D} I_o. \tag{21}$$

The current ripple of inductor L_m can be derived from Figure 7.

$$\Delta I_{Lm} = \frac{V_{in} D T_s}{L_m}. \tag{22}$$

The maximum and minimum current of L_m are obtained, respectively.

$$I_{Lmmax} = \frac{2 + 2n_2 + n_1}{1 - D} I_o + \frac{V_{in} D T_s}{2 L_m}, \tag{23}$$

$$I_{Lmmin} = \frac{2 + 2n_2 + n_1}{1 - D} I_o - \frac{V_{in} D T_s}{2 L_m}. \tag{24}$$

When the converter operates under boundary conduction mode (BCM) condition, I_{Lmmin} is equal to zero, L_m can be derived from (24).

$$L_m = \frac{V_{in}(1 - D) D T_s}{2(n_1 + 2n_2 + 2) I_{oB}}, \tag{25}$$

where I_{oB} is the output average current in BCM.

The peak current of diodes can be obtained.

$$I_{D1(pk)} = I_{D4(pk)} = I_{D5(pk)} = I_{D6(pk)} = \frac{2 I_o}{1 - D}, \tag{26}$$

$$I_{D2(pk)} = I_{D3(pk)} = I_{D7(pk)} = \frac{2 I_o}{D}. \tag{27}$$

The maximum current of the power switch is obtained.

$$I_{dsmax} = I_{Lmmax} + I_{D1(pk)}. \tag{28}$$

3.4 | DCM operation

For the simplicity of the steady state analysis of DCM operation, only Mode I and Mode III are discussed. The equations derived from these two modes are the same as Equations (1) and (2).

Using a volt-second balance on magnetizing inductor L_m, the following equations can be obtained.

$$\int_0^{DT_s} V_{in} dt + \int_{DT_s}^{(D+D_1)T_s} (V_{in} - V_{C2})\, dt = 0 \tag{29}$$

From Equations (1), (2) and (29), the voltage stresses of the capacitors can be derived as follows.

$$V_{C2} = \frac{(D_1 + D)}{D_1} V_{in}, \tag{30}$$

$$V_{C4} = V_{C5} = \frac{n_2 D V_{in}}{D_1}, \tag{31}$$

$$V_{C1} = \frac{(1 + n_1) D_1 + D}{D_1} V_{in}, \tag{32}$$

$$V_{Co2} = \frac{n_2 (2D + D_1) V_{in}}{D_1}, \tag{33}$$

$$V_{Co1} = \frac{(2n_1 + 2) D_1 + (2 + n_1) D}{D_1} V_{in}. \tag{34}$$

According to KCL and the charging balance, the following expression can be obtained.

$$\int_{DT_s}^{(D+D_1)T_s} i_{Lk} dt = \int_{DT_s}^{(D+D_1)T_s} \left(i_{Lm} + i_{np}\right) dt. \tag{35}$$

The normalized magnetizing inductor time constant is defined as

$$\tau_{Lm} = \frac{L_m}{R_o T_s}. \tag{36}$$

Combining (33)–(36) and the equation $V_o = V_{Co1} + V_{Co2}$, the voltage gain of the DCM operation M_{DCM} is derived as

$$M_{DCM} = \frac{A + F + \sqrt{\frac{B}{2}(C + D_o + E)}}{B}, \tag{37}$$

where A, B, C, D_o, E and F can be expressed as

$$A = \tau_{Lm} \left[2 (2n_1 + n_2) + 4{n_1}^2 + {n_2}^2\right]$$

$$B = 2\tau_{Lm} (2n_1 + 2n_1 n_2 + n_2)$$

$$C = 2D^2 n_1 n_2 (2 + 2n_2 + n_1)$$

$$D_o = \tau_{Lm} n_2 (2 + n_2)^2$$

$$E = \tau_{Lm} \left[n_1 \begin{pmatrix} 8 + 8{n_1}^2 n_2 + n_1 {n_2}^2 + 8{n_1}^2 + 2{n_2}^2 \\ +28 n_1 n_2 + 16 n_1 + 24 n_2 \end{pmatrix}\right]$$

$$F = \tau_{Lm} [2 n_1 n_2 (4 + 2n_1 + n_2)]$$

3.5 | Loss analysis

The total loss is divided into four parts which includes switch losses, diode losses, coupled inductor losses and capacitor losses.

The power switch losses include conduction loss P_{S_con} and switching loss P_{S_sw}. The conduction loss of the power switch can be obtained by the following expression.

$$P_{S\_con} = \frac{1}{T_s} \int_0^{T_s} r_{ds} {i_{dsrms}}^2 dt, \tag{38}$$

where r_{ds} is the on-resistance of the switch; i_{dsrms} is the RMS value of the power switch S.

The switching loss is caused by the opening delay time t_{on} and closing delay time t_{off} of the switch. In the following equation, I_{on} is the turn-on current and I_{off} is the turn-off current of S. The switching loss P_{ds_on}+P_{ds_off} is calculated as

$$P_{S\_on} + P_{S\_off} = \frac{V_{ds} I_{on} t_{on}}{6T_s} + \frac{V_{ds} I_{off} t_{off}}{6T_s}. \tag{39}$$

The total loss of the power switch S can be obtained.

$$P_{S\_Loss} = P_{S\_on} + P_{S\_off} + P_{S\_con}. \tag{40}$$

Referring to Figure 4b,d, the RMS current of the body diodes can be derived.

$$I_{D1rms} = I_{D4rms} = I_{D5rms} = I_{D6rms} = \frac{I_o}{\sqrt{1 - D}}, \tag{41}$$

$$I_{D2rms} = I_{D3rms} = I_{D7rms} = \frac{I_o}{\sqrt{D}}. \tag{42}$$

Diodes D_2~D_7 have the same on-resistance r_{d0}, so the diodes losses can be described as

$$\begin{aligned} P_{D2\_Loss} &= P_{D3\_Loss} = P_{D4\_Loss} = P_{D5\_Loss} \\ &= P_{D6\_Loss} = P_{D7\_Loss} = V_F I_o + {I_o}^2 r_{d0} \end{aligned}. \tag{43}$$

The on-state resistance of D_1 is r_{d1}, the on-state loss of D_1 can be obtained.

$$P_{D1} = V_F I_o + {I_o}^2 r_{d1}. \tag{44}$$

The total loss of the diodes P_{D_Loss} can be expressed as follows.

$$P_{D\_Loss} = 7 V_F I_o + {I_o}^2 r_{d1} + 6{I_o}^2 r_{d0}. \tag{45}$$

The inductor losses include two parts, the core loss P_{L_core} and the copper loss P_{L_Copper}. The copper loss is related to the copper resistance R_e and the RMS current of the leakage inductor I_{Lk_rms}, which can be derived as

$$I_{Lk\_rms} = \frac{2 + 2n_1 + n_2 + (n_2 - n_1) D}{1 - D} I_o, \tag{46}$$

$$P_{L\_Loss} = \frac{1}{T_s} \sqrt{\int_0^{T_s} {i_{Lk\_rms}}^2 r_e dt} = {I_{Lk\_rms}}^2 R_e. \tag{47}$$

Referring to Figure 4, the RMS current of the capacitors can be obtained.

$$I_{Co1rms} = \sqrt{{I_o}^2 D + \frac{D^2 {I_o}^2}{1 - D}}, \tag{48}$$

TABLE 1 Comparisons between the proposed converter and interrelated structures

Topology	S	D	C	CI+L	NC	Voltage gain (M)	Power switch voltage stress (V_{ds}/V_{in})	The full load efficiency (%)	Common Ground	Isolated
Converter in [8]	1	2	3	2^{2w}+1	9	$\frac{ND}{1-D}$	$\frac{M(M+N)}{MN}$	93.8%	No	Yes
Converter in [9]	2	4	6	1^{2w}+1	14	$\frac{2N}{1-D}$	$\frac{M}{2n}$	96.0%	No	Yes
Converter in [10]	4	2	4	1^{2w}+2	13	$\frac{2N}{1-D}$	$\frac{M}{2n}$	90.0%	No	Yes
Converter in [13]	1	5	5	0+1	12	$\frac{3}{1-D}$	$\frac{M}{3}$	91	Yes	No
Converter in [19]	4	6	9	2^{3w}+2	23	$\frac{2(1+N)}{1-D}$	$\frac{M}{2(1+N)}$	95.6	No	No
Converter in [20]	2	6	6	0+2	16	$\frac{2N}{1-D}$	$\frac{M}{2N}$	95.1	No	No
Converter in [21]	2	8	7	2^{3w}+0	19	$\frac{1+3N}{1-D}$	$\frac{M}{1+3N}$	95.2	No	No
Converter in [23]	1	8	8	1^{2w} +0	18	$\frac{4+N(2-D)-D}{1-D}$	$\frac{M-N-1}{3+N}$	94	Yes	No
Converter in [25]	2	6	5	1^{3w}+2	14	$\frac{2(1+N)}{1-D}$	$\frac{M}{2(1+N)}$	95.5	No	No
Converter in [26]	1	6	6	1^{3w}+0	14	$\frac{2+3N-ND}{1-D}$	$\frac{M^2-MN}{2M+2MN}$	94.3	Yes	No
Converter in [33]	2	5	5	1^{3w}+0	13	$\frac{2+N+D(N+1)}{1-D}$	$\frac{M^2+MN+M}{2MN+3M}$	94.2	No	No
Converter in [38]	1	5	6	1^{2w}+0	14	$\frac{2(1+N)}{1-D}$	$\frac{M}{2(1+N)}$	94.9	Yes	No
Converter in [39]	2	3	3	1^{3w}+0	9	$\frac{3+N+D}{1-D}$	$\frac{1+M}{4+n}$	96.2%	No	No
Proposed Converter	1	6	7	1^{3w}+0	15	$\frac{3N+2}{1-D}$	$\frac{M}{3N+2}$	94.96	Yes	No

S = Switch; L = Inductor; CL = Coupled Inductor; C = Capacitor; D = Diode; NC = Number of the used components.

$$I_{Co2rms} = \sqrt{\frac{(1-D)I_o^2}{D}}, \tag{49}$$

$$I_{C1rms} = I_{C2rms} = I_{C3rms} = I_{C4rms} = I_{C5rms} = \sqrt{\frac{I_o^2}{D} + \frac{I_o^2}{1-D}}. \tag{50}$$

According to former Equations (48), (49) and (50), the power loss of capacitor P_C can be expressed as

$$P_{C\_Loss} = \sum_{n=1}^{5} \left(r_{Cn} {i_{Cnrms}}^2 \right) + r_{Co1} {i_{Co1rms}}^2 + r_{Co2} {i_{Co2rms}}^2. \tag{51}$$

The inductor losses include two parts, the core loss P_{L_core} and the copper loss P_{L_Copper}. The copper loss is generated due to ESR. And it related to the equivalent value of copper resistance R_e and the RMS current of the leakage inductor I_{Lkrms}, which can be derived as

$$I_{Lkrms} = \frac{2 + 2n_1 + n_2 + (n_2 - n_1) D}{1 - D} I_o, \tag{52}$$

$$P_{L\_Copper} = \frac{1}{T_s} \sqrt{\int_0^{T_s} {i_{Lkrms}}^2 r_e dt} = {I_{Lkrms}}^2 R_e. \tag{53}$$

The total core loss of the coupled inductor can be calculated as

$$P_{L\_core} = K f_s \left(\frac{\Delta B}{2} \right)^{\alpha} V_e, \tag{54}$$

where K is the pyro conductivity of iron core, f_s is the frequency of the power switch, ΔB is the variation of the magnetic flux density, V_e is the volume of the core and α is determined by the core material.

P_{L_Loss} is the total loss of the proposed converter, which can be described as

$$P_{L\_Loss} = P_{L\_core} + P_{L\_Copper}. \tag{55}$$

Hence, from the above equations, by setting P_o is the output power, the efficiency of the proposed converter is obtained:

$$\eta = \frac{P_o}{P_o + P_{S\_Loss} + P_{D\_Loss} + P_{C\_Loss} + P_{L\_Loss}} \times 100\%. \tag{56}$$

3.6 | Comparisons

Table 1 shows the comparison between the proposed converter and the related high step-up topologies in the component count,

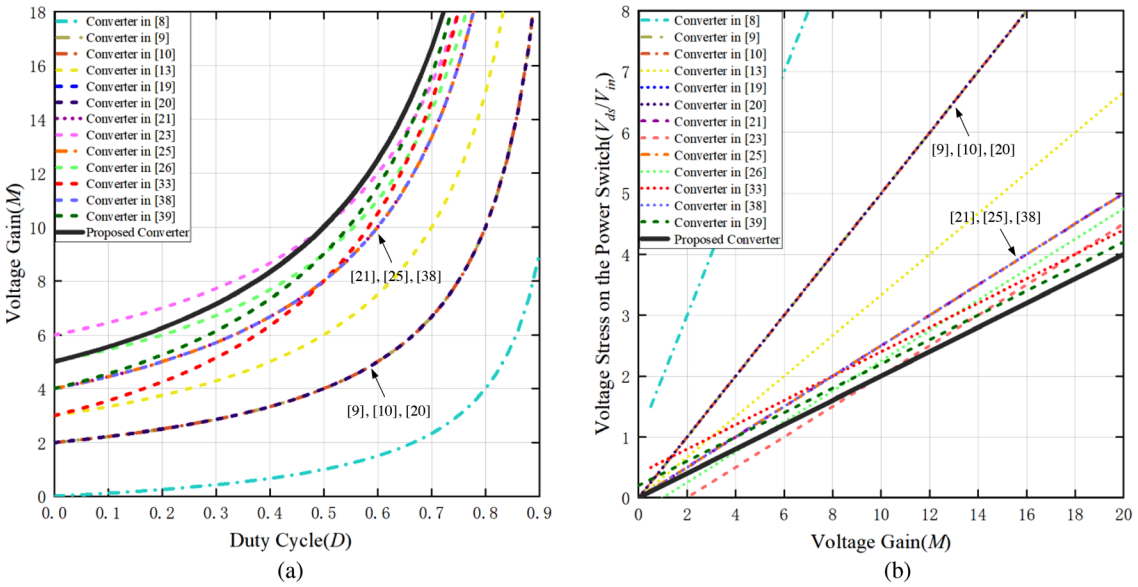

FIGURE 8 Under N = 1 (a) comparisons of the voltage gain versus duty cycle; (b) comparisons of voltage stress of power switch versus the voltage gain

voltage gain, voltage stress of the power switch and the full load efficiency. Figure 8a,b shows the voltage gain and the voltage stress curves of the listed converters, respectively.

Distinguish from other converters, isolated converters [8–10] have desirable features where galvanic isolation can improving safety and noise immunity. However, when turns ratio $N = 1$, the proposed converter has significant advantages of gain and voltage stress on the main switch over the isolated topologies. Thus, the high voltage gain of isolated converters requires a high turns ratio which enlarge the size and the cost of the transformer. Moreover, the uncommon ground structure increases the difficulties of control.

For non-isolated converters, it can be observed from Figure 8 that the proposed converter has advantages over high voltage gain and low voltage stress on the power switch. Moreover, compared to the converters [19-21, 25, 33] and [39], the proposed converter has a single switch and common ground structure, which reduces the difficulty of control.

TABLE 2 Experimental specifications and parameters

Parameter	Value
Input voltage, V_{in}	25-38 V
Output voltage, V_o	400 V
Maximum output power, P_o	320 W
Switching frequency, f_s	50 kHz
MOSFET S	IPP110N20N
Diodes D_1	MBR20100CT
Diodes D_2~D_7	MUR420
Capacitors C_1, C_{o1}	47 μF
Capacitors C_2~C_5, C_{o2}	56 μF
Coupled Inductor	Core EC4950
	Magnetizing inductance L_m = 45 μH
	Leakage Inductances L_k = 700 nH
Turns Ratio (N_p: N_{s1}: N_{s2})	10:10:10

4 | VERIFICATION BY EXPERIMENTAL RESULTS

4.1 | Experimental results

To validate the correctness of the theoretical analysis, a hardware prototype is built. Parameters of the major components are listed in Table 2.

Based on Figure 6 and specification, N is selected as 1. From (11) and (25), with an input voltage of 25 V, output voltage of 400 V and the load current I_{oB} = 0.24 A, the value of the inductor can be obtained under BCM operation:

$$L_m = \frac{V_{in}(1-D)DT_s}{2(n_1+2n_2+2)I_{oB}} \approx 45\mu H$$

The experiment results of CCM operation with the input voltage V_{in} = 25 V and the output power P_o = 320 W are shown in Figure 9. Figure 9a shows the experimental waveforms of the gate signal of the power switch S and the voltage stress and current stress of D_1 and V_{ds} over S. In Figure 9a, the voltage spike of S is supressed by C_2, and the voltage is about 81 V. The energy of the leakage inductance is absorbed in the capacitor C_1 to increase the efficiency of the proposed converter. Figure 9h depicts the stable output voltage of the circuit in the CCM operation, the leakage inductor current and the voltage of the capacitor C_1. Besides, Figure 10b–g mainly show the voltage and current over the diodes D_1~D_7. Furthermore, the voltages

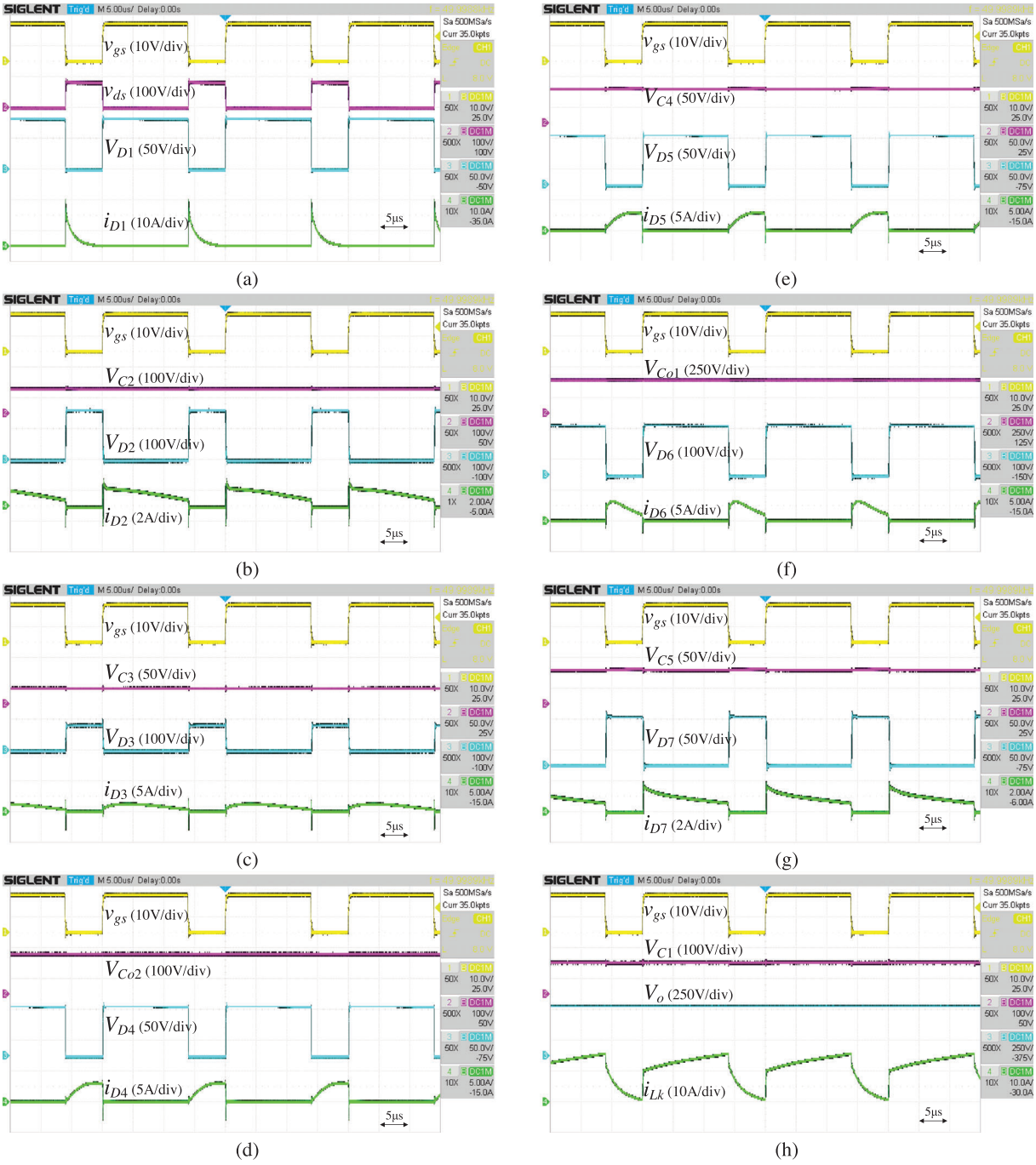

FIGURE 9 Experimental waveforms under V_{in} = 25 V, V_o = 400 V and P_o = 320 W (a) v_{gs}, v_{ds}, V_{D1}, i_{D1}; (b) v_{gs}, V_{C2}, V_{D2}, i_{D2}; (c) v_{gs}, V_{C3}, V_{D3}, i_{D3}; (d) v_{gs}, V_{Co2}, V_{D4}, i_{D4}; (e) v_{gs}, V_{C4}, V_{D5}, i_{D5}; (f) v_{gs}, V_{Co1}, V_{D6}, i_{D6}; (g) v_{gs}, V_{C5}, V_{D7}, i_{D7}; (h) v_{gs}, V_{C1}, V_o, i_{Lk}

across the capacitors are displayed in Figure 9b–h. The experimental measured parameters in Figure 10 are corresponding to the theoretical analysis.

The experiment results of DCM operation with the input voltage V_{in} = 25 V and the output power P_o = 48 W are plotted in Figure 10. As shown in Figure 10, the diode currents i_{D1}, i_{D4}, i_{D5} and i_{D6} become zero before the power switch S is turned on and the magnetizing inductor was resonated with the output capacitor, validating that the circuit is operating in DCM mode. The clamp circuit suppresses the voltage spike on the power switch S better than CCM operation. In general, the experimental waveforms verify the reliability of the theoretical analysis.

4.2 | Measured efficiency

To demonstrate the efficiency of the proposed converter, efficiency curves at input voltages of 25 V/30 V/38 V and output voltage of 400 V over the load range of 10–100% are shown in

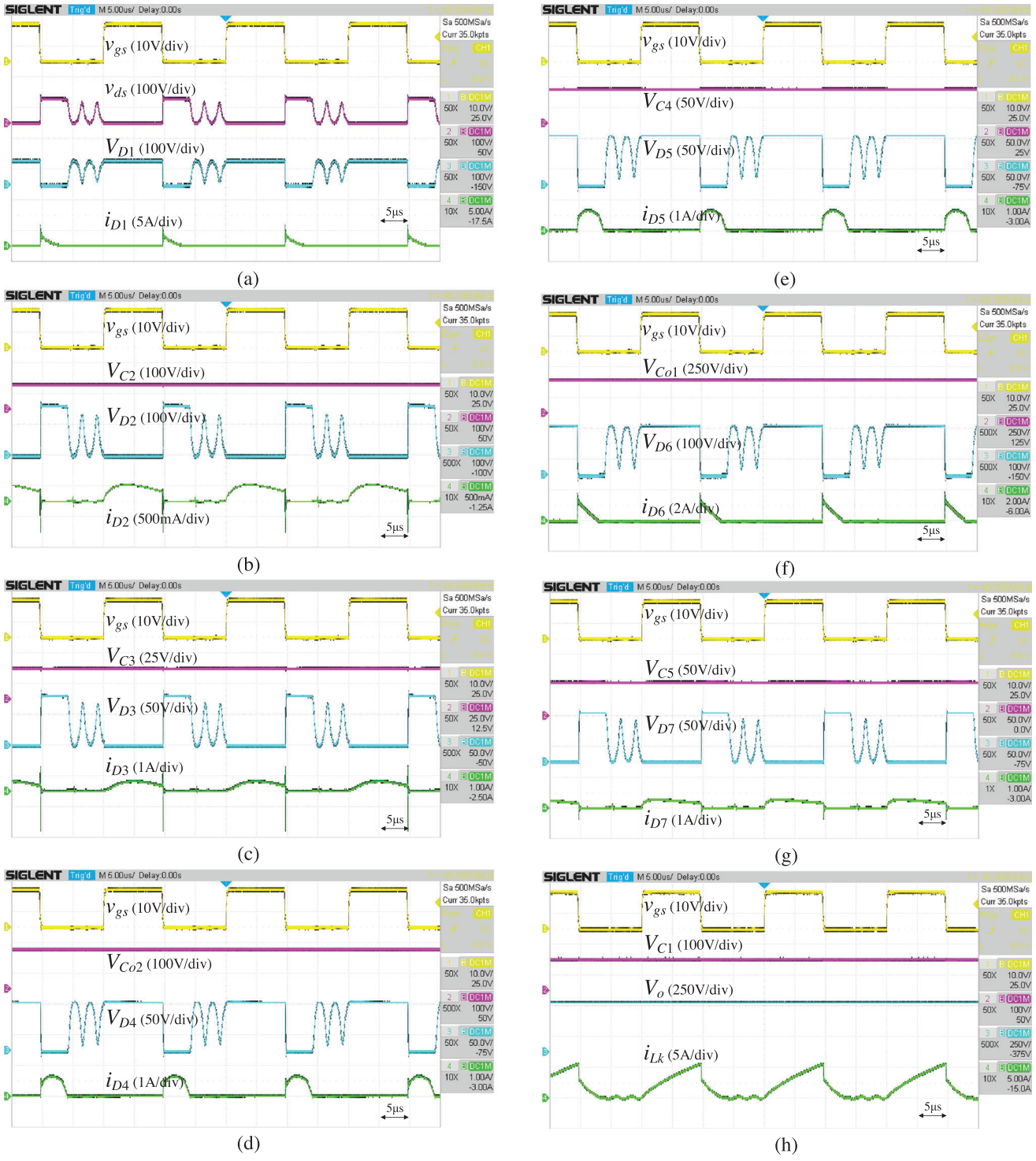

FIGURE 10 Experimental waveforms under V_{in} = 25 V, V_o = 400 V and P_o = 48 W (a) v_{gs}, v_{ds}, V_{D1}, i_{D1}; (b) v_{gs}, V_{C2}, V_{D2}, i_{D2}; (c) v_{gs}, V_{C3}, V_{D3}, i_{D3}; (d) v_{gs}, V_{Co2}, V_{D4}, i_{D4}; (e) v_{gs}, V_{C4}, V_{D5}, i_{D5}; (f) v_{gs}, V_{Co1}, V_{D6}, i_{D6}; (g) v_{gs}, V_{C5}, V_{D7}, i_{D7}; (h) v_{gs}, V_{C1}, V_o, i_{Lk}

Figure 11. It shows the superior performance of the proposed converter where the measured maximum and full load efficiencies are 95.83 % and 94.96 %, respectively. The losses analysis under full load conditions of V_{in} = 25 V and V_o = 400 V is illustrated in Figure 12. The total losses of the theoretical analysis is 15.8 W.

4.3 | Closed-loop experimental result

Figure 13a illustrates the control diagram of the proposed converter. The proportional integration (PI) controller is used to compare the actual output voltage value V_o with the given value V_{o_ref}. When differences exist between V_o and V_{o_ref}, the results

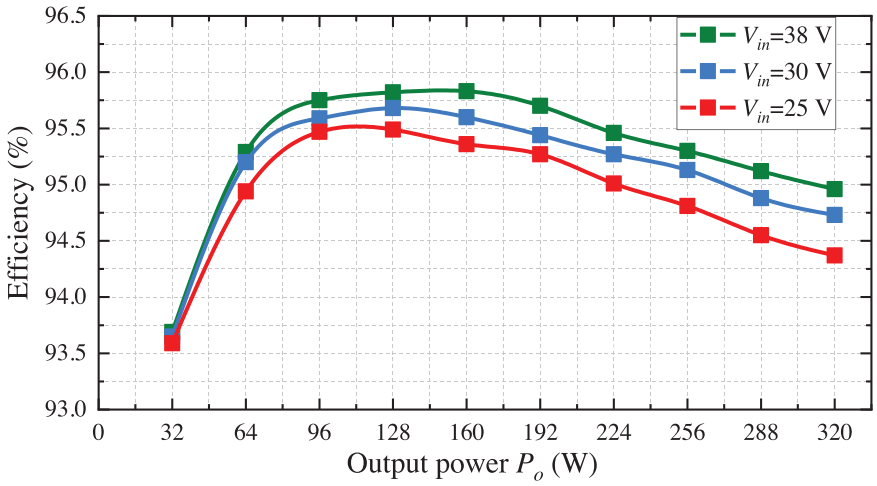

FIGURE 11 Measured efficiencies of the proposed converter

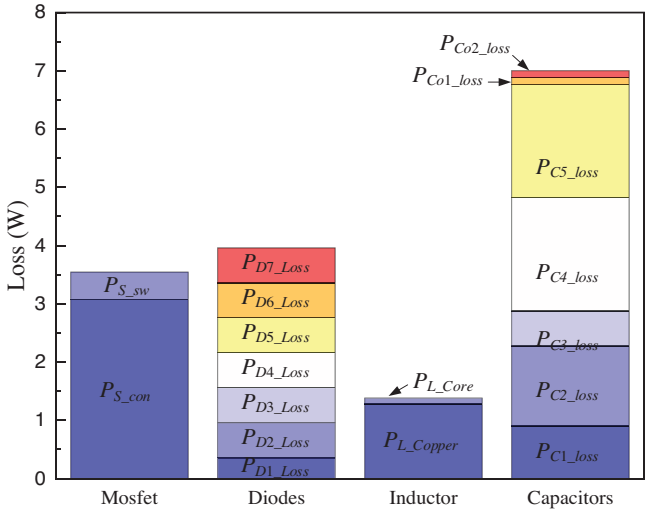

FIGURE 12 Histogram of full load efficiency and its total losses distribution when input voltage is 25 V

of the comparisons are applied to the PI controller to regenerate the appropriate duty cycle. The TMS320F28335 digital signal processor generates the PWM commands applied to the power switch using the SI8220 MOSFET driver.

Figure 13b indicates the dynamic response of the proposed converter for 50% step change in the output load with 30 V input voltage and 400 V output voltage. To test the dynamic characteristics of the output voltage when the input voltage varies, the transient response of the proposed converter with an input voltage value from 25 to 38 V and then back to 25 V at an output voltage of 400 V, output power of 320 W is depicted in Figure 13c. As it can be seen, when the input voltage or the load changes, the PI closed-loop control can regulate the output voltage at 400 V, validating the robustness of the proposed converter.

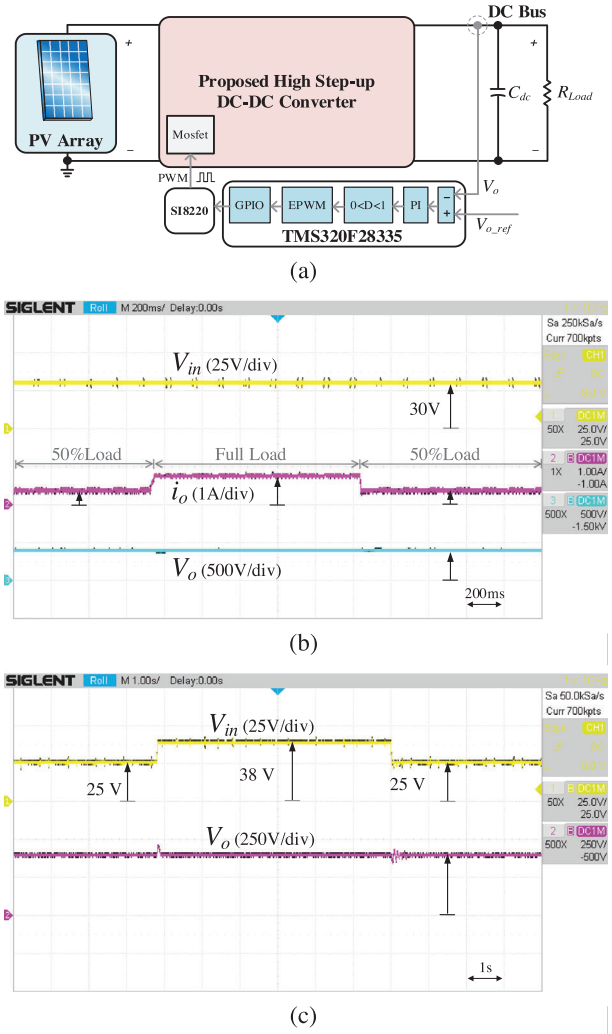

FIGURE 13 Dynamic responses of the proposed converter. (a) The control diagram of the testing. (b) A 50% step change of load variation when Vin = 30 V and Vo = 400 V. (c)The input voltage varies from 25 to 38 V and then back to 25 V under full-load condition

5 | CONCLUSION

A converter with higher voltage gain and lower voltage stress on the power switch is proposed in this paper. Three-winding coupled inductor and voltage multiplier cells are employed to enhance the voltage gain. A passive clamp circuit is used for degrading the voltage stress across the power switch. The suggested topology has the merits of high voltage gain, high efficiency, low voltage stress across the switch and the common ground structure. Moreover, the low voltage stress on the semiconductors is another advantage. The steady-state analysis of CCM and DCM conditions are presented. The key parameters of the present converter have been compared in detail with similar type of converters. Finally, a 320 W prototype with an input voltage of 30 V and an output voltage of 400 V was constructed to verify the correctness of the proposed converter. The calculated and measured efficiencies as well as the loss analysis are shown in Figures 11 and 12, respectively. Dynamic response of the proposed converter is shown in Figure 13.The presented result shows that the proposed converter has promising features for renewable energy applications.

AUTHOR CONTRIBUTIONS

Peng LUO: Writing – review & editing. Jie He: Resources, Validation, Writing – original draft. Huansheng Ji: Investigation, Validation. Fuwei Li: Methodology, Validation, Writing – original draft. Haoyu Jiang: Funding acquisition, Supervision. Limei Shi: Formal analysis, Software. Guanghao Chen: Validation.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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REFERENCES

1. Ai, J., Lin, M.: Ultralarge gain step-up coupled-inductor dc–dc converter with an asymmetric voltage multiplier network for a sustainable energy system. IEEE Trans. Power Electron. 32(9), 6896–6903 (2017)
2. Chen, S.-M., Liang, T.-J., Hu, K.-R.: Design, analysis, and implementation of solar power optimizer for dc distribution system. IEEE Trans. Power Electron. 28(4), 1764–1772 (2013)
3. Tseng, K.-C., Lin, J.-T., Huang, C.-C.: High step-up converter with three-winding coupled inductor for fuel cell energy source applications. IEEE Trans. Power Electron. 30(2), 574–581 (2015)
4. Majeed, Y.E., Ahmad, I., Habibi, D.: A multiple-input cascaded dc–dc converter for very small wind turbines. IEEE Trans. Ind. Electron. 66(6), 4414–4423 (2019)
5. Forouzesh, M., Shen, Y., Yari, K., et al.: High-efficiency high step-up dc–dc converter with dual coupled inductors for grid-connected photovoltaic systems. IEEE Trans. Power Electron. 33(7), 5967–5982 (2018)
6. Kumaravel, S., Achathuparambil Narayanankutty, R., Rao, V.S., et al.: Dual input–dual output dc–dc converter for solar pv/battery/ultra-capacitor powered electric vehicle application. IET Power Electron. 12(13), 3351–3358 (2019)
7. Kim, H., Parkhideh, B., Bongers, T.D., et al.: Reconfigurable solar converter: A single-stage power conversion pv-battery system. IEEE Trans. Power Electron. 28(8), 3788–3797 (2013)
8. Lee, S.-W., Do, H.-L.: Isolated sepic dc–dc converter with ripple-free input current and lossless snubber. IEEE Trans. Ind. Electron. 65(2), 1254–1262 (2018)
9. Yari, K., Shahalami, S.H., Mojallali, H.: High step-up isolated dc–dc converter with single input and double output and soft-switching performance for renewable energy applications. IET Power Electron. 12(11), 2942–2952 (2019)
10. Yang, N., Zeng, J., Hu, R., et al.: Analysis and design of an isolated high step-up converter without voltage-drop. IEEE Trans. Power Electron. 37(6), 6939–6950 (2022)
11. Tang, Y., Fu, D., Wang, T., et al.: Hybrid switched-inductor converters for high step-up conversion. IEEE Trans. Ind. Electron. 62(3), 1480–1490 (2015)
12. Salvador, M.A., de Andrade, J.M., Lazzarin, T.B., et al.: Nonisolated high-step-up dc–dc converter derived from switched-inductors and switched-capacitors. IEEE Trans. Ind. Electron. 67(10), 8506–8516 (2020)
13. Li, K., Hu, Y., Ioinovici, A.: Generation of the large dc gain step-up non-isolated converters in conjunction with renewable energy sources starting from a proposed geometric structure. IEEE Trans. Power Electron. 32(7), 5323–5340 (2017)
14. Liang, T.-J., Lee, J.-H., Chen, S.-M., et al.: Novel isolated high-step-up dc–dc converter with voltage lift. IEEE Trans. Ind. Electron. 60(4), 1483–1491 (2013)
15. Mohammadzadeh Shahir, F., Babaei, E., Farsadi, M.: Voltage-lift technique based nonisolated boost dc–dc converter: Analysis and design. IEEE Trans. Power Electron. 33(7), 5917–5926 (2018)
16. Luo, F.L., Ye, H.: Positive output cascade boost converters. IEE Proc. Electr. Power Appl. 151(5), 590–606 (2004)
17. Wang, Y., Qiu, Y., Bian, Q., et al.: A single switch quadratic boost high step up dc–dc converter. IEEE Trans. Ind. Electron. 66(6), 4387–4397 (2019)
18. Lee, S.-W., Do, H.-L.: Zero-ripple input-current high-step-up boost–sepic dc–dc converter with reduced switch-voltage stress. IEEE Trans. Power Electron. 32(8), 6170–6177 (2017)
19. He, L., Xu, X., Chen, J., et al.: A plug-play active resonant soft switching for current-auto-balance interleaved high step-up dc/dc converter. IEEE Trans. Power Electron. 34(8), 7603–7616 (2019)
20. Alzahrani, A., Ferdowsi, M., Shamsi, P.: High-voltage-gain dc–dc step-up converter with bifold dickson voltage multiplier cells. IEEE Trans. Power Electron. 34(10), 9732–9742 (2019)
21. Nouri, T., Hosseini, S.H., Babaei, E., et al.: Interleaved high step-up dc–dc converter based on three-winding high-frequency coupled inductor and voltage multiplier cell. IET Power Electron. 8(2), 175–189 (2015)
22. Ardi, H., Ajami, A., Sabahi, M.: A novel high step-up dc–dc converter with continuous input current integrating coupled inductor for renewable energy applications. IEEE Trans. Ind. Electron. 65(2), 1306–1315 (2018)
23. Andrade, A.M.S.S., Schuch, L., da Silva Martins, M.L.: Analysis and design of high-efficiency hybrid high step-up dc–dc converter for distributed pv generation systems. IEEE Trans. Ind. Electron. 66(5), 3860–3868 (2019)
24. Rahimi, R., Habibi, S., Shamsi, P., et al.: A three-winding coupled inductor-based dual-switch high step-up dc-dc converter for photovoltaic systems. IEEE Trans. Emerg. Sel. Topics Power Electron. 1–1 (2022)
25. Li, W., Li, W., Xiang, X., et al.: High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications. IEEE Trans. Power Electron. 29(6), 2829–2836 (2014)
26. Khalilzadeh, M., Abbaszadeh, K.: Non-isolated high step-up dc–dc converter based on coupled inductor with reduced voltage stress. IET Power Electron. 8(11), 2184–2194 (2015)
27. Chen, Z., Zhou, Q., Xu, J.: Coupled-inductor boost integrated flyback converter with high-voltage gain and ripple-free input current. IET Power Electron. 8(2), 213–220 (2015)
28. Lee, S.-W., Do, H.-L.: High step-up coupled-inductor cascade boost dc–dc converter with lossless passive snubber. IEEE Trans. Ind. Electron. 65(10), 7753–7761 (2018)

29. Wu, T.-F., Lai, Y.-S., Hung, J.-C., et al.: Boost converter with coupled inductors and buck–boost type of active clamp. IEEE Trans. Ind. Electron. 55(1), 154–162 (2008)
30. Abramovitz, A., Liao, C.-S., Smedley, K.: State-plane analysis of regenerative snubber for flyback converters. IEEE Trans. Ind. Electron. 28(11), 5323–5332 (2013)
31. Prudente, M., Pfitscher, L.L., Emmendoerfer, G., et al.: Voltage multiplier cells applied to non-isolated dc–dc converters. IEEE Trans. Power Electron. 23(2), 871–887 (2008)
32. Hu, X., Wang, J., Li, L., et al.: A three-winding coupled-inductor dc–dc converter topology with high voltage gain and reduced switch stress. IEEE Trans. Power Electron. 33(2), 1453–1462 (2018)
33. Liu, H., Li, F., Ai, J.: A novel high step-up dual switches converter with coupled inductor and voltage multiplier cell for a renewable energy system. IEEE Trans. Power Electron. 31(7), 4974–4983 (2015)
34. Rostami, S., Abbasi, V., Blaabjerg, F.: Implementation of a common grounded z-source dc–dc converter with improved operation factors. IET Power Electron. 12(9), 2245–2255 (2019)
35. Haji-Esmaeili, M.M., Babaei, E., Sabahi, M.: High step-up quasi-z source dc–dc converter. IEEE Trans. Power Electron. 33(12), 10563–10571 (2018)
36. Li, H., Cheng, L., Sun, X., et al.: High step-up combined boost-cuk converter with switched-inductor. IET Power Electron. 15(00), 1–11 (2022)
37. Elsayad, N., Moradisizkoohi, H., Mohammed, O.: A new sepic-based step-up dc-dc converter with wide conversion ratio for fuel cell vehicles: Analysis and design. IEEE Trans. Ind. Electron. 68(8), 6390–6400 (2021)
38. Abramovitz, A., Yao, J., Smedley, K.: Derivation of a family of high step-up tapped inductor sepic converters. Electron. Lett. 50(22), 1626–1628 (2014)
39. Liang, T.-J., Luo, P., Chen, K.-H.: A high step-up dc–dc converter with three-winding coupled inductor for sustainable energy systems. IEEE Trans. Ind. Electron. 69(10), 10249–10258 (2022)

How to cite this article: Luo, P., He, J., Ji, H., Li, F., Jiang, H., Shi, L., Chen, G.: A high step-Up DC-DC converter based on three-winding coupled inductor and voltage multiplier for renewable energy applications. IET Power Electron. 1–14 (2022). https://doi.org/10.1049/pel2.12443