

Synchronous Dual-Switch Ultrahigh Step-Up DC–DC Converter Based on Coupled Inductor and Voltage Multiplier for Photovoltaic Systems

Fuwei Li ^{ID}, Jie He ^{ID}, Daojiri Huang ^{ID}, Peng Luo ^{ID}, and Haoyu Jiang ^{ID}

Abstract—In this article, an ultrahigh step-up quadratic boost converter is proposed for photovoltaic systems. By integrating with a coupled inductor and a voltage multiplier, the voltage gain can be improved significantly without high turns ratio and the voltage stress across the power switches are alleviated. Thus, low on-resistance of the power switches is available to enhance efficiency. Common ground structure of quadratic boost and synchronous operation of the two switches facilitate the control. Also, the continuous input current promotes the maximum power point tracking (MPPT). Detailed description of the operation principles and steady-state analysis of this converter in continuous conduction mode and discontinuous conduction mode are presented. A 250-W rated laboratory prototype is fabricated and verified, demonstrating a maximum efficiency of 96.5%. Moreover, the dynamic response is tested to prove the stability of the proposed converter. Finally, a simulation is built to evaluate the feasibility of MPPT function.

Index Terms—DC–DC converter, high step-up, low voltage stress, photovoltaic (PV) systems, quadratic boost.

I. INTRODUCTION

TO REDUCE the pollution of fossil energy, electricity from environment friendly energy sources is developing rapidly. Among them, solar photovoltaic (PV) power generation is highly popular due to geographical independence and low maintenance costs [1], [2], [3]. The PV system, as shown in Fig. 1, requires high step-up dc–dc converters for boosting the low output voltage, and then, the energy can be transferred directly to dc loads or indirectly to ac loads or the grid via inverters.

Conventional boost converter is unable to achieve high voltage gain in the duty cycle/efficiency tradeoff, and the voltage stress on the power switch is equal to the output voltage [4], [5].

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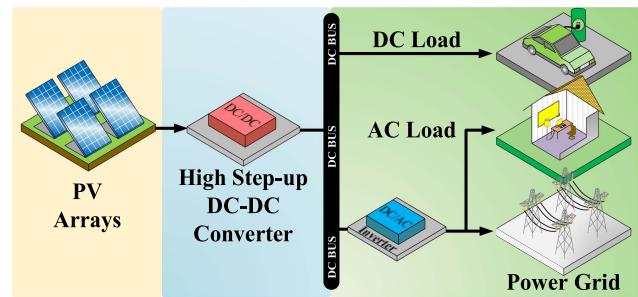


Fig. 1. Block diagram of a PV power conversion system.

Therefore, techniques and structures, such as switched inductor (SL), switched capacitor (SC), switched-capacitor-inductor (SCL) network, voltage multiplier (VM), voltage lift (VL), and multistage structure, are used to meet high step-up requirement. The concept of SL and SC with high voltage stress across the switch is initially introduced in [6] to improve the voltage gain. An SCL network is proposed in [7]. Nevertheless, it suffers from the discontinuity of input current. The VL technique can increase the output voltage through the addition of a charge path; however, the voltage gain is limited [8], [9]. A VM unit integrated with two diodes, an inductor, and a capacitor is suggested to enhance the gain exponentially in [10]. Multilevel converters essentially increase the conversion ratio by adding more boost units, yet the extra components increase losses as well as costs [11], [12].

To strike a balance between efficiency and the number of components, two methods are available [13]. The first approach is to apply coupled inductor (CI) technique. The adjustment of the turns ratio of the CI enables a significant increase in the conversion ratio, reducing the required duty cycle and conduction losses. Nonetheless, the leakage inductance of CI results in voltage spikes on the power switch, increasing the dissipation [14], [15]. Hence, active/passive clamp circuits are employed to suppress high spike voltage [16], [17]. The other method is to optimize the circuit without CI. By integrating SL and SC, a dual-switch converter with synchronous signals is proposed in [18]. However, the conversion ratio is constrained, and the discontinuous input current is not conducive to maximum power point tracking (MPPT) implementation. Featuring continuity of

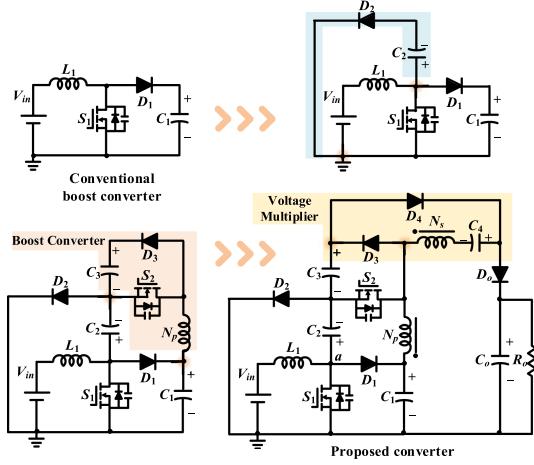


Fig. 2. Derivation process of the proposed converter.

input current, dual-switch converters with interleaved structure are presented [19], but the noncommon-ground property complicates the control. In consideration of input current continuity and common ground structure, quadratic boost converter is a promising option. Combining with VMs, quadratic structures are suggested in [20], [21], which substantially improves the voltage gain with lower voltage stress than the conventional quadratic boost converter.

Compared with a single-switch structure, dual-switch converters have broader explorability in terms of higher conversion ratio, lower voltage stress, and topology. In addition, in the CI-based topologies, energy flows through both electrical and magnetic paths, improving the performances. Consequently, researchers have investigated dual-switch high step-up converters based on CIs in recent years [22], [23], [24], [25]. A combination of a CI and a voltage doubler is presented in [22] to simultaneously improve conversion ratio and lower the devices stresses. In [23], a dual-switch converter consists of a boost, and a buck-boost converter is proposed, which realized a semiquadratic function. However, when the duty cycle improves, the voltage stress between two switches widens significantly. The converter suggested in [24] adds a quadrupler circuit to the conventional quadratic boost topology, which reduces the device stress, nonetheless, the parasitic parameters of extensive components lower the efficiency. A dual-switch high step-up converter using an integration of VM and CI is proposed in [25], but the dispersion of the input current increases the input ripple, compromising the MPPT acquisition in PV applications.

This article proposes a synchronous dual-switch ultrahigh step-up converter, with its step-by-step design shown in Fig. 2. Fig. 3 illustrates the equivalent circuit of the proposed converter, which exhibits the following features.

- 1) The common ground from the source to load and the continuity of input current facilitate control and MPPT implementation for PV applications, respectively.
- 2) The spikes generated by the leakage inductance are alleviated and the voltage stresses on switches are reduced, allowing the selection of low $r_{ds(on)}$ power switches and improving efficiency.

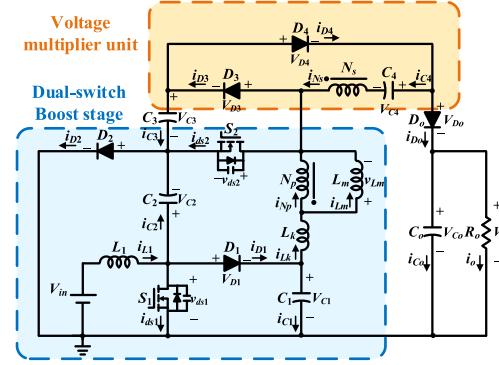


Fig. 3. Equivalent configuration of the proposed converter.

- 3) The VM shares its component with the clamp circuit of the subswitch, improving the voltage gain with lower components.
- 4) High voltage gain can be achieved at low duty cycle and low turns ratio.

The rest of this article is organized as follows. Section II analyzes the operating principles under continuous conduction mode (CCM) and discontinuous conduction mode (DCM) conditions. The theoretical analysis is demonstrated in Section III. In Section IV, a close-loop system is designed. Section V shows comparisons with relevant converters in recent years. In Section VI, the experimental results and the results of the dynamic response of the proposed converter are presented. A MATLAB-based MPPT simulation is performed in Section VII. Finally, Section VIII concludes this article.

II. PROPOSED TOPOLOGY AND OPERATIONAL PRINCIPLES

A. Assumption for Topology Analysis

To facilitate circuit analysis, the following assumptions are made.

- 1) All the power devices are ideal except the body diode of the power switch.
- 2) All capacitors are large enough that the voltage of all capacitors is considered constant for one switching cycle.
- 3) The turns ratio of the CI is defined as $N_p:N_s = 1:n$.

B. Operation Modes at CCM and DCM

In Fig. 4, the main theoretical waveforms of CCM and DCM are illustrated. Principal modes' current flow paths are presented in Fig. 5 and described as follows.

Mode I [t_0-t_1] [Fig. 5(a)]: S_1 and S_2 are turned ON synchronously. D_o is forward biased, and D_1, D_2, D_3 , and D_4 are reverse biased. i_{L1} increases linearly as L_1 receives energy from V_{in} . The energy stored in L_m is transferred to the load and C_o through N_s and C_4 . Thus, i_{Lm} decreases. This mode ends when $i_{Lm} = i_{Lk}$.

Mode II [t_1-t_2] [Fig. 5(b)]: S_1, S_2 , and D_4 are ON, D_1, D_2, D_3 , and D_o are OFF. L_1 is supply by V_{in} , so i_{L1} increases linearly. Through N_s and D_4 , the energy stored in C_3 discharges to C_4 . Meanwhile, C_1 and C_2 supply energy to L_m and L_k , so

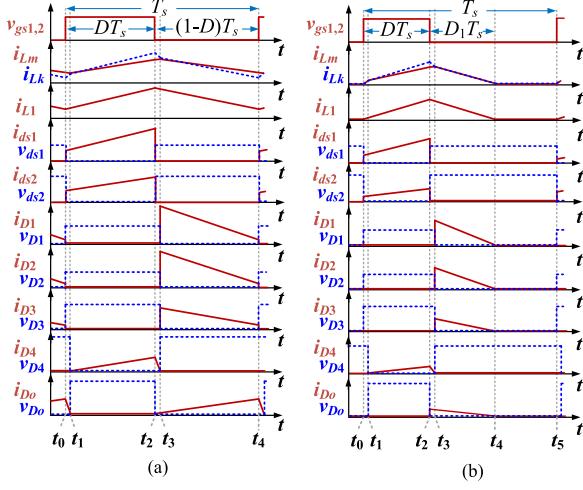


Fig. 4. Typical waveforms of the proposed converter. (a) CCM. (b) DCM.

currents i_{Lm} and i_{Lk} increase linearly. C_o transfers energy to load. This mode ends when V_{gs} is low.

Mode III [t_2-t_3] [Fig. 5(c)]: S_1 and S_2 are turned OFF. D_4 is remains forward biased, and D_1, D_2, D_3 , and D_o are reverse biased. C_1 and C_2 are connected in series to charge L_m , L_1 still receives power from V_{in} , so i_{Lm} and i_{L1} increases linearly. Meanwhile L_k releases energy and i_{Lk} decreases linearly. This mode ends when $i_{Lk} = i_{Lm}$.

Mode IV [t_3-t_4] [Fig. 5(d)]: S_1 and S_2 are OFF. D_1, D_2, D_3 , and D_o are forward biased, and D_4 is reverse biased. The voltages across S_1 and S_2 are clamped by C_1 and C_3 , respectively. The energy stored in L_1 is transfer to C_1 . L_m and C_4 supply the load and C_o through N_s and D_o . The energy stored in L_k is recycled to the load. Thus, currents i_{L1} and i_{Lm} decrease linearly.

There are five main modes during DCM operation in one switching period. Modes I–IV are the same as CCM, and only mode V is different as shown in Fig. 5(e).

Mode V [t_4-t_5] [Fig. 5(e)]: All semiconductor components are OFF. L_1 and L_m are no longer discharge energy, and C_o keeps transmitting power to the load. This mode ends when V_{gs} is high.

III. ANALYSIS AND DESIGN OF THE PROPOSED CONVERTER

A. Voltage Gain of the Converter at CCM

In CCM, the transition modes are ignored, only Mode II and Mode IV are considered. The following equations are derived during $0 \sim DT_s$ period:

$$V_{L1} = V_{in} \quad (1)$$

$$V_{Lm} = V_{C1} + V_{C2}. \quad (2)$$

During $DT_s - T_s$ period, the formulas can be obtained as

$$V_{L1} = V_{in} - V_{C1} = V_{in} - V_{C2} \quad (3)$$

$$V_{Lm} = V_{C2} - V_{C3}. \quad (4)$$

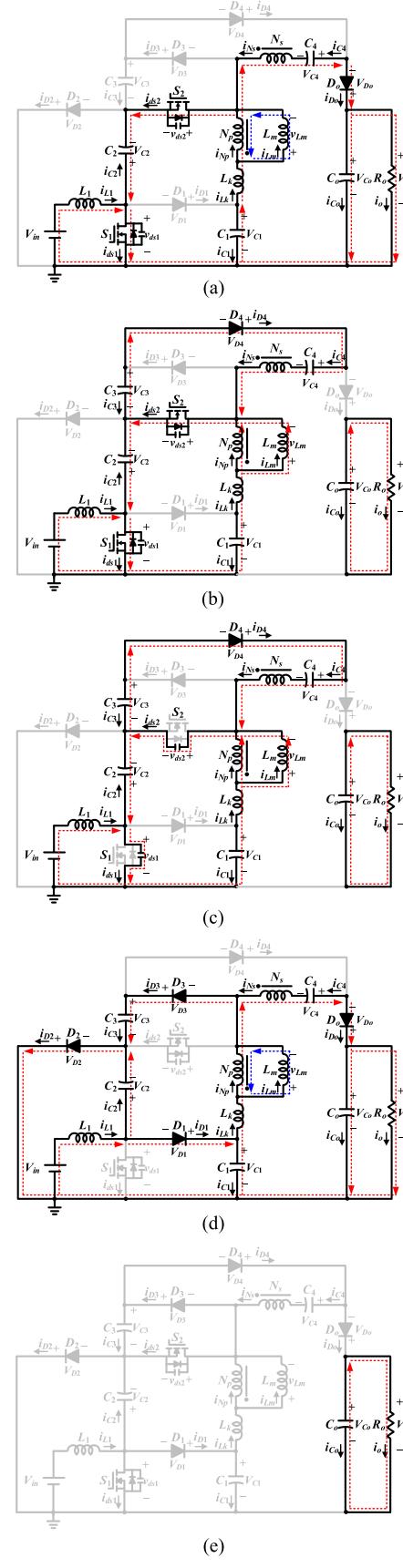


Fig. 5. Equivalent circuits of each switching state. (a) Mode I CCM and Mode I DCM. (b) Mode II CCM and Mode II DCM. (c) Mode III CCM and Mode III DCM. (d) Mode IV CCM and Mode IV DCM. (e) Mode V DCM.

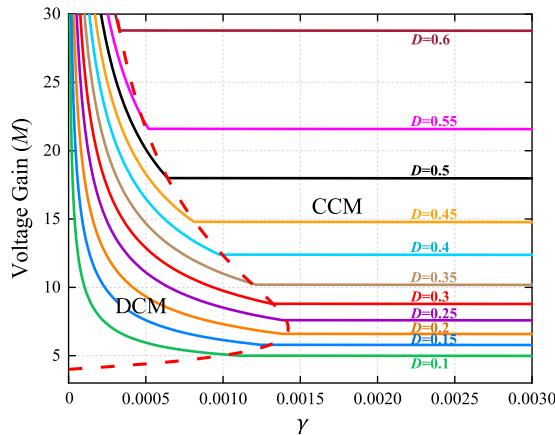


Fig. 6. External characteristic of the proposed converter.

Applying the volt-second balance on the L_1 yields

$$\int_0^{DT_s} V_{\text{in}} dt + \int_{DT_s}^{T_s} (V_{\text{in}} - V_{C1}) dt = 0 \quad (5)$$

Based on (3) and (5), we obtain

$$V_{C1} = V_{C2} = V_{\text{in}} / (1 - D) \quad (6)$$

Using (6), applying the volt-second balance on the L_m yields

$$\int_0^{DT_s} \left(\frac{2V_{\text{in}}}{1 - D} \right) dt + \int_{DT_s}^{T_s} \left(\frac{V_{\text{in}}}{1 - D} - V_{C3} \right) dt = 0. \quad (7)$$

Hence, the voltage across C_3 can be computed as

$$V_{C3} = (1 + D)V_{\text{in}} / (1 - D)^2. \quad (8)$$

Referring to Fig. 5(b) and Kirchhoff's voltage law, the voltage of C_4 is given by (2) and (8).

$$V_{C4} = nV_{Lm} + V_{C3} = (2n + 1 + D - 2nD)V_{\text{in}} / (1 - D)^2. \quad (9)$$

From Fig. 5(d), the output voltage V_o is derived according to (4), (8), and (9).

$$V_o = V_{C3} - nV_{Lm} + V_{C4} = (2 + 2n + 2D)V_{\text{in}} / (1 - D)^2. \quad (10)$$

Finally, the voltage gain M_{CCM} can be expressed as

$$M_{\text{CCM}} = V_o / V_{\text{in}} = (2 + 2n + 2D) / (1 - D)^2. \quad (11)$$

B. Voltage Stress Analysis of Switching Device

In accordance with Fig. 5(d), (6), and (8), the voltage stresses on S_1 and S_2 are, respectively, obtained as

$$V_{S1\text{-stress}} = V_{C1} = V_{\text{in}} / (1 - D) \quad (12)$$

$$V_{S2\text{-stress}} = V_{C3} = (1 + D)V_{\text{in}} / (1 - D)^2. \quad (13)$$

Referring to Fig. 5(b) and (d), the voltage stresses on $D_1 - D_5$ can be listed as follows, respectively:

$$\begin{cases} V_{D1\text{-stress}} = \frac{V_{\text{in}}}{1-D} \\ V_{D2\text{-stress}} = \frac{V_{\text{in}}}{1-D} \\ V_{D3\text{-stress}} = \frac{1+D}{(1-D)^2} V_{\text{in}} \end{cases} \quad \begin{cases} V_{D4\text{-stress}} = \frac{1+2n+D}{(1-D)^2} V_{\text{in}} \\ V_{Do\text{-stress}} = \frac{2n+2}{(1-D)^2} V_{\text{in}}. \end{cases} \quad (14)$$

C. Design of the Components

From (1), (2), and (6), the current ripples of L_m and L_1 are derived as

$$\Delta I_{L1} = 2V_{\text{in}} DT_s / L_1 \quad (15)$$

$$\Delta I_{Lm} = 2V_{\text{in}} DT_s / (1 - D) L_m. \quad (16)$$

During $DT_s - T_s$, according to Kirchhoff's current law, the following equation is written:

$$\int_{DT_s}^{T_s} i_{Lm} dt = \int_{DT_s}^{T_s} (i_{Lk} - i_{np}) dt = \int_{DT_s}^{T_s} (i_{D5} + i_{D3} - ni_{ns}) dt. \quad (17)$$

From (17), I_{Lm} is deduced as

$$I_{Lm} = (2 + n) I_o / (1 - D). \quad (18)$$

From (11), utilizing the principle of the power balance, the following equation can be attained:

$$I_{L1} = V_o I_o / V_{\text{in}} = 2I_o (1 + n + D) / (1 - D)^2. \quad (19)$$

From (15), (16), (18), and (19), the minimum currents via inductor L_m and L_1 are derived, respectively,

$$\begin{cases} I_{L1,\min} = I_{L1} - \frac{1}{2} \Delta I_{L1} = \frac{2(1+n+D)I_o}{(1-D)^2} - \frac{V_{\text{in}}}{2L_1} DT_s \\ I_{Lm,\min} = I_{Lm} - \frac{1}{2} \Delta I_{Lm} = \frac{(2+n)I_o}{1-D} - \frac{V_{\text{in}} DT_s}{(1-D)L_m}. \end{cases} \quad (20)$$

In accordance with (20), when the circuit operates in the boundary conduction mode (BCM), $I_{L1,\min}$ and $I_{Lm,\min}$ are equal to 0. Hence, the inductance values of L_1 and L_m can be obtained

$$L_1 = \left[V_{\text{in}} DT_s (1 - D)^2 \right] / 4(1 + n + D) I_o \quad (21)$$

$$L_m = V_{\text{in}} DT_s / (2 + n) I_o. \quad (22)$$

Considering the voltage ripple and the ampere-second balance, the minimum required capacitances are designed as

$$\begin{cases} C_1 \geq \frac{(n+2D)I_o}{(1-D)f_s \Delta V_{C1}} \\ C_2 \geq \frac{(n+2D)I_o}{(1-D)f_s \Delta V_{C2}} \\ C_3 \geq \frac{I_o}{f_s \Delta V_{C3}} \end{cases} \quad \begin{cases} C_4 \geq \frac{I_o}{f_s \Delta V_{C4}} \\ C_o \geq \frac{I_o}{f_s \Delta V_{Co}}. \end{cases} \quad (23)$$

where f_s is the switching frequency.

D. Voltage Gain of the Converter at DCM Operation

When the converter operates in DCM, four topological stages described for CCM are complemented by an additional fifth stage, which is depicted in Fig. 5(e). The main equations in DCM are the same as (1)–(10) in CCM. Utilizing (1), (3), and

volt-second balance equation on L_1 , we have

$$\int_0^{DT_s} V_{in} dt + \int_{DT_s}^{(D+D_1)T_s} (V_{in} - V_{C1}) dt = 0 \quad (24)$$

$$V_{C1} = V_{C2} = (D + D_1) V_{in} / D_1. \quad (25)$$

Similarly, using (2), (4), (25), and voltage-second balance on L_m , the following equations are given:

$$\int_0^{DT_s} (V_{C1} + V_{C2}) dt + \int_{DT_s}^{(D+D_1)T_s} (V_{C2} - V_{C3}) dt = 0 \quad (26)$$

$$V_{C3} = [2D^2 + (2n + 3)DD_1 + (2n + 1)D_1^2] V_{in} / D_1^2. \quad (27)$$

In Fig. 5(b), from (2), (6), and (27), V_{C4} can be derived as

$$V_{C4} = nV_{Lm} + V_{C3}$$

$$= [2D^2 + (2n + 3)DD_1 + (2n + 1)D_1^2 V_{in}] / D_1^2. \quad (28)$$

In Fig. 5(d), by using (4), (25), (27), and (28), V_o is written as

$$\begin{aligned} V_o &= V_{C3} - nV_{Lm} + V_{C4} \\ &= [(2n + 4)D^2 + (4n + 6)DD_1 + (2n + 2)D_1^2 V_{in}] / D_1^2. \end{aligned} \quad (29)$$

According to (29), D_1 is expressed as

$$D_1 = \frac{D \left[(2n + 3)V_{in} + \sqrt{V_{in}^2 + V_{in}V_o(2n + 4)} \right]}{V_o - (2n + 2)V_{in}}. \quad (30)$$

From Fig. 5(b), the maximum current value of L_m is given

$$I_{Lm\max} = 2(D + D_1) V_{in} DT_s / D_1 L_m. \quad (31)$$

Using ampere-second balance on C_4 , output current I_o is given

$$I_o = D_1 I_{Lm\max} / (4 + 2n). \quad (32)$$

From (30) to (32), the voltage gain in DCM is as follows:

$$M_{DCM} = (1 + n) + D^2 / (2 + n)\tau_{Lm} + A / \tau_{Lm}^2 \quad (33)$$

where $\tau_{Lm} = L_m / RT_s$ and $A = \sqrt{\tau_{Lm}^3 [2D^2 + \tau_{Lm}(n + 1)^2]}$.

E. External Characteristic of the Converter

To obtain the external characteristic of the proposed converter, a dimensionless parameter γ is defined as

$$\gamma = L_m I_o / V_{in} T_s. \quad (34)$$

Substituting (34) in (33), the critical value of γ is found as

$$\gamma = D^2 \left[(M + 1) + \sqrt{M^2 - 4M} \right] / 3M^2 (M - 4). \quad (35)$$

Isolating the duty cycle D in (11) and replacing the result in (34), the critical value of γ is expressed as a function of the static gain, which is depicted in Fig. 6, the dashed line shows the boundary of CCM and DCM operation.

F. Power Losses Calculation

To evaluate the conversion efficiency of the proposed converter, the parasitic parameters of the components are taken into account, and the calculation methods are shown in the following.

1) Switches Loss: The loss on the two switches consists of two parts: conduction loss (P_{Con_S}) and switching loss (P_{Sw_S}). The calculation formulas are as follows.

$$P_{Con_S} = r_{ds1} \frac{(n + nD + 4D)^2}{D(1 - D)^4} I_o^2 + r_{ds2} \frac{(1 + n + D)^2}{D(1 - D)^2} I_o^2 \quad (36)$$

$$\begin{aligned} P_{Sw_S} = & \left(\frac{n + nD + 4D}{6D(1 - D)^3} \right. \\ & \left. + \frac{(1 + D)(1 + n + D)}{6D^2(1 - D)^3} \right) V_{in} I_o f_s (t_{on} + t_{off}) \end{aligned} \quad (37)$$

where r_{ds} , t_{on} , and t_{off} are the on-resistance of MOSFETs, rise time, and fall time, respectively.

Hence, the total power loss of the switches is given.

$$P_{S_Loss} = P_{Con_S} + P_{Sw_S}. \quad (38)$$

2) Diodes Loss: The diodes' power losses are related to the average current (I_D), forward voltage drop (V_F), and the conduction resistance (r_D). The conduction losses of the diodes are as follows:

$$\begin{cases} P_{D1} = V_{F1} I_{D1} + \frac{r_{D1}(n+2)^2 I_o^2}{(1-D)^3} \\ P_{D2} = V_{F2} I_{D2} + \frac{r_{D2}(n+D+1)^2 I_o^2}{(1-D)^3} \\ P_{D3} = V_{F3} I_{D3} + \frac{r_{D3} I_o^2}{(1-D)^3} \end{cases} \begin{cases} P_{D4} = V_{F4} I_{D4} + \frac{r_{D4} I_o^2}{D^3} \\ P_{Do} = V_{Fo} I_{Do} + \frac{r_{Do} I_o^2}{(1-D)^3}. \end{cases} \quad (39)$$

The total diodes power loss can be given as

$$P_{D_Loss} = P_{D1} + P_{D2} + P_{D3} + P_{D4} + P_{Do}. \quad (40)$$

3) Capacitors Loss: The losses of the capacitors can be calculated as follows:

$$\begin{cases} P_{C1} = P_{C2} = r_{C1} \frac{(n+2D)^2 I_o^2}{D(1-D)^3} \\ P_{C3} = P_{C4} = r_{C3} \frac{I_o^2}{D(1-D)} \end{cases} \begin{cases} P_{Co} = r_{Co} \frac{DI_o^2}{(1-D)} \end{cases} \quad (41)$$

Thus, the total loss of the capacitors can be written as

$$P_{C_Loss} = P_{C1} + P_{C2} + P_{C3} + P_{C4} + P_{Co}. \quad (42)$$

4) Inductors Loss: The power losses of the inductors contain winding losses (P_{L1_Loss} , P_{CI_Loss}) and core losses (P_{L_Core}), so the following equations can be listed:

$$P_{L1_Loss} = \left[\left(\frac{n^2 + 4nD + 4D^2}{D^2 - 2D^3 + D^4} \right) D + \frac{4}{1 - D} \right] I_o^2 r_{Lp} \quad (43)$$

$$P_{CI_Loss} = \left(\frac{I_o}{D} \right)^2 r_{Lp} + \left[\frac{2I_o(1 + n + D)}{(1 - D)^2} \right]^2 r_{Ls} \quad (44)$$

$$P_{L_Core} = P_{cv,L1} V_{e,L1} + P_{cv,Lm} V_{e,Lm} \quad (45)$$

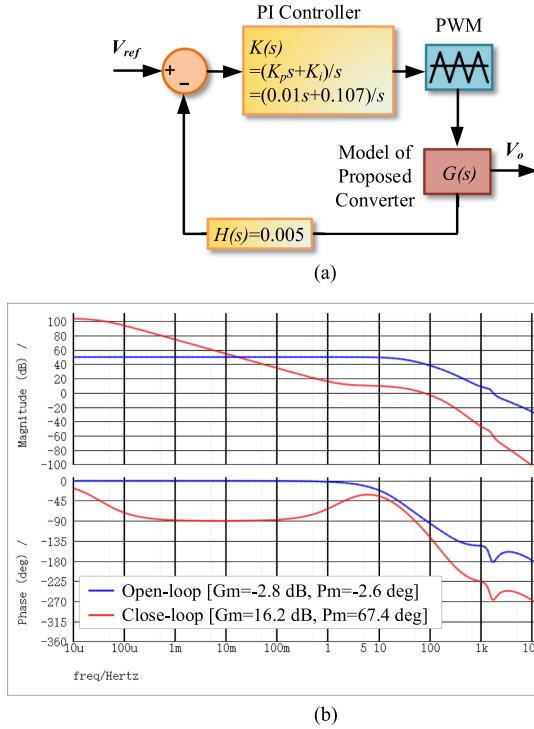


Fig. 7. (a) Designed closed-loop system of the proposed converter. (b) Bode diagrams of the open-loop and closed-loop transfer functions.

where \$r_L\$ is the equivalent resistance of inductor, \$P_{cv,L}\$ means the core loss per unit volume, and \$V_{e,L}\$ is the effective volume of the converter.

Hence, the total power loss of the inductors is as follows:

$$P_{L_Loss} = P_{L1_Loss} + P_{CI_Loss} + P_{L_core}. \quad (46)$$

Finally, the efficiency of the proposed converter can be concluded as

$$\eta = P_o / (P_o + P_S_Loss + P_D_Loss + P_C_Loss + P_L_Loss). \quad (47)$$

IV. CLOSED-LOOP SYSTEM DESIGN

To regulate the output voltage, Fig. 7(a) shows the designed closed-loop system of the proposed converter. The feedback transfer function \$H(s)\$ is set to 0.005, and the transfer function of voltage controller is defined as

$$K(s) = \frac{K_p s + K_i}{s} \quad (48)$$

where \$K_p\$ is compensator gain and \$K_i\$ represents integration factor.

By using frequency-sweep method in SIMetrix/SIMPLIS, Fig. 7(b) shows the Bode diagrams in the open-loop and closed-loop systems. The values of \$K_p\$ and \$K_i\$ are 0.01, and 0.107, respectively. Therefore, the phase and gain margins are \$-2.6^\circ\$ and \$-2.8\$ dB for the open-loop system and \$67.4^\circ\$ and \$16.2\$ dB for the closed-loop system, respectively, verifying the stability of the closed-loop system.

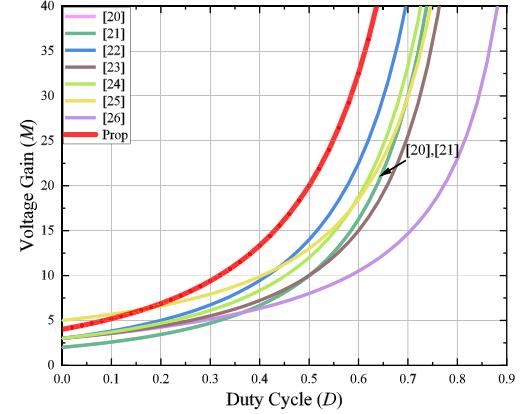


Fig. 8. Voltage gain comparisons of the proposed converter and related converters under \$n = 1\$.

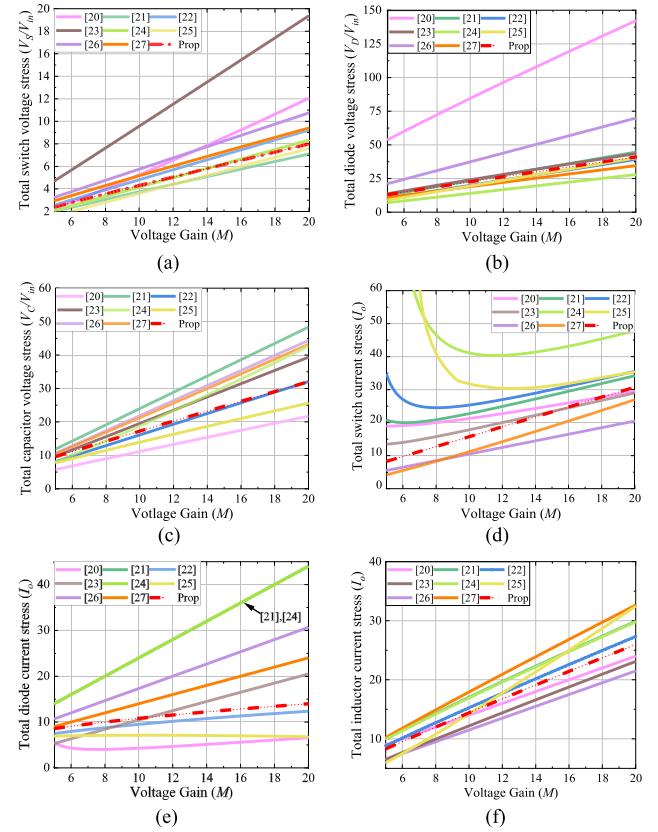


Fig. 9. Normalized comparisons with latest existing high step-up converter. (a) Total switch voltage stress. (b) Total diode voltage stress. (c) Total capacitor voltage stress. (d) Total switch current stress. (e) Total diode current stress. (f) Total inductor current stress.

V. PERFORMANCE COMPARISON

To demonstrate the performance of the proposed converter, comparisons are made with the relevant high step-up converters.

A. Voltage Stress and Current Stress Comparison

Table I illustrates the performance metrics, which contain the number of components, voltage gain, total voltage stress

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH RELATED CONVERTERS

Topology	Number of Components D/C/S/ L+CI/T	Voltage Gain (M)	Total Voltage Stress on Switches (V_{ds}/V_{in})	Full Load Efficiency (%)	Maximum Experimental Parameters			CG	SS	Continuous input current
					n	Duty Cycle (D)	Gain			
[20]	5/5/1/1+1/13	$\frac{n(3D+2)+(2-D)}{2(1-D)^2}$	$\frac{2+D(n-1)}{n(3D+2)+(2-D)}M$	92.96	2	0.5	16.7	yes	no	yes
[21]	6/5/1/1+1/14	$\frac{1+n+nD}{(1-D)^2}$	$\frac{M}{1+n+nD}$	92.3	1.9	0.31	10	yes	no	yes
[22]	5/5/2/1+1/14	$\frac{1+2n+D}{(1-D)^2}$	$\frac{2M}{1+2n+D}$	94.1	1	0.5	14	yes	yes	yes
[23]	4/4/2/1+1/12	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{2M}{1+D+2n(1-D)}$	93.6	0.6	0.55	10	yes	no	yes
[24]	6/6/2/1+1/16	$\frac{1+2n}{(1-D)^2}$	$\frac{2M}{1+2n}$	90.6	1.9	0.4	18	yes	yes	yes
[25]	5/5/2/1+1/14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{(2-D)M}{3+2n-D(3+n-D)}$	94.1	1.5	0.57	20	yes	no	yes
[26]	4/5/1/1+1/12	$\frac{2+n+D(n+1)}{1-D}$	$\frac{M}{2+n+D(n+1)}$	93.6	2	0.61	15	yes	no	yes
[27]	4/4/1/2+1/12	$\frac{n-1+nD}{(1-D)^2(n-1)}$	$\frac{(n-1)M}{n-1+nD}$	89.9	1.25	0.49	13.8	yes	no	yes
Prop	5/5/2/1+1/14	$\frac{2+2n+2D}{(1-D)^2}$	$\frac{M}{1+n+D}$	94.3	1	0.46	16.7	yes	no	yes

Prop = Proposed converter, D = Diode, C = Capacitor, S = Switch, L = Inductor, CI = Coupled inductor, T = Total number of components used, CG = Common ground, SS = Soft switching.

on the switches, full-load efficiency, experimental parameters, common ground structure, soft switching, and continuous input current. The voltage gain curves are shown in Fig. 8, and the normalized voltage stresses and current stresses are presented in Fig. 9.

In Fig. 8, the proposed converter features the highest voltage gain compared with the relevant converters. From Fig. 9(a) and (b), it can be observed that the total semiconductor voltage stresses of the proposed converter are lower than converters in [20], [22], [23], [26]. In addition, Fig. 9(d) shows that the proposed converter has lower total switch current stress compared with converters in [21], [24], [25]. Thus, a low on-resistance power switch can be used to effectively reduce the switch losses. The converter in [24] achieves soft switching with low total diode voltage stress. Nonetheless, higher total diode current stress leads to increased conduction losses and reduced efficiency. According to Fig. 9(c) and (f), the proposed converter has a medium level of total capacitor voltage stress and total inductor current stress. Overall, considering the PV application scenario, the proposed converter strikes a good balance between voltage gain and devices voltage and current stress.

B. Component Stress Factor (CSF) Comparison

CSF is an analytical method that estimates the converter stresses under specific operating conditions and quantitatively measures the performance of converter. The total CSF (TCSF) is divided into four parts as (49), namely, CSF_S for switches, CSF_D for diodes, CSF_W for inductor windings, and CSF_C for capacitors.

$$TCSF = CSF_S + CSF_D + CSF_W + CSF_C$$

$$= \sum_{i=1}^{N_S} \frac{V_{S,i(\max)} \times I_{S,i(\text{rms})}}{P_o} + \sum_{i=1}^{N_D} \frac{V_{D,i(\max)} \times I_{D,i(\text{rms})}}{P_o}$$

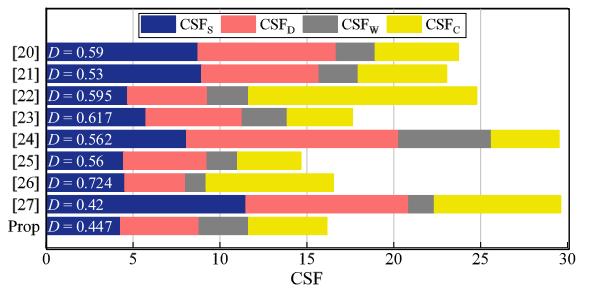


Fig. 10. CSF breakdown calculation.

$$\begin{aligned} &+ \sum_{i=1}^{N_W} \frac{V_{W,i(\max)} \times I_{W,i(\text{rms})}}{P_o} \\ &+ \sum_{i=1}^{N_C} \frac{V_{C,i(\max)} \times I_{C,i(\text{rms})}}{P_o}. \end{aligned} \quad (49)$$

With the operating power of $P_o = 250$ W, input voltage $V_{in} = 24$ V, $V_o = 400$ V, $f_s = 50$ kHz, and equal component weights, the CSF breakdown calculation is shown in Fig. 10. To minimize the impact of leakage inductance, turns ratio is selected as $n = 1.1$. As can be seen in Fig. 10, the proposed converter exhibits the best performance in CSF_S , exceeding that of the single switch topologies in [20], [21], [26], [27]. Moreover, the total CSF of the proposed converter is the best in terms of TCSF in comparison except for [25], indicating its relatively low cost and high efficiency.

C. Loss and Efficiency Comparison

The comparison of the estimated efficiency with relevant converters is shown in Fig. 11(a). It is shown that the proposed converter has a higher efficiency compared with the converters

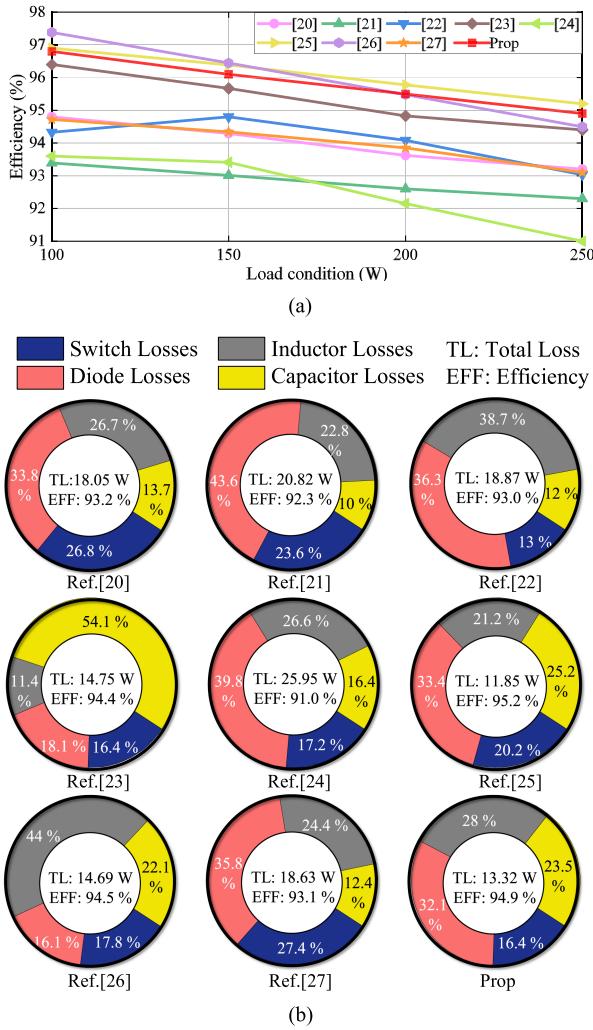


Fig. 11. (a) Estimated efficiency at 100, 150, 200, and 250 W. (b) Power loss breakdown comparison under $P_o = 250$ W.

in [20], [21], [22], [23], [24], [27]. Fig. 11(b) shows the loss distribution at 250 W. With the effective clamping circuits of C_1-D_1 and C_3-D_3 , the proposed converter performs lowest switch losses by reducing the conduction losses. Conversely, the converter in [27] has the highest switch losses due to inefficient discharge of the leakage inductor energy when the switch is OFF.

In summary, the results indicate that the proposed converter performs lower total losses among the other converters, resulting in higher estimated efficiency.

VI. EXPERIMENTAL RESULTS

To demonstrate the correctness of the theoretical analysis, a prototype of the proposed converter operating at 250 W was constructed and tested. The experimental parameters and circuit specifications are shown in Table II, and the experimental prototype is presented in Fig. 12. The pulsewidth modulation signal is generated by a TMS320F28335 microcontroller.

The inductance values L_1 and L_m can be given from (21) and (22) under the BCM condition of $V_{in} = 24$ V, $V_o = 400$ V,

TABLE II
EXPERIMENTAL PARAMETERS AND CIRCUIT SPECIFICATIONS

Experimental parameters	Specifications
Input voltage (V_{in})	24 V
Output voltage (V_o)	400 V
Rated Power (P_o)	250 W
Switching frequency (f_s)	50 kHz
Switches (S_1, S_2)	IP110N20N3
Diodes	D_1, D_2 : MBR20100; D_3 : MBR20300; D_4, D_o : MUR260
Capacitors	C_1, C_2, C_o : 220 μ F; C_3, C_4 : 47 μ F
Magnetizing inductor (L_m, L_k)	$L_m = 292 \mu$ H, $L_k = 4 \mu$ H, core material: 3C90, bobbin: PQ3535, $N_p, N_s = 25:25$
Inductor (L_1)	26 μ H, core material: 3C90 bobbin: PQ3230

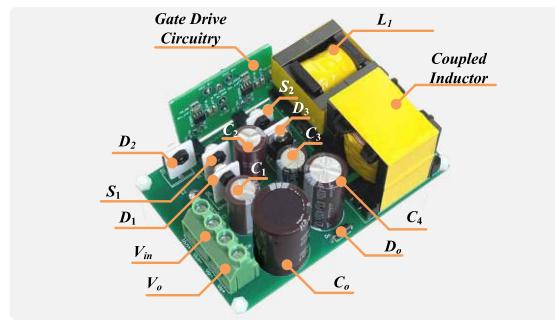


Fig. 12. Experimental prototype of the proposed converter.

$I_{o,BCM} = 0.25$ A, and the turns ratio $n = 1$, respectively.

$$\begin{aligned} L_1 &\geq \frac{V_{in}DT_s(1-D)^2}{4(1+n+D)I_{o,BCM}} \\ &= \frac{24 \times 0.46 \times 5 \times 10^{-4} \times (1-0.46)^2}{4 \times (1+1+0.46) \times 0.25} = 26 \mu\text{H} \\ L_m &\geq \frac{V_{in}DT_s}{(2+n)I_{o,BCM}} = \frac{24 \times 0.46 \times 5 \times 10^{-4}}{(2+1) \times 0.25} = 292 \mu\text{H}. \end{aligned}$$

The experimental waveforms under CCM are presented in Fig. 13. The waveforms of the drive signal, the voltages of S_1 , S_2 , and D_1 , and the currents of L_1 and D_1 are shown in Fig. 13(a) and (b). The current value of i_{L1} is always greater than zero, where the average value of i_{L1} is about 10.4 A. The voltages across switches S_1 and S_2 are about 45 V and 118 V, which are consistent with the theoretical analysis, and the voltage spikes of the switches are well suppressed. Fig. 13(c)–(f) indicates the current and voltage waveforms of the diodes and capacitors, all of which agree with the theoretical analysis. As shown in Fig. 13(g), with the duty cycle D about 0.46, the 24 V input power is converted to 400 V output power, which is 16.7 times of the voltage gain. Under $V_{in} = 24$ V, $V_o = 400$ V, and $P_o = 50$ W, Fig. 14 shows the measured DCM waveforms in open loop. During the turn-OFF time of switches, V_{ds1} resonates with

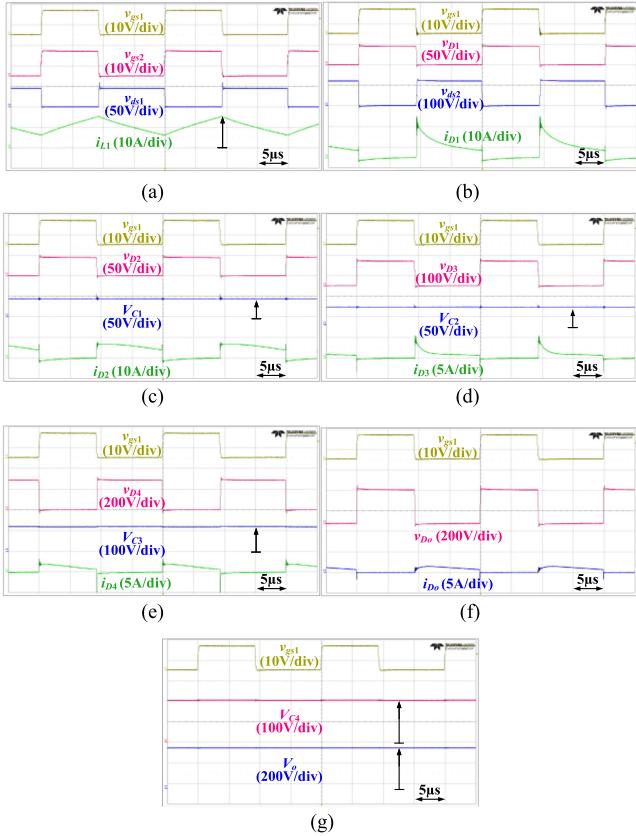


Fig. 13. Measured experimental waveforms under CCM ($V_{in} = 24$ V and $P_o = 250$ W). (a) v_{gs1} , v_{gs2} , v_{ds1} , i_{L1} . (b) v_{gs1} , v_{D1} , v_{ds2} , i_{D1} . (c) v_{gs1} , v_{D2} , V_{C1} , i_{D2} . (d) v_{gs1} , v_{D3} , V_{C2} , i_{D3} . (e) v_{gs1} , v_{D4} , V_{C3} , i_{D4} . (f) v_{gs1} , v_{Do} , i_{Do} . (g) v_{gs1} , V_{C4} , V_o .

L_1 and V_{ds2} resonates with L_1 and L_m in series, resulting in voltage oscillations on the diodes.

Fig. 15(a) indicates the dynamic response of the proposed converter for a 50% load step change. When the load varies, the PI closed-loop control is capable of regulating the output voltage at 400 V, confirming the stability of the proposed converter. Fig. 15(b) shows the transient response of the proposed converter with an input voltage from 22 to 26 V and then back to 22 V. When the input power varies, the output voltage can be regulated to 400 V.

Fig. 16 shows the estimated and experimental efficiency curves of the proposed converter at load conditions ranging from 25 to 250 W, and estimated efficiency curve ranging from 100 to 250 W. The full load efficiency of the experimental prototype is 94.3%, and the maximum efficiency is 96.5%. The efficiencies from light load to full load are greater than 90%, exhibiting the promising performance of the converter.

VII. MPPT EVALUATION

Applying the incremental conductance algorithm, an MPPT model is built in MATLAB/Simulink to fully exploit the capacity of the PV panel. It is assumed that the mathematical model simulates a daily operation where the surface temperature is selected as 25 °C. To analyze the dynamic response of the PV

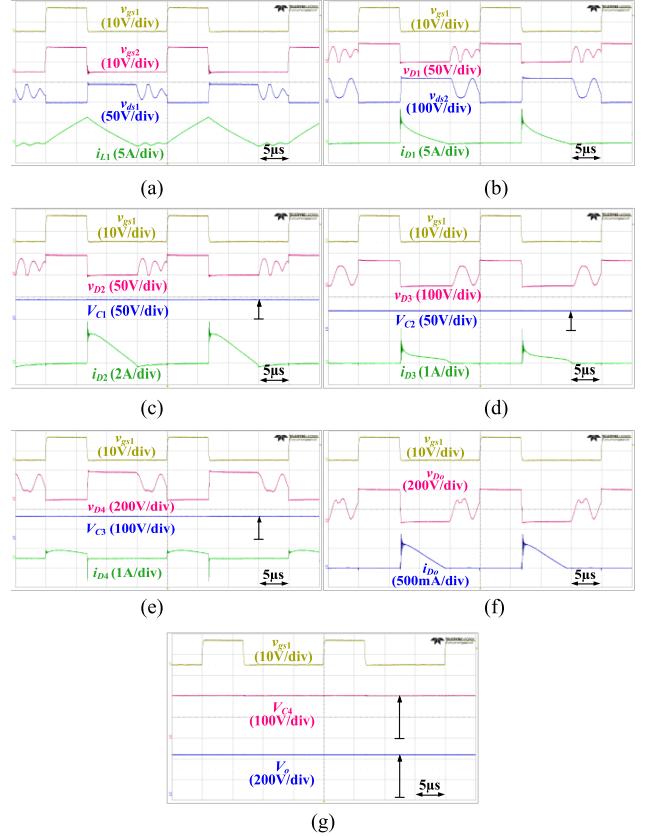


Fig. 14. Measured experimental waveforms under DCM ($V_{in} = 24$ V and $P_o = 50$ W). (a) v_{gs1} , v_{gs2} , v_{ds1} , i_{L1} . (b) v_{gs1} , v_{D1} , v_{ds2} , i_{D1} . (c) v_{gs1} , v_{D2} , V_{C1} , i_{D2} . (d) v_{gs1} , v_{D3} , V_{C2} , i_{D3} . (e) v_{gs1} , v_{D4} , V_{C3} , i_{D4} . (f) v_{gs1} , v_{Do} , i_{Do} . (g) v_{gs1} , V_{C4} , V_o .

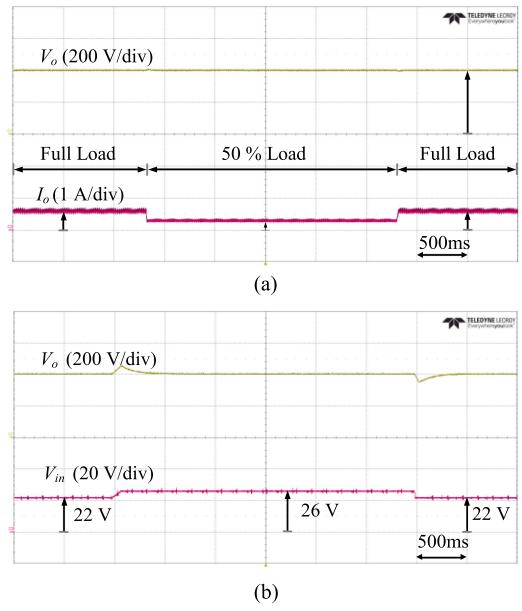


Fig. 15. Dynamic responses of the proposed converter. (a) 50% step change of load variation when $V_{in} = 24$ V and $V_o = 400$ V. (b) Input voltage varies from 22 to 26 V and then back to 22 V under full load.

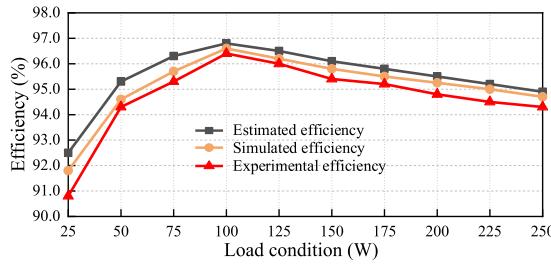


Fig. 16. Estimated, simulated, and experimental efficiencies of the proposed converter.

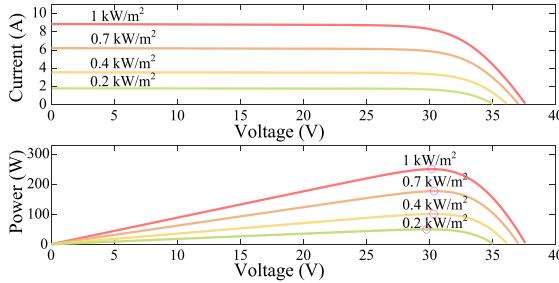


Fig. 17. I - V and P - V curves of solar array.

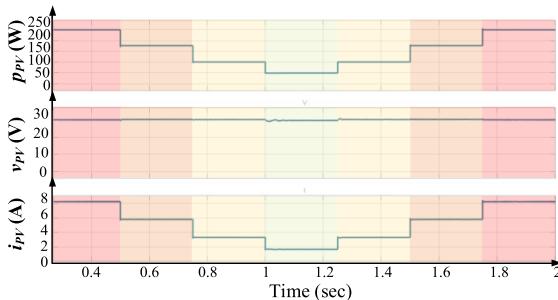


Fig. 18. Solar-powered high step-up converter input power, input voltage, and input current according to changing solar irradiance.

system, sudden changes in irradiance are considered as follows: 1000 W/m^2 , 700 W/m^2 , 400 W/m^2 , and 200 W/m^2 of irradiance are each given for 0.25 s as irradiance input to the PV panel. Fig. 17 exhibits the I - V and P - V curves of the PV panel at three different irradiance levels. As shown in Fig. 18, the maximum power of the PV-model is efficiently tracked when the irradiance varies.

VIII. CONCLUSION

In this article, a dual-switch ultrahigh step-up converter with continuous input current was proposed. With the implantation of the clamp circuit and the integration of CI and VM, the proposed converter exhibited lower voltage stress and higher voltage gain compared with the related converters. The recovery of the leakage inductance energy to the load and the utilization of low $r_{ds\text{on}}$ devices enabled the experimental realization of a 250-W prototype with a maximum efficiency of 96.5%. In addition, the dynamic response test was conducted to verify the stability of the proposed converter. Finally, the MPPT capability was estimated through MATLAB-based simulation.

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