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ORIGINAL ARTICLE

Quadratic-type high step-up DC–DC converter with continuous input current integrating coupled inductor and voltage multiplier for renewable energy applications

Fuwei Li[1] · Jie He[1] · Peng Luo[1] · Haoyu Jiang[1] · Mingxin Liu[1]

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Abstract
This paper presents a quadratic-type high step-up DC–DC converter for renewable energy applications with a continuous input current. To reduce the number of components while increasing the gain, a quadratic boost converter and two multiplier cells are applied as the primary and secondary circuit with one coupled inductor connected. In addition, the clamp circuit shares its components with both the second boost stage and the voltage multiplier, which increases the power density. As a result, the leakage energy is recycled and the voltage stress can be suppressed. The operation principles and steady-state analyses including loss analysis of the proposed converter are addressed in detail. Compared with relevant existing topologies of quadratic converter, the proposed converter performs a higher voltage gain and a lower power switch stress. To validate the performance, a 200 W experimental prototype is constructed and tested with 20 V of input voltage and 400 V of output voltage, where the highest efficiency is 95.2% and the full-load efficiency is 93.7%. The performance under dynamic conditions is also verified. In the end, an improved topology based on the proposed converter is supplemented.

Keywords DC–DC converter · Quadratic boost · Coupled inductor · High voltage gain · Renewable energy applications

1 Introduction

In recent years, the earth has experienced severe pollution problems due to the overuse of fossil fuel. To prevent environmental pollution, harvesting energy from renewable resources such as wind power, photovoltaic power, and fuel cells is a promising solution [1, 2]. However, the low output voltages provided by these renewable energy sources cannot be directly utilized [3]. Thus, high step-up DC–DC converters are in great demand for renewable energy applications [4]. As shown in Fig. 1, these converters can boost low voltage sources of energy. Thus, renewable energy can be transferred to the power grid or the AC load through an inverter or transferred directly into a DC load.

The conventional DC–DC boost converter is a common method for increasing the voltage gain [5]. However, an extremely high duty cycle is required. In addition, the voltage across the power switch is equivalent to the voltage of the output. Thus, a high $R_{ds\text{-}on}$ switch is required, which leads to more conduction losses. To obtain a high gain at a suitable duty cycle, the coupled inductor technique is widely used. It allows for employing a turns ratio to further increase the gain factor [6]. Nevertheless, achieving a high voltage gain with a coupled inductor requires a high turns ratio, which produces more conduction losses, and the major drawback of using coupled inductor is the voltage spike on the switch caused by the discharging energy of the leakage inductance [7]. Therefore, a snubber circuit is applied to alleviate the spike voltage of the switch. However, snubber circuits have dissipation problems [8], so the active clamp circuit is adopted. The leakage inductance energy is recovered by the active clamp circuit, improving efficiency, but the complexity and cost are increased due to the extra switch [9]. Hence, passive clamp circuits are worth considering due to their simple structure [10]. However, the voltage gain exhibited by these converters is not high enough.

To obtain a higher boost factor, some methods have been proposed such as cascade, interleaved, switched capacitor [11], switched inductor [12], and multiplier cells [13]. By combining the conventional boost with the above-mentioned

✉ Haoyu Jiang
john_h_y_walter@163.com

[1] School of Electronic and Information Engineering, Guangdong Ocean University, Zhanjiang, China

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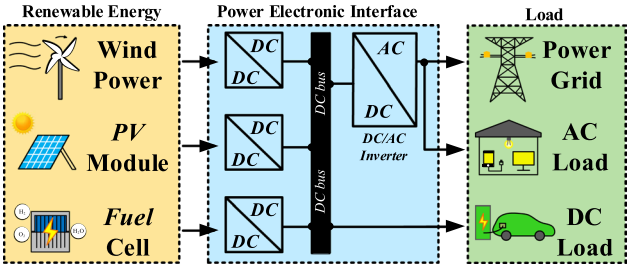

Fig. 1 Block diagram of renewable energy

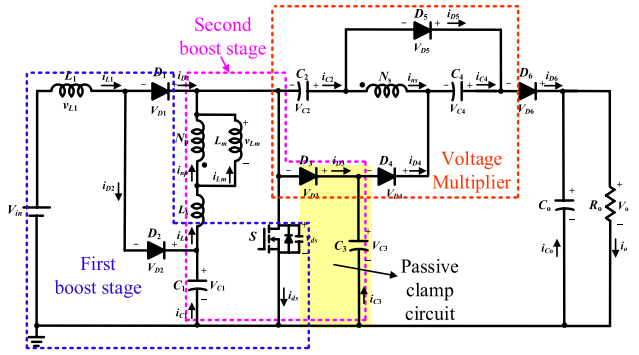

Fig. 2 Simplified circuit of the proposed converter

techniques, some topologies have been presented. A converter made up of a switched capacitor and a switched inductor to achieve a high voltage gain was presented in [14]. However, it has a large number of components, which increased the cost and size of the converter. By combining the interleaved technique and a voltage multiplier cell, a high transfer ratio was realized [15]. In addition, it can be extended by simply adding capacitor–diode stages. A cascaded boost converter with the multiple winding technique was adopted in [16]. However, the multiplicity of devices and the big transformer are the drawbacks of this converter. The cascade technique has two common types, one is the hybrid type, which connects two or more different types of converters to achieve a high voltage gain, and the other is the quadratic type [17].

The quadratic boost converter has a number of attractive features. It has a simple structure consisting of two stages of boost circuits connected in series and the two switches are integrated into one, which has the effect of improving the power density [18]. Moreover, it is noteworthy that its voltage gain is a quadratic function of a traditional boost circuit [19]. Therefore, quadratic boost technology can achieve a high voltage gain by slightly adjusting the duty cycle. However, it inherits the disadvantage of traditional boost, which is the fact that the high voltage stress on the switch is equal to the output voltage [20]. Consequently, to reduce the voltage stress and achieve a high boost ratio, the optimized quadratic boost converters were proposed in [21–30]. The converters in [21–23] consist of quadratic boost and voltage multipliers that were proposed without using coupled inductors. With the aid of voltage multipliers, the gain of these converters has been improved to some extent, but it is not raised significantly in [21] and [22] due to the lack of tunability of the coupling inductor in the structure. Although the converter in [23] achieved four times the gain of the quadratic circuit using a large number of components, the loss is extremely high. Nevertheless, versus a conventional quadratic boost, these circuits do have reductions in the voltage stress of the components. By adding a coupled inductor to the topology, the converter in [24–30] presents a greater advantage in terms of gain while the stresses on some components are further reduced when the turns ratio n increases. Naturally, the problem of the spikes caused by the leakage inductance owning to the coupled inductor cannot be ignored. Thus, a clamp circuit should be considered. The converter in [24] shows a quadratic boost converter stacked up with a flyback converter. The gain can be easily upgraded by increasing the turns ratio, while the voltage stress of the switch is suppressed by a clamp circuit where the clamp capacitor is in series with another output capacitor. Quadratic converters based on a coupled inductor with a passive snubber/clamp circuit were presented in [25] and [26]. The voltage spike caused by the leakage inductance is reduced. Hence, low-voltage-rating switches can be used, which reduces the cost. Furthermore, the leakage energy of these converters is recycled to minimize the dissipation. The research reported in [27–30] introduced quadratic boost converters that combine voltage multipliers and a coupled inductor. These converters are capable of achieving a high gain and a relatively high efficiency without the need for extremely high duty cycles and high turn ratios.

Inspired by the previously presented topologies, a quadratic boost converter integrated with a coupled inductor, voltage multiplier is proposed as shown in Fig. 2. Generally, a discontinuous input current leads to a high current ripple, which means a large filter should be employed at the input port. Hence, continuous input current is considered in this paper to avoid this problem, reducing the stresses of the input port and enlarging the lifetime of the components. Moreover, the continuous input feature makes the proposed converter ideal for current-sensitive energies such as batteries and fuel cells. Conventionally, a cascade boost converter needs two or more switches to enhance a high voltage gain. However, this requires many components and complicates the control. By optimizing the structure, the quadratic boost technique is insert into the proposed topology, where only one switch and one control circuit are required. In addition, no additional devices are needed to form the clamp circuit. The clamp circuit shares its components with the second boost stage and the voltage multiplier, improving the

power density. Furthermore, the leakage inductance energy is recycled to the output which results in a high-efficiency performance.

The remainder of this paper is organized as follows. Section 2 shows the analysis of operating principles. In Sect. 3, a steady-state analysis is demonstrated in the continuous conduction mode (CCM), which includes analyses of the voltage gain, voltage stress, current stress, and power loss. Furthermore, the performance of the proposed circuit is compared with those of other quadratic-boost-based circuits in Sect. 4. In Sect. 5, a prototype with an input voltage of 20 V, an output voltage of 400 V, and an output power of 200 W is constructed, and the feasibility of the converter is verified by experimental results. In addition, the dynamic response performance of the proposed converter is verified in this section. To illustrate the extendibility of the circuit, an improved topology based on the proposed converter is presented in Sect. 6. Finally, the conclusion is given in Sect. 7.

2 Operating principles

To simplify the analysis of the proposed circuit, the following conditions are assumed to be true.

1) All the power devices excluding the body diode of power switch are ideal.

2) The capacitors C_1, C_2, C_3, C_4, and C_o are large enough, and the voltages V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{Co} can be seen as constant.

3) The turns ratio of the coupled inductor is defined as $Np{:}N_S = 1{:}n$.

Based on the above assumptions, the key waveforms of the proposed converter operating in the CCM during one switching period are shown in Fig. 3. In one switching period, the converter operating in the CCM can be divided into four modes, and the current flow paths for each of the modes are demonstrated in Fig. 4a–d.

Mode I [$t_0 \sim t_1$]: During this mode, the switch S is turned on, and the diodes D_1 and D_6 are on, while D_2, D_3, D_4, and D_5 are off. The paths of the currents are shown in Fig. 4a. V_{in} charges the inductor L_1 through D_1. Therefore, i_{L1} and i_{D1} start to increase. L_m releases energy to the primary side of the coupled inductor, the leakage inductance, and capacitor C_1. Therefore, the magnetizing inductance current i_{Lm} decreases, and the leakage inductance current i_{Lk} increases. Meanwhile, the capacitors C_2 and C_4 release energy to the load through D_6. This mode ends when i_{Lm} is equal to i_{Lk}.

Mode II [$t_1 \sim t_2$]: In this interval, the switch S is turned on, and the diodes D_1, D_4, and D_5 conduct. The equivalent circuit is shown in Fig. 4b. V_{in} provides energy for the inductor L_1, and the current across L_1 increases linearly. The energy stored in C_1 is released to the magnetic inductance L_m and the leakage inductance L_k. Thus, i_{Lm} and i_{Lk} continue rising.

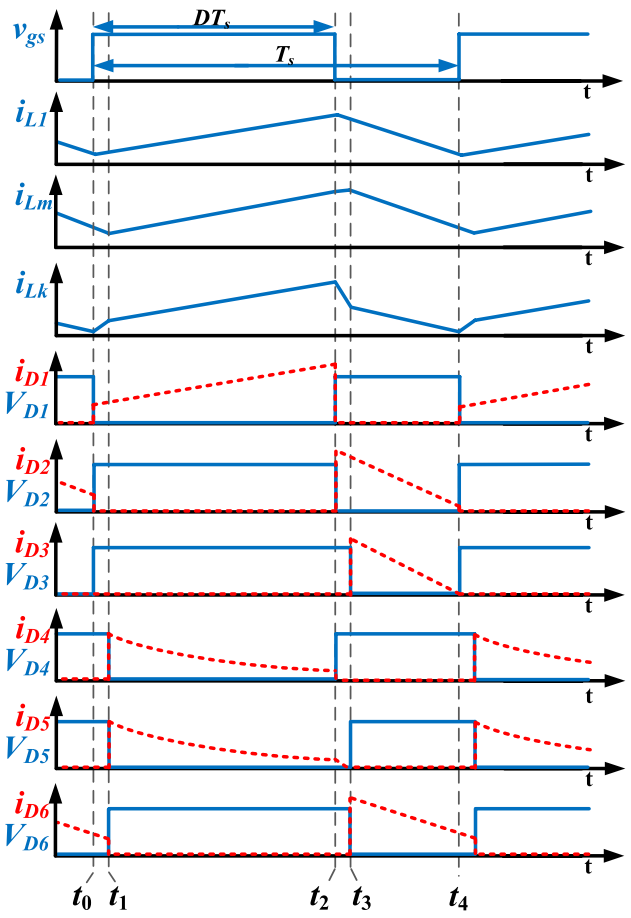

Fig. 3 Key waveforms of the proposed converter in the CCM

The energy stored in N_s is released to the capacitors C_2 and C_4 through D_4 and D_5, respectively. The clamp capacitor C_3 transfers energy to C_2. Therefore, the currents i_{D4} and i_{D5} increase. C_o provides energy to the load. This mode ends when the switch is turned off.

Mode III [$t_2 \sim t_3$]: In this mode, the diode D_5 continues to conduct and D_2 becomes forward biased. Figure 4c shows the current flow path. V_{in} in series with the inductor L_1 provide energy to C_1 and the current of L_1 deceases. i_{Lk} charges the output capacitor C_o of the power switch, which results in an increase of v_{ds}. The energy stored in L_m is released to C_4 through N_s and D_5, and the current through D_5 decreases. The output capacitor C_o continuously releases energy to the load. This mode ends when D_3 is forward biased.

Mode IV [$t_3 \sim t_4$]: in this transition interval, the power switch S and the diodes D_1, D_4, and D_5 are off. V_{in} and L_1 provide energy to C_1 and the current of L_1 decreases. Figure 4d shows the corresponding equivalent circuit and current flow path. C_1, L_m, and L_k provide energy to C_3 through D_3, and the voltage stress of the switch is clamped to V_{C3}. At the same time, L_k and L_m together with the capacitors C_2 and C_4 provide energy to the output. Therefore, i_{Lk} and i_{Lm}

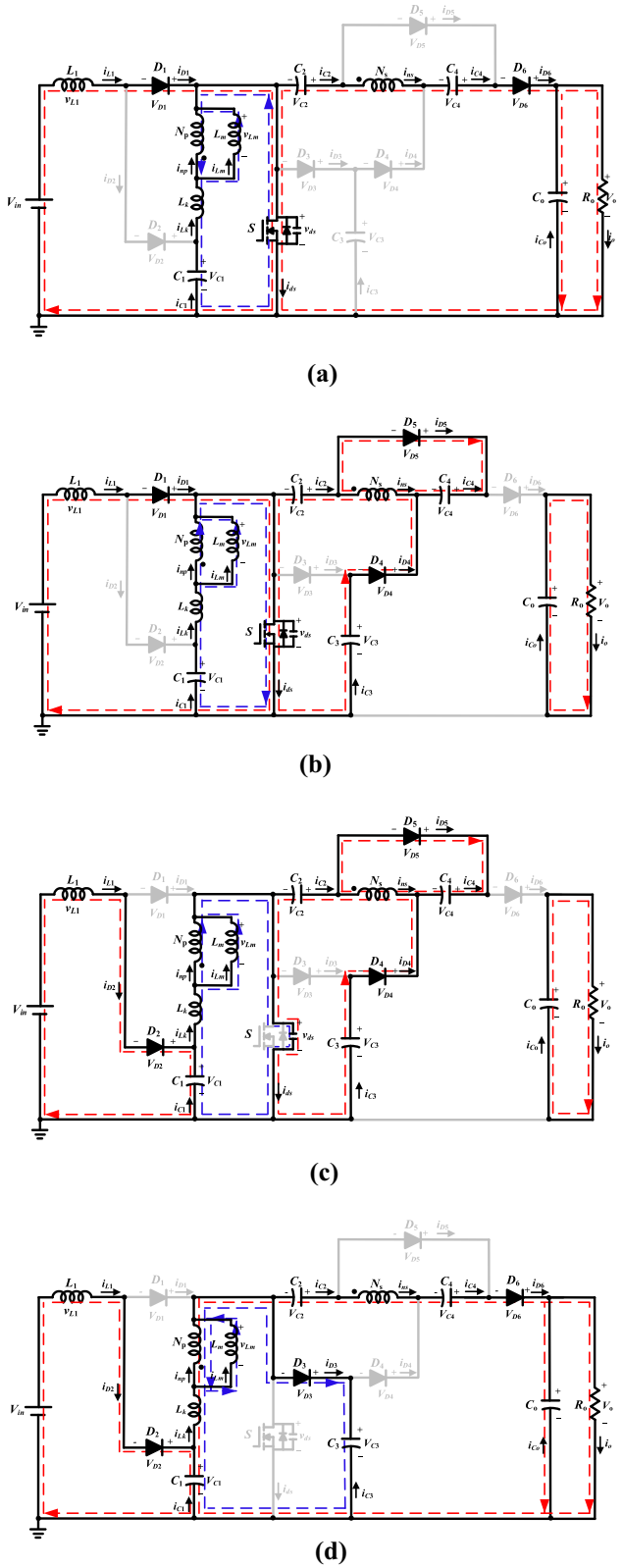

Fig. 4 Four operating modes of the proposed circuit: **a** Mode I, **b** Mode II, **c** Mode III, and **d** Mode IV

decrease and the current of D_6 rises. Afterwards, the operation modes repeat.

3 Steady-state characteristic analysis of the proposed converter

3.1 Voltage gain

For simplification of the steady-state analysis of the converter, there are only two modes, mode II and mode IV, under consideration.

As shown in Fig. 4b, during the $0 \sim DT_s$ period, in accordance with Kirchhoff's voltage law (KVL), the equations are deduced as

$$V_{in} = V_{L1} \tag{1}$$

$$V_{Lm} = V_{C1} \tag{2}$$

$$nV_{Lm} - V_{C2} + V_{C3} = 0 \tag{3}$$

$$nV_{Lm} = V_{C4} \tag{4}$$

During the period of $DT_s \sim T_s$ shown in Fig. 4d, the equations are formulated as

$$V_{L1} + V_{C1} = V_{in} \tag{5}$$

$$V_{Lm} = V_{C1} - V_{C3} \tag{6}$$

$$V_{Lm} + nV_{Lm} - V_{C2} - V_{C4} + V_o - V_{C1} = 0 \tag{7}$$

From ((1)) and ((5)), the following equation is derived using the volt-second balance principle on L_1:

$$\int_0^{DT_s} V_{in}dt + \int_{DT_s}^{T_s} (V_{in} - V_{C1})dt = 0 \tag{8}$$

The voltage across C_1 can be derived from ((8)) as

$$V_{C1} = \frac{1}{1-D} V_{in} \tag{9}$$

By utilizing the volt–second balance principle on L_m from ((2)) and ((6)), the following formula is derived as

$$\int_0^{DT_s} V_{C1}dt + \int_{DT_s}^{T_s} (V_{C1} - V_{C3})dt = 0 \tag{10}$$

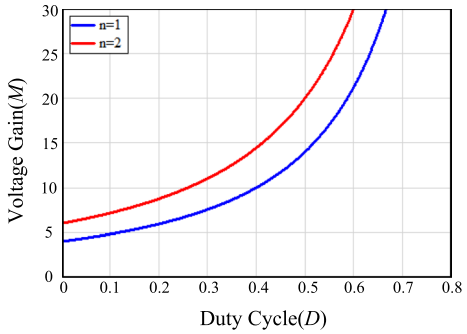

Fig. 5 Voltage gain versus duty cycle of the proposed converter for turn ratios of 1 and 2

The voltage across C_3 can be obtained from ((9)) and ((10)) as follows:

$$V_{C3} = \frac{1}{(1-D)^2} V_{in} \tag{11}$$

By substituting ((2)), ((9)), and ((11)) into ((3)), V_{C2} can be obtained:

$$V_{C2} = \frac{n - nD + 1}{(1-D)^2} V_{in} \tag{12}$$

From (4), the voltage of C_4 is derived as follows:

$$V_{C4} = \frac{n}{1-D} V_{in} \tag{13}$$

By substituting Eqs. (6), (9), (11), (12), and (13) into (7), the voltage gain M can be obtained as

$$M = \frac{V_o}{V_{in}} = \frac{2n + 2 - nD}{(1-D)^2} \tag{14}$$

Figure 5 shows curves of the voltage gain versus the duty cycle while considering the effect of the turns ratio n. The turns ratio is set as $n=1$ and $n=2$, and the duty cycle is set from 0 to 0.8, respectively. As can be seen, the presented converter can achieve a high voltage gain in the moderate duty cycle range. When the duty ratio is 0.5 and the turns ratio is $n=2$, the voltage gain can reach 20 times, avoiding the problems with operation at high duty cycles or a high turns ratio. Moreover, the proposed converter can work in a wide range of conversion ratios.

3.2 Voltage stress analysis

During $DT_s \sim T_s$, the voltage stress on the power switch is given by the following derivation:

$$V_{ds} = V_{C3} = \frac{1}{(1-D)^2} V_{in} = \frac{1}{2n + 2 - nD} V_o \tag{15}$$

From (15), it can be concluded that when the turns ratio n increase, the voltage stress on the switch decreases simultaneously.

From Fig. 4b and c, the voltage stresses of the diodes are derived as

$$V_{D1} = V_{C3} - V_{C1} = \frac{D}{(1-D)^2} V_{in} \tag{16}$$

$$V_{D2} = V_{C1} = \frac{1}{1-D} V_{in} \tag{17}$$

$$V_{D3} = V_{C3} = \frac{1}{(1-D)^2} V_{in} \tag{18}$$

$$V_{D4} = V_{D6} = V_o - V_{C4} - V_{C3} = \frac{n+1}{(1-D)^2} V_{in} \tag{19}$$

$$V_{D5} = V_o - V_{C3} - V_{C2} = \frac{n}{(1-D)^2} V_{in} \tag{20}$$

3.3 Current stress analysis

By utilizing the ampere–second balance principle and Kirchhoff's Current Law (KCL) on the capacitor C_1, C_2, C_3, and C_4, the average currents of the diodes and the switch S can be obtained as

$$I_{in} = I_{D1} + I_{D2} \tag{21}$$

$$I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{ns} = \frac{I_{np}}{n} = I_o \tag{22}$$

$$I_{ds} = I_{D1} + I_{D2} - I_{D3} \tag{23}$$

During the $DT_s \sim T_s$ period, based on KCL, the following equation can be derived:

$$i_{Lk} = i_{Lm} - i_{np} = i_{D3} + i_{D6} \tag{24}$$

By integrating (24) over the time period $DT_s \sim T_s$ as in (25), I_{Lm} can be calculated in (26) as follows:

$$\frac{1}{T} \int_{DT_s}^{T_s} \left(i_{Lm} - i_{np}\right) dt = \frac{1}{T} \int_{DT_s}^{T_s} \left(i_{D3} + i_{D6}\right) dt \tag{25}$$

$$I_{Lm} = \frac{(2+n) I_o}{1-D} \tag{26}$$

From Fig. 4b, it can be seen that the current ripple of L_m can be defined as

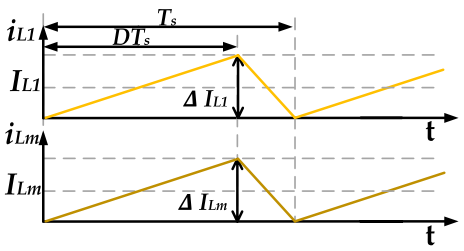

Fig. 6 Inductor current waveforms in the BCM

$$\Delta I_{Lm} = \frac{V_{in} D T_s}{(1-D) L_m} \tag{27}$$

The maximum and minimum currents through the inductor L_m can be obtained from (26) and (27) as

$$I_{Lm\max} = I_{Lm} + \Delta I_{Lm} = \frac{(2+n) I_o}{1-D} + \frac{V_{in} D T_S}{2(1-D) L_m} \tag{28}$$

$$I_{Lm\min} = I_{Lm} - \Delta I_{Lm} = \frac{(2+n) I_o}{1-D} - \frac{V_{in} D T_S}{2(1-D) L_m} \tag{29}$$

From Fig. 6, L_m can be deduced from (29) when the proposed converter operates in the boundary conduction mode (BCM):

$$I_{Lm\min} = 0 \Rightarrow L_m = \frac{V_{in} D T_s}{2(n+2) I_o} \tag{30}$$

According to (14) and the power balance principle, I_{L1} is obtained as

$$I_{L1} = \frac{V_o}{V_{in}} I_o = \frac{2n+2-nD}{(1-D)^2} I_o \tag{31}$$

From Fig. 4b, the current ripple of L_1 is written as

$$\Delta I_{L1} = \frac{V_{in}}{L_1} D T_s \tag{32}$$

From (31) and (32), the maximum and minimum currents through the inductor L_1 can be deduced from (31) and (32) as follows:

$$I_{L1\max} = I_{L1} + \Delta I_{L1} = \frac{2n+2-nD}{(1-D)^2} I_o + \frac{V_{in} D T_S}{2 L_1} \tag{33}$$

$$I_{L1\min} = I_{L1} - \Delta I_{L1} = \frac{2n+2-nD}{(1-D)^2} I_o - \frac{V_{in} D T_S}{2 L_1} \tag{34}$$

When the converter operates in the BCM as in Fig. 6, L_1 can be derived from (34):

$$I_{L1\min} = 0 \Rightarrow L_1 = \frac{V_{in} D (1-D)^2 T_s}{2(2n+2-nD) I_o} \tag{35}$$

By charge balance, the current stresses D_1–D_6 are obtained as follows:

$$I_{D1\max} = I_{D2\max} = I_{L1\max} \tag{36}$$

$$I_{D3\max} = I_{D6\max} = \frac{2 I_o}{1-D} \tag{37}$$

$$I_{D4\max} = I_{D5\max} = \frac{2 I_o}{D} \tag{38}$$

By substituting (21) and (22) into (23), the average current of S is equal to I_{in}-I_o, and the minimum current of S is equal to $I_{L1min}+I_{Lmmin}$. Thus, the following formulas can be written as

$$I_{ds} = I_{in} - I_o = \frac{\left(I_{ds\max} - I_{ds\min}\right) D T_s}{2 T_s} \tag{39}$$

$$I_{ds\min} = I_{L1\min} + I_{Lm\min} \tag{40}$$

From (29), (34), (39), and (40), the current stress of S can be achieved as

$$I_{ds\max} = \frac{(2-D) I_{in}}{D} - \frac{(2+nD) I_o}{D(2-D)} + \frac{\Delta I_{L1} + \Delta I_{Lm}}{2} \tag{41}$$

The formula to calculate the capacitor voltage ripple is as follows:

$$\Delta V_C = \frac{1}{C_1} I_C D T \tag{42}$$

Based on Fig. 4, (22), (24), and (42), the capacitance values for each of the capacitors in the converter are derived from the following inequalities. In addition, the capacitors need to withstand the corresponding rated voltages as described in (9), (11), (12), and (13):

$$C_1 \geq \frac{\left[\frac{2nI_o}{D} + \frac{(2+n)I_o}{(1-D)}\right] D T_s}{\Delta V_{C1}} \tag{43}$$

$$C_2 \geq \frac{I_o (1-D) T_s}{\Delta V_{C2}} \tag{44}$$

$$C_3 \geq \frac{I_o (1-D) T_s}{\Delta V_{C3}} \tag{45}$$

$$C_4 \geq \frac{I_o (1-D) T_s}{\Delta V_{C4}} \tag{46}$$

$$C_o \geq \frac{I_o D T_s}{\Delta V_{Co}} \tag{47}$$

3.4 Loss analysis

For the losses generated by the converter, they are divided into four parts as follows.

3.4.1 Switching loss

The loss of the power switch consists of switching loss and conduction loss. The switching loss of the switch is shown as follows:

$$P_{S\_Switchingloss} = \frac{1}{2} V_{ds} I_{ds} (t_{on} + t_{off}) f_s \tag{48}$$

where V_{ds} and I_{ds} are the average voltage and average current of the switch, respectively. Meanwhile, t_{on} and t_{off} are the turn-on and turn-off delay times of the power switch, respectively.

The conduction loss can be expressed as

$$P_{S\_Conductionloss} = (i_{dsrms})^2 r_{ds\_on} \tag{49}$$

where i_{dsrms} is the RMS value of i_{ds}, r_{ds_on} is the turn-on resistance of the switch, and R represents the resistance of the load.

Thus, the total switching loss can be obtained as

$$P_{S\_Loss} = P_{S\_Switchingloss} + P_{S\_Conductionloss} \tag{50}$$

3.4.2 Diode loss

The total loss of the six diodes is obtained as

$$P_{D\_Loss} = \sum_{n=1}^{6} (V_{Fn} \cdot I_{Dn} + i_{Dn\_rms}^2 \cdot r_{Dn\_on}) \tag{51}$$

where V_{Fn} is the forward-voltage of the diodes, while i_{Dn_rms} and r_{Dn_on} are the RMS value and the turn-on resistance of the diodes, respectively.

3.4.3 Capacitor loss

The total loss of the diode can be obtained as

$$P_{C\_Loss} = \sum_{n=1}^{5} (i_{Cn\_rms})^2 r_{Cn} \tag{52}$$

where i_{Cn_rms} and r_{Cn} are the RMS value of i_C and the resistance of the capacitors, respectively.

3.4.4 Inductor loss

The equations of the losses of the inductors are formulated as follows:

$$\begin{cases} P_{L1\_Loss} = i_{L1\_rms}^2 r_{L1} \\ P_{Lk\_Loss} = i_{Lk\_rms}^2 r_{Lk} \\ P_{Ls\_Loss} = i_{Ls\_rms}^2 r_{Ls} \end{cases} \tag{53}$$

where i_{L_rms} and r_L are, respectively, the RMS value of i_L and the resistance of the inductor.

The total loss of the inductors is expressed as

$$P_{L\_Loss} = P_{L1\_Loss} + P_{Lk\_Loss} + P_{Ls\_Loss} \tag{54}$$

3.4.5 Total loss

The total loss of the proposed converter can be concluded from (49) as follows:

$$P_{Loss} = P_{S\_Loss} + P_{D\_Loss} + P_{C\_Loss} + P_{L\_Loss} \tag{55}$$

Hence, the efficiency of the proposed converter is formulated as

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{56}$$

4 Performance comparison

In this part, to verify the superiority of the proposed converter, a comparison is made with a number of existing topologies that also use the quadratic boost technique and provide a high voltage gain. Equations of the voltage gains and the voltage stresses are shown in Table 1. Moreover, the number of components for each of the compared topologies are given. All the converters in Table 1 have a common ground between the load and the source.

Figures 7 and 8 present comparison results of the voltage gains and the voltage stresses, respectively. To ensure the fairness of the comparison, the turns ratios n of all the converters is defined as 2. The comparison results indicate that the proposed converter requires a lower duty cycle to achieve the same voltage gain when compared to the existing topologies. In the meantime, the voltage stress across

Table 1 Comparison of relevant converters with the proposed converter

Topology	S	L+CL	C	D	NC	Voltage stress of switch (V_{ds}/V_{in})	Voltage gain (M)	Input voltage (V)	Output voltage (V)	Maximum experimental voltage gain	The full load efficiency (%)
Proposed converter	1	1+1	5	6	14	$\frac{M}{2n+2-nD}$	$\frac{2n+2-nD}{(1-D)^2}$	20	400	20	93.7
[21]	2	2+0	4	4	12	S1: $\frac{(1-D)M}{4-4D+D^2}$	$\frac{4-4D+D^2}{(1-D)^2}$	24	200	8.3	90.0
						S2: $\frac{M}{4-4D+D^2}$					
[22]	1	3+0	4	4	12	$\frac{M}{1+D}$	$\frac{1+D}{(1-D)^2}$	10	100	10	90.0
[23]	1	2+0	5	7	16	$\frac{M}{2}$	$\frac{4}{(1-D)^2}$	24	150	6.25	85.33
[24]	1	1+1	3	5	11	$\frac{M}{1+nD}$	$\frac{1+nD}{(1-D)^2}$	20	400	20	89.3
[25]	1	1+1	4	6	13	$\frac{M}{1+nD}$	$\frac{1+nD}{(1-D)^2}$	48	400	8.3	92.2
[26]	1	1+1	3	5	11	$\frac{(1+n)(1-D)}{1+n-D}M$	$\frac{1+n-D}{(1-D)^2}$	36~48	300	8.3	92.6
[27]	1	1+1	5	6	14	$\frac{[2+D(n-1)]M}{n(3D+2)+2-D}$	$\frac{n(3D+2)+2-D}{2(1-D)^2}$	24	400	16.7	92.96
[28]	1	1+1	5	6	14	$\frac{M}{1+n+nD}$	$\frac{1+n+nD}{(1-D)^2}$	25	250	10	92.3
[29]	1	1+1	4	5	12	$\frac{M}{1+n}$	$\frac{1+n}{(1-D)^2}$	9~16	115	12.8	92.0
[30]	1	1+1	4	5	12	$\frac{M}{2+n}$	$\frac{2+n}{(1-D)^2}$	30	230	7.7	92.5

S Switch, *L* Inductor, *CL* Coupled inductor, *C* Capacitor, *D* Diode, *NC* Number of the used components

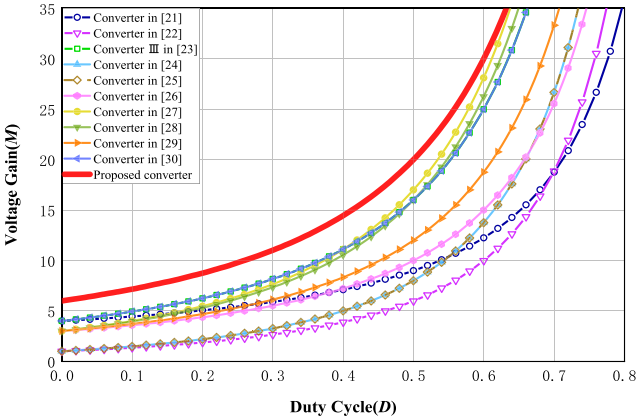

Fig. 7 Comparison of the voltage gain and duty cycle of the proposed converter with other quadratic converters under $n=2$

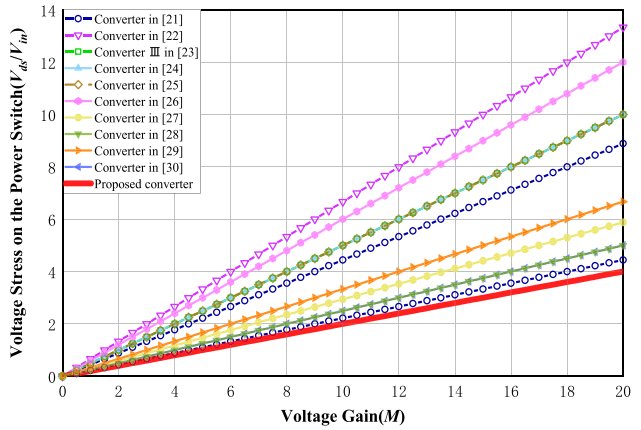

Fig. 8 Comparison of the voltage stress on the power switch between the proposed converter and other quadratic converters at different voltage gains under $n=2$ and $D=0.5$

the switch is lower than those of the converters in [21–30] in the cases of $n=2$ and $D=0.5$.

To further examine the performance of the proposed converter, the maximum experimental voltage gain of each converter is shown in Table 1. The proposed converter has a maximum experimental voltage gain that is higher than the other converters except [24], which can reach up to 20 times. The proposed converter has significant improvements in terms of a high gain, low switching stress, and high efficiency at a low duty cycle when compared to other quadratic converters with the same number of components in Table 1. Although the switch S_1 of the converter in [21] is close to the switch of the proposed converter regarding voltage stress, it is noteworthy that [21] employs two switches, which results in an increased cost. At the same time, it does not have an

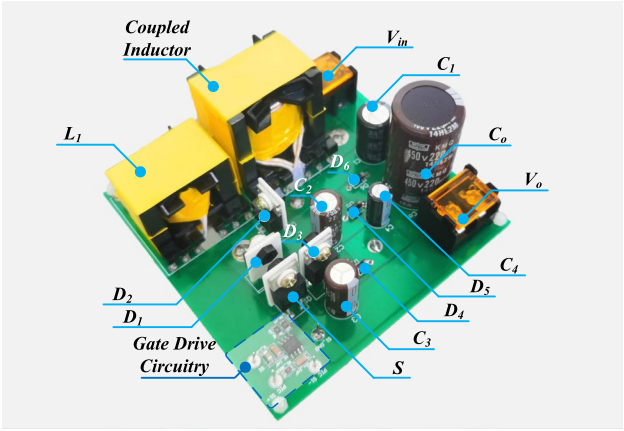

Fig. 9 Experimental prototype of the proposed converter

advantage in terms of gain since it does not utilize a coupled inductor.

5 Experimental tests

To verify the analysis results, a prototype model is implemented and tested. The selected component parameters and system specification are summarized in Table 2, and the experimental prototype is shown in Fig. 9.

By setting the boundary conditions at $V_{in}=20$ V, $V_o=400$ V, and $I_o=0.2$ A, and the turns ratio under $n=1$, the magnetizing inductors L_1 and L_m can be obtained from (14), (30), and (35) as

$$L_1 = \frac{V_{in}D(1-D)^2T_s}{2(2n+2-nD)I_o} = 29.35\mu H$$

$$L_m = \frac{V_{in}DT_s}{2(n+2)I_o} = 195.8\mu H$$

L_1 is designed as 29 µH, and L_m is designed as 196 µH.

5.1 Experimental results

Experimental waveforms are shown in Figs. 10, 11, 12, 13, 14, and 15 under the rated conditions. Figure 10 shows the driver signal v_{gs}, the voltage v_{ds} across the switch, the current of the inductor L_1, and the current i_{D1}. It can be seen that the voltage across the switch is 117 V, which verify the effectiveness of the clamp circuit. Therefore, a low power rating switch can be employed in the proposed converter. The current flowing through L_1 is continuous. i_{L1} increases when the switch is turned on, and decreases

Table 2 Experimental parameters and system specifications

Parameters	Values
Input voltage, V_{in}	20 V
Output voltage, V_o	400 V
Rated output power, P_o	200 W
Switch frequency, f_s	50 kHz
Power switch, S	220N25NF
Inductor, L_1	29 µH (Core-PQ3225)
Coupled inductor (L_m, L_k)	$L_m=196$ µH, $L_k=3$ µH (Core-PQ3535)
Turns ratio of the coupled inductor (N_p: N_s)	14:14
Capacitors C_1, C_o	220 µF
Capacitors C_2, C_3	22 µF
Capacitors C_4	47 µF
Diodes D_1, D_2	MBR20100CT
Diode D_3	MBR20300CT
Diodes D_4, D_5, D_6	MUR160

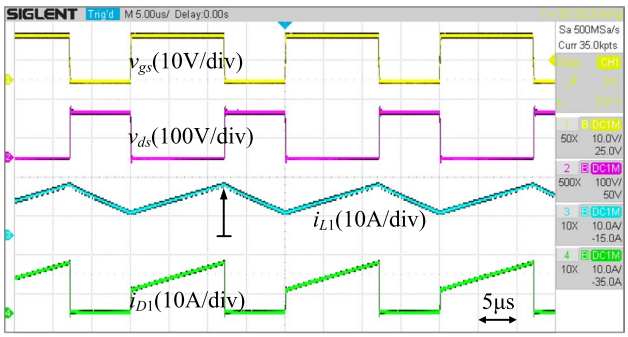

Fig. 10 Waveforms of v_{gs}, v_{ds}, i_{L1}, and i_{D1} under the full load

when the switch is turned off. In addition, from Figs. 10 and 14, all the currents of the diodes and the voltages across the diodes are in agreement with the theoretical analysis. As shown in Figs. 14 and 15, the voltages of the experimental results for the capacitors C_1, C_2, C_3, and C_4 are about 48, 162, 117, and 46 V, respectively. The capacitors provide the expected voltages. In addition, the experimental waveforms are in accordance with the theoretical analysis.

5.2 Measured efficiency

Figure 16 shows efficiency curves of the proposed converter under load conditions of 20–200 W. The maximum efficiency is about 95.2% under the 80 W load condition. The efficiency under the full load is 93.7%. Figure 17 depicts the conversion efficiency at the full load and its loss distribution. It can be observed that the diode losses account for 42% of the total losses. Meanwhile, the switch losses have the lowest

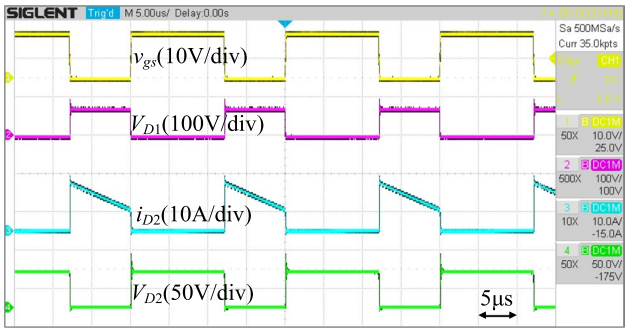

Fig. 11 Waveforms of v_{gs}, V_{D1}, i_{D2}, and V_{D2} under the full load

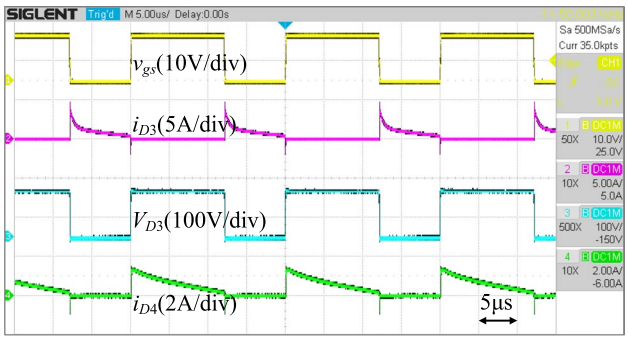

Fig. 12 Waveforms of v_{gs}, i_{D3}, V_{D3}, and i_{D4} under the full load

percentage of 15%. The "else" represents the losses that are not included in the loss analysis.

5.3 Closed-loop experimental result

The procedure of the closed-loop control is exhibited in Fig. 18. The TMS320F28335 digital signal processor generates PWM commands that are applied to the power switch using a SI8220 MOSFET driver. To control the output voltage, a proportional-integral (PI) controller is used to compare the actual output voltage value with the given value

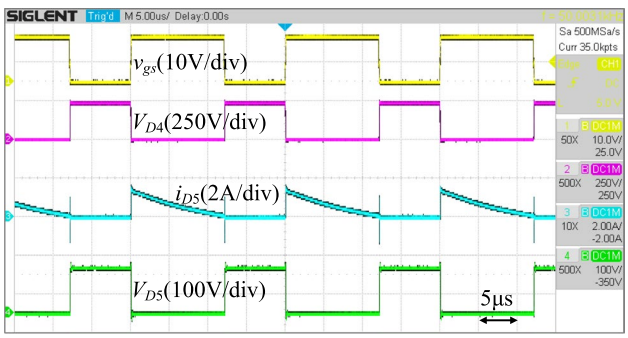

Fig. 13 Waveforms of v_{gs}, V_{D4}, i_{D5}, and V_{D5} under the full load

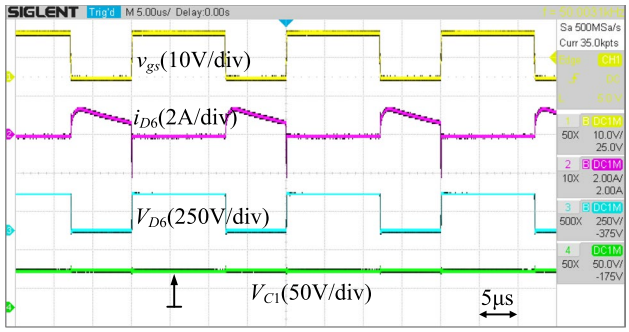

Fig. 14 Waveforms of v_{gs}, i_{D6}, V_{D6}, and V_{C1} under the full load

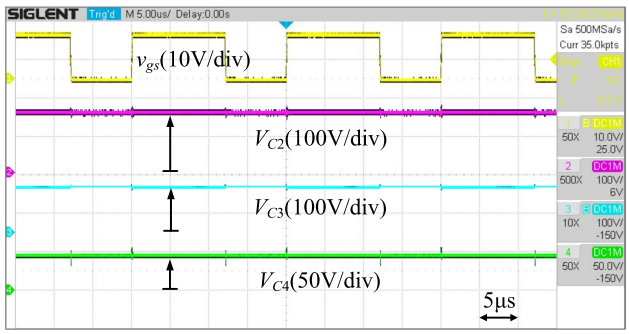

Fig. 15 Waveforms of v_{gs}, V_{C2}, V_{C3}, and V_{C4} under the full load

V_{o_ref}. When there is a difference between V_o and V_{o_ref}, the result of the comparison is applied to the PI controller to regenerate a proper duty cycle. Figure 19 shows closed-loop experimental results of the proposed converter from 50% load and full load conditions. It is obvious that the proposed converter maintains a relatively stable output voltage from a 50% load to a full load and then back to a 50% load, which demonstrates the dynamic response performance of the proposed converter.

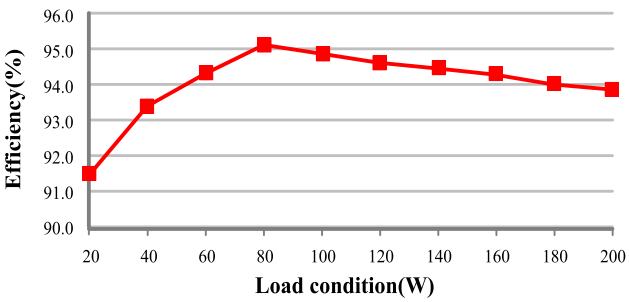

Fig. 16 Efficiency curves of the proposed converter

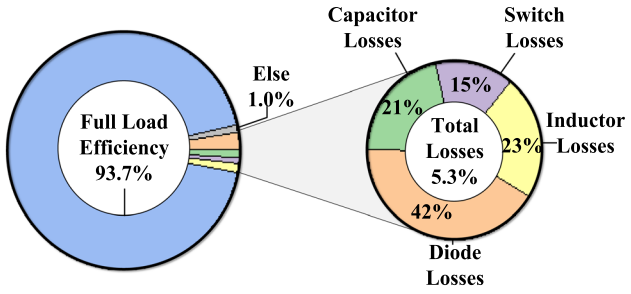

Fig. 17 Pie chart of the full-load efficiency and its total loss distribution

6 Improved topology

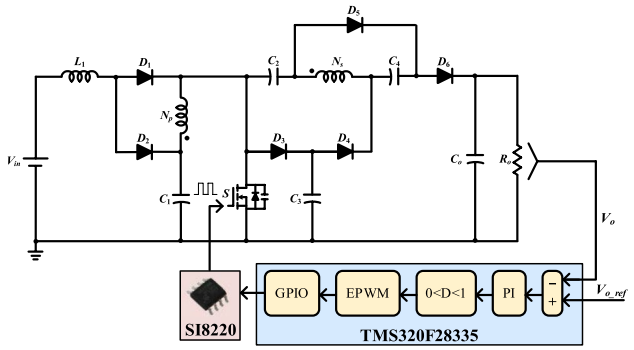

Fig. 18 Control diagram of the testing procedure

To obtain a higher voltage gain, a three winding technique and a voltage multiplier are inserted into the proposed topology. The structure of the improved topology is shown in Fig. 20. The three output capacitors C_{o1}, C_{o2}, and C_{o3} are in series to further boost the output voltage. N_p, N_{s1}, and N_{s2} are the primary, secondary, and tertiary windings of the transformer, respectively. In addition, the turns ratio of the improved topology n_p:n_{s1}:n_{s2} is defined as 1:n_1:n_2.

By analyzing the operating rules of the improved topology in the case of the CCM, its voltage gain is concluded as follows:

$$M = \frac{V_o}{V_{in}} = \frac{2n_1 + n_2 + 2 - n_1 D}{(1-D)^2} \tag{57}$$

When compared to the original circuit, a new gain factor n_2 was added to the numerator of the improved topology. Meanwhile, the adjustability of the upgraded circuit is improved due to the utilize of the three winding technique.

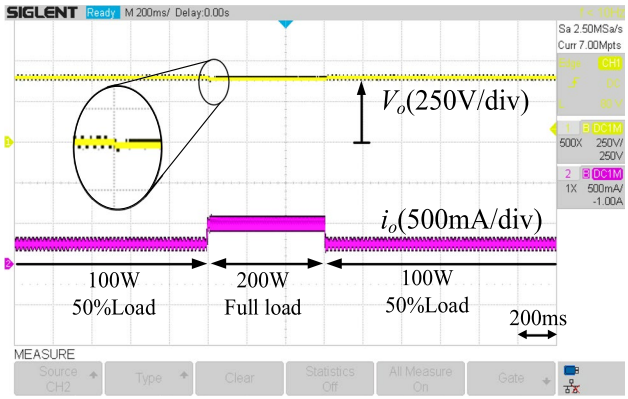

Fig. 19 Closed-loop experimental result at 50% load to the full load and back to 50% load

Moreover, when the improved circuit operates at $D = 0.59$, n_p: n_{s1}: n_{s2} = 1:1:1, the voltage gain can reach 28 times the input voltage.

7 Conclusion

By combining a quadratic boost converter with a coupled inductor and the voltage multiplier technique, this paper presents a high boost converter with a continuous input that can be utilized by renewable energy applications. Due to the design of the clamp circuit, the voltage stress on the power switch is clamped and the energy of the leakage inductance is reused. Therefore, switching elements with lower on-resistances can be used. To verify its performance, the converter is compared with relevant converters in terms of different criteria. As shown in the comparison results, the proposed converter presents a higher voltage gain and a lower voltage stress. A prototype of 200 W was implemented with a 20 V input and a 400 V output voltage. The highest efficiency is 95.2%, and the full-load efficiency is approximately 93.7%. Experimental results confirm the feasibility of the theoretical analysis and the proposed configuration. Finally, an extended topology based on the proposed converter was addressed and shown to exhibit the expandability of the circuit.

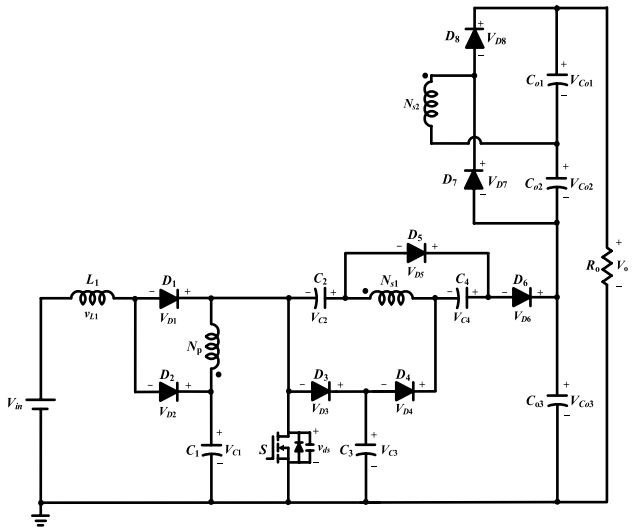

Fig. 20 Structure of the improved topology

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Data availability The data that support the findings of this study are available on request from the corresponding author.

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Fuwei Li was born in Guangdong, China, in 2000. He is presently working towards his B.S. degree at Guangdong Ocean University, Zhanjiang, China. His current research interests include power electronics, high step-up DC–DC converters, and renewable energy systems.

Jie He was born in Guangdong, China, in 2001. She is presently working towards her B.S. degree at Guangdong Ocean University, Zhanjiang, China. Her current research interests include power electronics and renewable energy systems.

Peng Luo received his B.S. degree from the Henan Polytechnic University, Jiaozuo, China, in 2012; and his M.S. degree from the China University of Mining and Technology, Xuzhou, China, in 2015. He worked as an Assistant Electrical Engineer at the China Nuclear Power Simulation Technology Co., Ltd., Shenzhen, China. Since 2016, he has been a Lecturer at Guangdong Ocean University, Zhanjiang, China. His current research interests include power electronics converters and energy conversion.

Haoyu Jiang received his B.S. degree from the College of Energy Engineering, Zhejiang University, Hangzhou, China, in 2011; and his Ph.D. degree from the State Key Laboratory of Clean Energy Utilization, Zhejiang University, Hangzhou, China, in 2017. He is presently working as an Associate Professor in the School of Electronics and Information Engineering, Guangdong Ocean University, Zhanjiang, China; and as the Director of Industrial Internet Co., Ltd., Hangzhou, China. He is also the Deputy Secretary-General of the Cognitive System and Information Processing Committee of the China Artificial Intelligence Society, and a Committee Member of the Chinese Society of Automation. Since 2017, he has been working in the Provincial Key Enterprise Research Institute of Cloud-Energy Internet, Hangzhou Zhongheng Electric Co., Ltd., Hangzhou, China; and as a Post-Doctoral Fellow in the School of Automation, Southeast University, Nanjing, China. His current research interests include the optimization of data quality characteristic curve prediction method state estimations, failure mode diagnosis, and renewable energy conversion.

Mingxin Liu received his B.S. degree in Communication Engineering; and his M.S. and Ph.D. degrees in Circuits and Systems from Yanshan University, Qinhuangdao, China, in 1999, 2003, and 2006, respectively. He is presently working as a Professor in the College of Electronics and Information Engineering, Guangdong Ocean University, Zhanjiang, China. His current research interests include the performance analysis of wireless sensor networks and underwater acoustic communication networks.