A Single Switch Quadratic Step-up DC-DC Converter Based on Three-winding Coupled Inductor and Switch-capacitor

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***Abstract*—A transformerless high step-up dc-dc converter for fuel cell (FC) systems is proposed in this paper. The configuration of the proposed converter is a quadratic boost converter with the three-winding coupled inductor. The output voltage of three capacitors is applied to generate energy for the load. Thus, high step-up voltage gain can be achieved with a small duty ratio. Moreover, due to the leakage inductance energy is recycled, the efficiency is improved and the voltage stress of the power switch is clamped. Finally, a simulation experiment with input voltage of 24V, output voltage of 400V, and wattage rating of 200W is implemented to verify the performance.**

Keywords—High voltage gain; three-winding coupled inductor; DC-DC converter; switched capacitor; quadratic boost

I. INTRODUCTION

Renewable energy resources are widely used due to energy resource diversity and environmental concerns [1]. Commonly, the produced voltage of renewable energy like fuel cells, solar power and wind turbines is low [2]. Therefore, high step-up converters are essential for providing power for the subsequent voltage inverter and meeting the requirement of the power gird [3]. One of the techniques to obtain a high voltage ratio is to employ the coupled inductor. Due to adjustable property of coupled inductor, the voltage gain enhances conspicuously. However, the existence of leakage inductance occurs a voltage spike on the switch, lower the conversion efficiency [4]. To improve the effect of voltage spike, active-clamped circuit is applied. However, the control may be complex. By using the voltage-lift method, switched inductor technique or switched capacitor technique can achieve high voltage gain. However, extra components are needed to further increase the voltage gain.

This paper presents a high efficiency, high step-up voltage gain converter, with reduction of the voltage stress of the switch and no requirement of high duty ratio. It integrates the technique of switched-capacitor, coupled-inductor and multiplier capacitor. The structure of the proposed non-isolated DC-DC topology is shown in Fig.1. The proposed converter consists of magnetizing inductance L_1, L_m, leakage inductance L_k, one switch, six capacitors, seven diodes. A boost converter is applied to generate a stable voltage V_{C1} and supply the energy for V_{C2} when the switch is off. V_{C2} and the secondary side of coupled inductor generate voltage for V_{C3}. The energy of V_{C2} and V_{C3} are pulsed by the cascade technique to obtain a higher voltage for V_{Co3}. The output voltage V_o is the sum of V_{Co1}, V_{Co2} and V_{Co3}. Moreover, the switch has a low conducting resistance $r_{ds_}$on. Thus, the proposed converter is able to obtain high efficiency.

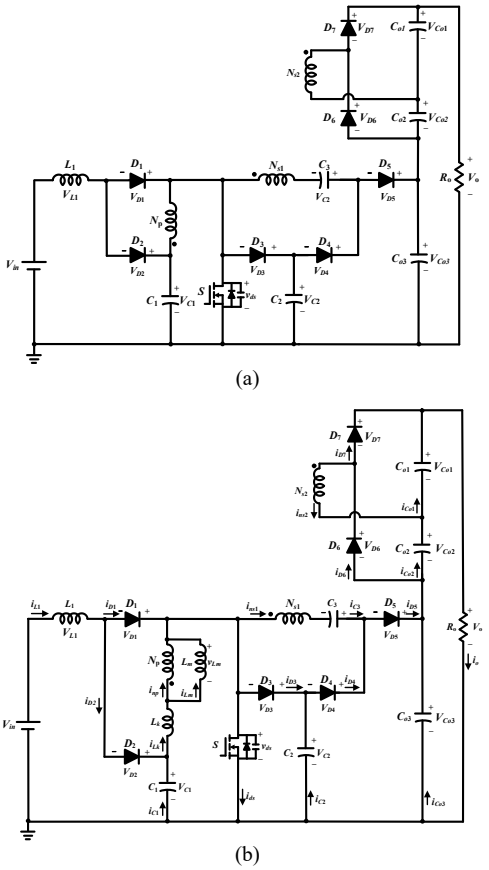

Fig. 1. The structure of the circuit topology. (a) Original circuit; (b) Equivalent circuit.

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II. Operation Of The Proposed Converter

To simply analyze the circuit, the circuit works in the following assumptions:

(1) All components are regarded as ideal.

(2) The proposed converter is operated in continuous current mode (CCM).

(3) Capacitors C_1, C_2, C_3, C_{o1}, C_{o2} and C_{o3} are large enough. Thus, the output voltage of those capacitors can be considered as constant.

(4) The turns ratio of the coupled inductor $N_p : N_{s1} : N_{s2}$ is $n_1 : n_2 : n_3$.

The proposed converter operating in CCM is analyzed as follow:

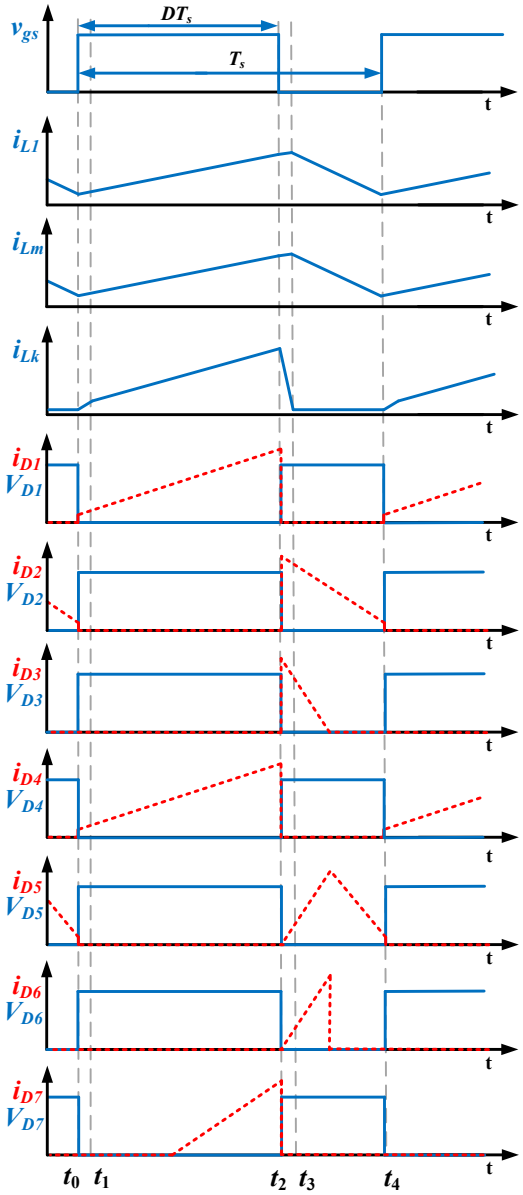


Fig. 2. The key waveforms of the proposed converter in CCM.

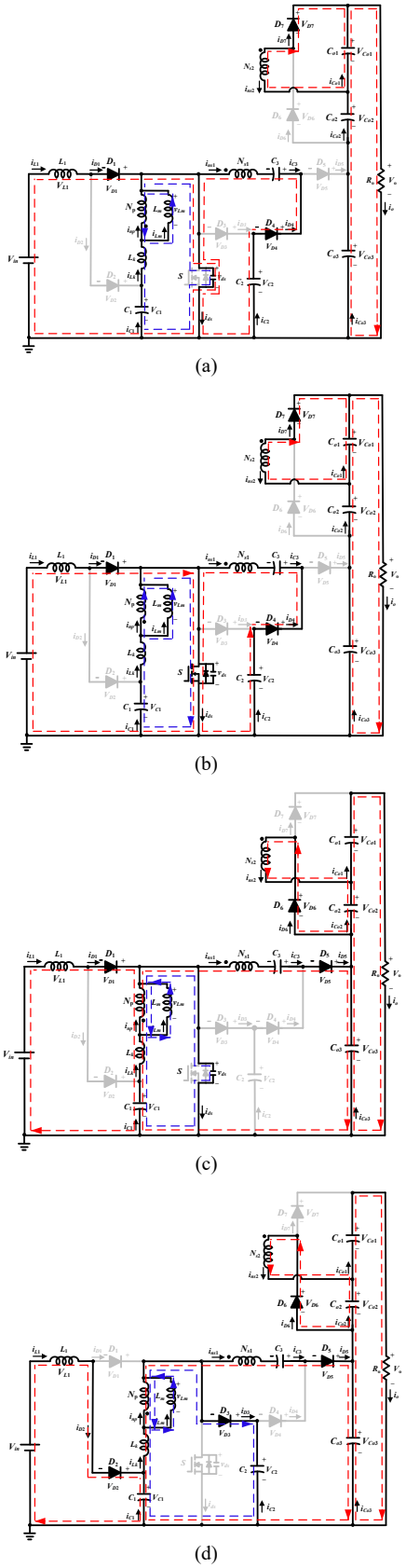


Fig. 3. Operating principles (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV

Mode I [t_0~t_1] [in Fig.3(a)]: v_{gs} becomes high at t=t_0. Diodes D_1, D_4, and D_7 are on, D_2, D_3, D_5, and D_6 are reverse biased. V_{in}, L_1, L_m, C_2, C_{o1} and C_{o3} provide energy to the load. i_{L1}, i_{Lk}, i_{Lm} increase at the same time.

Mode II [t_1~t_2] [in Fig.3(b)]: V_{in} releases energy to L_1. Diodes D_1, D_4, and D_7 are on, D_2, D_3, D_5, and D_6 are reverse biased. The secondary side of coupled inductor N_{s1} and N_{s2} charge the capacitor C_3 and C_{o1} respectively. i_{L1}, i_{Lm} and i_{Lk} increase. This mode ends when v_{gs} becomes low at t=t_2.

Mode III [t_2~t_3] [in Fig.3(c)]: v_{gs} becomes low at t=t_2. Diodes D_1, D_5 and D_6 are on, D_2, D_3, D_4, and D_7 are reverse biased. V_{ds} is clamped by C_1. i_{Lm} and i_{Lk} are reduced in this mode. This mode ends when v_{ds} is equal to V_{C1} at t=t_3.

Mode IV [t_3~t_4] [in Fig.3(d)]: Diodes D_2, D_3, D_5, and D_6 are on, D_1, D_4 and D_7 are off by reverse voltage. V_{in}, L_1, L_m, C_3, C_{o1}, and C_{o3} provide energy to the load. This mode ends when the drive signal of S becomes high.

III. Steady-State Characteristic Analysis of the Proposed Converters

A. The Voltage Gain

From Fig.2 (b), during the (t_1~t_2) period, the power switch is on, the equation can be obtained:

$$V_{in} = V_{L1} \tag{1}$$

$$V_{Lm} = V_{C1} \tag{2}$$

$$n_1 V_{Lm} - V_{C2} + V_{C3} = 0 \tag{3}$$

$$V_{Co1} + V_{Co2} + V_{Co3} = V_o \tag{4}$$

From Fig.2 (d), during the (t_3~t_4) period, the power switch is off; the equation can be obtained:

$$V_{L1} + V_{C1} = V_{in} \tag{5}$$

$$V_{Lm} = V_{C1} - V_{C2} \tag{6}$$

$$V_{Lm} + n_2 V_{Lm} - V_{C3} + V_{Co3} - V_{C1} = 0 \tag{7}$$

By using the volt-second balance principle on L_1, the equation can be derived from (1) and (5)

$$\int_0^{DT_s} V_{in}\,dt + \int_{DT_s}^{T_s} (V_{in} - V_{C1})\,dt = 0 \tag{8}$$

The voltage across C_1 can be written by (8) as

$$V_{C1} = \frac{1}{1-D} V_{in} \tag{9}$$

By using the volt-second balance principle on L_m, the equation can be derived from (2) and (6):

$$\int_0^{DT_s} V_{C1}\,dt + \int_{DT_s}^{T_s} (V_{C1} - V_{C2})\,dt = 0 \tag{10}$$

The voltage across C_2 and C_3 can be obtained as

$$V_{C2} = \frac{1}{(1-D)^2} V_{in} \tag{11}$$

$$V_{C3} = \frac{n_2 - n_2 D + 1}{(1-D)^2} V_{in} \tag{12}$$

The voltage across C_{o1}, C_{o2}, and C_{o3} can be obtained as

$$V_{Co1} = \frac{n_3}{1-D} V_{in} \tag{13}$$

$$V_{Co2} = \frac{D n_3}{(1-D)^2} V_{in} \tag{14}$$

$$V_{Co3} = \frac{2 + n_2}{(1-D)^2} V_{in} \tag{15}$$

The voltage gain in CCM can be derived as follow:

$$M = \frac{V_o}{V_{in}} = \frac{n_2 + n_3 + 2}{(1-D)^2} \tag{16}$$

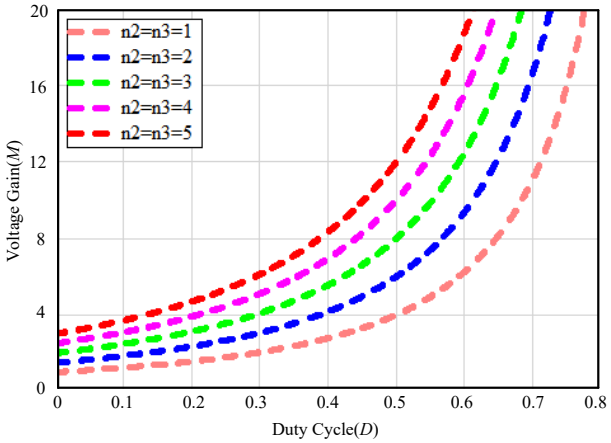


Fig. 4. Voltage gain versus duty cycle of the proposed converter.

B. Voltage Stress Analysis

According to the operation principle of the proposed converter, the voltage stresses on the diodes and switch can be presented as:

$$V_{D1} = V_{C2} - V_{C1} = \frac{D}{(1-D)^2} V_{in} \tag{17}$$

$$V_{D2} = V_{C1} = \frac{1}{1-D} V_{in} \tag{18}$$

$$V_{D4} = V_{D5} = V_{Co3} - V_{C2} = \frac{1 + n_2}{(1-D)^2} V_{in} \tag{19}$$

$$V_{D6} = V_{D7} = V_{Co1} + V_{Co2} = \frac{n_3}{(1-D)^2} V_{in} \tag{20}$$

$$V_{ds} = V_{D3} = V_{C2} = \frac{1}{(1-D)^2} V_{in} \tag{21}$$

C. Current Stress Analysis

According to Kirchhoff's current law (KCL) and the ampere-second balance principle on capacitor C_2, C_3 and C_4, C_{o1}, C_{o2}, C_{o3} the average currents of the diodes can be obtained:

$$I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_o \tag{22}$$

During (t_3~t_4) period, the following equations are derived as

$$I_{Lk} = I_{D3} + I_{D5} \tag{23}$$

$$I_{Lk} = I_{Lm} - I_{np} \tag{24}$$

From Fig.2(d), during the (t_3~t_4) period, we have:

$$i_{ns} = i_{D5} \tag{25}$$

The current ripple of L_m is obtained as

$$\Delta I_{Lm} = \frac{V_{C1}}{L_m} DT_s \tag{26}$$

From (22)-(25), the current across L_m can be obtained:

$$I_{Lm} = \frac{(n_2+2)I_o}{1-D} \tag{27}$$

When the converter operates in the Boundary Conduction Mode (BCM), L_m can be derived from (26) and (27):

$$L_m = \frac{V_{in} DT_s}{2(n_2+2)I_o} \tag{28}$$

From (16) and the power balance principle, I_{L1} is obtained as

$$I_{L1} = \frac{V_o}{V_{in}} I_o = \frac{n_2+n_3+2}{(1-D)^2} I_o \tag{29}$$

The current ripple of L_1 is obtained as

$$\Delta I_{L1} = \frac{V_{in}}{L_1} DT_s \tag{30}$$

When the converter operates in the BCM, L_1 can be derived from (29) and (30):

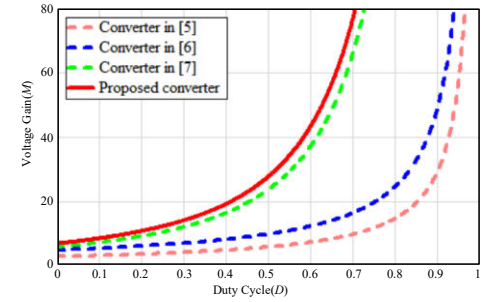
$$L_1 = \frac{V_{in} D(1-D)^2 T_s}{(2n_2+2n_3+4)I_o} \tag{31}$$

D. Performance Comparisons

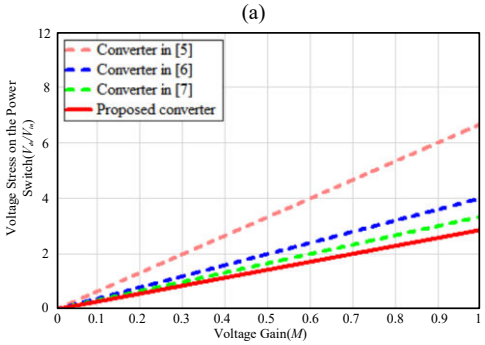
To verify the superiority of the proposed circuit in terms of gain and voltage stress, several references are provided in this section.

TABLE I. CONTRAST THE PROPOSED CONVERTER WITH RELEVANT CONVERTERS

Topology	[5]	[6]	[7]	Proposed converter
No. of Switches	1	1	1	1
No. of Diodes	3	4	5	7
Voltage Gain(M)	$\frac{2+n_1}{1-D}$	$\frac{1+2n_3-n_2}{(n_3-n_2)(1-D)}$	$\frac{2n_2+n_3-1}{(n_2-1)(1-D)^2}$	$\frac{2+n_2+n_3}{(1-D)^2}$
Voltage Stress of Switch (V_{ds}/V_{in})	$\frac{M}{2+n_1}$	$\frac{(n_3-n_2)M}{1+2n_3-n_2}$	$\frac{(n_2-1)M}{2n_2+n_3-1}$	$\frac{M}{2+n_2+n_3}$
Common Ground	Yes	Yes	Yes	Yes



(a)



(b)

Fig. 5. (a) Voltage gain of several converters for different duty ratios(b) The relationship between voltage stress on the power switch and the voltage gain in different converters. (for n_1=1, n_2=2 and n_3=3)

IV. VERIFICATION ON SIMPLIS

In order to verify the analysis results, the proposed circuit is verified on SIMPLIS and the following table shows the selected component parameters.

TABLE II. EXPERIMENTAL PARAMETERS

Parameter	Value
Input voltage, V_{in}	24V
Output voltage, V_o	400V
Switch frequency, f_s	50kHz
Maximum output power, P_o	200W
Magnetizing inductance of L	36.7μH
Magnetizing inductance of L_m	204μH
Magnetizing inductance of L_k	3μH
Capacitors C_1	150μH
Capacitors C_2 and C_3	47μH
Output capacitor of C_{o1}, C_{o2} and C_{o3}	220μH
Turns Ratio (n_1 : n_2 : n_3)	1:1:1

From Fig.6, the output voltage is close to the analysis value. The current and voltage of S are shown in Fig.7, and the presented waveforms of i_{Lm} is match the theoretical values of the currents through L_m. The maximum current of S is 20A and the maximum voltage of S is 100V, which are close to the theoretical values. The voltage and current of the seven diodes are shown respectively in Fig.8 and Fig.9, which are similar to the theoretical values. Fig.10 shows the voltage of C_1, C_2, C_3, C_{o1}, C_{o2}, and C_{o3}, which are also similar to the theoretical values.

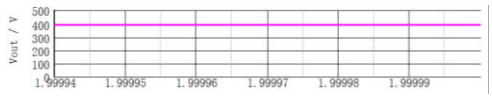


Fig. 6. The waveforms of V_o at P_o=200W.

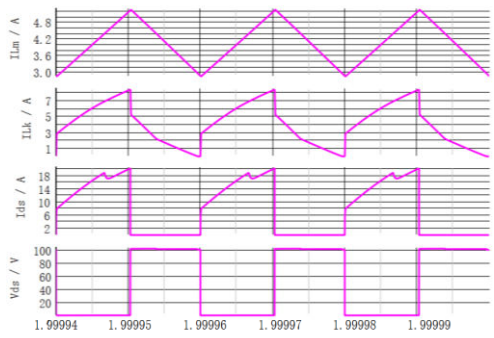


Fig. 7. The waveforms of i_{Lm}, i_{Lk}, i_{ds}, and V_{ds} at P_o=200W.

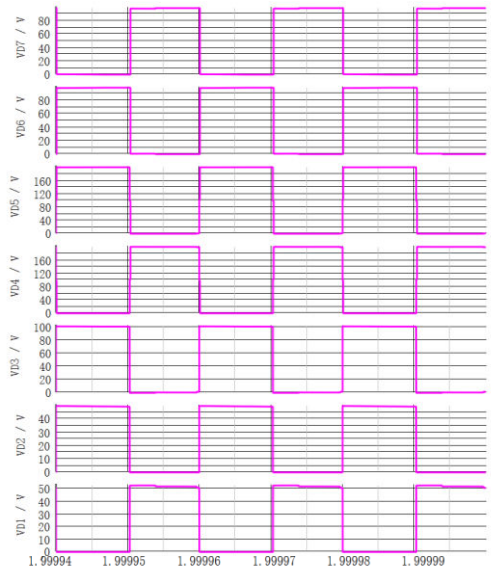


Fig. 8. The waveforms of V_{D1}, V_{D2}, V_{D3}, V_{D4}, V_{D5}, V_{D6}, and V_{D7} at P_o=200W.

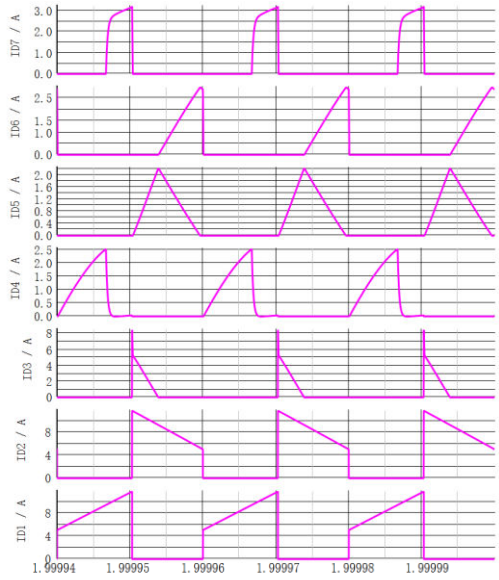


Fig. 9. The waveforms of i_{D1}, i_{D2}, i_{D3}, i_{D4}, i_{D5}, i_{D6}, and i_{D7} at P_o=200W.

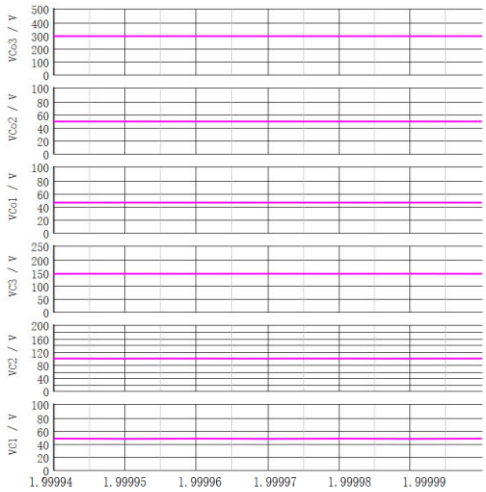


Fig. 10. The waveforms of V_{C1}, V_{C2}, V_{C3}, V_{Co1}, V_{Co2}, and V_{Co3} at P_o=200W.

V. Conclusion

The proposed high step-up DC-DC converter contains a quadratic boost converter and three-winding coupled inductor techniques. It eliminated the voltage spike of the switch and recycled the leakage current without using any extra circuit. In the end, a converter with voltage ratio of 24/400V and wattage rating of 200W has been simulated in SIMPLIS. The simulation results confirmed the viability of the theoretical analyses and presented configuration.

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