Academy of Innovative Semiconductor and Sustainable Manufacturing

ANALOG INTEGRATED CIRCUIT DESIGN AND LAYOUT LAB

MOSFET CHARACTERISTIC CURVE

Student: Pham Lo Hoang Khang

Student ID: XZ4138222

Group: B1

LAB2-1-4. INVERTER TRANSIENT WAVEFORM

Parameter:

.subckt INV in out vdd gnd

MM1 in out vdd vdd P_18 W=6.8u L=0.18u m=2

MM2 in out gnd gnd N_18 W=2u L=0.18u m=2

.ends

LAB2_1_4.sp × INV.cir

```
subckt   xinv1        xinv1
element    1:m1         1:m2
model      0:p_18.1     0:n_18.1
region   Linear       Cutoff
 id       -44.541217p   37.341165p
 ibs      6.47085e-27 -1.26652e-26
 ibd      7.40756e-24   -1.070830f
 vgs       -1.800000     0.
 vds       -7.804781n    1.800000
 vbs        0.           0.
 vth     -528.450300m  463.164469m
 vdsat   -927.415768m   53.208422m
 vod       -1.271550  -463.164469m
 beta       6.712453m    7.931224m
 gam eff  557.084657m  507.445914m
 gm        18.715164p    1.225275n
 gds        5.716894m   28.095903p
 gmb        9.952535p  182.035537p
 cdtot     40.974837f    4.787874f
 cgtot     30.478874f    4.560853f
 cstot     39.615562f    6.519503f
 cbtot     33.954846f    9.655385f
 cgs       15.448926f    1.553244f
 cgd       14.881572f    1.553200f


******
* testbench for mos characteristic *

****** transient analysis tnom=  25.000 temp=  27.000 ******
vmax=   1.839554     at=  10.033833n
            from=   0.            to= 100.000000n
vmin= -19.702757m    at=  40.131790n
            from=   0.            to= 100.000000n
trise=  94.722757p  targ=  40.263272n   trig=  40.168550n
tfall=  94.210498p  targ=  30.169511n   trig=  30.075301n
trise_tfall_diff_%= 542.264698m
tplh=  55.191856p  targ=  20.205192n   trig=  20.150000n
tphl=  68.767887p  targ=  30.118768n   trig=  30.050000n
```

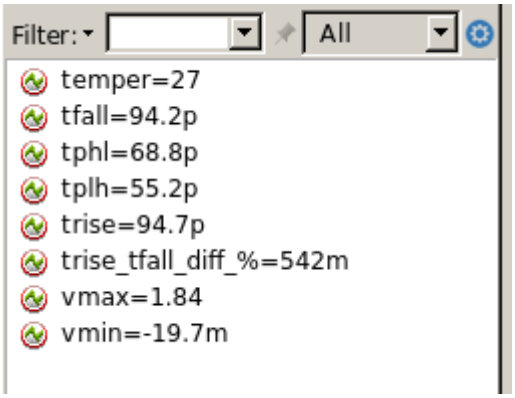
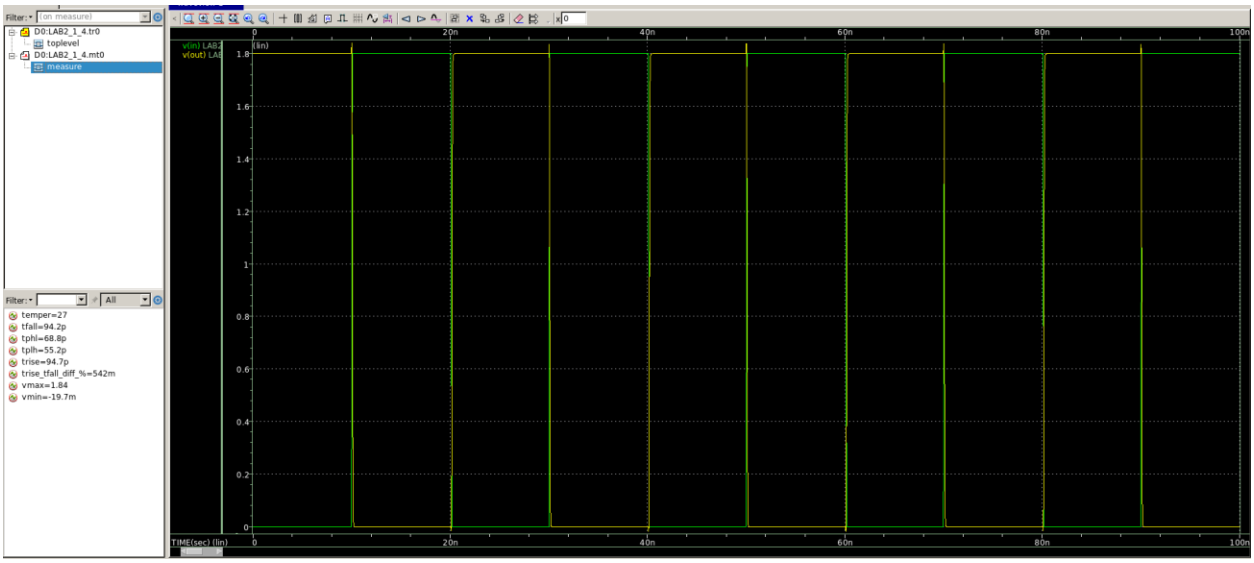


Figure 1. Spec



Comment:

- *Fall Time (tfall): 94.2 ps*

* Increase tfall by:

- Decreasing the W/L ratio of the NMOS transistor. This reduces its drive strength, slowing down the discharge rate of the output capacitance.

- *Rise Time (trise): 94.7 ps*

* Increase trise by:

- Decreasing the W/L ratio of the PMOS transistor. This reduces its drive strength, slowing down the charge rate of the output capacitance.

- *High-to-Low Propagation Delay (tphl): 68.8 ps*

* Time for the output to switch from high to low after the input changes. Influenced by the NMOS transistor's drive strength and load conditions.

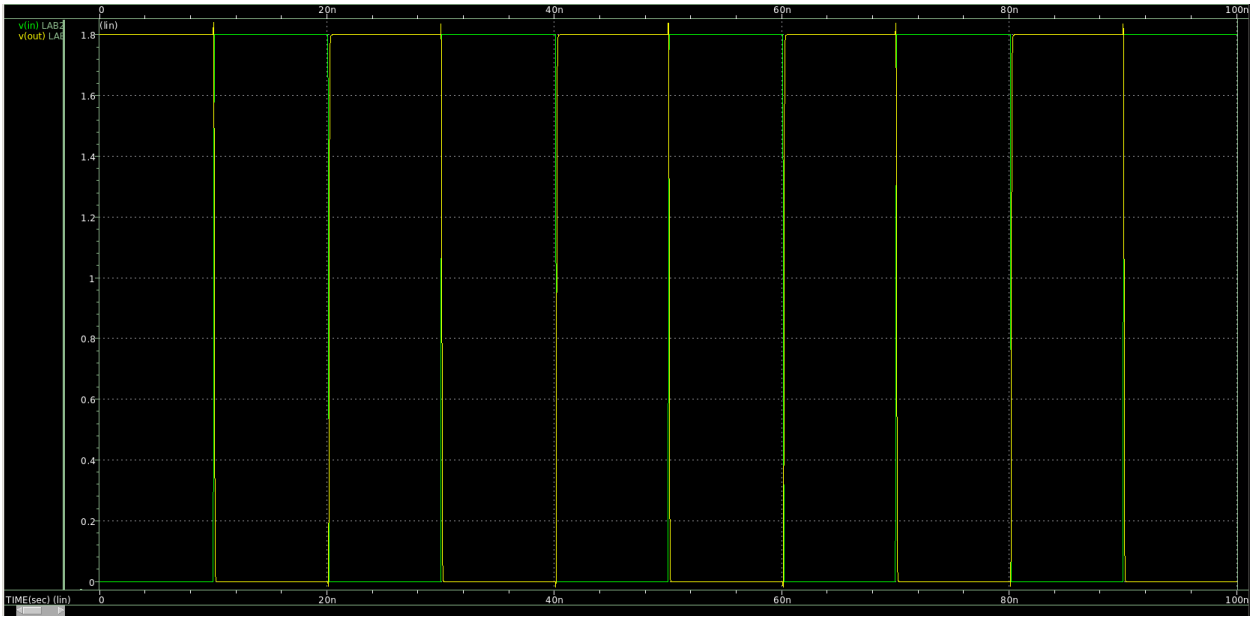
- *Low-to-High Propagation Delay (tplh): 55.2 ps*

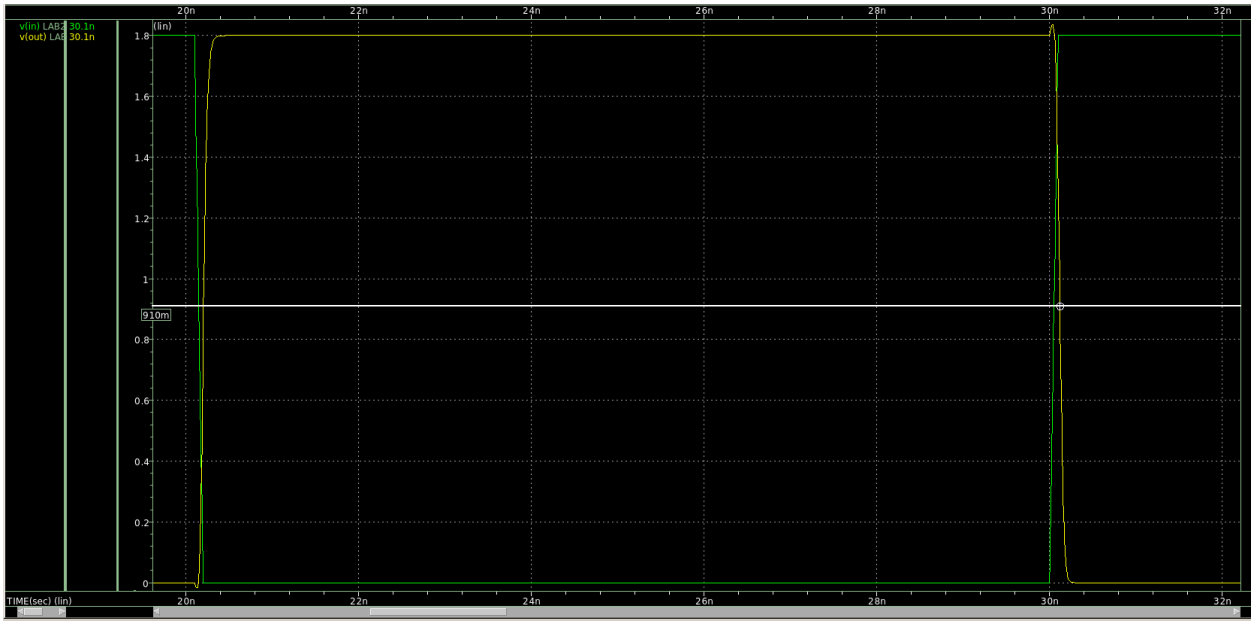
* Time for the output to switch from low to high after the input changes. Influenced by the PMOS transistor's drive strength and load conditions.

- *Rise to Fall Time Difference (trise_tfall_diff%): 0.542%*

* Decrease trise_tfall_diff% by:

- Balancing the W/L ratios of the PMOS and NMOS transistors to ensure symmetrical drive strengths. Fine-tuning the W/L ratios so that the drive strengths of both transistors match, resulting in similar rise and fall times.





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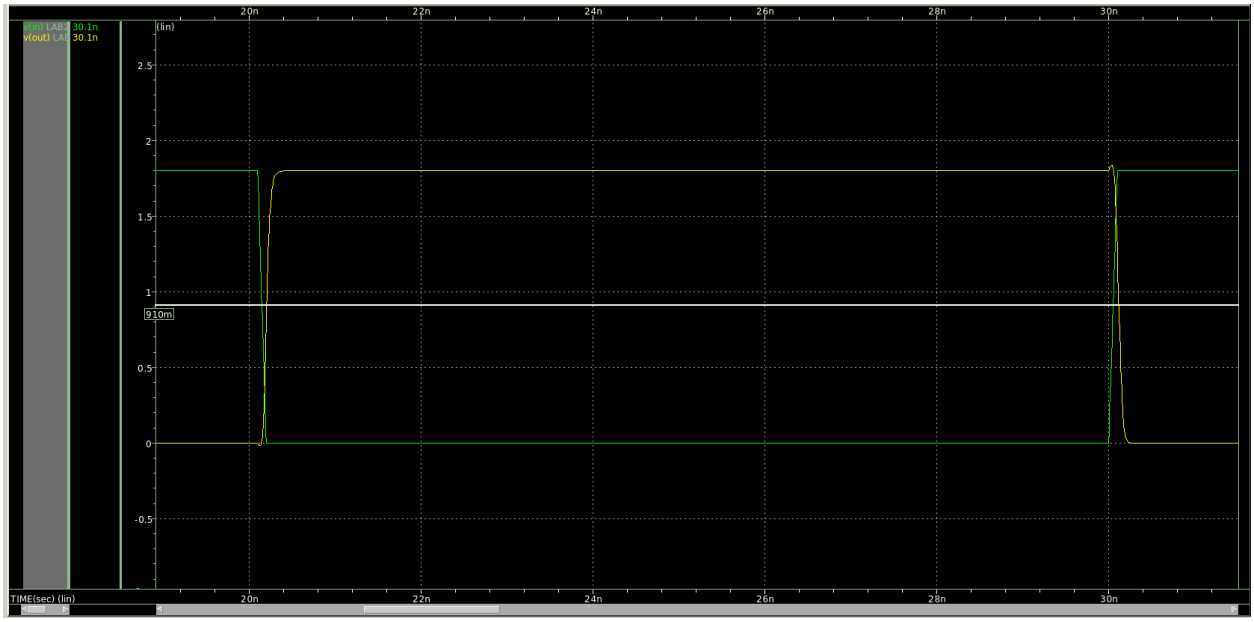

Figure 2. Output Waveform

Comment:

- When Vi = 0, the NMOS is off, the PMOS is on, Vout is up to 1.8V.

- When 0 < Vi < V_{TH}: the NMOS is off, the PMOS is on, Vout is pulled up close to Vdd, but may drop slightly due to voltage drop across the PMOS.

- When Vi is approximately V_{TH}, the NMOS is on, the PMOS is off, Vout starts converting from V_{dd} to GND.

- When V_{TH} < Vi < (V_{dd} – V_{TH}), the NMOS is on, the PMOS is off, Vout is pulled down close to GND, but there may be a slight positive voltage due to the voltage drop across the NMOS.

- When Vi is approximately V_{dd}, the NMOS is on, the PMOS is off, Vout is 0 (GND).

- With H Cursor, the intersection position between Vin and Vout is at Vin = 910mV. We want that intersection point to be located exactly at the position Vdd/2 = 900mV.

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