National Cheng Kung University (NCKU)

Academy of Innovative Semiconductor and Sustainable Manufacturing

Analog Integrated Circuit Design and Layout

Final Project

Single-Ended Differential Two-Stage OPAMP Layout

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Introduction

To begin, this laboratory will pertain to designing and laying out a single-ended differential two-stage operational amplifier (OPAMP). The circuit schematic of the single-ended differential two-stage OPAMP can be found in figure 1, this OPAMP consists of three sections:

1. Bias Circuit. This portion of the circuit is denoted by the teal portion of figure 1. The bias circuit will bias the current sources transistors (M5 and M6) and the compensation transistor (M16) into the saturation region. Please note that this portion of the circuit will not be implemented in our layout.
2. Differential-input (first stage).
    a. Current Source. This section is denoted by the purple portion of figure 1 and consists of the M5 transistor
    b. Differential Pair. This section is denoted by the pink portion of figure 1 and consists of the M1 and M2 transistors.
    c. Common-Mode Feedback (CMFB). This section is denoted by the yellow portion of figure 1 and consists of transistors M3 and M4.
3. Common source (second stage)
    a. OPAMP Compensator. This is denoted by capacitor Cc and transistor M16
    b. Current Source. This section is denoted by the blue portion of figure 1 and consists of transistor M6.
    c. Common Source Amplifier. This is denoted by the yellow section of figure 1 and consists of transistor M7.

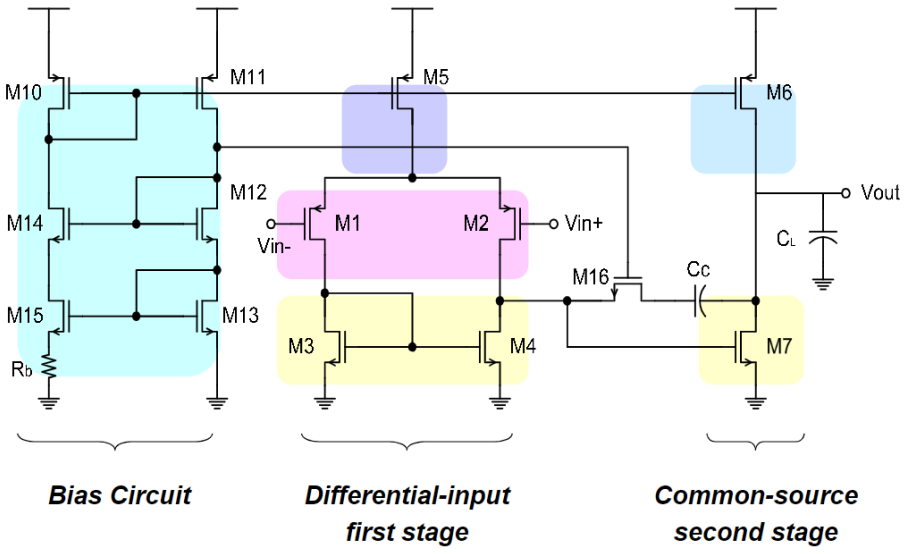


Figure 1 - Schematic of the single-ended differential two-stage OPAMP

Since the circuit in figure 1 will be implemented in biomedical sensing applications, we must reach a certain design specification to optimize the signal readout of the patient.

The desired specification can be found below in table 1. Please note that there is a difference between the pre-layout specification and a post-layout specification. The reasoning for this is that it is expected that phase margin, bandwidth and slew rate (SR) may change during the layout due to parasitic capacitances, antenna effects and unwanted changes in resistance from MOS transistors implemented as resistors. As such, we must compensate for the unwanted effects by over-engineering the specification by around 10%. The conditions in which the transistor will be exposed to is shown in figure 2.

Table 1 - Design specifications

Parameters	Pre-layout specification	Post-layout specification
DC gain	≥ 63dB	≥ 63dB
Phase Margin(PM)	≥ 65	≥ 60
Output Swing	63 dB (1413)	63 dB (1413)
Unity-Gain Bandwidth	≥ 170 MHz	≥ 160 MHz
Slew Rate	≥ 80 V/us	≥ 75 V/us
Power Consumption	Try to optimize	Try to optimize
Chip Area	Try to optimize	Try to optimize

Table 2 - Design Conditions

Design Conditions	
Process Technology	CIC 0.18um 1.8V 1P6M virtual Process
Corner	TT
Temperature	27°C
Power supply	VDD=1.8V & VSS=0V
Loading (C_L)	2pF
Input common mode voltage (V_{cmi})	0.9V
Output common mode voltage (V_{cmo})	0.9V

1-1. OPAMP design methods and process

From table 1, we notice that we must minimize the power consumption and chip area, however, this can only be done once we reach the desired specification of the other required parameters. The chip area can also not be optimized during the pre-layout aside from minimizing the individual transistor sizes. To minimize induvial transistor sizes, transistors adjacent to each other must be of same parallels (m) and widths. The reasoning for this is to avoid bending in the routing of metal wire guides, this will minimize space used on chip and any added resistance.

As such, minimizing the overall chip area will mainly be done during the layout by reducing the space between components. During this section, we will elaborate on how we methodically tuned certain transistors to meet the specification.

Firstly, we must design the circuit to meet the phase margin, bandwidth and gain since these are the most essential parameters of the biomedical sensor. The first stage functions to create gain for the circuit with $A_V = g_{m1,2}(r_{o1,2}//r_{o3,4})$. The second stage functions to extend the output swing. The compensation part is used to adjust the phase margin. That said, we will first maximize the gain via stage 1, then optimize the bandwidth with stage 2 and finally tune the phase margin with the compensation transistor M16 and capacitor Cc.

After achieving the desired gain and bandwidth, we noticed that the slew rate was below the desired specification. To improve the slew rate, we needed to increase the drain current (I_D), meaning increasing the width of the current source transistor M6 in stage 2. However, increasing the width has its limits in stage 2, as excessively increasing the width does not significantly enhance the slew rate.

$$SR < \frac{I_2}{C_c + C_L}$$

Therefore, we can reduce the value of the compensation capacitor (C_C) to increase the slew rate and simultaneously increase the bandwidth. However, this also reduces the phase margin. To increase the phase margin, we can increase g_{m7} as it will shift the second pole to a higher frequency as show by the following equations. For large C_L we can make the following approximations:

$$\omega_{p2} \approx \frac{g_{m7}}{C_L}$$

$$\omega_{p1} \approx \frac{1}{g_{m7} R_S R_L C_c}$$

$$\omega_z \approx \frac{1}{C_c(g_{m7}^{-1} - R_Z)}$$

$\omega_{ta} = \frac{g_{m1}}{C_C}$ (unity-gain frequency) `

$$Phase\ at\ unity\ gain\ frequency = \angle(FirstPole) + \angle(SecondPole) + \angle(Zero, if any)$$

$$PM = 180 - (\angle(Phase\ at\ unity\ gain\ frequency))$$

$$phase\ at\ unity\ gain\ frequency = \arctan\left(\frac{\omega_{ta}}{\omega_{p1}}\right) + \arctan\left(\frac{\omega_{ta}}{\omega_{p2}}\right) + \arctan\left(\frac{\omega_{ta}}{\omega_z}\right)$$

$$PM = 180 - \left(\arctan\left(\frac{\omega_{ta}}{\omega_{p1}}\right) + \arctan\left(\frac{\omega_{ta}}{\omega_{p2}}\right) + \arctan\left(\frac{\omega_{ta}}{\omega_z}\right)\right)$$

Substitute:

$$PM = 180 - \left(\arctan(dc-gain) + \arctan\left(\frac{g_{m1}C_L}{g_{m7}C_c}\right) + \arctan\left(\frac{g_{m1}(1-g_{m7}R_S)}{g_{m7}}\right)\right)$$

$$PM = 180 - \left(90 + \arctan\left(\frac{g_{m1}C_L}{g_{m7}C_c}\right) + \arctan\left(\frac{g_{m1}(1-g_{m7}R_S)}{g_{m7}}\right)\right)$$

$$PM = 90 - \left(\arctan\left(\frac{g_{m1}C_L}{g_{m7}C_c}\right) + \arctan\left(\frac{g_{m1}(1-g_{m7}R_S)}{g_{m7}}\right)\right)$$

Finally, to minimize the power consumption, we can change the width of the transistors while still staying relatively close to the specification. This should be done symmetrically across transistors adjacent to each other to ensure we don't vary the functionality of the differential input stage (stage 1), and the common source stage (stage 2). We will not change the width of transistors M5 and M6 since these transistors will be current sources driving their respective stages, as such, we optimize width for other transistors. When trading off these values, we achieved component parameters that meet the specifications which are shown in figures 2 and 3.

```
*Stage1
m05 n0   vb1 vdd vdd p_18 l=0.18u w=2.48u m=4
m01 vbn  vin n0  n0  p_18 l=0.68u w=6.06u m=4
m02 von1 vip n0  n0  p_18 l=0.68u w=6.06u m=4
m03 vbn  vbn gnd gnd n_18 l=3.50u w=4.37u m=2
m04 von1 vbn gnd gnd n_18 l=3.50u w=4.37u m=2
```

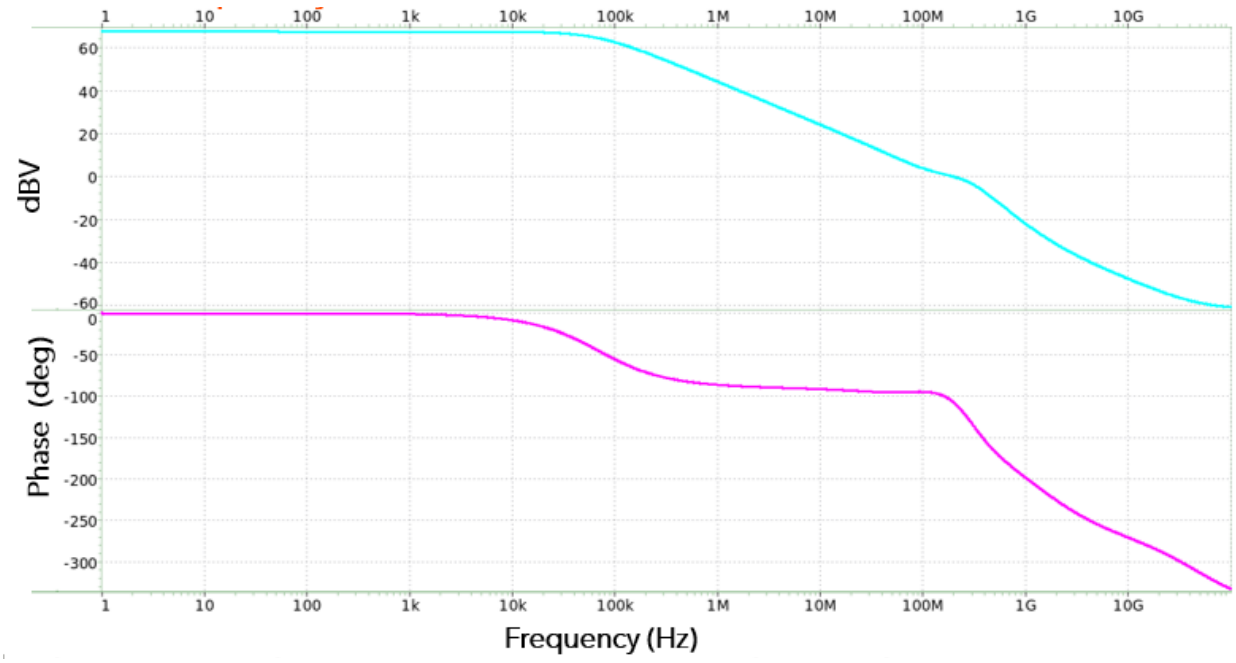
Figure 2 . First Stage parameters

```
*Stage2
m06 vout vb1  vdd vdd p_18 l=0.20u w=5.60u m=16
m07 vout von1 gnd gnd n_18 l=0.31u w=4.60u m=8
************************************************
$ Bias (external)
* vvb1 vb1 gnd 1.17
* vvbr vbr gnd 1.17
************************************************
$ write your zero compensation here
ccp vout  nrcp 0.25p
m16 nrcp vbr von1 gnd n_18 l=0.21u w=0.75u m=6
```

Figure 3. Second Stage parameters

1-2. OPAMP Pre-layout simulation results

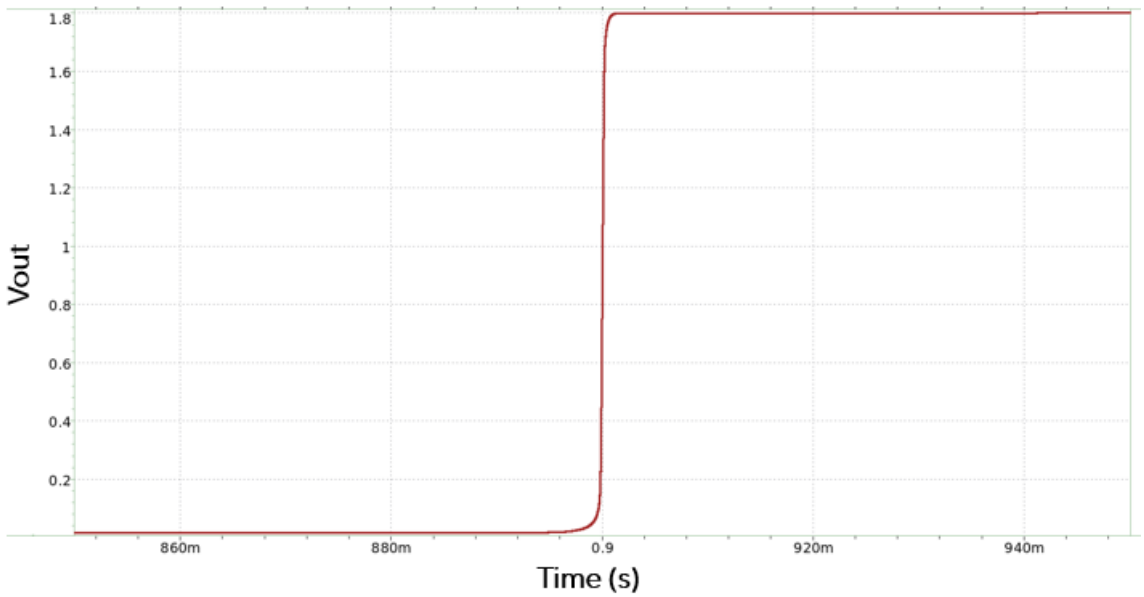
In this section we demonstrate the AC, DC and Transient pre-layout simulations. The waveforms and their respective output parameters are shown in figures 4,5 and 6. The bode plot in figure 4 is a result of AC simulation and demonstrates the voltage and phase of the output signal versus the frequency on the log scale. From figure 4, we can extract the gain, gain bandwidth (GBW), phase, phase margin and power consumption. Based on the parameters implemented in the previous section, we are nearly 10% above the desired pre-layout specifications for all parameters. The second pole around 100Mhz is relatively flat which indicates a relatively large GBW as we can see in the parameters below.



gain	gbw	phase	phase_margin
power_avg	temper	alter#	
67.4658191263	1.962723937e+08	-106.8235346388	73.1764653612
8.537603618e-04	27.0000000000	1	

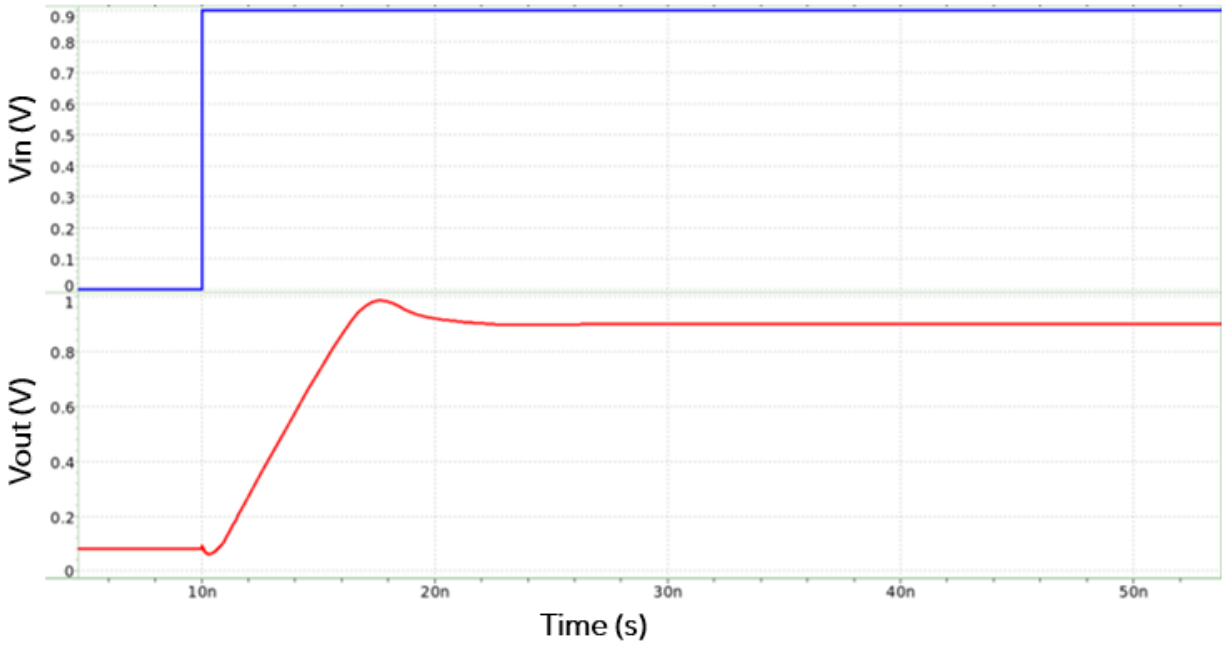
Figure 4. AC pre-layout simulations consisting of a bode plot and various output parameters.

Figure 5 demonstrates the DC output swing and figure 6 shows the transient response showing the slew rate. The DC output swing is well above the required specification whereas the slew rate extracted from the transient response in figure 6 is nearly double of the required specification shown in table 1. This section clearly demonstrates the satisfaction of the desired specifications. As such, we will be moving to the layout of the single output differential dual stage operational amplifier.



top_gain	bottom_gain	power_avg	temper alter#
3.363006242e+03	3.064520661e+03	5.306101176e-04	27.0000000000

Figure 5. DC pre-layout simulations consisting of output swing plot and various output parameters.



sr_rate	power_avg	temper	alter#
1.557452752e+08	8.281830229e-04	27.0000000000	1

Figure 6. Transient pre-layout simulations consisting of the input and output voltages as a function of time and various output parameters. Note that the slew rate is derived from output voltage as a function of time.

2-1. OPAMP Layout considerations and placement methods

As the pre-layout simulations were successful, we will attempt to maintain the specification as best we can in the layout implementation. This will be done by minimizing the distance between the electrical components without breaking any design rule checks. As shown in figures 5-8 below, the space between adjacent components was implemented to be as small as possible. This will also minimize the delay it will take for a signal to reach one component to another, reducing unwanted phase changes. Further, longer metal connections present unwanted parasitic capacitance in the circuit, change the overall system capacitance, potentially changing the phase and bandwidth. Reducing the distance between components also reduces power consumption since the resistance scales with length of metal wire guides.

Further, we must avoid any 90-degree bends in metal layers unless they are directly connected to vias. 90-degree bends in a metal wireguide will build lead to a dissipation of charge and cause significant signal loss. To avoid this, we implemented 45-degree metal wire guide bends when routing to various components on chip as seen in figures 5-8 below.

Guard rings were implemented around every stage of transistors to avoid crosstalk between analog circuits. This is perhaps one of the most essential components as multiple transistors will be processing the signal over a given number of ns,

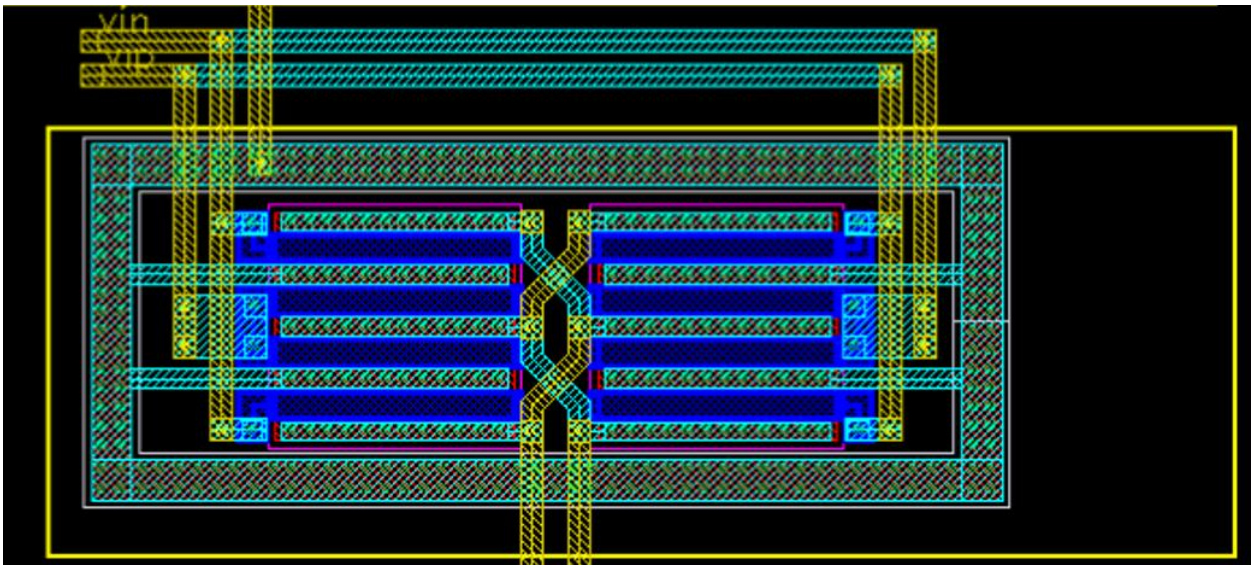


Figure 5. Stage 1 differential pair layout in laker.

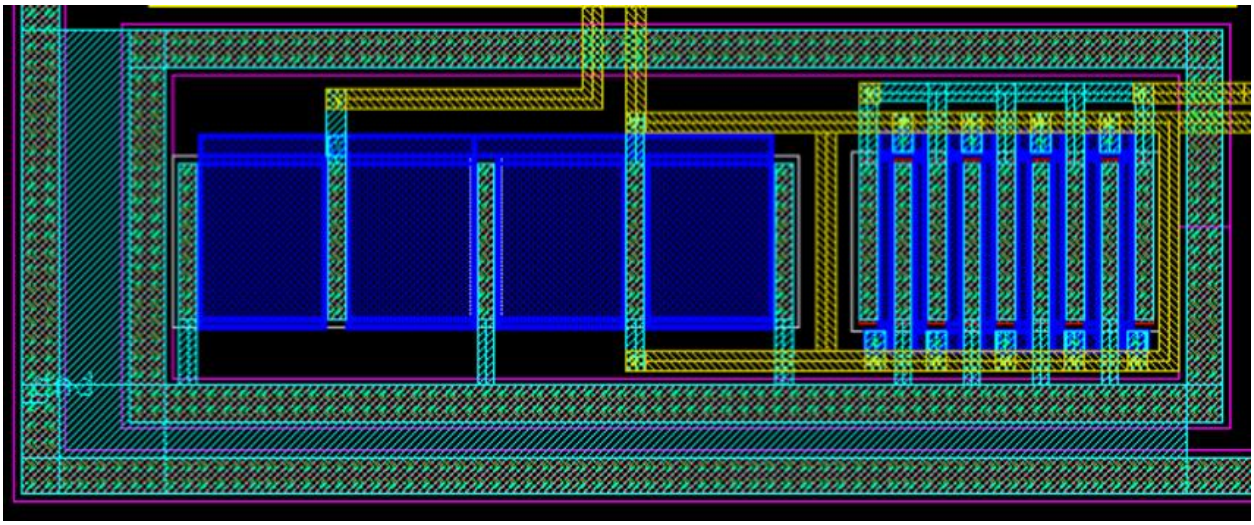


Figure 6. Stage 1 and 2 showing transistors M3, M4 and M7 layout in laker.

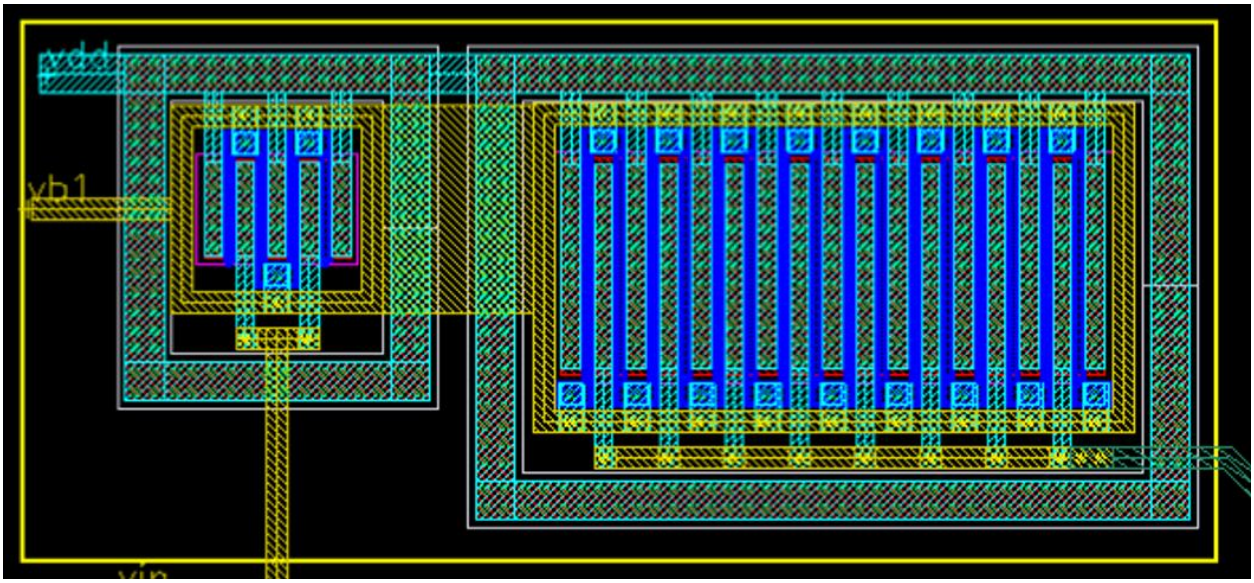


Figure 7. Layout of stage 1 and 2 current sources including transistor M5 and M6.

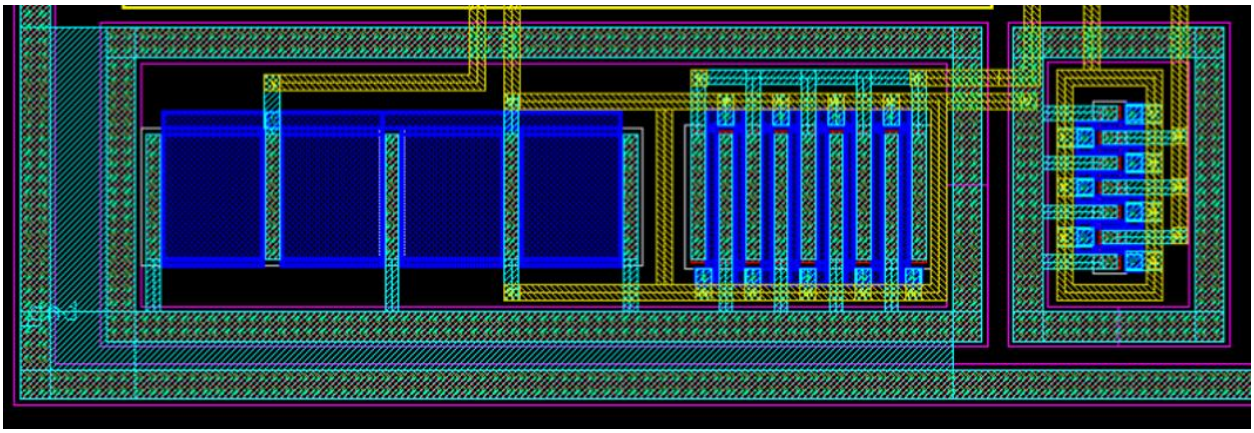


Figure 8. Layout of the M16 compensation transistor.

The capacitor was much more problematic than anticipated, it should be noted that the MIM capacitor is directly coupled to the compensation capacitor M16. For the implementation of this capacitor, it is important to use several capacitors to minimize process variation during fabrication. As such, 4 MIM capacitors of 0.0625pF were connected in parallel to meet the required value of 0.25pF.

$$C \approx C_S.N\ (with\ C = 0.25pf\ and\ N = 4)$$

To create the capacitor, we utilized the create capacitor in laker and and entered the value of 0.0625pF. Since the laker create capacitor function did not include the Metal6 and MIMDUM layers, we removed the Metal5 and VIA5 layer and created a MIMDUM layer of the same size as the underlying Metal5 layer. Following this, we created a CTM and Metal6 layer of the same size and created a VIA to connect the Metal6 layer down to the Metal5 layer. A more understandable of a MIM capacitor can be seen in figure 9.

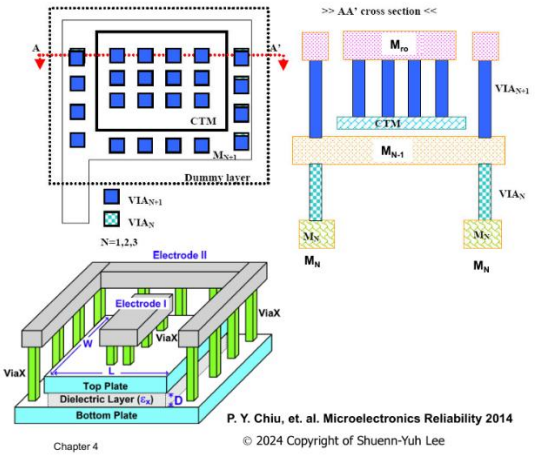


Figure 9 – MIM capacitor Schematic

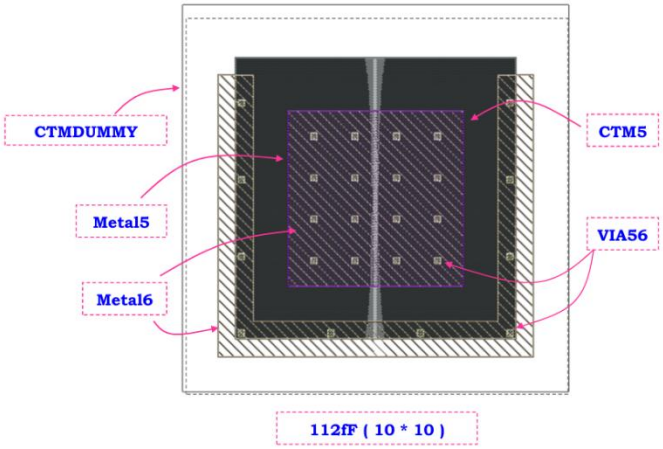


Figure 10 – Demonstration of the layout of a MIM capacitor in laker.

Following the implementation of the individual capacitor, we copied the capacitor into 4 different capacitors and connected Metal5 and Metal6 wires to link these capacitors. Following this we created a dummy cell with smaller capacitors. We created a P-guard ring on the outer layer and created a Metal5 and Metal6 path from the Dummy to the P-guard ring. We created a VIA from Metal6 down to Metal5 and straight down to the P-sub layer. Finally, we connected the Metal5 and Metal6 wires from the capacitors to the outside to connect to the remaining parts of the OPAMP.

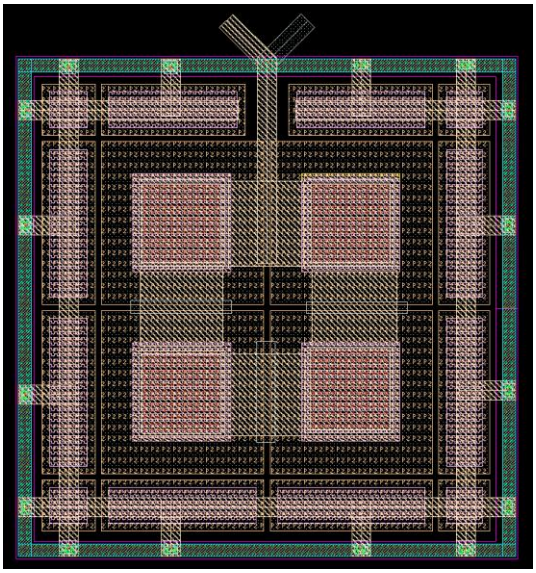


Figure 9. Cc capacitor layout in Laker.

2-2. Final layout and verification

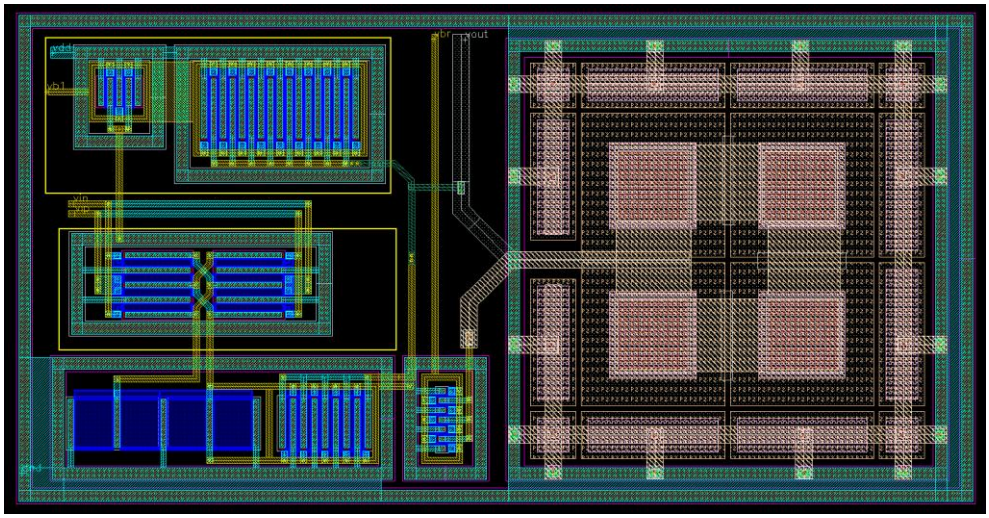


Figure 10. Single-ended differential two-stage operational amplifier layout.

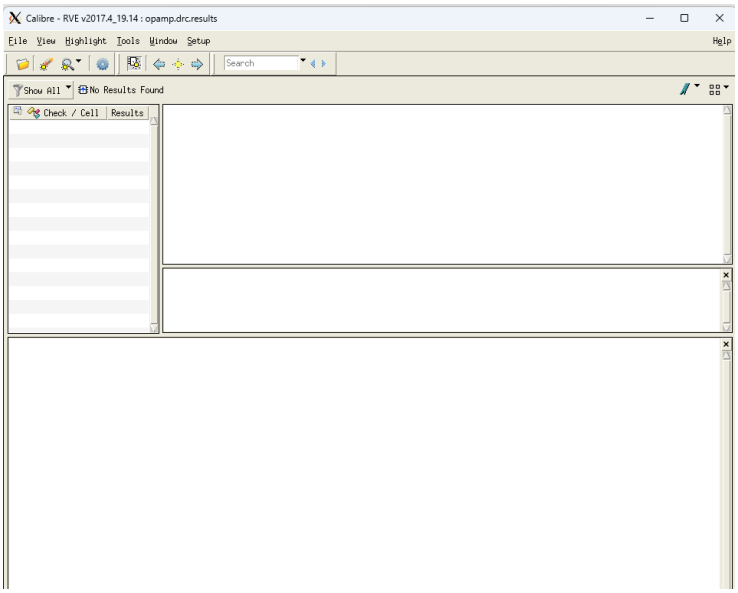


Figure 11. OPAMP DRC Pass

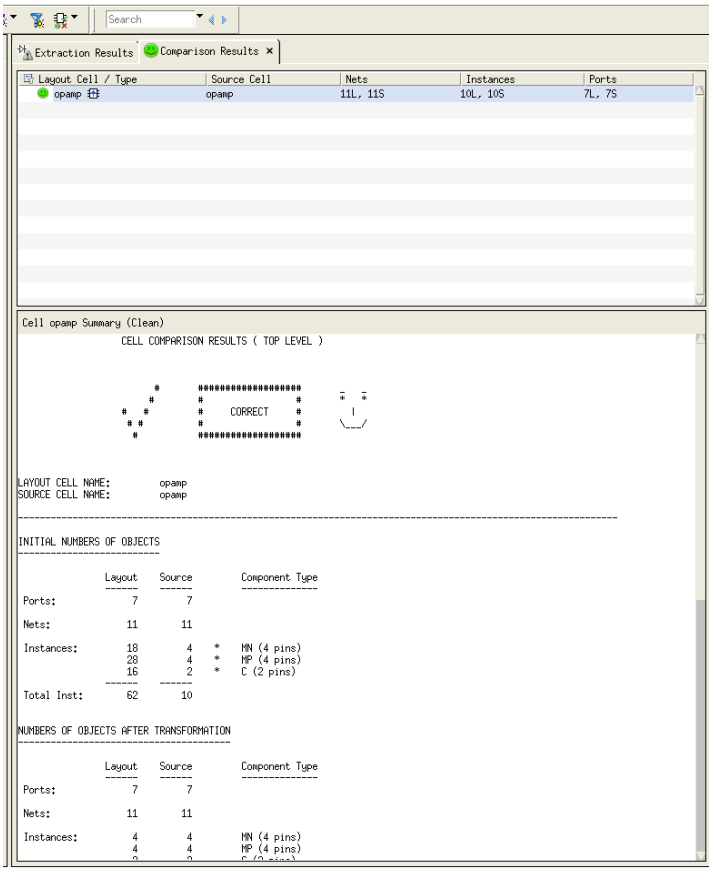


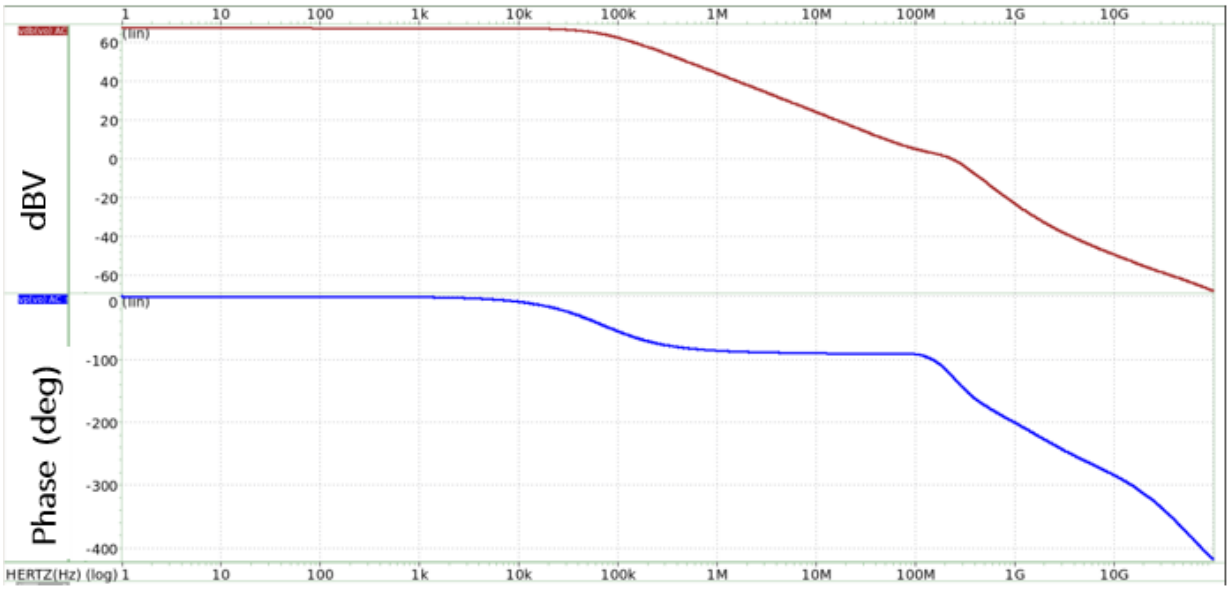
Figure 12. OPAMP LVS Pass

2-3. OPAMP post-layout simulation results

As the layout passed all required verifications, we were able to export the spice netlist and run the post-layout simulations. The Bandwidth value increases significantly, but the Phase Margin decreases. This can be explained as follows. Parasitic Capacitance and Inductance: The layout introduces parasitic elements such as capacitance and inductance due to the physical interconnections between components. These parasitics can affect the frequency response of your circuit. Increased parasitic capacitance can lead to a reduction in phase margin by introducing additional phase lag, but it can also increase the bandwidth if it changes the poles and zeros of the system. Other parameters do not change significantly between pre-sim and post-sim.

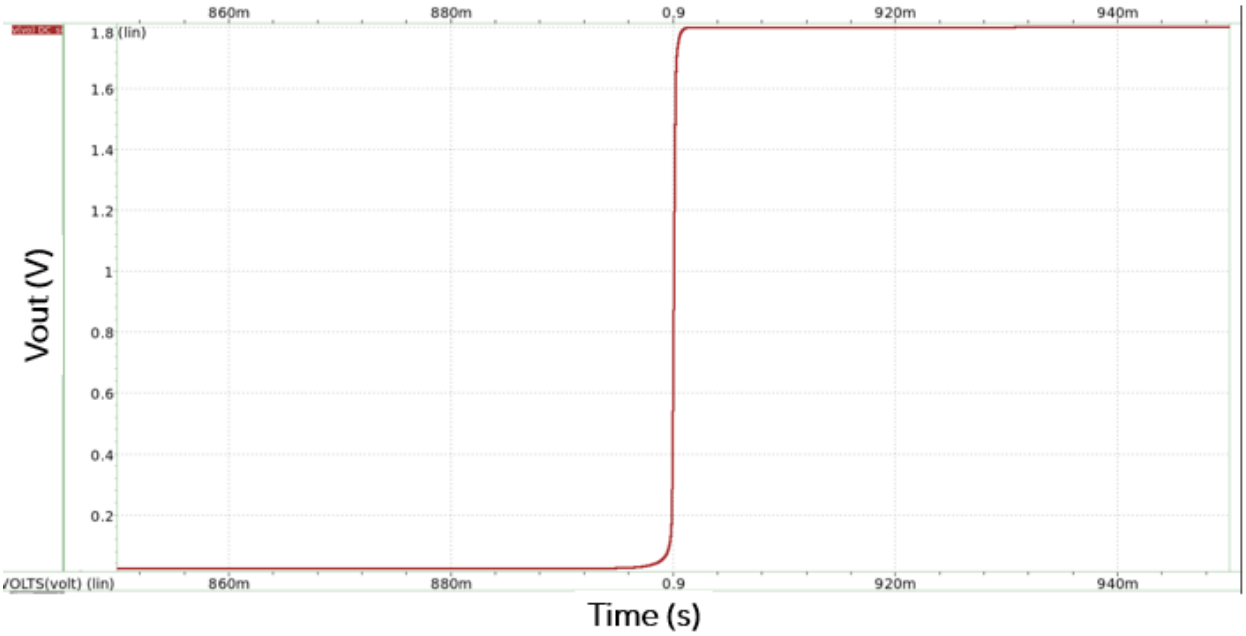
Table 3. Comparison of pre and post layout simulation results

Parameters	Specification	Pre-layout	Post-layout
DC gain (dB)	≥ 63	67.46	67.22
Output Swing	Top gain : 3363 Bottom gain : 3063	Top gain : 3363 Bottom gain : 3063	Top gain : 3576 Bottom gain : 3082
Unity Gain Bandwidth (MHz)	≥ 170	196	232
Slew Rate (V/us)	≥ 80	155	151
Power Consumption (mW)	Try to optimize	0.853	0.881
Phase Margin (°)	≥ 65	73.2	54.1
Layout Area	Try to optimize	N/A	85.825um X 44.039um



gain	gbw	phase	phase_margin
power_avg	temper	alter#	
67.2213995861	2.323747172e+08	-125.7856991286	54.2143008714
8.808402761e-04	27.0000000000	1	

Figure 13. AC post-layout simulations consisting of a bode plot and various output parameters.



top_gain	bottom_gain	power_avg	temper
alter#			
3.576785135e+03	3.082900027e+03	5.258342869e-04	27.0000000000

Figure 14. *DC post-layout simulations consisting of output swing plot and various output parameters.*

sr_rate	power_avg	temper	alter#
1.518298394e+08	8.216712935e-04	27.0000000000	1

Figure 15. Transient *post-layout simulations consisting of the input and output voltages as a function of time and various output parameters. Note that the slew rate is derived from output voltage as a function of time.*

Conclusion

We can increase the Metal6 layer and CTM or decrease the Metal5 layer and MIMDUM to increase the capacitor value to meet the required Phase Margin while still ensuring good Bandwidth.

Coming to this course, this is the first time we have learned more deeply about analog circuit design. This is also the first time we have done circuit layout. This final project is the first project we have experienced. After this course, we have gained much more experience to further pursue our studies in analog circuit design. We want to express our gratitude to Prof. Shuenn-Yuh Lee and all the TAs who have supported us over the past week. Our report may have some shortcomings, and we hope everyone can overlook them.