Academy of Innovative Semiconductor and Sustainable Manufacturing

ANALOG INTEGRATED CIRCUIT DESIGN AND LAYOUT LAB

TWO STAGE OPAMP

Student: Pham Lo Hoang Khang

Student ID: XZ4138222

Group: B1

LAB2-3: SINGLE-ENDED DIFFERENTIAL TWO-STAGE OPAMP

```
**************************************************************
.subckt opamp vip vin vout vdd gnd vb1 vbr
**************************************************************
$ write your stage1+stage2 here

*Stage1
m05 n0   vb1 vdd vdd p_18 l=0.18u w=2.48u m=4
m01 vbn  vin n0  n0  p_18 l=0.68u w=6.06u m=4
m02 von1 vip n0  n0  p_18 l=0.68u w=6.06u m=4
m03 vbn  vbn gnd gnd n_18 l=3.50u w=4.37u m=2
m04 von1 vbn gnd gnd n_18 l=3.50u w=4.37u m=2
*Stage2
m06 vout vb1  vdd vdd p_18 l=0.20u w=5.60u m=8
m07 vout von1 gnd gnd n_18 l=0.31u w=4.60u m=4
**************************************************************
$ Bias (external)
* vvb1 vb1 gnd 1.17
* vvbr vbr gnd 1.17
**************************************************************
$ write your zero compensation here
ccp vout  nrcp 0.3p
m16 nrcp vbr von1 gnd n_18 l=0.21u w=1u m=4
**************************************************************
.ends
```

Figure 1. Opamp Parameter

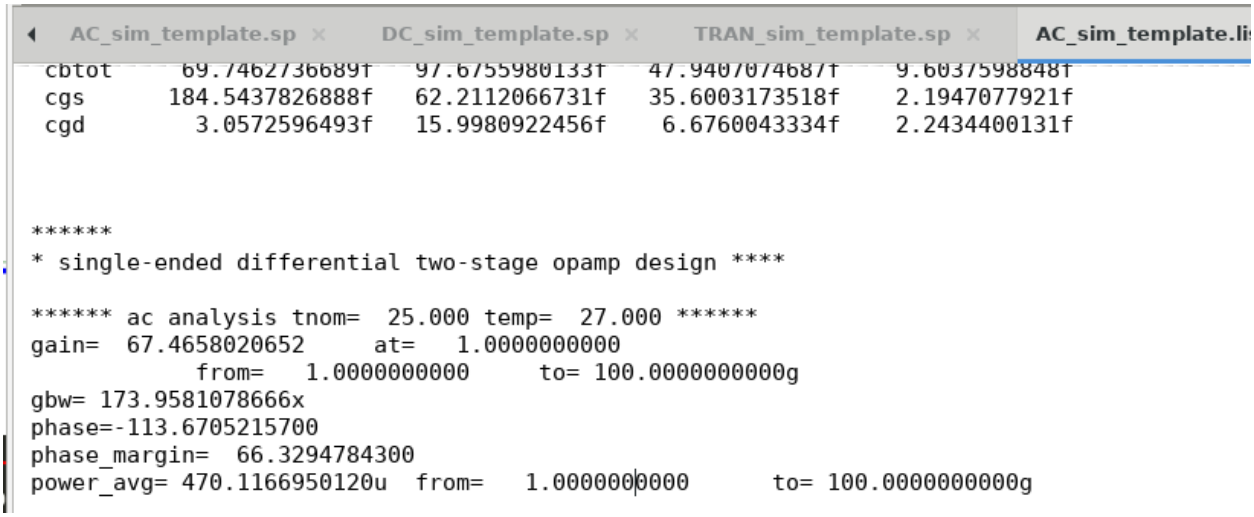

Figure 2. Gain, Bandwidth, Phase, Phase Margin & Power Consumption

```
**info** set option symb=1 internally to help for convergence.
*****************************************************************
******  option summary
******
runlvl  = 5         bypass  = 2.0000000000
 Opening plot unit= 15
file=DC_sim_template.pa0

******
* single-ended differential two-stage opamp design ****

****** dc transfer curves tnom=  25.000 temp=  27.000 ******
top_gain=   3.3630955630k
bottom_gain=   3.0643893203k
power_avg= 308.2543604534u  from= 850.0000000000m     to= 950.0000000000m
**info** dc convergence successful at Newton-Raphson method
******
* single-ended differential two-stage opamp design ****

****** operating point information tnom=  25.000 temp=  27.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage            node    =voltage

+0:vb1     =   1.1700000000  0:vbr     =   1.1700000000
+0:vdd     =   1.8000000000  0:vin     =   1.8000000000
+0:vip     =   0.            0:vo      =  11.8842182429m
+1:n0      =   1.7999998184  1:nrcp    =   1.0840905013
+1:vbn     =  18.0759881697m 1:von1    =   1.7999997870
```

Figure 3. Top gain and Bottom gain

```
******
* single-ended differential two-stage opamp design ****

****** transient analysis tnom=  25.000 temp=  27.000 ******
sr_rate=  84.2183109219x
power_avg= 457.3257141551u  from=   0.            to=  10.0000000000u
```

Figure 4. Slew rate

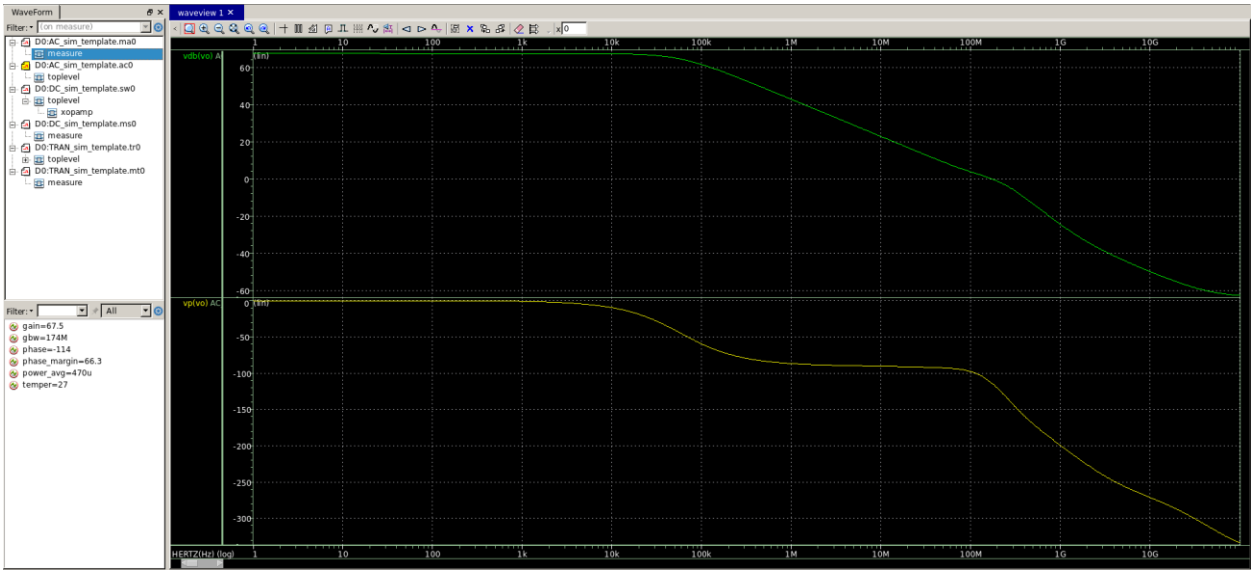

Figure 5. Bode plot of Opamp

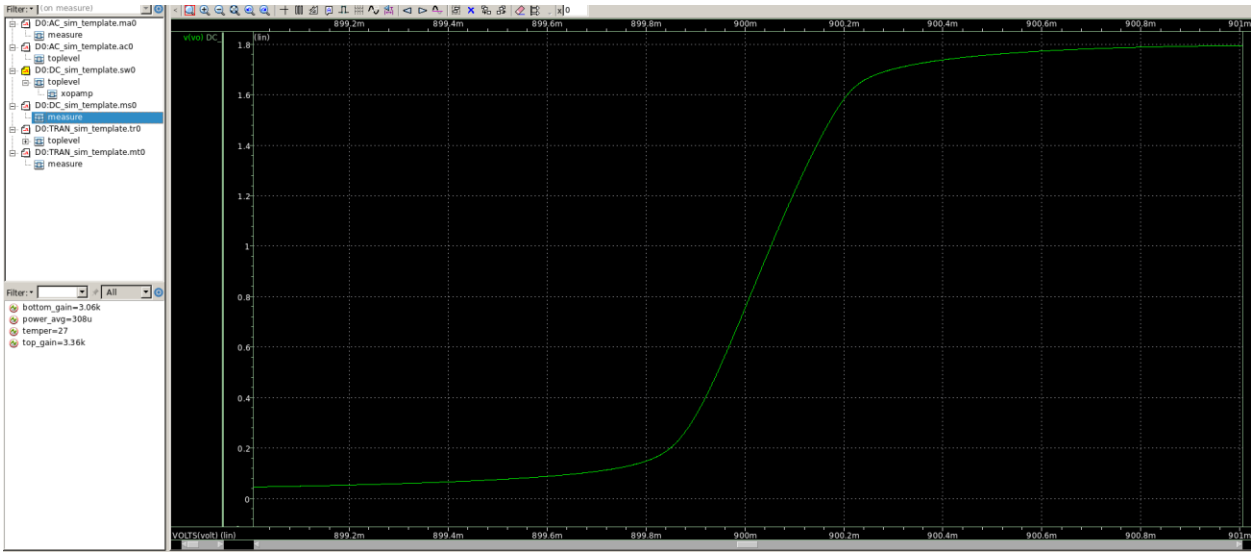

Figure 6. Output Swing of Opamp

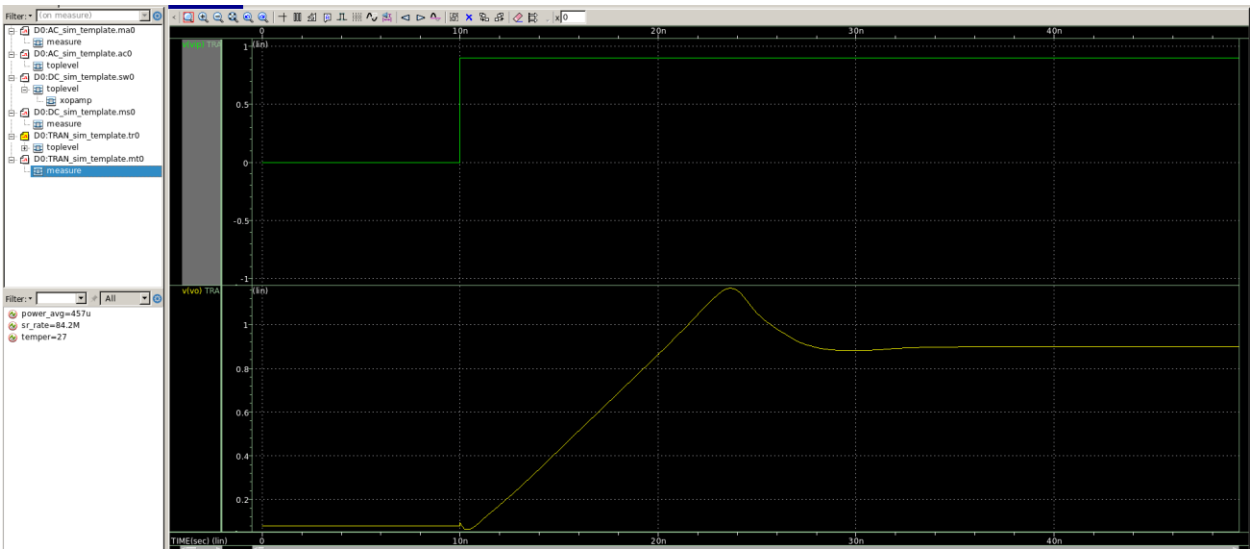

Figure 7. Slew rate of Opamp

Comment:

First, I noticed that the slew rate is low, so to increase the slew rate, I need to increase the drain current (I_D), which means increasing the width (W). However, increasing W has its limits in stage 2, as excessively increasing W does not significantly enhance the slew rate. Therefore, I reduce the value of the compensation capacitor (C_C) to increase the slew rate and simultaneously increase the bandwidth, but this also reduces the Phase margin. When trading off these values, I finally achieve results that meet the specifications.

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