FINAL PROJECT

SINGLE-ENDED DIFFERENTIAL TWO-STAGE OPAMP LAYOUT

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OUTLINE

- Introduction
- OPAMP design methods and processes
- OPAMP pre-simulation results
- OPAMP layout considerations and placement methods
- OPAMP layout diagrams
- OPAMP post-simulation results
- Conclusion

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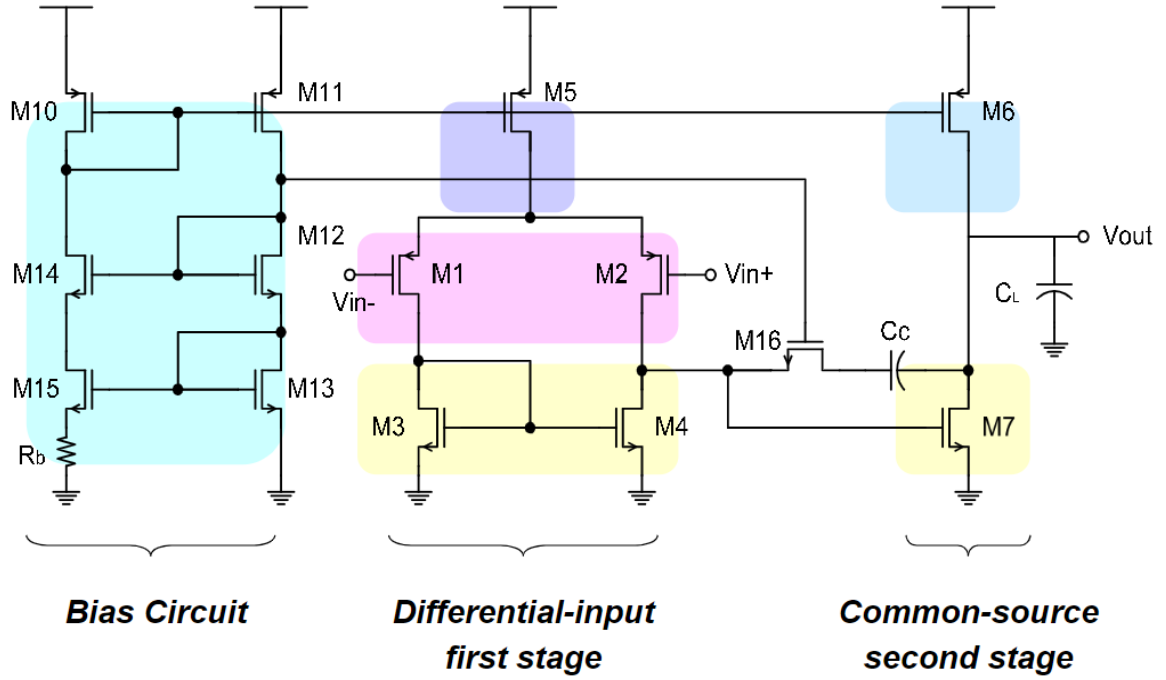
• INTRODUCTION

To begin, this laboratory will pertain to designing and laying out a single-ended differential two-stage OPAMP. The circuit schematic of the single-ended differential two-stage OPAMP can be found in figure this OPAMP consists of three sections:

1.Bias Circuit.
2.Differential-input (first stage).
    a.) Current Source
    b.) Differential Pair
    c.) Common-Mode-Feedback(CMFB)
3.Common source (second stage)
    a.) OPAMP Compensator.
    b.) Common source Amp.



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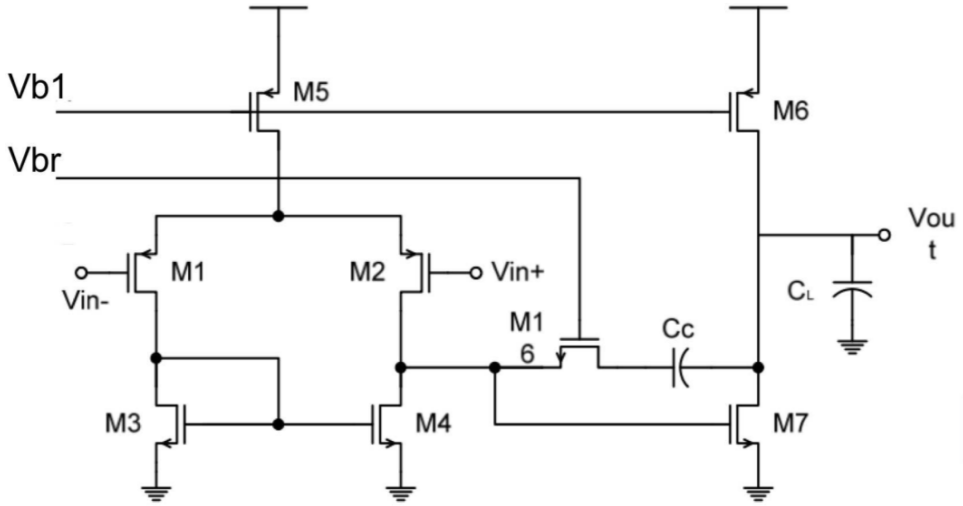
• OPAMP DESIGN METHODS

Design Specification

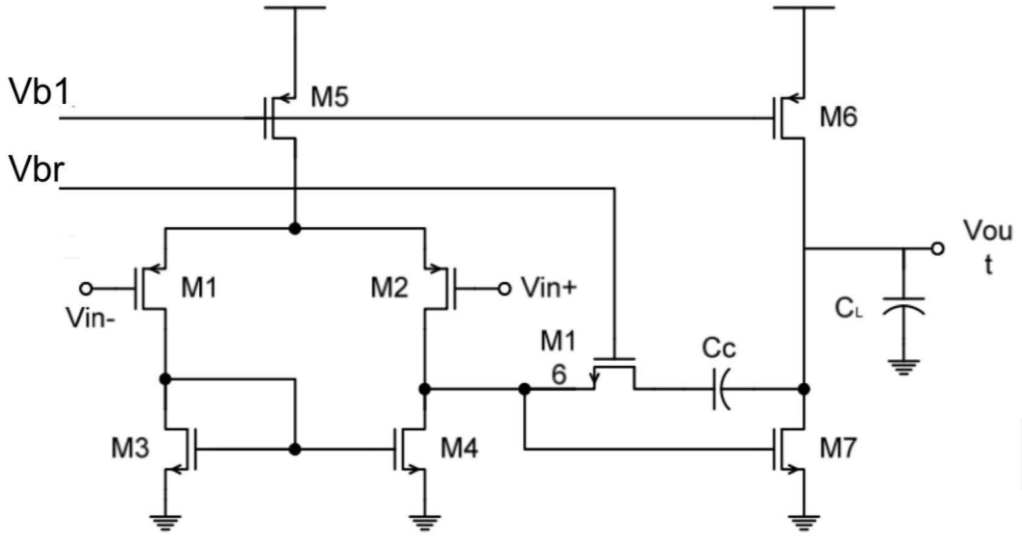
Parameters	Pre-layout specification	Post-layout specification
DC gain	≥ 63dB	≥ 63dB
Phase Margin(PM)	≥ 65	≥ 60
Output Swing	63 dB (1413)	63 dB (1413)
Unity-Gain Bandwidth	≥ 170 MHz	≥ 160 MHz
Slew Rate	≥ 80 V/us	≥ 75 V/us
Power Consumption	Try to optimize	Try to optimize
Chip Area	Try to optimize	Try to optimize



OPAMP DESIGN CONSIDERATIONS

```
.subckt opamp vip vin vout vdd gnd vb1 vbr
**********************************************************************
$ write your stage1+stage2 here

*Stage1
m05 n0   vb1 vdd vdd p_18 l=0.18u w=2.48u m=4
m01 vbn  vin n0  n0  p_18 l=0.68u w=6.06u m=4
m02 von1 vip n0  n0  p_18 l=0.68u w=6.06u m=4
m03 vbn  vbn gnd gnd n_18 l=3.50u w=4.37u m=2
m04 von1 vbn gnd gnd n_18 l=3.50u w=4.37u m=2
*Stage2
m06 vout vb1  vdd vdd p_18 l=0.20u w=5.60u m=16
m07 vout von1 gnd gnd n_18 l=0.31u w=4.60u m=8
**********************************************************************
$ Bias (external)
* vvb1 vb1 gnd 1.17
* vvbr vbr gnd 1.17
**********************************************************************
$ write your zero compensation here
ccp vout  nrcp 0.25p
m16 nrcp vbr von1 gnd n_18 l=0.21u w=0.75u m=6
**********************************************************************
.ends
```



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• OPAMP DESIGN METHODS

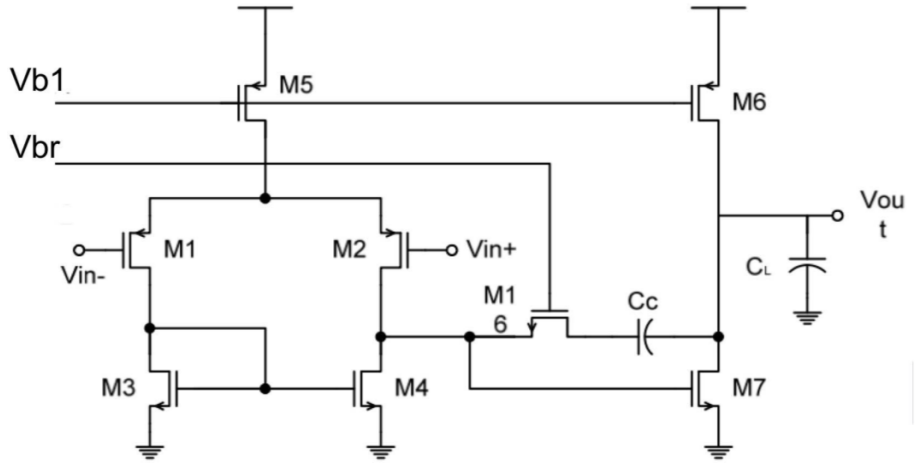
Slew Rate (SR) $< \dfrac{I5}{Cc + CL}$

Unity-Gain Bandwidth $= \dfrac{gm_{1,2}}{Cc}$

DC gain $= gm_{1,2}gm_7(ro_{1,2}//ro_{3,4})(ro_6//ro_7)$

Phase Margin (PM) = 180 -∠Phase at unity gain frequency

Phase at unity gain frequency $= \arctan(\dfrac{\omega_{at}}{\omega_z}) + \arctan(\dfrac{\omega_{at}}{\omega_{p1}}) + \arctan(\dfrac{\omega_{at}}{\omega_{p2}})$



For large CL :

$\omega_z \approx \dfrac{gm_7}{C_L}$

$\omega_{p1} \approx \dfrac{1}{gm_7(ro_{1,2}//ro_{3,4})(ro_6//ro_7)Cc}$

$\omega_{p2} \approx \dfrac{1}{(gm_7\text{-}Rz)Cc}$

$\omega_{at} \approx \dfrac{gm_{1,2}}{Cc}$

Substitute:

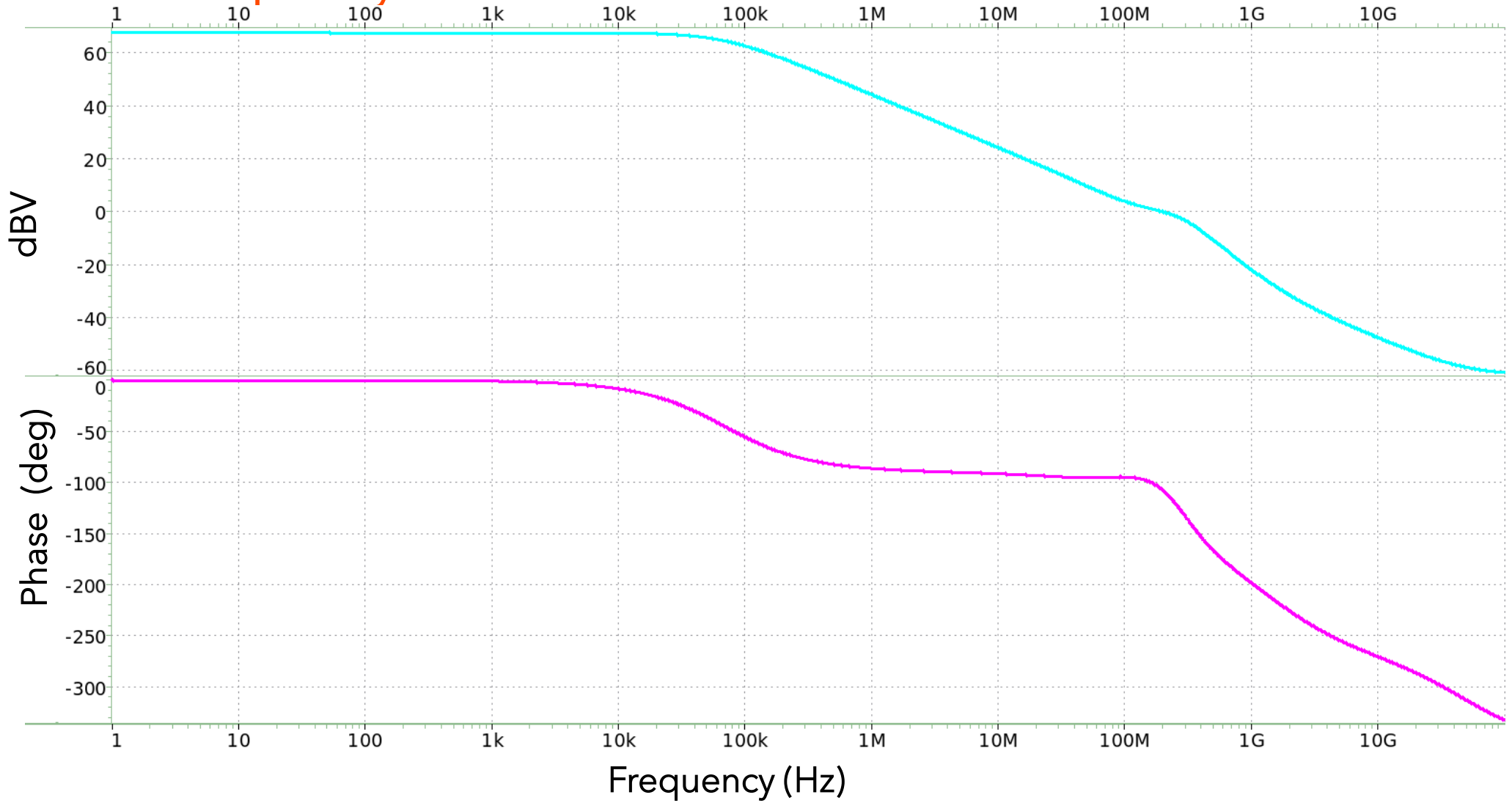
Phase Margin (PM) $= 180 - \left(\arctan(\dfrac{\omega_{at}}{\omega_z}) + \arctan(\dfrac{\omega_{at}}{\omega_{p1}}) + \arctan(\dfrac{\omega_{at}}{\omega_{p2}}) \right)$

Phase Margin (PM) $= 180 - \left(\arctan(\dfrac{gm_1(1 - gm_1Rz)}{gm_7}) + \arctan(\text{DC gain }) + \arctan(\dfrac{gm_1C_L}{gm_7Cc}) \right)$

Phase Margin (PM) $= 180 - \left(\arctan(\dfrac{gm_1(1 - gm_1Rz)}{gm_7}) + 90 + \arctan(\dfrac{gm_1C_L}{gm_7Cc}) \right)$

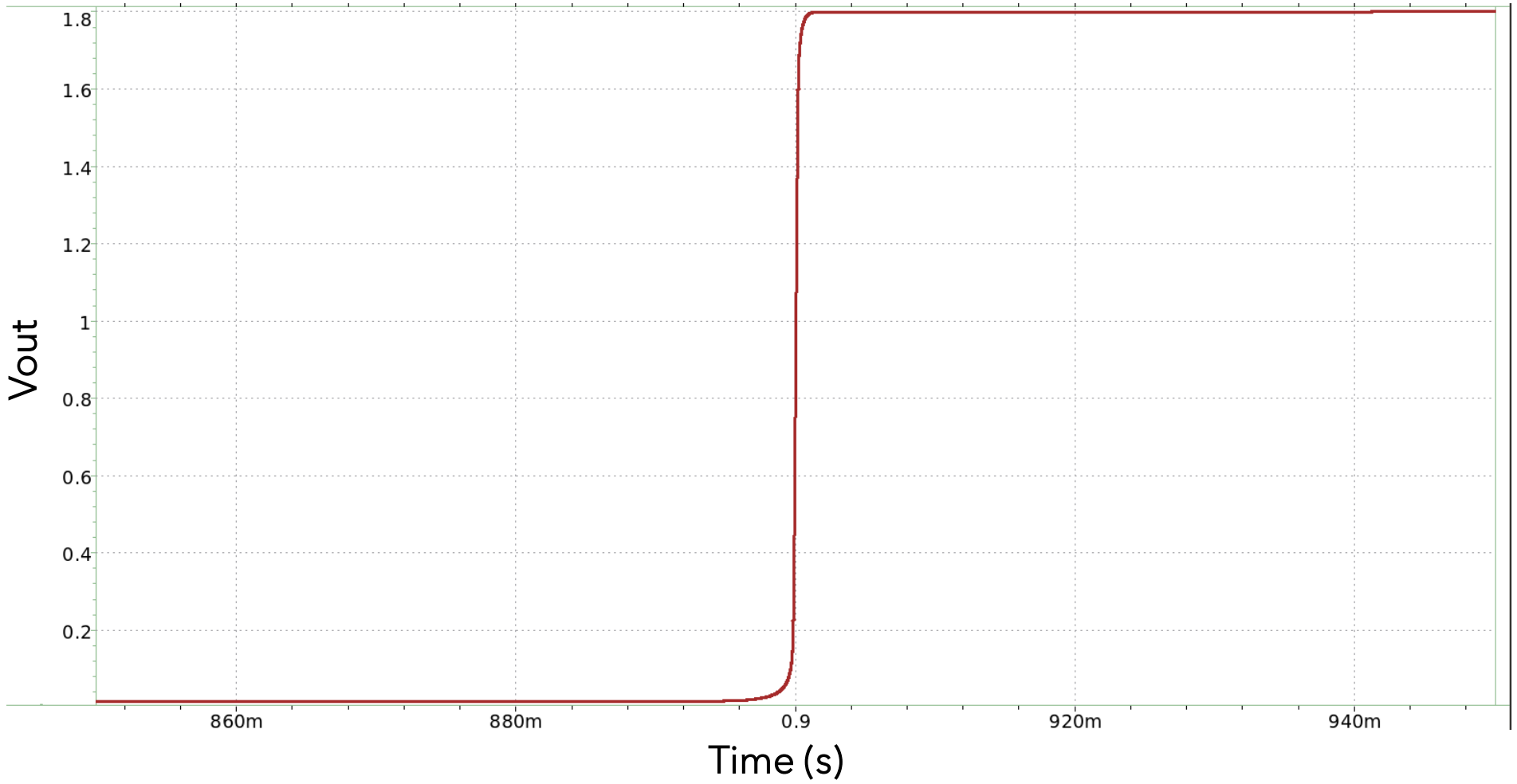
Phase Margin (PM) $= 90 - \left(\arctan(\dfrac{gm_1(1 - gm_1Rz)}{gm_7}) + \arctan(\dfrac{gm_1C_L}{gm_7Cc}) \right)$

OPAMP AC pre-layout simulation results:



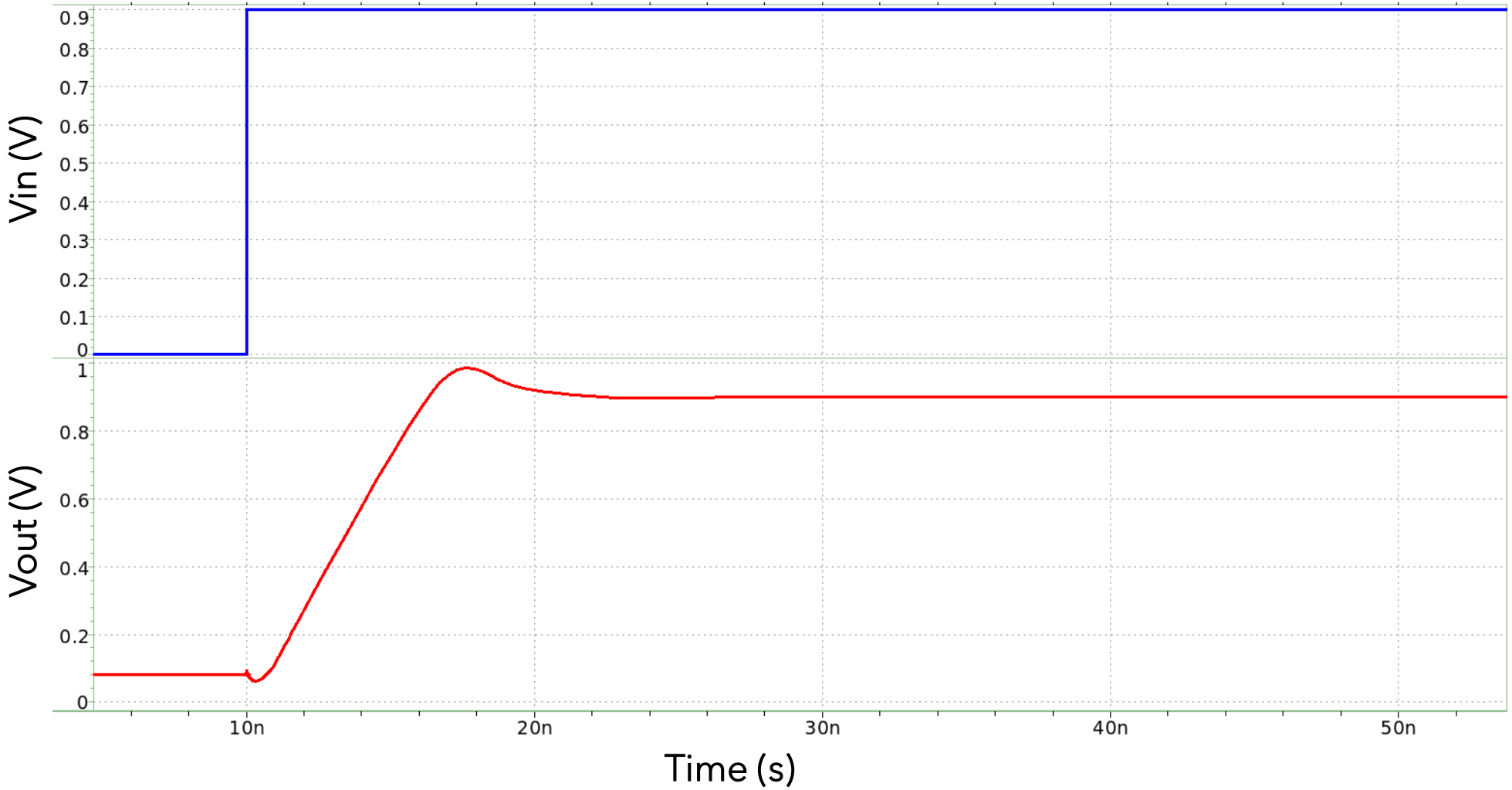
gain	gbw	phase	phase_margin
power_avg	temper	alter#	
67.4658191263	1.962723937e+08	-106.8235346388	73.1764653612
8.537603618e-04	27.0000000000	1	

OPAMP DC pre-layout simulation results:



top_gain	bottom_gain	power_avg	temper
alter#			
3.363006242e+03	3.064520661e+03	5.306101176e-04	27.0000000000

OPAMP Transient pre-layout simulation results:



sr_rate	power_avg	temper	alter#
1.557452752e+08	8.281830229e-04	27.0000000000	1

OPAMP PRE-SIMULATION RESULTS

Parameters	Specification	Result
DC gain	≥ 63dB	✓67.46 dB
Phase Margin(PM)	≥ 65	✓ 73
Output Swing	Top gain : 3363 Bottom gain : 3063	✓Top gain : 3363 ✓Bottom gain : 3064
Unit Gain Bandwidth	≥ 170 MHz	✓ 196 MHz
Slew Rate	≥ 80 V/us	✓ 155 V/us
Power Consumption	Try to optimize	✓ 0.853 mW

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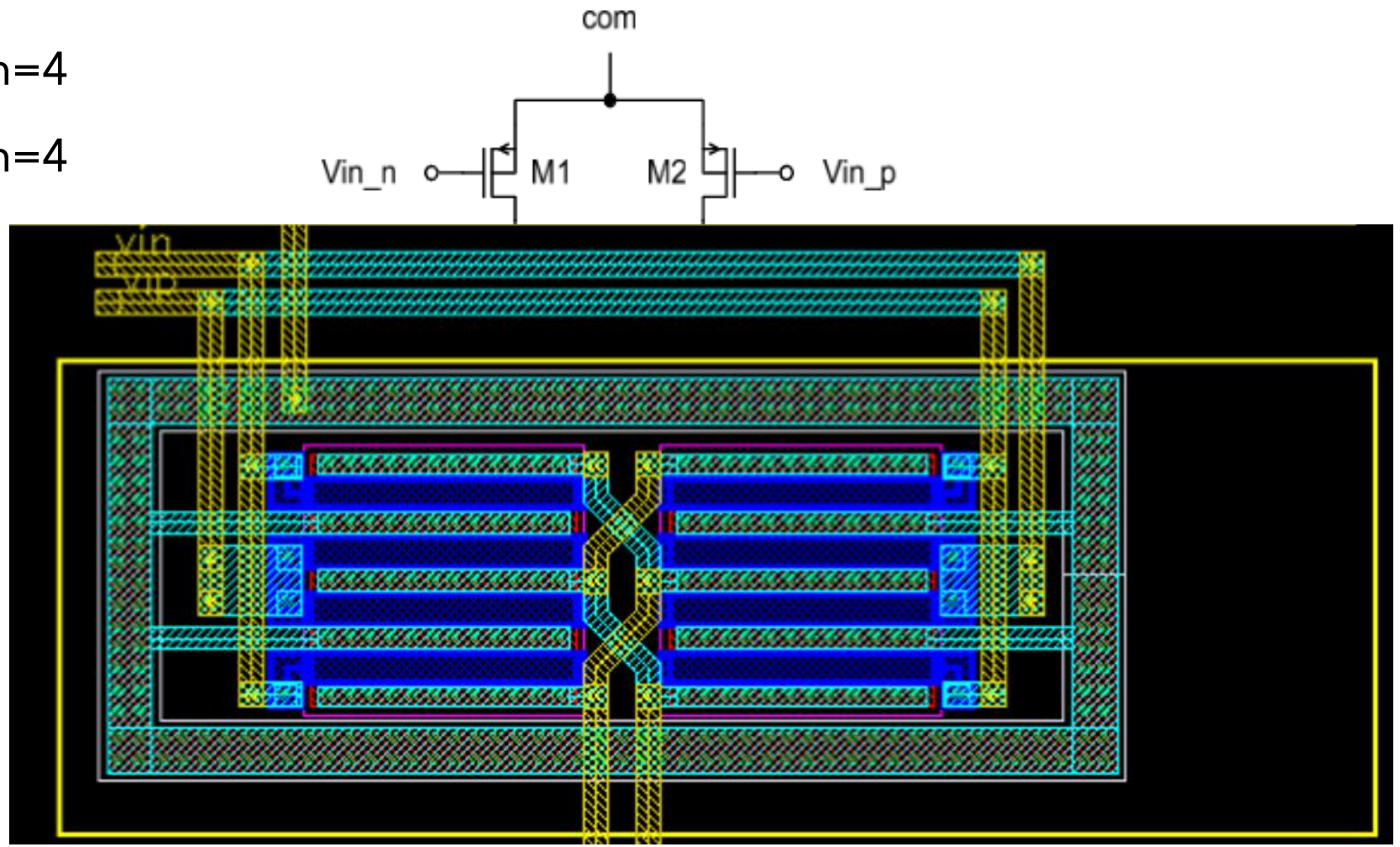
- OPAMP LAYOUT CONSIDERATIONS AND PLACEMENT METHODS

  - Stage 1 - Differential Pair
  - Stage ½ - M3, M4 and M7
  - Stage ½ - Current Sources
  - Stage 2 – M16 Compensation

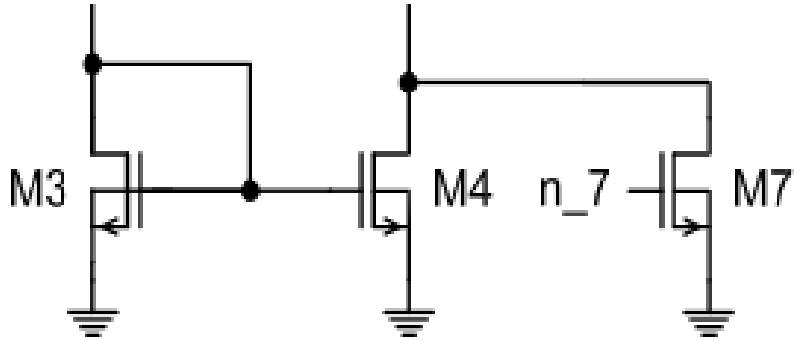
STAGE 1
LAYOUT OF DIFFERENTIAL PAIR

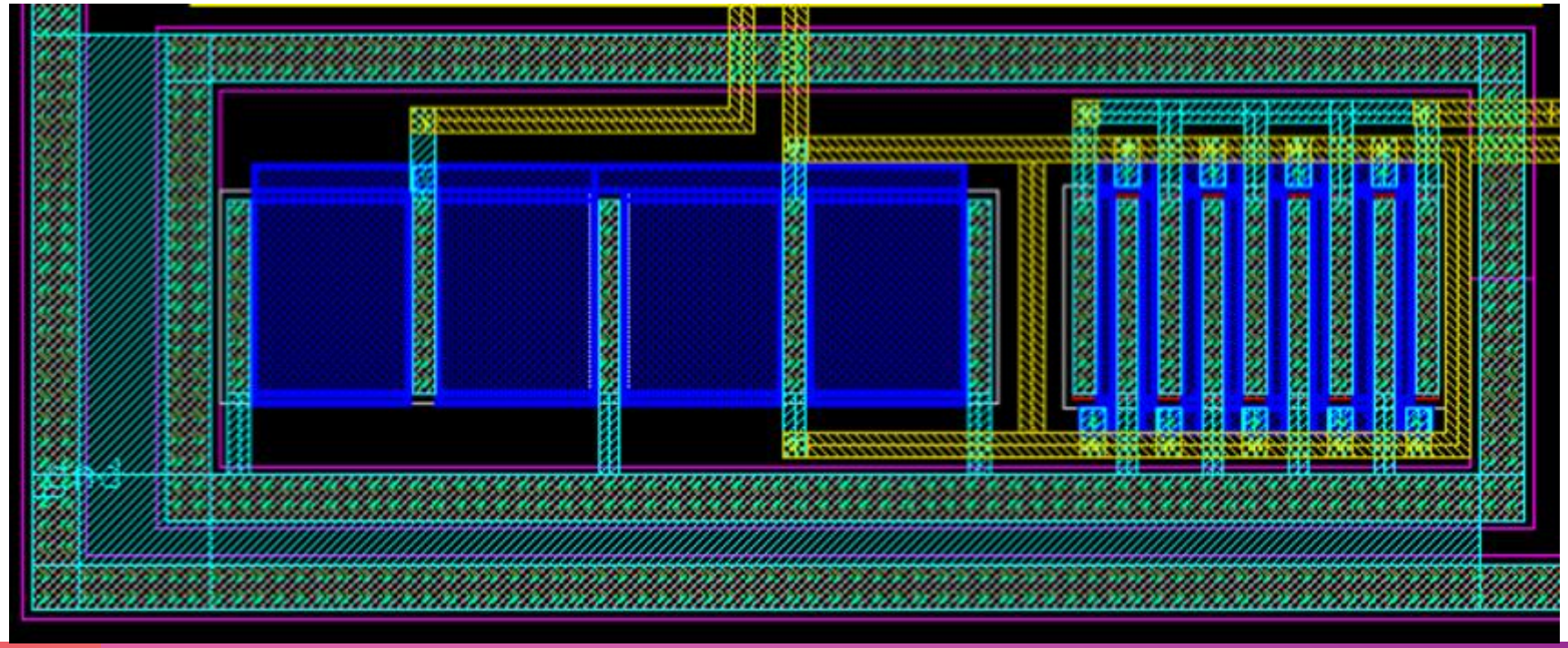
- M1 W=6.06um L=0.68um m=4
- M2 W=6.06um L=0.68um m=4



STAGE 1/2
LAYOUT OF M3, M4 AND M7

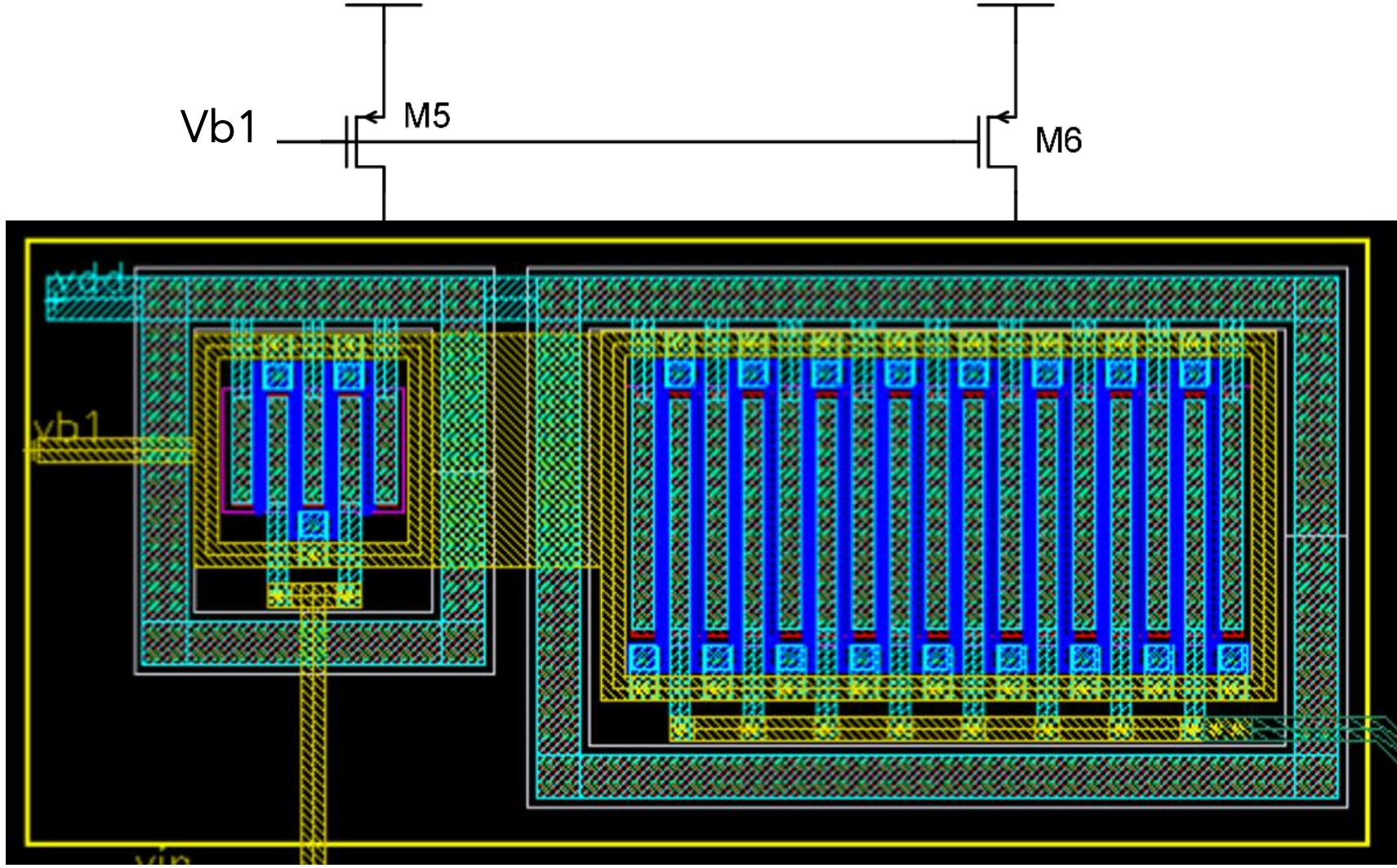
- M3 W=4.37um L=3.5um m=2
- M4 W=4.37um L=3.5um m=2
- M7 W=4.60um L=0.31um m=8





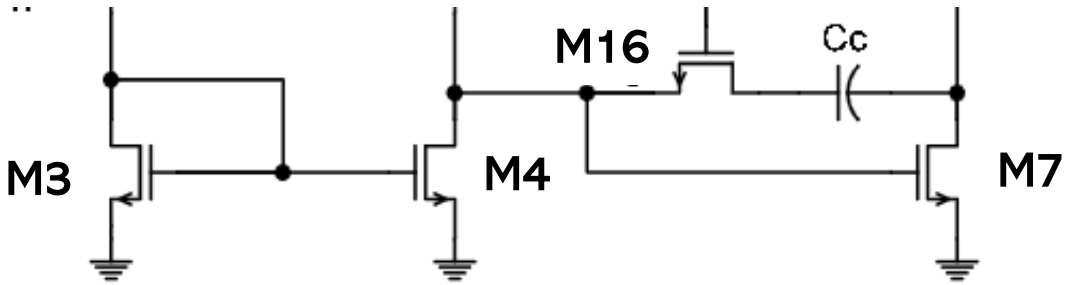
STAGE 1/2
LAYOUT OF CURRENT SOURCES

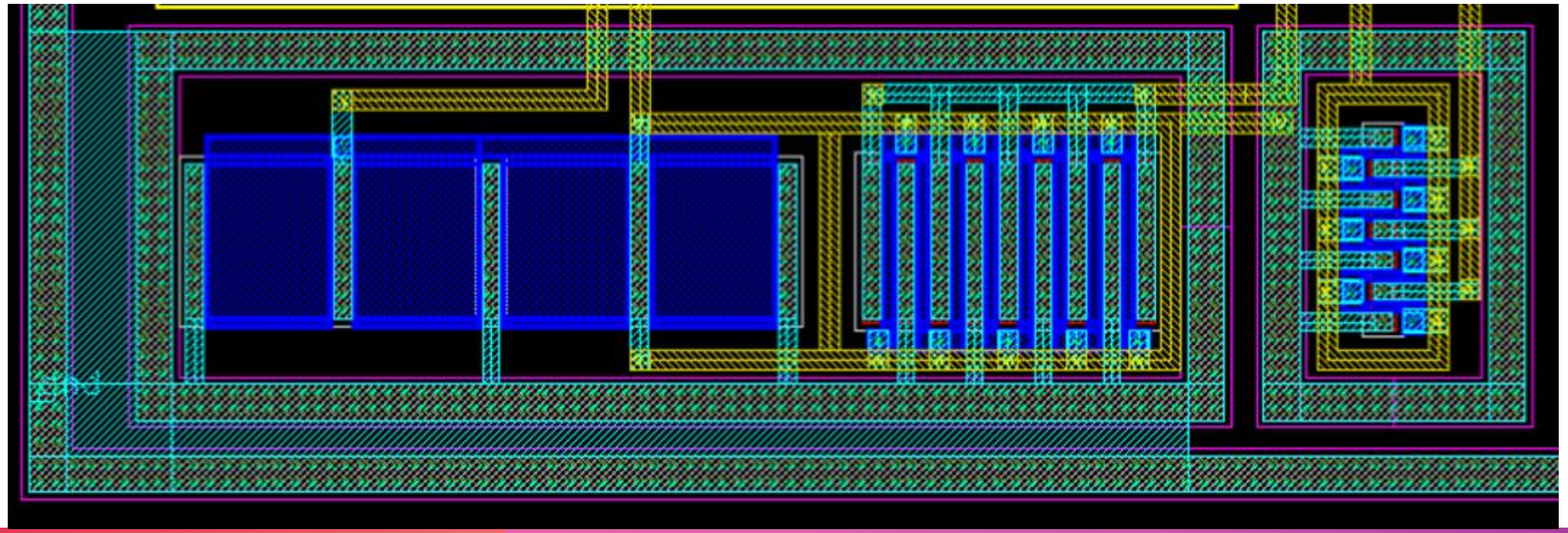
- M5 W=2.48um L=0.18um m=4
- M6 W=5.6um L=0.2um m=16



STAGE 2
LAYOUT M16 COMPENSATION

- M16 W=0.75um L=0.21um m=6





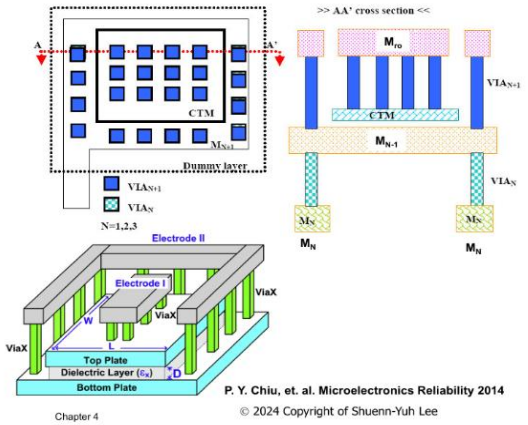
• OPAMP LAYOUT CONSIDERATIONS AND PLACEMENT METHODS : COMPENSATION

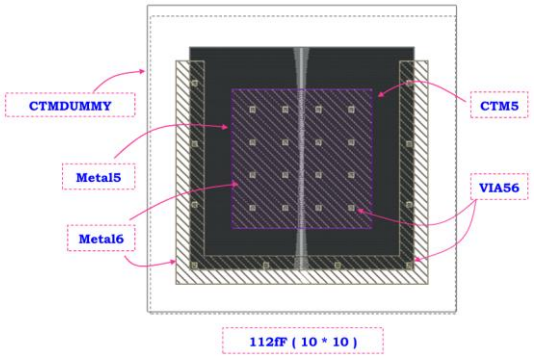
C≈CS.N (with C=0.25pf and N=4)$C \approx CS.N$ $with$ C=0.25pf and N=4

- We use MIM capacitor with value is 0.25pF, and we divided it into 4 capacitors with a value of 0.0625pF connected in parallel.
- To create a capacitor, we went to Create --> Capacitor and entered the value of 0.0625pF to create a capacitor.
- Then we noticed that this capacitor did not have the Metal6 and MIMDUM layers, so we removed the Metal5 layer on top and also deleted the VIA5 layer.

We created a MIMDUM layer of the same size as the underlying Metal5 layer.

- Next, we created a CTM and Metal6 layer of the same size and created a VIA5 to connect the Metal6 layer down to the Metal5 layer.



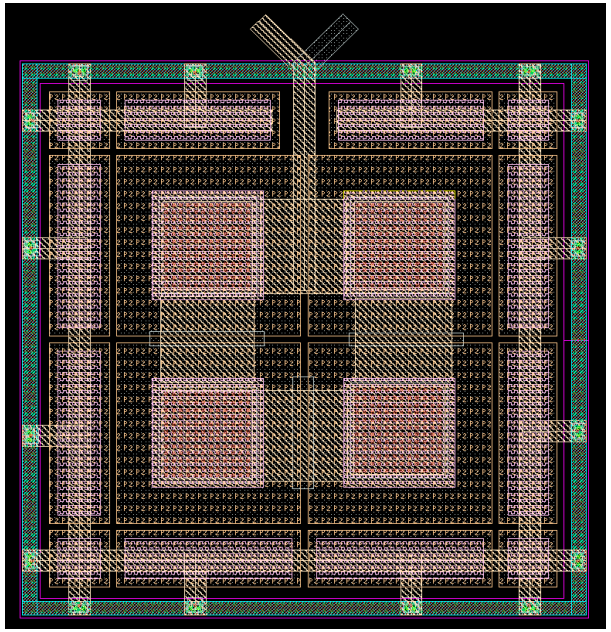


• OPAMP LAYOUT CONSIDERATIONS AND PLACEMENT METHODS: COMPENSATION

Copied the sample capacitor into 4 different capacitors and connected Metal5/Metal6 wires to link these capacitors.

Created a Dummy Cell with smaller capacitors. We created a P-guard ring on the outer layer, then created a Metal5 and Metal6 path from the Dummy to the P-guard ring. We created a VIA from Metal6 down to Metal5 and straight down to the P-sub layer

Connected the Metal5 and Metal6 wires from the capacitors to the outside to connect to the remaining parts of the Op Amp.



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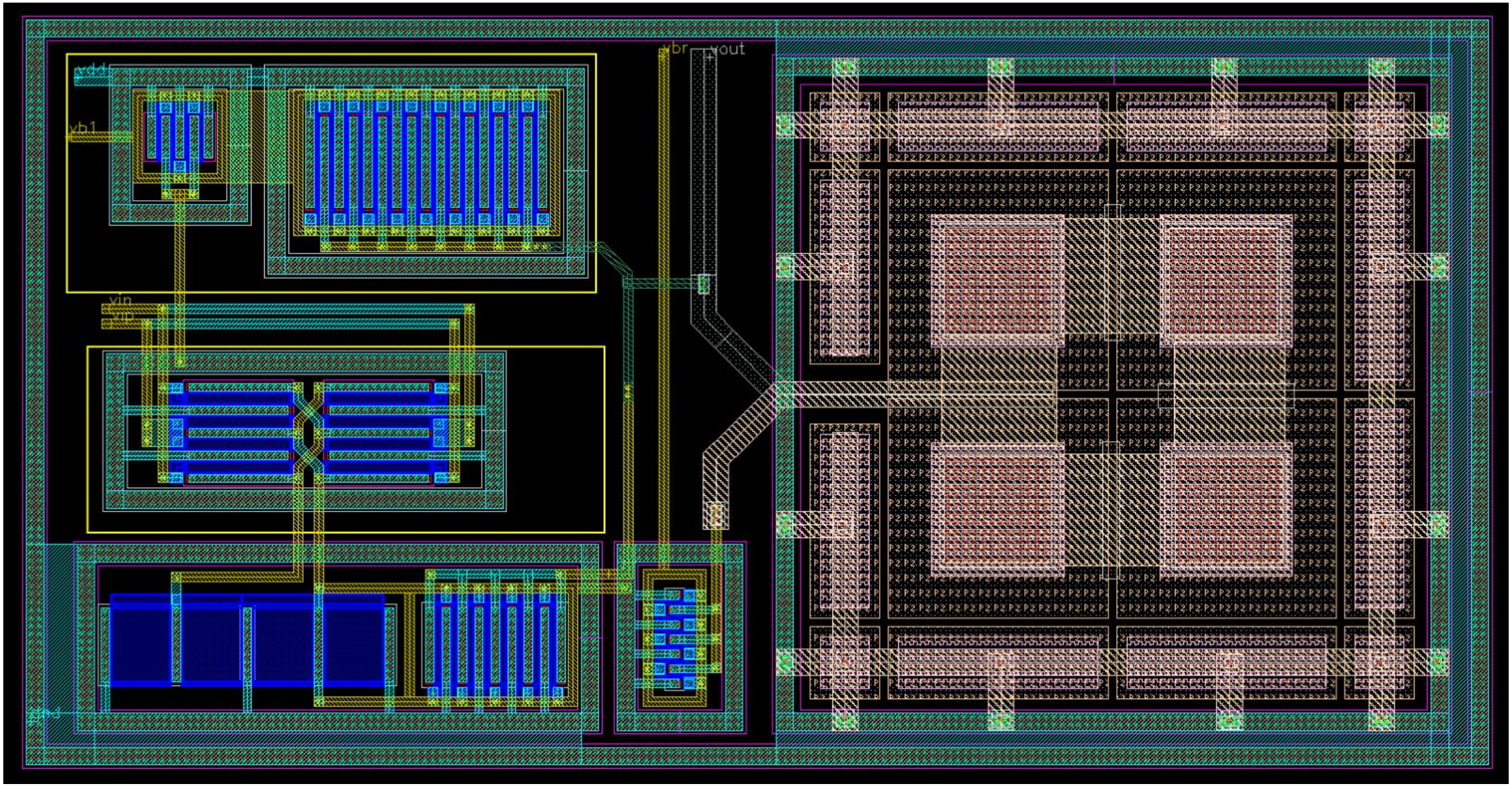
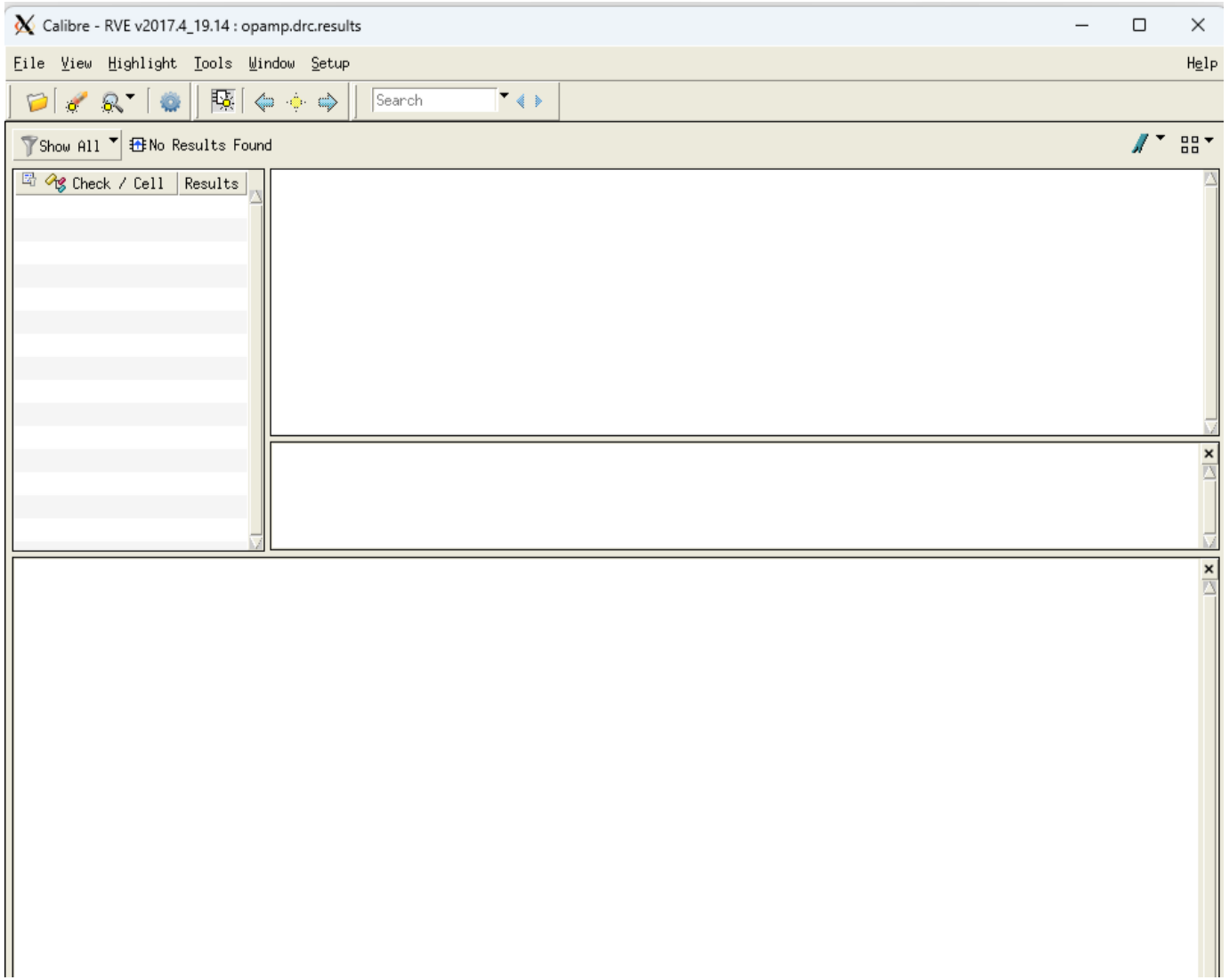
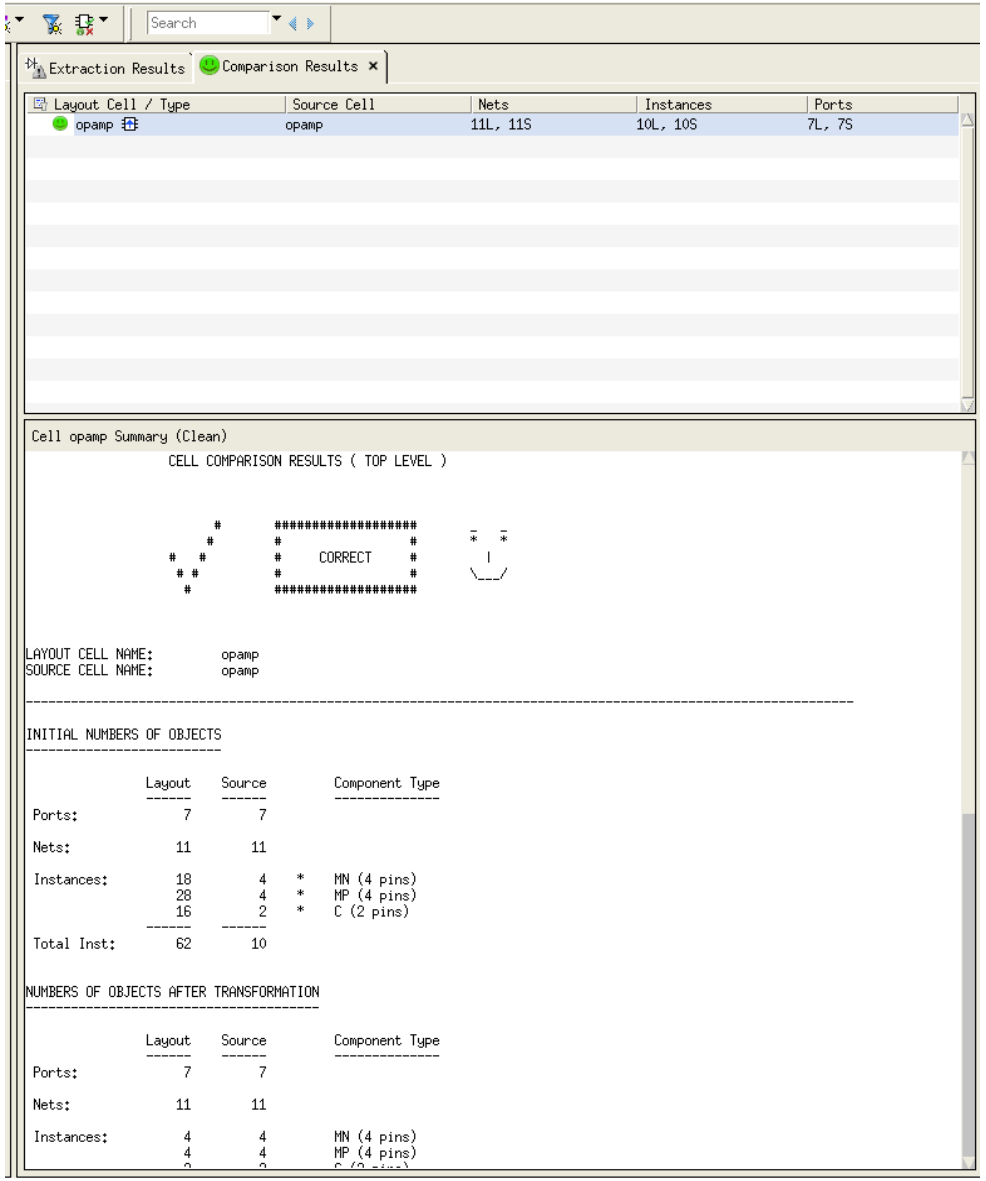
OPAMP LAYOUT DIAGRAM



OPAMP Layout Post-simulation results : DRC all pass and LVS pass





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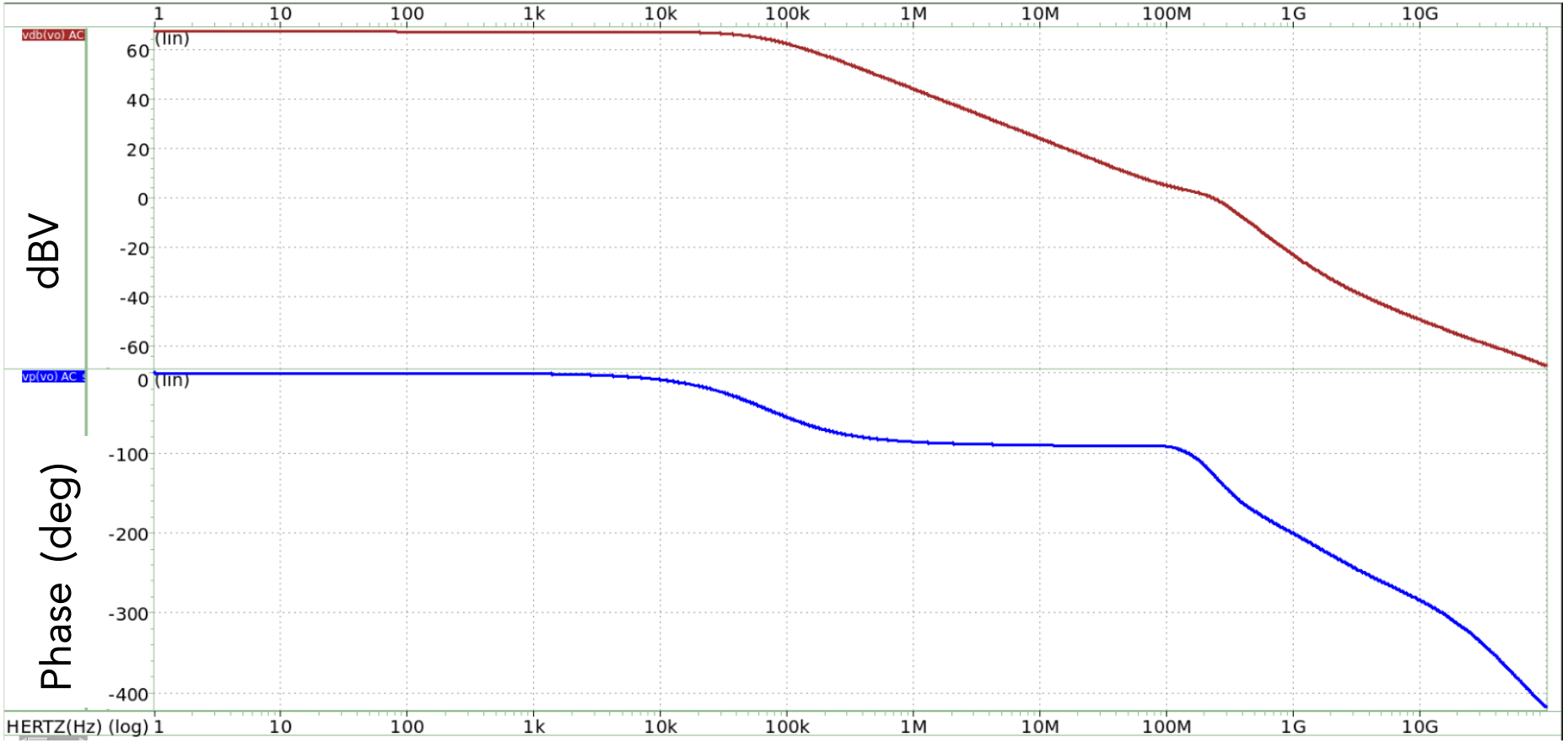
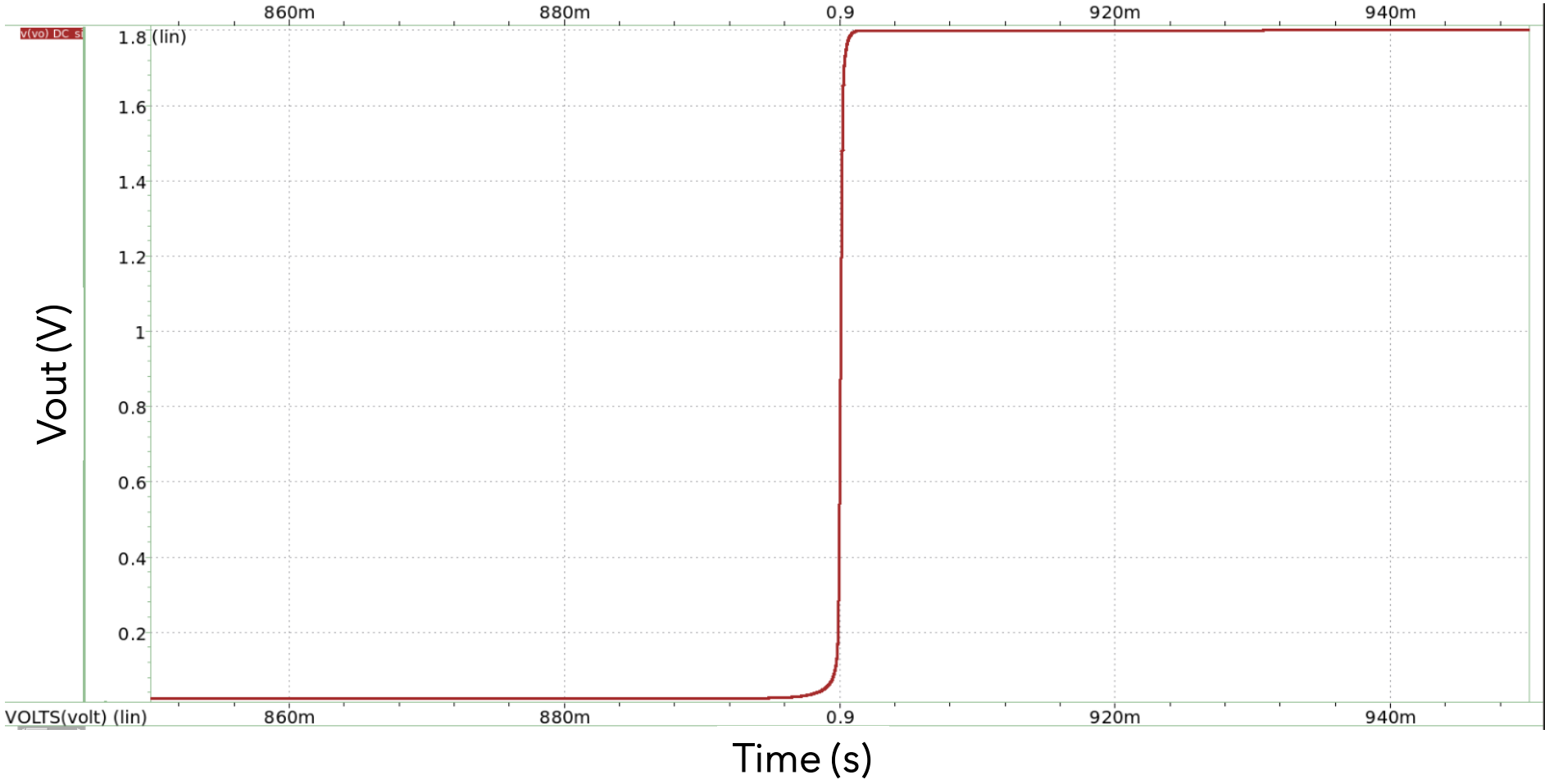
OPAMP AC Post-layout simulation results:



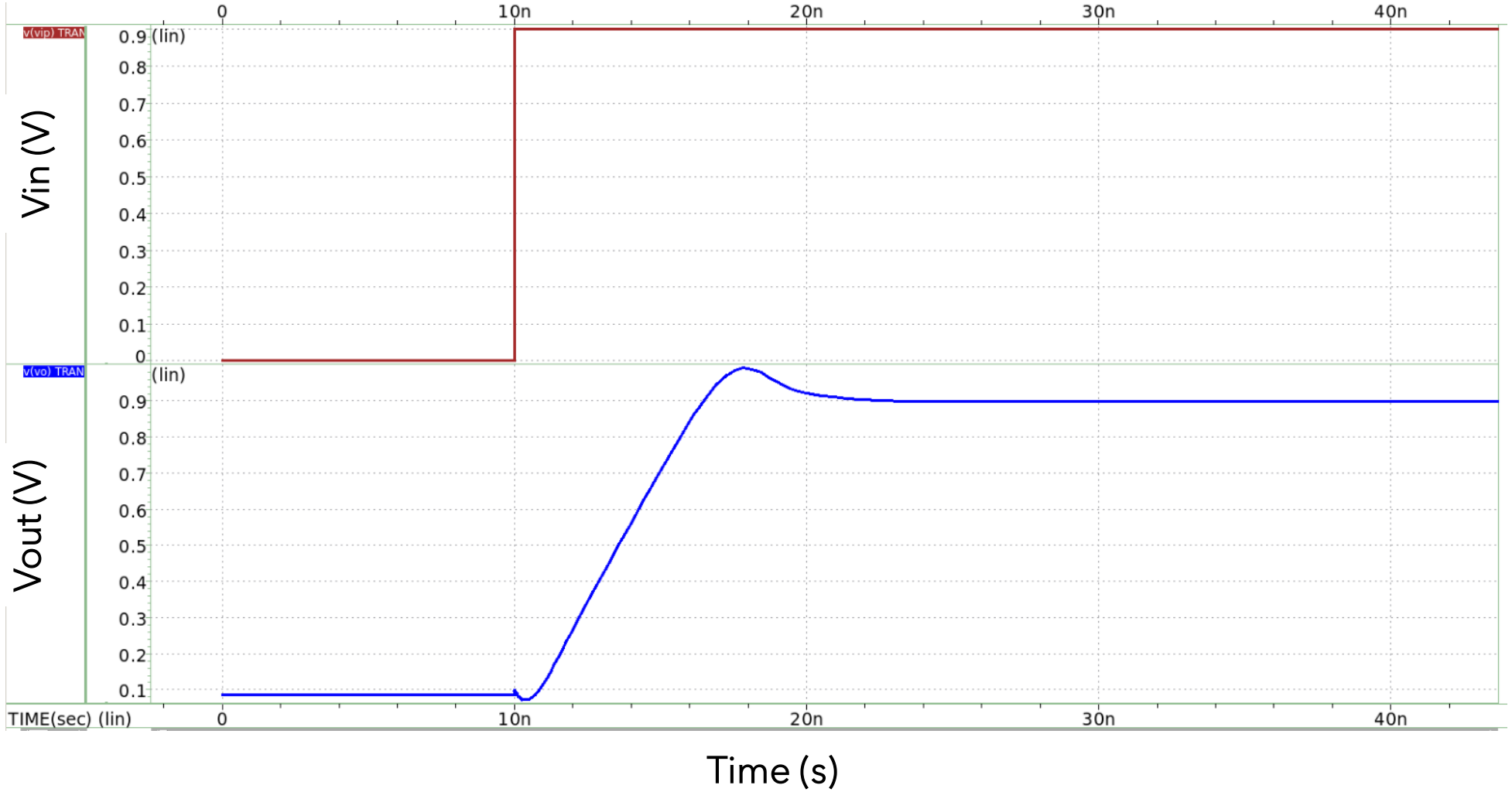
gain	gbw	phase	phase_margin
power_avg	temper	alter#	
67.2213995861	2.323747172e+08	-125.7856991286	54.2143008714
8.808402761e-04	27.0000000000	1	

OPAMP DC post-layout simulation:



top_gain	bottom_gain	power_avg	temper
alter#			
3.576785135e+03	3.082900027e+03	5.258342869e-04	27.0000000000

OPAMP Transient Post-layout simulation results:



sr_rate	power_avg	temper	alter#
1.518298394e+08	8.216712935e-04	27.0000000000	1

OPAMP PRE-SIMULATION RESULTS

Parameters	Specification	Result
DC gain	≥ 63dB	✓67.46 dB
Phase Margin(PM)	≥ 65	✓ 73
Output Swing	Top gain : 3363 Bottom gain : 3063	✓Top gain : 3363 ✓Bottom gain : 3064
Unit Gain Bandwidth	≥ 170 MHz	✓ 196 MHz
Slew Rate	≥ 80 V/us	✓ 155 V/us
Power Consumption	Try to optimize	✓ 0.853 mW

ALL RESULTS

Parameters	Specification	Pre-layout	Post-layout
DC gain (dB)	≥ 63	67.46	67.22
Output Swing	Top gain : 3363 Bottom gain : 3063	Top gain : 3363 Bottom gain : 3063	Top gain : 3576 Bottom gain : 3082
Unity Gain Bandwidth (MHz)	≥ 170	196	232
Slew Rate (V/us)	≥ 80	155	151
Power Consumption (mW)	Try to optimize	0.853	0.881
Phase Margin (°)	≥ 65	73.2	54.1
Layout Area	Try to optimize	N/A	85.825um X 44.039um

DISCUSSION OPAMP POST-LAYOUT RESULTS

Parameters	Pre-layout	Post-layout
DC gain	67.46dB	67.22 dB
Phase Margin(PM)	73	54
Output Swing	Top gain : 3363 Bottom gain : 3063	Top gain : 3576 Bottom gain : 3082
Unit Gain Bandwidth	196 MHz	232 MHz
Slew Rate	155 V/us	151 V/us
Power Consumption	0.853 mW	0.88 mW

The Bandwidth value increases significantly, but the Phase Margin decreases. This can be explained as follows. Parasitic Capacitance and Inductance: The layout introduces parasitic elements such as capacitance and inductance due to the physical interconnections between components.

These parasitic effects can vary the frequency response of your circuit. Increased parasitic capacitance can lead to a reduction in phase margin by introducing additional phase lag, but it can also increase the bandwidth if it changes the poles and zeros of the system.

Other parameters do not change significantly between pre-sim and post-sim.

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- # CONCLUSION

Not bad for our first time learning analog electronic circuit layout!
This course provided a fruitful learning environment.
<u>Better to make our mistakes here than in a real tape out!</u>

Points to improve:

- In our workflow, always allow for extra time to tune the layout according to post-layout simulation results:
- We could have optimized the compensation region of the layout to meet the specified phase margin of 65 deg.
- Chip layout area should be a higher priority since it drastically affect cost
- Power consumption should be a higher priority as this is a main concern for end users.

ACNOWLEDGEMENTS

Yi-Ting Hsieh

Ming-Yueh Ku

Jia-Jun Liu

Prof. Shuenn-Yuh Lee

QUESTIONS?