Academy of Innovative Semiconductor and Sustainable Manufacturing

ANALOG INTEGRATED CIRCUIT DESIGN AND LAYOUT LAB

LAYOUT AND POST-LAYOUT SIMULATION

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Group: B1

LAB3-1. INVERTER LAYOUT

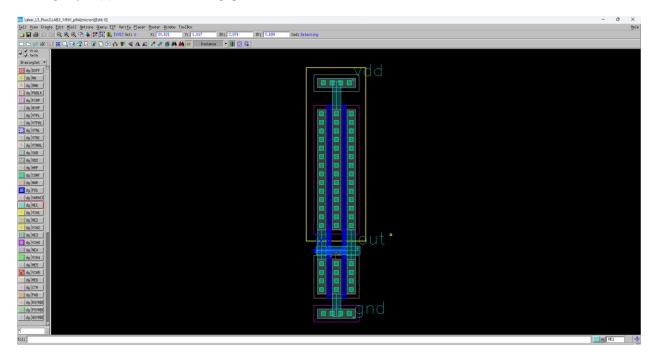


Figure 1. Full Layout

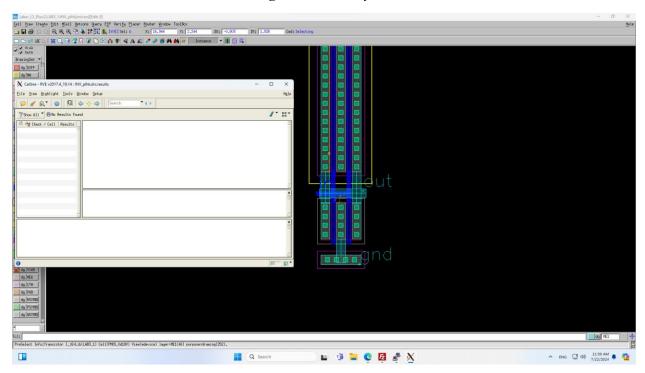


Figure 2. DRC

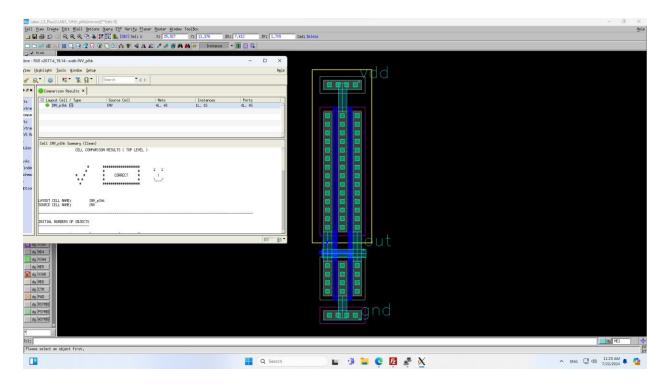


Figure 3. LVS

```
INV_plhk.pex.netlist
                    LAB2_1_4.sp
* File: INV plhk.pex.netlist
* Created: Mon Jul 22 11:33:52 2024
* Program "Calibre xRC"
* Version "v2017.4_19.14"
.include "INV_plhk.pex.netlist.pex"
.subckt INV plhk GND VDD OUT IN
* IN
        TN
* 0UT
        0UT
* VDD
        VDD
* GND
        GND
MO N_GND_MO_d N_IN_MO_g N_OUT_MO_s N_GND_MO_b N_18 L=1.8e-07 W=2e-06 AD=6.5e-13
+ AS=1.12e-12 PD=6.5e-07 PS=3.12e-06
M1 N_GND_M1_d N_IN_M1_g N_OUT_M1_s N_GND_M0_b N_18 L=1.8e-07 W=2e-06 AD=6.5e-13
+ AS=1.12e-12 PD=6.5e-07 PS=3.12e-06
M2 N_VDD_M2_d N_IN_M2_g N_OUT_M2_s N_VDD_M2_b P_18 L=1.8e-07 W=6.8e-06
+ AD=2.21e-12 AS=3.808e-12 PD=6.5e-07 PS=7.92e-06
M3 N_VDD_M3_d N_IN_M3_g N_OUT_M3_s N_VDD_M2_b P_18 L=1.8e-07 W=6.8e-06
+ AD=2.21e-12 AS=3.808e-12 PD=6.5e-07 PS=7.92e-06
.include "INV_plhk.pex.netlist.INV_PLHK.pxi"
.ends
```

Figure 4. File PEX

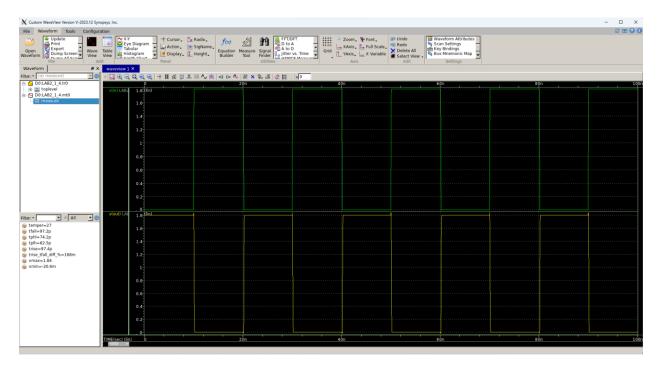


Figure 5. Output Waveform

```
*****
* testbench for mos characteristic *
***** transient analysis tnom= 25.000 temp= 27.000 *****
      1.839554
                  at= 10.033833n
                  0.
                               to= 100.000000n
           from=
                                                                 SPEC
vmin= -19.702757m
                  at= 40.131790n
                              to= 100.000000n
           from=
trise= 94.722757p targ= 40.263272n
                                           40.168550n
                                    trig=
tfall= 94.210498p targ= 30.169511n
                                    trig=
                                           30.075301n
trise_tfall_diff_%= 542.264698m
tplh= 55.191856p targ= 20.205192n trig= 20.150000n
                                   trig= 30.050000n
tphl= 68.767887p targ= 30.118768n
```

Figure 6. Spec Lab2 1 4

Comment:

When comparing the Spec results with the layout results, the Trise and Tfall of the layout results are larger than those in the Spec. This increases the delay time, which is not good for the Inverter circuit. The decrease in the trise_tfall_diff value indicates the symmetry of the transition time from high to low and vice versa.