

**Academy of Innovative Semiconductor and Sustainable Manufacturing**

**ANALOG INTEGRATED CIRCUIT DESIGN AND LAYOUT LAB**

**LAYOUT AND POST-LAYOUT SIMULATION**

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## LAB3-1. INVERTER LAYOUT

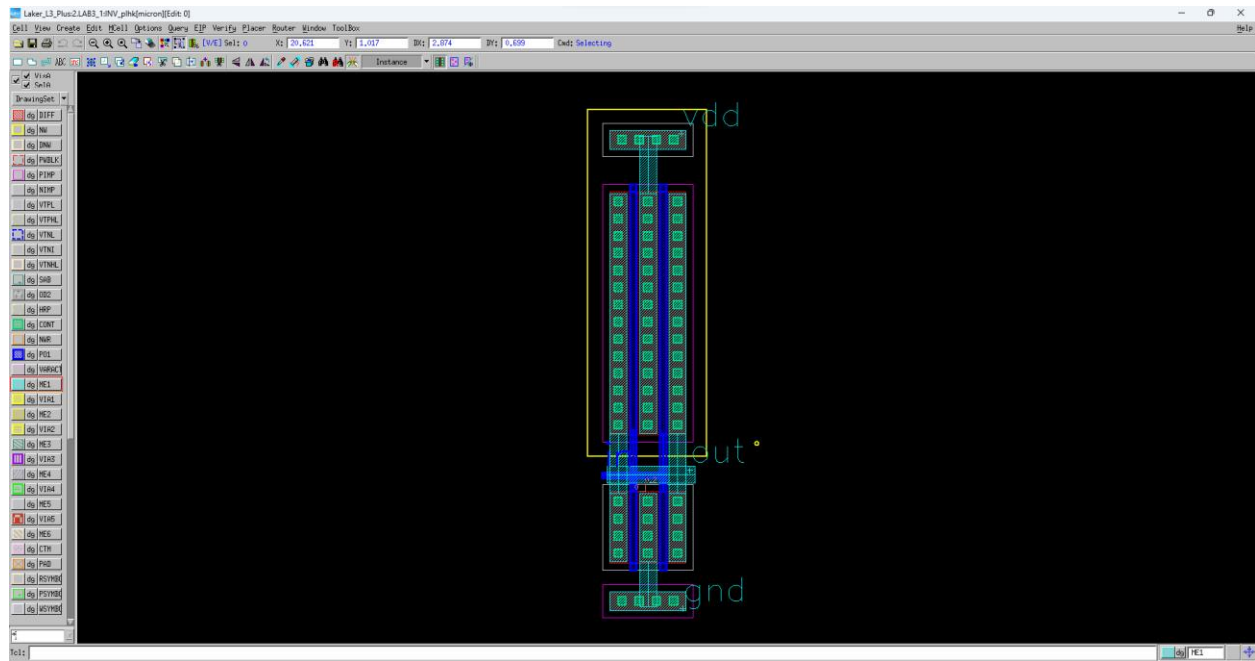


Figure 1. Full Layout

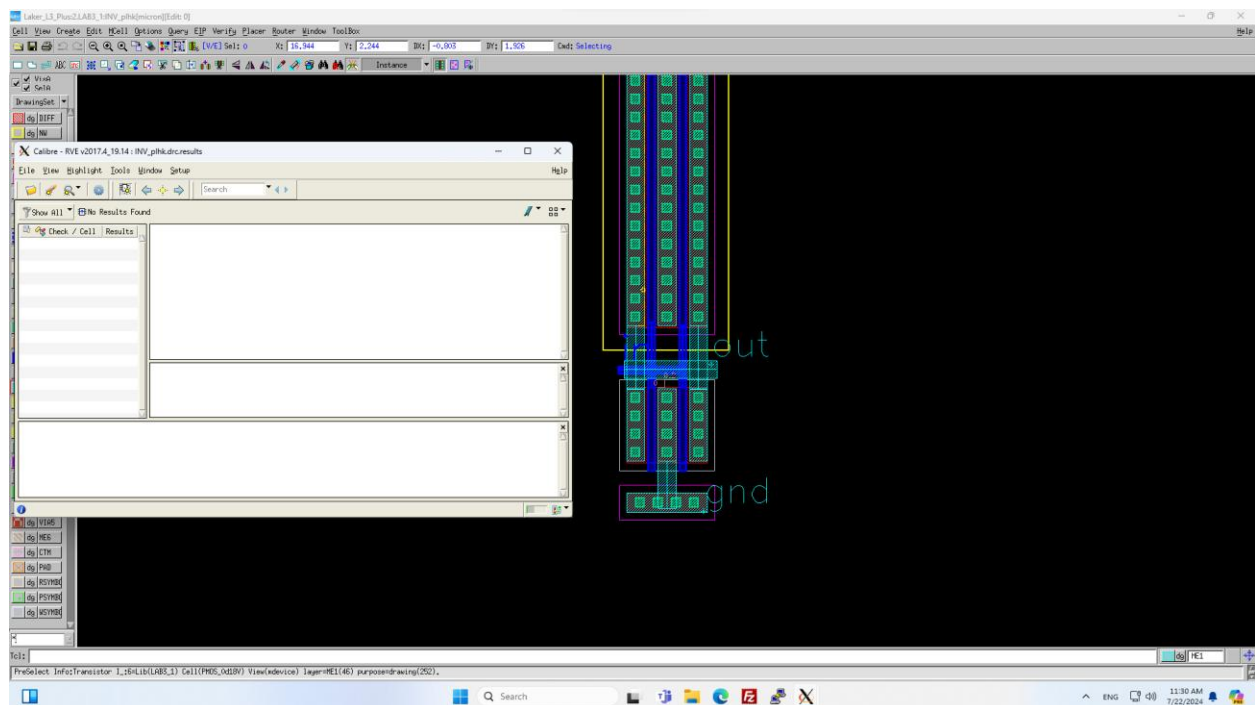


Figure 2. DRC

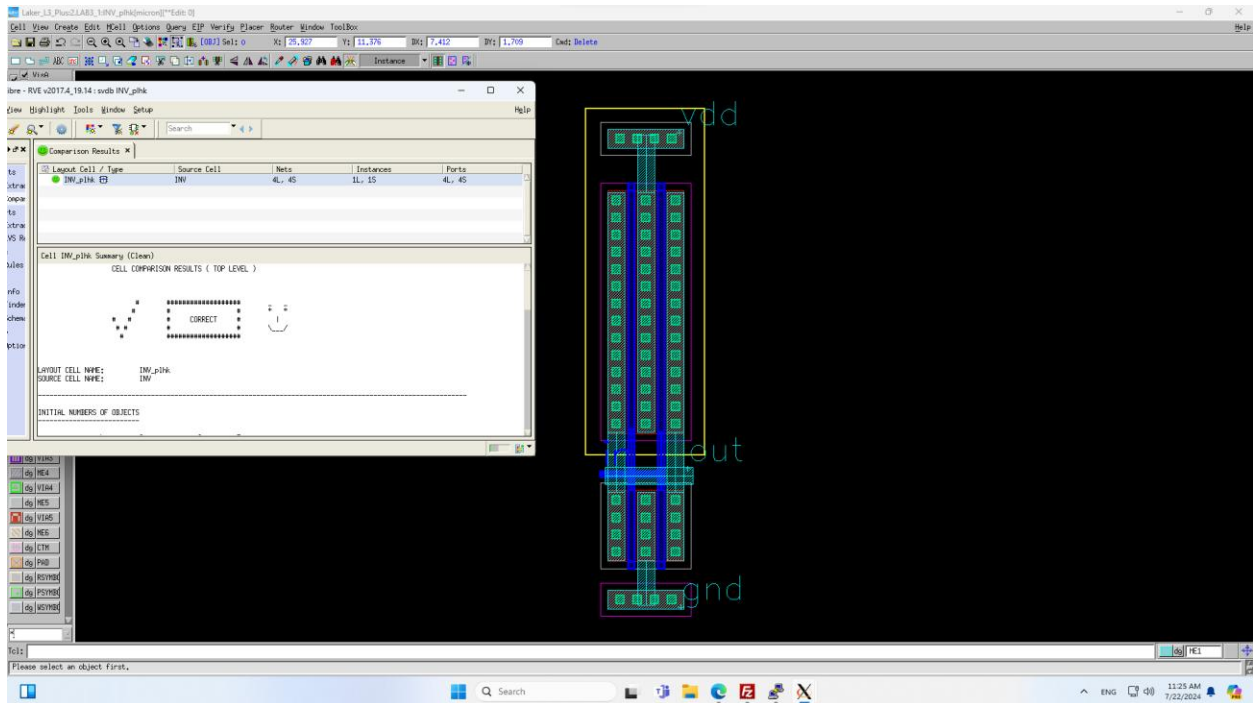


Figure 3. LVS

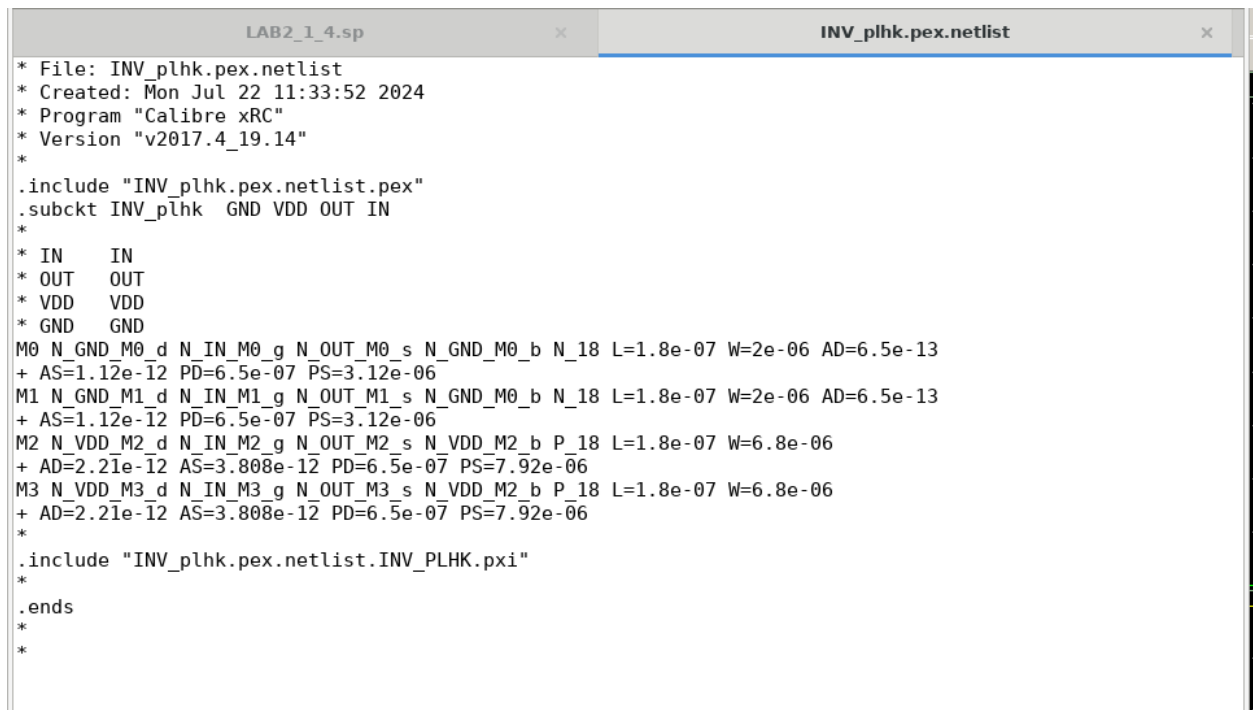


Figure 4. File PEX

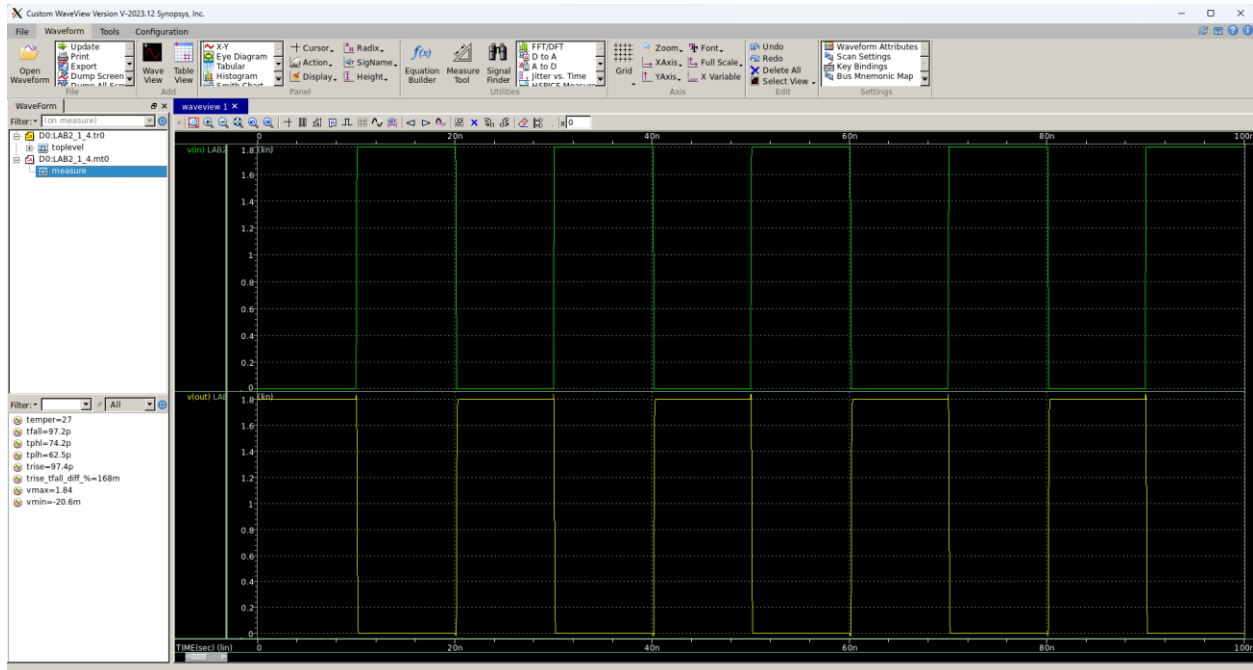


Figure 5. Output Waveform

```
*****
* testbench for mos characteristic *

***** transient analysis tnom= 25.000 temp= 27.000 *****
vmx= 1.839554 at= 10.033833n
      from= 0. to= 100.000000n
vmin= -19.702757m at= 40.131790n
      from= 0. to= 100.000000n
trise= 94.722757p targ= 40.263272n trig= 40.168550n
tfall= 94.210498p targ= 30.169511n trig= 30.075301n
trise_tfall_diff_%= 542.264698m
tplh= 55.191856p targ= 20.205192n trig= 20.150000n
tphl= 68.767887p targ= 30.118768n trig= 30.050000n
```

**SPEC**

Figure 6. Spec Lab2\_1\_4

### Comment:

When comparing the Spec results with the layout results, the Trise and Tfall of the layout results are larger than those in the Spec. This increases the delay time, which is not good for the Inverter circuit. The decrease in the trise\_tfall\_diff value indicates the symmetry of the transition time from high to low and vice versa.

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