FARADAY

PHASE-LOCKED LOOP

FXPLL357HN0U
UMC 22 nm Logic and Mixed-Mode Process

Data Book

Rev.: 0.6
Issue Date: July 2021

REVISION HISTORY

FXPLL357HN0U Data Book

Date	Rev.	From	To
Aug. 2019	0.1	-	Original
Nov. 2019	0.2	-	Updated the IP version to (0.2.0)
Aug. 2020	0.3	-	Updated the IP version to (0.3.0)
Sept. 2020	0.4	-	Updated the IP version to (0.4.0)
May 2021	0.5	-	Updated the IP version to (0.5.0)
Jul. 2021	0.6	-	• Updated the IP version to (0.6.0) • Updated Section 1.2 and Section 4.1 • Updated **Table 1-1**, **Table 4-1**, and **Table 4-3**

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PREFACE

Data Book Organization

This data specification is organized as follows:
Chapter 1: **PLL Overview**, provides an introduction to the intellectual Property (IP) and its features.
Chapter 2: **PLL Architecture**, provides a high-level description of the IP block.
Chapter 3: **PLL Signal Descriptions**, describes the Input Output (IO) signals of the IP.
Chapter 4: **PLL Electrical Specifications**, describes the electrical specification met by the IP.
Chapter 5: **PLL Power Supply and Power Management**, describes the power sequence as well as the power sequencing used inside the IP.
Chapter 6: **PLL Testing**, describes the detailed information on the testing features provided for the IP.
Chapter 7: **PLL Integration**, describes the pad/package board requirements and integration guidelines.
Chapter 8: **Verilog Functional Verification**, provides the detailed information of the RTL model and how to run the functional simulation.

Version of the IP

IP release version: 0.6.0

Web Resources

For the detailed information of web resources, please contact the Faraday customer service team for further assistance.

Reference Documentation

There is no reference document at this release.

Customer Support

For the detailed information of support issues, please contact the Faraday customer service team for further assistance.

Terminology/Glossary

Term	Definition
ASIC	Application-Specific Integrated Chip
ESD	Electrostatic Discharge
GDSII	Graphic Database System II
IO	Input Output
LPF	Low-Pass Filter
PLL	Phase-Locked Loop
RTL	Register Transfer Level
VCO	Voltage-Controlled Oscillator

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Chapter 1
PLL Overview

This chapter contains the following sections:

1.1 IP Module Configuration

There is no IP module configuration available at this release.

1.2 Features

- UMC 22 nm logic and Mixed-Mode process (SVT, LVT, and IO device used)
- Operating voltage range:
  - 0.72 V ~ 1.05 V for VCC08A
  - 1.62 V ~ 1.98 V for VCC18A
- Operating junction temperature range: -40 °C ~ 125 °C
- Minimum metal requirement: 6 metal layers
- Low-jitter clock output
- Low power consumption
- Built-in loop filter
- No external component required
- FREF input frequency range: 10 MHz ~ 20 MHz
- Internal VCO frequency range: 2500 MHz ~ 5000 MHz
- CKOUT output frequency range: 312.5 MHz ~ 5000 MHz

1.3 Standards

There is no standard information available at this release.

1.4 Operating Conditions

Table 1-1. Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VCC08A	0.72	0.8	1.05	V
VCC18A	1.62	1.8	1.98	V
Temperature	-40	25	125	°C

1.5 Process Technology

Table 1-2. Process Technology

Parameter	Value
Foundry	UMC
Technology node	22 nm
Metal option	6M (1P6M)
Devices	SVT, LVT, IO
Packaging	-

Chapter 2
PLL Architecture

This chapter contains the following sections:

2.1 Functional Block Diagram

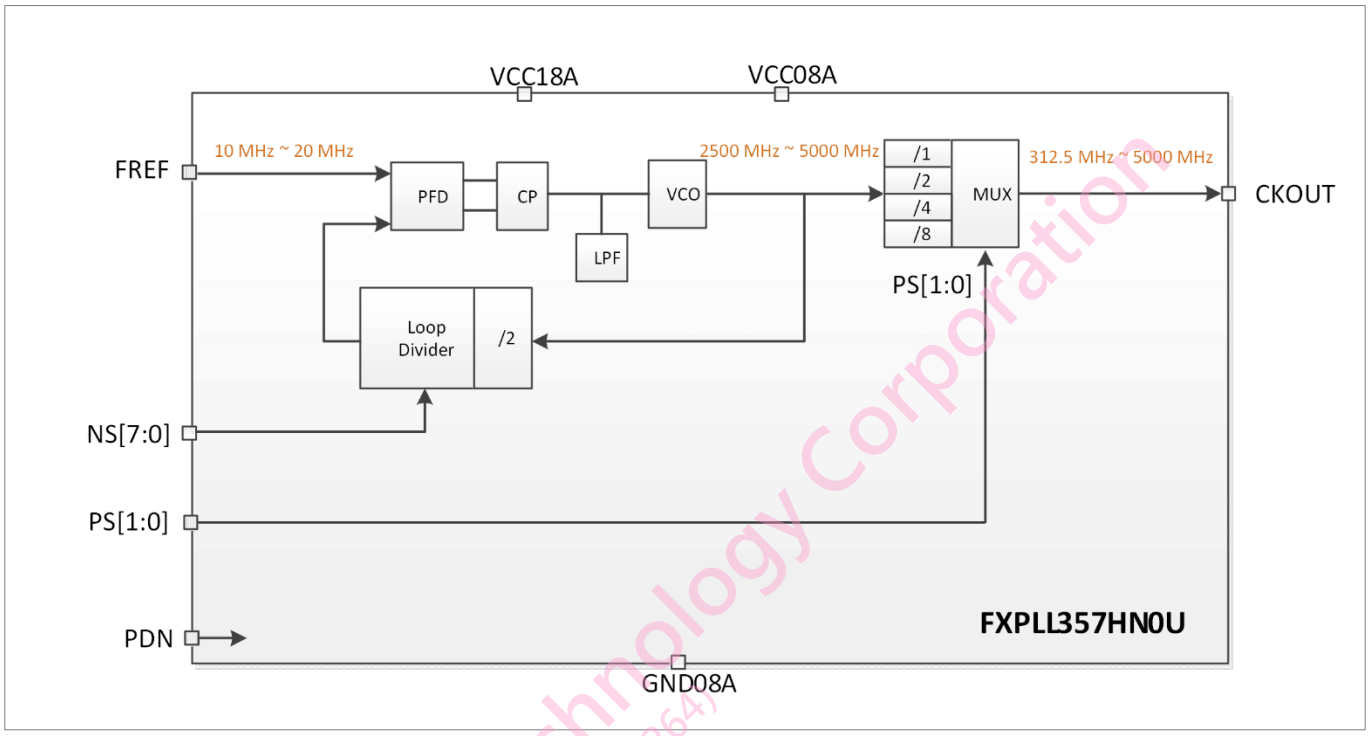

Figure 2-1. Functional Block Diagram

FXPLL357HN0U is a Phase-Locked Loop (PLL) circuit that is used to generate the high-speed clock with an operating frequency up to 5000 MHz. This PLL is designed by using the UMC 22 nm logic and Mixed-Mode process. It can be integrated into a chip to generate an accurate clock. The loop divider allows users to boost the output frequency up to 5000 MHz. FXPLL357HN0U supports an operating voltage ranging from 0.72 V to 0.88 V for VCC08A and 1.62 V to 1.98 V for VCC18A with an operating junction temperature ranging between -40 °C and 125 °C. FXPLL357HN0U can be used for high-frequency multiplications.

2.1.1 PFD (Phase-Frequency Detector)

This block compares the phase differences between the output signals of pre-divider and loop divider. Based on these signals, the PFD block will then generate the control signals to be used by the charge pump.

2.1.2 CP (Charge Pump)

This block utilizes the control output signals generated by the PFD block to determine whether to charge or discharge on LPF.

2.1.3 LPF (Low-Pass Filter)

This block cooperates with the charge pump to convert the current to voltage to be used by the VCO block.

2.1.4 VCO (Voltage-Controlled Oscillator)

This block generates the output clock frequency according to the voltage level that is received from the LPF block. Faraday high-performance VCO can supply a stable output clock signal with a very low jitter value.

2.1.5 Divider (Loop Divider/Post Divider)

These blocks are used to generate the desired output clock frequency.

2.2 Timing Parameters

Please refer to Section 5.2 for more detailed information.

2.3 Application Circuit

PLL is inherently sensitive to noise. The noise on PLL_VCC will cause phase jitter at the PLL output. To provide isolation from the noisy internal logic VCC signal, the PLL_VCC and PLL_GND signals are connected to a pair of the dedicated package pins.

In order to minimize the on-board VCC and ground noise, an adequate chip decoupling capacitor for the high-frequency noise and low-frequency noise must be used, as shown in **Figure 2-2**. It is recommended that users place one minimum capacitor of 0.1 µF as close to each VCC pin as possible. It is also recommended that users minimize the trance length between the ASIC power and bypass capacitor pins.

If little noise is expected at the board level, the PLL_VCC signal can be directly connected to the logic VCC plane. In most cases, however, it is best to place a filter circuit on the PLL_VCC pin, as shown in **Figure 2-3**. All wire lengths should be kept as short as possible to minimize the coupling noise from other signals.

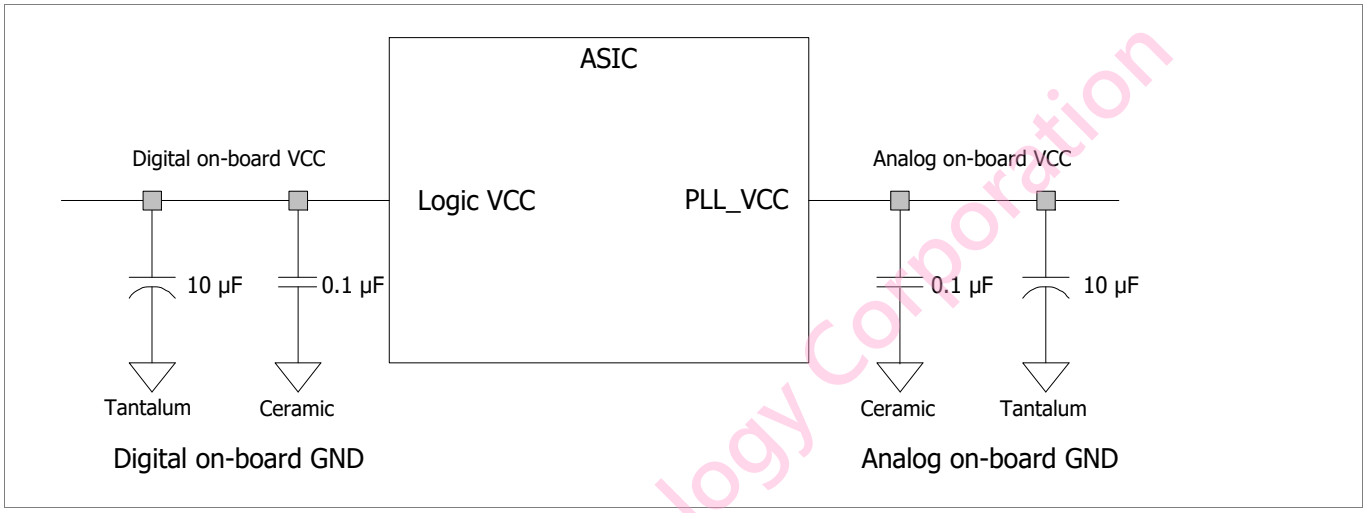

Figure 2-2. Application Circuit (1)

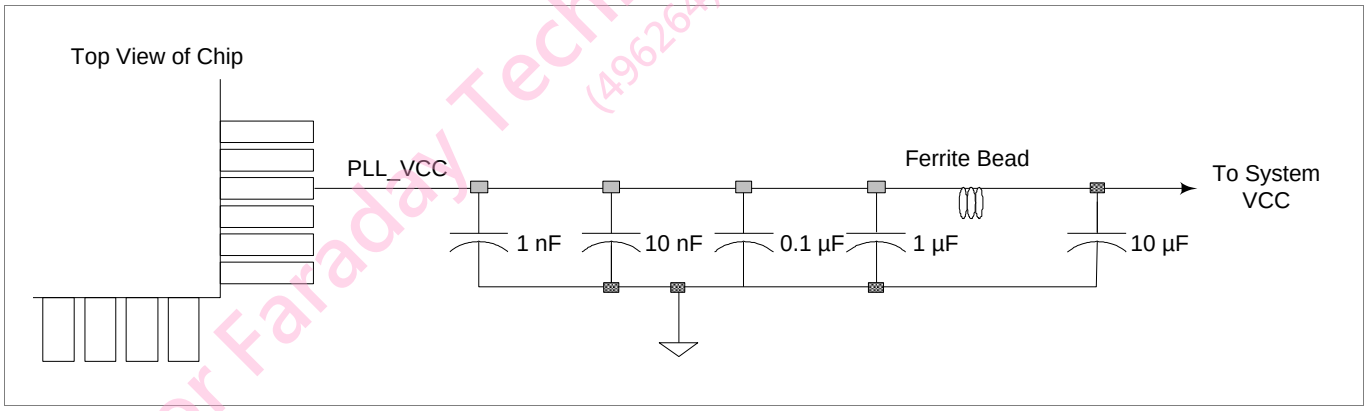

Figure 2-3. Application Circuit (2)

Chapter 3
PLL Signal Descriptions

This chapter contains the following section:

3.1 Pin Descriptions

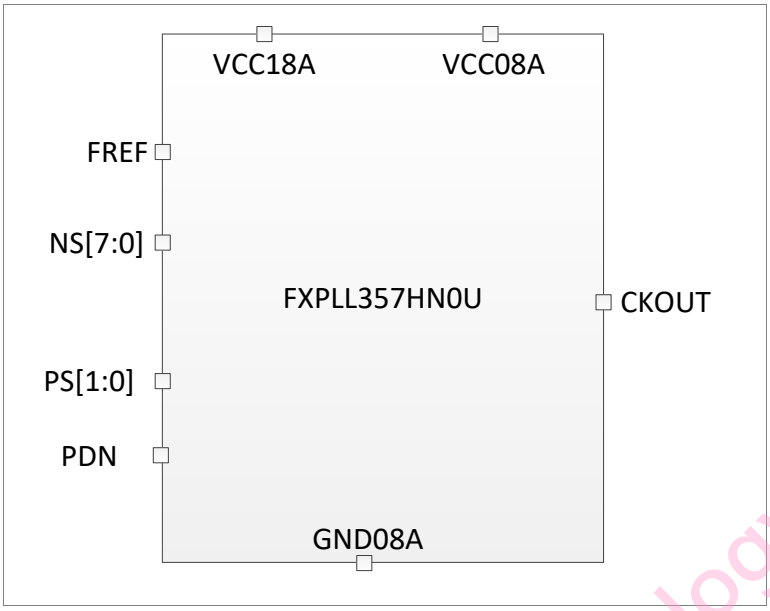

Figure 3-1. PLL Signal Diagram

Table 3-1. Pin Descriptions

Signal	Direction	Description
VCC18A	I	1.8 V analog supply
VCC08A	I	0.8 V analog supply
GND08A	I	Analog ground
FREF	I	Reference input clock 10 MHz ~ 20 MHz
NS[7:0]	I	8 bits for loop divider ratio setting (62 ~ 250)
PS[1:0]	I	2 bits for post divider ratio setting (1/2/4/8) PS[1:0] = 00, PS = 1 PS[1:0] = 01, PS = 2 PS[1:0] = 10, PS = 4 PS[1:0] = 11, PS = 8
PDN	I	Power-down mode setting Active low For IP working correctly, PDN needs a 0 state at initial to reset IP.
CKOUT	O	Output clock Frequency = Fvco/PS

Chapter 4
PLL Electrical Specifications

This chapter contains the following sections:

4.1 Power Noise Electrical Specifications

FXPLL357HN0U supports a DC operating voltage VCC08A in the ranges of 0.8 V ±10%, 0.9 V ±10%, and up to 1.05 V; VCC18A in range of 1.8 ±10%.

FXPLL357HN0U can stand the following power noise specification under the worst-case condition of a real-life environment. Please make sure that ASIC meets the following specifications:

- High-frequency noise (5 MHz ~ 120 MHz): Typical resonance frequency at package and on-die power delivery, known at 1st droop (Amp. max. 35 mVpp)
- Mid-frequency noise (100 kHz ~ 5 MHz): Typical 2nd droop frequency. Please refer to the set that is close to the PLL loop BW to mimic the worst-case condition of a real-life environment (Amp. max. 10 mVpp).
- Low-frequency noise (Around 100 kHz): Typical 3rd droop frequency. From the VR/Board loop (Amp. max. 5 mVpp)

Table 4-1 summarizes the power noise specification as below:

Table 4-1. Power Noise Electrical Specifications

Item	Description	Condition	Min.	Typ.	Max.	Unit
Vdc_{VCC08A}	Power supply DC level	-	0.72	0.8	1.05	V
Vdc_{VCC18A}	Power supply DC level	-	1.62	1.8	1.98	V
Vac	Power supply AC noise	High-frequency	-	-	35	mVpp
		Mid-frequency	-	-	10	mVpp
		Low-frequency	-	-	5	mVpp

4.2 Input FREF Clock Electrical Specifications

The FREF input clock quality is critical to the performance of the PLL output clock. For applications that require a high-quality clock, users should pay attention to the FREF input clock quality.

It is recommended that users use the XO oscillator as input for this IP, and the distance from crystal I/O to the PLL FREF input port should be kept as close as possible. It is recommended that the total FREF input path, including crystal I/O and buffer, should use analog power to reduce FREF clock quality degradation due to buffer power noise.

The final clock to PLL FREF input should meet the specification in **Table 4-2**.

Table 4-2. Input FREF Electrical Specifications

Item	Description	Min.	Typ.	Max.	Unit
Duty	Input clock duty ratio	20	50	80	%
PN	Input clock phase noise At 100 kHz and above offset frequency	-	-	-135	dBc/Hz
J_{PJ}	Period jitter (Peak-to-peak)	-	-	±0.5%	Clock period
J_{LT}	Long-term jitter (Peak-to-peak)	-	-	±2%	Clock period

4.3 PLL Electrical Specifications

The following power consumption values were obtained through simulation. The typical values were obtained at room temperature by using the typical process corner as well as nominal analog and digital power supply levels. The maximum values were obtained through simulation from -40 °C to 125 °C across the process corners and +10% power supply level.

Table 4-3. PLL Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VCC18A	1.8 V Analog supply voltage	-	1.62	1.8	1.98	V
VCC08A	0.8 V Analog supply voltage	-	0.72	0.8	1.05	V
T_J	Operating junction temperature	-	-40	25	125	°C
I_{VCC08A}	VCC08A current consumption	Normal operation (Simulation)	-	1.28	3	mA
		Power-down mode (Simulation)	-	0.015	0.5	mA
I_{VCC18A}	VCC18A current consumption	Normal operation (Simulation)	-	2.93	4.5	mA
ss	-	Power-down mode (Simulation)	-	4e-6	1.5	mA
V_{ih}	Input logic level high	-	90% of VCC08A	-	-	V
V_{il}	Input logic level low	-	-	-	10% of VCC08A	V
FREF	Input clock	-	10	-	20	MHz

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
FREFX	PFD frequency	FREF	10	-	20	MHz
VCOOUT	VCO output frequency	FREFX*NS[7:0]*2	2500	-	5000	MHz
CKOUT	Output clock	VCOOUT/PS	312.5	-	5000	MHz
J_{cc}	Cycle-to-cycle jitter (RMS)	1250 MHz < CKOUT ≤ 2500 MHz	-	12	15	ps
		2500 MHz < CKOUT ≤ 5000 MHz	-	8	10	ps
	Cycle-to-cycle jitter (Peak-to-peak)	1250 MHz < CKOUT ≤ 2500 MHz	-	±40	±50	ps
		2500 MHz < CKOUT ≤ 5000 MHz	-	±25	±30	ps
J_p	Period jitter (RMS)	1250 MHz < CKOUT ≤ 2500 MHz	-	9	12	ps
		2500 MHz < CKOUT ≤ 5000 MHz	-	6	8	ps
	Period jitter (Peak-to-peak)	1250 MHz < CKOUT ≤ 2500 MHz	-	±30	±40	ps
		2500 MHz < CKOUT ≤ 5000 MHz	-	±20	±25	ps
T_{pd} [1]	Reset time	-	5	-	-	µs
T_{lock}	Locking time	-	-	-	50	µs
DR_{in}	Input clock duty ratio	-	20	-	80	%
DR_{out}	Output clock duty ratio	312.5 MHz < CKOUT ≤ 2500 MHz	47.5	50	52.5	%
		2500 MHz < CKOUT ≤ 5000 MHz	45	50	55	

[1] Reset time is required for all control bits to settle and reset all internal nodes of PLL to a pre-determined level.

Chapter 5
PLL Power Supply and Power Management

This chapter contains the following sections:

5.1 PLL Power Consumption

Table 5-1. PLL Power Consumption in Dynamic and Power-down Modes

Power Domain	Dynamic Power (mW) at 0.8/1.8 V	Power-down (mW) at 0.8/1.8 V
VCC08A	1.024 (Typ.)	0.017 (Typ.)
VCC18A	5.274 (Typ.)	7.2e-6 (Typ.)

5.2 Power Supply Sequencing

Because there is only one power domain used by this IP, no specific power-up/power-down sequence is required.

To guarantee that IP will be properly locked, please follow the operation sequence shown in **Figure 5-1**. After IP power ramp is finished, PDN needs a 0 state at least 5 µs width to reset IP after all input pins are set.

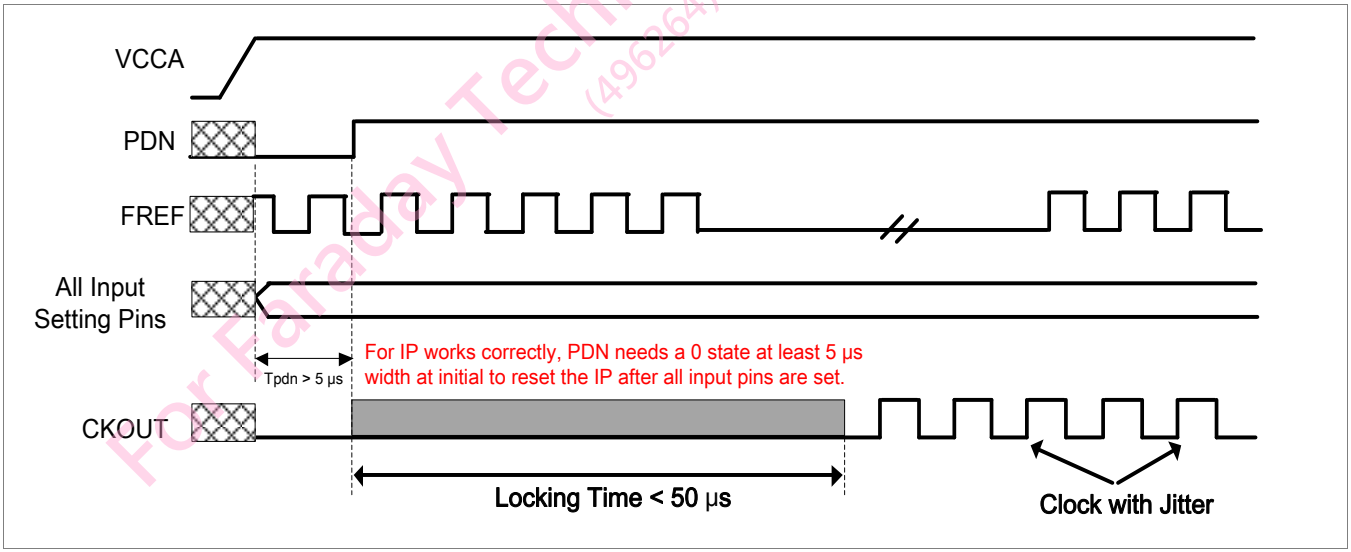

Figure 5-1. IP Operation Sequence

Chapter 6
PLL Testing

This chapter contains the following sections:

6.1 Test Methodology

FXPLL357HN0U does not have an isolated self-testing environment. It means that PLL does not have a test mode. Customers can perform the detailed tests in the normal mode by adding the testing Mux circuit and the test enable pin to set all the control input pins of PLL. Under this condition, customers will be able to run the real-time tests on the user applications. The input/output pins of PLL must be accessible. A Mux pin can be inserted after the output signal of PLL is asserted so that the output clock can be measured by the tester. The status of the test-enable pin is determined by system designers.

6.2 Test Wrapper

Step 1: Set PDN
Step 2: Set control pins as IS[2:0], MS[1:0], NS[8:0], P20[3:0], PA, PT[2:0], and PS[3:0]
Step 3: Set the input clock to FREF
Step 4: Monitor the clock frequency

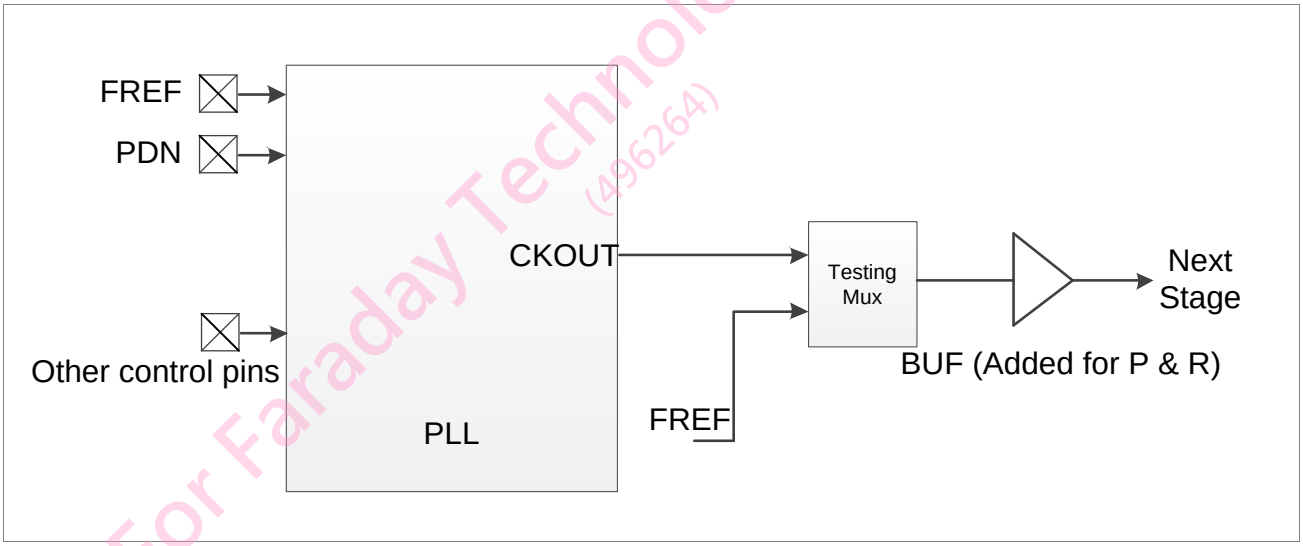

Figure 6-1. Testing Block Diagram

Chapter 7
PLL Integration

This chapter contains the following sections:

7.1 ASIC Integration

7.1.1 PLL is Sensitive in ASIC

The jitter performance of a PLL is highly dependent on the floor plan of ASIC. Because PLL is a sensitive cell when integrated into an ASIC design, the best way to maximize its capacity is to keep PLL away from the noisy blocks in the core region (Such as the memory block and the high-driving logic circuit) and the I/O region (Such as the high-driving I/O). This PLL must be placed around the I/O area as shown in **Figure 7-1** and **Figure 7-2**. Providing sufficient space between this PLL and noisy blocks is a simple and effective approach to reduce the coupled substrate noise.

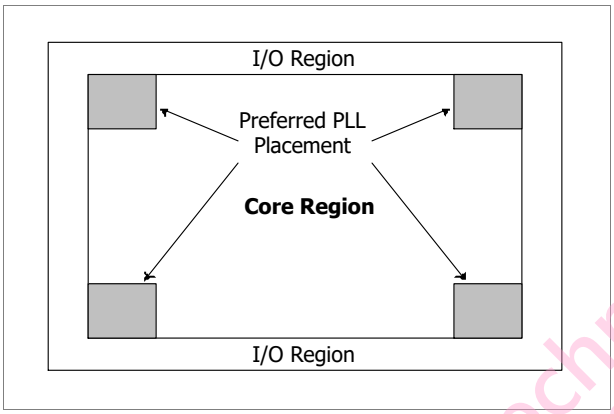

Figure 7-1. First Priority Position to Place PLL in ASIC

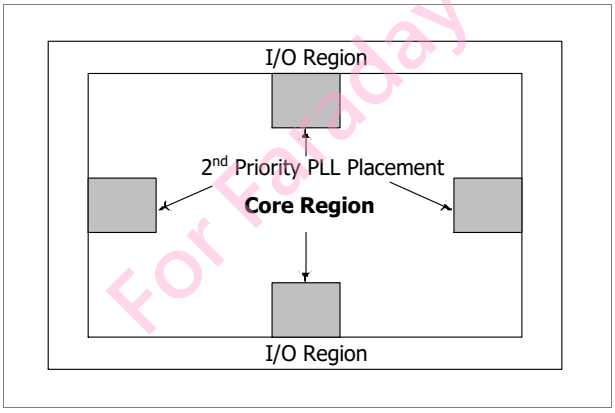

Figure 7-2. Second Priority Position to Place PLL in ASIC

The width of a wire used to connect the VCC and GND pin between the power/ground ports and cells of PLL should be equal to the width of the power port. The length of the wire should be minimized by placing PLL close to the corresponding power pins.

7.1.2 Multiple PLL Cells in ASIC

When two or more PLLs are used, they should be placed at the preferred locations to maximize the separation and minimize the coupled noise through the substrate. If two or more PLLs share the same input, they should be placed near the input source with the maximum separation between these PLLs to minimize the interference. If one PLL is used to drive another PLL, the downstream PLL must have a greater loop bandwidth to track the output of the upstream PLL (BWPLL2 > BWPLL1).

7.1.3 Power and Ground Considerations

FXPLL357HN0U needs two pair of power/ground ports for IP power/ground connection as shown in **Table 7-1**.

Table 7-1. Power Pin Description

Signal	Direction	Description
VCC08A	I	0.8 V analog power Please make VCC08A/D metal short in ASIC.
VCC18A	I	1.8 V analog power
GND08A	I	Analog ground Please make GND08A/D metal short in ASIC.

The power and ground are critical to the performance of this IP. The system should provide stable and clean sources to the power and ground with dedicated power I/O or high-quality regulator output.

The trace from power I/O or regulator output to IP power port should be as short and wide as possible, which helps reduce power trace IR drop and possible noise collection during long traces.

Figure 7-3 shows a power/ground connection guide for PLL in ASIC integration.

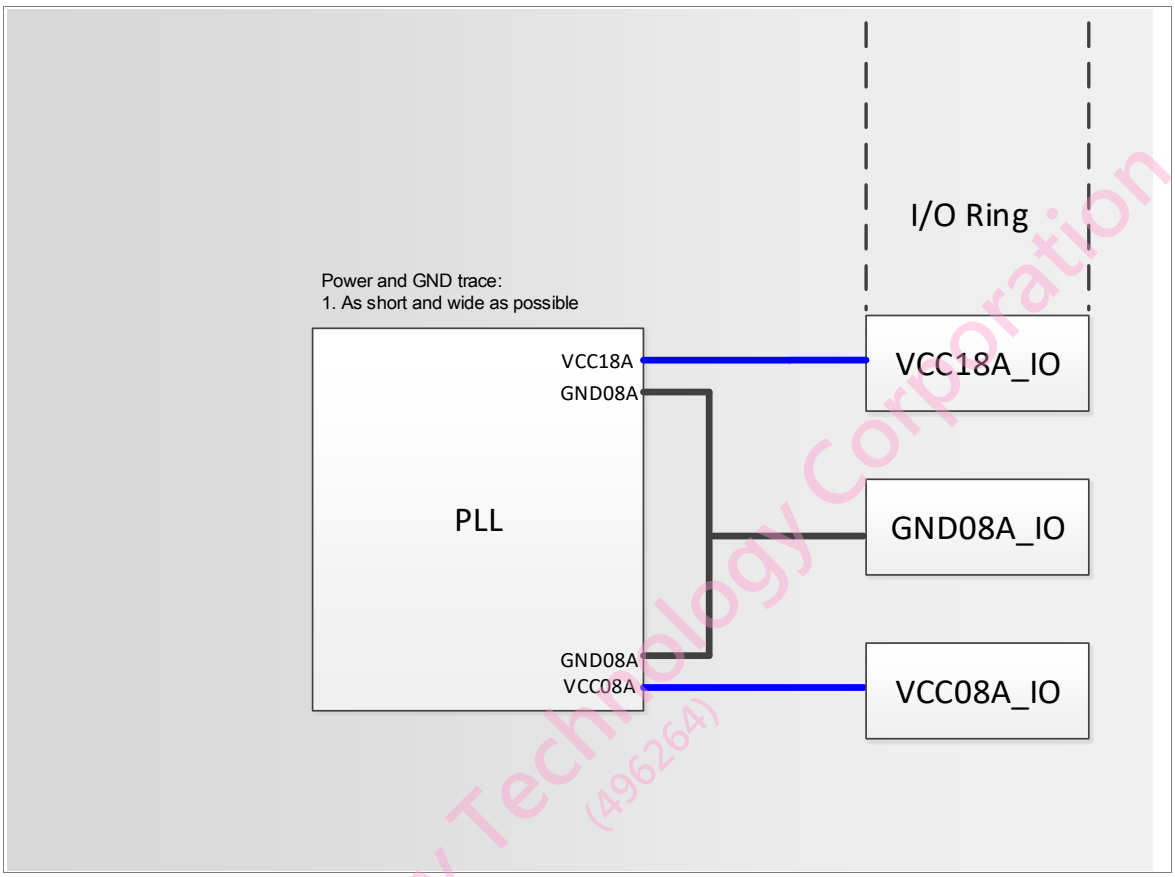

Figure 7-3. Power/Ground Connection Guide

7.1.4 ESD and Latch-up Issues

FXPLL357HN0U does not have a built-in ESD protection circuit under the multiple power and ground conditions. During ASIC integration, it is recommended that users take the signal integrity, ESD protection, and latch-up effect into consideration when connecting the power and ground cells to this PLL.

Figure 7-4 shows an example of the ESD connections when interfacing with K-power in ASIC.

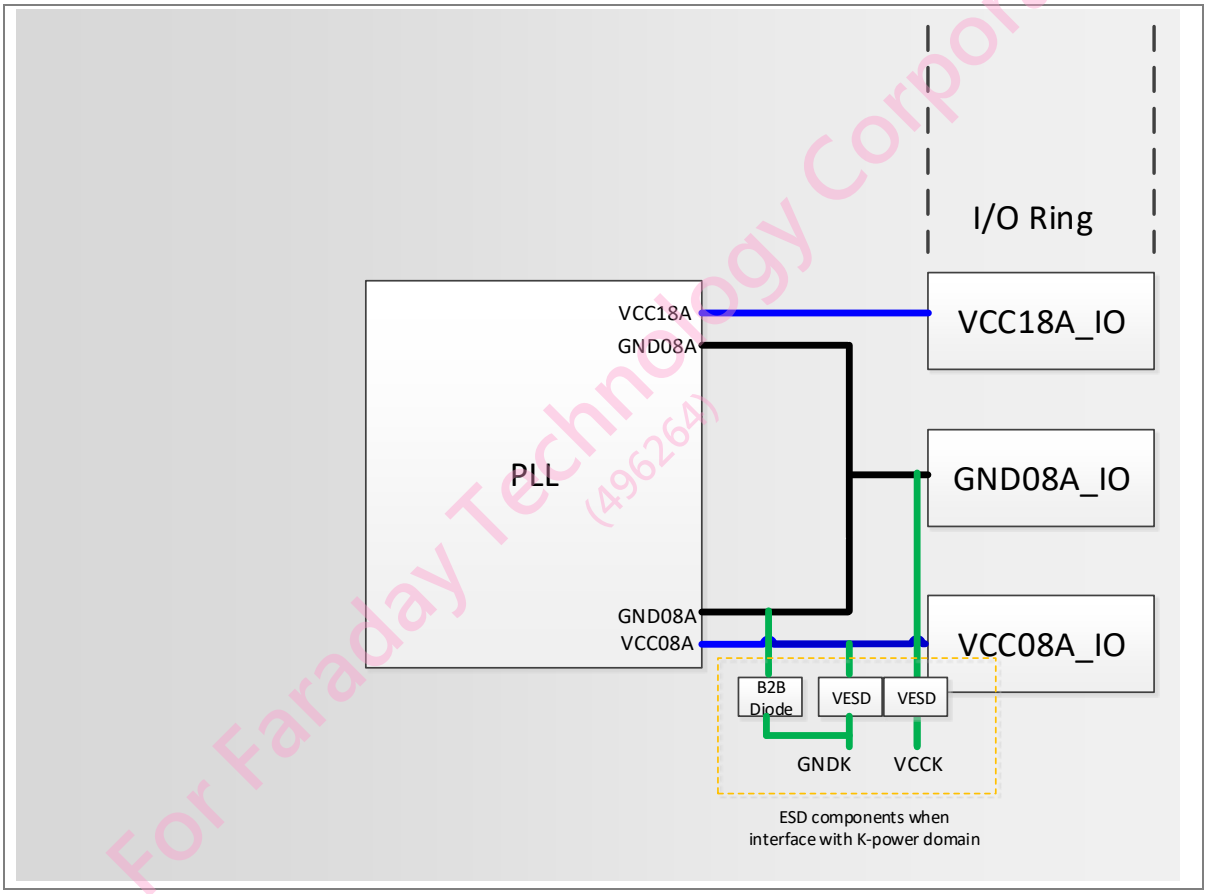

Figure 7-4. Connections of ESD Protection Circuit

For the second ESD protection, all input pins of FXPLL357HN0U have built-in second ESD protection circuits. Therefore, users only need to add the second ESD protection at the output pin of CKOUT at the ASIC integration phase.

7.2 Physical & Spacing

7.2.1 Bump Plan

Because there is no ESD I/O in PLL IP, users need to plan a bump location with external ESD I/O.

7.2.2 PLL Area

Area: X = 250 µm, Y = 220 µm (GDS Area)

7.3 PLL Spacing

For a highly integrated complex chip, many circuits are placed together. In this situation, the performance of a sensitive IP may be downgraded due to it is interfered by another nearby IP. Generally, an IP is interfered by another IP through the following paths:

1. Substrate noise: Ideally, the substrate voltage of an analog IP is the same as its ground voltage. During the chip operation, the analog IP substrate voltage may be varied because the ground noises are coupled by the nearby IPs. The substrate noises may downgrade the performance of the analog IP.
2. Metal-to-metal coupling noise: In a complex SoC chip, a noisy signal wire may be routed to the nearby area of a sensitive analog IP. For a sensitive analog circuit, the operation may be interfered by that noisy wire through the metal-to-metal coupling effect. That may downgrade the performance of the analog IP.

To avoid this situation, the chip designers have to take care of the substrate noise and metal-to-metal coupling noise at the chip layout stage. The noise reductions are achieved through the reserved spacing between the sensitive analog IP and noisy IP. To find out an adequate space for the noise reduction, while keeping the competitive chip area, Faraday IP designers have to perform a lot of simulations to conclude the minimum space for placing other IPs away from the analog IP, as well as the minimum space for the metal wires to route through.

Table 7-2 summarizes the minimum placement space between the analog IP and other IPs. **Table 7-3** summarizes the minimum routing space between the analog IP and other signal wires.

Table 7-2. General Recommended Space Placement Information

Side	Minimum Placement Space	Unit
Left side	10	µm
Right side	10	µm
Top side	10	µm
Bottom side	10	µm

Table 7-3. General Recommended Routing Metal Information

Metal Layer	Minimum Routing Space	Unit
Metal 1	5.0	µm
Metal 2	5.0	µm
Metal 3	5.0	µm
Metal 4	5.0	µm
Metal 5	5.0	µm
Metal 6	5.0	µm
Metal 7	5.0	µm
Metal 8	5.0	µm

7.4 Package Considerations

The package should consider the following recommendations:

- Design the package signal traces for the correct impedance as required for that particular implementation
- The reference planes should be designed to have the impedance as low as possible.
- Package designers should consider electrical performance issues, such as d_I/d_t and IR drops, especially on the PLL VCC/GND tracks.
- Minimize or eliminate the neck-down regions when routing the tracks
- Avoid the tracks jumping reference planes. De-coupling the planes where the jumps occur only when it is necessary.
- When using a wire-bond package, please pay attention to the diameters of the bond wires in order to minimize L, R, and M.
- Assign the corresponding PLL VCC/GND as close as possible to reduce loop inductance
- If PLL VCC/GND are routed as the trace type, users should keep the trace width to be a minimum of 200 µm, and keep the space between PLL VCC/GND and other power or signals to be a minimum of 100 µm. The trace should be as short as possible and PLL VCC/GND should be kept away from noisy signals. Furthermore, please route PLL VCC/GND on the power layers if necessary and keep them symmetric and close to each other.
- If PLL VCC/GND are assigned on the inner ring, assign the PLL VCC/GND ball at the location near to its finger in order to keep the traces as short as possible. Please also keep the PLL VCC/GND balls next to each other.
- The PLL reference clocks (FREF) should be kept far away from the noisy signals, and the trace should be as short as possible. If necessary, please use GND to shield FREF trace.
- **Figure 7-5** depicts an illustrative placement and surrounding of the critical ball pads in the package. The diagram does not imply the absolute ball arrangement; however, it shows the relative positions and quiet neighbor restrictions.

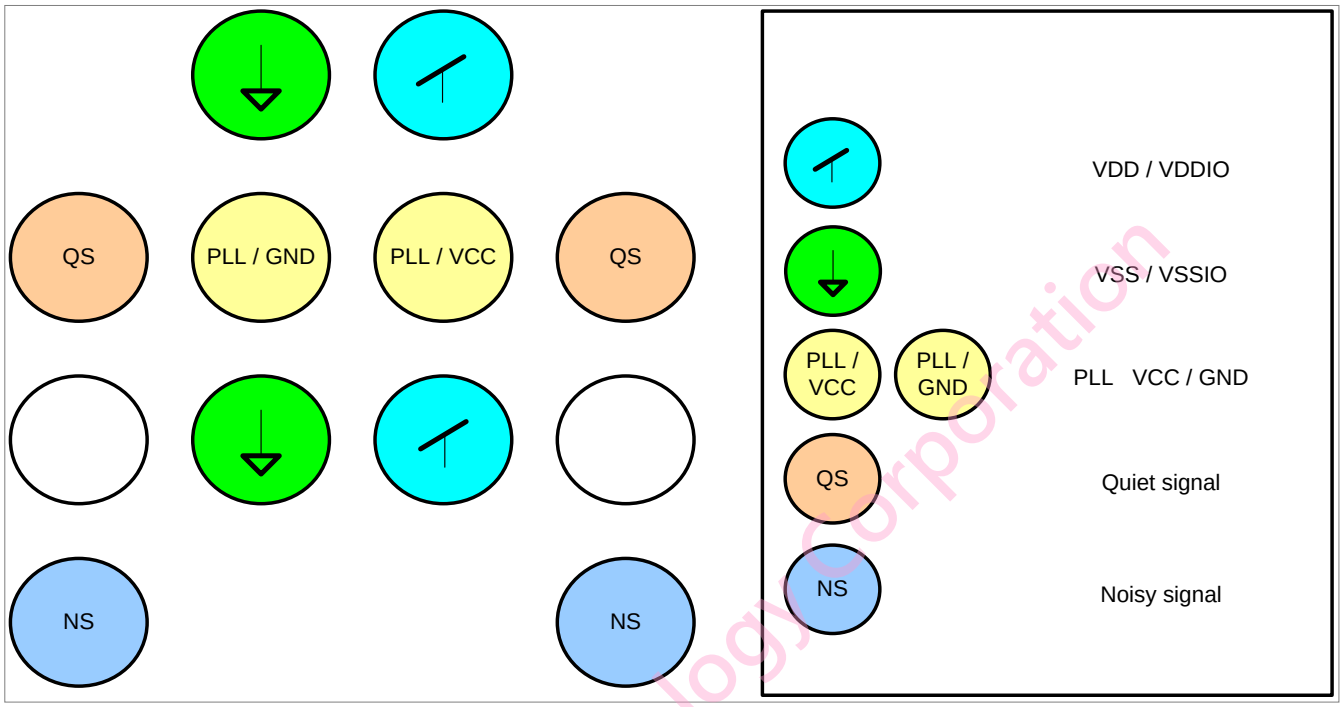

Figure 7-5. Diagram of Illustrative Package Ball Placement

7.5 IP Deliverables

- IP data book
- LEF file
- GDSII
- Liberty timing model files
- Behavioral analog model
- Verilog test benches for functional verification

Chapter 8
Verilog Functional Verification

This chapter contains the following sections:

8.1 Verilog Model

A Verilog model that describes the behavioral function of FXPLL357HN0U is available for customers to verify the system function at the top level.

A test-bench example for the behavioral Verilog model is also available in the IP deliverable file package.

File Name	Description
FXPLL357HN0U.v	FXPLL357HN0U Verilog model
test_ FXPLL357HN0U.v	Test-bench example of FXPLL357HN0U Verilog model

8.2 Simulation Model Usage

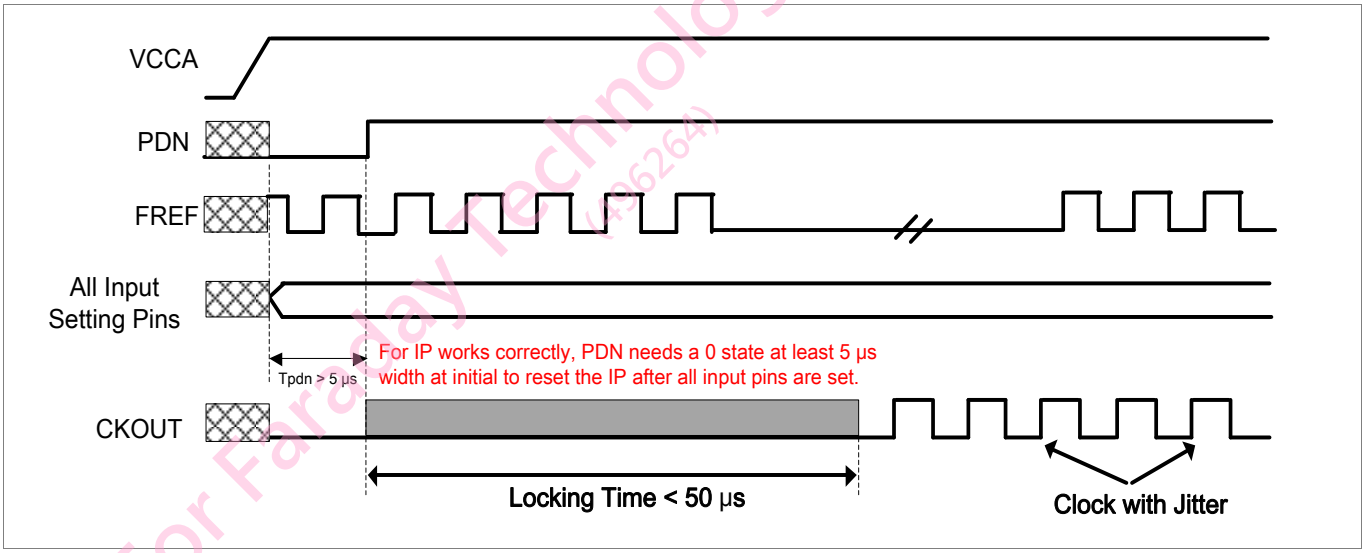

Figure 8-1. Timing Diagram in Normal Mode

Figure 8-1 shows the timing diagram in the normal mode when using the simulation model of this IP.

To guarantee the correct model behaviors, the following requirements need to be observed:

- Please use PDN to reset IP at the power-on phase. When users want to change the output frequency by changing the control setting, please also reset IP. All settings of the dividers and control inputs should be ready before the rising edge of PDN. The minimum pulse requirement of PDN low is 5 µs.
- The default behavior of the PLL model is to stop simulation when the FREF and CKOUT signals are out of the pre-defined working frequency range. Users can modify the “stop” parameter to ‘0’ to resume the simulation, if needed. However, under this circumstance, the PLL model will not reflect the correct behavior of an actual PLL design. Users should use it with caution.
- The default value of the CKOUT signal is “X” (Unknown) before the locking time elapses. The value can be updated if the “No_initial_unknown” parameter is set to ‘1’ to resolve the “unknown” clock propagation problem. However, under this circumstance, the PLL model will not reflect the correct behavior of an actual PLL design. Users should use it with caution.
- The locking time is defined as the “T_acq” parameter in the model. If users need to shorten the locking time to speed up the simulation at the pre-layout stage, users may set the “speed” parameter to ‘1’ through the test bench. The default value of “T_acq” is then set to 5 µs. Users should use it with caution.
- Faraday PLL behavioral model output clock can include the simple jitter model when the “No_jitter” parameter is set to ‘0’. However, due to internal model limitation, the reference clock input to PLL (FREF) should contain no jitter to prevent PLL function fail. Users can use an ideal clock for PLL FREF input or turn off PLL jitter whose output is served as FREF input by setting “No_jitter” to ‘1’.

Another concern of the Verilog model of this IP is that the output clock jitter performance may deviate from a real chip, so users should be aware of this and refer to the jitter specification listed in **Table 4-3** when dealing with timing-related design.

Figure 8-2 shows an example of Verilog test bench.

```
initial begin
  //---- set NS ----
  NS = 8'd125;
  PDN = 1'b0;
  PS = 2'd0;
  force FREF = clk1;
  -> FREF_10M_evt;
  #10000000 PDN = 1'b1;
  #10000000 PDN = 1'b0;
  #10000000 PDN = 1'b1;
  #10000000 PDN = 1'b0;

  #10000000 PDN = 1'b1;
  -> FREF_15M_evt;
  force FREF = clk2;



  #10000000 PDN = 1'b0;
  #10000000 PDN = 1'b1;
  -> FREF_20M_evt;
  force FREF = clk3;
  #10000000 force FREF = 0;
  #10000000 force FREF = clk3;
```

Figure 8-2. Example of Verilog Test Bench

Figure 8-3 shows a simulation result of the behavioral model with jitter-off.

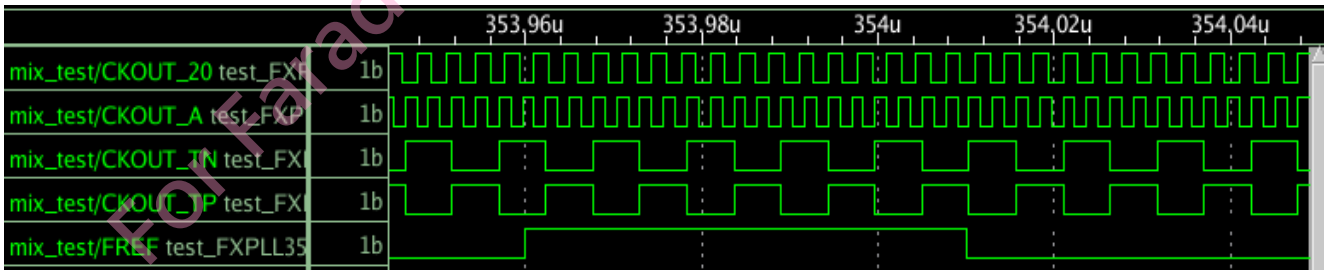

Figure 8-3. Simulation Result of Behavioral Model with Jitter-off

Table 8-1 shows a summary of error messages if violation occurs.

Table 8-1. Summary of Error Messages if Violation Occurs

Violation Item	Cause of Error
PLL_Error (0)	Unable to change the configurable value of the divider
PLL_Error (1)	Users must reset PLL.
PLL_Error (2)	The configurable pins (Such as MS* or NS*) are not ready.
PLL_Error (3)	The PDN reset period time is too short.
PLL_Error (4)	Unable to change the test pin in the simulation time
PLL_Error (5)	The output frequency is too low.
PLL_Error (6)	The output frequency is too high.
PLL_Error (7)	Setup time violation for PDN and FREF
PLL_Error (8)	FREF/FPFD is too low/high.
PLL_Error (9)	Stop simulation
PLL_Error (10)	All divider configurable pins are zero.
PLL_Error (11)	The simulation model does not support the test mode.
PLL_Error (12)	The locking time is only for speeding up the simulation time.