|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Duong Minh Tam | No. | T050 | Div/Dept | DSD/ACD/ACT1 | Job  Date：2022/05/27  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 🗹W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

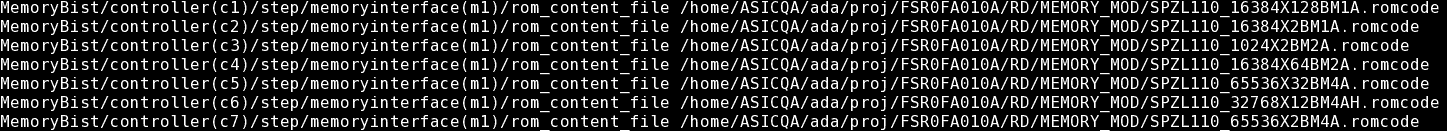
1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. FSR0FA010A MEM Test-chips, |
| 1. What are the problems encountered this week? Any actions taken? Any help needed? 2. flec, 3. Clock uncertainty, |
| 3. What are the tasks for next week? Any preparation needed in advance? |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Alden Duong (2022/05/27) | Charles Le  (Signature/Date) | (Signature/Date) |

【Note】

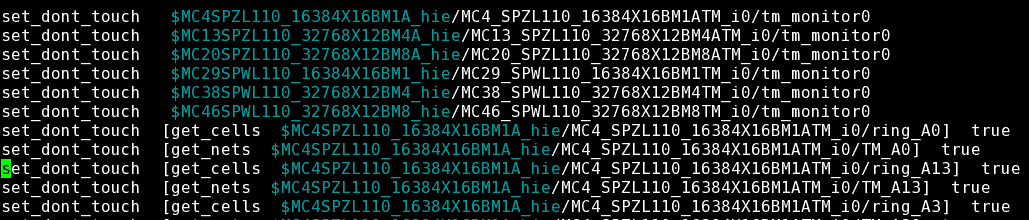
1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. **romcode**



File.romcode



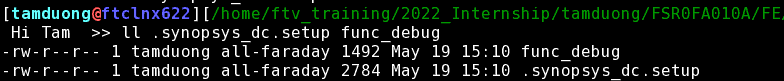
1. **set\_dont\_touch**

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Sets the dont\_touch attribute on cells and nets in the current design, on designs and library cells, to prevent these objects from being modified or replaced by Design Compiler during optimization.

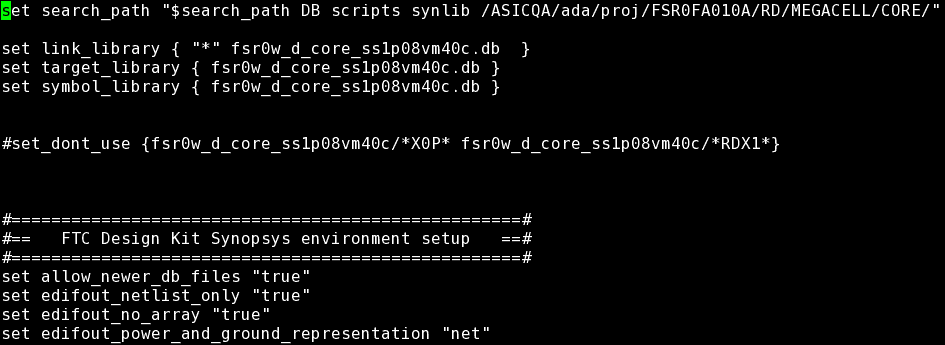
**Ref:** [*https://www.micro-ip.com/STA/dictionary\_512\_17/set\_dont\_touch.html*](https://www.micro-ip.com/STA/dictionary_512_17/set_dont_touch.html)

1. **The distinction between *“.filename”* and *“filename”***



.synopsys\_dc.setup: Design compiler setup file. It will contain search paths to all of the standard cell libraries that you need.

Ref: [*https://s2.smu.edu/~manikas/CAD\_Tools/SDC/lab2/lab2\_synopsys\_dc.pdf*](https://s2.smu.edu/~manikas/CAD_Tools/SDC/lab2/lab2_synopsys_dc.pdf)



**link\_library** : the library used for interpreting input description

**target\_library** : the ASIC technology which the design is mapped

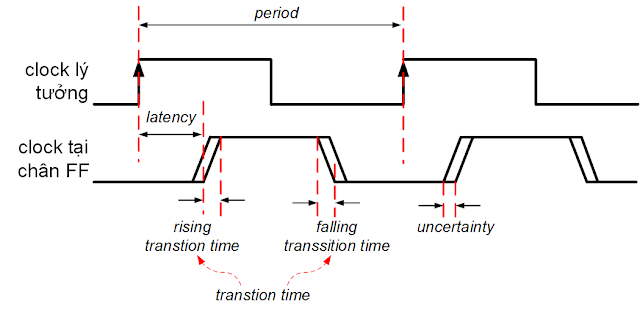
**symbol\_library** : used for schematic generation : used for schematic generation

**search\_path** : the path for unsolved reference library

**synthetic\_path** : designware library

Ref: [*http://www.ee.ncu.edu.tw/~jfli/vlsi21/lecture/dc.pdf*](http://www.ee.ncu.edu.tw/~jfli/vlsi21/lecture/dc.pdf)

1. **Clock Uncertianty**



Ref:[*https://www.physicaldesign4u.com/2020/04/skew-latency-uncertaintyjitter.html#:~:text=Clock%20Uncertainty%3A%20clock%20uncertainty%20is,static%20and%20dynamic%20clock%20uncertainties.*](https://www.physicaldesign4u.com/2020/04/skew-latency-uncertaintyjitter.html#:~:text=Clock%20Uncertainty%3A%20clock%20uncertainty%20is,static%20and%20dynamic%20clock%20uncertainties.)

Uncertain factors (like skew, jitter, OCV, CROSS TALK, MARGIN or any other pessimism)

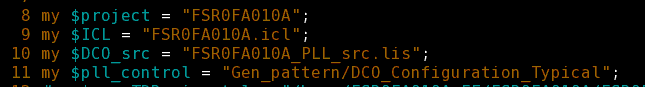
# **Gen pattern**

* 1. **Summarize data:**

**Exc:** */home/ftv\_training/2022\_Internship/tamduong/FSR0FA010A/FE/DFT/MBIST/Intern\_20220519/Gen\_pattern/sum\_mem\_info\_new.pl*

**Update information in *sum\_mem\_info****\_****new.pl***

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Project |  |  |  | # Project name |
| ICL |  |  |  | …/top\_tsdb\_outdir/…/\*.icl |
| PLL\_src |  |  |  | # PLL source list for MMEM clock period |
| DCO\_config | |  |  | # Config PLL clock / DCO clock |

**Run gen summarize script**

**./sum\_mem\_info\_new.pl -gen\_db**

|  |  |  |
| --- | --- | --- |
| Output: |  | FSR0FA010A\_MBIST\_PAT\_config.csv |

**./sum\_mem\_info\_new.pl -gen\_pt**

|  |  |  |
| --- | --- | --- |
| Output: |  | FSR0FA010A\_pt |



* 1. **Gen pattern:**

**Exc:** */home/ftv\_training/2022\_Internship/tamduong/FSR0FA010A/FE/DFT/MBIST/Intern\_20220519/DATA/Prepare\_data\_for\_gen\_pattern*

**Output:**

…/\*wgl.gz

**Modify file** *mbist\_pattern.dof*

|  |  |  |  |
| --- | --- | --- | --- |
| set\_tsdb\_output\_directory | |  | Set PAT gen directory |
| read\_core\_descriptions | |  | core library |
| read\_config\_data |  |  | pattern\_spec |



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**./run\_gen\_pattern**

|  |  |  |
| --- | --- | --- |
| Output: |  | ./PAT\_GEN\_tsdb\_outdir/patterns/FSR0FA010A\_gate.patterns\_spec\_signoff/\*wgl.gz |

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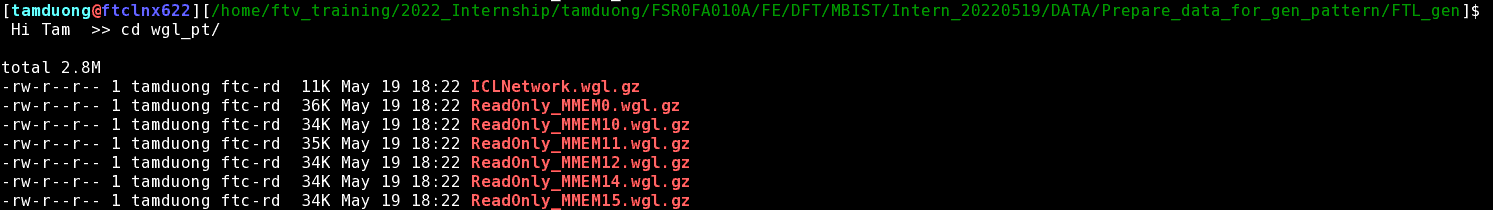
* 1. **Resequence patterns:**

**Path:**

*/home/ftv\_training/2022\_Internship/tamduong/FSR0FA010A/FE/DFT/MBIST/Intern\_20220519/DATA/Prepare\_data\_for\_gen\_pattern/FTL\_gen*

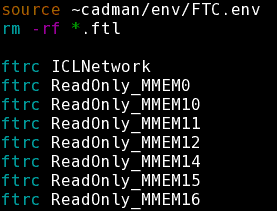
* + 1. **Gen FTL file**

**Make directory and copy the *wgl file* pattern**

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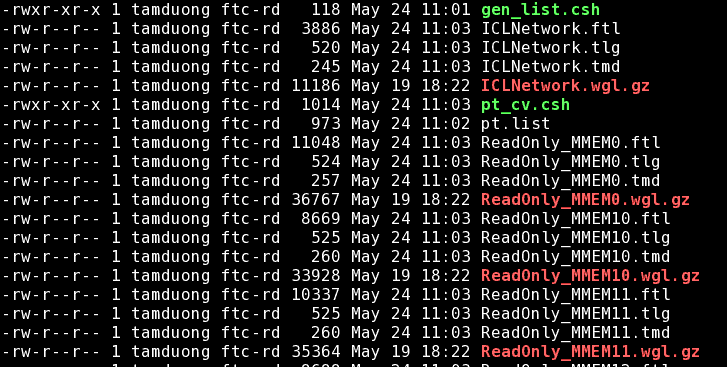
**Make ftrc script**

|  |  |
| --- | --- |
| touch | pt\_cv.csh |
| cp -rf | setup.ftc |

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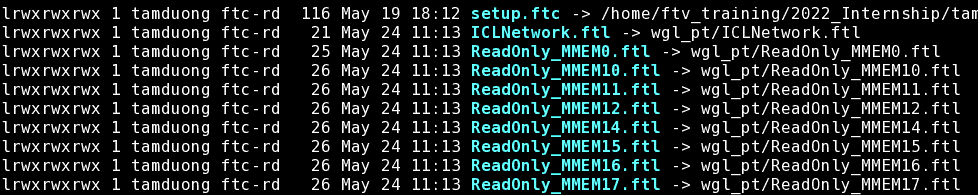
**Run script**

|  |  |
| --- | --- |
| source | pt\_cv.csh |

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* + 1. **Resequence pattern**

Link the *.ftl file* to *FTL\_gen folde*r: ***ln -sf wgl\_pt/\*.ftl ./***

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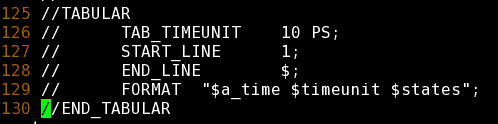
**Run fpad in Pre\_sim folder**

|  |  |  |
| --- | --- | --- |
| Ouput: |  | <Project>.pad  <Project>.th |

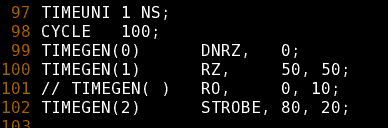
****

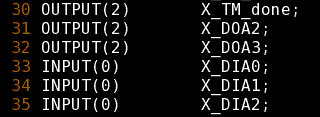
**# Modify file <Project>.th**

**Comment out all line after line 125**

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**Fix timegen**

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**Link .pad file and .th file to FTL\_gen folder**

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**Run gen pattern: ./gen\_vt.csh**

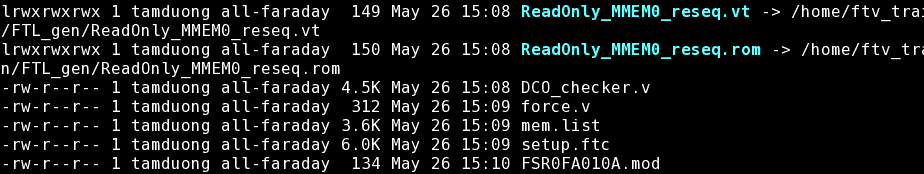
****

.xce.opt

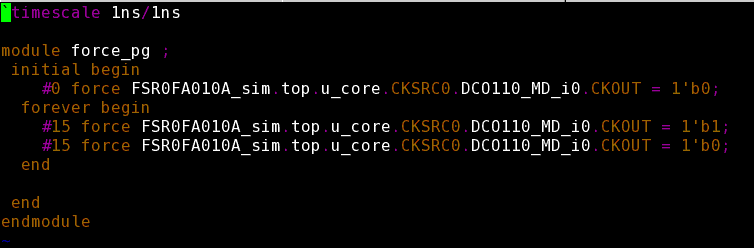
This file is the intermediate command file used to run the XCELIUM simulator. The actual XCELIUM command line options are listed in this file.

1. **FSIM**
   1. **Run FSIM with MMEM0**

* **Link file .vt and .rom to folder MMEM\***
* **Copy file DCO\_checker.v**



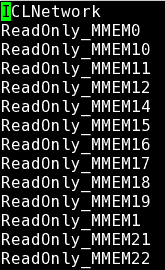
* **Create file force.v**

****

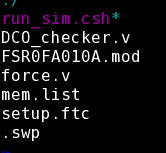
* **Run fsim**

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* 1. **Run FSIM all**
* **pt.list**

****

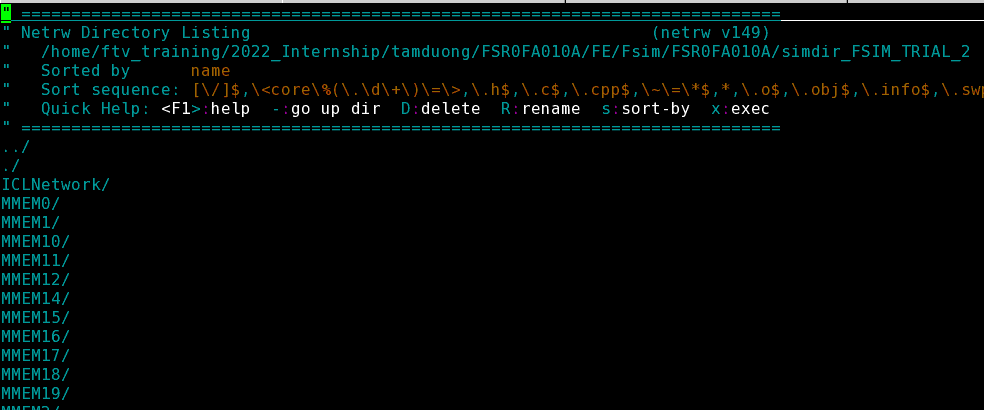
* **template**

****

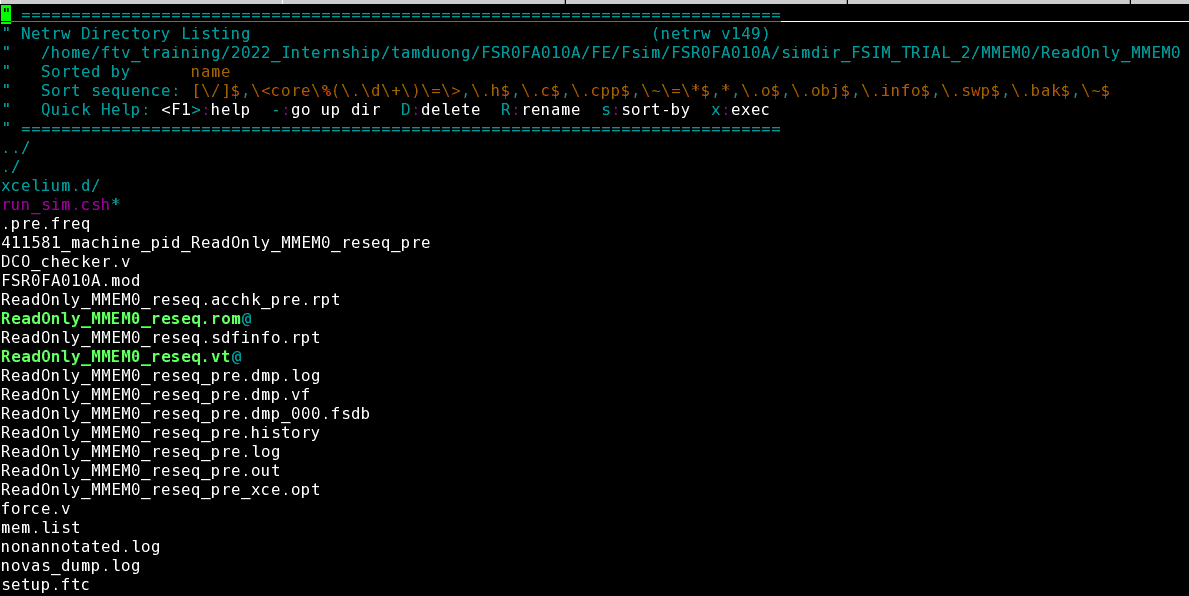
* **script**

****

* **simdir\_FSIM\_TRIAL\_2**

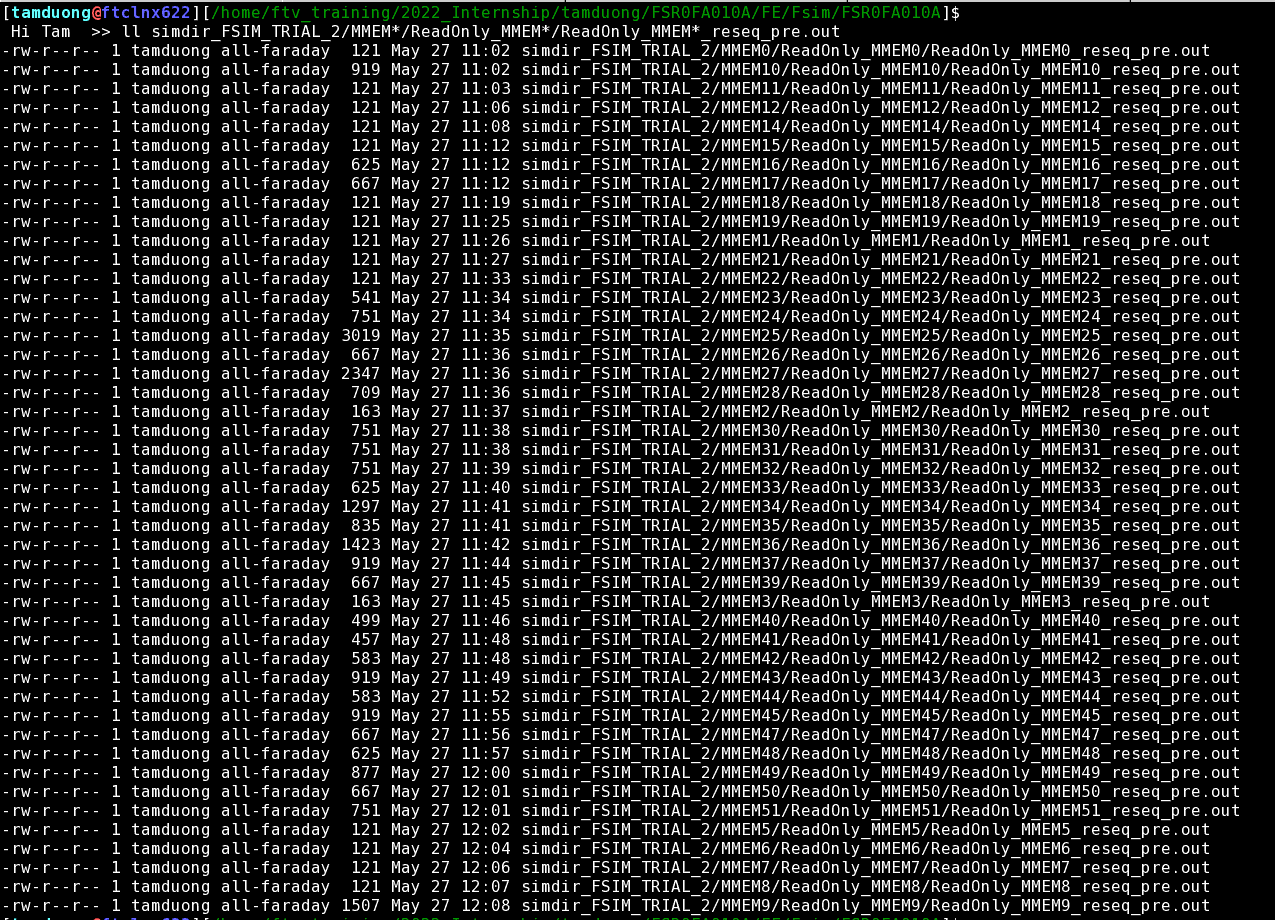
****

* **ReadOnly\_MMEM\***

****

**Exc:**

*ll simdir\_FSIM\_TRIAL\_2/MMEM\*/ReadOnly\_MMEM\*/ReadOnly\_MMEM\*\_reseq\_pre.out*

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**Reference:**

* [T:\Vietnam\DSD\DSD\_ACD\2022\_New\_Comer\_Traning\MBIST\_TC\_ Guid\_Danny.xlsx](../../../2022_New_Comer_Traning/MBIST_training/MBIST_TC_Guide_Danny.xlsx)
* [T:\Vietnam\DSD\DSD\_ACD\2022\_New\_Comer\_Traning\MBIST\_training\MBIST\_running\_flow.pptx](../../../2022_New_Comer_Traning/MBIST_training/MBIST_running_flow.pptx)

Linux env:

·         Path: /home/FSR0FA010A\_FE/FSR0FA010A\_Danny/DATA

You can prefer my project:

·         Path: /home/FSR0FA010A\_FE/FSR0FA010A\_Danny/FE/DFT/MBIST/JAN\_24\_FDI/DATA