|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Duong Minh Tam | No. | T050 | Div/Dept | DSD/ACD/ACT1 | Job  Date：2022/07/01  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 🗹W4 | | | | | |
| Third Month | 🗹W1 🗹W2 □W3 □W4 | | | | | |

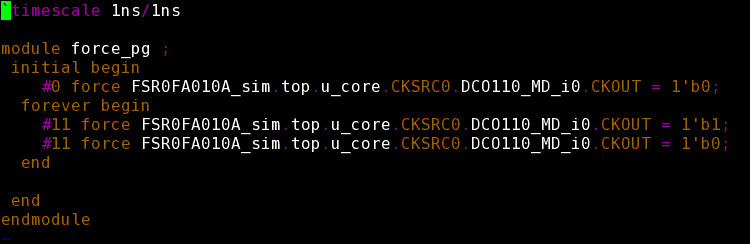
1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. How to create setup file, 2. Trial *FSN0FS102A* MEM Test-chips |
| 1. What are the problems encountered this week? Any actions taken? Any help needed? |
| 3. What are the tasks for next week? Any preparation needed in advance? |
|  |

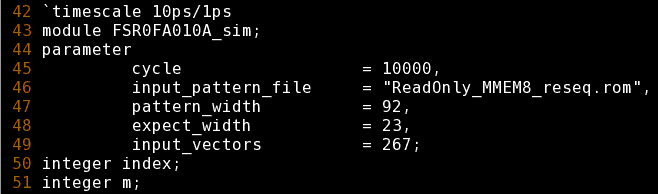
|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Alden Duong (2022/07/01) | Charles Le  (Signature/Date) | (Signature/Date) |

【Note】

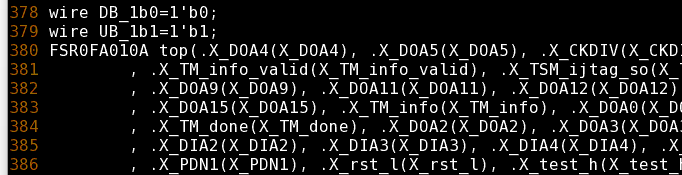
1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. **What is *FSR0FA010A\_sim* ?**



After run ftl2ver => file tb (.vt)

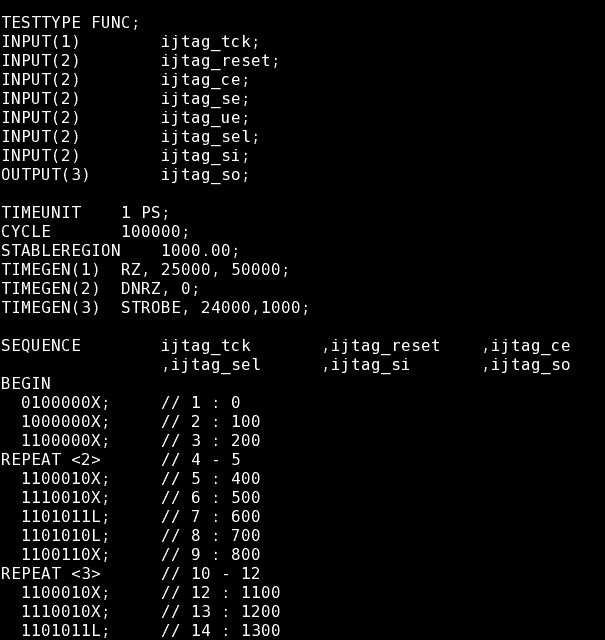


***FSR0FA010A\_sim*** is the name of module Testbench.



1. Why need Resequence pattern.
2. Mode (RESEQ, MASK) ?

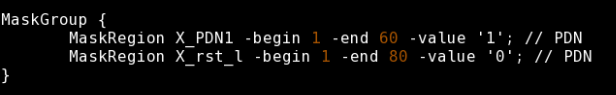
**ReadOnly\_pattern.ftl**



Mode = RESEQ => ReadOnly\_pattern\_tmp.ftl

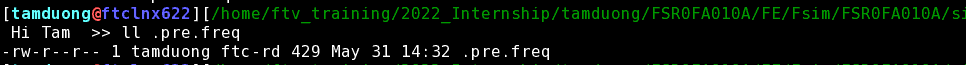
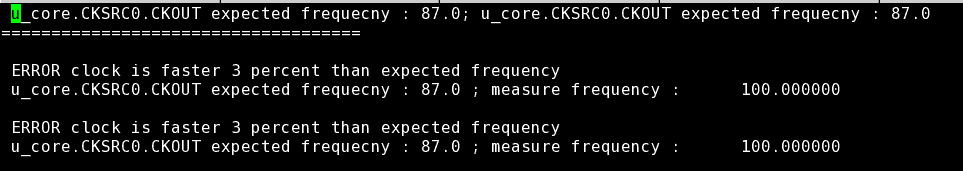


Mode = MASK => ReadOnly\_pattern\_reseq.ftl





1. What is DCO\_Checker used for ?

Check freq of MEM

1. How memory work?
2. Learn about MBIST and BISR.
3. How to test in ram/rom?

The main memory inside a computer is based on two kinds of chip: a temporary, volatile kind that remembers only while the power is on (RAM) and a permanent, nonvolatile kind that remembers whether the power is on or off (ROM).

Memory Built-In Self-Test (MBIST) gives the best solution to test such memories. Built in self-repair (BISR) widely used to test/repair RAM, where each RAM uses dedicated BISR circuit. The BISR feature helps to check Memory BIST logic and memory wrapper interface. Memory testing will become more effective when it adds repair features like Built-In Redundancy Analysis (BIRA) into it.

MBIST is a self-testing and repair mechanism which tests the memories through an effective set of algorithms to detect possibly all the faults that could be present inside a typical memory cell : stuck-at (SAF), transition delay faults (TDF), coupling (CF) or neighborhood pattern sensitive faults (NPSF).

**What is Memory Repair?**

The memory repair feature diverts faulty areas of memories (e.g. row, column or both) by spare or redundant rows and columns available.

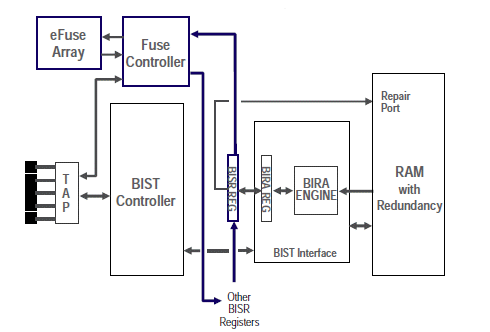
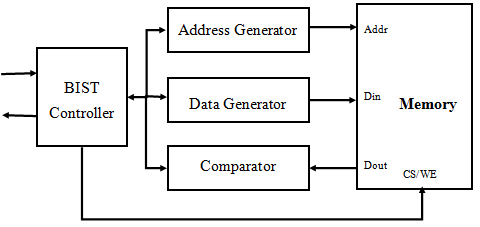


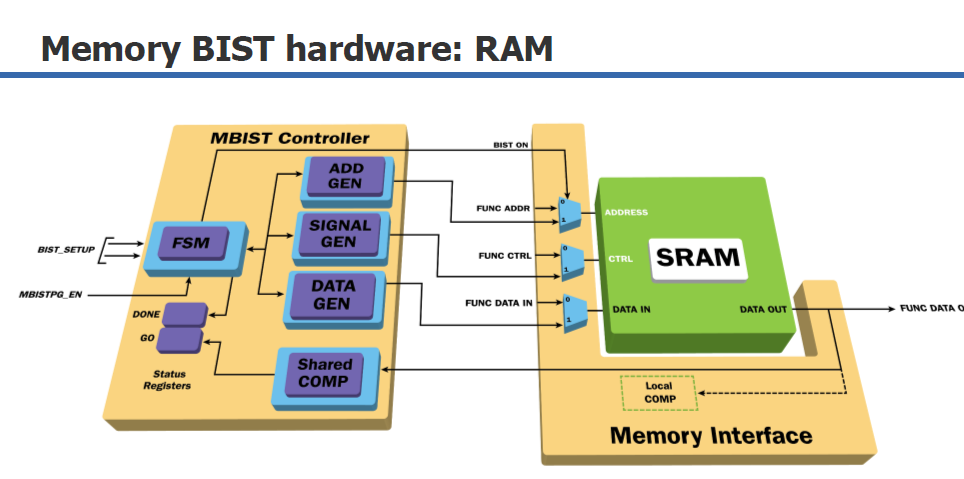
Figure 1 BISR Architecture

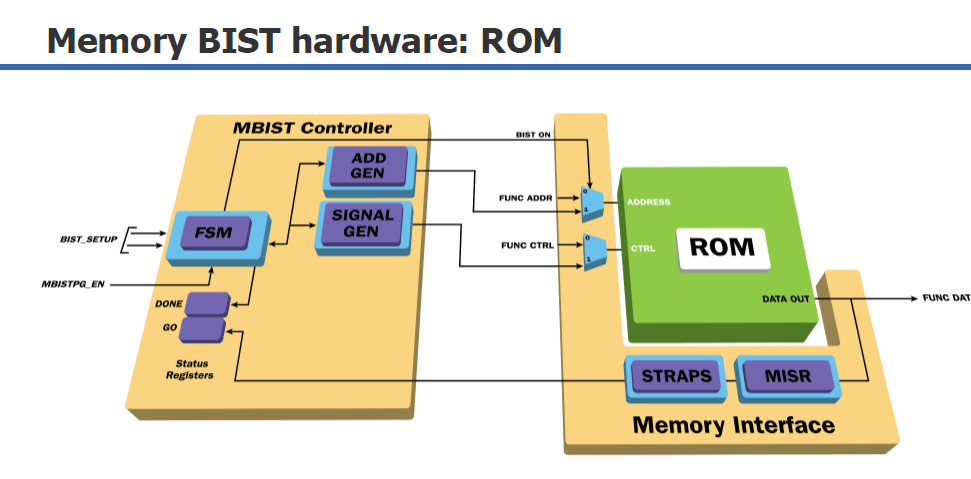
Ref: <https://www.design-reuse.com/articles/46328/testing-of-repairable-embedded-memories-in-soc.html>

**MBIST Model**



Ref: <https://www.einfochips.com/blog/memory-testing-an-insight-into-algorithms-and-self-repair-mechanism/>





Ref: [T:\Vietnam\DSD\DSD\_ACD\Mentor\_Doc\Tessent\_Frarday\_training\_MBIST.pdf](file:///T:\Vietnam\DSD\DSD_ACD\Mentor_Doc\Tessent_Frarday_training_MBIST.pdf)

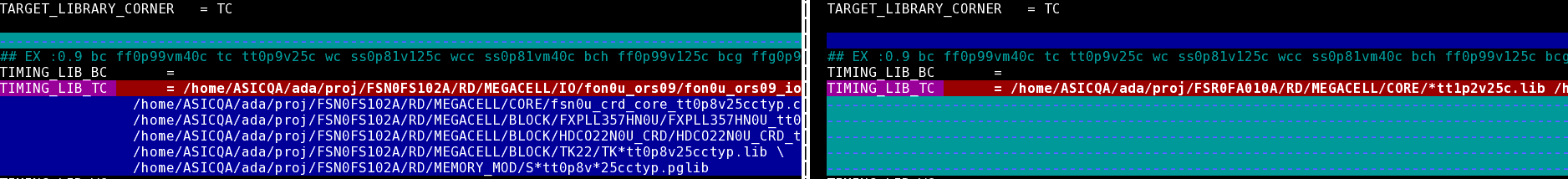
# **Run MBIST with project FSN0FS102A**

## Create setup file:

In previous weeks, use the available setup file to running the DKs (ferc, flre, … ).

In this week, learn how to create setup file.

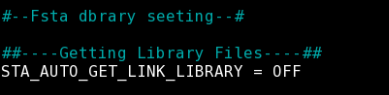
Setup file to run ferc, flre, … (NOMINAL\_VOLTAGE, IO\_VOLTAGE, DESIGN, …)

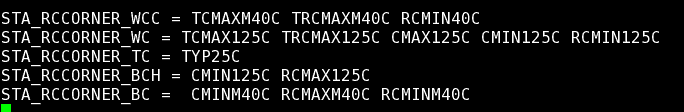


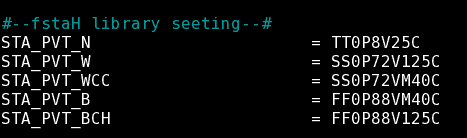
File ***setup.ftc.fsta***

LIBRARY, NOMINAL\_VOLTAGE, DESIGN

**Base on file sign-off**

****





Base on file **APR data in check information FSN0FS102A**



****

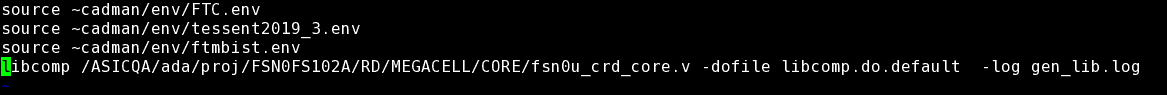
## **MBIST\_insertion**

## Compile standard library to tessent library

**Path:** */home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/INPUT/Standard\_Cell*

|  |  |  |
| --- | --- | --- |
| Input |  | libcomp.do.default |
| **Runfile:** |  | run\_libcomp |
| Ouput: |  | libcomp.atpglib |

Core library is ***FSN0U\_CRD***

****

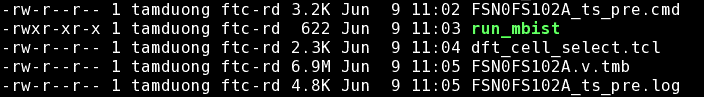
****

1. **<Project>\_ts\_pre.cmd**

**Path:** */home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA*

|  |  |  |  |
| --- | --- | --- | --- |
| **<Project>\_ts\_pre.cmd** | | | |
| Intput |  | <Project>.v | |  | |  | |  | |  | |  | |  | | |  | |  | |  | |  | |  | |  | |  |  |
|  |  | <Project>\_ts\_pre.cmd | | | |  | |  | |  | |  | |  | | |  | |  | |  | |  | |  | |  | |  |  |
|  |  | dft\_cell\_select.tcl | | | | | |  | |  | |  | | | | | | | | | | | | | | | | | | |
|  |  |  |  | |  | |  | |  | |  | |  | | |  | |  | |  | |  | |  | |  | |
| Output: |  | <Project>.v.tmb | | | |  | |  | |  | |  | |  | | |  | |  | |  | |  | |  | |  | |  |  |
|  |  | <Project>\_ts\_pre.log | | | | | |  | |  | |  | |  | | |  | |  | |  | |  | |  | |  | |  |  |
|  | | | | | | | | | | | | | | |

**Exc:** *tessent -shell -dofile FSN0FS102A\_ts\_pre.cmd -logfile FSN0FS102A\_ts\_pre.log -replace*

****

1. **MBIST Insertion**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| mbist\_insertion.dof | Default |  | # Insert mbist circuit, could be modified based on feature of type and project | | | | | |
| go\_make\_add\_clock.csh | Default |  | # Script to extract clock period | | | | | |
| FSR0FA010A\_PLL\_src.lis | RD |  | # PLL clock source list for memories | | | | | |
| Instance\_need\_MBIST.dof | Default |  | # Set memories instance option for BIST and BISR | | | | | |
| func\_debug | Default |  |  |  |  |  |  |  | |  |  |
| .synnosyp\_dc.setup | Default |  |  |  |  |  |  |  | |  |  |
| rom\_content.dof | Create |  | # Rom code file pattern | | |  |  |  | |  |  |
| mem.list | Create |  | # memories list path | | | | | |
| register\_tdr.dof | Create |  | # set static register static dft signal | | | | | |
| add\_clock.dof | Create |  | # Clock period file | | | | | |

**Path:**

*/home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA*

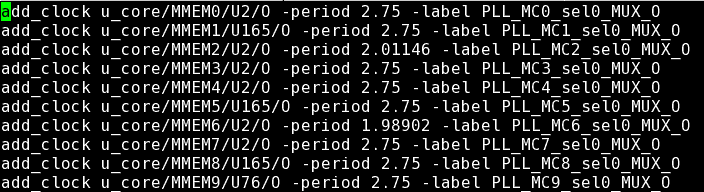
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Extract file memories into mem.list** | | | |  |  |
| * /home/ASICQA/ada/proj/FSN0FS102A/RD/MEMORY\_MOD/verilog/\*.v | | | | | |
| Out | mem.list |  |  |  |  |

****

****

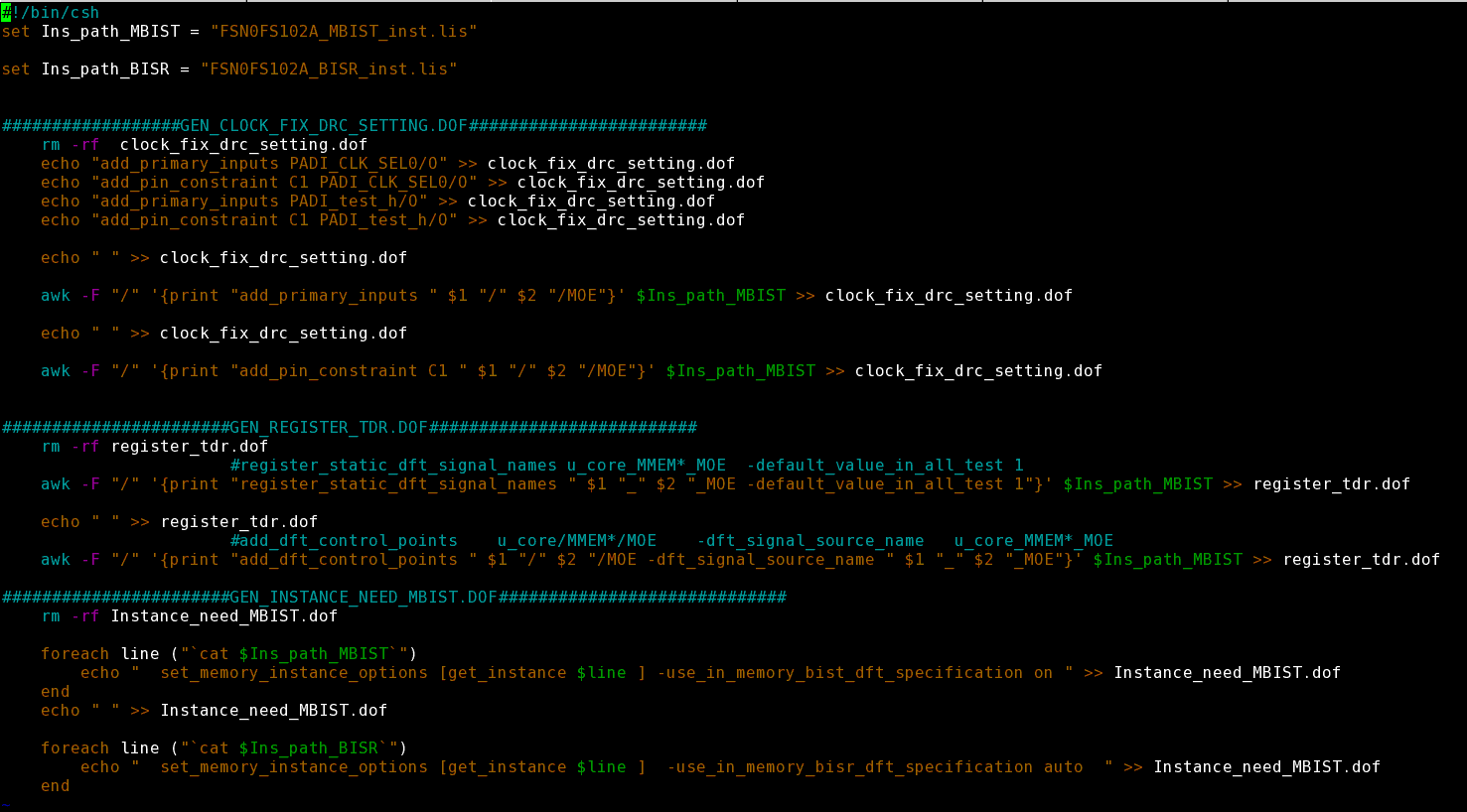
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Make clock data file : Prepare file run go\_make\_add\_clock.csh** | | | | |
| >> | ./go\_make\_add\_clock.csh | |  |  |
| Out | add\_clock.dof |  |  |  |

****

****

**File name:** gen\_dof\_file.csh

**Path:** *home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA/gen\_dof\_file.csh*

****

**Create:**

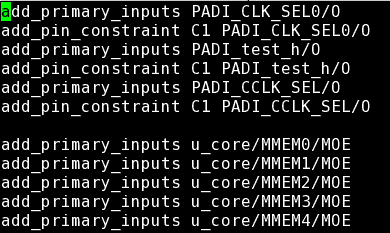
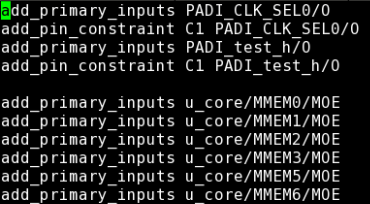
clock\_fix\_drc\_setting.dof

register\_tdr.dof

Instance\_need\_MBIST.dof

**File name:** clock\_fix\_drc\_setting.dof

**Path:** */home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA/clock\_fix\_drc\_setting.dof*

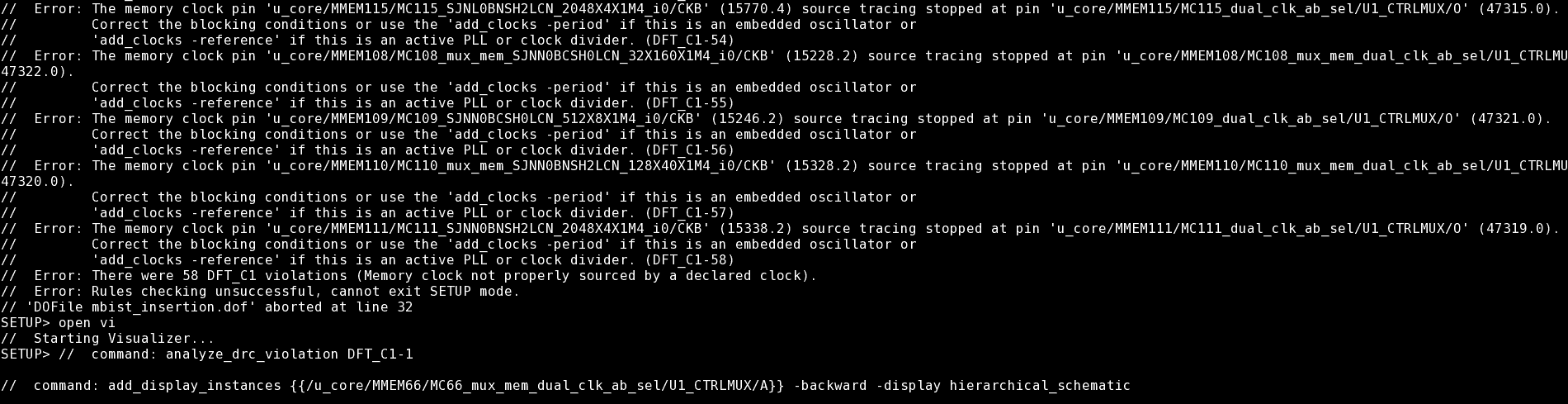


102A 010A

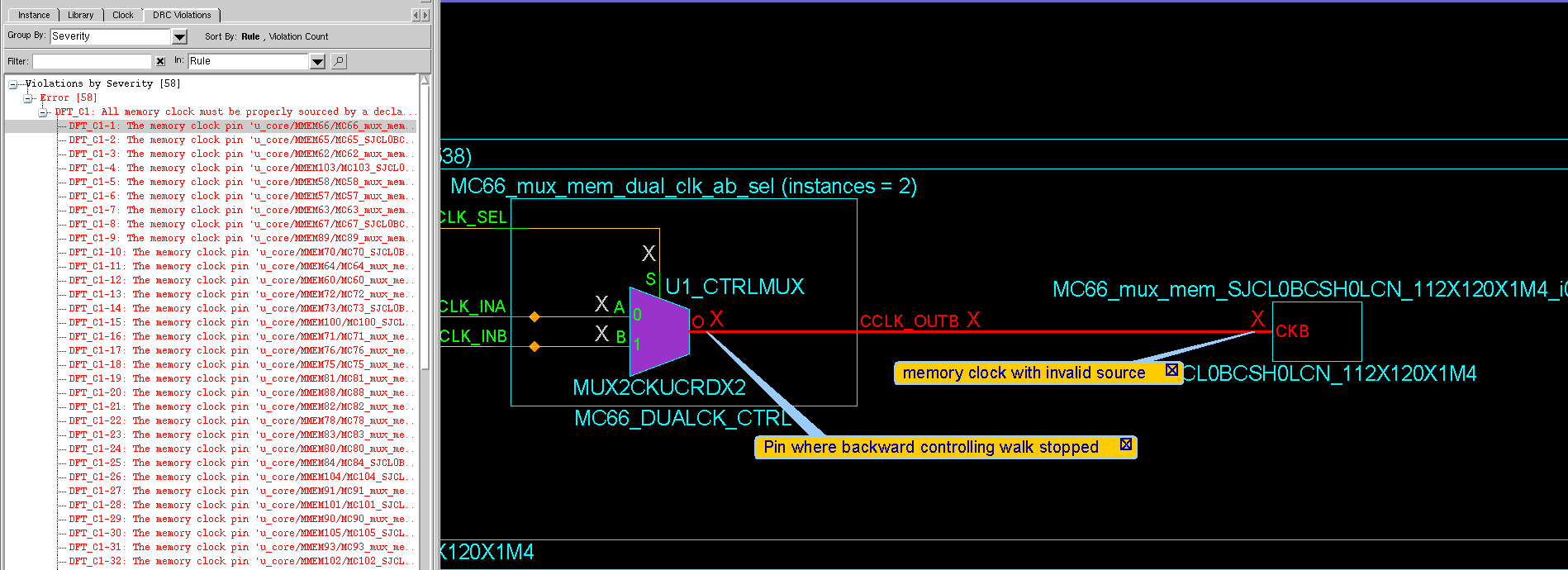
???

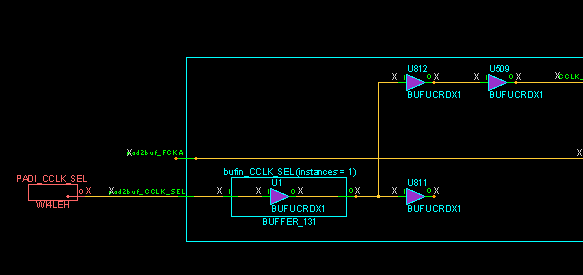
add\_primary\_inputs PADI\_CCLK\_SEL/O

add\_pin\_constraint C1 PADI\_CCLK\_SEL/O

When running without these 2 lines will have error:

Open vi => tab DRC Violation => double-click on 1 error



Find the reason why is equal = x

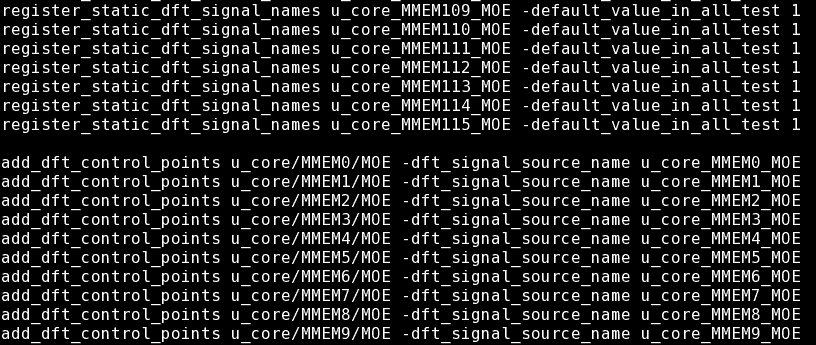
PADI\_CCLK\_SEL = x => so need to add 2 lines

add\_primary\_inputs PADI\_CCLK\_SEL/O

add\_pin\_constraint C1 PADI\_CCLK\_SEL/O

**File name:** register\_tdr.dof

**Path:** */home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA/register\_tdr.dof*



**File name:** Instance\_need\_MBIST.dof

**Path:** */home/ftv\_training/2022\_Internship/tamduong/FSN0FS102A/FE/DFT/MBIST/DATA/Instance\_need\_MBIST.dof*

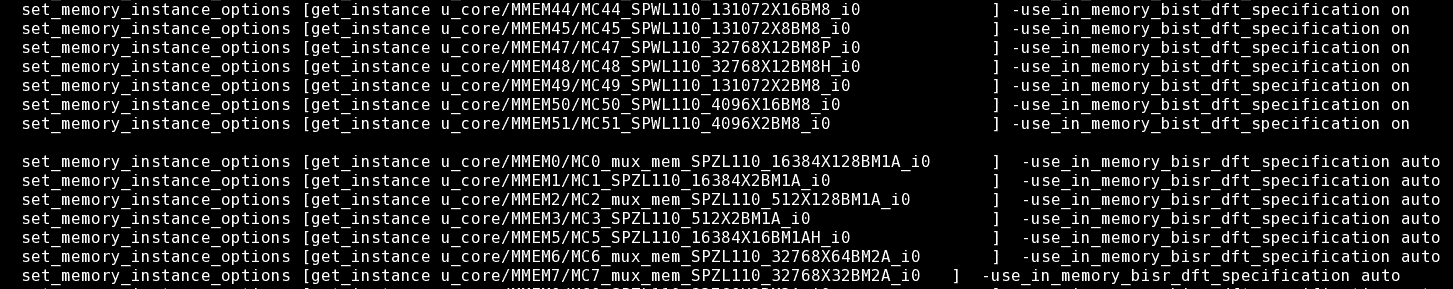
****

Figure 3 010A

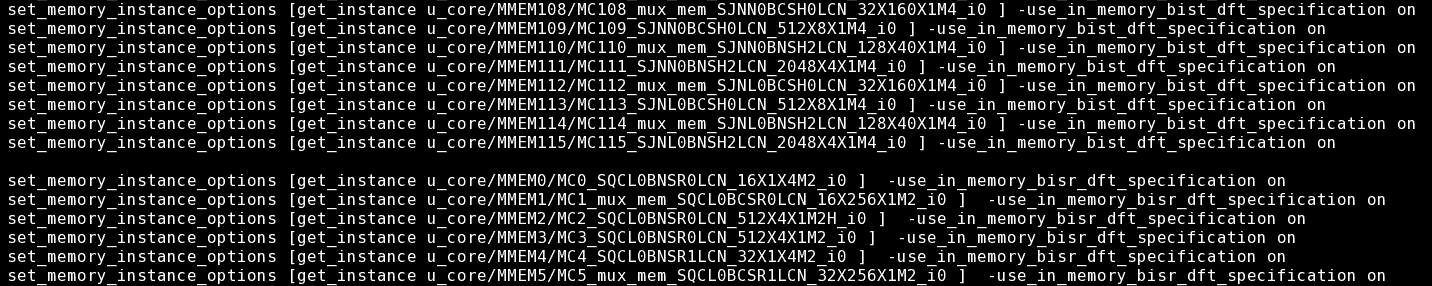
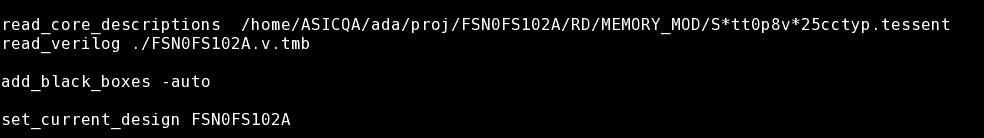
****

Figure 4 102A

***Difference between auto and on ?***

**File mbist\_insertion.dof**

****

Run mbist\_insertion → top\_tsdb\_outidr/…/FSR0FA010A.vg

Modify file *.synopsys\_dc.setup*





|  |  |  |
| --- | --- | --- |
| Output: |  | FSR0FA010A.vg |
|  |  | FSR0FA010A.sdc |

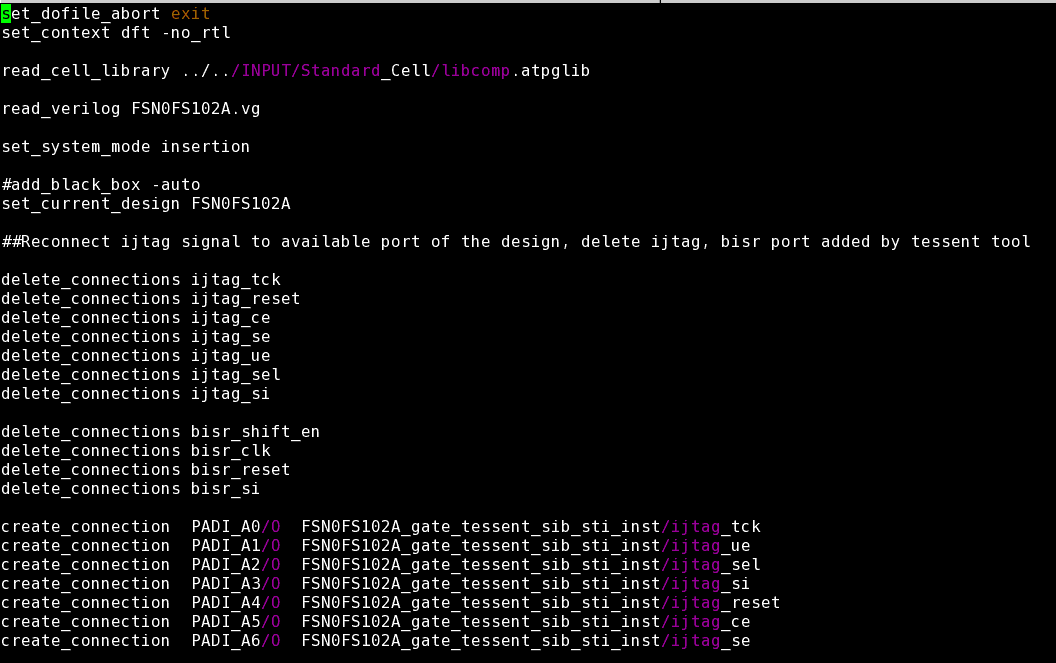
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **<Project>\_ts\_post.cmd** | | |  |  |  |  | | |  | |  |  |
|  | Intput |  | FSR0FA010A.vg | | # Netlist MBIST | | |
|  |  |  | <Project>\_ts\_post.cmd | | # Do file | |  | | |
|  |  |  |  |  |  |  | | |  | |  |  |
|  | Output: |  | FSR0FA010A.v.tstmb | |  |  | | |  | |  |  |

****

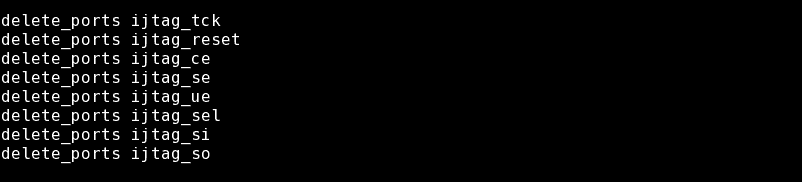
**Reading file** [T:\Vietnam\DSD\DSD\_ACD\ACT1\Tony\Post\_mbist\_eco.pptx](file:///T:\Vietnam\DSD\DSD_ACD\ACT1\Tony\Post_mbist_eco.pptx) **and refer Harry env.**

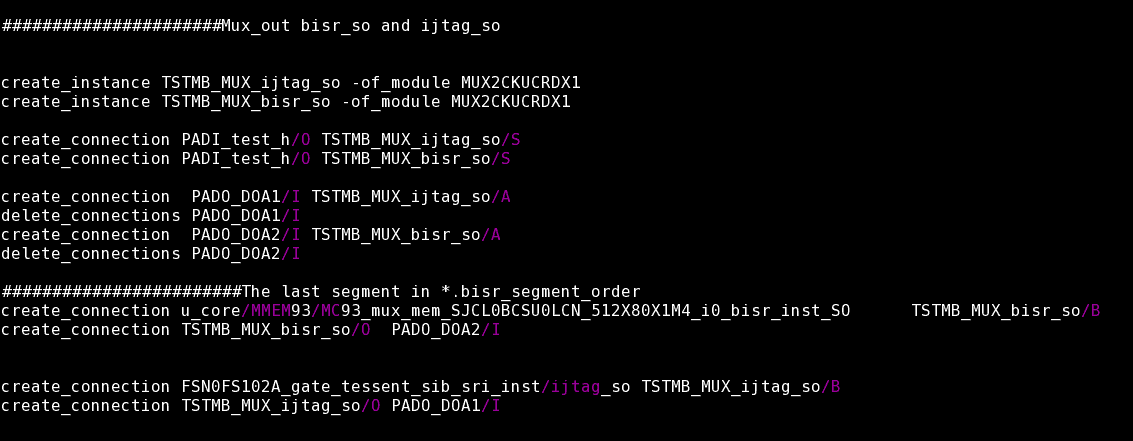
**Create file …\_ts\_post.cmd**

* **“Tessent tool insert ijtag port to netlist automatically, this increase port the design and is not allowed”**

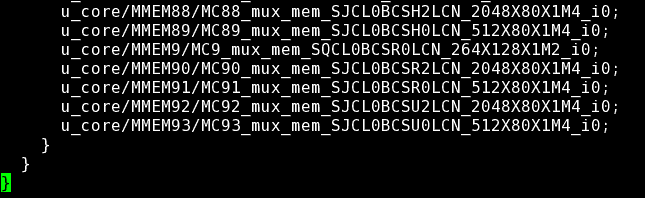
****

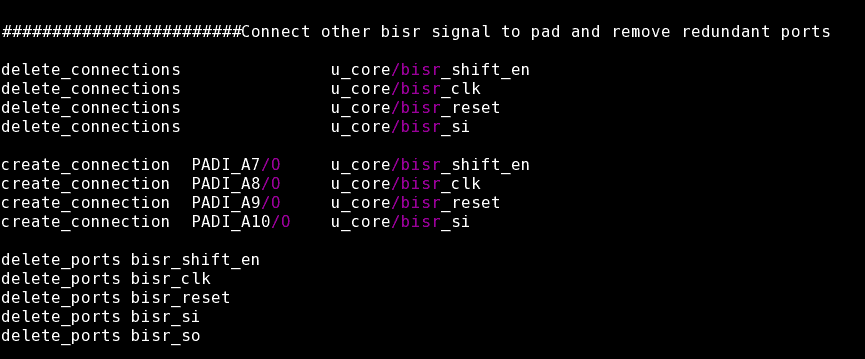
**Remove redundant port**

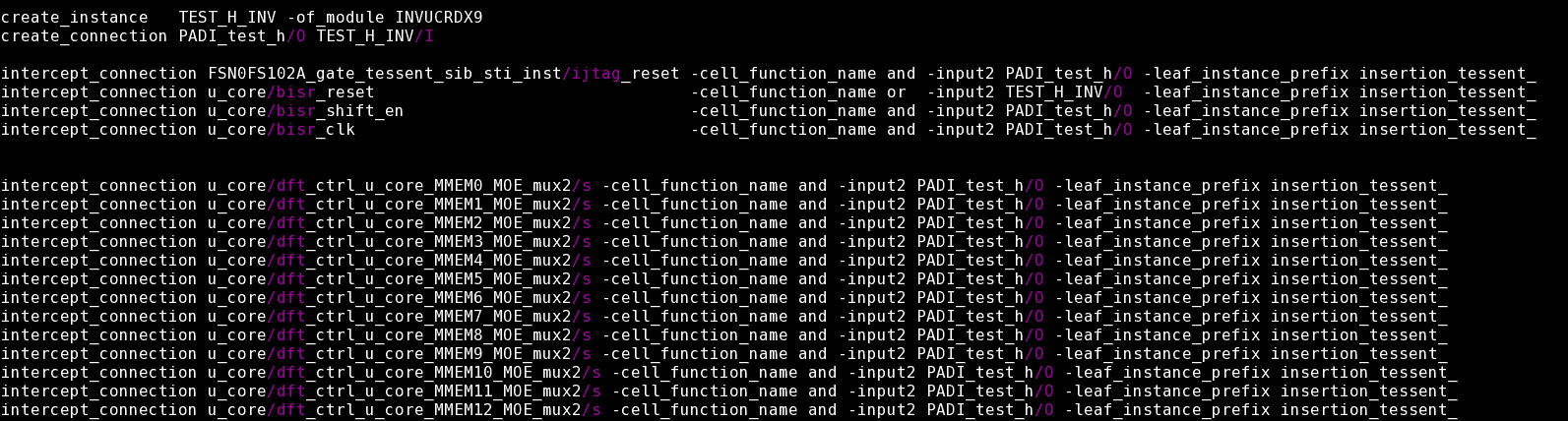
****

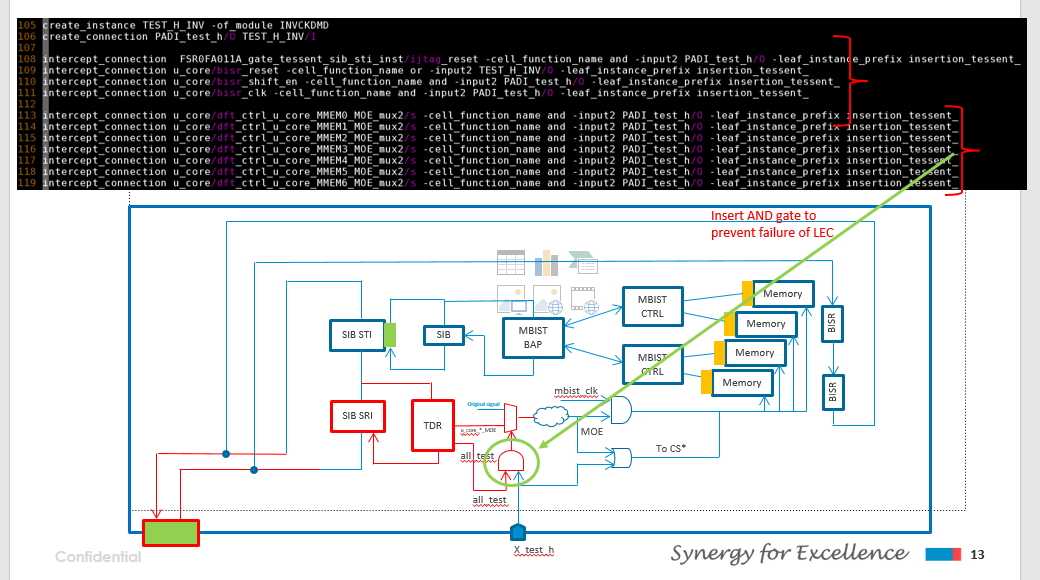
****

File ***FSN0FS102A.bisr\_segment\_order***

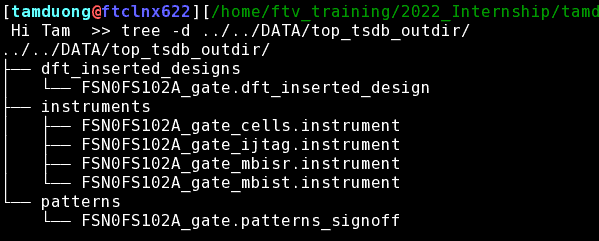
****

****

****

****

**After run project\_eco.cmd**

****

**Modify sdc**

**Make file mbist\_sdc\_tail.sdc**

Copy all the set hierarchy setting.

Add clock source macro hierarchy setting.

Add the set case analysis.

Modify the value of X\_test\_h and clock Selection.

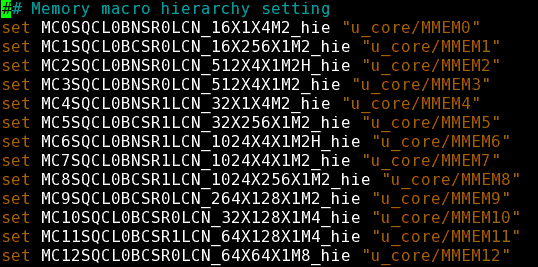


**\*set\_clock\_uncertainty: value in file sign-off**

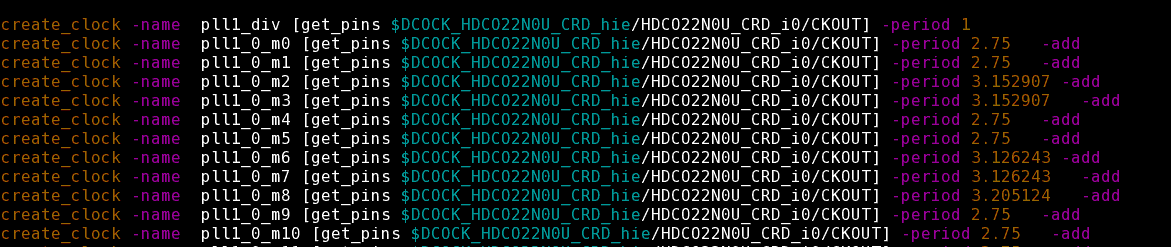
**\*bisr**

**Make file user\_clk.sdc**

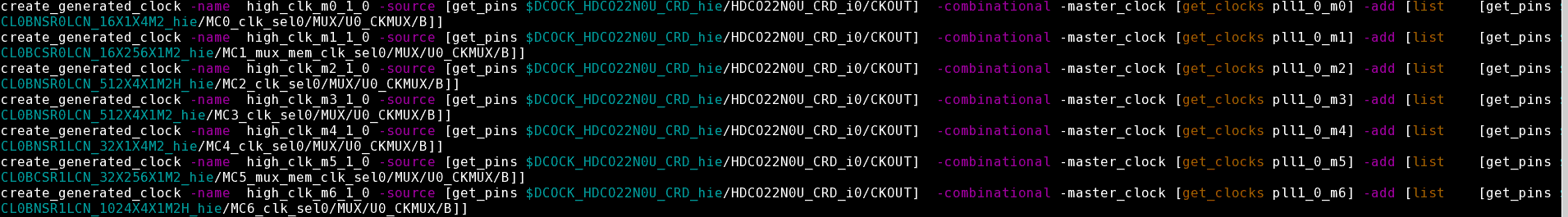
**Copy Memory macro hierarchy setting**

****

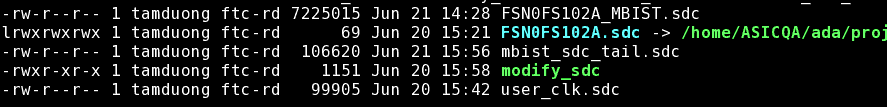
**Copy all the clock constraint**

****

**Copy all the clock constraint**

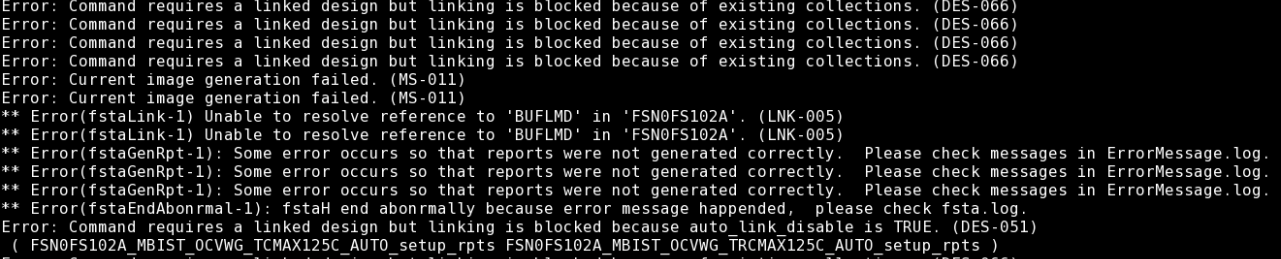
****

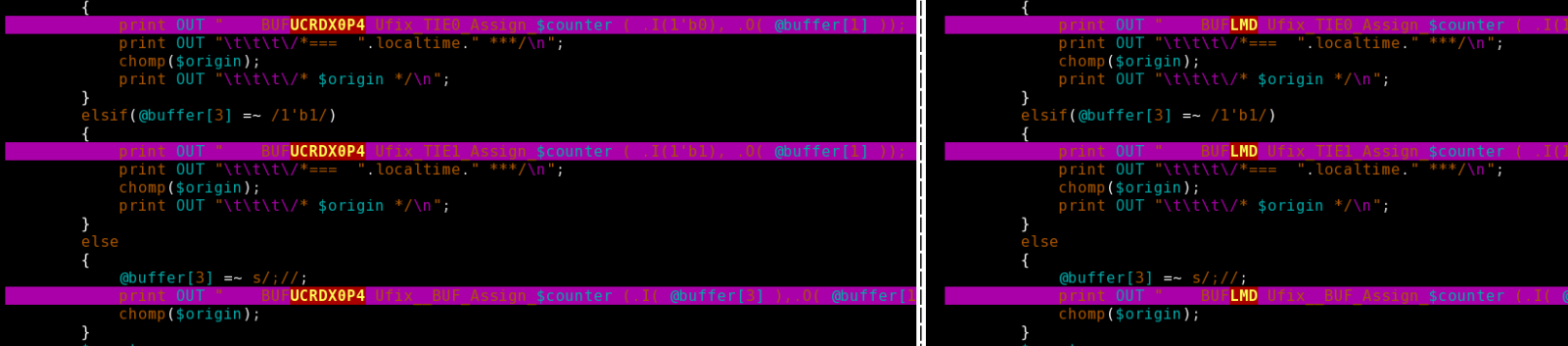
**After run**

****

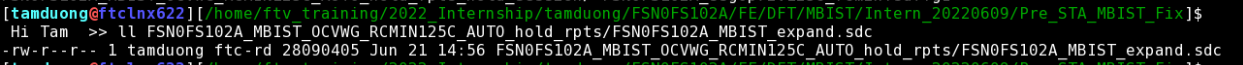
|  |  |  |
| --- | --- | --- |
| Output: |  | FSR0FA010A\_MBIST.sdc |

**Fix file Fix\_assign.pl**

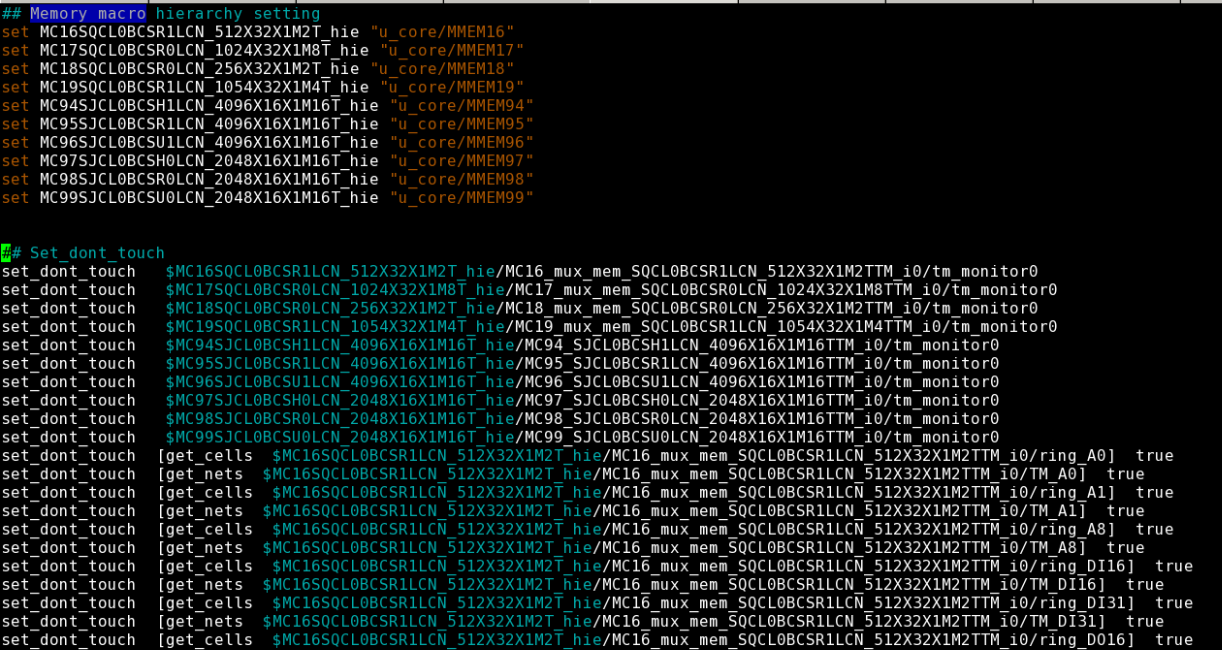
****

**eKMS => eDatabook => FSN0U\_CRD => BUF (BUFUCRDX0P4)**

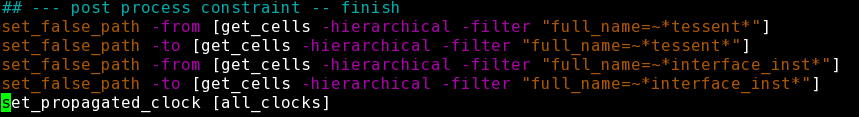
**Run Pre-STA**

****

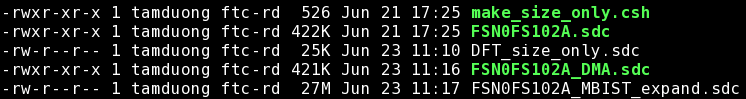
**DFT\_size\_cell\_only**

****

**Modify DMA.sdc:** Add the below part at the end of DMA.sdc

****

**Modify MBIST\_expand.sdc:** Set the propagated clock for the MBIST sdc

****

**Run Design tool kit check**

**Check FERC**

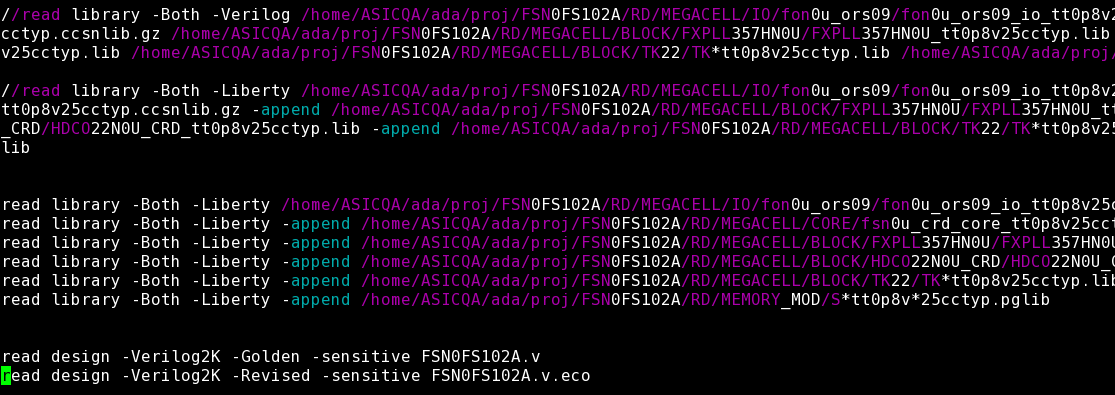
**Check FLEC**

**Check FSTA**

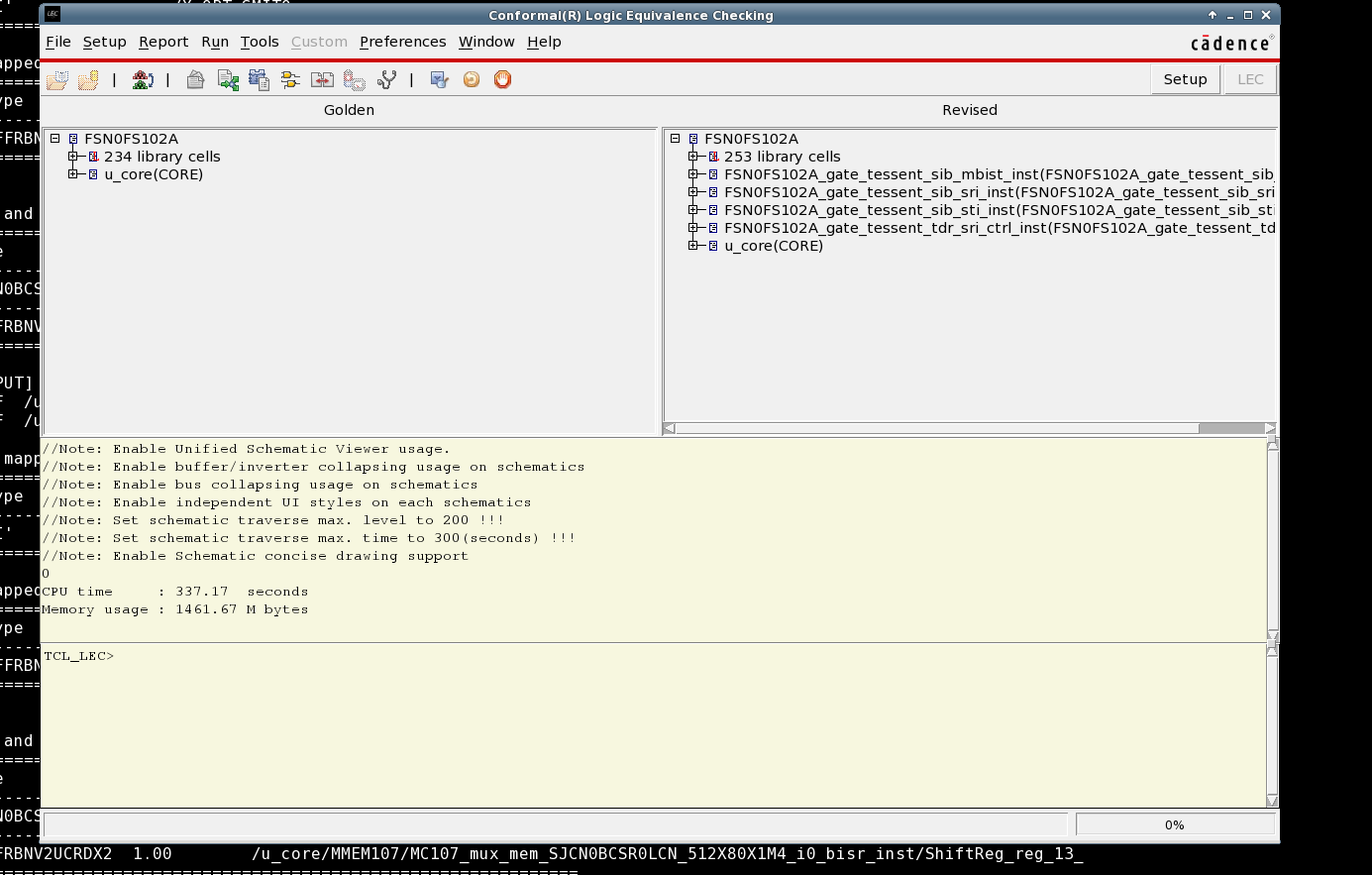
|  |  |  |  |
| --- | --- | --- | --- |
| Run | STA | for both new SDC | |
| >> | FSTA | MBIST\_expand.sdc | |
| >> | FSTA | DMA.sdc |

**Run FLEC**

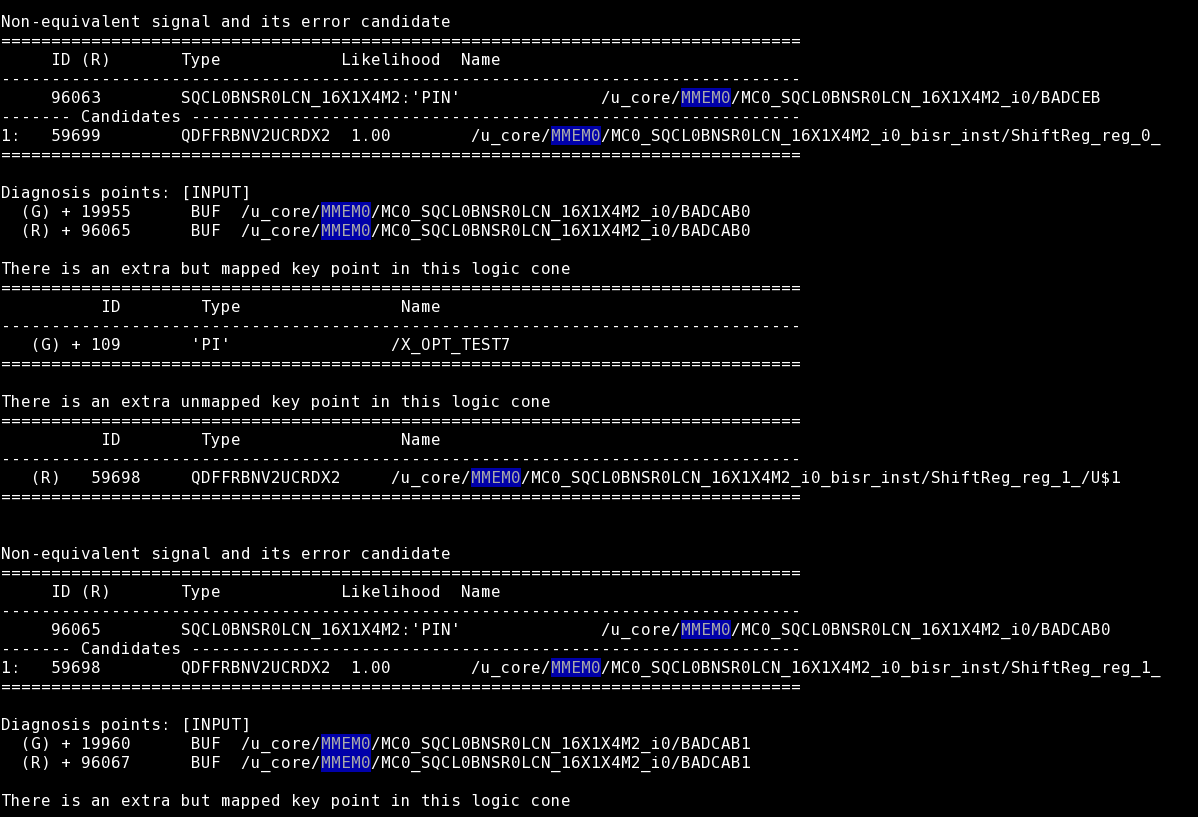
**Modify flec.cmd**

****

**When run flec will have GUI**

****

**Check flec.log**

****

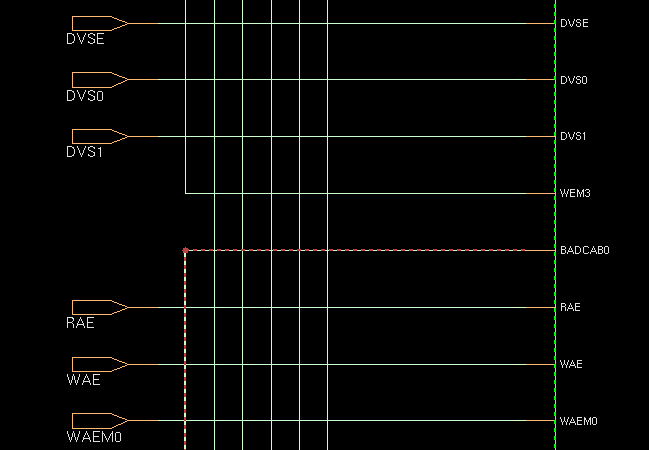
Mở Verdi kiểm tra, khi tạo ra bisr, đường tín hiệu của bisr sẽ được tao ra và nối vào mạch, làm mất đường function, nên flec bị fail. => Phải tạo ra một con mux để lựa chọn test mod hay function mod.

**ECO netlist**

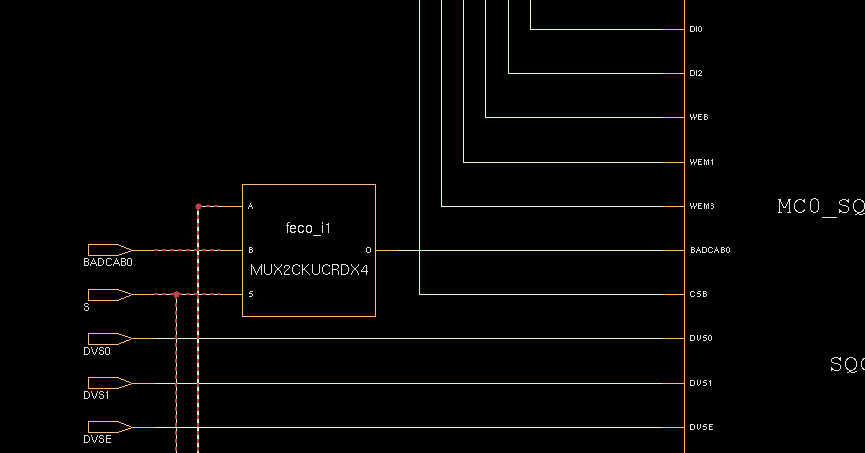
**<netlist>.v**

****

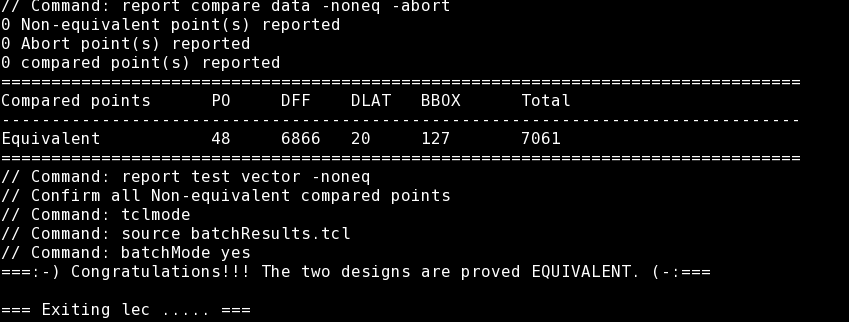
**<mbist netlist>.v**

****

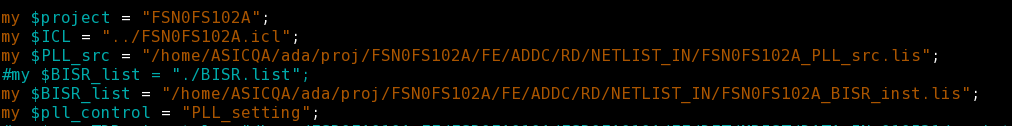
**<netlist>.v.eco**

****

**Result =>**

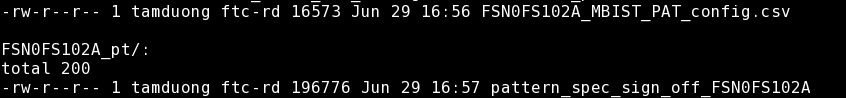
****

**Summaries data**

****

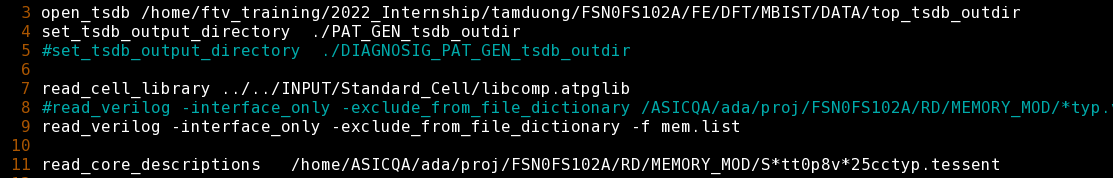
**PLL\_setting ?** (.ftlcon)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| >> | ./sum\_mem\_info\_new.pl -gen\_db | | | |  |
| Output: |  | FSN0FS102A\_MBIST\_PAT\_config.csv | | | |
|  |  |  |  |  |  |
| >> | ./sum\_mem\_info\_new.pl -gen\_pt | | | |  |
| Output: |  | FSN0FS102A\_pt | |  |  |

****

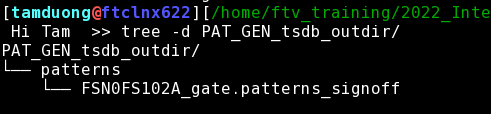
**Gen-pattern**

**Modify** mbist\_pattern\_gen.dof



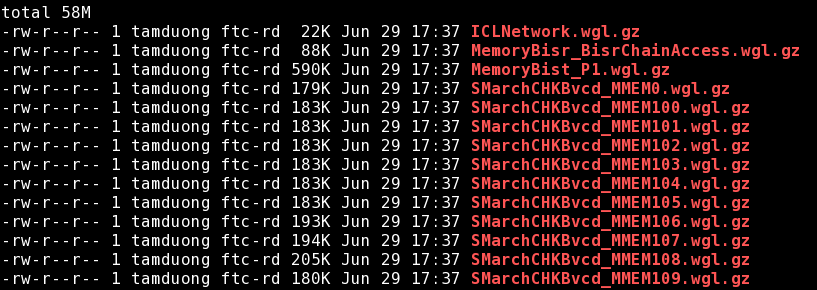
****

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| >> | ./run\_gen\_pattern |  |  |  |  |  |  |  |
| Output: | ./PAT\_GEN\_tsdb\_outdir\_Practice\_Data/patterns/FSR0FA010A\_gate.patterns\_spec\_signoff | | | | | | | |

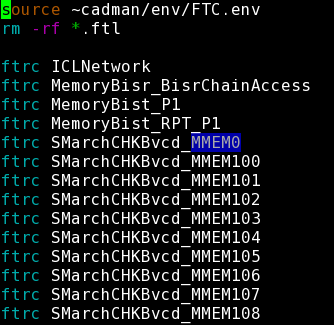
****

**Resequence pattern**

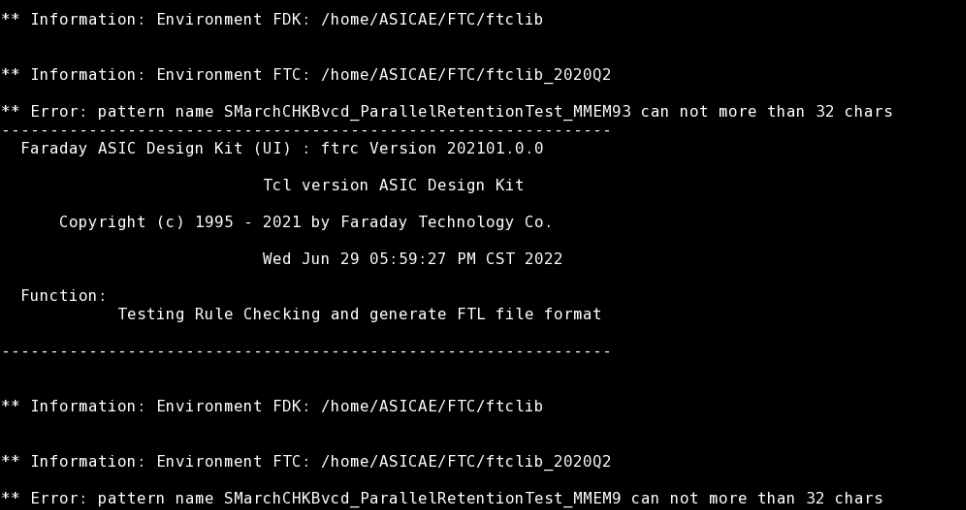
**Copy pattern file => wgl\_pt**

****

**Create file pt\_cv.csh**

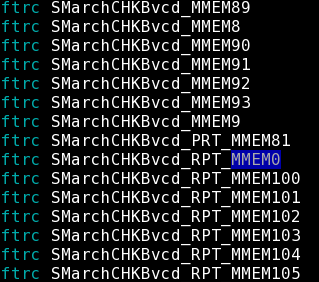
****

**Run script file =>**

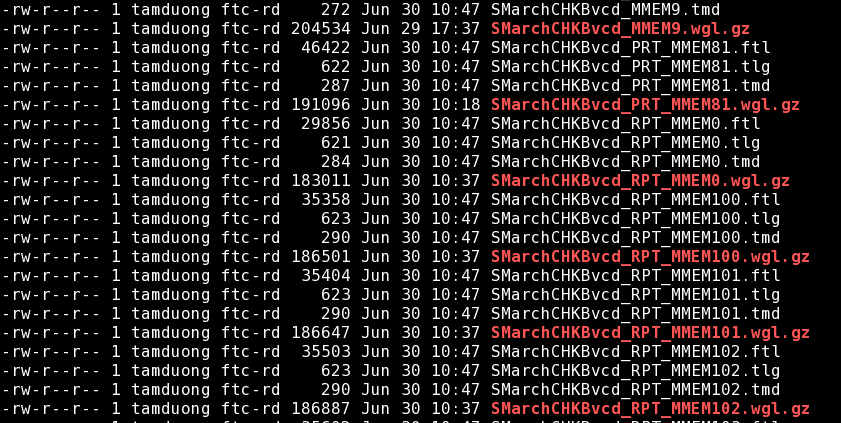
****

**Error: Name can not more than 32 chars => rename file pattern.**

awk -F "\_" '{print "mv " $0 " "$1"\_RPT\_"$2"" }' file\_name >> rename\_pattern\_file

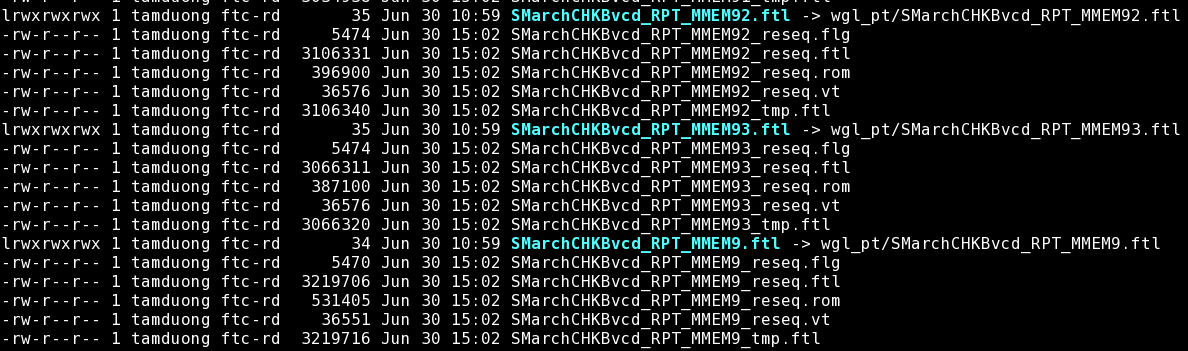


|  |  |  |
| --- | --- | --- |
| **Run script file** | |  |
| **>>** | **source** | **pt\_cv.csh** |
|  |  |  |
| Ouput: |  |  |

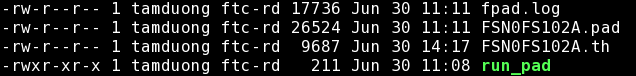


Recequence pattern

Link the .ftl file



Run fpad



Modify .th

|  |  |  |  |
| --- | --- | --- | --- |
| # | Run gen pattern | |  |
| >> | ./gen\_vt.csh | |  |
|  |  |  |  |
| Output: |  | <pattern>.rom | |
|  |  | <pattern>.vt | |

Summary Final Report

How to built basic setup file to run ferc, fsta, flre.

Trong project 010A chỉ được làm quen với flow chạy của MBIST là như thế nào, các file hầu như đã có sẵn, chỉ chạy theo flow và hiểu nó hoạt động như thế nào, gồm những bước gì.

Đến với 102A, có được thêm những khái niệm về MBIST là gì, MISR, BISR, BIRA.

Cách tạo ra file setup, các thông số cơ bản cần phải define trong file setup để chạy fsta, ferc, flre.