|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Nguyen Anh Huy | No. | T062 | Div/Dept | DSD/ACD/ACT2 | Job  Date：2022/09/30  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 🗹W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. Introduce fstaH   + Task: Read slide, search in eFaraday.  + Achievement: Know about STA tool using in Faraday.   1. Execute fstaH   + Task: Read slide.  + Achievement: Know how to run STA for pre-layout.   1. Test Chip: Insert MBIST to the design   + Task: Read slide, excel, taking trial in Linux environment.  + Achievement: Know detail how to insert MBIST in Test Chip flow. |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Issue: * Have trouble while trying to figure command purpose. * Some docs and web can’t access using company mail. * How to solve: * Ask mentor for these command. |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Continue running Test Chip flow |
|  |

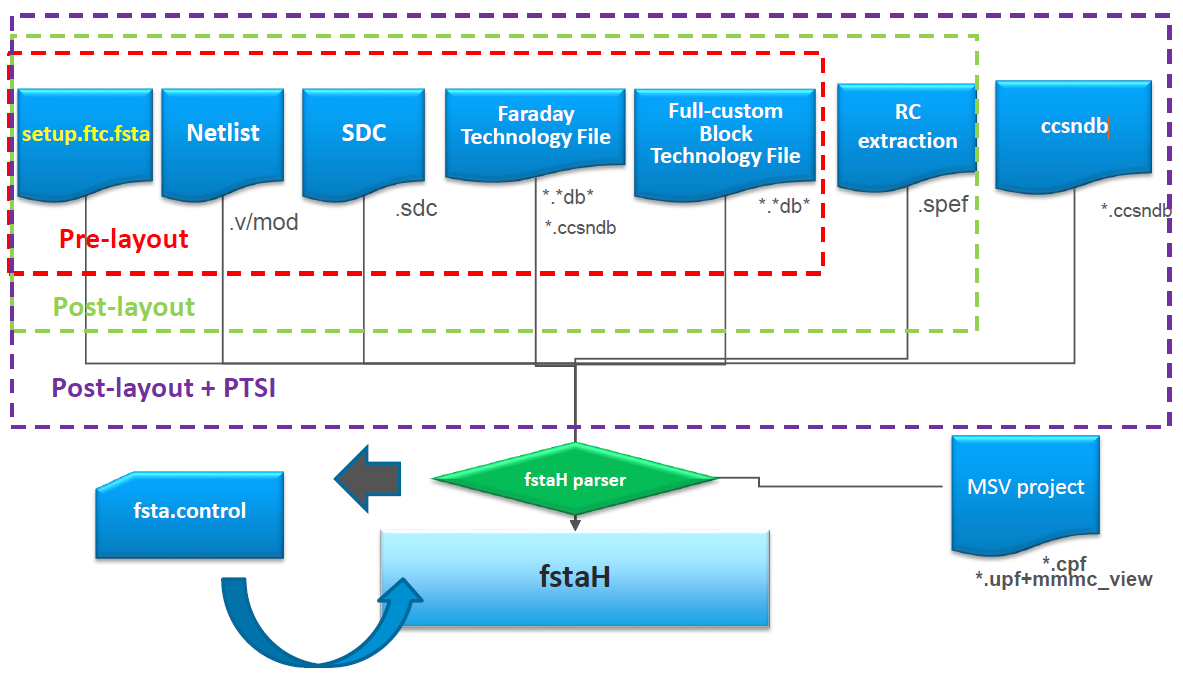
|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Huy Nguyen (2022/09/30) | (Signature/Date) | (Signature/Date) |

【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.

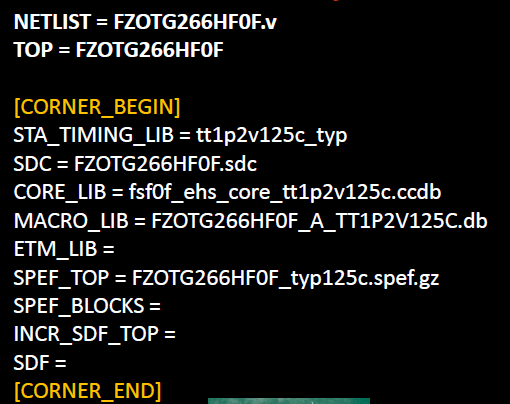
# Introduce fstaH

fstaH is a Faraday tool kit that help user perform Static Timing Analysis on ASIC designs, this UI employs the commonly-used static timing analysis tool, PrimeTime, as the analysis engine.



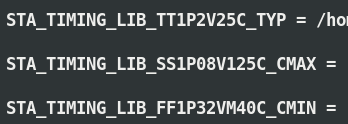
Input of fstaH include

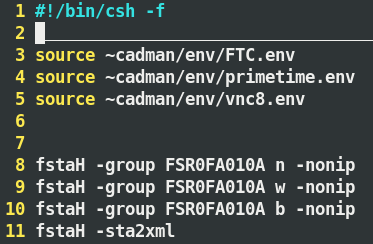
* Setup.ftc.fsta
* Netlist
* SDC:
* Faraday Technology File
* RC Extraction
* Ccsndb
* MSV project (.cpf: Cadence power format, .upf: unified power format, .mmmc: multi mode multi corner file during the physical design gives the analysis of the design over varied modes & corners.)
* .cpf file is Cadence Power format, which describe the features of the multi-voltage project. This is only required if users run fstaH with the CPF-in flow syntax.
* Fsta.control: After fstaH parser will generate a file, which contain information for fstaH to run

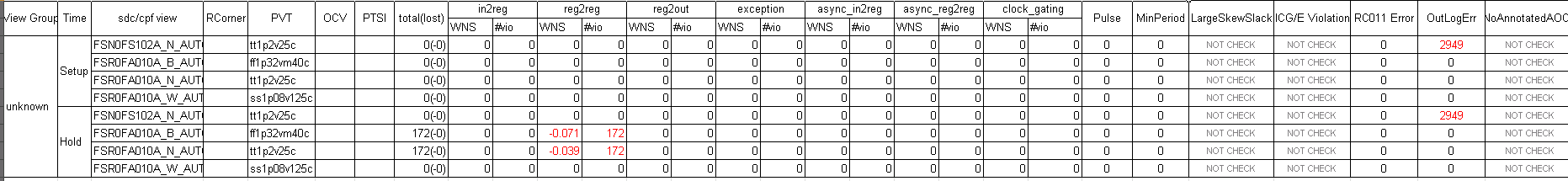


# execute fsta

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/Fsta/Pre\_STA/Dtb





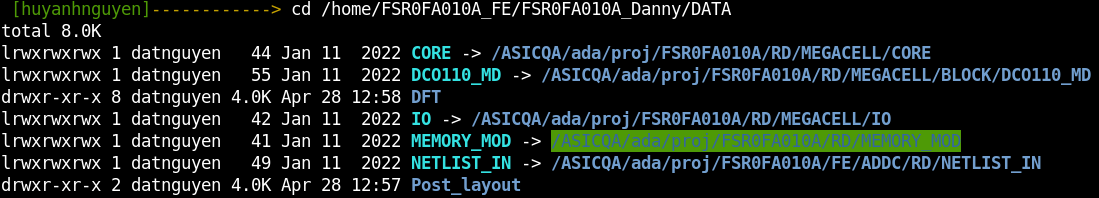


# mbist\_test chip

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/

## input data for project

My mentor gave me a link which contain data for this project



## compile standard library to tessent library

**Woriking directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/INPUT/Standard\_Cell

|  |  |
| --- | --- |
| **INPUT** | |
| libcomp.do.default | # file contain command to translate models to library |
|  | |
| **EXECUTE** | |
| run\_libcomp | # file contain directory to source to environment |
|  | |
| **OUTPUT** | |
| libcomp.atpglib | library file |
|  | |

## mbist insertion

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/MBIST\_insertion

### FSR0FA010A\_ts\_pre.cmd

|  |  |
| --- | --- |
| **INPUT** | |
| <Project>.v | # Netlist |
| <Project>\_ts\_pre.cmd | # Dofile: Insert or gate to test\_h signal to control clock, could be modified base on each project |
|  | |
| dft\_cell\_select.tcl | # Default |
|  | |

**Execute command:** tessent -shell -dofile FSR0FA010A\_ts\_pre.cmd -logfile FSR0FA010A\_ts\_pre.log –replace

|  |  |
| --- | --- |
| **OUTPUT** | |
| <Project>.v.tmb | # Netlist after running this step |
| <Project>\_ts\_pre.cmd.log | # log file include contain from terminal |

### MBIST Insertion

To start running Mbist insertion, user have to prepare input data first

|  |  |  |
| --- | --- | --- |
| **INPUT** | | |
| mbist\_insertion.dof | Default | # Insert mbist circuit, could be modified based on feature of type and project |
|  | | |
| go\_make\_add\_clock.csh | Default | # Script to extract clock period, output is add\_clock.dof |
| FSR0FA010A\_PLL\_src.lis | RD | # PLL clock source list for memories, use script to generate .dof file from this file |
| Instance\_need\_MBIST.dof | Create | # Set memories instance option for BIST and BISR |
| func\_debug | Default | # run to debug function of the design |
| .synnosyp\_dc.setup | Default |  |
|  | | |
| clock\_fix\_drc\_setting.dof | Create | # add pin and pin constraints to memory |
| rom\_content.dof | Create | # Rom code file pattern |
| mem.list | Create | # memories list path |
| register\_tdr.dof | Create | # set static register static dft signal |
| add\_clock.dof | Create | # Clock period file |

Mem.list, add\_clock.dof, register\_tdr.dof, Instance\_need\_MBIST.dof, rom\_content.dof have been generated by user.

Execute file: run\_mbist

#### Create mem.list

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/MBIST\_insertion/script/

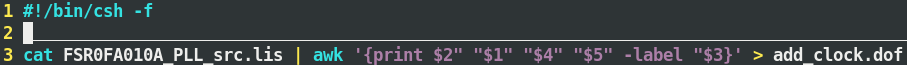
To create mem.list, user have to extract all memory file into mem.list

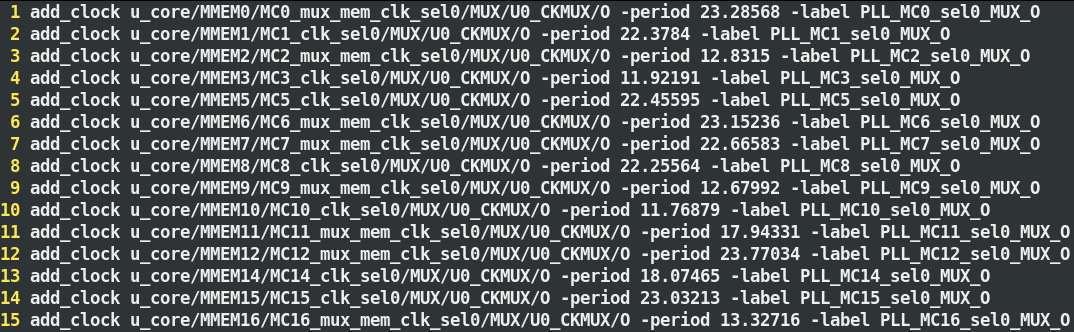




#### Create add\_clock.dof

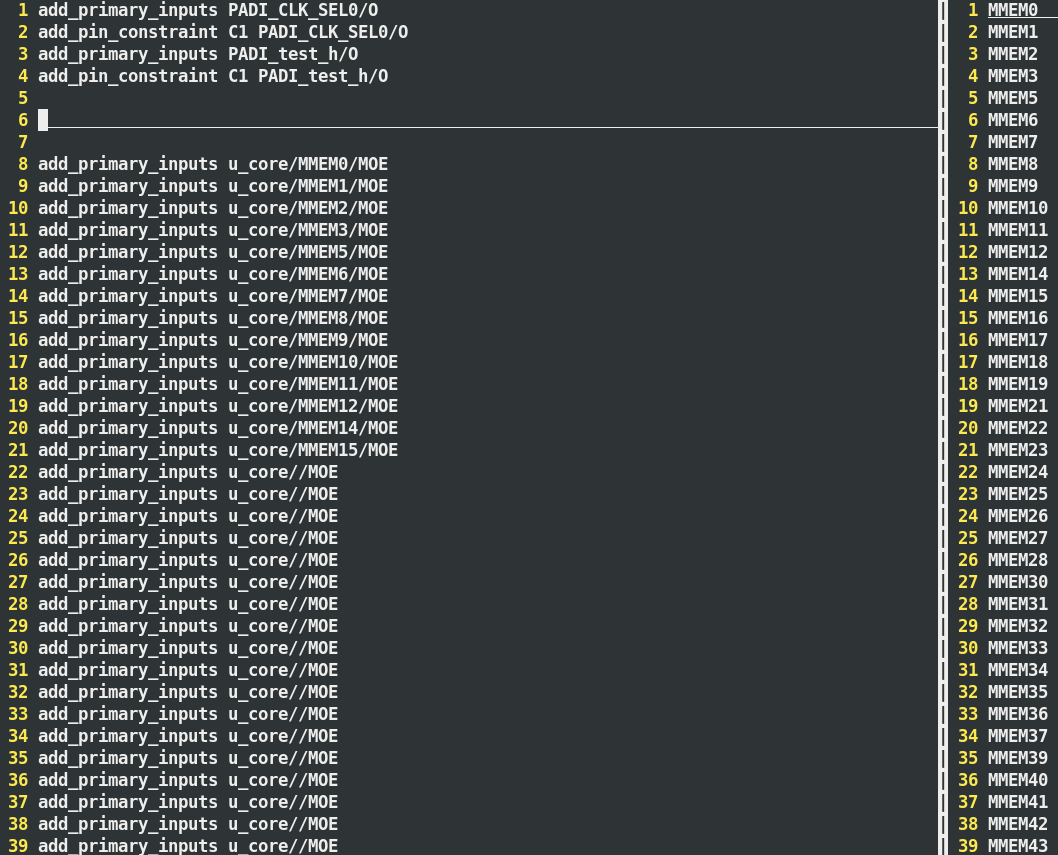
This file have script to generate this file, to generate add\_clock.dof, user have to put script file and FSR0FA010A\_PLL\_src.lis at the same directory.



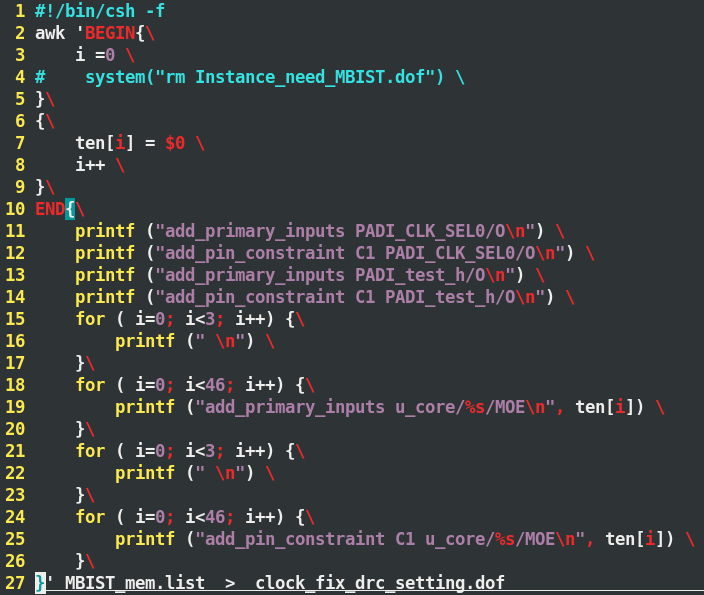


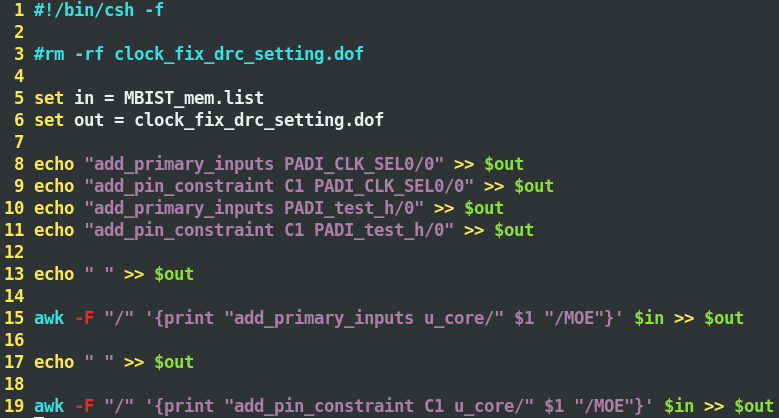
#### Create clock\_fix\_drc\_setting.dof

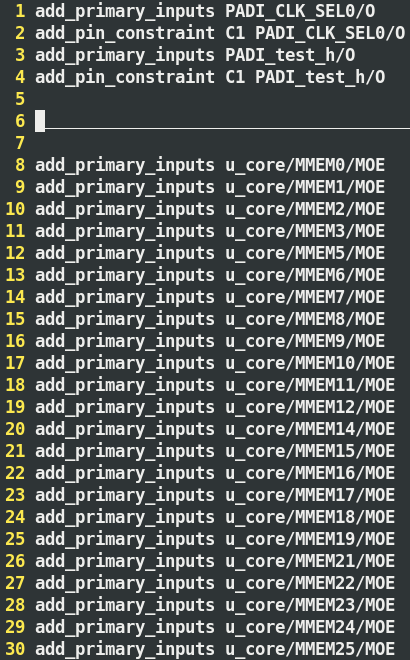
At the beginning, there isn’t script to create clock\_fix\_drc\_setting.dof, so I have to make this file by hand.



To create this file, I have to create a script to generate clock\_fix\_drc\_setting.dof. This script and MBIST\_mem.list have to be same directory to create this file.

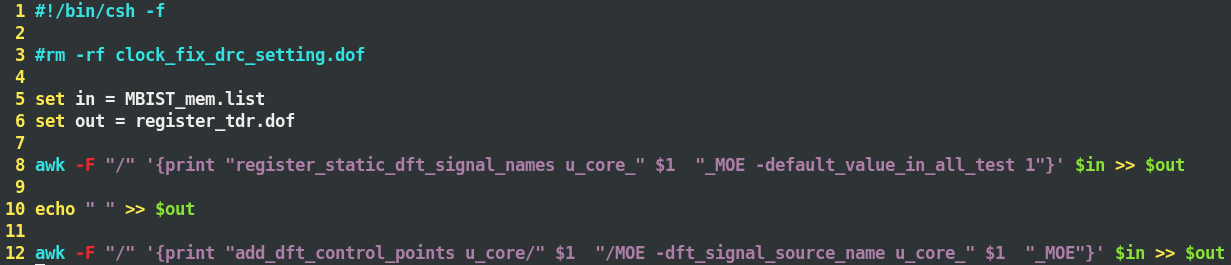


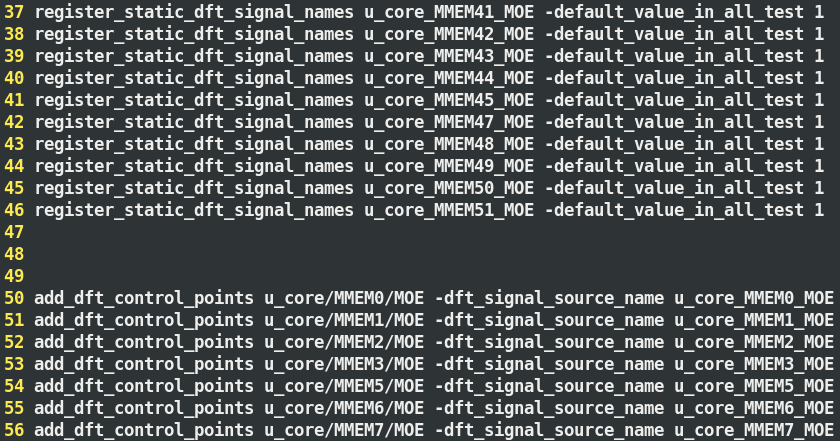




#### Create register\_tdr.dof

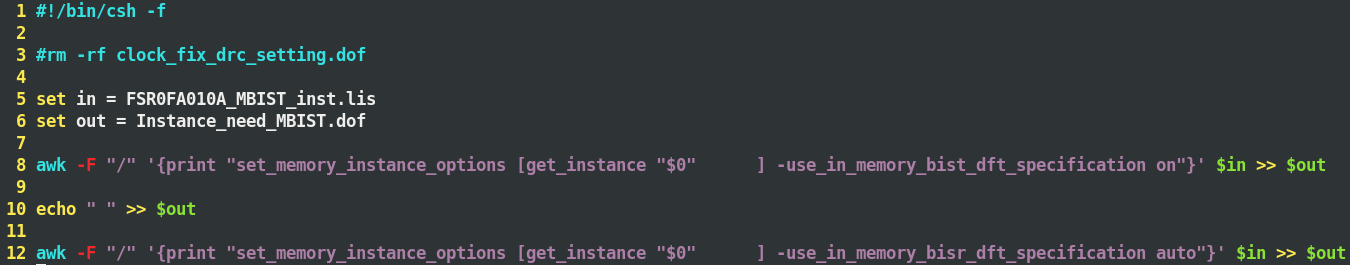


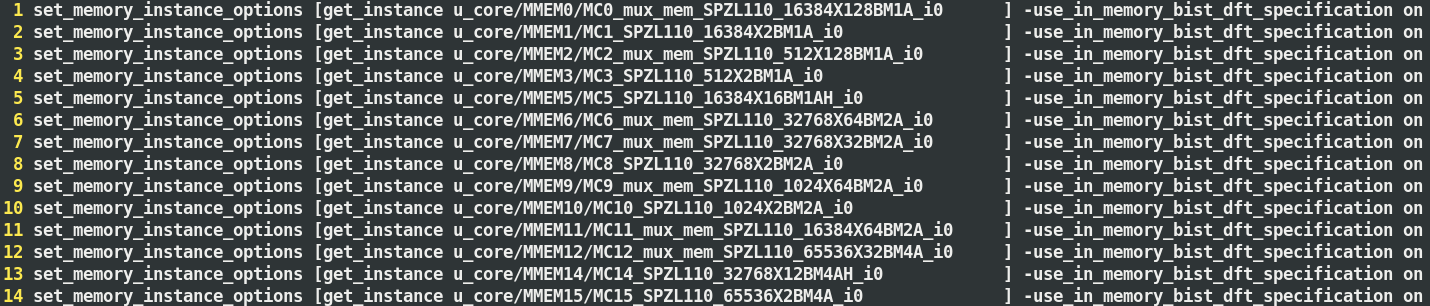




#### Create Instance\_need\_MBIST.dof

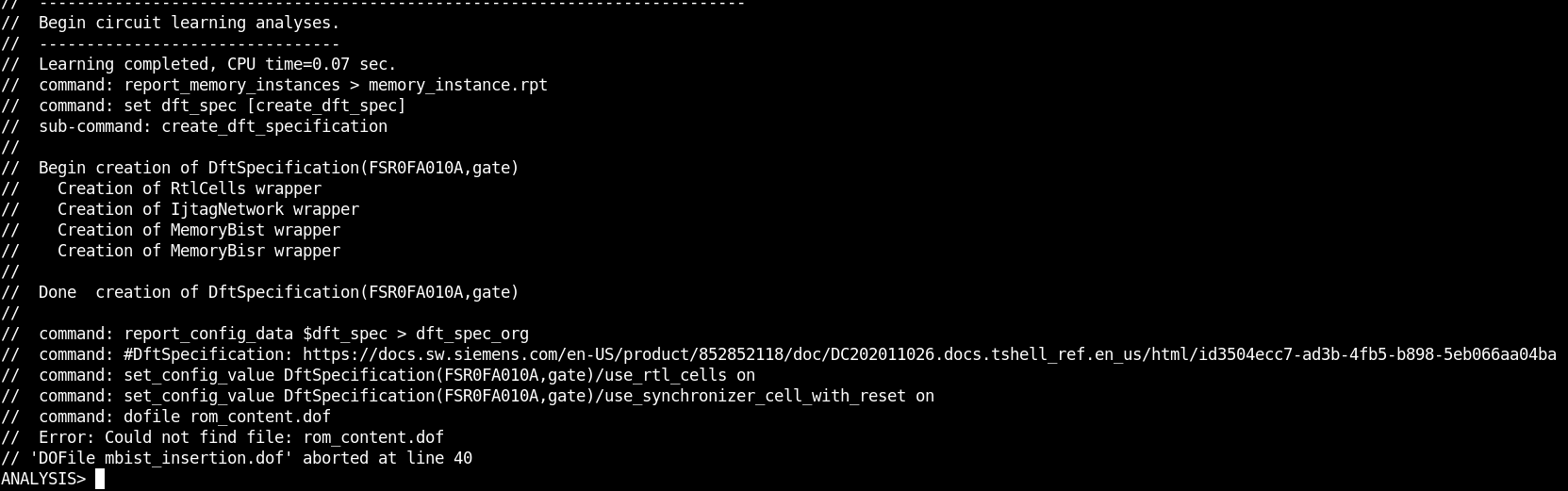






#### Insert MBIST first time

First time running insert MBIST, tool will detech that there is a missing file while running mbist\_insertion.dof. So the tool will stop execute and generate dft\_spec.org file



#### Create rom\_content.dof





#### Pre-insert MBIST

Run MBIST insertion step again to insert to design after create rom\_content.dof

