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| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Nguyen Anh Huy | No. | T062 | Div/Dept | DSD/ACD/ACT2 | Job  Date：2022/10/07  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | 🗹W1 □W2 □W3 □W4 | | | | | |
| Third month | □W1 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. Test chip: MBIST Insertion   + Task: Read slide, practice to apply MBIST to the netlist.  + Achievement: Know the flow how to insert MBIST.   1. Test chip: Modify SDC   + Task: Read slide.  + Achievement: Know how modify SDC.   1. Test chip: Run design toolkit check   + Task: Read slide.  + Achievement: Know validate the design after MBIST insertion. |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Issue: * How to solve: |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Run step gen pattern and run pre-sim in TestChip flow. |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Huy Nguyen (2022/10/07) | (Signature/Date) | (Signature/Date) |

【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. Why there is only 4 main corner: best case, best hot case, worst case, worst cold case ?

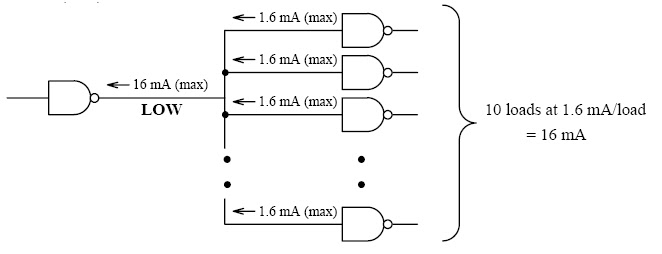
There isn’t

1. What is OCV ?

OCV (On Chip Variation): when the chip is completedly manufactured, there is some part on the chip will work in different variations, these different is called OCV. We have to take care these parameter because this can affect to the arrival time and required time of the signal in the timing paths.

1. What is the purpose to set max fanout ?

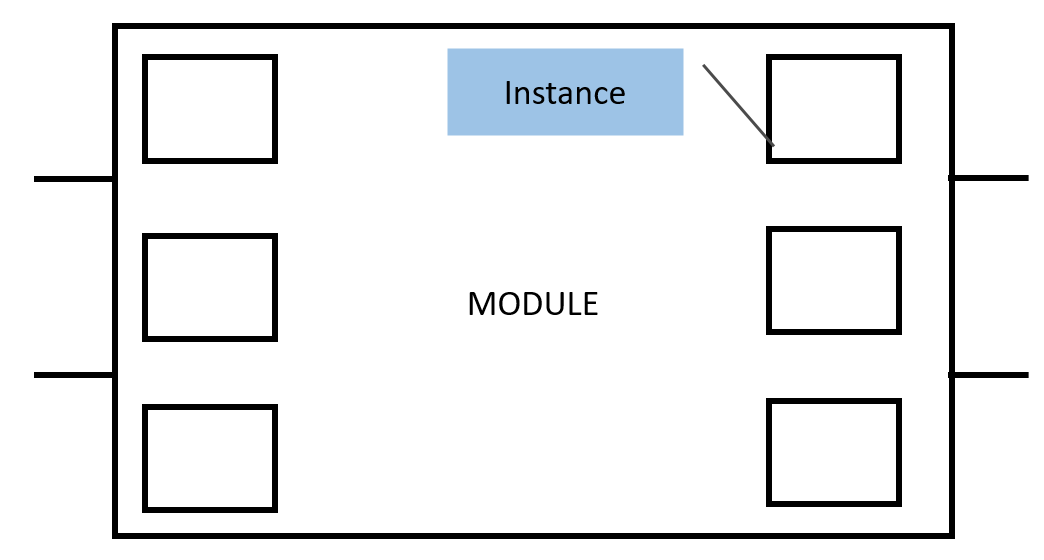
Because each cell have a specific current to drive cell, so we have to limit the number of driven cell to ensure that that cell have enough current for those cell.



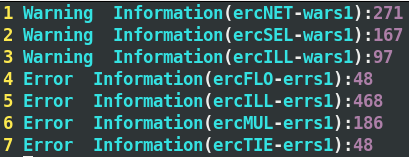
1. What is module and instances

Module contain a lot of logics inside.

Instance is a module till it is called from other module.

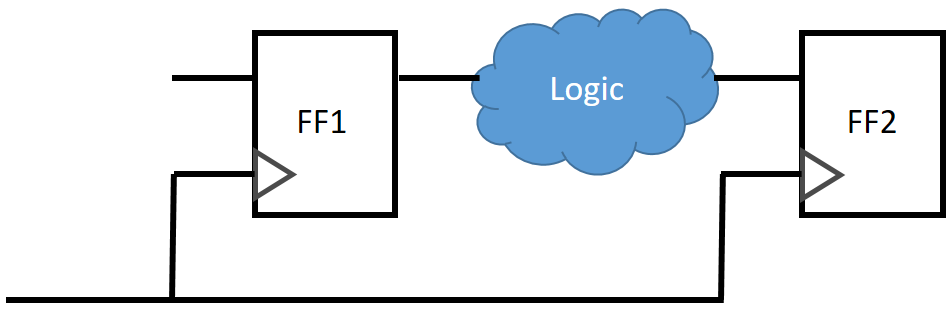


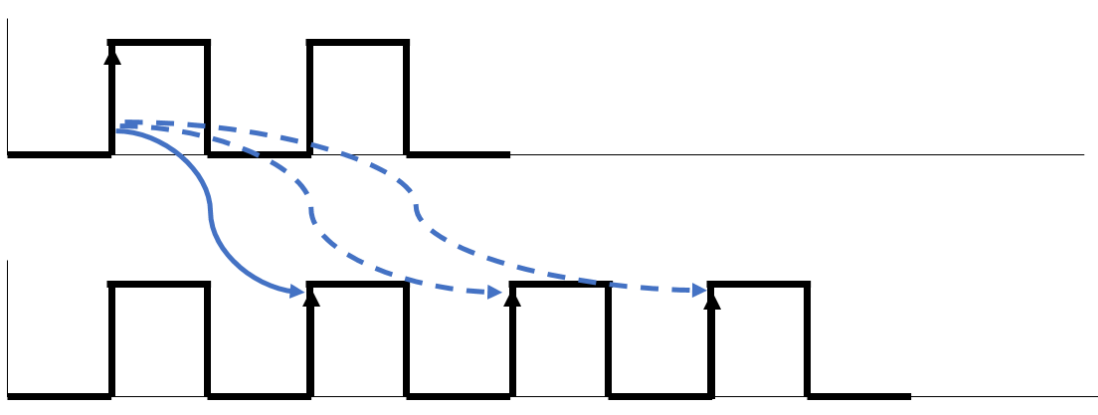
1. Write script to summarize all error from ferc.log file.



1. What is the multicycle path ?

Multicycle path is an exception that will be apply when combination logic delay in between flops take more than 1 cycle.



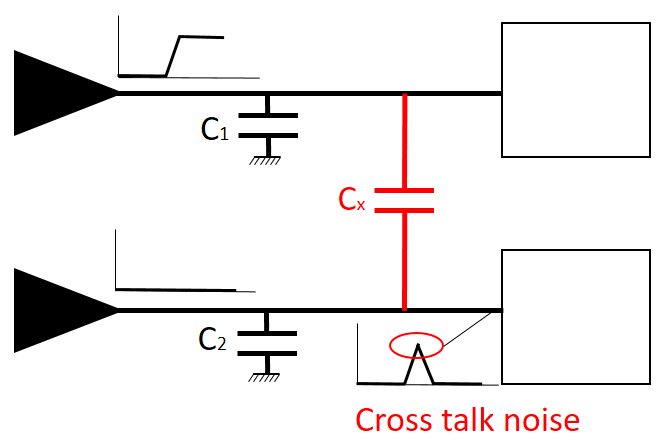


1. What is behavior level ?

Behavior level contain procedural, which control manipulate variables of the data types. Normally people will use truth table to design based on specific output.

1. What is crosstalk ?

Crosstalk is a undesired issue when logic transmitting of one net because of switching of the nearby net.



1. What is SI ?

SI (Signal Integrity) is to ensure reliable, high-speed data transmission from one point to another point inside the chip.

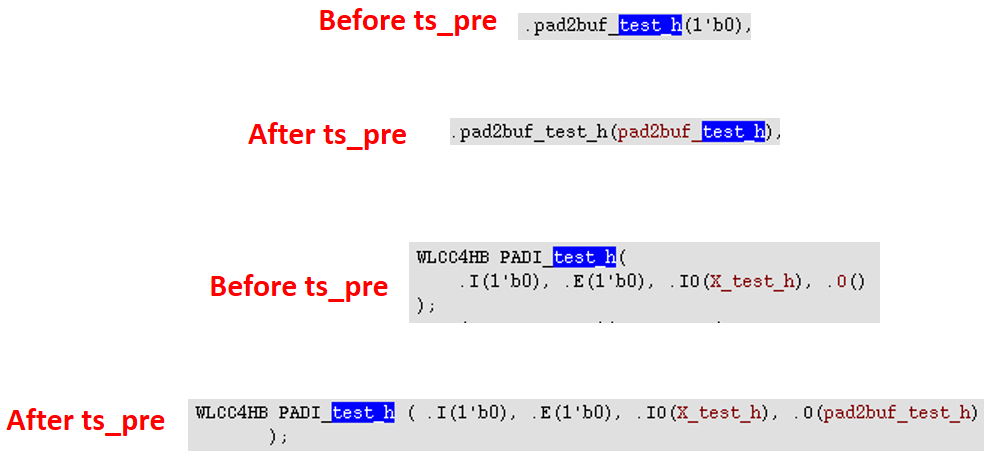
1. What is FF and SS in PVT go for ?

FF or SS is determined the parameter of MOS

Ex: FF: Fast nMOS Fast pMOS

Fast mean the the current in the design run faster than normal.

1. What is the difference between <project>.v.tmb and <project>.v ?



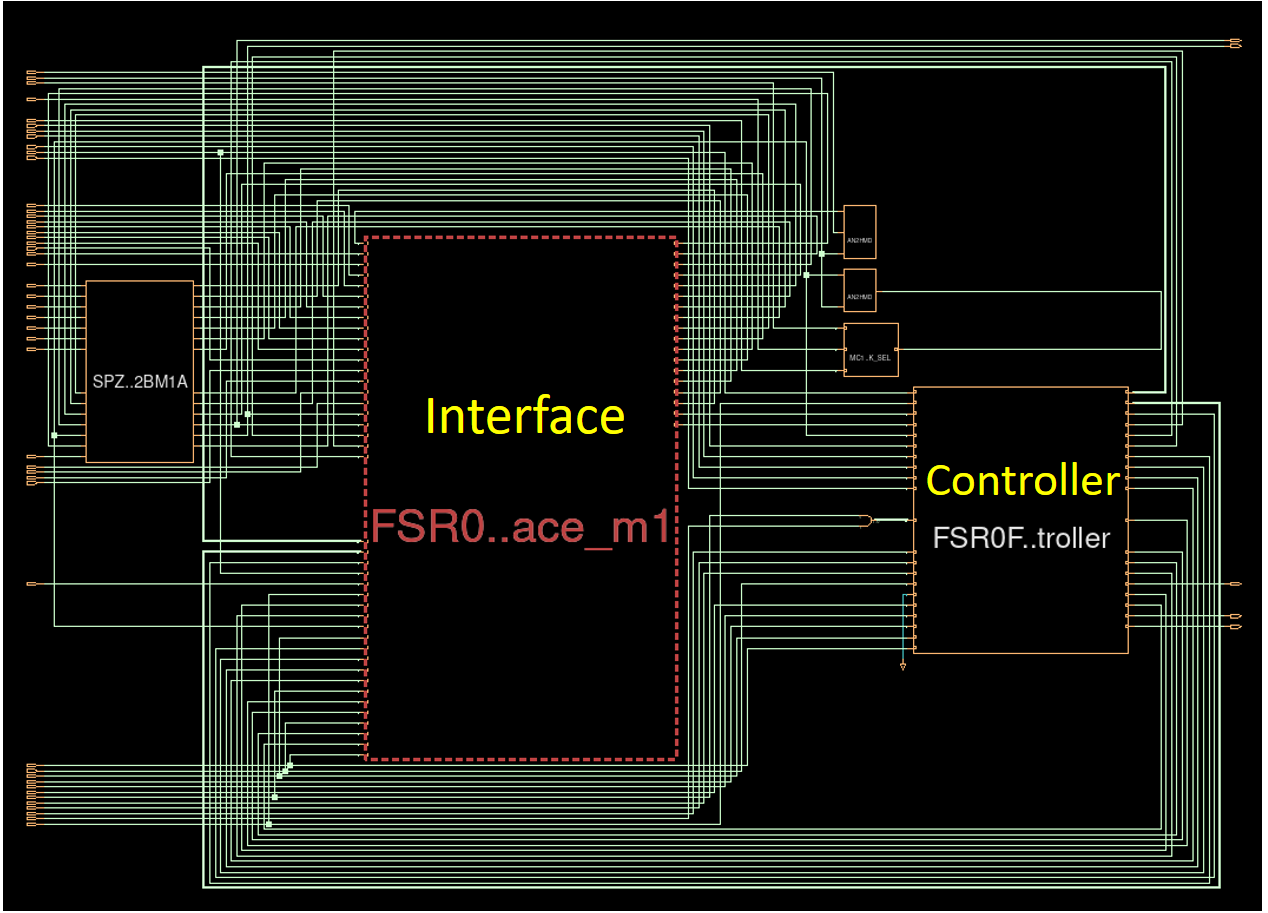
1. What is test\_h signal ?

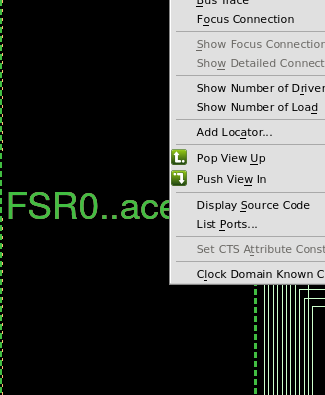
test.h signal is a signal that allow user can choose which mode the design will perform. 0 mean perform function mode and 1 mean perform dft mode.

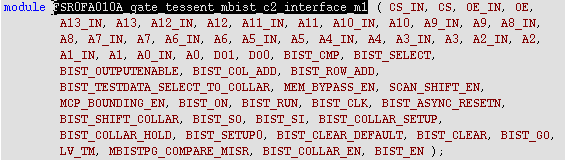
1. What is “C1” in add\_pin\_constraint mean ?

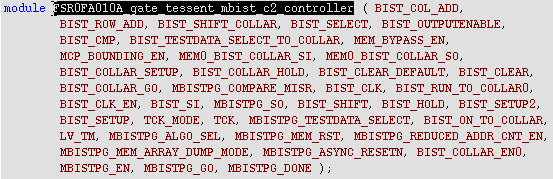
Define the DFT scan mode is C1.

1. Find the interface module and controller module in Verilog file.







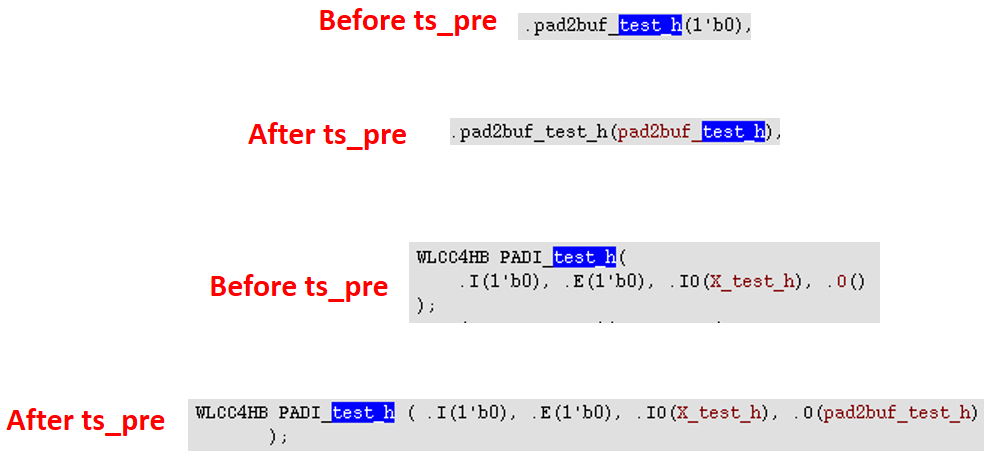


# Test chip: MBIST Insertion

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/MBIST\_Insertion

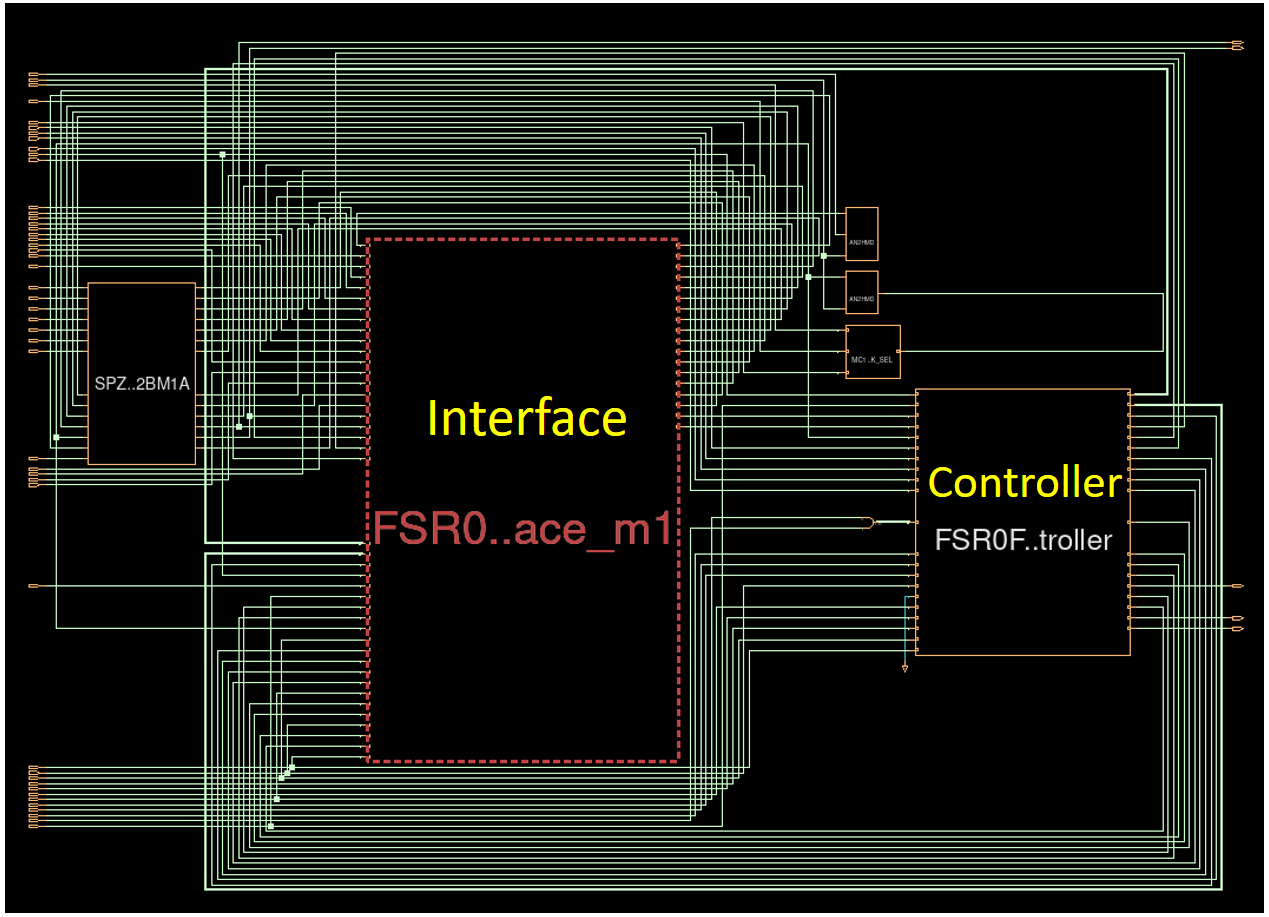
## FSR0FA010A\_ts\_pre.cmd

test.h: signal allow us user can choose the design work as function mode or dft mode. 0 mean running function mode and 1 mean running dft mode



## MBIST insertion

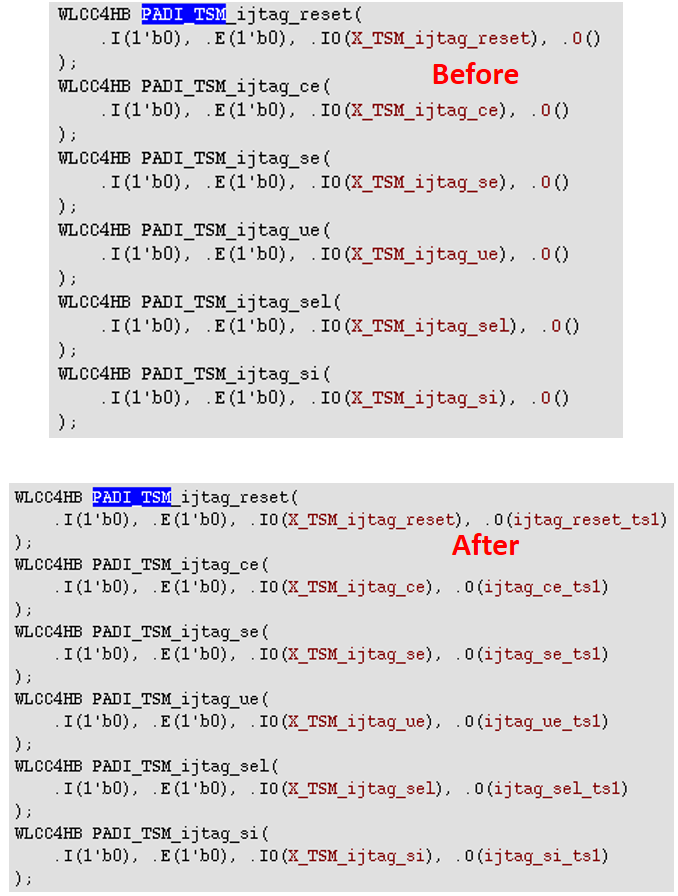
After this step, script will insert 2 new module to the MEM: Interface module and Controller module.



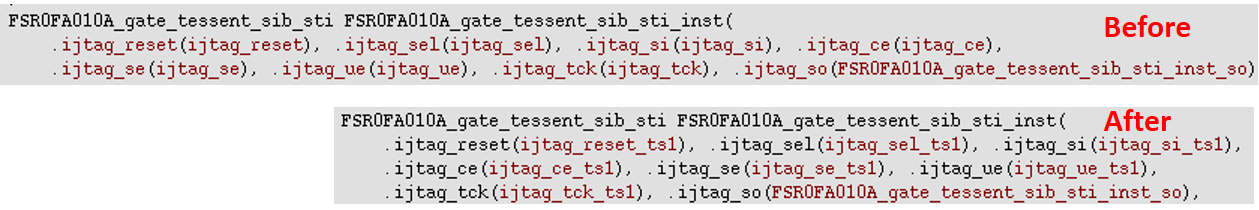
## FSR0FA010A\_ts\_post.cmd

|  |  |
| --- | --- |
| **INPUT** | |
| <Project>.vg | Netlist after insert MBIST |
| <Project>\_ts\_post.cmd | Do file |
| **Execute command:** tessent -shell -dofile FSR0FA010A\_ts\_post.cmd -logfile FSR0FA010A\_ts\_post.log -replace | |
| **OUTPUT** | |
| <Project>.tstmb | Output netlist for this step |
| <Project>\_ts\_post.log | Contain while running this step will be saved in this file |

About this step, do file will modify ijtag signal inside the design.



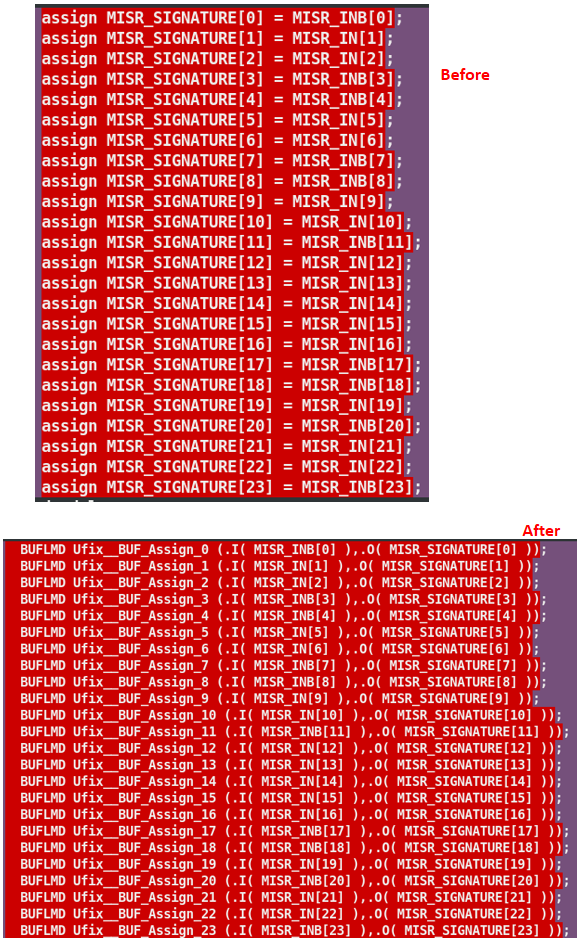


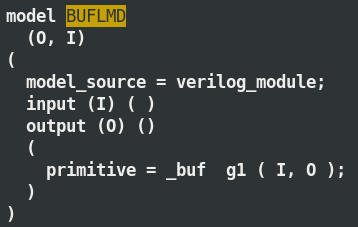


## Fix\_assign

|  |  |
| --- | --- |
| **INPUT** | |
| <Project>.tstmb | Netlist after modify ijtag |
| Fix\_Assign.pl | Do file |
| **Execute command:** Fix\_Assign.pl FSR0FA010A.v.tstmb FSR0FA010A.v.fixass | |
| **OUTPUT** | |
| <Project>.v.fixass | Output netlist for this step |
| <Project>\_ts\_post.log | Contain while running this step will be saved in this file |

About this step, .pl file will modify some assign syntax to define module.

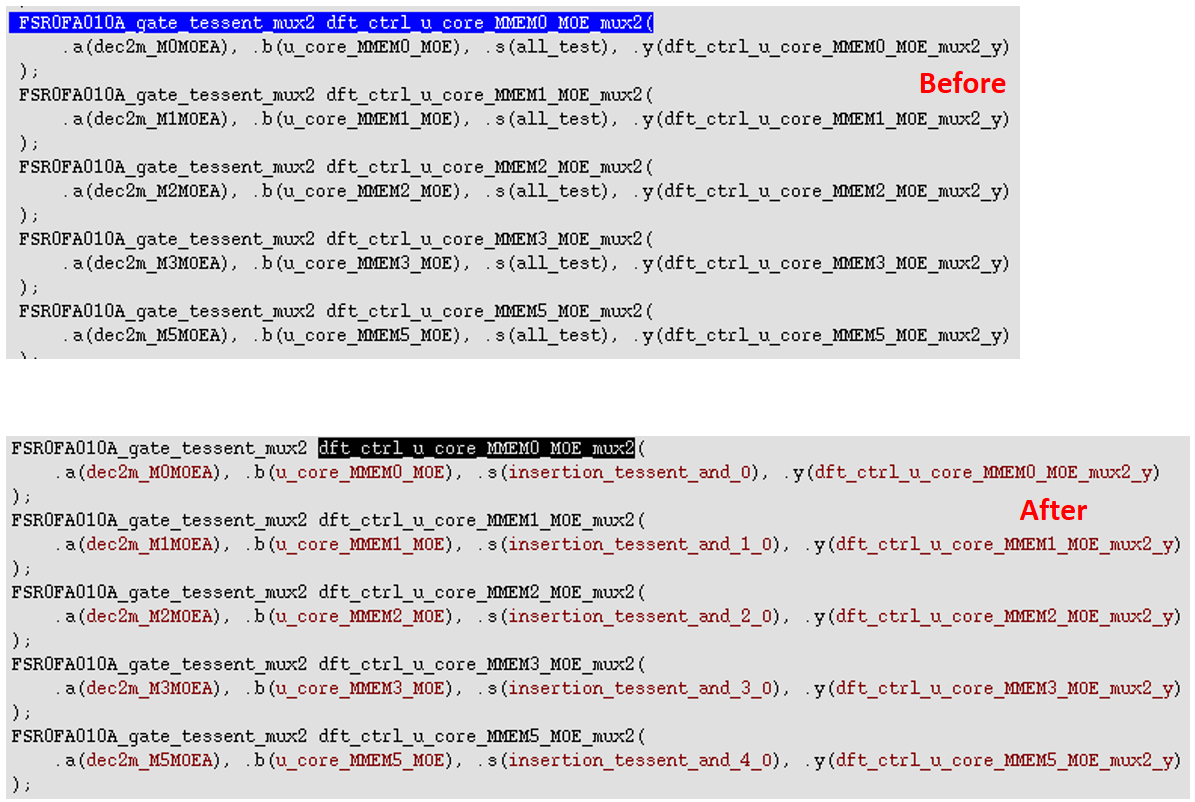


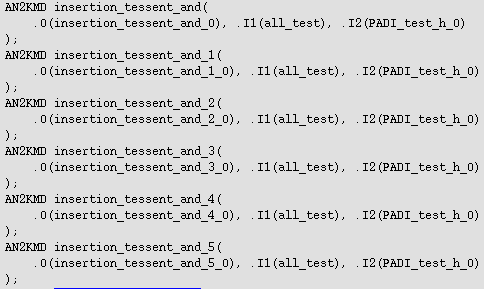


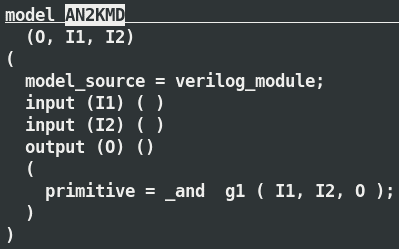
This “BUFLMD” module is defined in libcomp.atpglib which have function like a buffer.

## Eco.cmd

|  |  |
| --- | --- |
| **INPUT** | |
| <Project>.v.fixass | Netlist after modify syntax |
| <Project>\_eco.cmd | Do file |
| **Execute command:** tessent -shell -dofile FSR0FA010A\_eco.cmd -logfile FSR0FA010A\_eco.log –replace | |
| **OUTPUT** | |
| <Project>.v.eco | Output netlist for this step |
| <Project>\_ts\_post.log | Contain while running this step will be saved in this file |







This “AN2KMD” module is defined in libcomp.atpglib which have function like a and.

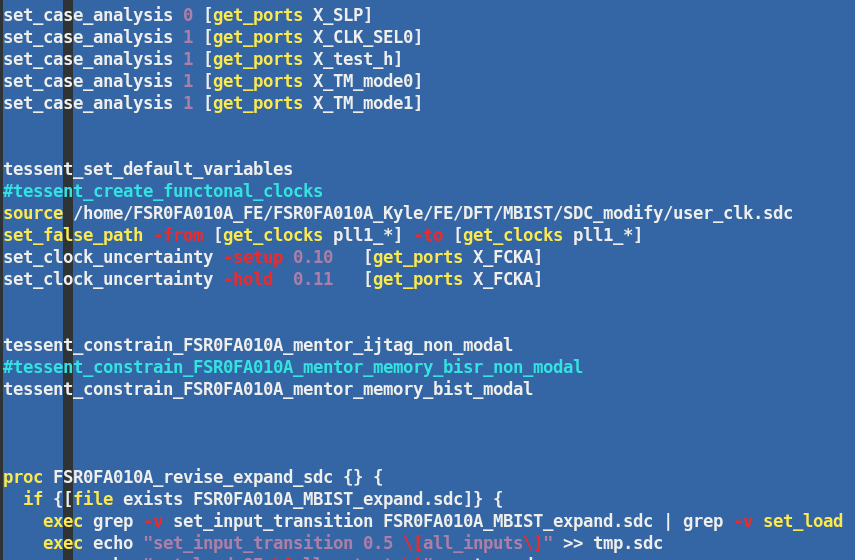
# Modify sdc

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/DFT/MBIST/SDC\_Modify

## FSR0FA010A\_MBIST.sdc

|  |  |
| --- | --- |
| **INPUT** | |
| FSR0FA010A.sdc | MBIST SDC, will be generated after insert MBIST |
| user\_clk.sdc | #Create |
| mbist\_sdc\_tail.sdc | #Created from datain sdc |
| **EXECUTE** | |
| modify\_sdc.csh | Do file |
| **Execute command:** ./modify\_sdc.csh | |
| **OUTPUT** | |
| FSR0FA010A\_MBIST.sdc | Output sdc |

## 



## FSR0FA010A\_MBIST\_EXPAND.sdc

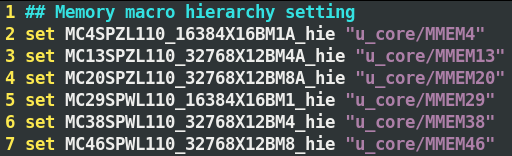
|  |  |
| --- | --- |
| **INPUT** | |
| FSR0FA010A\_MBIST.sdc | SDC is generated from previous step |
| library |  |
| setup.ftc.fsta | Setup file |
| **EXECUTE** | |
| FSR0FA010A\_run\_sta | Do file |
| **Execute command:** ./FSR0FA010A\_run\_sta | |
| **OUTPUT** | |
| FSR0FA010A\_MBIST\_expand.sdc | Output sdc |

## SDC\_ECO

|  |  |
| --- | --- |
| **INPUT** | |
| FSR0FA010A\_MBIST\_expand.sdc | SDC is generated from previous step |
| **EXECUTE** | |
| make\_size\_only.csh | Do file |
| **Execute command:** ./make\_size\_only.csh | |
| **OUTPUT** | |
| DFT\_size\_only.sdc | Output sdc |

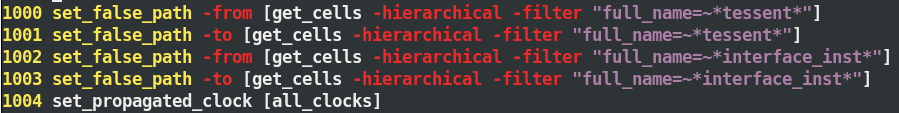
### DFT\_size\_only.sdc

Add list of memory doesn’t apply DFT in the design at the beginning of the file.



### DMA.sdc

Copy the input sdc and change name to DMA.sdc, add these script at the end of the file.



### FSR0FA010A\_MBIST\_expand.sdc

Add this command at the end of the file to define the propagated clock.



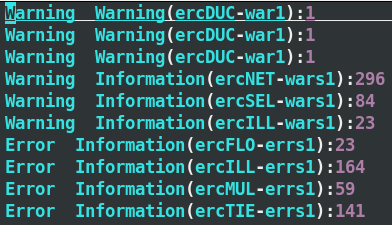
# RUN DESIGN TOOLKIT CHECK

**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/Pre\_Sim/PostDFT

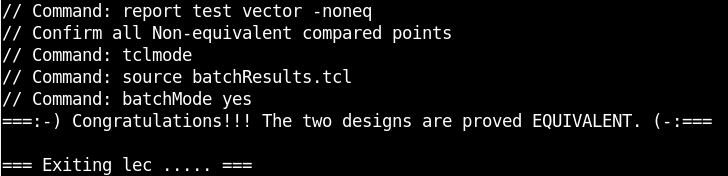
## FERC





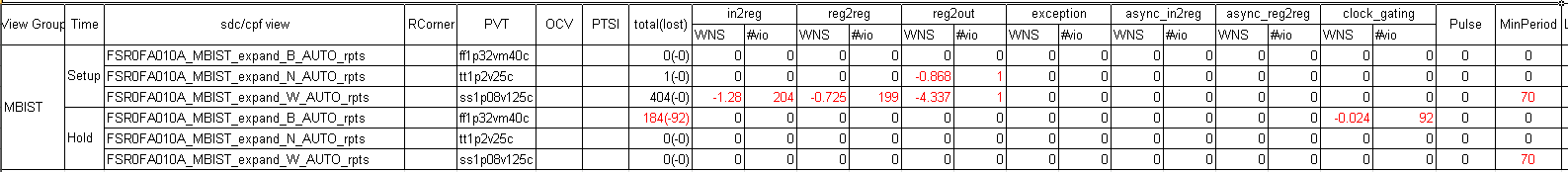


## FLEC



## FSTA

### FSR0FA010A\_MBIST\_expand.sdc



### DMA.sdc

