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| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Nguyen Anh Huy | No. | T062 | Div/Dept | DSD/ACD/ACT2 | Job  Date：2022/10/14  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 🗹W2 □W3 □W4 | | | | | |
| Third month | □W1 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. Test chip: Gen Pattern   + Task: Read slide, practice to generate file for fsim.  + Achievement: Know the flow how to generate pattern.   1. Test chip: Run fsim   + Task: Read slide, practice to run fsim  + Achievement: Know how to run and pass fsim. |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Issue: * How to solve: |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Run data check for FSR0FA010A |
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| Name  (Date) | Mentor | Direct Supervisor |
| Huy Nguyen (2022/10/14) | (Signature/Date) | (Signature/Date) |

【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. What is behavior level ?

This level will use Algorithm to describle the function of the design

1. What is Signal Intergrity ?

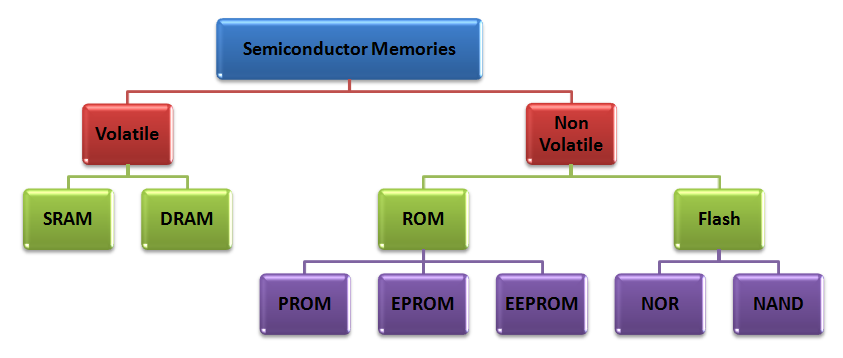
Signal Integrity is to ensure reliable, high-speed data transmission from one point to another point inside the chip through the metal lines.

* **Crosstalk (Delay and Noise )**
* Ground bounce
* IR Drop
* Antenna effect
* Electromigration

1. What is “C1” in add\_pin\_constraint mean ?

It’s mean the logic of this pin is equal to 1.

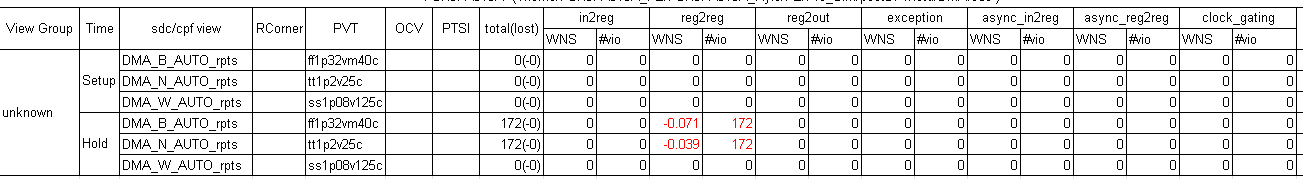
1. How many kind of memory ?



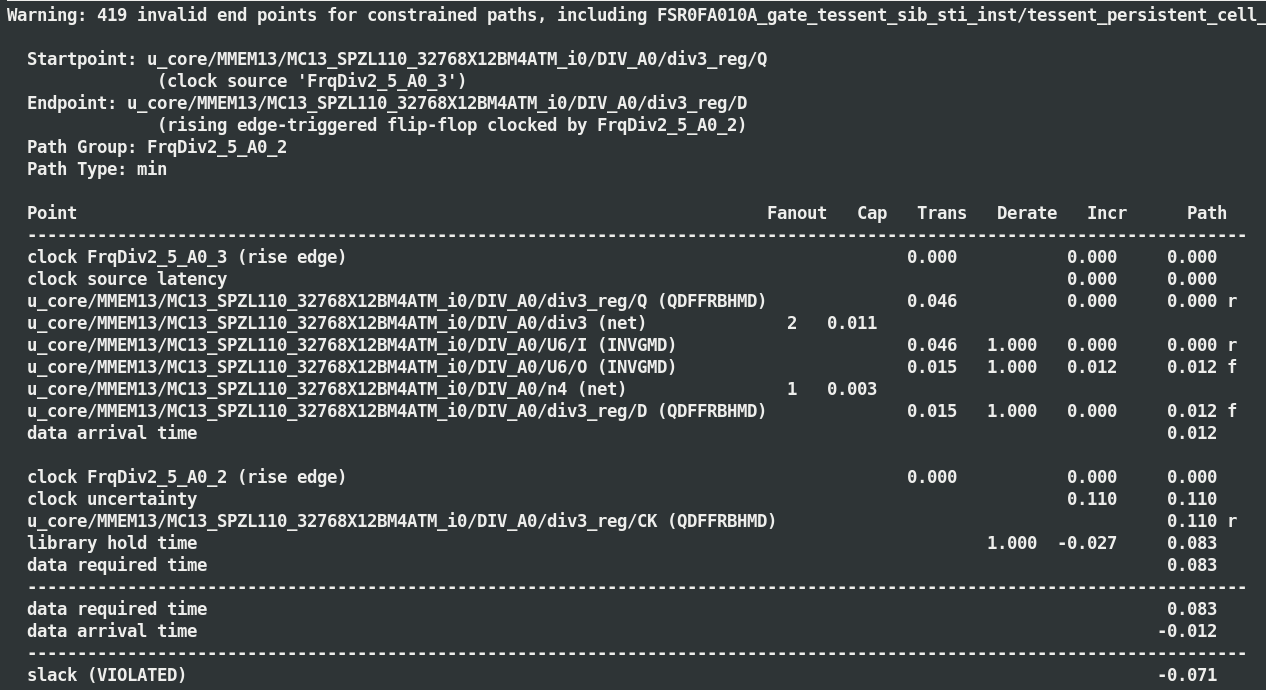
1. What does “AUTO” in “FSR0FA010A\_MBIST\_expand\_W\_AUTO\_rpts” directory mean  ?

Because we run this at pre STA, which mean it doesn’t have.spef file (contain delay information of cell). So the tool will use “Wire load model” to estimate delay, in other to run tool. So tool will generate a folder name AUTO in this folder.

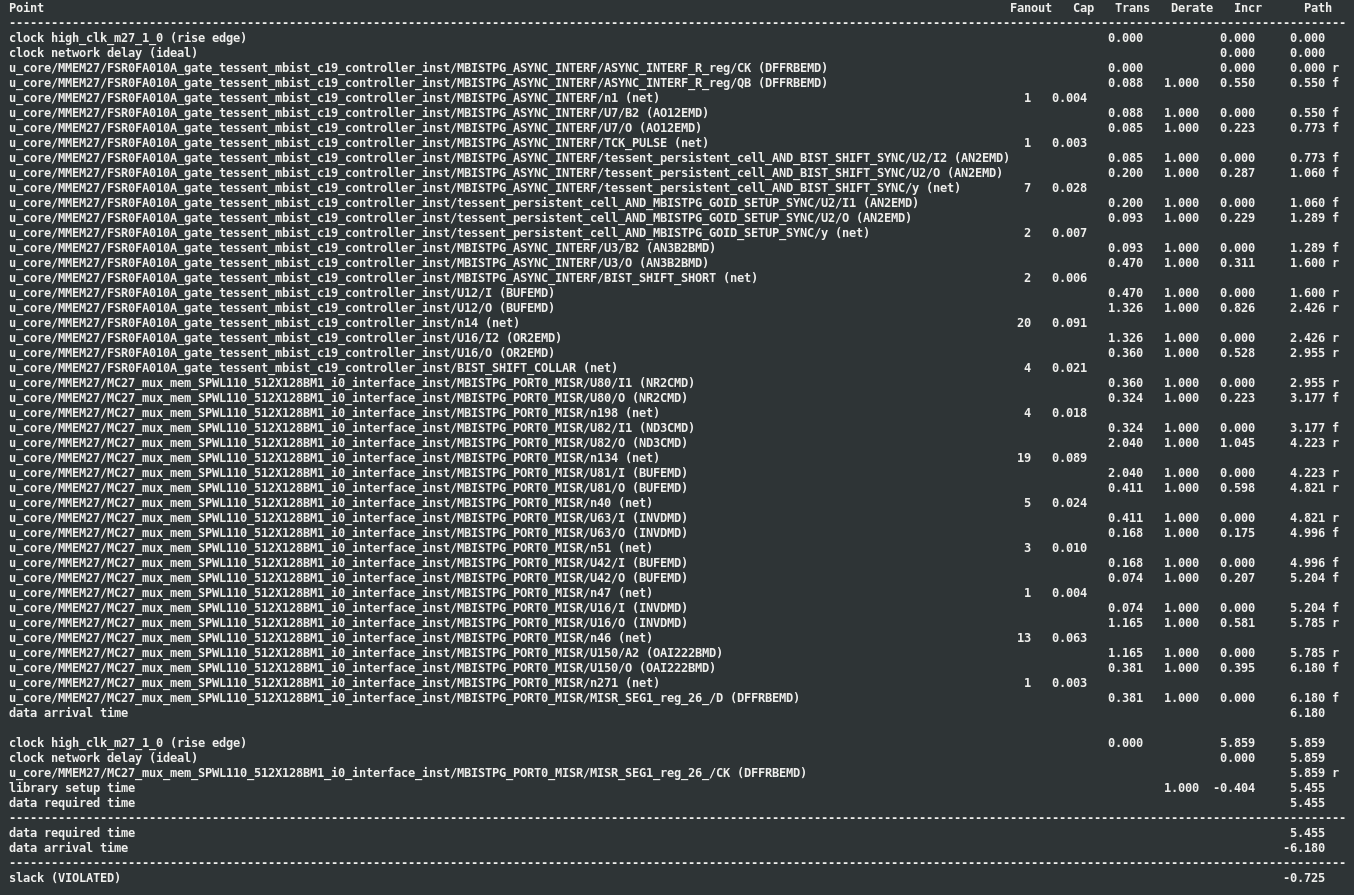
1. Where can we see detail report about violation in Constraint.xml ?



Go to folder have name “\*B\_AUTO\_rpts” -> show file name “HoldChk\_reg2reg.rpt”

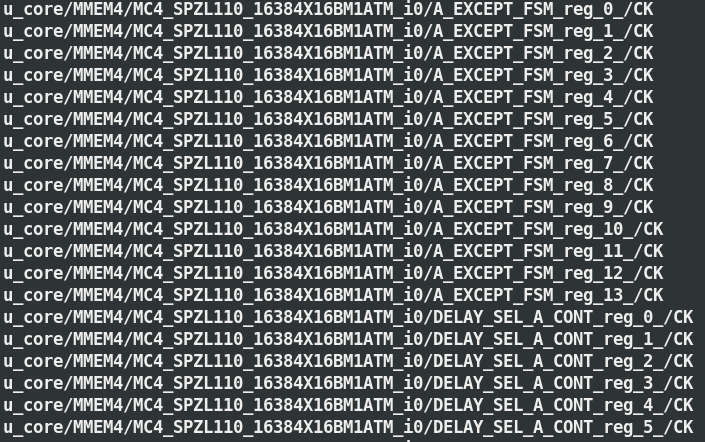


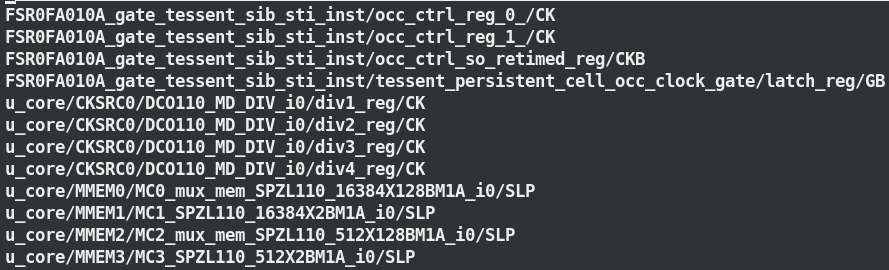
1. Analyze which reason make the first timing path in “SetupChk\_reg2reg.rpt” violated? How can we fix this violated ?



* Improve drivability of cell (increase cell size, reduce Vth).
* Reduce net length.
* Reduce redundant cell (like buffers/inverters).

1. Why there is 3928 warning in file “CheckTiming.rpt.gz” ?





# gen pattern

## Summarize data

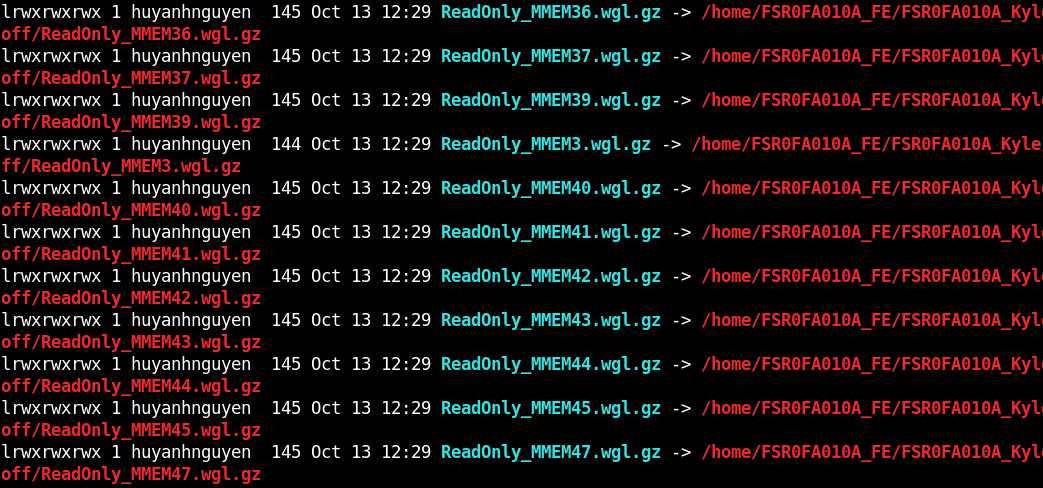
|  |  |
| --- | --- |
| **INPUT** | |
| ICL |  |
| PLL\_src |  |
| DCO\_config |  |
| **Execute command:** ./sum\_mem\_info\_new.pl -gen\_db | |
| **OUTPUT:** FSR0FA010A\_MBIST\_PAT\_config.csv | |
| **Execute command:** ./sum\_mem\_info\_new.pl -gen\_pt | |
| **OUTPUT:** FSR0FA010A\_pt | |

## geN PATTERN

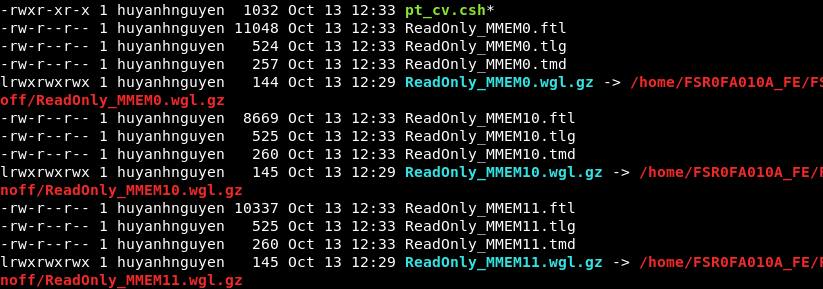
|  |  |
| --- | --- |
| **INPUT** | |
| mbist\_gen\_pattern.dof |  |
| run\_gen\_pattern | Do file |
| **Execute command:** ./run\_gen\_pattern | |
| **OUTPUT** | |
| PAT\_GEN\_tsdb\_outdir.bak/patterns/<PROJECT>\_gate.patterns\_signoff/\*wgl | |

## Gen FTL file

**Working Path:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/Ftl\_Gen/wgl\_pt



|  |  |
| --- | --- |
| **INPUT** | |
| setup.ftc |  |
| pt\_cv.csh | Do file |
| **Execute command:** ./pt\_cv.csh | |
| **OUTPUT** | |
| <Pattern\_Path>.ftl |  |
| <Pattern\_Path>.flg |  |
| <Pattern\_Path>.tmd |  |



## resequence pattern

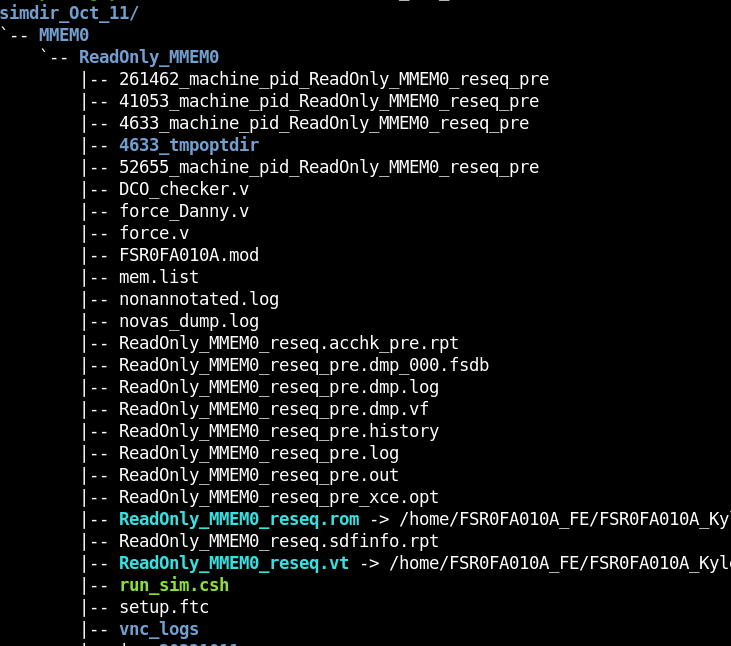
**Working directory:** /home/FSR0FA010A\_FE/FSR0FA010A\_Kyle/FE/Ftl\_Gen/postDFT

|  |  |
| --- | --- |
| **INPUT** | |
| setup.ftc |  |
| pt\_cv.csh | Do file |
| **Execute command:** ./pt\_cv.csh | |
| **OUTPUT** | |
| <Project>.pad |  |
| <Project>.th |  |

|  |  |
| --- | --- |
| **INPUT** | |
| gen\_vt\_file.csh | Do file |
| DCO\_config |  |
| MBIST\_PAT\_config.csv |  |
| pt.list |  |
| 00\_reseq\_mbist\_at\_speed\_sample.cmd\_bak |  |
| PLL\_control\_file\_sample.cmd |  |
| <Project>.pad |  |
| <Project>.th |  |
| **Execute command:** ./gen\_vt\_file.csh | |
| **OUTPUT** | |
| <Pattern\_Path>.rom |  |
| <Pattern\_Path>.vt |  |

# run fsim

|  |  |
| --- | --- |
| **INPUT** | |
| gen\_pre\_sim\_with\_period.csh | Do file |
| pt\_list |  |
| template\_ReadOnly |  |
| **Execute command:** ./gen\_pre\_sim\_with\_period.csh | |
| **OUTPUT** | |
| simdir\_<Ver> |  |



|  |  |
| --- | --- |
| **INPUT** | |
| gen\_sim\_dir.csh | Do file |
| simdir\_<Ver> |  |
| **Execute command:** ./gen\_sim\_dir.csh | |
| **OUTPUT** | |
| <Pattern\_path>.out |  |



