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| Name | Nguyen Anh Huy | No. | T062 | Div/Dept | DSD/ACD/ACT2 | Job  Date：2022/10/21  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 🗹W3 □W4 | | | | | |
| Third month | □W1 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

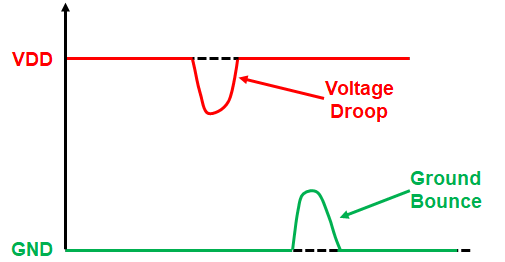
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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. Test chip: Run fsim   + Task: Read slide, practice to generate file for fsim.  + Achievement: Know how to run and pass fsim.   1. Test chip: Post data check (ferc, flec, fsta)   + Task: Read slide, practice to run ferc, flec, fsta  + Achievement: Know how to run, analyze log and report. |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Issue: * How to solve: |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Rerun pre simulation for FSR0FA010A * Run post simulation for FSR0FA010A |
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| Name  (Date) | Mentor | Direct Supervisor |
| Huy Nguyen (2022/10/21) | (Signature/Date) | (Signature/Date) |

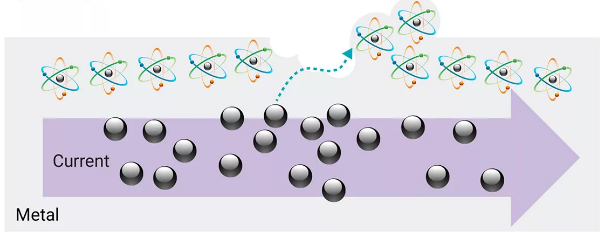
【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. Explain Ground bounce, IR drop, Antenna effect and Electromigration.

* Ground bounce: is a phenomenon associated with [transistor](https://en.wikipedia.org/wiki/Transistor) switching where the [Vth](https://en.wikipedia.org/wiki/Gate_voltage) can appear to be less than the local [ground potential](https://en.wikipedia.org/wiki/Ground_potential).
* IR drop: As current flows through a resistor, the voltage drops – this is what is referred to as IR drop. When the voltage at a transistor drops, it becomes slower and this could impact the circuit timing.



* Antenna effect: During the fabrication of MOS integrated circuits, especially at the time of plasma etching, there will be a chance of collecting more charges at the gate and causes damage to the gate oxide layer since it is very thin.
* Electromigration: is the movement of atoms based on the flow of current through a material. If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them. This displaced from their original position and might creating open or short with other signal.

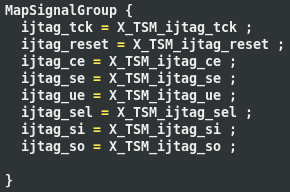


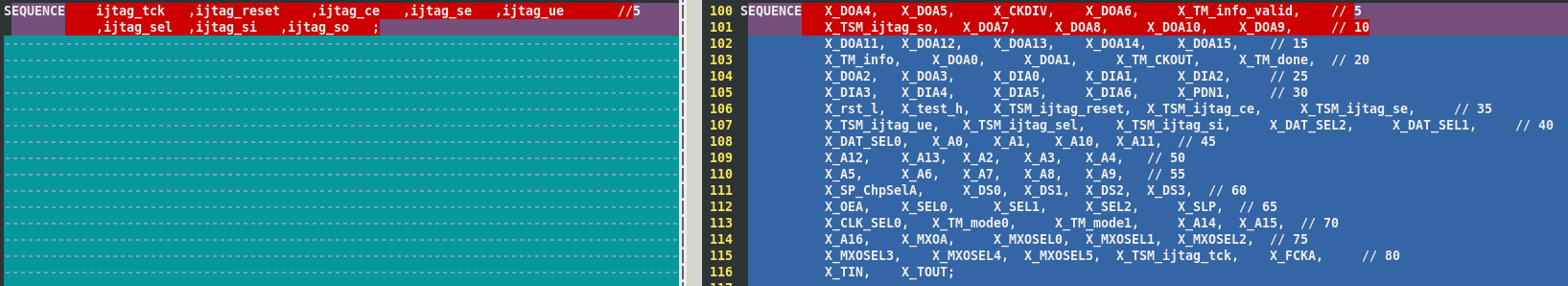
1. How to fix setup timing ?

* Reduce the clock delay launch flop: using a flop with a smaller clock delay for launch flip-flop will ease timing requirement.
* Decrease the logic delay by improve drivability of cell (increase cell size, reduce Vth).
* Increasing the clock latency on capture flop
* Increasing the clock period

1. What is resequence pattern ?

It will connect port from top module to pin of instances.





1. Why STA show “no clock” error about DCO clock after MBIST insertion ?

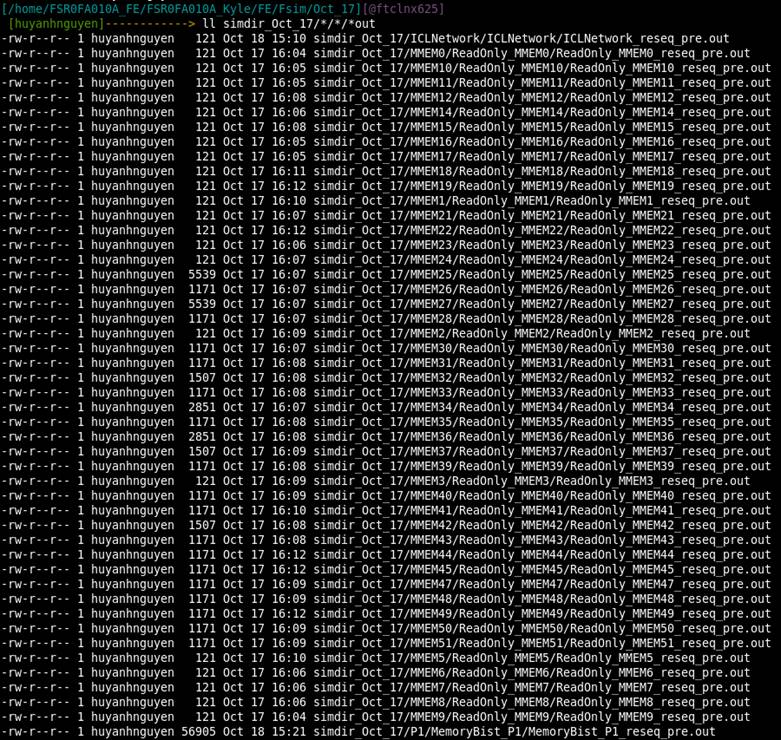
Because fstaH tool ensures that the design is fully constrained, unconstrained paths will lose the timing reports. So tool will include “Missing clocks reaching one register pin” in the report file. But in SDC file, ot don’t define clock for memory which doesn’t apply DFT circuit. So fstaH tool will list missing clock for those memory.



1. Why we have to force clock while running fsim although we have config DCO clock ?

Because clock data while we working with DCO clock isn’t generated as well as PLL clock , so we force memory to run at specific frequency in other check the optimize frequency for each memory, and to test that memory can pass or not.

# Run fsim



After force clock to memory, only memory from MMEM0->MMEM24 pass the fsim. All other memory have failed the fsim. After analyze the error in log file, I found that this error come from missing romcode file from directory “/home/aicestar2/users/peacatxu/FSR0W\_L\_SP/FSR0W\_L\_SP\_V0\_1\_0/working/testchip”.

After I modify the single directory to existence romcode directory for MMEM25, fsim for MMEM25 have passed.cid:image004.png@01D8E475.A5991810

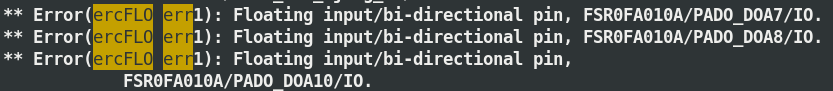
I will modify all other directory for all other and run fsim again to rerun the test.

# post data check

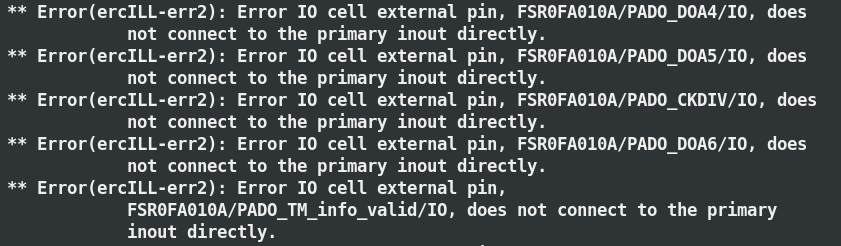
## Ferc

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| **Pre-layout** | **Post-layout** |
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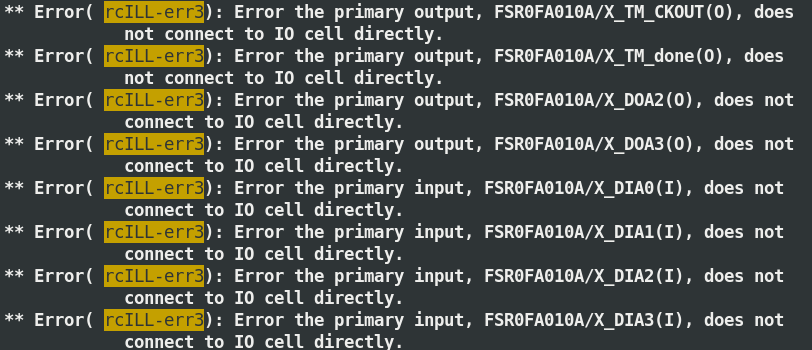
* ercENV-13: Some libraries are not compatible.
* ercFLO-err1: Floating floating input/ bi-directional pin. (Ouput at top module connect directly to inout pin => floating input at pin of PAD Cell, can pass this because it belong to PAD Cell)



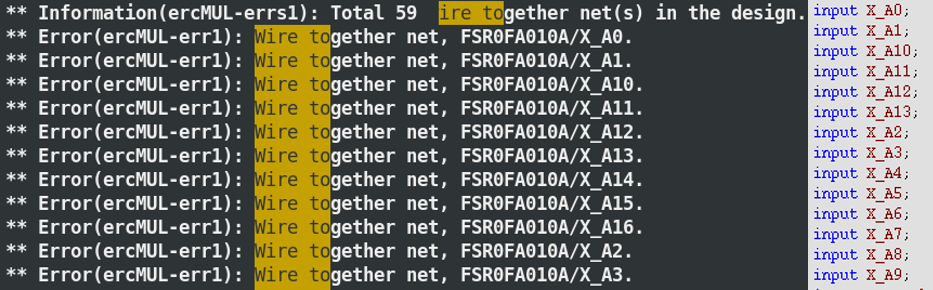
* ercILL-err2: Doesn’t connect directly to the primary inout directly (Because inout pin of PAD Cell doesn’t connect to inout port, just connect to input or output of top module).

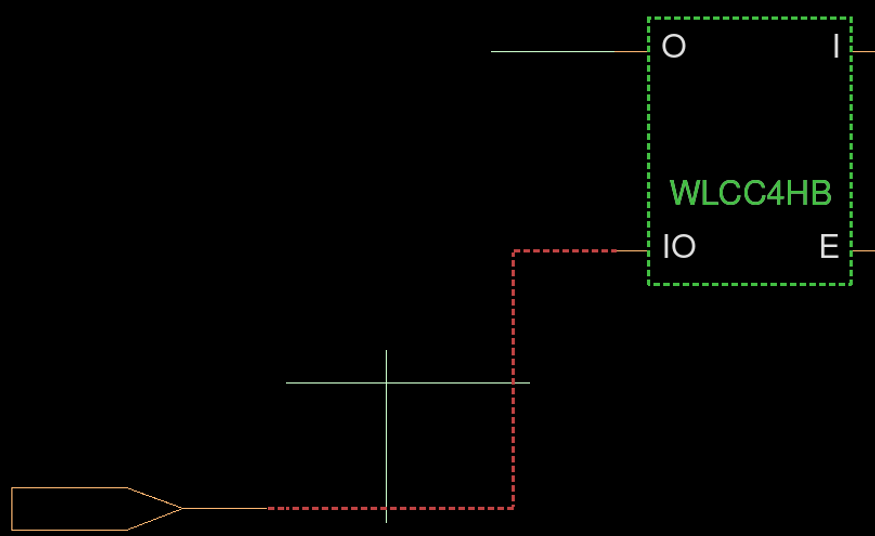


* ercILL-err3: Primary input/output doesn’t connect to IO cell directly. (Because input or output port connect to inout pin of PAD Cell, which have both input or output port).

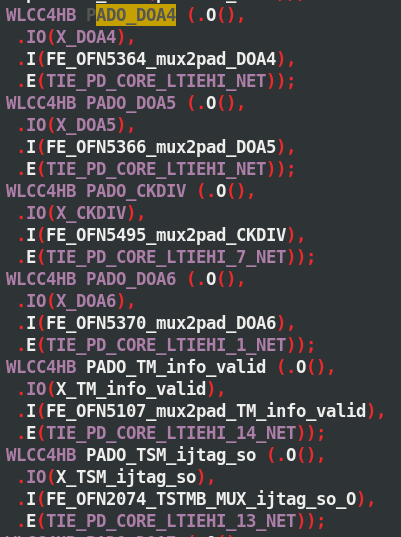


* ercMUL-err1: Wire together net (Input at top module connect to pin which have input and output, which is violated net wiring rule)

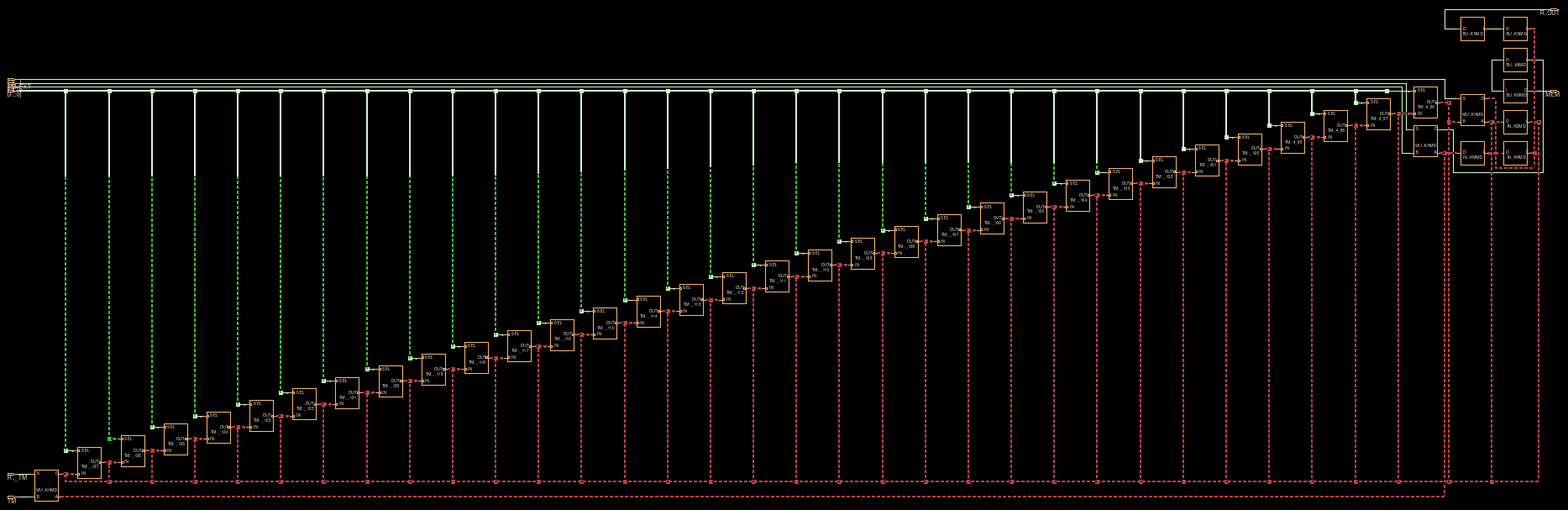




* ercTIE-err1: Pin isn’t connecting to a Tie1 cell.
* ercTIE-err3: Pin isn’t connecting to a Tie0 cell.
* ercDUC-war1: Don’t use cell is used in the design
* ercILL-war1: Floating connection on output pin (Output pin of PAD Cell doesn’t connect to anything)

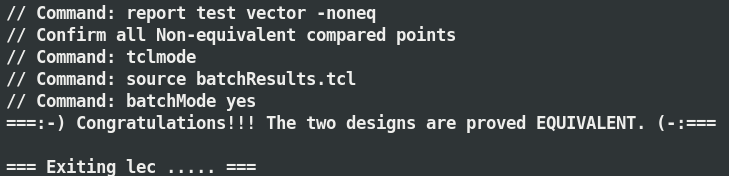


* ercNET-war1: Large fanout wire.
* ercSEL-war1: Combinational loop.



## Flec





## fsta



Will use .spef file for input



Don’t use the zero-wire-load model to estimate the timing performance.

