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| Name | Nguyen Anh Huy | No. | T062 | Div/Dept | DSD/ACD/ACT2 | Job  Date：2022/10/28  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 🗹W4 | | | | | |
| Third month | □W1 | | | | | |

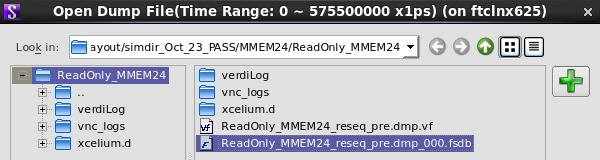
1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

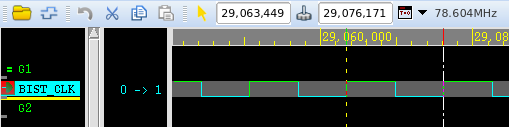
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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2022, below are a brief description of the tasks and what I learned:   1. Test chip: Run pre simulation  * Task: Read slide, practice to run and pass pre simulation. * Achievement: Know how to run and pass pre simulation.  1. Test chip: Run post simulation  * Task: Read slide, practice to run and pass post simulation. * Achievement: Know how to run and pass post simulation. |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Issue: * How to solve: |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Make a final term power point report |
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| Name  (Date) | Mentor | Direct Supervisor |
| Huy Nguyen (2022/10/28) | (Signature/Date) | (Signature/Date) |

【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.
3. What is DCO and PLL ?
4. Does PLL need to force frequency ?
5. If script doesn’t generate .pre.freq file, how can check which frequency does the memory run? Check the frequency of memory run using waveform.

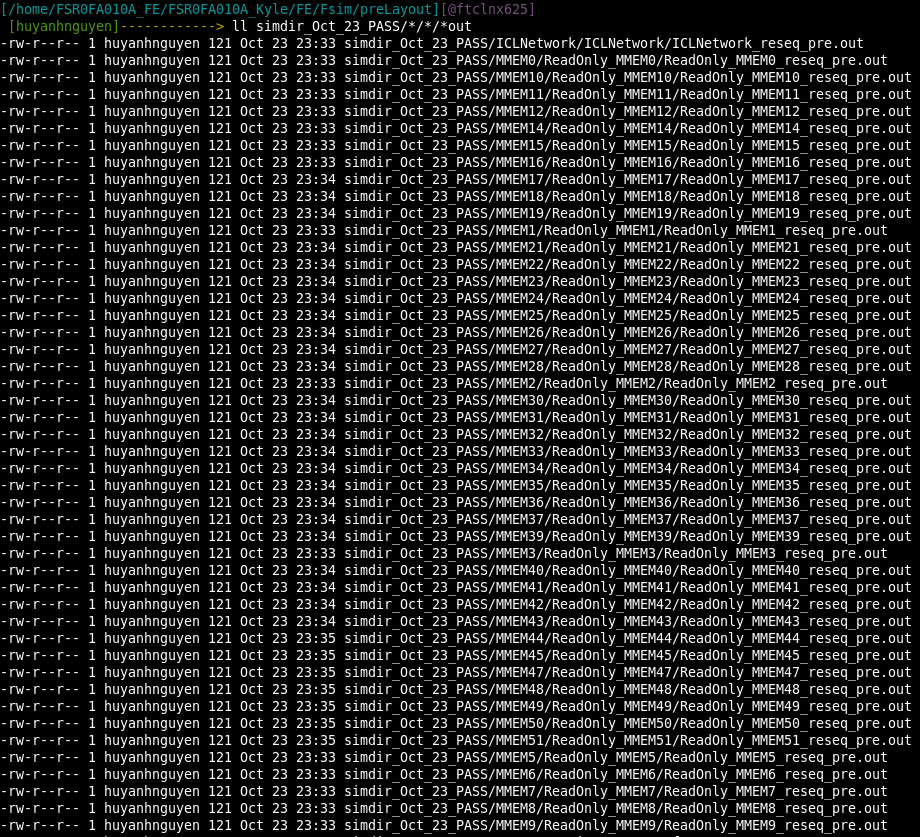






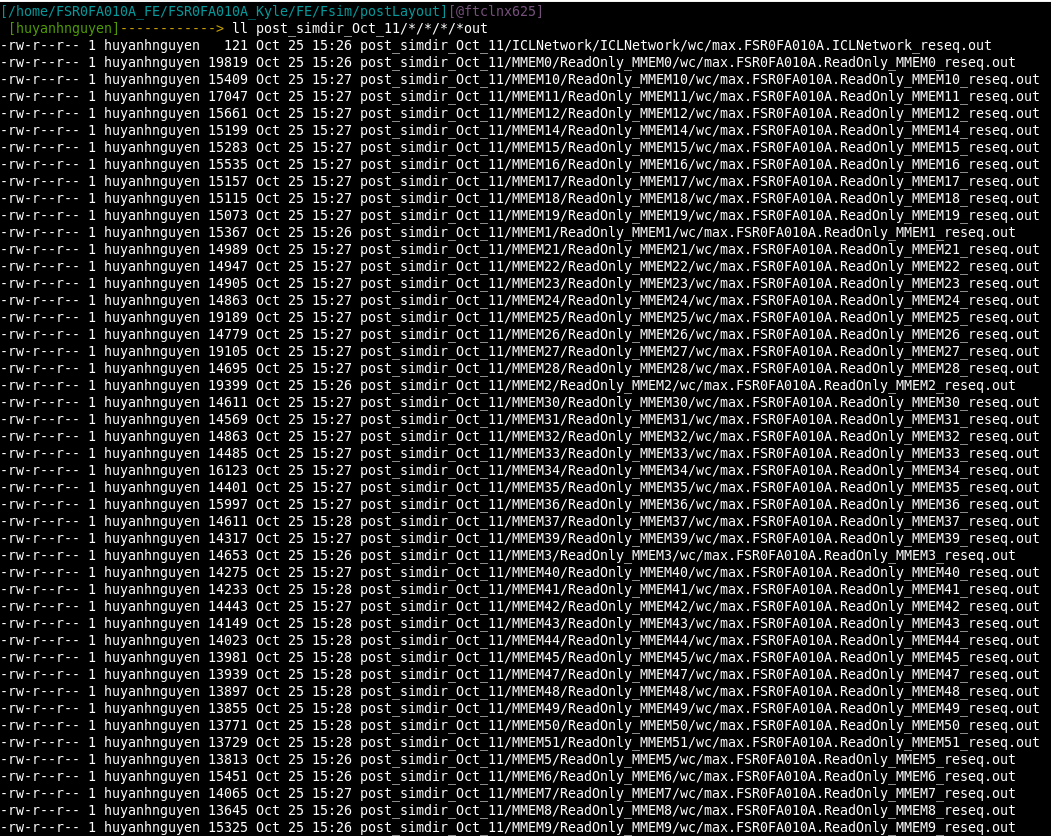
1. What is PAD Cell and IO PAD ?

# Pre simulation

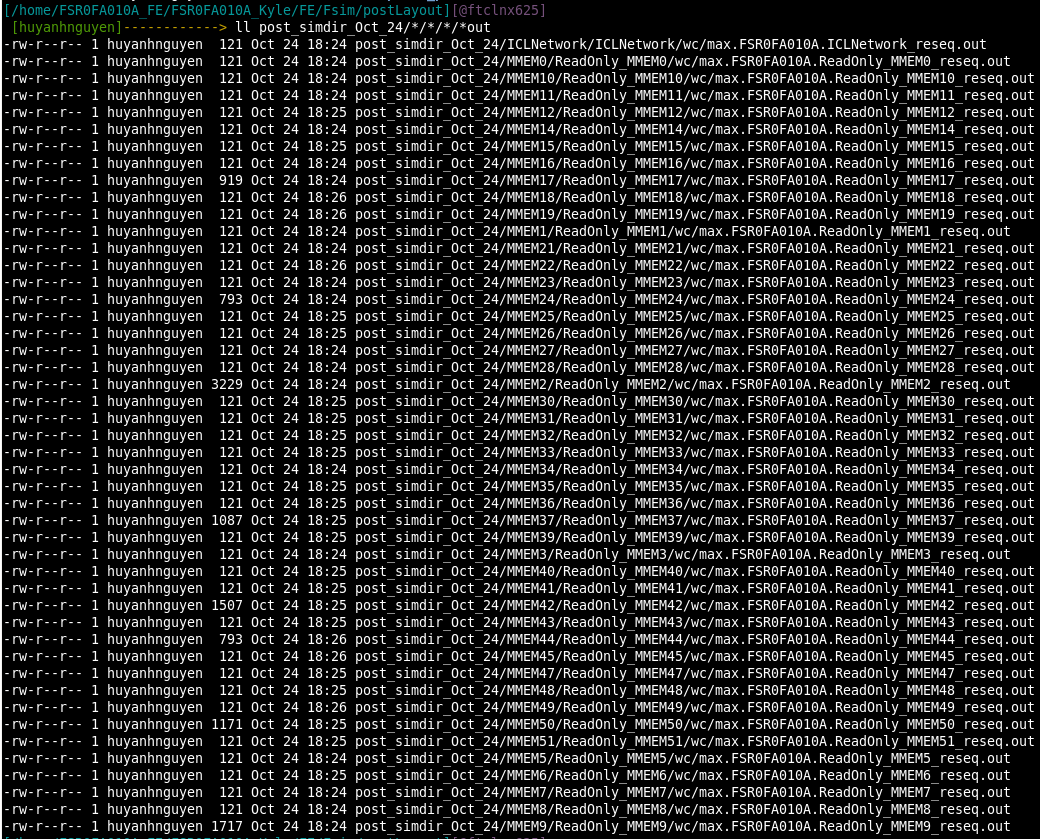


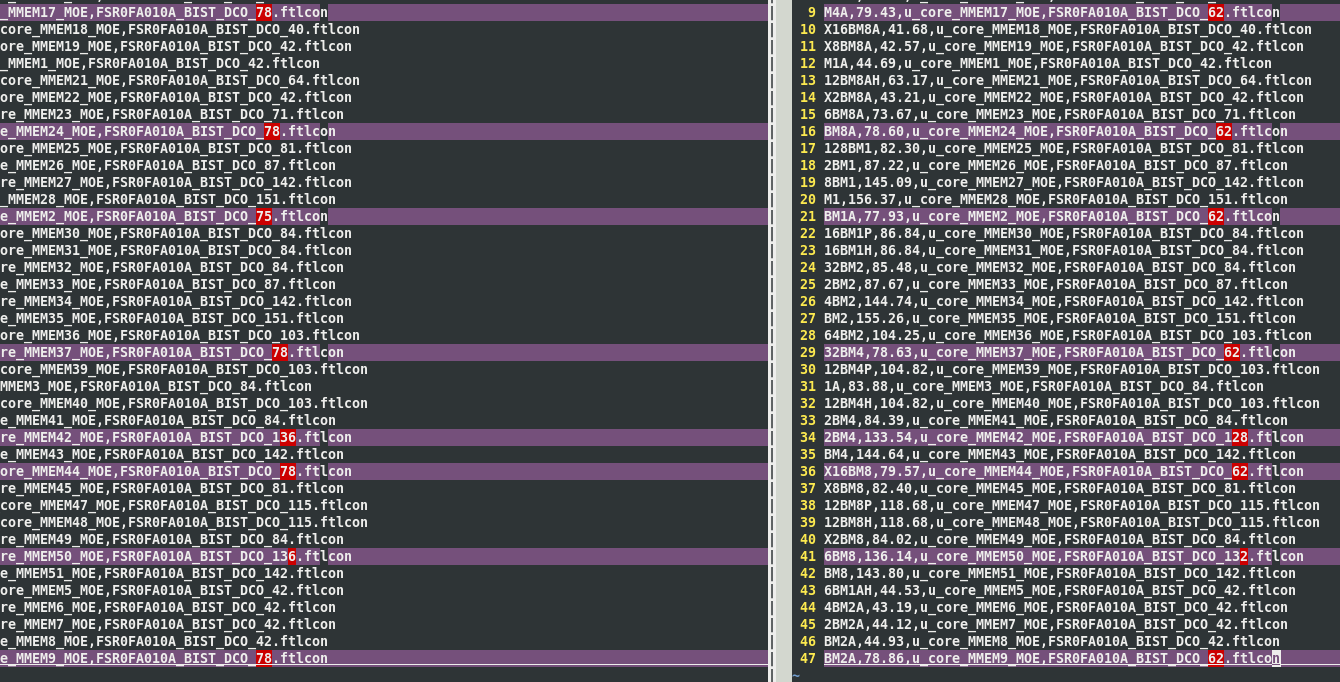
After modify the directory of mem.list file, I rerun pre simulation again and

# post simulation



First time running post simulation, there isn’t memory pass. So I check the pattern again and found that the pattern wasn’t generated correctly. After a few checking step and generate the pattern again, the result is better than before but it still fail at some memory.





After changing the .ftlcon file of each failed memory, I rerun the fsim and all the memory pass this time.

