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| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Tran Duy Minh | No. | T154 | Div/Dept | DSD/ACD/ACT | Job  Date：2024/06/03  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 🗹W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2023, below are a brief description of the tasks and what I learned:   * Practicing Test Chip Flow |
| 2. What are the problems encountered this week? Any actions taken? Any help needed? |
| 3. What are the tasks for next week? Any preparation needed in advance? |
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| Name  (Date) | Mentor | Direct Supervisor |
| Tran Duy Minh (2024/05/28) | (Signature/Date) | (Signature/Date) |

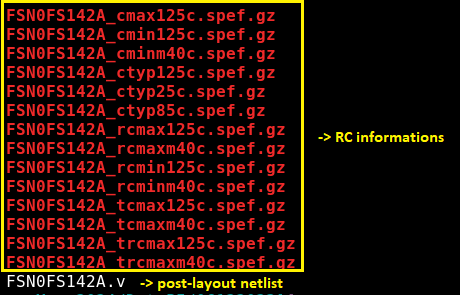
## Action Items

## TESTCHIP FLOW

**II/ POST-LAYOUT**

**1/ DATA-IN CHECK**

- Data directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/DataPI/06122023

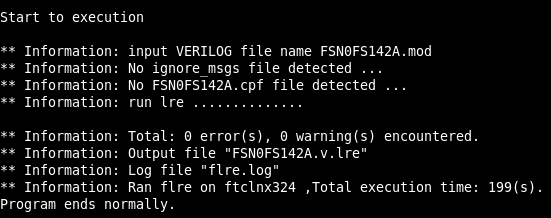


***a. flre***

- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Post\_Sim/TDI\_28\_05/ferc\_flre

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| --- | --- |
| **Input files** | |
| Netlist | Setup |
| FSN0FS142A.v (post-layout)  TMU1\_GCLD.v  TMU2\_GCLD.v | setup.ftc |

**Result:**

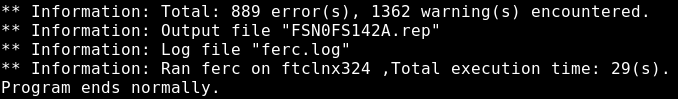


**b. ferc**

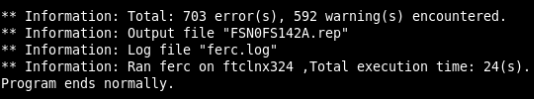
- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Post\_Sim/TDI\_28\_05/ferc\_flre

|  |  |
| --- | --- |
| **Input files** | |
| Netlist | Setup |
| FSN0FS142A.v (post-layout)  TMU1\_GCLD.v  TMU2\_GCLD.v | setup.ftc |

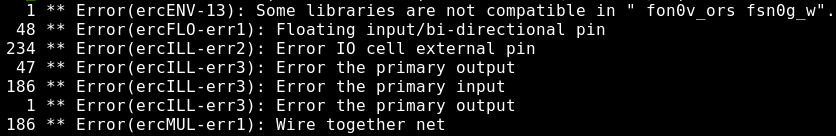
**Result:**

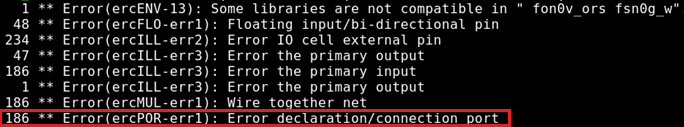
****

- Compare post-layout result to pre-layout (post-DFT) result:

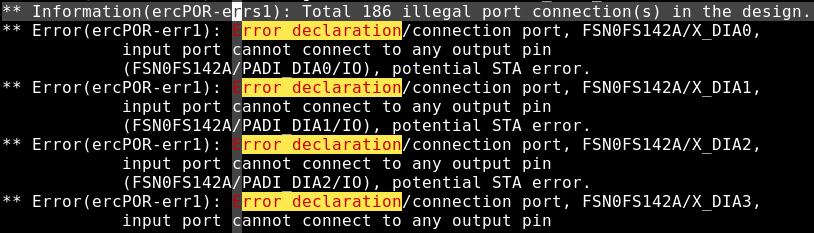
****

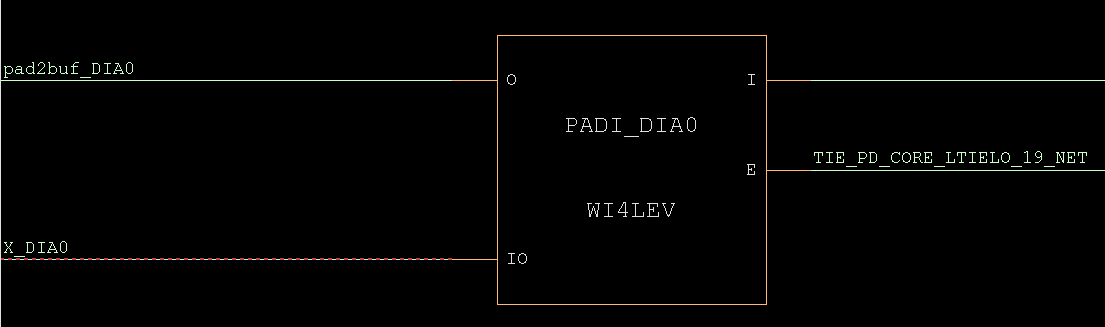
- Summary result:





There are new 186 errors occur in post-layout ferc. Details of the new errors:





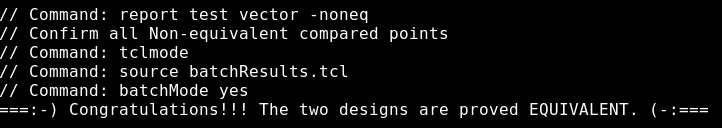
***c. flec***

- Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/FLEC/Post\_layout/TDI\_2805

|  |  |
| --- | --- |
| **FSN0FS142A.pre** | **FSN0FS142A.post** |
| FSN0FS142A.v (pure) | FSN0FS142A.v (post-layout) |
| TMU1\_GCLD.v  TMU2\_GCLD.v | |

**Result:**

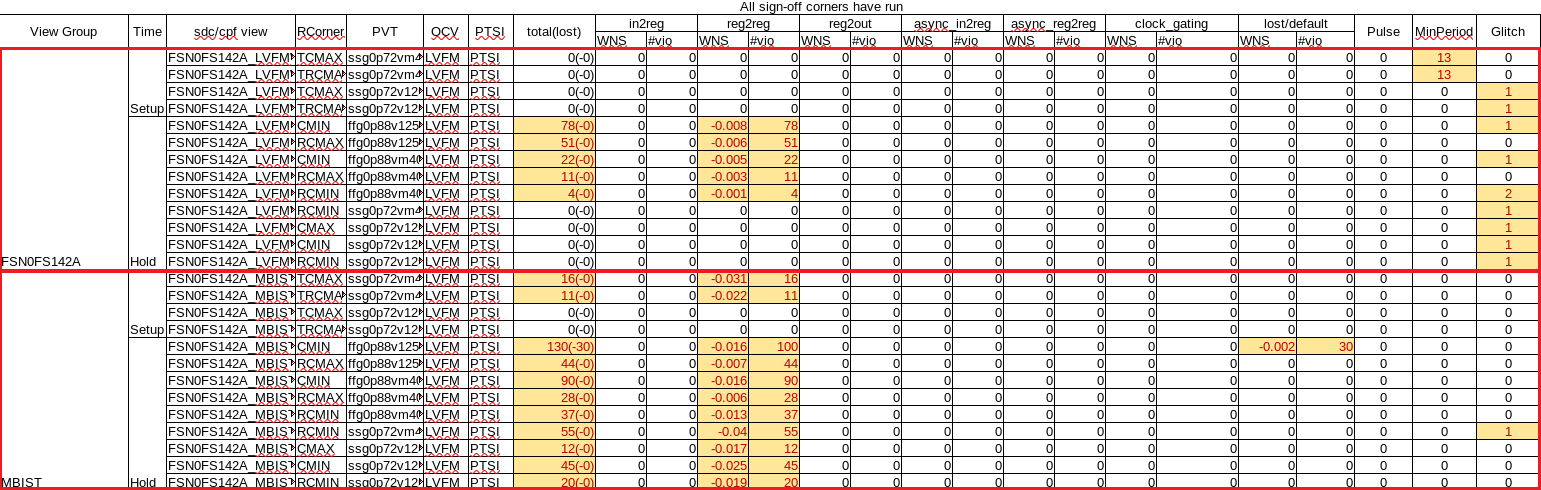


***d. fsta***

- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Fsta/Post\_STA/TDI\_2905

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| **Input Files** | | |
| Netlist | SDC | Setup |
| FSN0FS142A.v (post-layout)  TMU1\_GCLD.v  TMU2\_GCLD.v | FSN0FS142A\_MBIST\_expand.sdc  FSN0FS142A.sdc | setup.ftc.sta |

**Result:**



All timing violations are lesser than uncertainty value in SDC file (setup: 0.05ns, hold: 0.07ns)



**2/ GEN SDF (Standard Delay Format)**

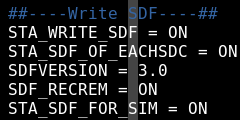
- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Fsta/Post\_STA/TDI\_2905

|  |  |  |  |  |
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| **Input Files** | | | | |
| Netlist | SDC | Setup | block1\_ann.tcl | .spef |
| FSN0FS142A.v (post-layout)  TMU1\_GCLD.v  TMU2\_GCLD.v | FSN0FS142A\_MBIST\_expand.sdc  FSN0FS142A.sdc | setup.ftc.sta |

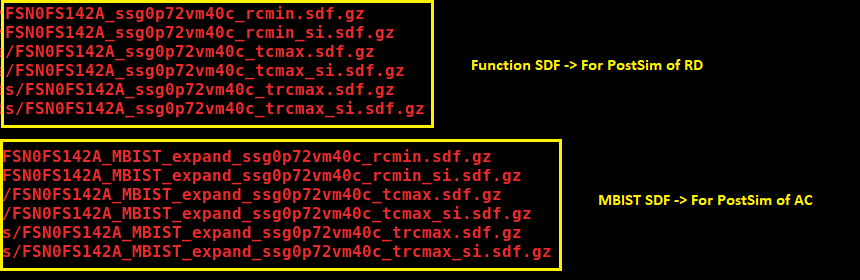
\*Note: “block1\_ann.tcl” is used to avoid SDF generation of ansyschronous circuit

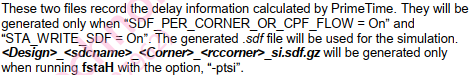
We need to run fsta to generate SDF

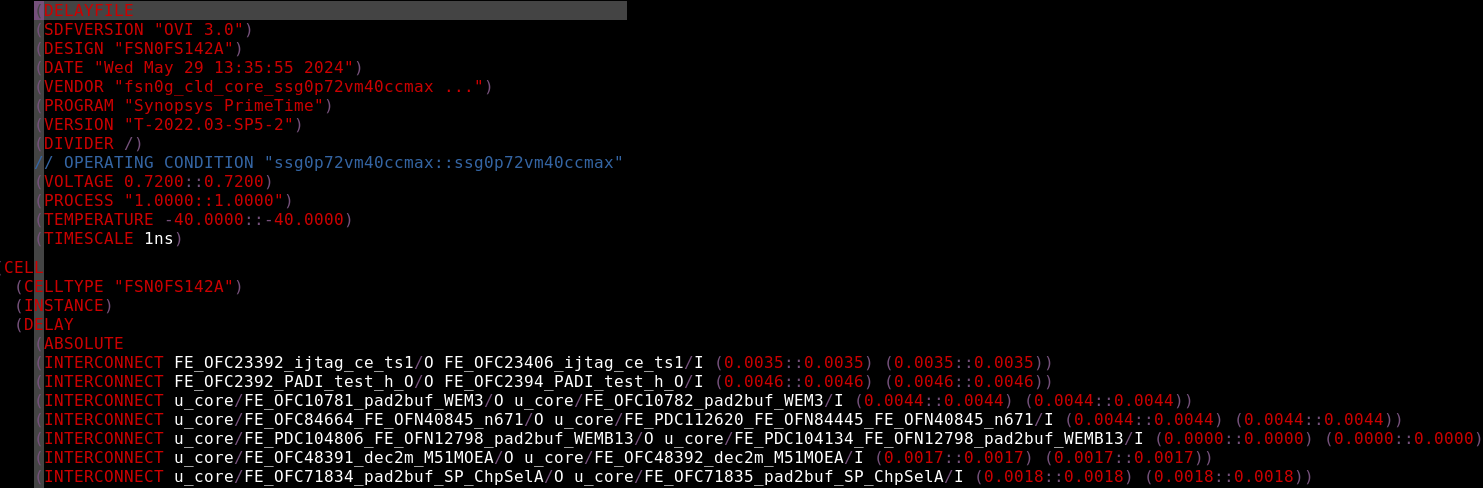
\*Note: Ensure “STA\_WRITE\_SDF” is “ON” and “SDF\_PER\_CORNER\_OR\_CPF\_FLOW” is “ON” (SPEF-in flow)



**Output:**





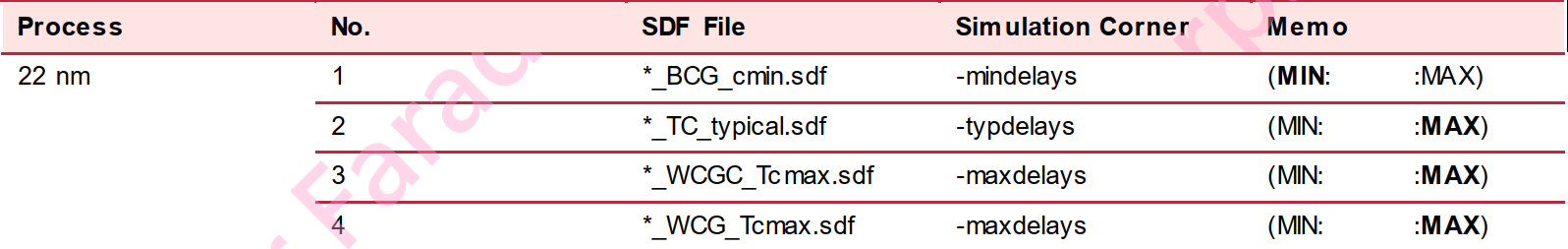


**3/ Run PostSim**

- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Fsim/Post\_sim

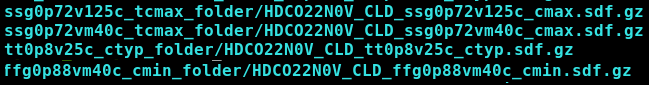
|  |  |  |  |  |  |  |
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| **Input Files** | | | | | | |
| Netlist | Setup | SDF | run\_sim.csh | pt.list | FSN0FS142A.sdfmod |
| FSN0FS142A.v (post-layout)  TMU1\_GCLD.v  TMU2\_GCLD.v  DCO\_checker.v  HDCO22N0V\_CLD.v  TK22/\*.v  fsn0g\_cld\_core.v  fon0v\_ors09\_io.v | setup.ftc | SDF\_folder (<MBIST>.sdf.gz)  DCO SDF |

- Prepare MBIST SDF file in SDF\_folder according to RD requirement on process of project

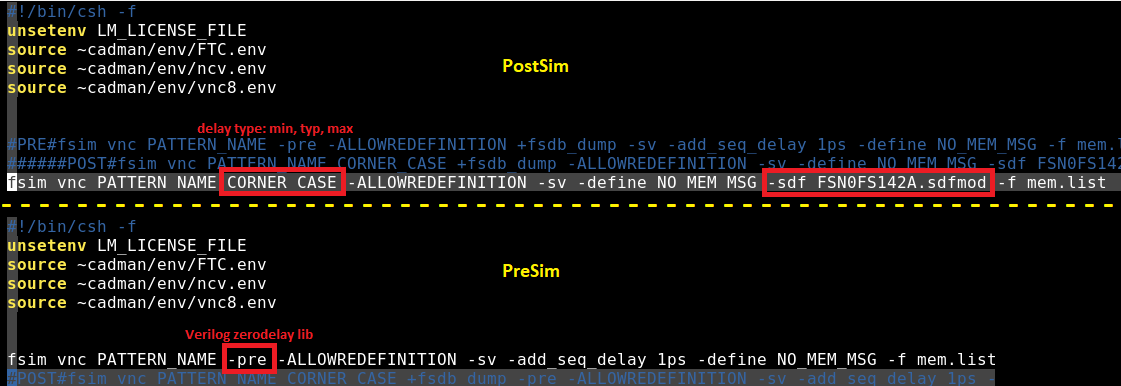




- Prepare DCO SDF provided by RD

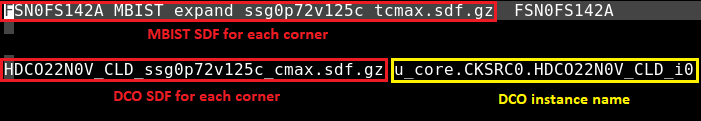


- Ensure run file for PostSim include –sdf option





- FSN0FS142A.sdfmod:



**Result:**



