|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Tran Duy Minh | No. | T154 | Div/Dept | DSD/ACD/ACT | Job  Date：2024/05/28  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | 🗹W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2023, below are a brief description of the tasks and what I learned:   * Practicing Test Chip Flow |
| 2. What are the problems encountered this week? Any actions taken? Any help needed? |
| 3. What are the tasks for next week? Any preparation needed in advance? |
|  |

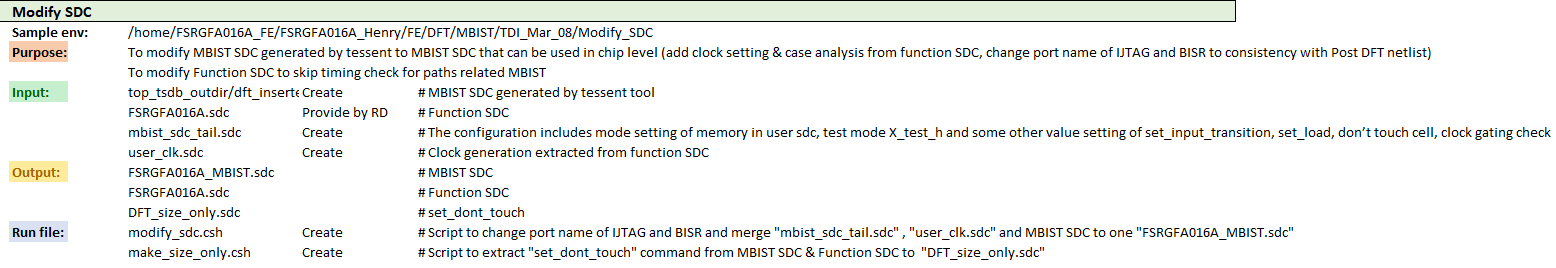
|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Tran Duy Minh (2024/05/28) | (Signature/Date) | (Signature/Date) |

## Action Items

## MBIST FLOW (continue)

**e. Modify SDC**

- Reference directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC

****

- Modify Tessent MBIST SDC to MBIST SDC can be used in chip level (clock setting, case analysis, change port name of UTAG & BISR to consistency with Post DFT netlist)

- Modify Function SDC -> skip timing check for paths related MBIST (set false path..)

- Working directory: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC

**Step 1: mbist\_tail.sdc**

* Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC

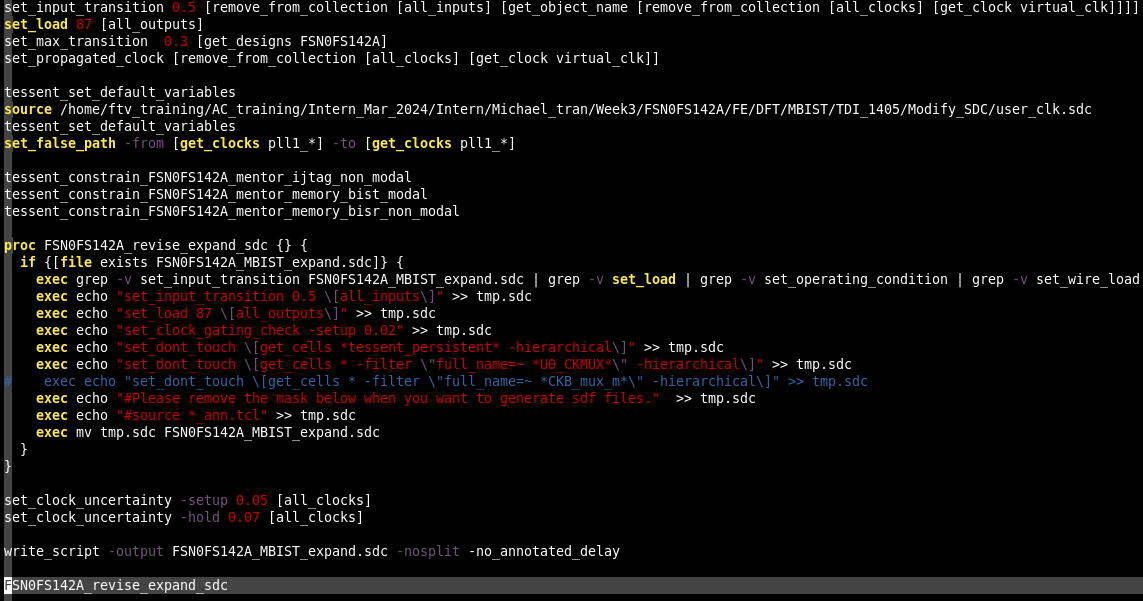
* Make mbist\_tail.sdc
* Copy from Function SDC and paste to mbist\_tail.sdc:

+ memory hierarchy setting

+ clock source hierarchy setting

+ set case analysis

+ Copy & update this setting:



**Revise Expand SDC**

**Update this path**

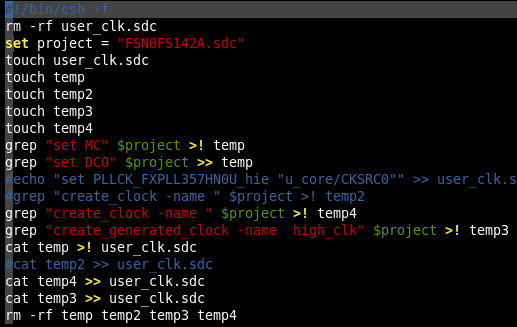
\*Note: Please ensure that these constrains are placed correctly same as position in this picture

**Step 2: user\_clk.sdc**

Make clock setting for all memories in MBIST mode

* Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC

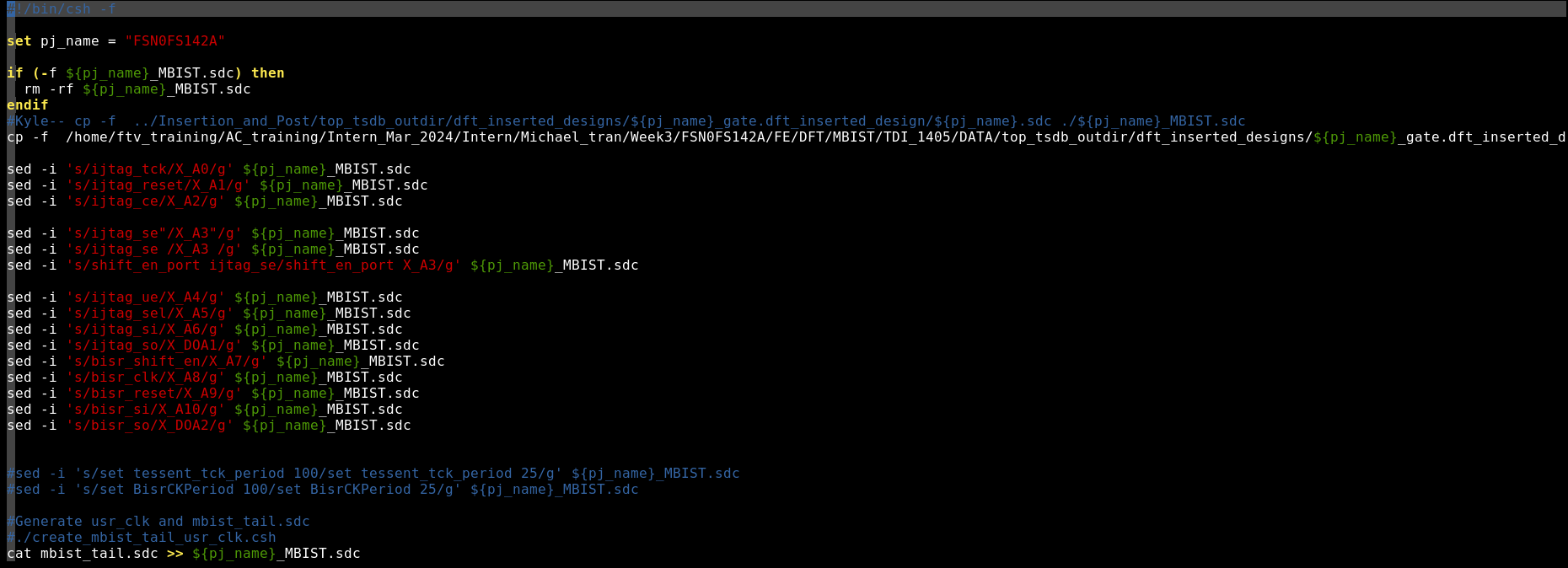
****

\*Note: Remember to remove create\_clock & create\_generated\_clock include “TM\_TREE”

**Step 3: FSN0FS142A\_MBIST.sdc**

To modify Tessent MBIST SDC to MBIST SDC that can be used in chip level

- Use modify\_sdc.csh to generate “FSN0FS142A\_MBIST.sdc”



**Change IJTAG port name to consist consistency with Post DFT netlist**

**Update this path**

**Step 4: MBIST\_expand.sdc**

Convert SDC (tessent format) to SDC format that can be read by both primetime & innovus

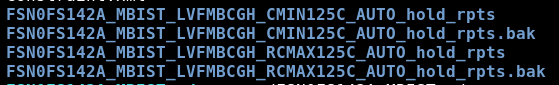
* Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC/Gen\_MBIST\_Expand

* Run FSTA to generate “FSN0FS142A\_MBIST\_expand.sdc”



**Result:**





- Copy “FSN0FS142A\_MBIST\_expand.sdc” to: /home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC/SDC\_ECO

+ Add this below constrain to copy file:



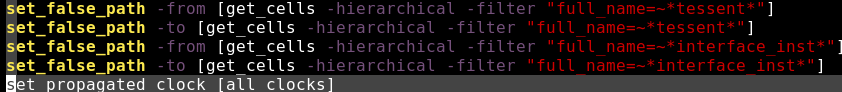
**Step 5: FSN0FS142A.sdc**

To modify Function SDC to skip timing check for paths related MBIST

* Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC/SDC\_ECO

- Copy Function SDC to SDC\_ECO folder and add these below setting:



**Step 6: DFT\_size\_only.sdc & dont\_touch\_only.sdc**

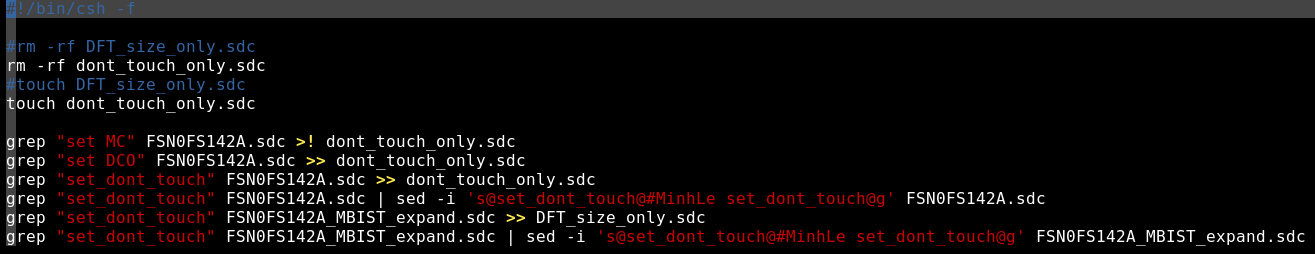
To extract "set\_dont\_touch" command from Function SDC and MBIST SDC to DFT\_size\_only.sdc

To separate don’t touch type for PI, for TM cell, R&D already define as don’t touch, but for tessent cell, it should still be allow to use size cell

* Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Modify\_SDC/SDC\_ECO

- Use “make\_size\_only.csh” to make “DFT\_size\_only.sdc” & “dont\_touch\_only.sdc”



**Set don’t touch for memories and clock source**

**Take all “set don’t touch” from Function SDC**

**For tessent cell, it should still be allow to use size cell**

POST DFT DATA CHECK

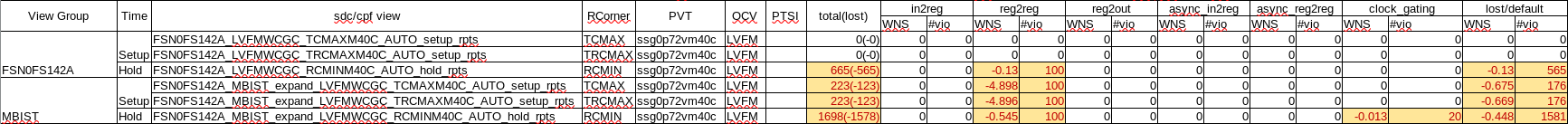
* **FLEC (has been done after FECO)**
* **FLRE**
* **FERC**
* **FSTA:**

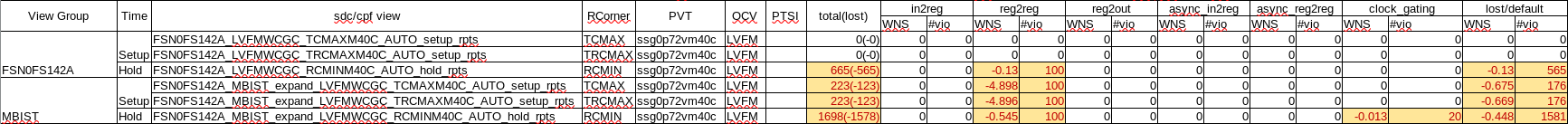
Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Fsta/Pre\_STA/TDI\_21\_05

|  |  |  |
| --- | --- | --- |
| **Input Files** | | |
| Netlist | SDC (after modifications) | Setup |
| FSN0FS142A.v.feco0  TMU1\_GCLD.v  TMU2\_GCLD.v | FSN0FS142A\_MBIST\_expand.sdc  FSN0FS142A.sdc | setup.ftc.sta |

**First result:**



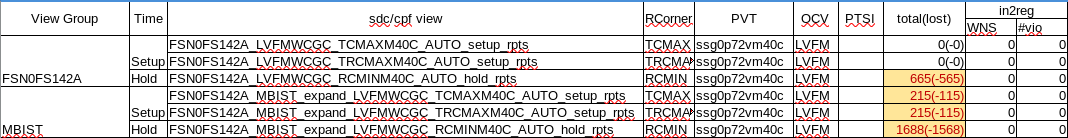


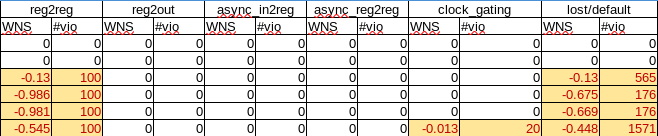
With FSN0FS142A\_MBIST\_expand.sdc, the WNS value is quite big.

\*Note: Add 2 below “set\_case\_analysis” to FSN0FS142A\_MBIST\_expand.sdc for reducing timing violation



**Second result:**





## PRE SIMULATION

a. Gen pattern

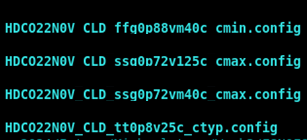
Step 1: Generate DCO config file

Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data/ gen\_DCO\_config\_by\_script

- Prepare config files:

DCO config for all clock for each corner

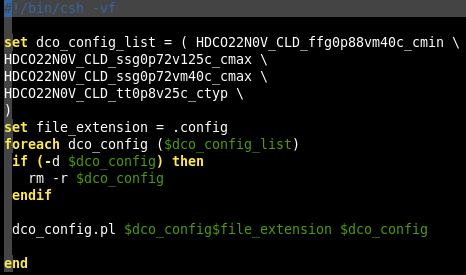


- Update project name in “dco\_config.pl”

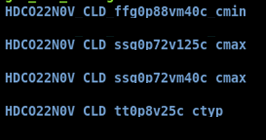
Script to convert DCO config from \*.config to \*.ftlcon format



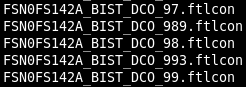
- Run “gen\_dco\_config.csh”

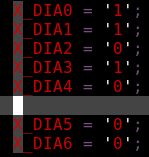


**Output:** 4 folers of 4 DCO config files contains .ftlcon files



DCO config each clock





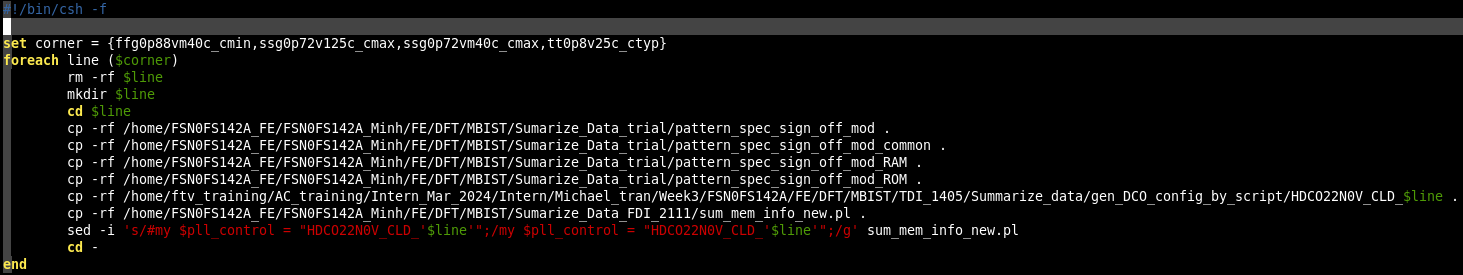
Step 2: Summarize data

Generate sign-off pattern based on tsdb (tessent database) after inserting mbist circuit

* Working directory:

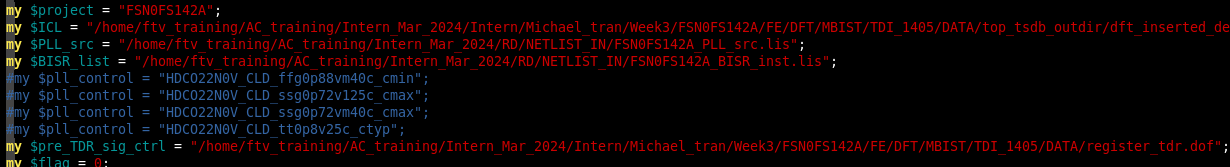
/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data

* Use “make\_file.csh” to create 4 folders for 4 corners with “pattern\_spec\_sign\_off\_mod”, “sum\_mem\_info.pl” & DCO config folders for each corner.

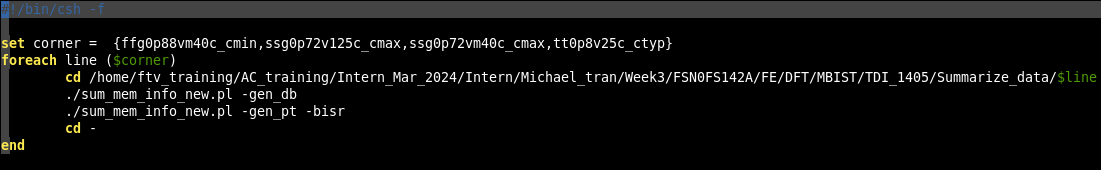


**Uncomment “my $pll\_control” for corresponding corner**

* Update information in “sum\_mem\_info\_new.pl”



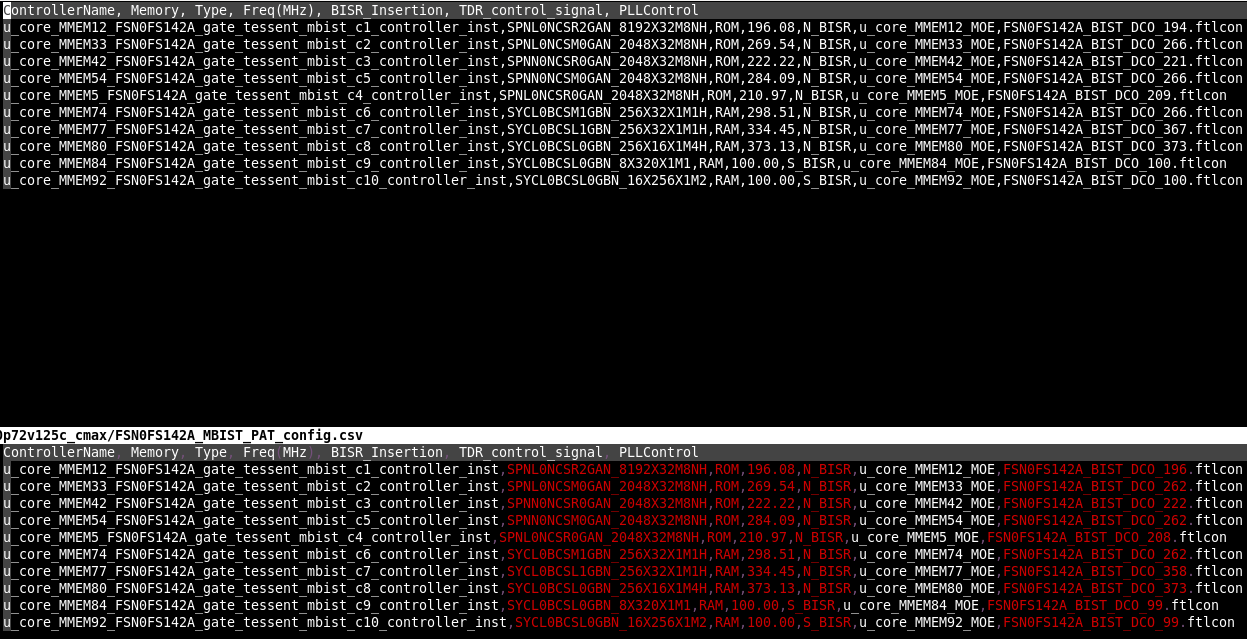
- Run “gen\_db\_pt.csh”

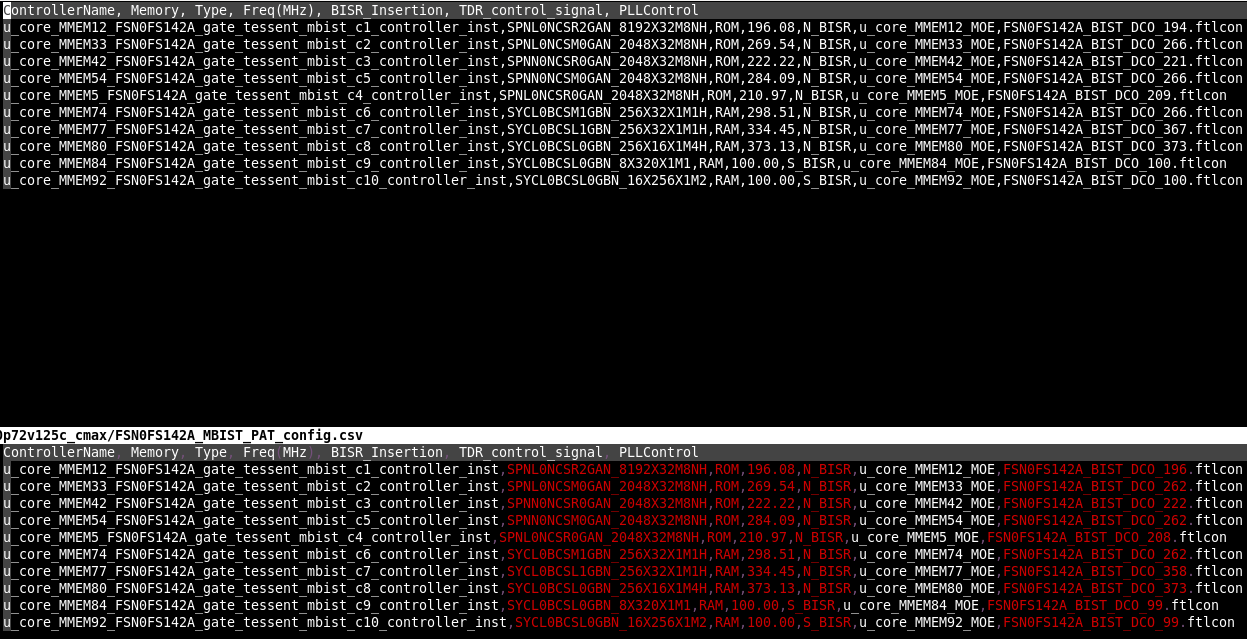


**2 options to summarize data**

**Output:**

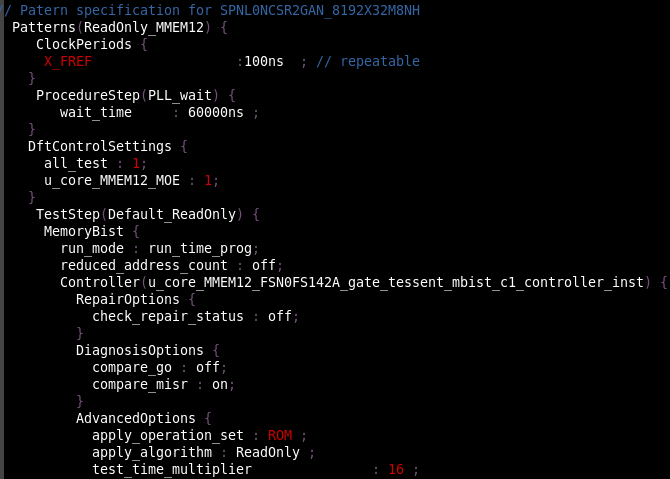
FSN0FS142A \_MBIST\_PAT\_config.csv (include MBIST informations)





FSN0FS142A\_pt/pattern\_spec\_sign\_off\_FSN0FS142A (pattern specifications for each corner)





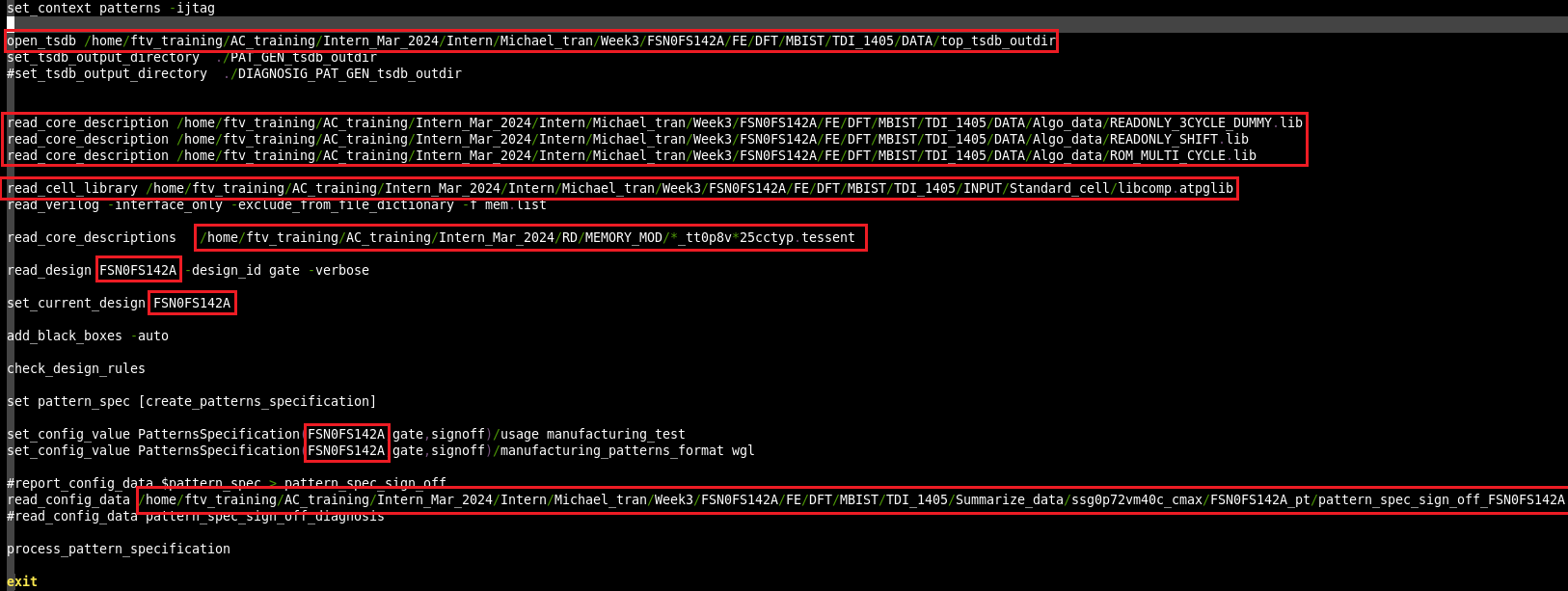
Step 3: Gen pattern

\*Note: Just choose worst corner to gen pattern

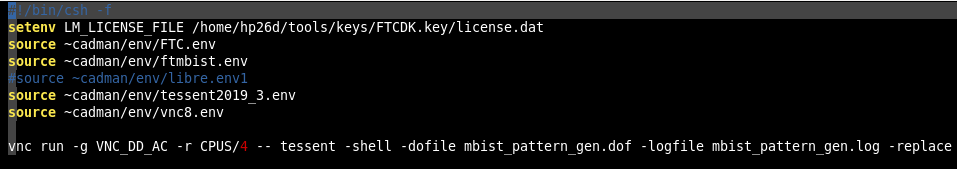
Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data/Gen\_pattern

- Modify “mbist\_pattern\_gen.dof”

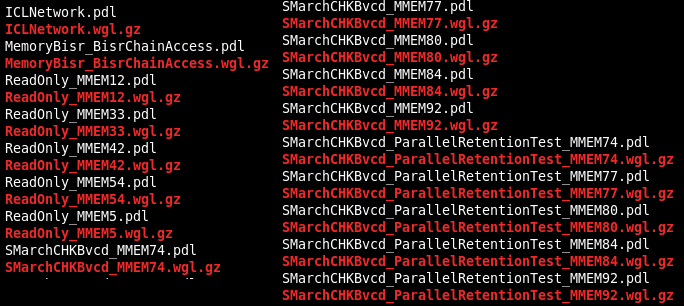


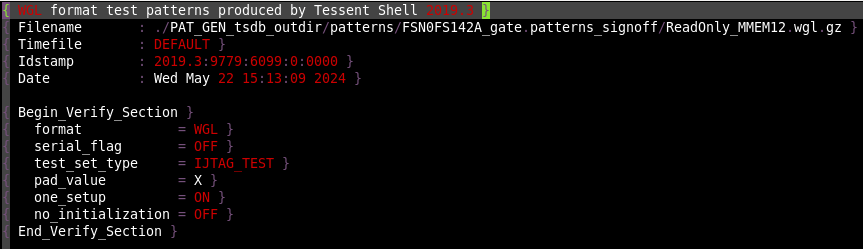
- Run “run\_gen\_pattern”



**Output:**

PAT\_GEN\_tsdb\_outdir/patterns/ FSN0FS142A\_gate.patterns\_signoff/.\*wgl.gz





Step 4: Resequence patterns

1/ Gen FTL file

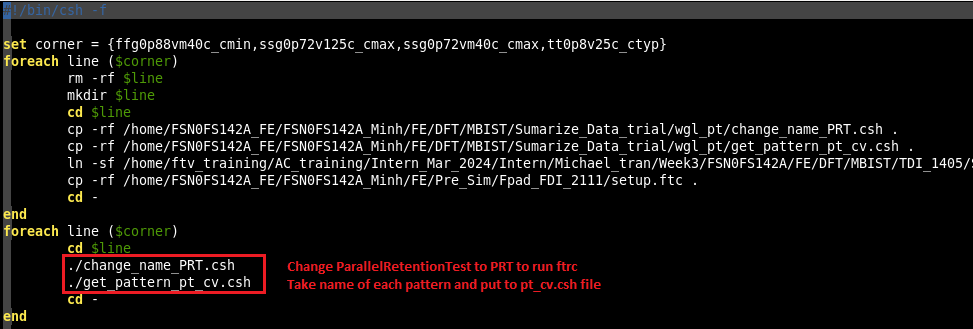
Convert .wgl.gz patterns to .ftl patterns

\*Note: Just choose worst corner to gen pattern

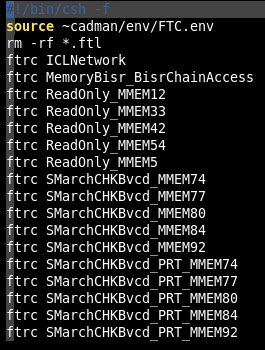
Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data/wgl\_pt

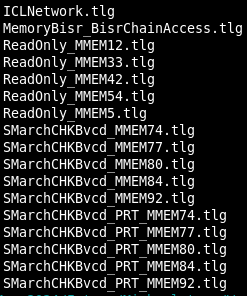
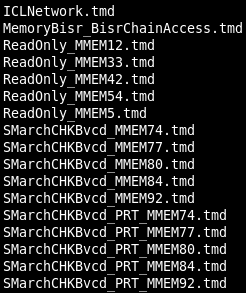
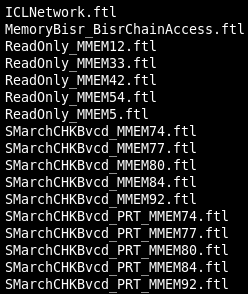
- Use “make\_file.csh” to create 4 folders for 4 corners with “change\_name\_PRT.csh”, “get\_pattern\_pt\_cv.csh”, “setup.ftc” & correspoding .wgl.gz files for each corner.

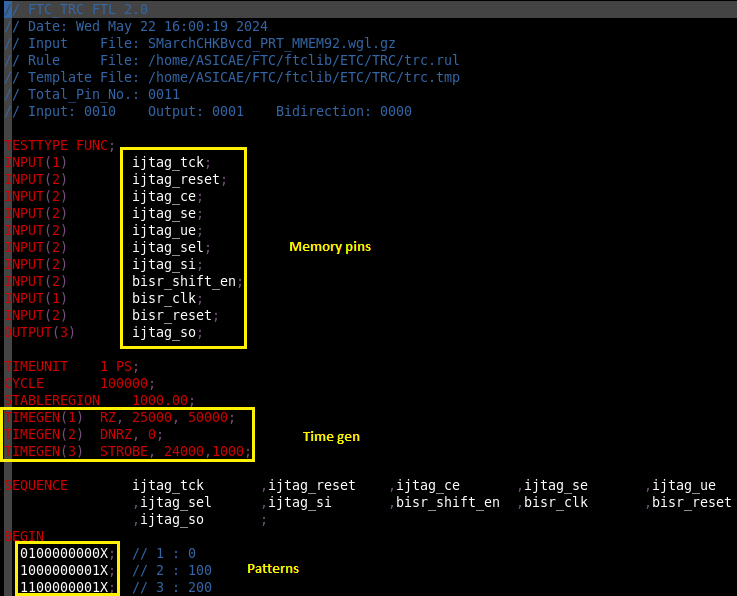


- Run “pt\_cv.csh” in worst corner to run FTRC (Faraday Test Rule Check)



**Output: .ftl (patterns), .tmd (options for ftrc), .tlg (log files)**





2/ Resequence pattern

Mapping memory pins to control from top level module

Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data/FTL\_gen

- Run FPAD in Pre-Sim folder:

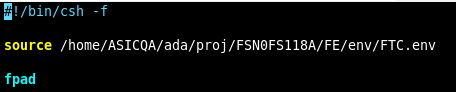
/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/Pre\_Sim/TDI\_Post\_DFT/fpad/

|  |  |  |
| --- | --- | --- |
| **Input Files** | | |
| Netlist | Pin pad assignment (ppa) | Setup |
| FSN0FS142A.v.feco0  TMU1\_GCLD.v  TMU2\_GCLD.v | FSN0FS142A.ppa   * Generate template for FTL header file | setup.ftc |

* Modify “setup.ftc”



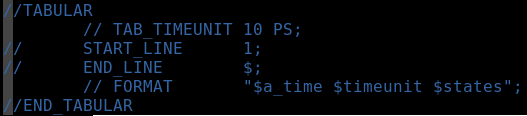
* Run “run\_fpad.csh”



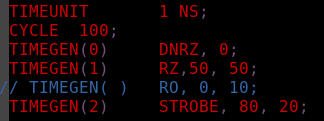
**Output:**



* Modify “FSN0FS142A.th”
* Comment out all the lines below

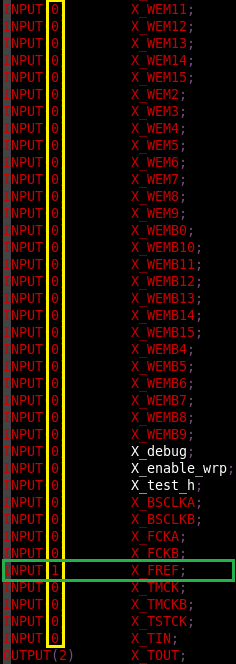
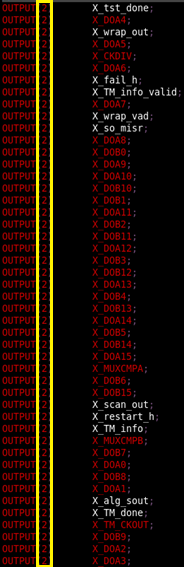


* Fix the timegen



* Fix the value timegen



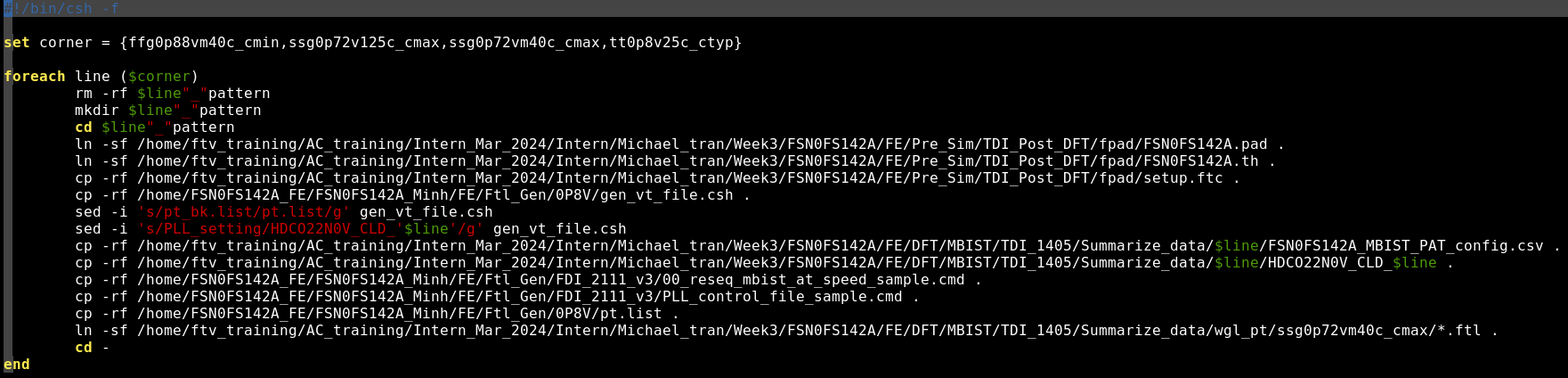


3/ Gen pattern

Working directory:

/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Michael\_tran/Week3/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/Summarize\_data/FTL\_gen

- Run “make\_file\_ftl.csh” to gen 4 folders for 4 corners. In each corner:



+ link .pad, .th file from FPAD folder

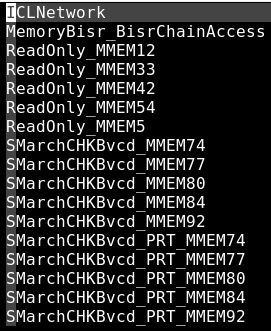
+ prepare “setup.ftc"

+ copy “gen\_vt\_file.csh” and modify the define of pattern list, DCO config folder for each corner

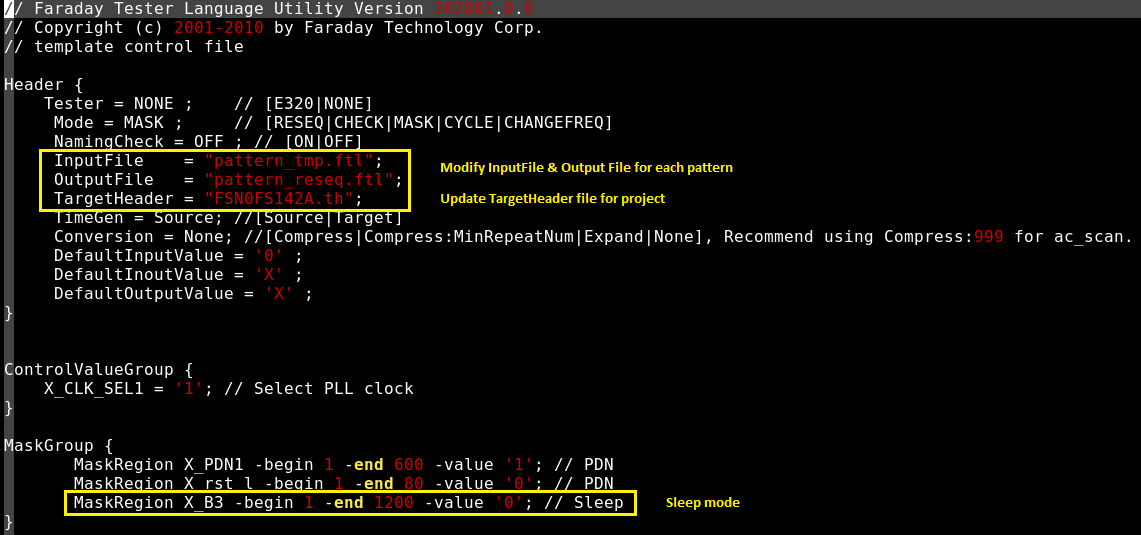
+ copy .csv files, DCO config folders (.ftlcon files) of corresponding corner

+ Link all .ftl file from worst corner folder at Resequence pattern step

+ Make “pt.list” contains pattern name:

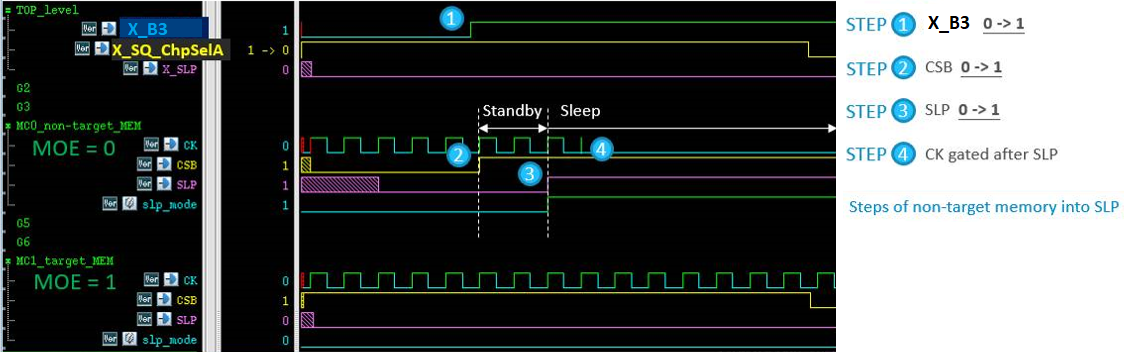


+ Prepare “PLL\_control\_file\_sample.cmd” & “reseq\_mbist\_at\_speed\_sample.cmd”

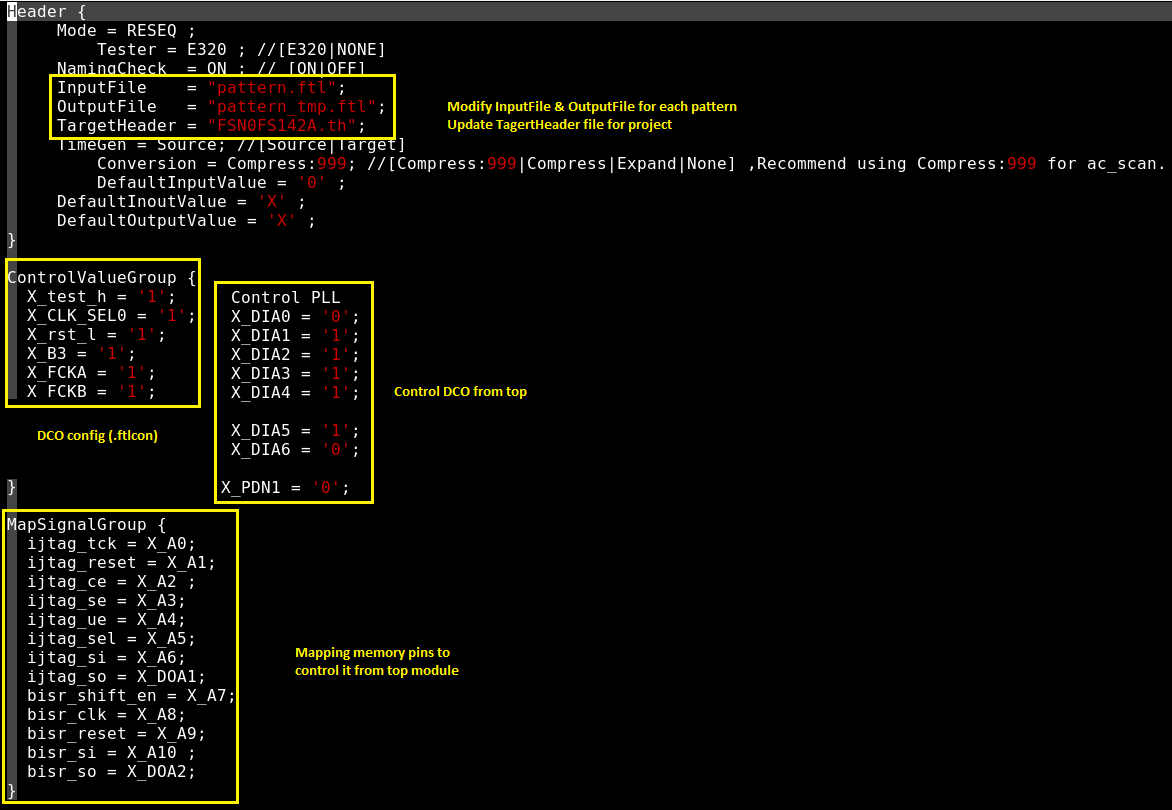


**“PLL\_control\_file\_sample.cmd”**

\*Sleep mode:

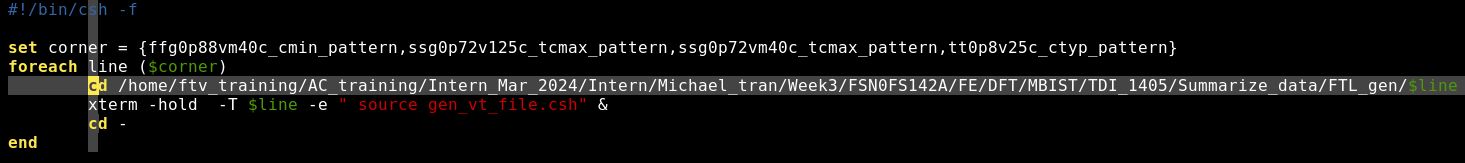






**“reseq\_mbist\_at\_speed\_sample.cmd”**

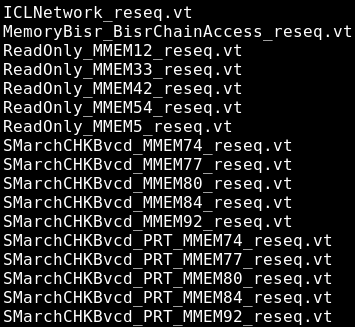
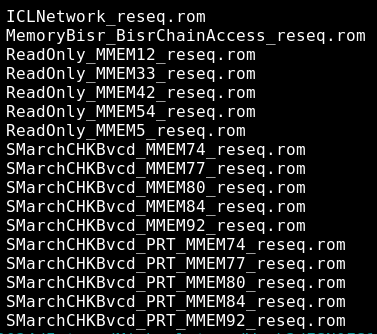
* Run “run\_file\_ftl.csh” to generate .vt & .rom files for each corner



gen\_vt\_file.csh



**Output:**



Step 5: Run simulation Fsim