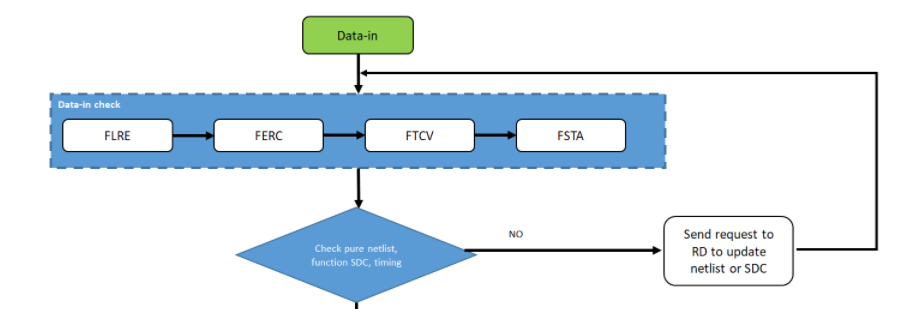
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name |  | No. |  | Div/Dept | DSD/ACD/ACT | Job  Date：2024/03/29  Title | Intern |
| Please tick  the period | First Month | □W1 🗹W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

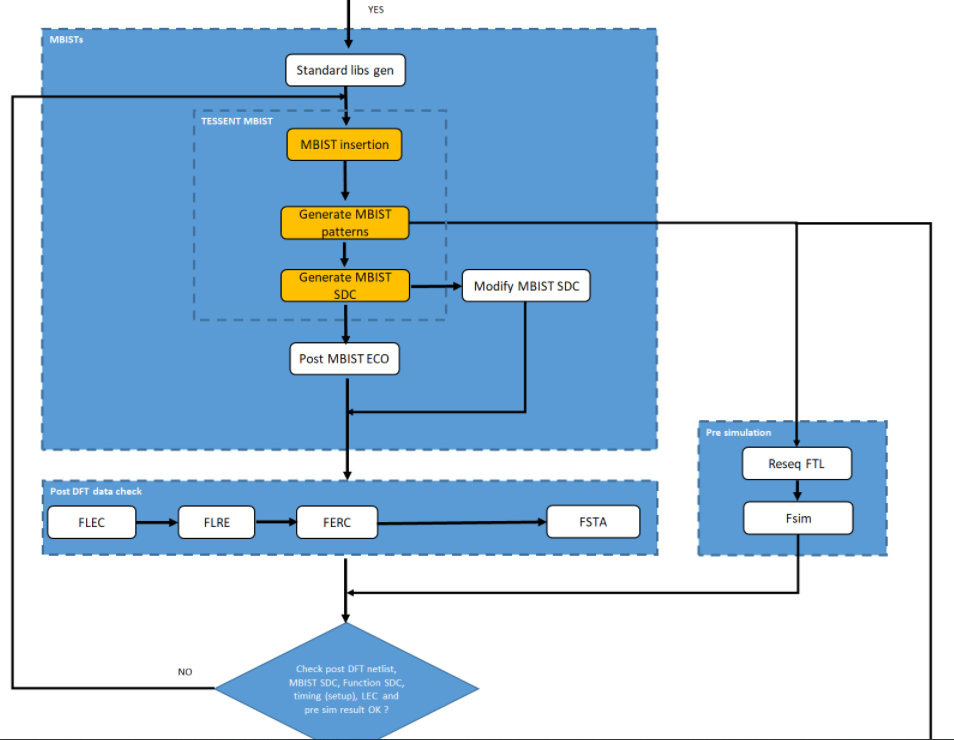
1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

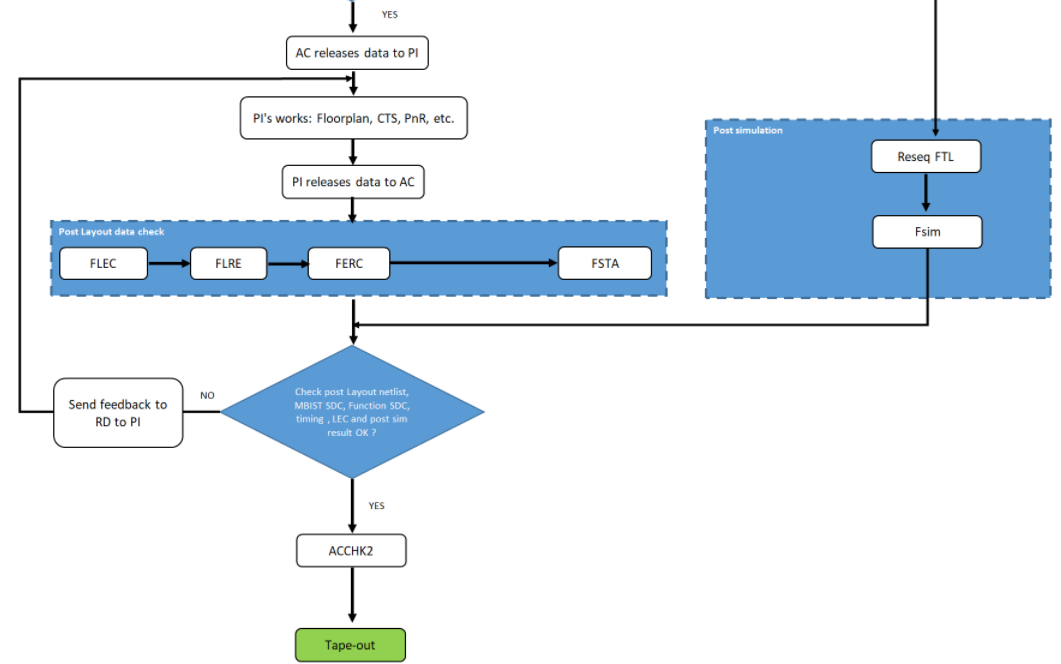
|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2024, below are a brief description of the tasks and what I learned:   * Understanding Test chip flow * Reading basic about MBIST concept * Practice to insert MBIST to the netlist |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Have trouble while trying to figure command purpose * Don’t understand clearly about Rom code file pattern |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Continue running Test Chip flow |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Ho Nguyen Hoang 27/07/2024 | (Signature/Date) | (Signature/Date) |

**I. Test chip flow**







# **2. MBIST concept**

## **a. BIST (Built-In Self-Test):**

- BIST is a DFT technique used in VLSI to test the functionality of integrated circuits (ICs) during the manufacturing process and throughout the product's life.

- This circuitry can be designed to test various aspects of the IC, such as logic gates, memory and communication interfaces.

## **b. MBIST (Memory Built-In Self-Test)**

**- MBIST architecture:**

+ Controller: Provide control signal to address/background generators

+ Comparator: CP data read from memory during a read operations with the golden data

+ Background Pattern generator: Generate data for memory to perform the write operations, which controlled by the controller

\_Binary/Gray counter

\_LSFR

+ Address generator:

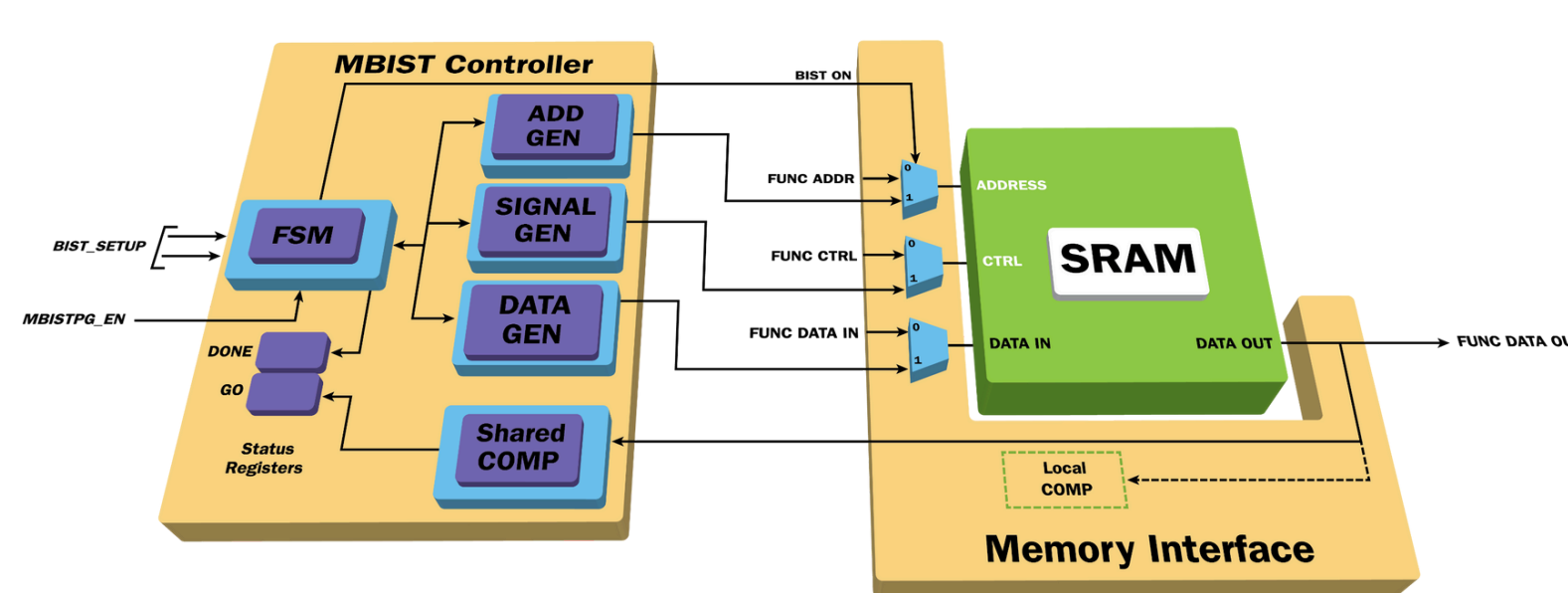
+ FSM: Control read and write signals

+Mux

\_Test\_mode: select the address and data generators

\_Normal\_mode: select the address and data from the processor

|  |  |
| --- | --- |
| Memory RAM test | Memory ROM test |
| March Test Pattern  March C+ Algorithm  Checkerboard algorithm | MISR (Multiple Input Shift Register) Algorithm: (Reduce test logic by using multiple bit streams to create a signature.) |



## **c. MBIST insertion**

**- Compile standard library to tessent library**

**Working directory: /INPUT/Standard\_cell**

|  |  |
| --- | --- |
| **Input** | libcomp.do.default |
| **Output** | libcomp.atpglib |
| **Run file** | run\_libcomp |



**- Mbist insertion**

**+ mbist\_insertion.dof**

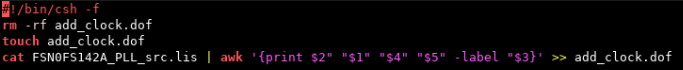
**Working directory: /DATA**

|  |  |  |
| --- | --- | --- |
| **Input** | <Project>\_PLL\_src.lis  <Project>.v  <Project>\_MBIST\_inst.lis  go\_make\_add\_clock.csh  func\_debug  .synnosyp\_dc.setup  dft\_cell\_select.tcl  mbist\_insertion.dof  Instance\_need\_MBIST.dof  mem.list  register\_tdr.dof  add\_clock.dof | PLL clock source list for memories  # Pure netlist  # MEM instances need MBIST  # Script to extract clock period  # For synthesis  # For synthesis  # Define cell type for MBIST insertion, it can be modified for design intention  # Insert mbist circuit, could be modified based on feature of type and project  # Set memories instance option for BIST and BISR  # memories list path  # set static register static dft signal  # Clock period file |
| **Output** | <Project>.vg  <Project>.sdc | # Post MBIST netlist  # MBIST SDC |
| **Run file** | run\_mbist.csh |  |

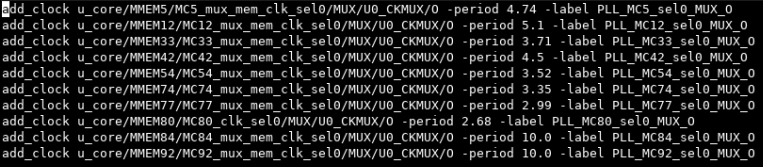
**Step 1:** *>> mem.list*



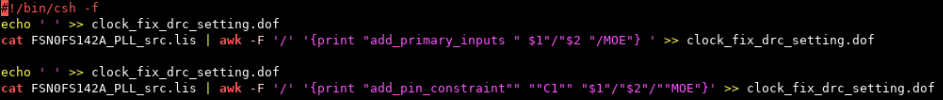
**Step 2*:*** *./go\_make\_add\_clock.csh*



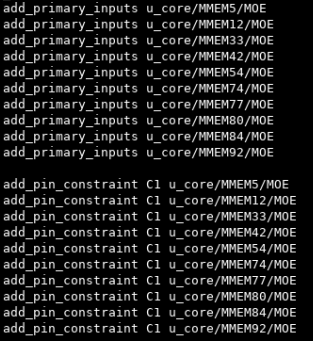
*>> add\_clock.dof: Define the clock applied to primary input that is used for MBIST*



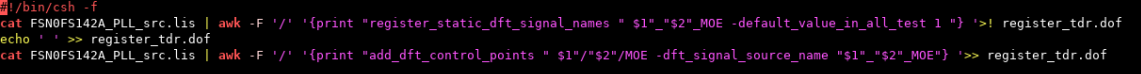
**Step 3**: *./go\_make\_clock\_fix\_drc.csh*



*>> clock\_fix\_drc\_setting.dof*



**Step 4:** *./go\_make\_register\_tdr.dof*

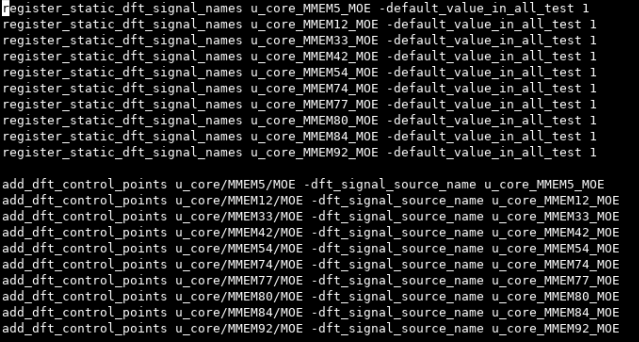


*>> register\_tdr.dof*

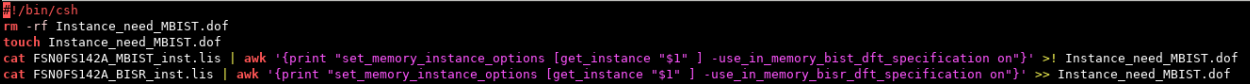
*register\_static\_dft\_signal\_name: create a new dft\_signal and specify its behavior -default\_value\_in\_all\_test: all signals use the specified default value*

*add\_dft\_control\_points: insert the controlling logic during DFT insertion –*

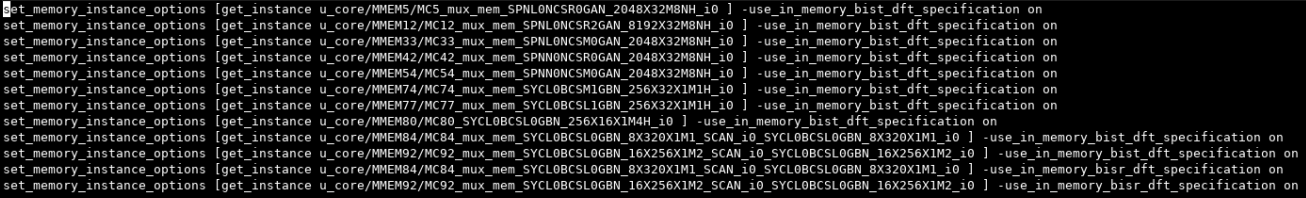
*dft\_signal\_source\_name: source the pins during test mode.*



**Step 5:** *./go\_make\_Instance\_need\_MBIST.dof*



>> *Instance\_need\_MBIST.dof*

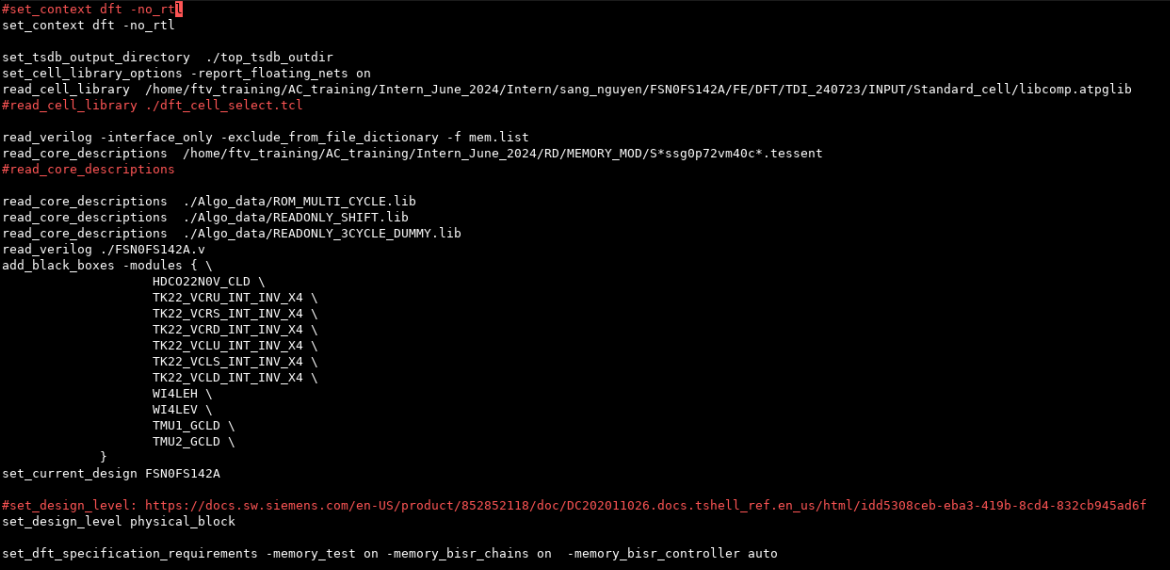


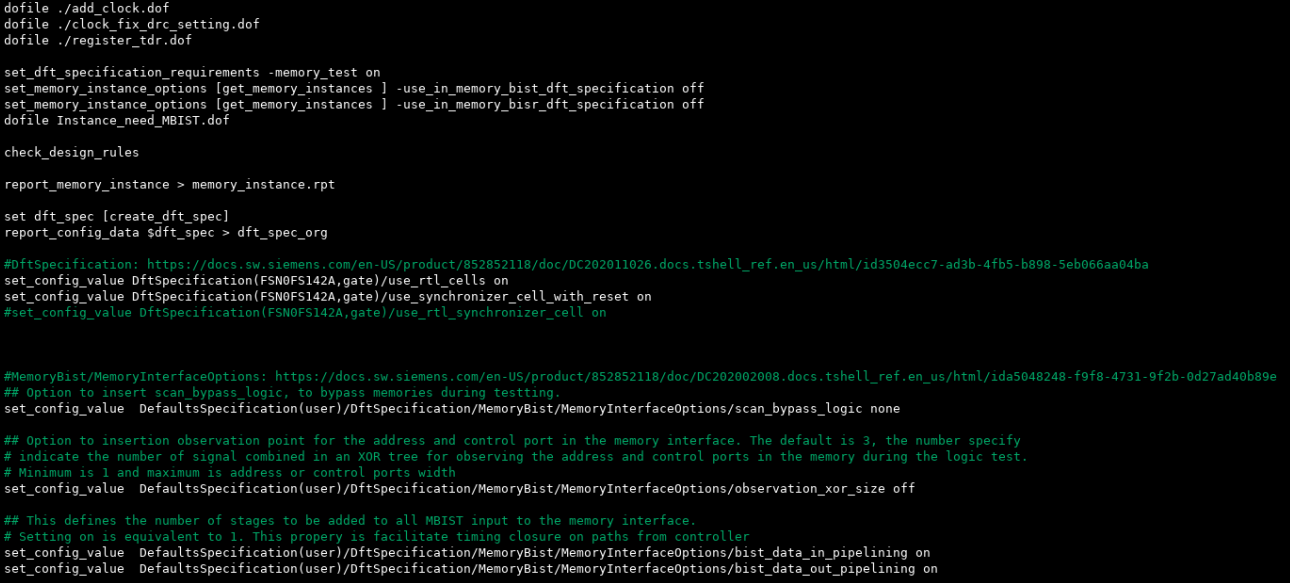
**Step 6:**

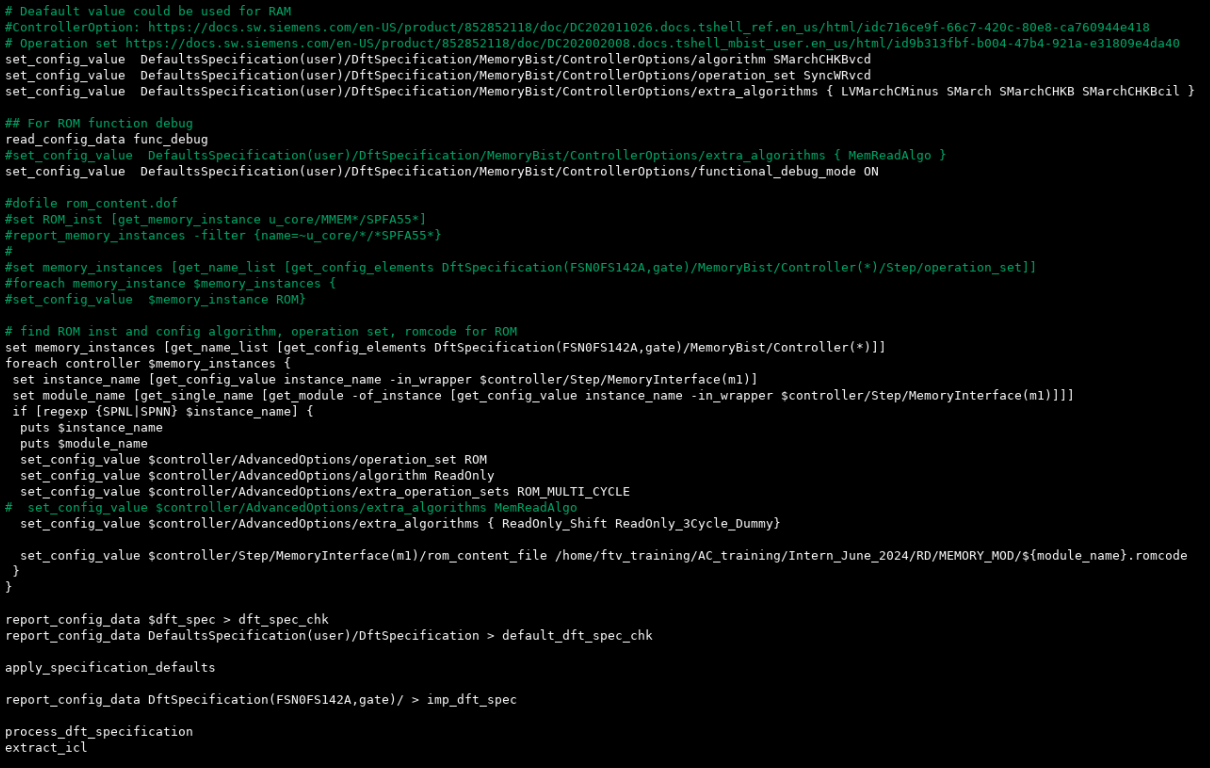
*>> func\_debug*

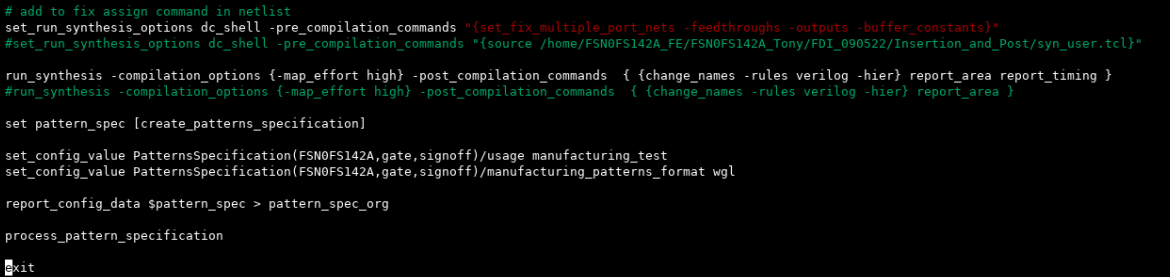
*>>./synopsys\_dc.setup*

**Step 7:** *>> mbist\_insertion.dof*

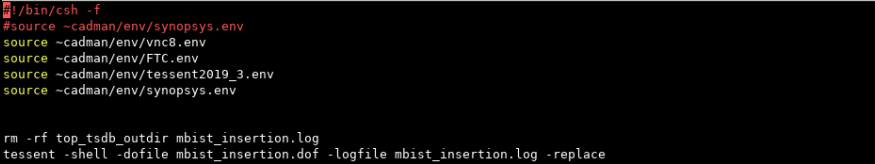








**Step 8:** **./run\_mbist.csh**



*>> top\_tsdb\_outdir*

**+<Project>\_ts\_post.cmd**

**Working directory: /MBIST\_Post**

|  |  |  |
| --- | --- | --- |
| **Input** | <Project>.vg  <Project>\_ts\_post.cmd  dft\_cell\_select.tcl  Fix\_Assign.pl | # Post MBIST netlist  # Do file for post MBIST ECO  # Define cell type for MBIST insertion, it can be modified for design intention  # Script to fix assign command in gate netlist (connect buffer from port chip) |
| **Output** | <Project>.v.fixass | # Post MBIST netlist after replacing assign command |
| **Run file** | run\_mbist.csh |  |

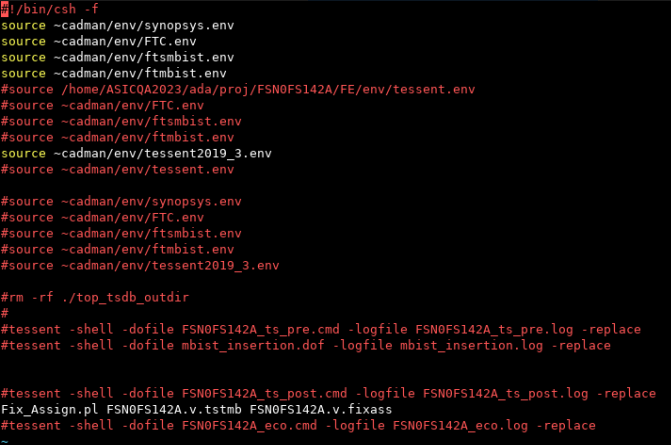
**Step 1:** *>> dft\_cell\_select.tcl*



**Step 2:** *>> <Proj>\_ts\_post.cmd*

***Step 3:* Run post MBIST ECO**

*./run\_mbist.csh*



*>> <Proj>.v.tstmb*

*>> <Proj>.v.fixass*

**+ ECO to fix "Non-equivalent signal" when running FLEC for pure netlist and post MBIST netlist**

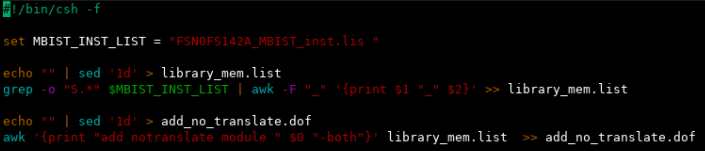
**Working directory: /ECO**

|  |  |  |
| --- | --- | --- |
| **Input** | <PROJ>\_MBIST\_inst.lis  <PROJ>.v  <PROJ>.v.fixass  gen\_no\_translate.csh  gen\_mbist\_constraint.pl  flec.cmd  batchResults.tcl  flec.log  <PROJ>.mod  <PROJ>.v.fixass  setup.ftc  make\_eco.csh | # List of memory needs MBIST  # Pure netlist  # Post MBIST netlist after replacing assign command  # Script to generate "library\_mem.list" and "add\_no\_translate.dof"  # Script to generate "mbist\_constraint.dof"  # Command file of FLEC, need to update for each project  # Log file of FLEC  # List \*.v file  # Post MBIST netlist after replacing assign command  # Design Kit setup file  # Generate "eco\_reconnect\_bisr.tcl" file |
| **Output** | <PROJ>.v.feco0 | # Post MBIST netlist after replacing assign command |
| **Run file** | run\_flec.csh  run\_feco.csh |  |

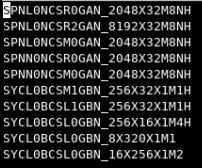
**Step 1: RUN FLEC**

**Working directory: /ECO/FLEC\_post\_dft**

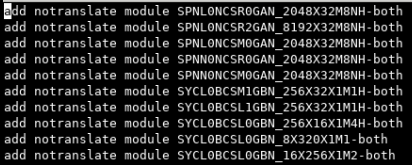
./gen\_no\_translate.csh



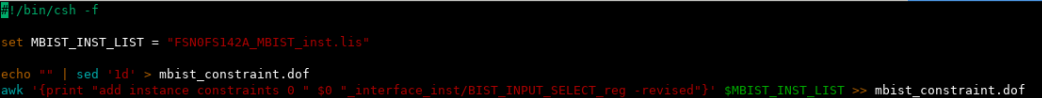
**>>**library\_mem.list



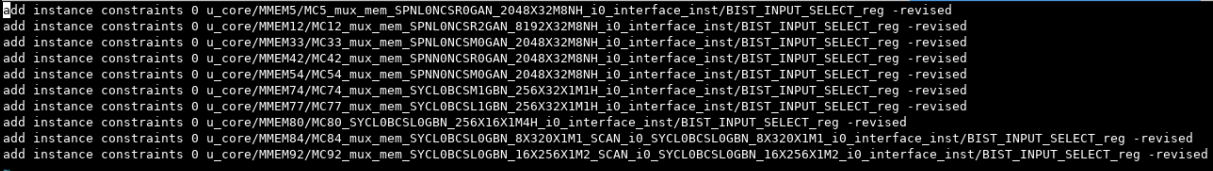
**>>**add\_no\_translate.dof



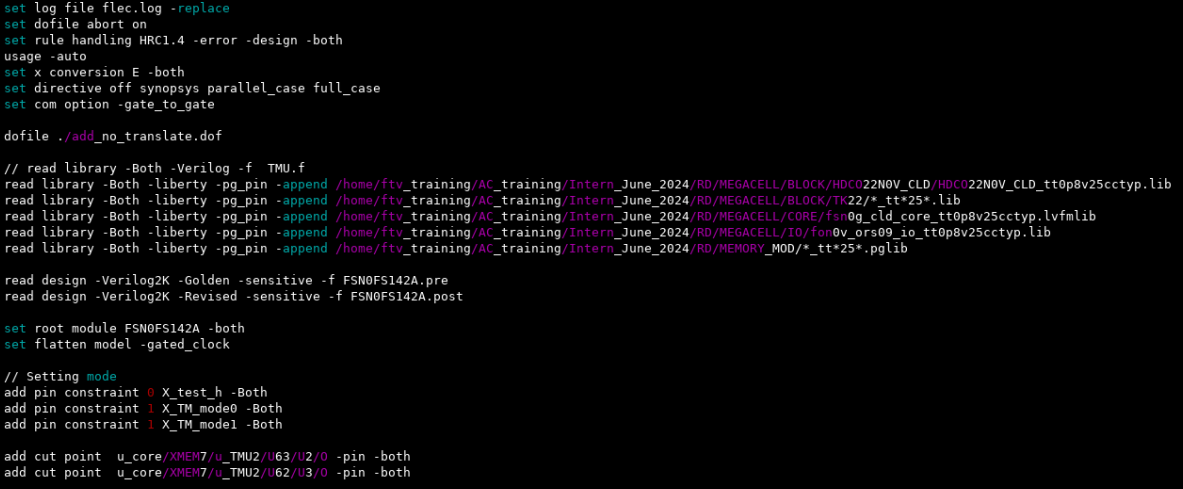
./gen\_mbist\_constraint.pl



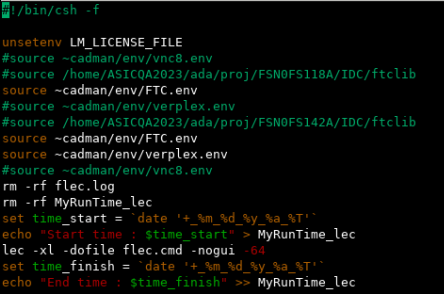
>> mbist\_constraint.dof



Update flec.cmd



*./run\_flec.csh*

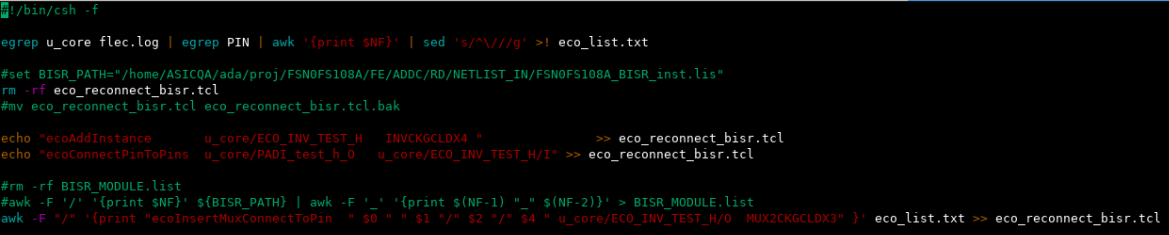


*>>flec.log*

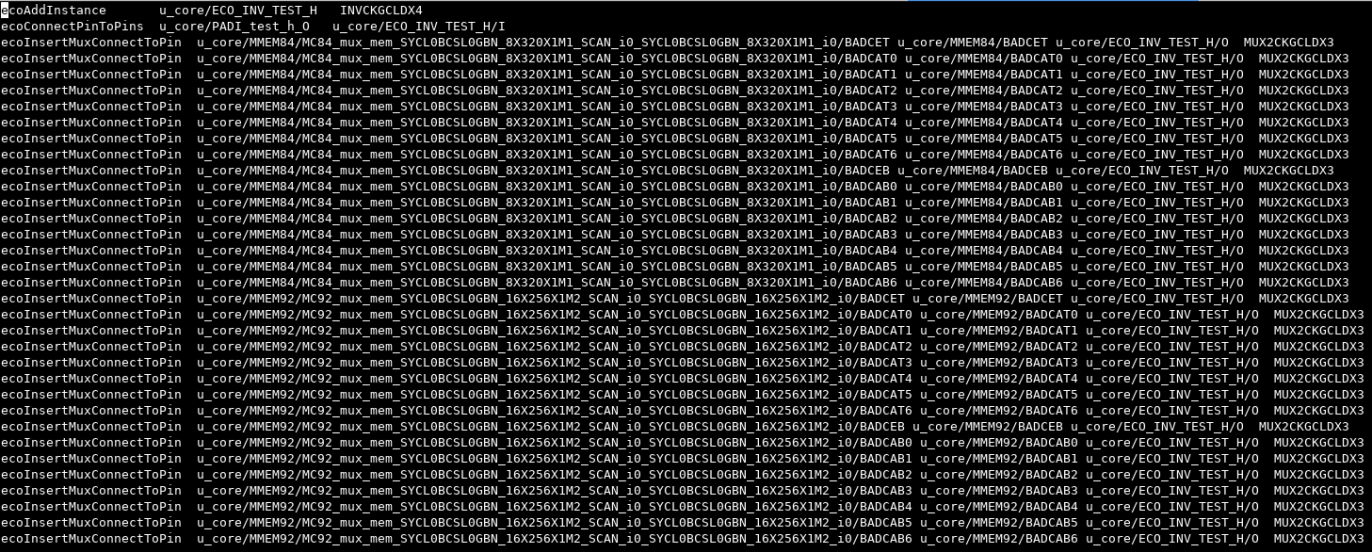
**Step 2: Run ECO**

**Working directory: /ECO/ECO\_post\_dft**

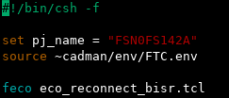
*./make\_eco.csh*



*>>* eco\_reconnect\_bisr.tcl



*./run\_feco.csh*



*>> <Proj>.v.feco0*

**Step 3: Re-run FLEC**