|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name |  | No. |  | Div/Dept | DSD/ACD/ACT | Job  Date：2024/03/29  Title | Intern |
| Please tick  the period | First Month | □W1 🗹W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2024, below are a brief description of the tasks and what I learned:   * Practicing Test Chip Flow: Know how to generate pattern |
| 2. What are the problems encountered this week? Any actions taken? Any help needed? |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Practice to run and pass fsim |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Ho Nguyen Hoang 02/08/2024 | (Signature/Date) | (Signature/Date) |

# **I. Modify SDC**

**Working directory: /Modify\_SDC**

|  |  |  |
| --- | --- | --- |
| **Input** | FSN0FS142A.sdc FSN0FS142A.sdc mbist\_sdc\_tail.sdc  user\_clk.sdc | **#** MBIST SDC generated by tessent tool  **#** Function SDC  **#** The configuration includes mode setting of memory in user sdc, test mode X\_test\_h and some other value setting of set\_input\_transition, set\_load, don’t touch cell, clock gating check  **#** Clock generation extracted from function SDC |
| **Output** | FSN0FS142A\_MBIST.sdc  FSN0FS142A.sdc DFT\_size\_only.sdc | **#** MBIST SDC  **#** Function SDC  **#** set\_dont\_touch |
| **Run file** | modify\_sdc.csh  make\_size\_only.csh | **#** Script to change port name of IJTAG and BISR and merge "mbist\_sdc\_tail.sdc" , "user\_clk.sdc" and MBIST SDC to one " FSN0FS142A\_MBIST.sdc"  **#** Script to extract "set\_dont\_touch" command from MBIST SDC & Function SDC to "DFT\_size\_only.sdc" |

**1. mbist\_sdc\_tail.sdc**

**2. user\_clk.sdc**

**3. FSN0FS142A\_MBIST.sdc**

**4. MBIST\_expand.sdc**

**5. FSN0FS142A.sdc**

**6. DFT\_size\_only.sdc**

# **II. Post DFT data check**

## **1. FLRE**

**Working directory: /flre**

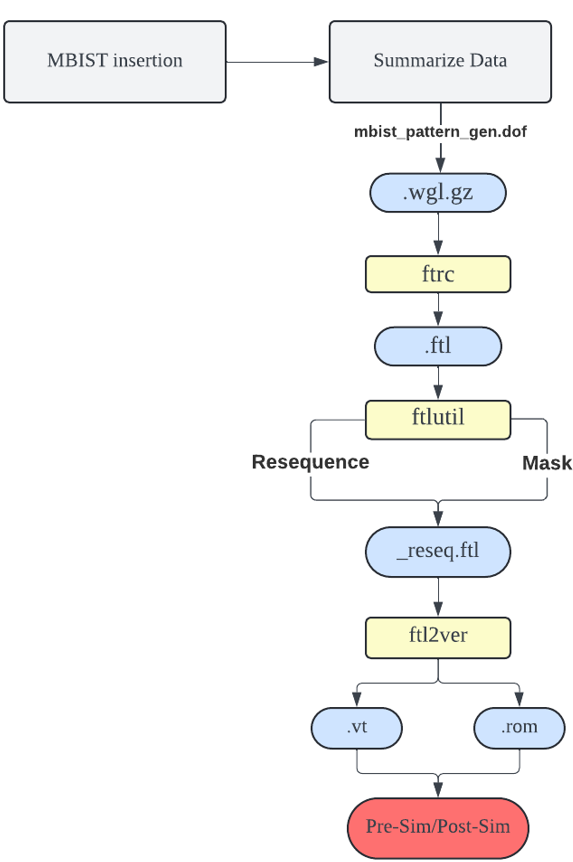
## **2. FERC**

**Working directory: /ferc**

## **3. FSTA**

**Working directory:**

# **III. Pre simulation**



1. **Gen pattern**
2. **Gen DCO config**

**Working directory: /Summarize\_data/gen\_DCO\_config\_by\_script**

|  |  |  |
| --- | --- | --- |
| **Input** | dco\_config.pl DCO110\_GVA\_<corner>.config | # Script to convert DCO config from \*.config to \*.ftlcon format  # DCO config for all clock for each corner |
| **Output** | FSN0FS142A \_BIST\_DCO\_<freq>.ftlcon | # DCO config each clock |
| **Run file** | gen\_dco\_config.csh | # Execution script to gen DCO config |

Step 1: 'Update "gen\_dco\_config.csh"

Step 2: 'Update "gen\_dco\_config.csh"

Step 3: 'Run "gen\_dco\_config.csh"

1. **Summarize data**

**Working directory: /Summarize\_data**

|  |  |  |
| --- | --- | --- |
| **Input** | pattern\_spec\_sign\_off\_mod pattern\_spec\_sign\_off\_mod\_common  pattern\_spec\_sign\_off\_mod\_RAM  pattern\_spec\_sign\_off\_mod\_ROM  FSN0FS142A\_PLL\_src.lis  PLL\_setting\_v2  register\_tdr.dof | # PLL source list |
| **Output** | FSN0FS142A\_MBIST\_PAT\_config.csv  pattern\_spec\_sign\_off\_FSN0FS142A | # DCO config each clock |
| **Run file** | sum\_mem\_info\_for\_PLL.pl | # Execution script to geenerate sign-off pattern |

Step 1: Update sum\_mem\_info\_for\_PLL.pl

Step 2: Gen DB: sum\_mem\_info\_for\_PLL.pl -gen\_db

Step 3: Gen PT: sum\_mem\_info\_for\_PLL.pl -gen\_pt -bisr

1. **Gen pattern**

**Working directory: /Summarize\_data/Gen\_pattern**

|  |  |
| --- | --- |
| **Input** | mbist\_pattern\_gen.dof |
| **Output** | PAT\_GEN\_tsdb\_outdir/patterns/<PROJECT>\_gate.patterns\_signoff/\*wgl.gz |
| **Run file** | run\_gen\_pattern |

Step 1: make file mbist\_pattern\_gen.dof

Step 2: Run script run\_gen\_pattern

1. **Resequence patterns**

Gen FTL file

**Working directory: /Summarize\_data/wgl\_pt**

|  |  |
| --- | --- |
| **Input** | Setup.ftc  <Pattern\_path>/wgl.gz |
| **Output** | \*\_PRT\_\*.ftl  \*\_PRT\_\*.tlg  \*\_PRT\_\*.tmd |
| **Run file** | change\_name\_PRT.csh  get\_pattern\_pt\_cv.csh  pt\_cv.csh |

Step 1: ./change\_name\_PRT.csh

Step 2: ./get\_pattern\_pt\_cv.csh

Step 3: ./pt\_cv.csh

Resequence pattern

**Working directory: /fpad**

|  |  |
| --- | --- |
| **Input** | FSN0FS142A.v.feco0  setup.ftc  FSN0FS142A.mod |
| **Output** | FSN0FS142A.pad  FSN0FS142A.th |
| **Run file** | run\_fpad.csh |

Step 1: Modify setup.ftc



Step 2: ./run\_fpad.csh

Step 3: Modify file <Project>.th

Gen pattern

**Working directory: /FE/Ftl\_gen**

|  |  |
| --- | --- |
| **Input** | FSN0FS142A.pad  FSN0FS142A.th  PLL\_control\_file\_sample.cmd  FSN0FS142A\_MBIST\_PAT\_config.csv  pt.list  setup.ftc  PLL\_setting\_v2 |
| **Output** | PLL\_control\_file\_\*́.cmd  00\_reseq\_\*.cmd |
| **Run file** | gen\_vt\_file.csh |

Step 1: Link "\*pad" and "\*.th" from fpad

Step 2:

PLL\_control\_file\_sample.cmd

00\_reseq\_mbist\_at\_speed\_sample.cmd

Step 3: List all MEMORY name to pt.list

Step 4: ./gen\_vt\_file.csh

1. **Run simulation Fsim**

**Working directory: /Fsim/Pre\_sim**

|  |  |
| --- | --- |
| **Input** | Template  pt.list |
| **Output** | ? |
| **Run file** | gen\_pre\_sim\_dir.csh  run\_sim\_dir.csh |

Step 1: template

Step 2: ./gen\_pre\_sim\_dir.csh

Step 3: ./run\_sim\_dir.csh

-Generate DCO\_config

\*.config to \*.ftlcon format

=> 4 folder ~ 4 corner => ftlcon format

-Summarize data

+Pattern spec for each corner

**Output:** FSN0FS142A \_MBIST\_PAT\_config.csv

FSN0FS142A\_pt/pattern\_spec\_sign\_off\_FSN0FS142A

-Gen pattern

+ mbist\_pattern\_gen.dof

**Ouput:** PAT\_GEN\_tsdb\_outdir/patterns/ FSN0FS142A\_gate.patterns\_signoff/.\*wgl.gz

- Resequence patterns

+Gen FTL file: Convert .wgl.gz patterns to .ftl patterns

*Use ftrc to generate .ftl pattern and and detect violations against the rules of testers*

*Rename the ParallelRetentionTest in to PRT to run ftrc*

+Reseq pattern: use fpad to to generate the pad file information for the test and simulation flow.

=> <DESIGN>.pad :Pad cell information of the design

<DESIGN.>.th: A template of the FTL header file

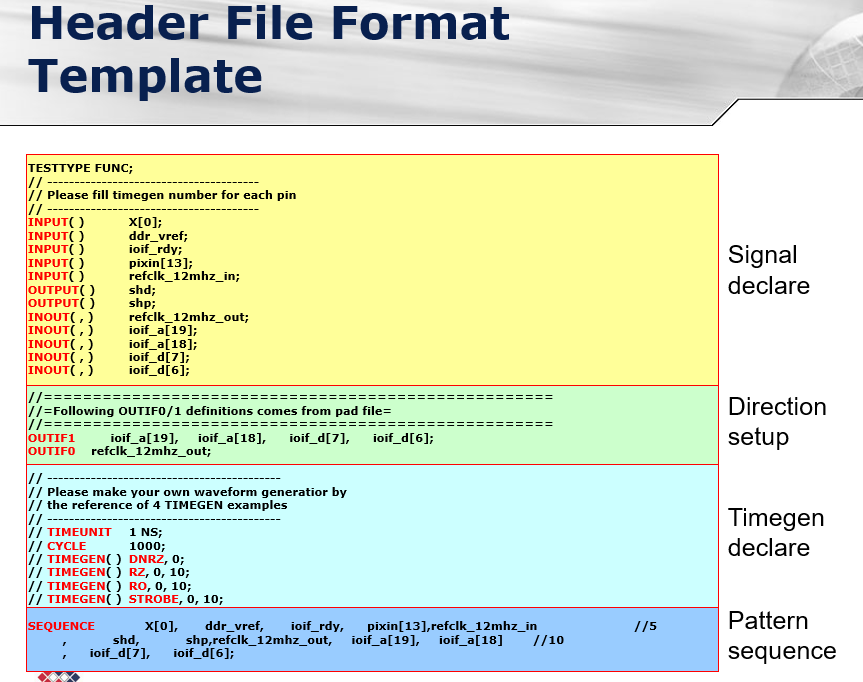
**Output: .ftl (patterns), .tmd (options for ftrc), .tlg (log files)**

FTRC (Faraday Test Rule Check)

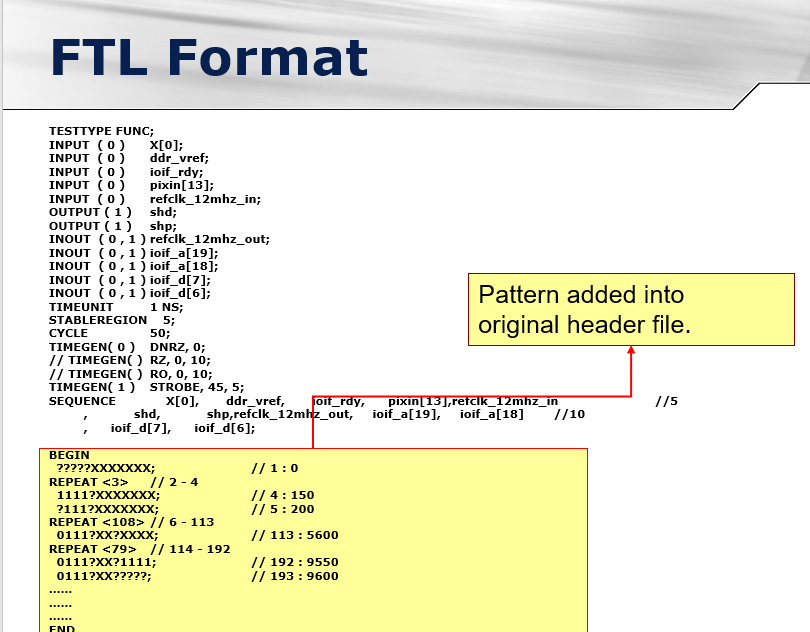
+Gen pattern: FTL gen

*PLL\_control\_file\_sample.cmd*

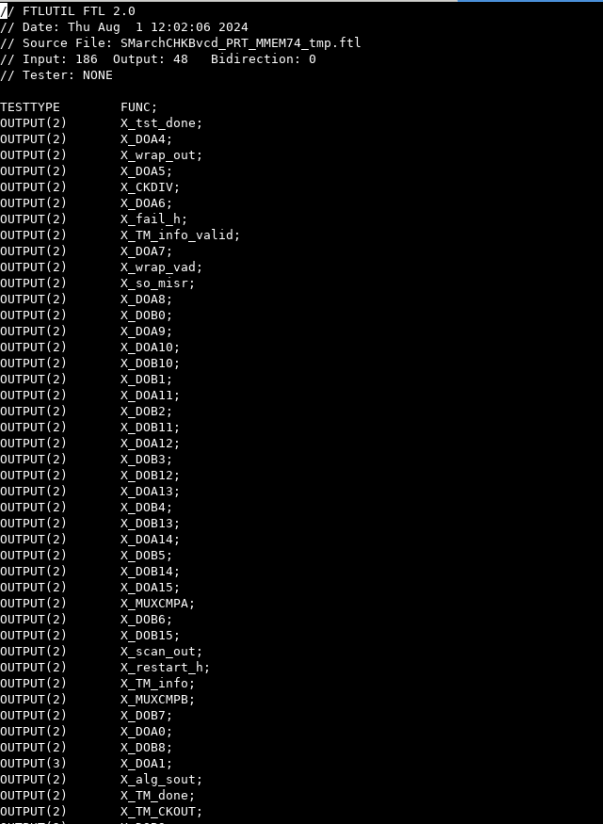
*00\_reseq\_mbist\_at\_speed\_sample.cmd*



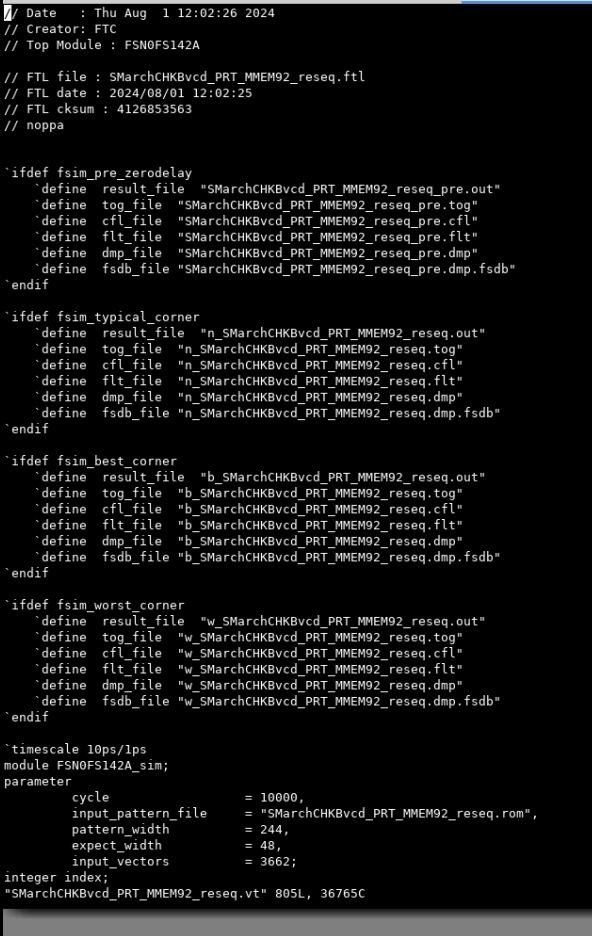
Use (header file ?) ftrc => .ftl



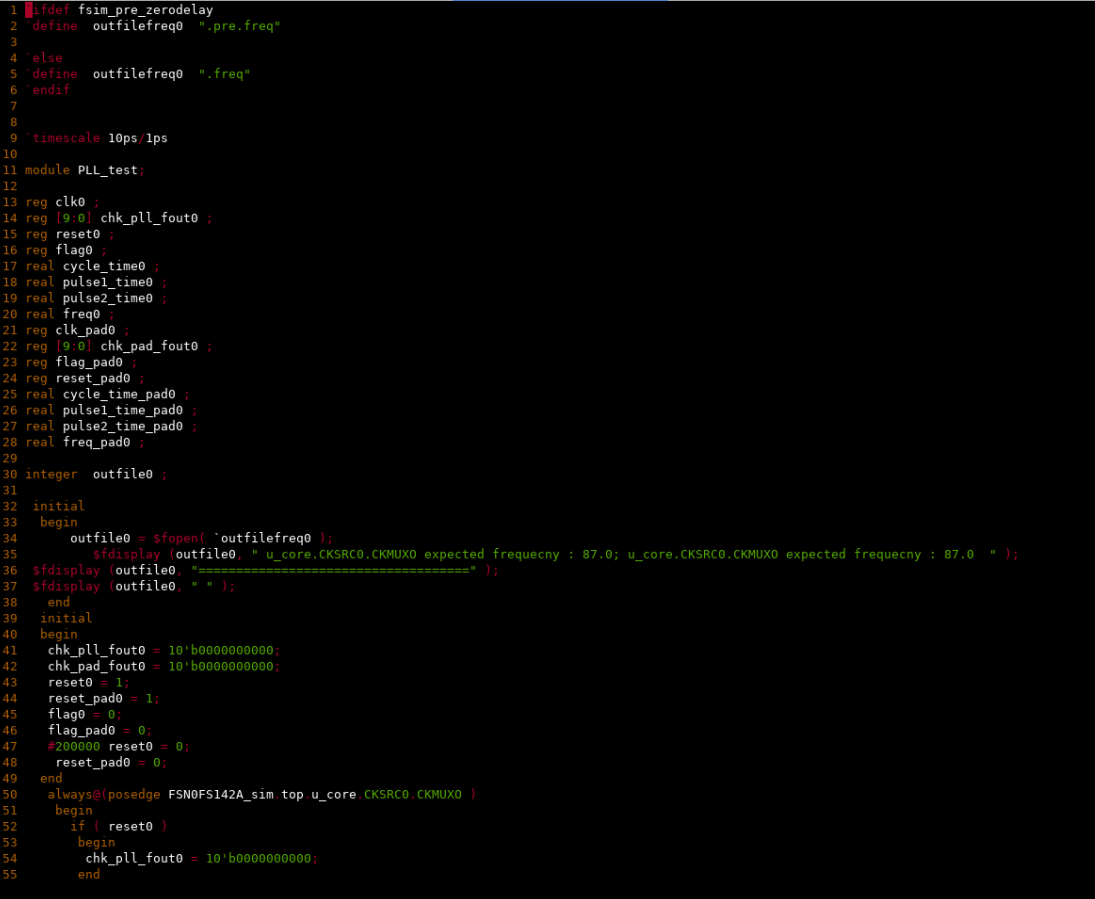
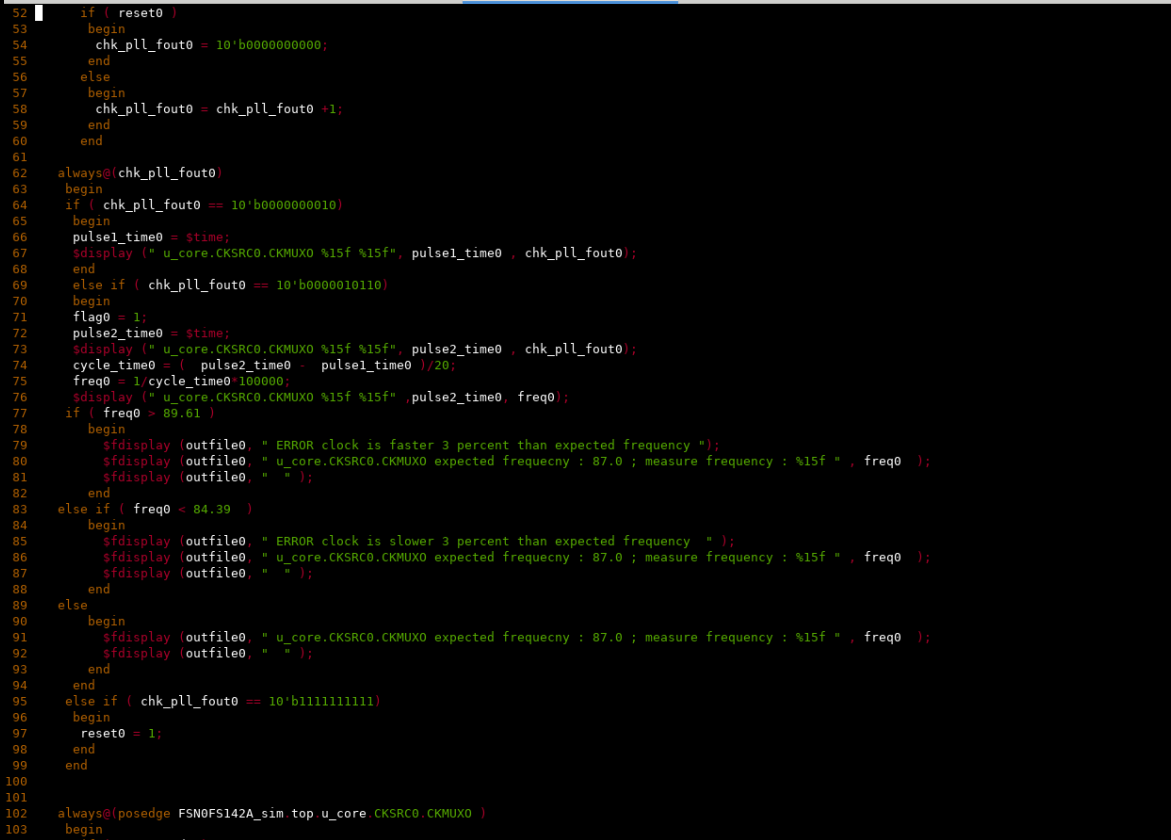
+ RESEQ => use



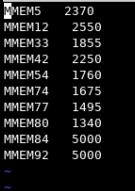
File .vt (.rom) => use ftlutil & ftl2ver



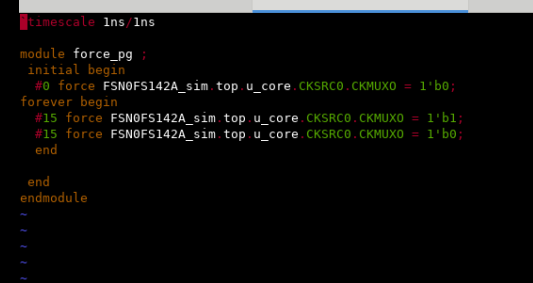
File dco\_checker

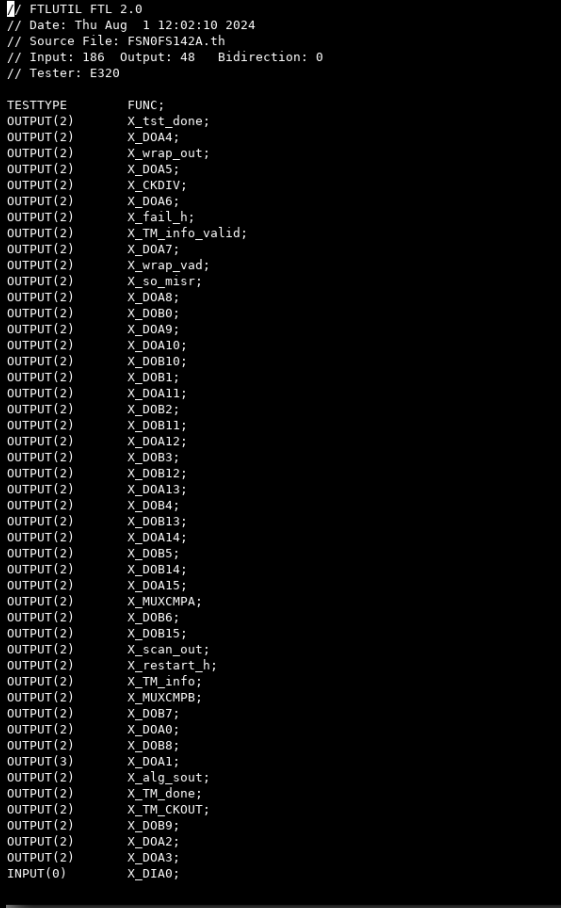
Period

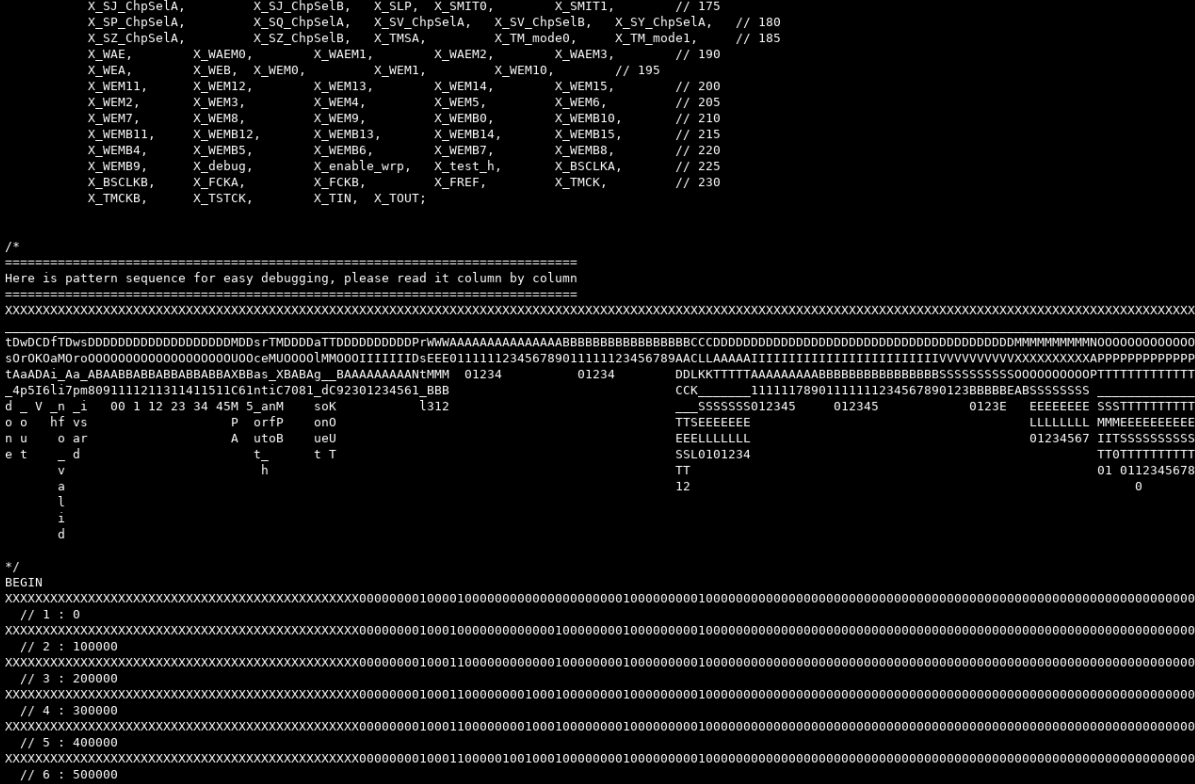


Force.v

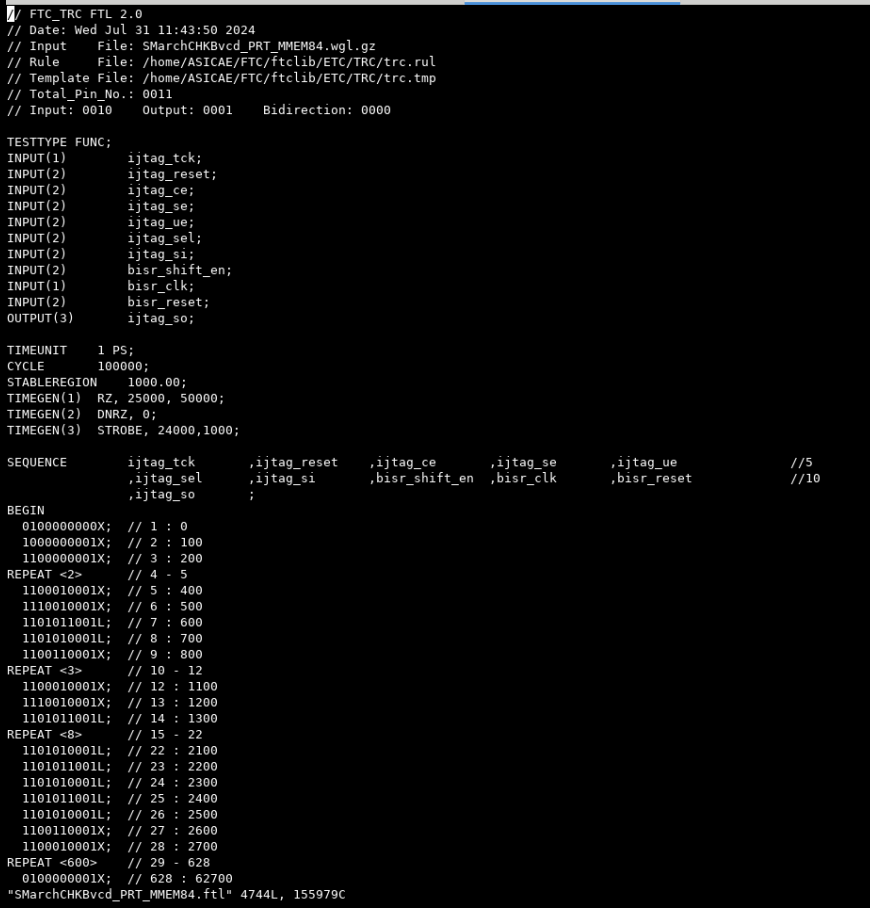


File tmp.ftl

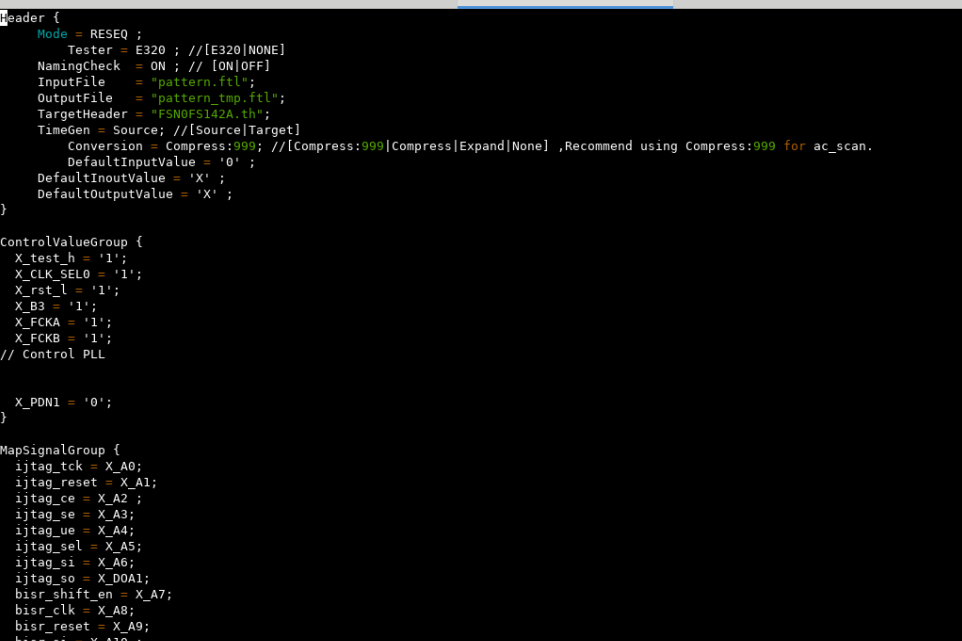




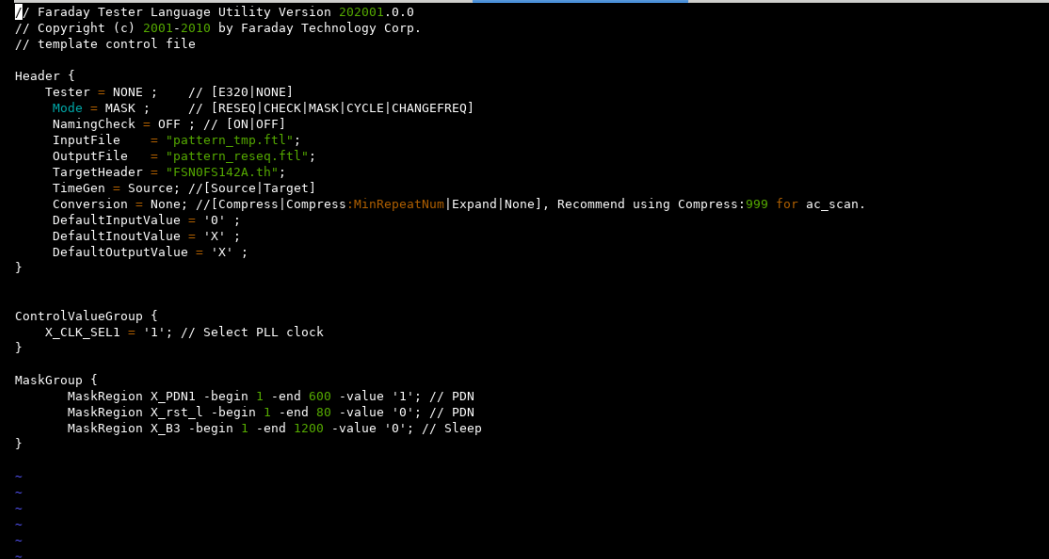
Filoe ftl pure



File 00\_



File pll\_



File resq\_ftl

