|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name |  | No. |  | Div/Dept | DSD/ACD/ACT | Job  Date：2024/03/29  Title | Intern |
| Please tick  the period | First Month | □W1 🗹W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 □W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2024, below are a brief description of the tasks and what I learned: |
| 2. What are the problems encountered this week? Any actions taken? Any help needed? |
| 3. What are the tasks for next week? Any preparation needed in advance? |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
|  | (Signature/Date) | (Signature/Date) |

-Generate DCO\_config

\*.config to \*.ftlcon format

=> 4 folder ~ 4 corner => ftlcon format

-Summarize data

+Pattern spec for each corner

**Output:** FSN0FS142A \_MBIST\_PAT\_config.csv

FSN0FS142A\_pt/pattern\_spec\_sign\_off\_FSN0FS142A

-Gen pattern

+ mbist\_pattern\_gen.dof

**Ouput:** PAT\_GEN\_tsdb\_outdir/patterns/ FSN0FS142A\_gate.patterns\_signoff/.\*wgl.gz

- Resequence patterns

+Gen FTL file: Convert .wgl.gz patterns to .ftl patterns

*Use ftrc to generate .ftl pattern and and detect violations against the rules of testers*

*Rename the ParallelRetentionTest in to PRT to run ftrc*

+Reseq pattern: use fpad to to generate the pad file information for the test and simulation flow.

=> <DESIGN>.pad :Pad cell information of the design

<DESIGN.>.th: A template of the FTL header file

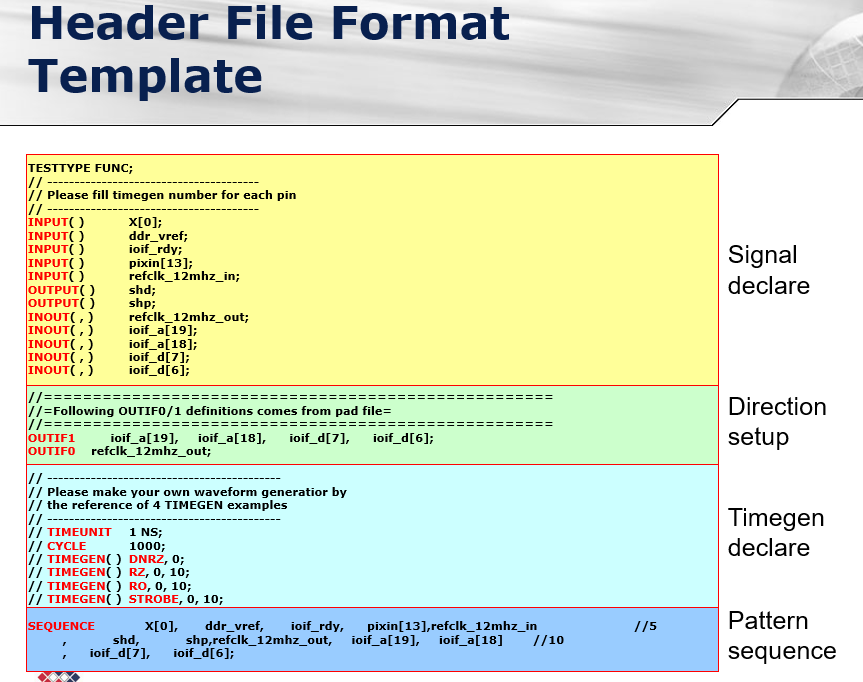
**Output: .ftl (patterns), .tmd (options for ftrc), .tlg (log files)**

FTRC (Faraday Test Rule Check)

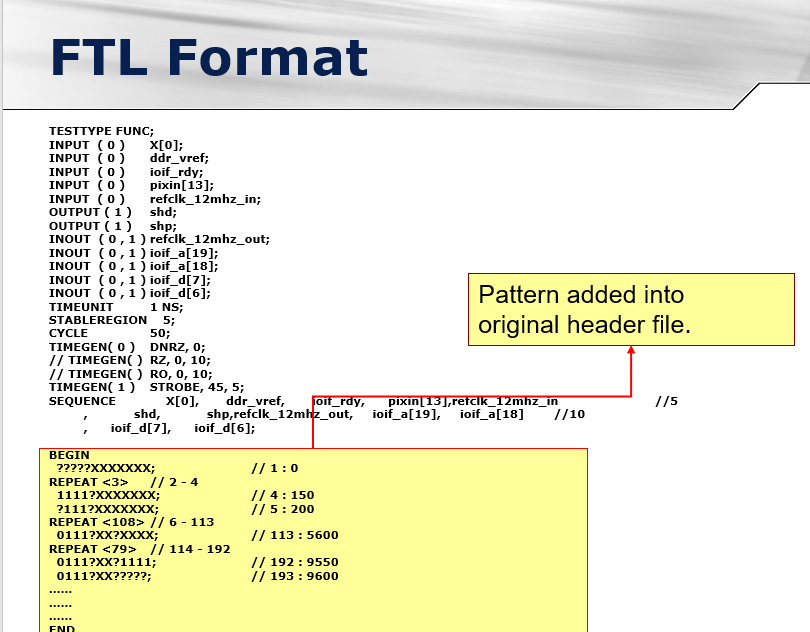
+Gen pattern: FTL gen

*PLL\_control\_file\_sample.cmd*

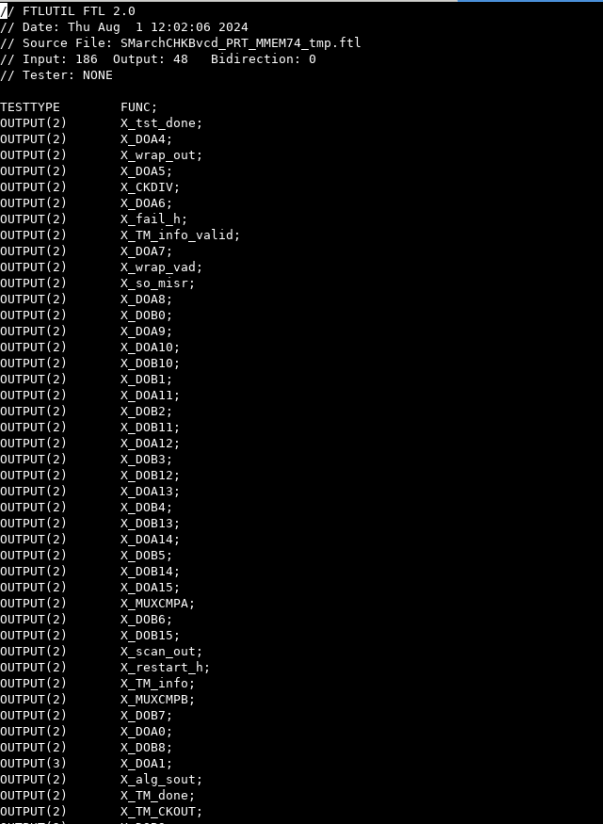
*00\_reseq\_mbist\_at\_speed\_sample.cmd*



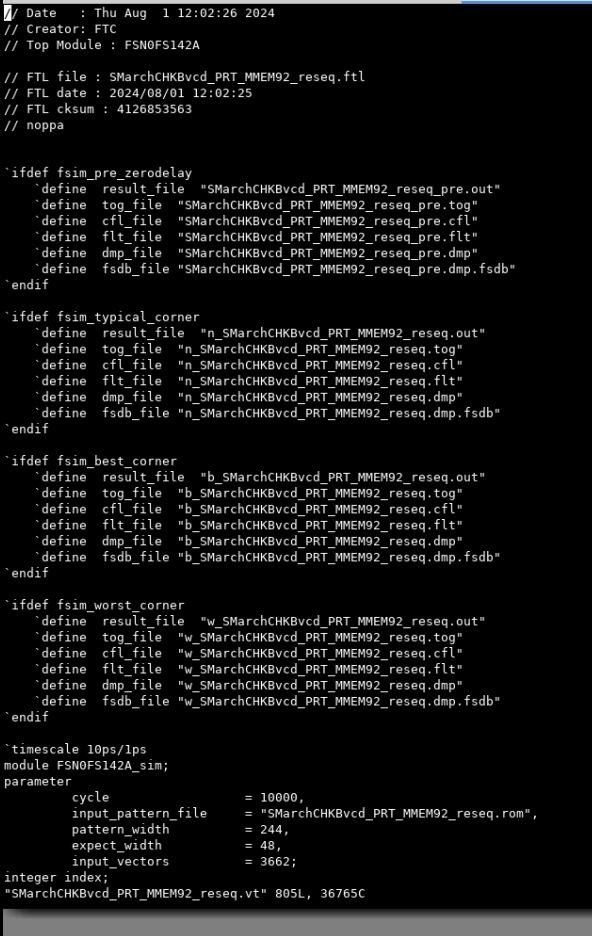
Use (header file ?) ftrc => .ftl



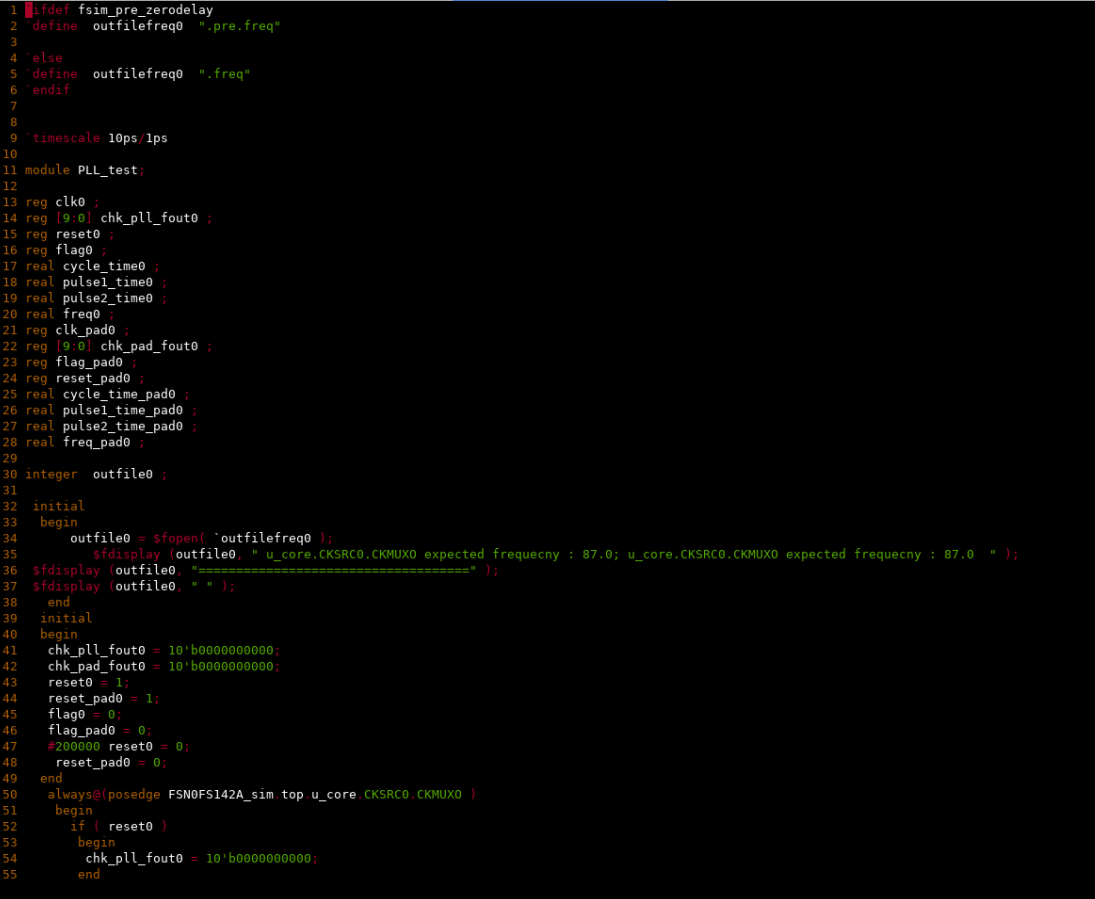
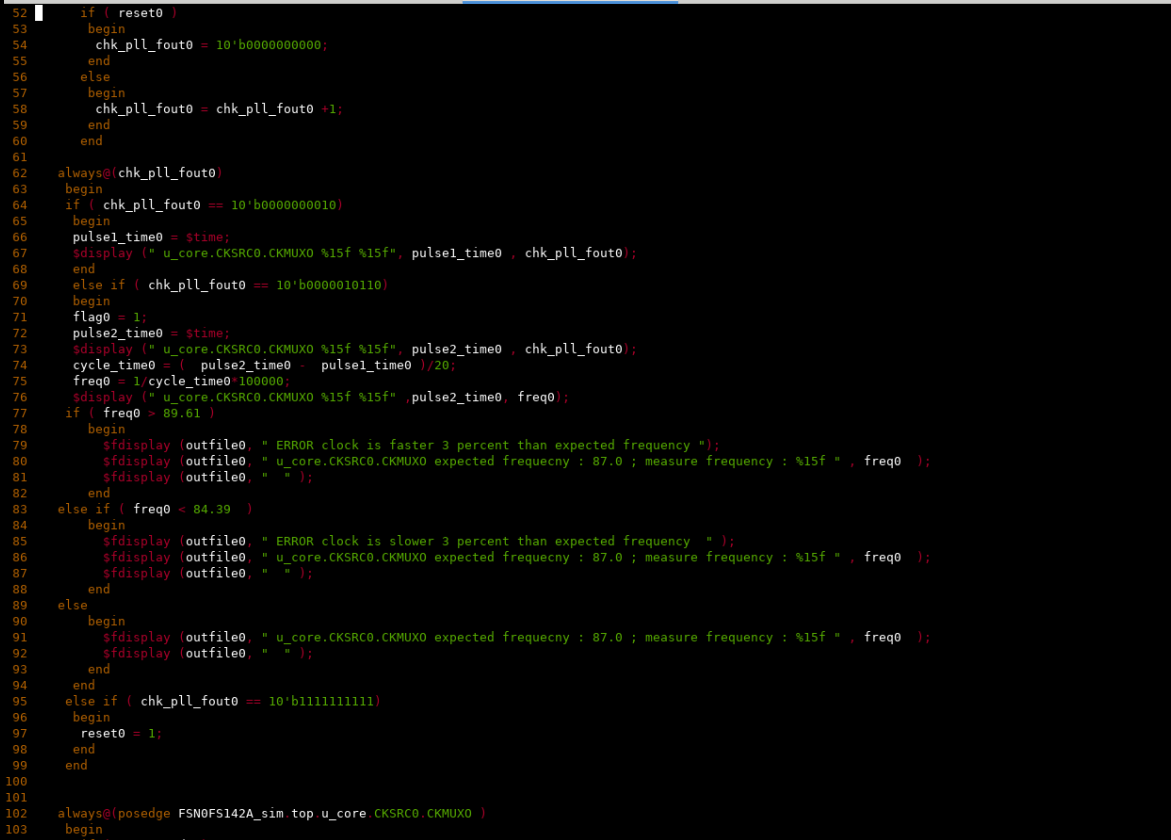
+ RESEQ => use



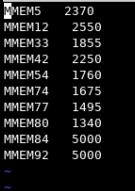
File .vt (.rom) => use ftlutil & ftl2ver



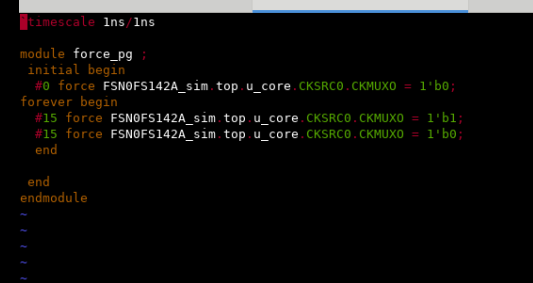
File dco\_checker

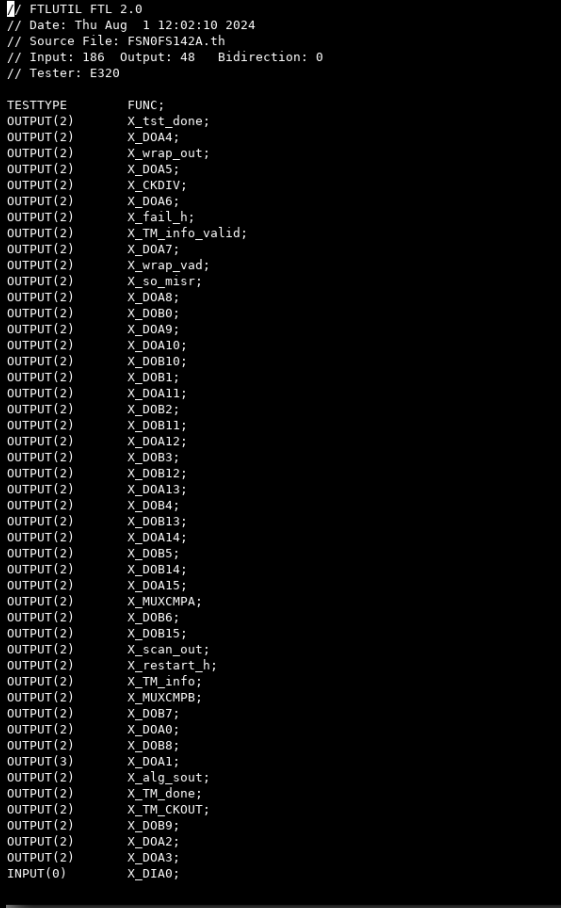
Period

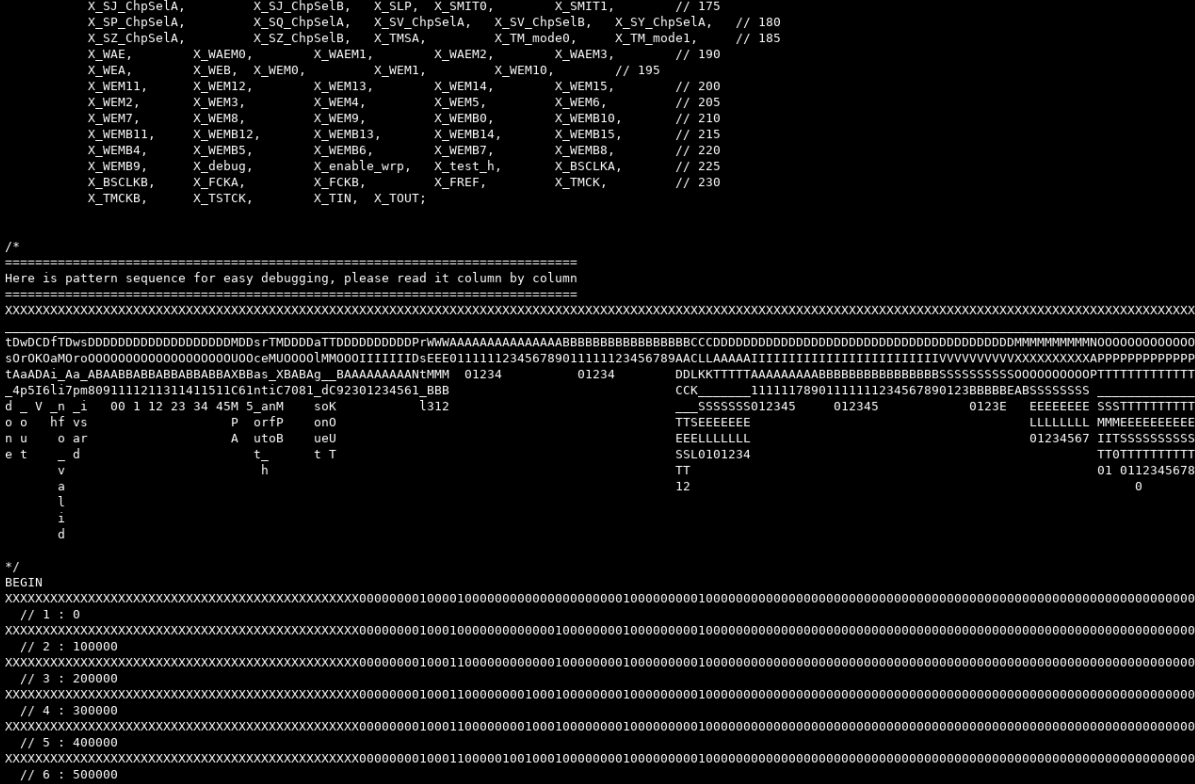


Force.v

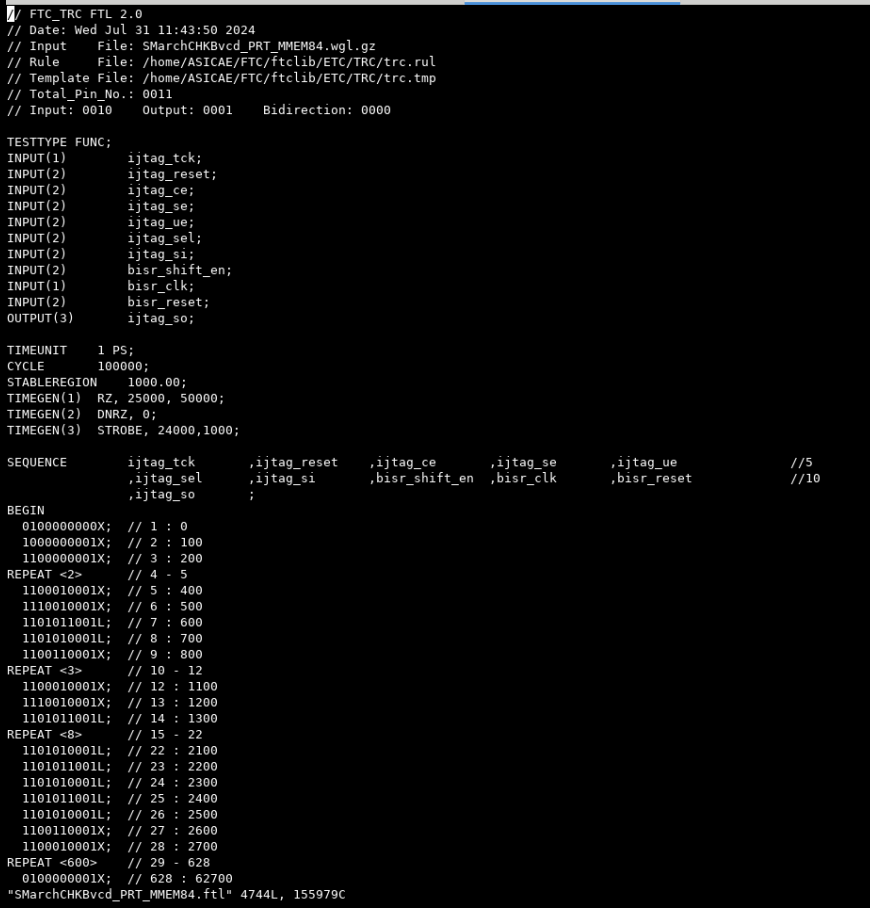


File tmp.ftl

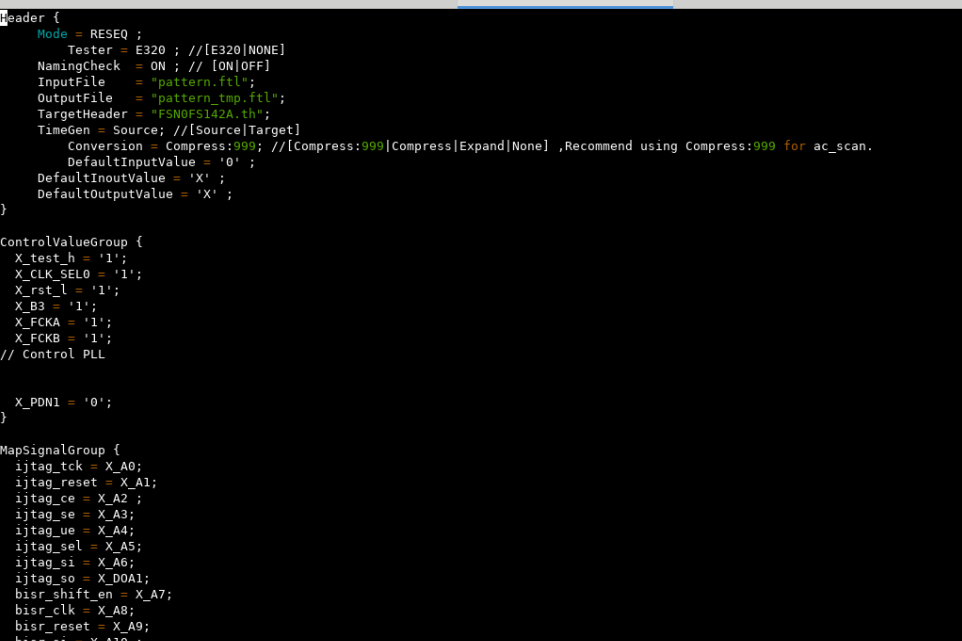




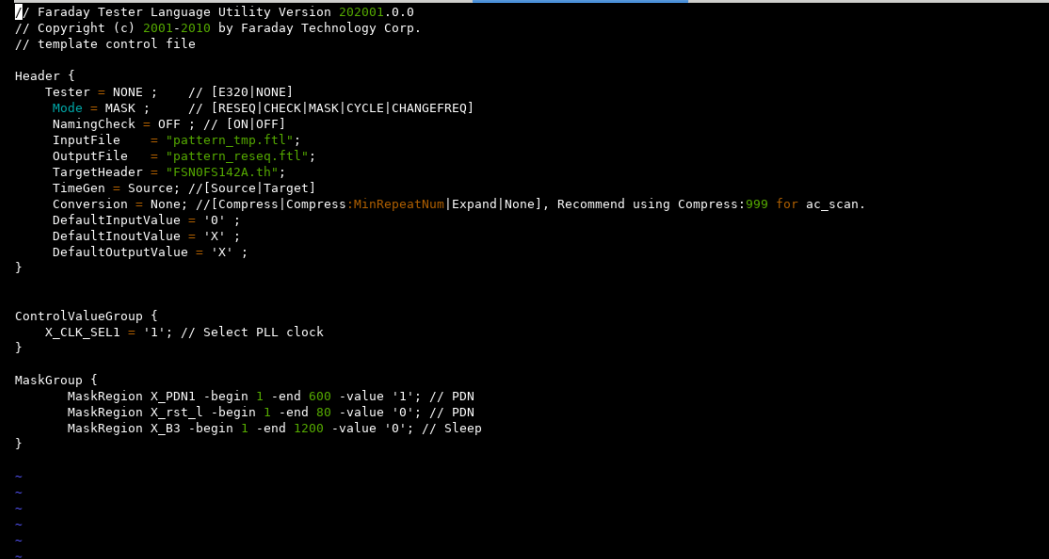
Filoe ftl pure



File 00\_



File pll\_



File resq\_ftl

