|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Ta Minh Trung | No. | T066 | Div/Dept | DSD/ACD/ACT1 | Job  Date：2023/05/05  Title | Intern |
| Please tick  the period | First Month | □W1 □W2 □W3 □ W4 | | | | | |
| Second Month | □ W1 □W2 □W3 🗹W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

|  |
| --- |
| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this sixth week are based on the training plan of 2023, below are a brief description of the tasks and what I learned:   1. Doing midterm-report:  * Task: Presentation Midterm-report * Achievement: Revision about knowledge through 7 weeks  1. Practice about MBIST  * Task : reading basic about MBIST concept and try to MBIST implement * Achivement : Know the usuage of MBIST   . |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * + - Not yet |
| 3. What are the tasks for next week? Any preparation needed in advance?  \_FSN0FS118A MEM Test-chip (continue) |
|  |

|  |  |  |
| --- | --- | --- |
| Name  (Date) | Mentor | Direct Supervisor |
| Ta Minh Trung (2023/05/17) | (Signature/Date) | (Signature/Date) |

【Note】

1. Please include your afterthought on this week’s training lectures.
2. At the end of each report, Manager is to indicate review completion in the blank space.

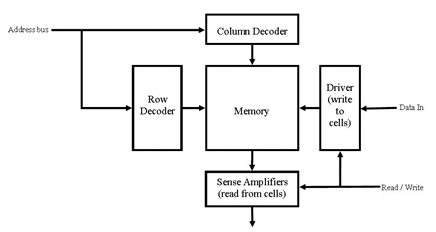
### CHAPTER1: MBIST (Memory Built-in Self-test)

BIST: is a design-for-testability that places the testing functions physically with the circuit under test

The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a comparator and a test controller. The test pattern generator generates for the CUT

MBIST is a self-testing within the memory chip which tests the memories through an effective set of algorithms to detect possibly all the faults. The self-test circuit is designed to write a test pattern to the memory, read it back, and compare the results with the expected results

**Basic memory model :**



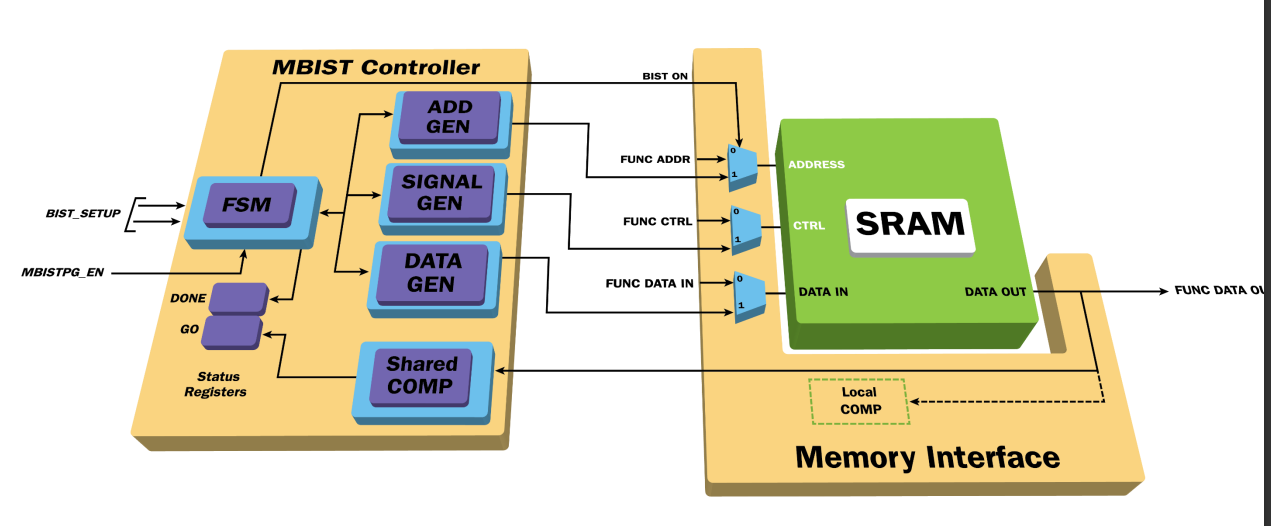
An architecture of a memory model constitutes of an array of memory cells. The array of memory cells are in the two-dimensional form. A full address is fed to memory through an address bus to row decoder and a column decoder.

The Read or Write enable signal is passed to the special circuitry to perform the memory operations.

**Fault Models in the memory cell array in Memory Testing:**

* Stuck-At fault: Here there can be two faults, a stuck at 1 fault and a stuck at 0 fault
* Transition fault: Here there can be two faults, a rising transient fault, and a falling transient fault
* Coupling fault: are three kinds of coupling faults but commonly fault occurs when one cell transition leads to a faults of other cell content.
* Address decoder faults: Row and column decoder comprises the address decoder of a memory. Four types of faults are considered in address decoder.

**Architecture of MBIST:**

****

**FSM of MBIST controller:** generates control signals based on the MBIST operation by controlling the memory operation mode. Also, these control signals drive address and data generator and a write/read signal

**The memory:** will operate in 2 nodes

1. Function mode
2. Test mode

Mux is used to select the inputs based on the BIST on. In function mode, the mux select the address and data sent by the processor .In test mode, the mux select address, write/read signal, data

**Data generator**: generate the data for memory to perform a write operation

Address generator: generate an address for memory to access the cell for performing read/write operations

**A comparator:** check the data read from the memory during a read operation with the golden data .If there are different – fault

**Advantages of MBIST:**

* It allows for robust testing of memories
* Lesser test cost
* Reduced test time
* All the memories of the design can be tested in parallel

**Disadvantage of MBIST:**

* Increase in area. However, this increase in area is very small as comparison to the benefits it provides

**BISR** stands for Built-In Self-Repair, which is a technique used in Memory Built-In Self-Test (MBIST) to automatically identify and repair faults or defects in the memory array. The memory repair feature diverts faulty areas of memories (e.g. row, column or both) by spare or redundant rows and columns available

# Chapter2: TESTCHIP FSN0FS118A WITH MBIST INSERTION

|  |  |  |  |
| --- | --- | --- | --- |
| **Stage (Phase)** | **Process (sub-tasks)** | | **TC (MEM)** |
| Data-in check | FLRE | | Yes |
| FERC | | Yes |
| FTCV | | Yes |
| FSTAH | | Yes |
| MBIST Insertion | Compile standard lib | | Yes |
| Mbist\_pre.cmd | | Yes |
| Mbist\_insertion.cmd | | Yes |
| Mbist\_post.cmd | | Yes |
| Fix\_assign | | Yes |
| Eco.cmd | | No |
| Modify\_SDC | | No |
| Pre-layout (Post-DFT) data check | FSTA (Gen environment) | | No |
| FSTA (Run – pre) | | No |
| FLEC | | No |
| FERC | | No |
| Pre sim | Gen pattern | | No |
| Fsim | SSA | No |
| OCC | No |
| MBIST | No |
| Post-layout data check | Fsta (run post) | | No |
| Flec | | No |
| Flre | | No |
| Ferc | | No |
| ACCHK1/2 |  | | No (skipped) |
| Post-sim | Fsim | | No |

**Data-in check** of FSN0FS118A by FLRE,FERC,FTCV,FSTAH have been done

Flre: /home/ftv\_training/AC\_training/Intern\_Mar\_2023/Eric\_Ta/FSN0FS118A/FE/Pre\_Sim/flre

Ferc: /home/ftv\_training/AC\_training/Intern\_Mar\_2023/Eric\_Ta/FSN0FS118A/FE/Pre\_Sim/ferc

Ftcv,Fstah: /home/ftv\_training/AC\_training/Intern\_Mar\_2023/Eric\_Ta/FSN0FS118A/FE/Fsta/Pre\_STA

**MBIST Insertion:**

1. **Compile standard library to tessent library:**

Purpose: To convert standard cell library to Tessent cell library

|  |  |  |
| --- | --- | --- |
| Input |  | libcomp.do.default |
| Runfile: |  | run\_libcomp |
| Ouput: |  | libcomp.atpglib |

1. **Mbist insertion:**

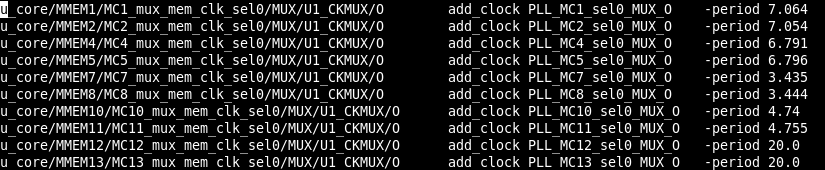
Purpose: To insert MBIST logic into pure netlist

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Input |  | mbist\_insertion.dof | Default |  |  |
|  |  | go\_make\_add\_clock.csh | Default |  |  |
|  |  | <Project>\_PLL\_src.lis | RD |  | | |  |  |
|  |  | Instance\_need\_MBIST.dof | Default |  | | |  |  |
|  |  | func\_debug | Default |  | | |  |  |
|  |  | .synnosyp\_dc.setup | Default |  | | |  |  |
|  |  | rom\_content.dof | Create |  | | |  |  |
|  |  | mem.list | Create |  | | |  |  |
|  |  | register\_tdr.dof | Create |  | | |  |  |
|  |  | add\_clock.dof  <Project>\_MBIST\_inst.lis | Create  RD |  | | |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Run file:** |  | run\_mbist.csh |  |  |  | # Execution script |

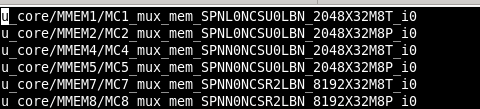
**<Project>\_PLL\_src.lis**

|  |
| --- |
| # PLL clock source list for memories |



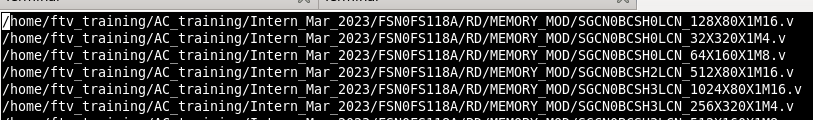
**<Project>\_MBIST\_inst.lis**

|  |
| --- |
| # MEM instances need MBIST |



**mem.list**

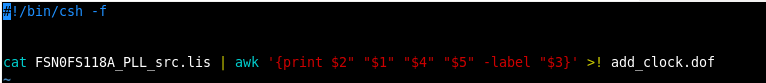
# memories list path



ls -a1 /home/ftv\_training/AC\_training/Intern\_Mar\_2023/FSN0FS118A/RD/MEMORY\_MOD/\*.v > mem.list

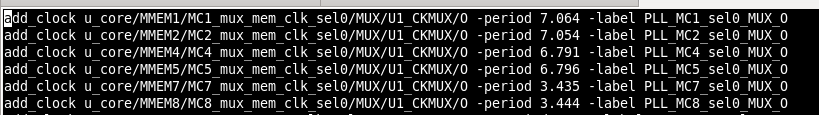
**go\_make\_add\_clock.csh**

# Script to extract clock period

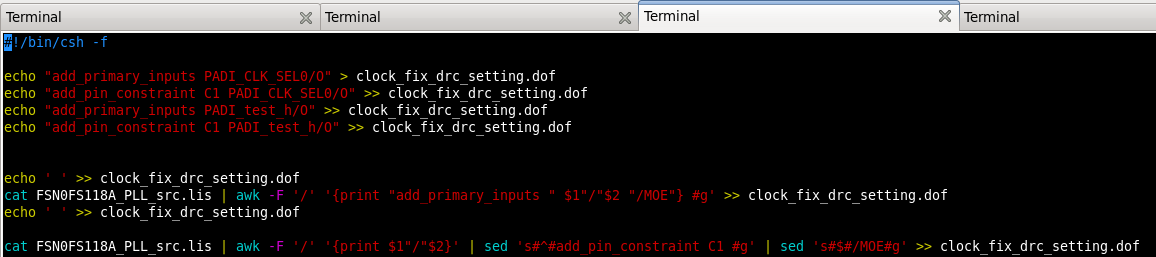
****

**add\_clock.dof**

# Clock period file

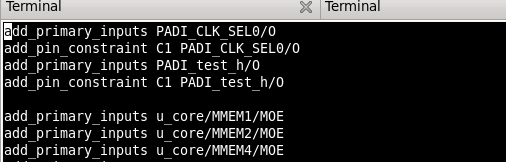


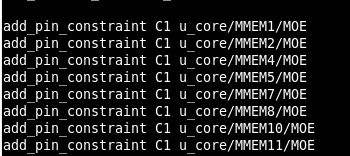
**go\_make\_clock\_fix\_drc\_setting.csh (scripts)**



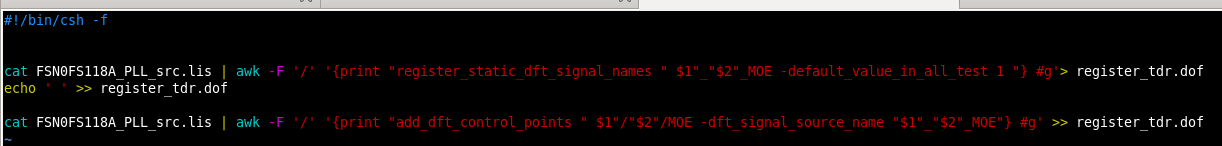
clock\_fix\_drc\_setting.dof

## Add all memory primary input in this file set pin constraint



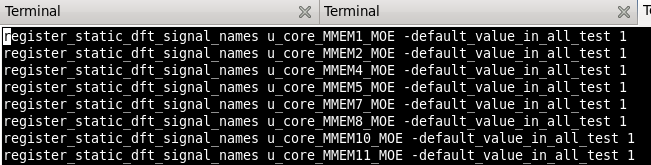


**go\_make\_register\_tdr.csh (scripts)**

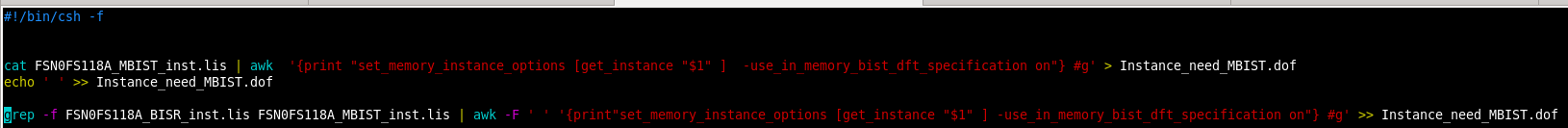
****

**register\_tdr.dof**

# set static register static dft signal

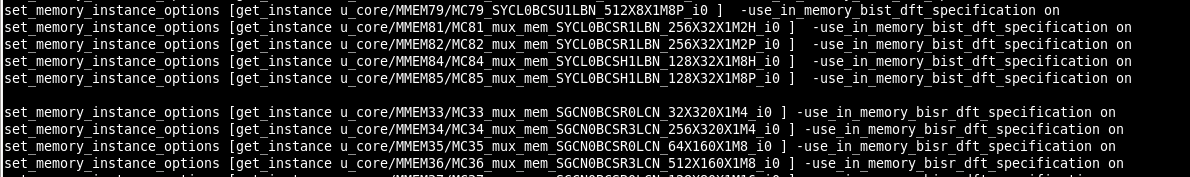
****

**go\_make\_Instance\_need\_MBIST.csh**

****

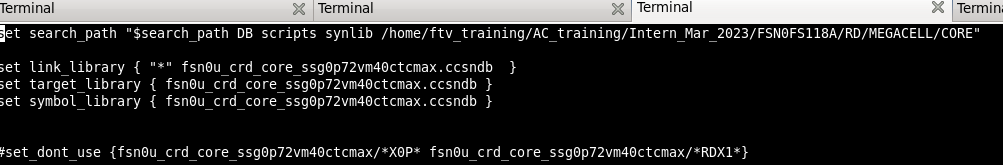
**Instance\_need\_MBIST.dof**

# Set memories instance option for BIST and BISR

****

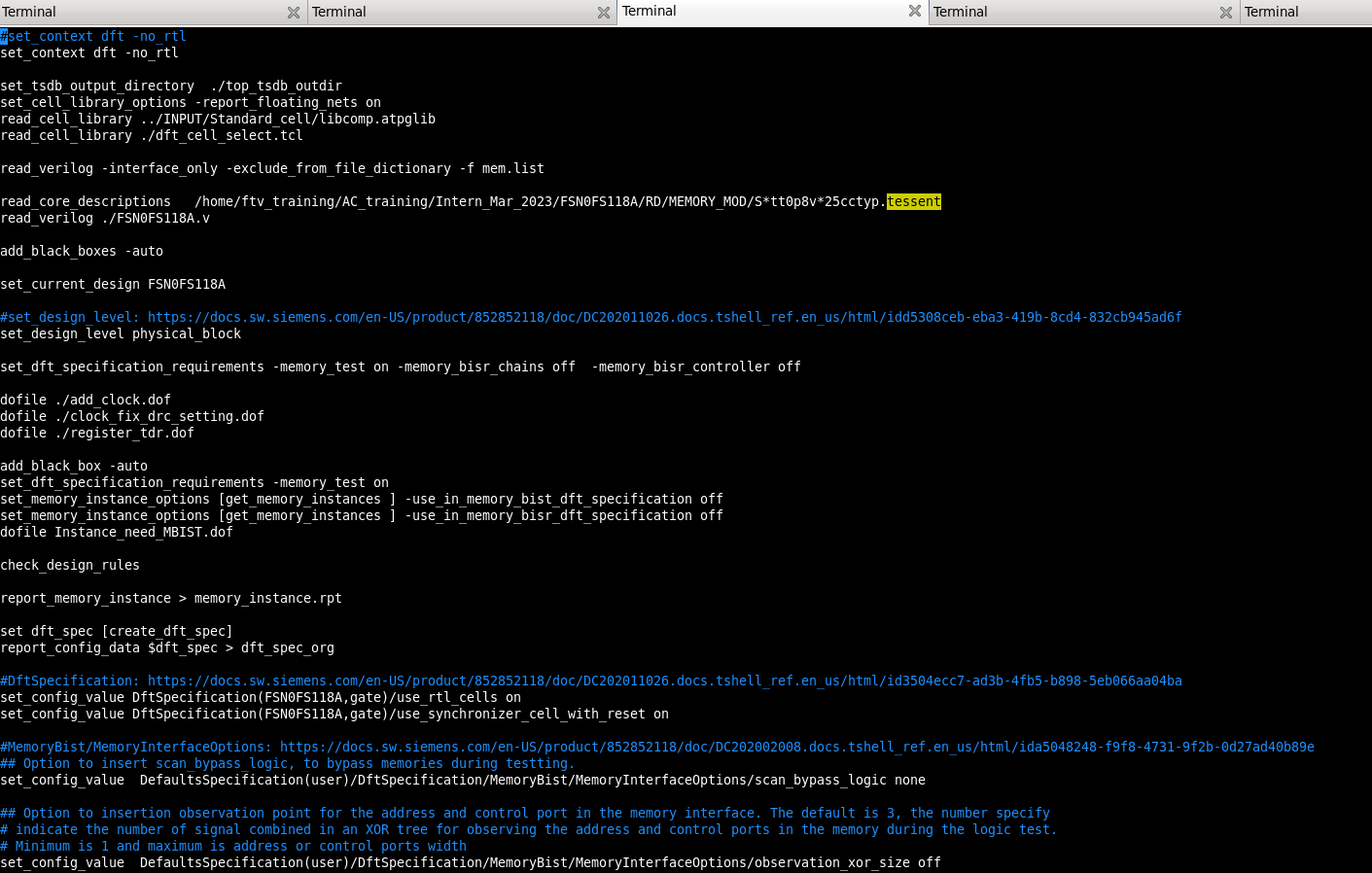
**.synnosyp\_dc.setup**

**# use WC or WCC library for synthesis**

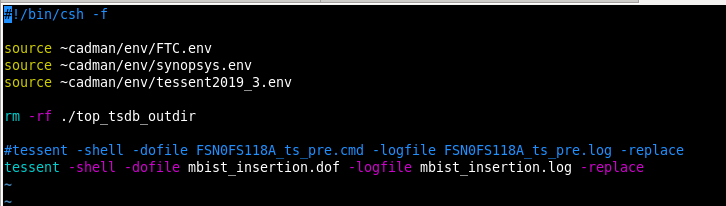
****

**mbist\_insertion.dof**

# Insert mbist circuit, could be modified based on feature of type and project



**run\_mbist.csh**



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Ouput: |  | |  |  |  |  |  | | --- | --- | --- | --- | --- | | FSN0FS118A.vg |  |  |  | # Post MBIST netlist | |