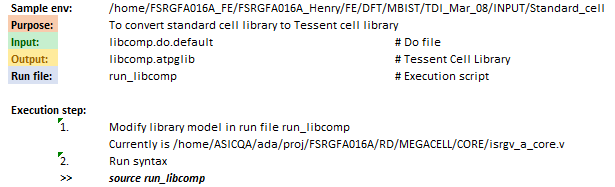
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Name | Vance Hang | No. | T161 | Div/Dept | DSD/ACD/ACT | Job  Date：2024/05/13  Title | Intern |
| Please tick  the period | First Month | □W1 □ W2 □W3 □W4 | | | | | |
| Second Month | □W1 □ W2 □W3 🗹W4 | | | | | |
| Third Month | □W1 □ W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

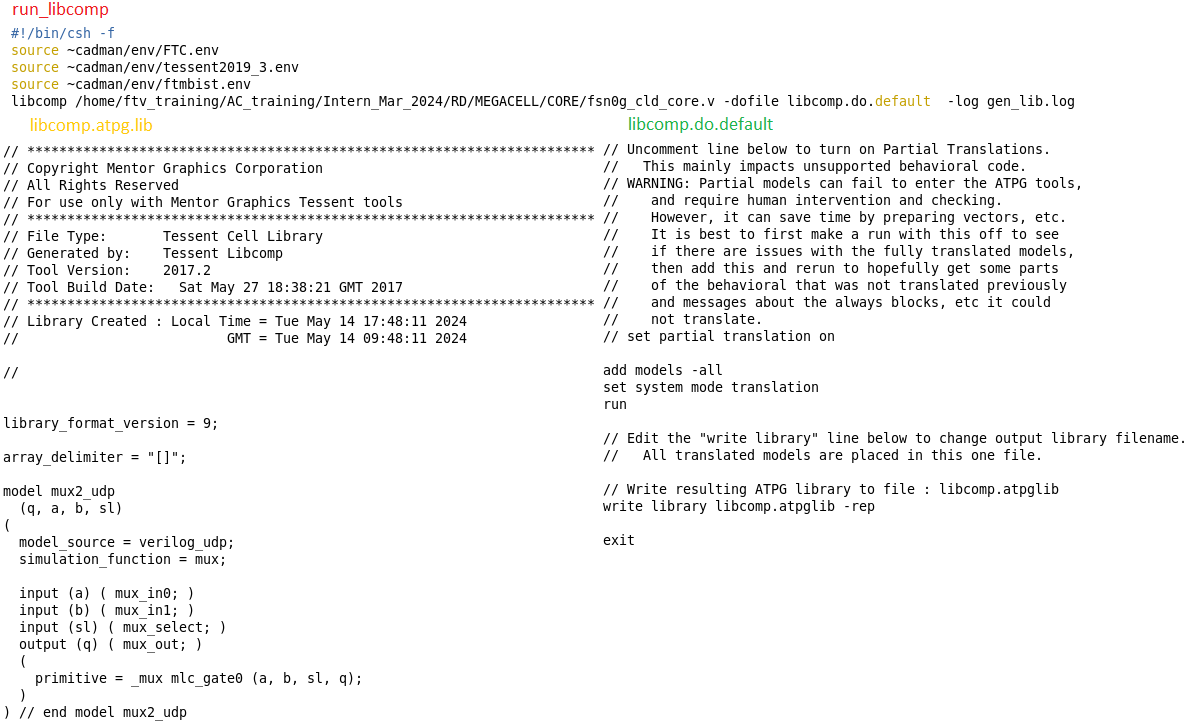
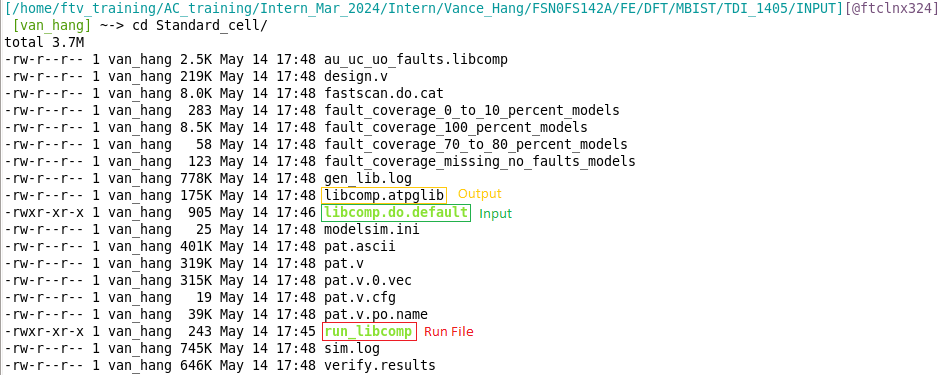
|  |  |  |
| --- | --- | --- |
| Work Experience Record | | |
| 1. Please describe the tasks and achievements you learned/executed :  All of the tasks I learned during this first week are based on the training plan of 2024, below are a brief description of the tasks and what I learned:   1. Run Sim | | |
| 2. What are the problems encountered this week? Any actions taken? Any help needed? | | |
| 3. What are the tasks for next week? Any preparation needed in advance? | | |
| Name  (Date) | Mentor | Direct Supervisor | |
| Vance Hang (2024/05/13) | Alden Duong (Signature/Date) | Xen Ha  (Signature/Date) | |

# MBIST

## Compile Standard library to Tessent library



/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Vance\_Hang/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/INPUT/Standard\_cell



## MBIST Insertion

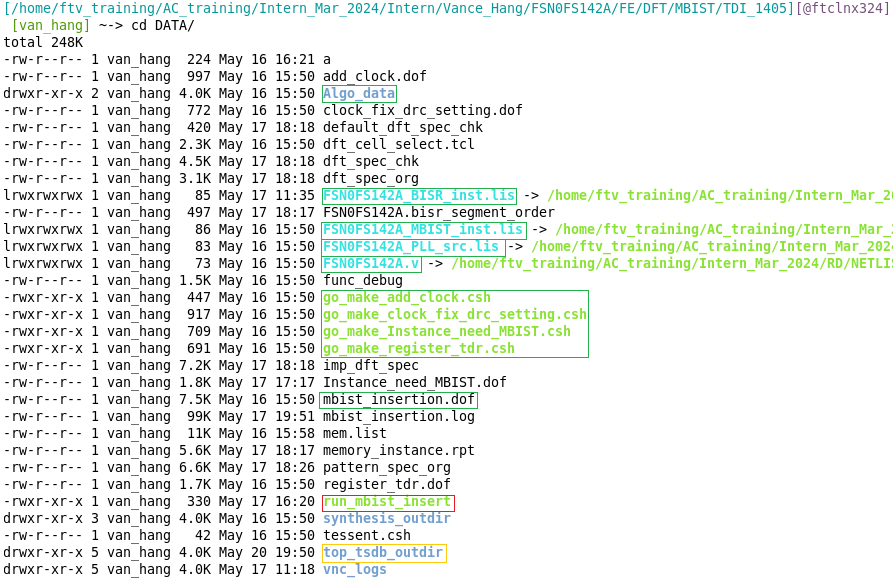
Purpose: To insert MBIST logic into pure logic

### <Proj>\_ts\_pre.cmd



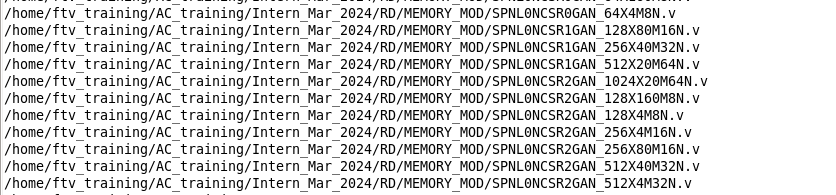
*/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Vance\_Hang/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/DATA*

### <Proj>\_insertion.dof



#### Step 1: Make memlist

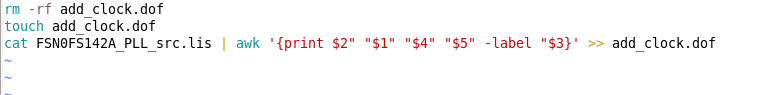
>> *ls –a1 /home/ftv\_training/AC\_training/Intern\_Mar\_2024/RD/MEMORY\_MOD/\*.v >! Mem.list*



**Out**: mem.list

#### Step 2: Make *add\_clock\_dof* file

>> *./go\_make\_add\_clock.csh*

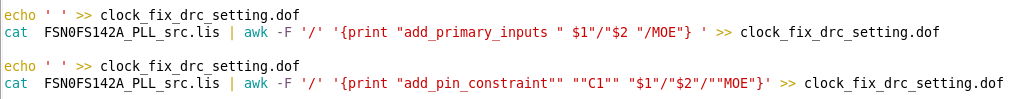


*add\_clock.dof*

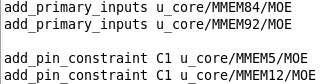


#### Step 3: Make ­*clock\_fix\_drc\_setting.dof* file

>> *./go\_make\_clock\_fix\_drc.csh*

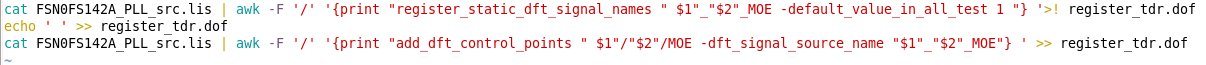


*clock\_fix\_drc\_setting.dof*

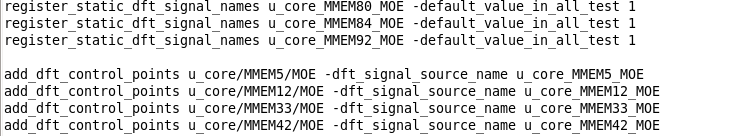


#### Step 4: Make *register\_tdr.dof* file

>> *./go\_make\_register\_tdr.dof*

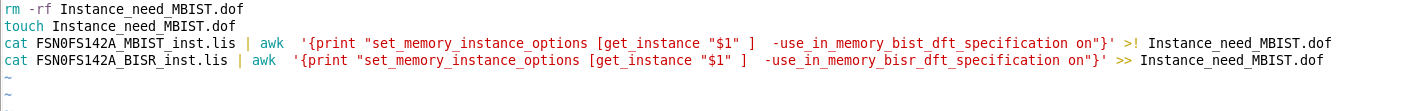


***register\_tdr.dof***

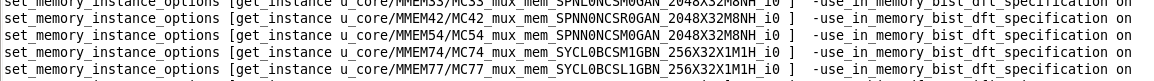


#### Step 5: Make *Instance\_need\_MBIST.dof* file

>> *./go\_make\_Instance\_need\_MBIST.dof*

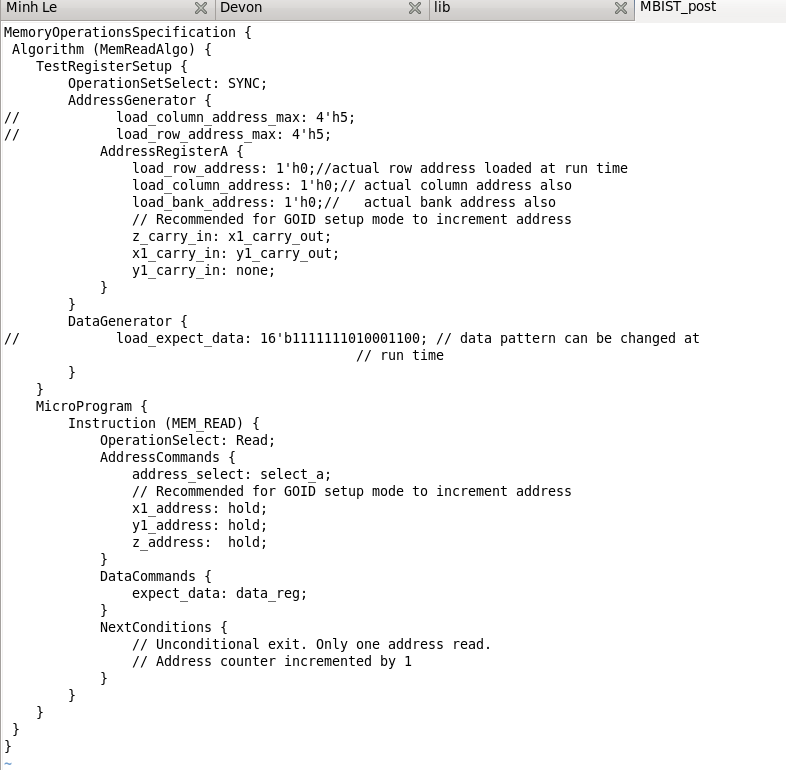
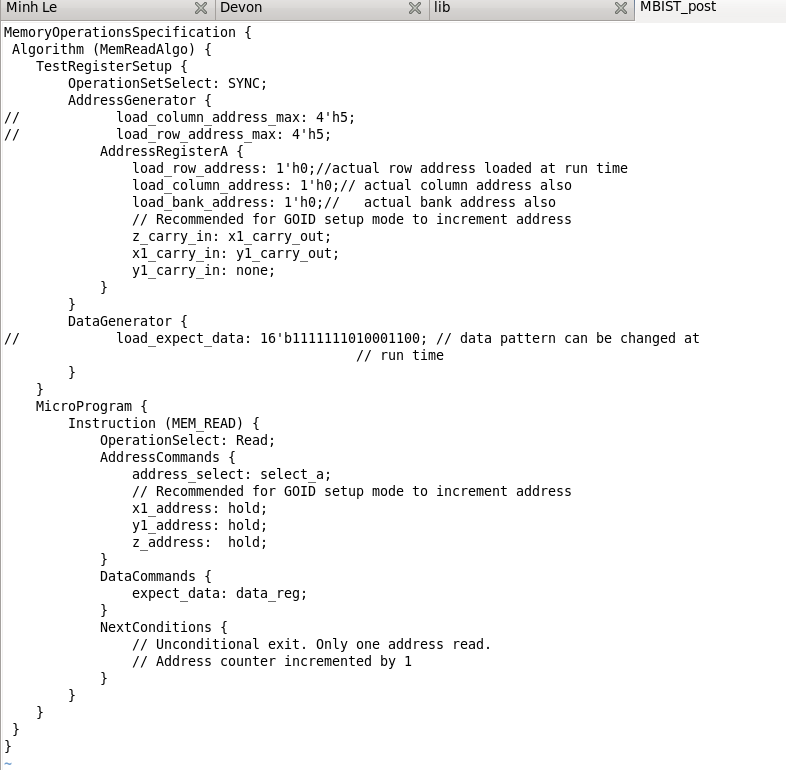


***Instance\_need\_MBIST.dof***

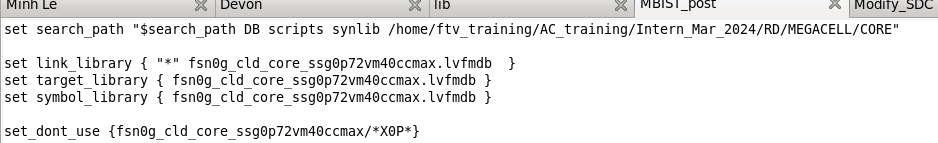


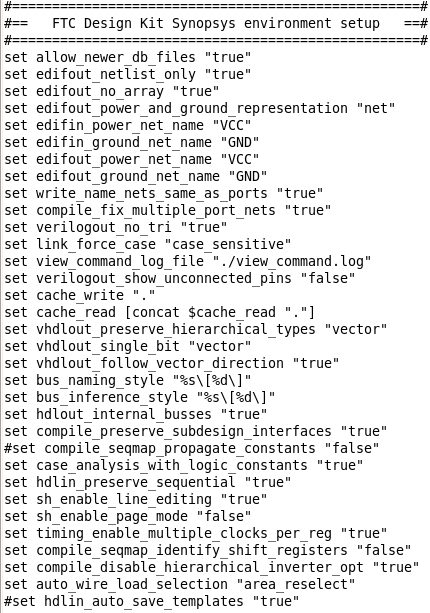
#### Step 6: Input some default files for synthesis

>> func\_debug

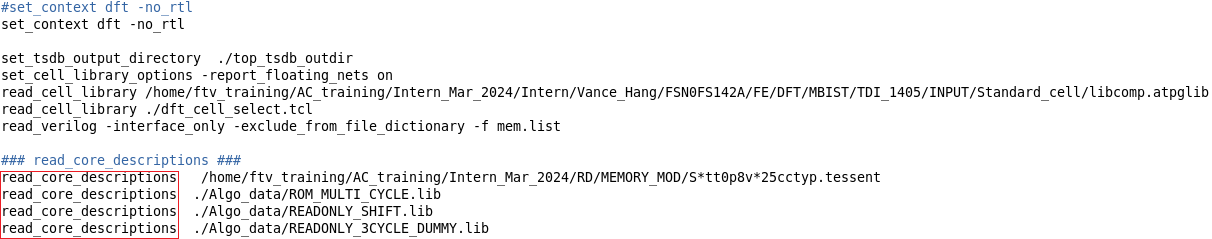


***./synopsys\_dc.setup***



#### Step 7: Prepare *mbist\_insertion.dof* file

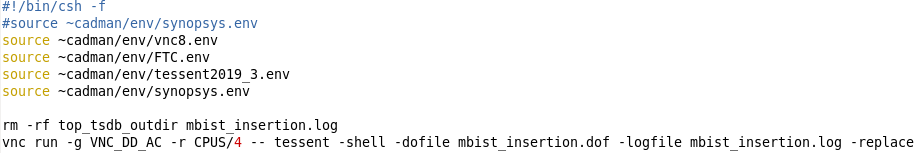








#### Step 8: Run the mbist insertion



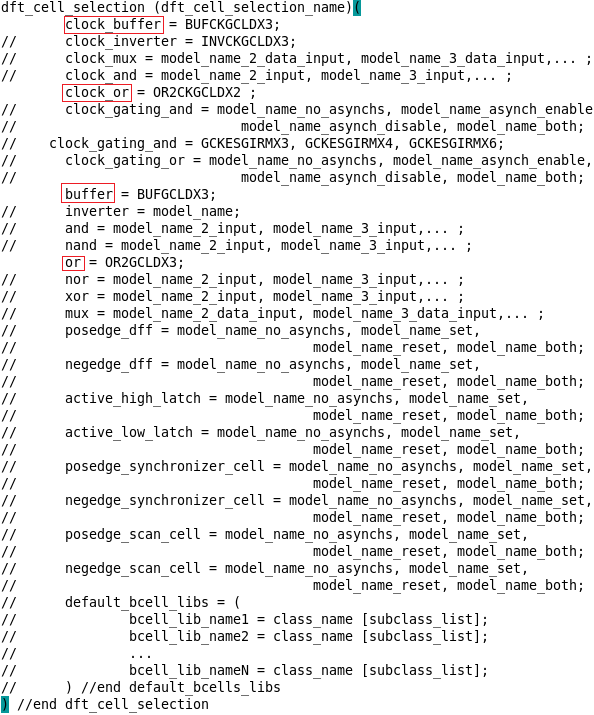
### <Proj>\_ts\_post.cmd

Purpose: Do file for post MBIST ECO

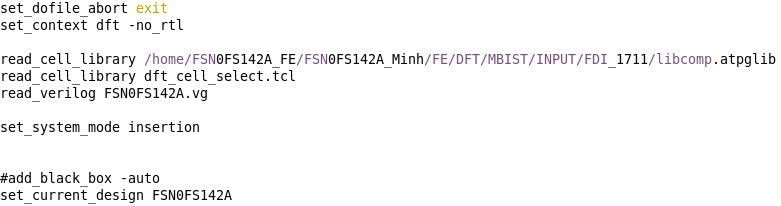
/home/ftv\_training/AC\_training/Intern\_Mar\_2024/Intern/Vance\_Hang/FSN0FS142A/FE/DFT/MBIST/TDI\_1405/MBIST\_post

#### Step 1: Prepare *dft\_cell\_select.tcl* file

Purpose: Define cell type for MBIST insertion, it can be modified for design intention

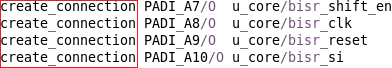


#### Step 2: Prepare *<Proj>\_ts\_post.cmd* file

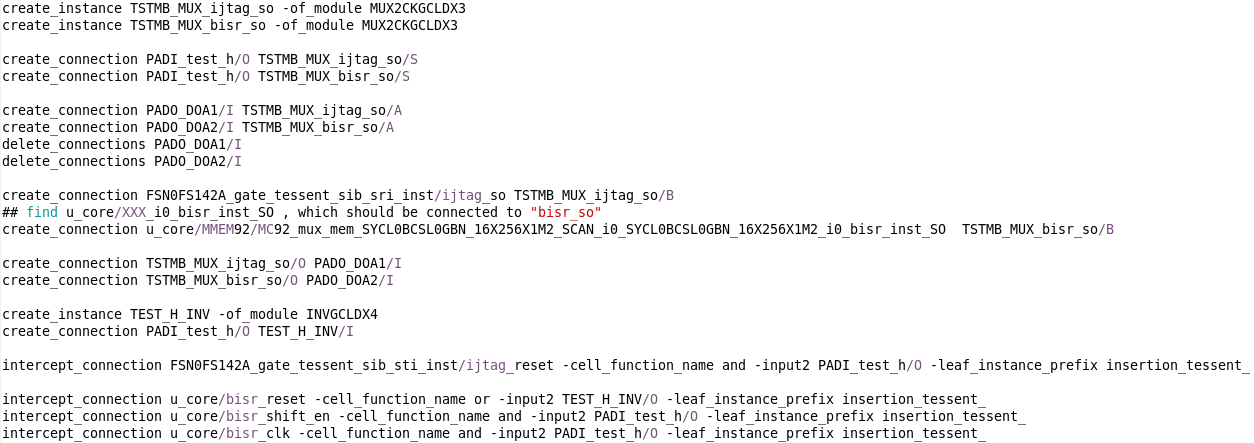


# Connect JTAG and BISR pin from module to port of chip

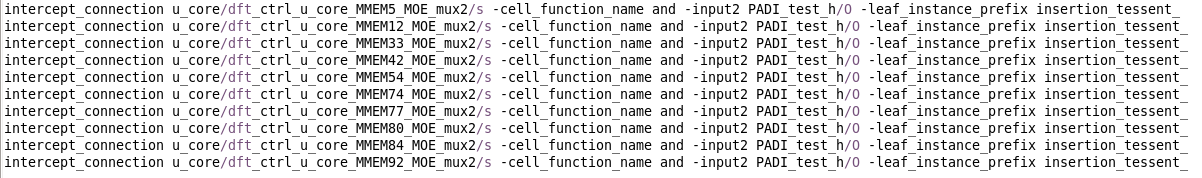




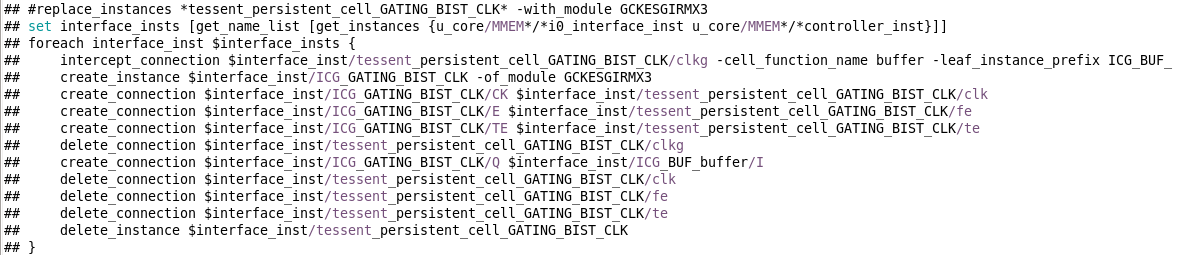




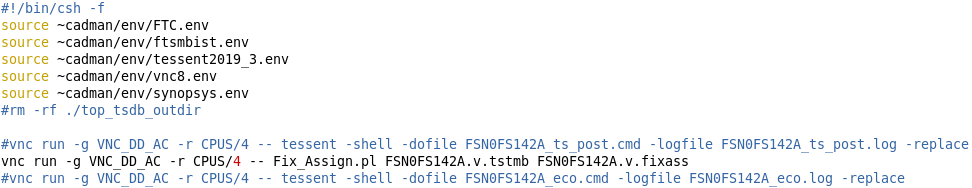
# Insert MUX to select MOE signal between DMA and MBIST mode (control signal is X\_test\_h)



# Replace gating cell by ICG to improve timing issue



#### Step 3: Run post MBIST ECO



## Modify SDC

### mbist\_tail.sdc

#### Step 1: Memory macro hierarchy setting

#### Step 2: set\_case\_analysis

#### Step 3: set\_disable\_clock\_gating\_check

#### Step 4: set\_false\_path

### user\_clk.sdc

#### Step 1: Memory macro hierarchy setting

#### Step 2: clock constrains

### <Proj>\_MBIST.sdc

#### Run modify\_sdc.csh

### MBIST\_expand.sdc

### <Proj>.sdc

### DFT\_size\_only.sdc

### dont\_touch\_only

# POST DFT DATA CHECK

# AC RELEASE DATA TO PI

# PRE SIMULATION

## Gen pattern

### Gen DCO config

#### Step 1: gen\_dco\_config.csh

#### Step 2: dco\_config.pl

### Summarize data

#### Step 1: Update info in sum\_mem\_info\_for PLL.pl

#### Step 2: Gen DB

#### Step 3: Gen PT

### Gen pattern

#### Step 1: make file mbist\_pattern\_gen.dof

#### Step 2: run\_gen\_pattern

### Resequence patterns

#### Step 1: Gen FTL file