컴퓨터공학 기초 실험2

Week #4 (Lab #5)

Traffic Light Controller with/without Left Turn Signals

Kwangwoon University
Embedded System Architecture Lab

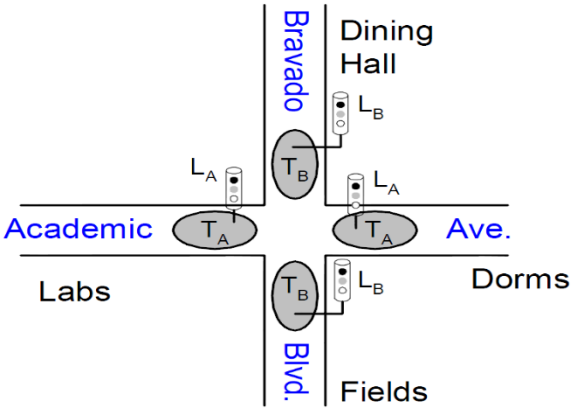
KWANGWOON UNIVERSITY

ESAL Embedded System Architecture Lab

TRAFFIC LIGHT CONTROLLER

Traffic Light Controller

- 신호등을 제어하는 logic을 구현
  - 신호등 L_A는 'Academic Ave.'의 차량 통행을 제어하는 신호등
  - L_B는 'Bravado Blvd.'의 차량 통행을 제어하는 신호등
  - 시간에 따라 변하는 신호등이 아닌 거리에 차량이 있을 때 신호등이 초록색이 되고, 없을 때는 빨간색이 된다.
  - 차량이 있음을 감지하기 위하여 'Academic Ave.'에 traffic sensor인 T_A를, 'Bravado Blvd.'에 traffic sensor인 T_B를 설치



Traffic Light Controller(Cont.)

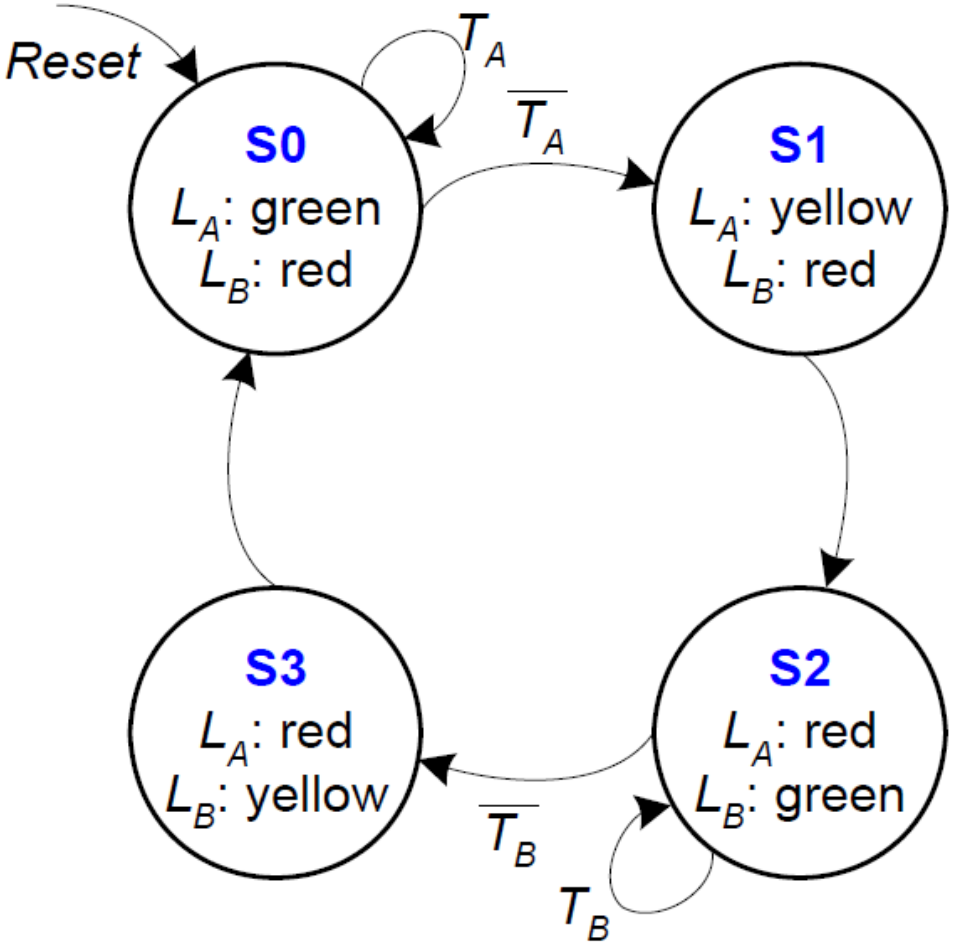
- 다음 규칙을 만족해야 한다.
  - Traffic light는 교통이 없을 때 초록색에서 노란색을 거쳐 빨간색으로 변한다.
  - 만약 traffic light L_A가 초록색이거나 노란색이면, traffic light L_B는 빨간색이다. 반대의 경우도 마찬가지이다.

Finite State Machine

- Design
  1. Drawing the finite state diagram
     - Define states
     - Define inputs
     - Define outputs
     - Draw the diagram
  2. Encoding states
  3. Coding the module header
  4. Coding state registers(flip-flops) – sequential circuits
  5. Coding combinational circuits

FSM State Transition Diagram

- Moore FSM: outputs labeled in each state
- States: Circles
- Transitions: Arcs



FSM Encoded State Transition Table

Current state		Inputs		Next state	
Q_1	Q_0	T_A	T_B	D_1	D_0
0	0	0	X	0	1
0	0	1	X	0	0
0	1	X	X	1	0
1	0	X	0	1	1
1	0	X	1	1	0
1	1	X	X	0	0

$$D_1 = Q_1 \oplus Q_0$$

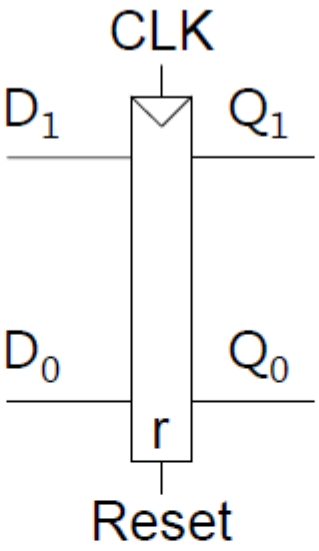
$$D_0 = \overline{Q}_1\overline{Q}_0\overline{T}_A + Q_1\overline{Q}_0T_B$$

FSM output table

Current state		Outputs			
Q_1	Q_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}
0	0	0	0	1	0
0	1	0	1	1	0
1	0	1	0	0	0
1	1	1	0	0	1

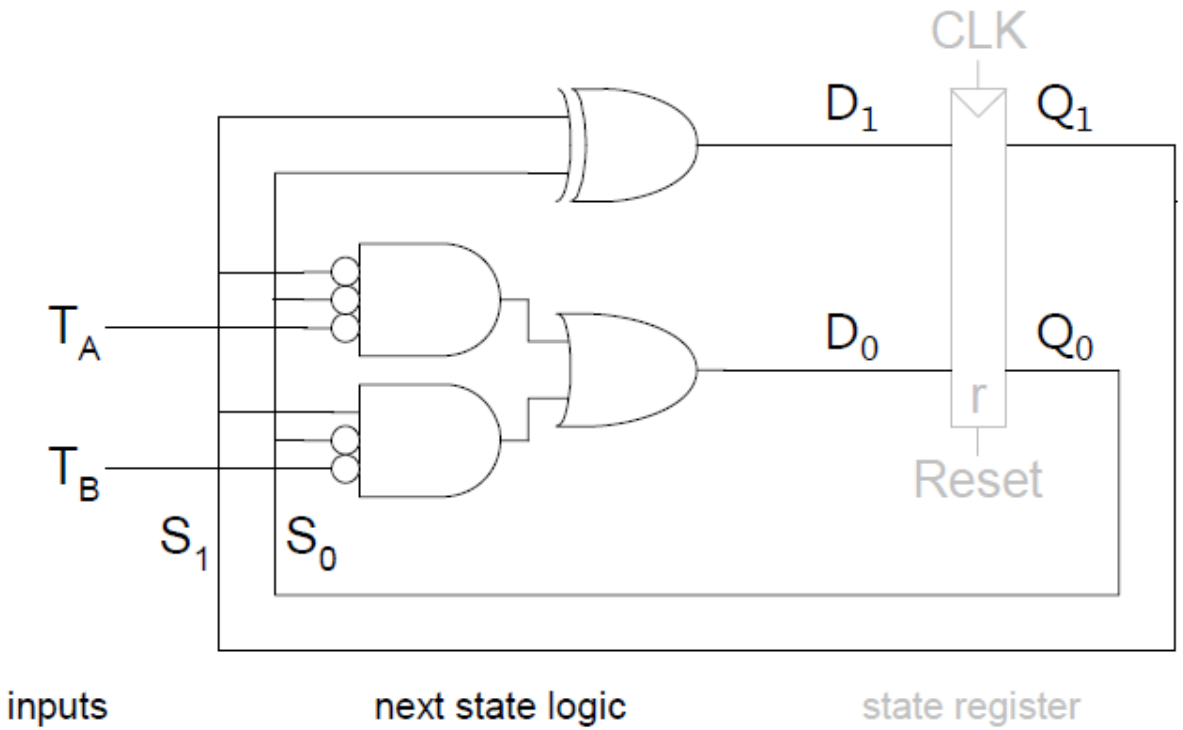
$$L_{A1} = Q_1$$
$$L_{A0} = \overline{Q}_1 Q_0$$
$$L_{B1} = \overline{Q}_1$$
$$L_{B0} = Q_1 Q_0$$

FSM Schematic: State Register

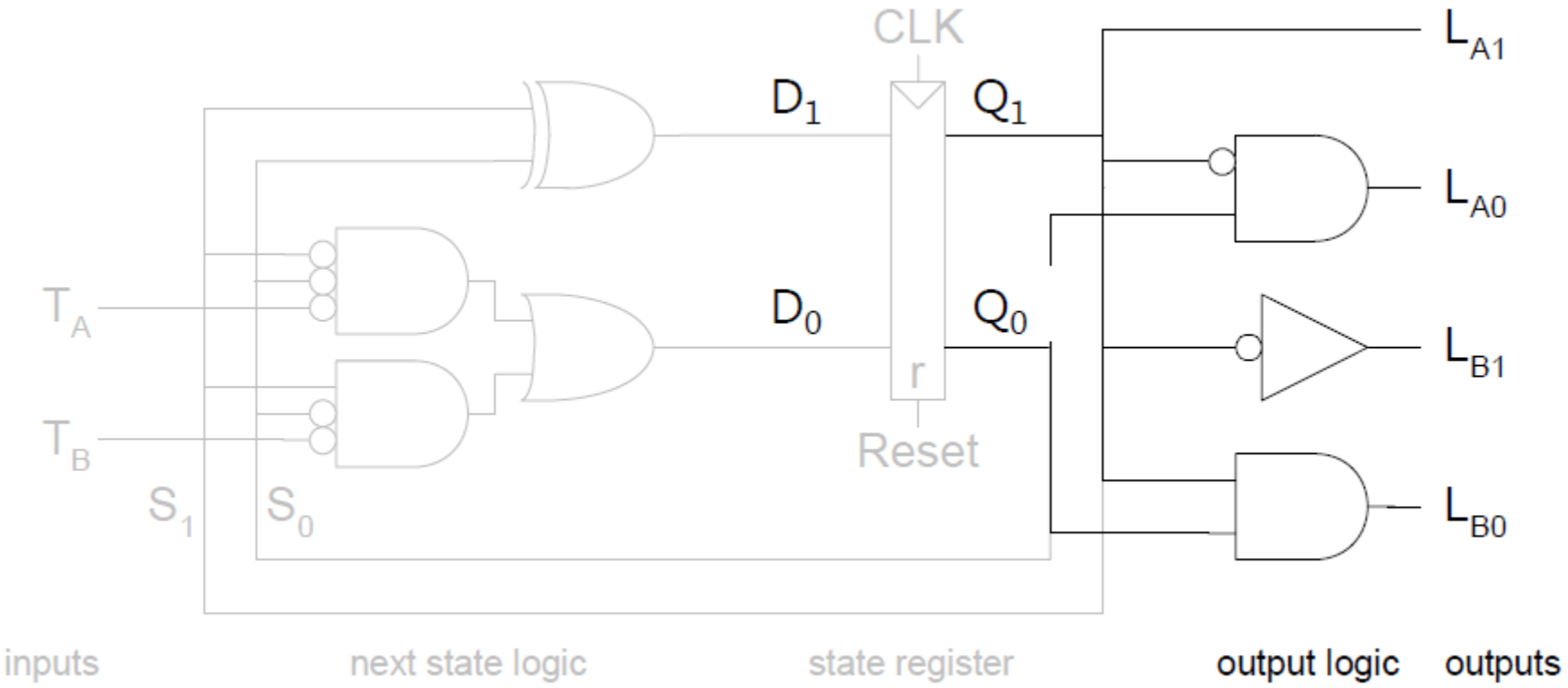


state register

FSM Schematic: Next State Logic



FSM Schematic: Output Logic



Traffic Light Controller(Cont.)

- Module configuration

구분	이름	설명
Top module	tl_cntr	Traffic light controller의 top module
Sub module	ns_logic	Traffic light controller의 next state를 결정하는 combinational logic
Sub module	_register2_r	2-bit resettable register with active low asynchronous reset module (내부에 d_ff_r_async를 instance) - 현재 state의 값을 저장하고 있다.
Sub module	_dff_r	Resettable D flip-flop with active low asynchronous reset
Sub module	o_logic	현재 state의 값에 기반하여 output 값을 결정하는 combinational logic

Traffic Light Controller(Cont.)

- I/O Configuration

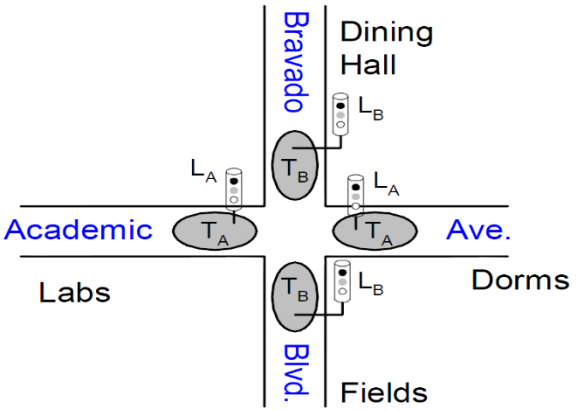
Module 이름	구분	이름	비트 수	설명
tl_cntr	input	clk	1-bit	Clock
		reset_n	1-bit	Active low에 동작하는 reset 신호로 state를 초기화
		Ta	1-bit	Traffic sensor A('Academic Ave.'에 위치)
		Tb	1-bit	Traffic sensor B('Bravado Blvd.'에 위치)
	output	La	2-bit	신호등 값 출력 A('Academic Ave'에 위치)
		Lb	2-bit	신호등 값 출력 B('Bravado Blvd.'에 위치)

TRAFFIC LIGHT CONTROLLER WITH LEFT TURN SIGNALS

Traffic Light Controller with Left Turn Signals

- 신호등을 제어하는 logic을 구현
  - 앞서 실습한 traffic light controller에 left turn signal을 추가하여 구현

  - 신호등 L_A는 'Academic Ave.'의 차량 통행을 제어하는 신호등
  - L_B는 'Bravado Blvd.'의 차량 통행을 제어하는 신호등
  - 시간에 따라 변하는 신호등이 아닌 거리에 차량이 있을 때 신호등이 초록색이 되고, 없을 때는 빨간색이 된다.
  - 차량이 있음을 감지하기 위하여 'Academic Ave.'에 traffic sensor인 T_A, T_{AL}를, 'Bravado Blvd.'에 traffic sensor인 T_B, T_{BL}를 설치
  - Traffic sensor인 T_A, T_B는 직진에 대한 차량 감시
  - Traffic sensor인 T_{AL}, T_{BL}은 좌회전에 대한 차량 감시



TLC with LTS(Cont.)

- 다음 규칙을 만족해야 한다.
  - ✓ Traffic light는 교통이 없을 때 초록색에서 노란색을 거쳐 좌회전으로 변한다.
  - ✓ Traffic light는 교통이 없을 때 좌회전에서 노란색을 거쳐 빨간색으로 변한다.
  - ✓ Traffic light는 비록 좌회전하는 교통이 없더라도 초록색에서 좌회전으로 우선 변해야 한다.
  - ✓ 만약 traffic light L_A가 초록색, 노란색, 좌회전일 동안에 L_B는 빨간색이어야 한다. 반대의 경우도 마찬가지이다.

Finite State Machine

- Design
  1. Drawing the finite state diagram
     - Define states
     - Define inputs
     - Define outputs
     - Draw the diagram
  2. Encoding states
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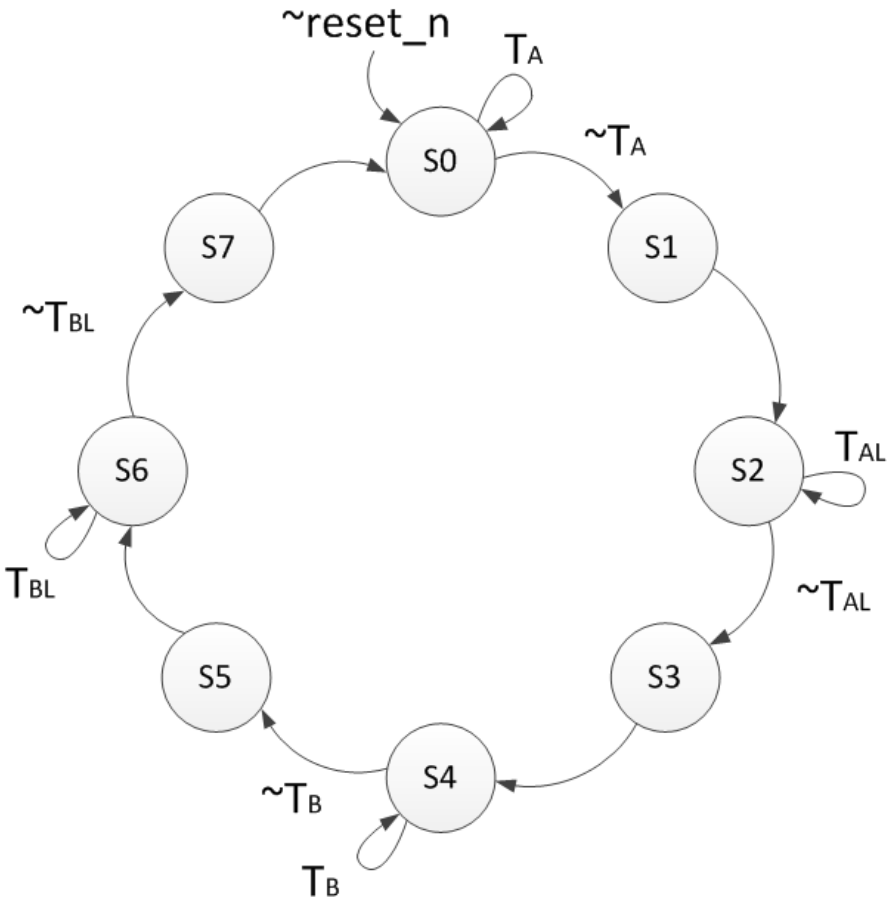
FSM State Transition Diagram

- Moore FSM



State	L_A	L_B
S0	Green	Red
S1	Yellow	Red
S2	Left	Red
S3	Yellow	Red
S4	Red	Green
S5	Red	Yellow
S6	Red	Left
S7	Red	Yellow

FSM State Transition Table

Current State	Inputs				Next State
	T_A	T_{AL}	T_B	T_{BL}	
S0	1	X	x	x	S0

State	Code
S0	000
S1	001
S2	010
S3	011
S4	100
S5	101
S6	110
S7	111

FSM Encoded State Transition Table

Q_2	Q_1	Q_0	T_A	T_{AL}	T_B	T_{BL}	D_2	D_1	D_0
0	0	0	0	X	X	X	0	0	1
0	0	0	1	X	X	X	0	0	0
0	0	1	X	X	X	X	0	1	0
0	1	0	X	0	X	X	0	1	1
0	1	0	X	1	X	X	0	1	0
0	1	1	X	X	X	X	1	0	0
1	0	0	X	X	0	X	1	0	1
1	0	0	X	X	1	X	1	0	0
1	0	1	X	X	X	X	1	1	0
1	1	0	X	X	X	0	1	1	1
1	1	0	X	X	X	1	1	1	0
1	1	1	X	X	X	X	0	0	0

FSM Encoded State Transition Table

Q_2	Q_1	Q_0	T_A	T_{AL}	T_B	T_{BL}	D_2	D_1	D_0
0	0	0	0	X	X	X	0	0	1
0	0	0	1	X	X	X	0	0	0
0	0	1	X	X	X	X	0	1	0
0	1	0	X	0	X	X	0	1	1
0	1	0	X	1	X	X	0	1	0
0	1	1	X	X	X	X	1	0	0
1	0	0	X	X	0	X	1	0	1
1	0	0	X	X	1	X	1	0	0
1	0	1	X	X	X	X	1	1	0
1	1	0	X	X	X	0	1	1	1
1	1	0	X	X	X	1	1	1	0
1	1	1	X	X	X	X	0	0	0

$D_2 =$

$D_1 =$

$D_0 =$

quine-mccluskey method of Next State D_2 (1/10)

Q_2	Q_1	Q_0	T_A	T_{AL}	T_B	T_{BL}	D_2	D_1	D_0
0	0	0	0	X	X	X	0	0	1
0	0	0	1	X	X	X	0	0	0
0	0	1	X	X	X	X	0	1	0
0	1	0	X	0	X	X	0	1	1
0	1	0	X	1	X	X	0	1	0
0	1	1	X	X	X	X	1	0	0
1	0	0	X	X	0	X	1	0	1
1	0	0	X	X	1	X	1	0	0
1	0	1	X	X	X	X	1	1	0
1	1	0	X	X	X	0	1	1	1
1	1	0	X	X	X	1	1	1	0
1	1	1	X	X	X	X	0	0	0

quine-mccluskey method of Next State D_2 (2/10)

Q_2	Q_1	Q_0	T_A	T_{AL}	T_B	T_{BL}	Deci.
0	1	1	0	0	0	0	48
0	1	1	0	0	0	1	49
0	1	1	0	0	1	0	50
0	1	1	0	0	1	1	51
0	1	1	0	1	0	0	52
0	1	1	0	1	0	1	53
0	1	1	0	1	1	0	54
0	1	1	0	1	1	1	55
0	1	1	1	0	0	0	56
0	1	1	1	0	0	1	57
0	1	1	1	0	1	0	58
0	1	1	1	0	1	1	59
0	1	1	1	1	0	0	60
0	1	1	1	1	0	1	61
0	1	1	1	1	1	0	62
0	1	1	1	1	1	1	63
1	0	0	0	0	0	0	64
1	0	0	0	0	0	1	65
1	0	0	0	0	1	0	66
1	0	0	0	0	1	1	67
1	0	0	0	1	0	0	68
1	0	0	0	1	0	1	69
1	0	0	0	1	1	0	70
1	0	0	0	1	1	1	71
1	0	0	1	0	0	0	72
1	0	0	1	0	0	1	73
1	0	0	1	0	1	0	74
1	0	0	1	0	1	1	75
1	0	0	1	1	0	0	76
1	0	0	1	1	0	1	77
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

Q_2	Q_1	Q_0	T_A	T_{AL}	T_B	T_{BL}	Deci.
1	0	1	0	0	0	0	80
1	0	1	0	0	0	1	81
1	0	1	0	0	1	0	82
1	0	1	0	0	1	1	83
1	0	1	0	1	0	0	84
1	0	1	0	1	0	1	85
1	0	1	0	1	1	0	86
1	0	1	0	1	1	1	87
1	0	1	1	0	0	0	88
1	0	1	1	0	0	1	89
1	0	1	1	0	1	0	90
1	0	1	1	0	1	1	91
1	0	1	1	1	0	0	92
1	0	1	1	1	0	1	93
1	0	1	1	1	1	0	94
1	0	1	1	1	1	1	95
1	1	0	0	0	0	0	96
1	1	0	0	0	0	1	97
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101
1	1	0	0	1	1	0	102
1	1	0	0	1	1	1	103
1	1	0	1	0	0	0	104
1	1	0	1	0	0	1	105
1	1	0	1	0	1	0	106
1	1	0	1	0	1	1	107
1	1	0	1	1	0	0	108
1	1	0	1	1	0	1	109
1	1	0	1	1	1	0	110
1	1	0	1	1	1	1	111

quine-mccluskey method of Next State D_2 (3/10)

Num of 1	input
0	
1	64 1000000
2	48 0110000 65 1000001 66 1000010 68 1000100 72 1001000 80 1010000 96 1100000
3	49 0110001 50 0110010 52 0110100 56 0111000 67 1000011 69 1000101 70 1000110 73 1001001 74 1001010 76 1001100 81 1010001 82 1010010 84 1010100 88 1011000 97 1100001 98 1100010 100 1100100 104 1101000

Num of 1	input
4	51 0110011 53 0110101 54 0110110 57 0111001 58 0111010 60 0111100 71 1000111 75 1001011 77 1001101 78 1001110 83 1010011 85 1010101 86 1010110 89 1011001 90 1011010 92 1011100 99 1100011 101 1100101 102 1100110 105 1101001 106 1101010 108 1101100
5	55 0110111 59 0111011 61 0111101 62 0111110 79 1001111 87 1010111 91 1011011 93 1011101 94 1011110 103 1100111 107 1101011 109 1101101 110 1101110

Num of 1	input
6	63 0111111 95 1011111 111 1101111

quine-mccluskey method of Next State D_2 (4/10)

First Comparison	input
0	
1	(65 , 64) 100000- (66 , 64) 10000-0 (68 , 64) 1000-00 (72 , 64) 100-000 (80 , 64) 10-0000 (96 , 64) 1-00000
2	(49 , 48) 011000- (50 , 48) 01100-0 (52 , 48) 0110-00 (56 , 48) 011-000 (67 , 65) 10000-1 (69 , 65) 1000-01 (73 , 65) 100-001 (81 , 65) 10-0001 (97 , 65) 1-00001 (67 , 66) 100001- (70 , 66) 1000-10 (74 , 66) 100-010 (82 , 66) 10-0010 (98 , 66) 1-00010 (69 , 68) 100010- (70 , 68) 10001-0 (76 , 68) 100-100 (84 , 68) 10-0100 (100 , 68) 1-00100 (73 , 72) 100100- (74 , 72) 10010-0 (76 , 72) 1001-00 (88 , 72) 10-1000 (104 , 72) 1-01000 (81 , 80) 101000- (82 , 80) 10100-0 (84 , 80) 1010-00 (88 , 80) 101-000 (97 , 96) 110000- (98 , 96) 11000-0 (100 , 96) 1100-00 (104 , 96) 110-000

First Comparison	input
3	(51 , 49) 01100-1 (53 , 49) 0110-01 (57 , 49) 011-001 (51 , 50) 011001- (54 , 50) 0110-10 (58 , 50) 011-010 (53 , 52) 011010- (54 , 52) 01101-0 (60 , 52) 011-100 (57 , 56) 011100- (58 , 56) 01110-0 (60 , 56) 0111-00 (71 , 67) 1000-11 (75 , 67) 100-011 (83 , 67) 10-0011 (99 , 67) 1-00011 (71 , 69) 10001-1 (77 , 69) 100-101 (85 , 69) 10-0101 (101 , 69) 1-00101 (71 , 70) 100011- (78 , 70) 100-110 (86 , 70) 10-0110 (102 , 70) 1-00110 (75 , 73) 10010-1 (77 , 73) 1001-01 (89 , 73) 10-1001 (105 , 73) 1-01001 (75 , 74) 100101- (78 , 74) 1001-10 (90 , 74) 10-1010 (106 , 74) 1-01010 (77 , 76) 100110- (78 , 76) 10011-0 (92 , 76) 10-1100 (108 , 76) 1-01100 (83 , 81) 10100-1 (85 , 81) 1010-01 (89 , 81) 101-001

First Comparison	input
3	(83 , 82) 101001- (86 , 82) 1010-10 (90 , 82) 101-010 (85 , 84) 101010- (86 , 84) 10101-0 (92 , 84) 101-100 (89 , 88) 101100- (90 , 88) 10110-0 (92 , 88) 1011-00 (99 , 97) 11000-1 (101 , 97) 1100-01 (105 , 97) 110-001 (99 , 98) 110001- (102 , 98) 1100-10 (106 , 98) 110-010 (101 , 100) 110010- (102 , 100) 11001-0 (108 , 100) 110-100 (105 , 104) 110100- (106 , 104) 11010-0 (108 , 104) 1101-00

quine-mccluskey method of Next State D_2 (5/10)

First Comparison	input
4	(55 , 51) 0110-11 (59 , 51) 011-011 (55 , 53) 01101-1 (61 , 53) 011-101 (55 , 54) 011011- (62 , 54) 011-110 (59 , 57) 01110-1 (61 , 57) 0111-01 (59 , 58) 011101- (62 , 58) 0111-10 (61 , 60) 011110- (62 , 60) 01111-0 (79 , 71) 100-111 (87 , 71) 10-0111 (103 , 71) 1-00111 (79 , 75) 1001-11 (91 , 75) 10-1011 (107 , 75) 1-01011 (79 , 77) 10011-1 (93 , 77) 10-1101 (109 , 77) 1-01101 (79 , 78) 100111- (94 , 78) 10-1110 (110 , 78) 1-01110 (87 , 83) 1010-11 (91 , 83) 101-011 (87 , 85) 10101-1 (93 , 85) 101-101 (87 , 86) 101011- (94 , 86) 101-110 (91 , 89) 10110-1 (93 , 89) 1011-01 (91 , 90) 101101- (94 , 90) 1011-10

First Comparison	input
4	(93 , 92) 101110- (94 , 92) 10111-0 (103 , 99) 1100-11 (107 , 99) 110-011 (103 , 101) 11001-1 (109 , 101) 110-101 (103 , 102) 110011- (110 , 102) 110-110 (107 , 105) 11010-1 (109 , 105) 1101-01 (107 , 106) 110101- (110 , 106) 1101-10 (109 , 108) 110110- (110 , 108) 11011-0
5	(63 , 55) 011-111 (63 , 59) 0111-11 (63 , 61) 01111-1 (63 , 62) 011111- (95 , 79) 10-1111 (111 , 79) 1-01111 (95 , 87) 101-111 (95 , 91) 1011-11 (95 , 93) 10111-1 (95 , 94) 101111- (111 , 103) 110-111 (111 , 107) 1101-11 (111 , 109) 11011-1 (111 , 110) 110111-

quine-mccluskey method of Next State D_2 (6/10)

Second Comparison	input
0	
1	(67 , 66 , 65 , 64) 10000-- (69 , 68 , 65 , 64) 1000-0- (73 , 72 , 65 , 64) 100-00- (81 , 80 , 65 , 64) 10-000- (97 , 96 , 65 , 64) 1-0000- (70 , 68 , 66 , 64) 1000--0 (74 , 72 , 66 , 64) 100-0-0 (82 , 80 , 66 , 64) 10-00-0 (98 , 96 , 66 , 64) 1-000-0 (76 , 72 , 68 , 64) 100--00 (84 , 80 , 68 , 64) 10-0-00 (100 , 96 , 68 , 64) 1-00-00 (88 , 80 , 72 , 64) 10--000 (104 , 96 , 72 , 64) 1-0-000
2	(51 , 50 , 49 , 48) 01100-- (53 , 52 , 49 , 48) 0110-0- (57 , 56 , 49 , 48) 011-00- (54 , 52 , 50 , 48) 0110--0 (58 , 56 , 50 , 48) 011-0-0 (60 , 56 , 52 , 48) 011--00 (71 , 69 , 67 , 65) 1000--1 (75 , 73 , 67 , 65) 100-0-1 (83 , 81 , 67 , 65) 10-00-1 (99 , 97 , 67 , 65) 1-000-1 (77 , 73 , 69 , 65) 100--01 (85 , 81 , 69 , 65) 10-0-01 (101 , 97 , 69 , 65) 1-00-01 (89 , 81 , 73 , 65) 10--001 (105 , 97 , 73 , 65) 1-0-001 (71 , 70 , 67 , 66) 1000-1- (75 , 74 , 67 , 66) 100-01- (83 , 82 , 67 , 66) 10-001- (99 , 98 , 67 , 66) 1-0001- (78 , 74 , 70 , 66) 100--10 (86 , 82 , 70 , 66) 10-0-10

Second Comparison	input
2	(102 , 98 , 70 , 66) 1-00-10 (90 , 82 , 74 , 66) 10--010 (106 , 98 , 74 , 66) 1-0-010 (71 , 70 , 69 , 68) 10001-- (77 , 76 , 69 , 68) 100-10- (85 , 84 , 69 , 68) 10-010- (101 , 100 , 69 , 68) 1-0010- (78 , 76 , 70 , 68) 100-1-0 (86 , 84 , 70 , 68) 10-01-0 (102 , 100 , 70 , 68) 1-001-0 (92 , 84 , 76 , 68) 10--100 (108 , 100 , 76 , 68) 1-0-100 (75 , 74 , 73 , 72) 10010-- (77 , 76 , 73 , 72) 1001-0- (89 , 88 , 73 , 72) 10-100- (105 , 104 , 73 , 72) 1-0100- (78 , 76 , 74 , 72) 1001--0 (90 , 88 , 74 , 72) 10-10-0 (106 , 104 , 74 , 72) 1-010-0 (92 , 88 , 76 , 72) 10-1-00 (108 , 104 , 76 , 72) 1-01-00 (83 , 82 , 81 , 80) 10100-- (85 , 84 , 81 , 80) 1010-0- (89 , 88 , 81 , 80) 101-00- (86 , 84 , 82 , 80) 1010--0 (90 , 88 , 82 , 80) 101-0-0 (92 , 88 , 84 , 80) 101--00 (99 , 98 , 97 , 96) 11000-- (101 , 100 , 97 , 96) 1100-0- (105 , 104 , 97 , 96) 110-00- (102 , 100 , 98 , 96) 1100--0 (106 , 104 , 98 , 96) 110-0-0 (108 , 104 , 100 , 96) 110--00

quine-mccluskey method of Next State D_2 (7/10)

Second Comparison	input
3	(55 , 53 , 51 , 49) 0110--1 (59 , 57 , 51 , 49) 011-0-1 (61 , 57 , 53 , 49) 011--01 (55 , 54 , 51 , 50) 0110-1- (59 , 58 , 51 , 50) 011-01- (62 , 58 , 54 , 50) 011--10 (55 , 54 , 53 , 52) 01101-- (61 , 60 , 53 , 52) 011-10- (62 , 60 , 54 , 52) 011-1-0 (59 , 58 , 57 , 56) 01110-- (61 , 60 , 57 , 56) 0111-0- (62 , 60 , 58 , 56) 0111--0 (79 , 75 , 71 , 67) 100--11 (87 , 83 , 71 , 67) 10-0-11 (103 , 99 , 71 , 67) 1-00-11 (91 , 83 , 75 , 67) 10--011 (107 , 99 , 75 , 67) 1-0-011 (79 , 77 , 71 , 69) 100-1-1 (87 , 85 , 71 , 69) 10-01-1 (103 , 101 , 71 , 69) 1-001-1 (93 , 85 , 77 , 69) 10--101 (109 , 101 , 77 , 69) 1-0-101 (79 , 78 , 71 , 70) 100-11- (87 , 86 , 71 , 70) 10-011- (103 , 102 , 71 , 70) 1-0011- (94 , 86 , 78 , 70) 10--110 (110 , 102 , 78 , 70) 1-0-110 (79 , 77 , 75 , 73) 1001--1 (91 , 89 , 75 , 73) 10-10-1 (107 , 105 , 75 , 73) 1-010-1 (93 , 89 , 77 , 73) 10-1-01 (109 , 105 , 77 , 73) 1-01-01 (79 , 78 , 75 , 74) 1001-1- (91 , 90 , 75 , 74) 10-101- (107 , 106 , 75 , 74) 1-0101- (94 , 90 , 78 , 74) 10-1-10 (110 , 106 , 78 , 74) 1-01-10 (79 , 78 , 77 , 76) 10011-- (93 , 92 , 77 , 76) 10-110-

Second Comparison	input
3	(109 , 108 , 77 , 76) 1-0110- (94 , 92 , 78 , 76) 10-11-0 (110 , 108 , 78 , 76) 1-011-0 (87 , 85 , 83 , 81) 1010--1 (91 , 89 , 83 , 81) 101-0-1 (93 , 89 , 85 , 81) 101--01 (87 , 86 , 83 , 82) 1010-1- (91 , 90 , 83 , 82) 101-01- (94 , 90 , 86 , 82) 101--10 (87 , 86 , 85 , 84) 10101-- (93 , 92 , 85 , 84) 101-10- (94 , 92 , 86 , 84) 101-1-0 (91 , 90 , 89 , 88) 10110-- (93 , 92 , 89 , 88) 1011-0- (94 , 92 , 90 , 88) 1011--0 (103 , 101 , 99 , 97) 1100--1 (107 , 105 , 99 , 97) 110-0-1 (109 , 105 , 101 , 97) 110--01 (103 , 102 , 99 , 98) 1100-1- (107 , 106 , 99 , 98) 110-01- (110 , 106 , 102 , 98) 110--10 (103 , 102 , 101 , 100) 11001-- (109 , 108 , 101 , 100) 110-10- (110 , 108 , 102 , 100) 110-1-0 (107 , 106 , 105 , 104) 11010-- (109 , 108 , 105 , 104) 1101-0- (110 , 108 , 106 , 104) 1101--0

quine-mccluskey method of Next State D_2 (8/10)

Second Comparison	input
4	(63 , 59 , 55 , 51) 011--11 (63 , 61 , 55 , 53) 011-1-1 (63 , 62 , 55 , 54) 011-11- (63 , 61 , 59 , 57) 0111--1 (63 , 62 , 59 , 58) 0111-1- (63 , 62 , 61 , 60) 01111-- (95 , 87 , 79 , 71) 10--111 (111 , 103 , 79 , 71) 1-0-111 (95 , 91 , 79 , 75) 10-1-11 (111 , 107 , 79 , 75) 1-01-11 (95 , 93 , 79 , 77) 10-11-1 (111 , 109 , 79 , 77) 1-011-1 (95 , 94 , 79 , 78) 10-111- (111 , 110 , 79 , 78) 1-0111- (95 , 91 , 87 , 83) 101--11 (95 , 93 , 87 , 85) 101-1-1 (95 , 94 , 87 , 86) 101-11- (95 , 93 , 91 , 89) 1011--1 (95 , 94 , 91 , 90) 1011-1- (95 , 94 , 93 , 92) 10111-- (111 , 107 , 103 , 99) 110--11 (111 , 109 , 103 , 101) 110-1-1 (111 , 110 , 103 , 102) 110-11- (111 , 109 , 107 , 105) 1101--1 (111 , 110 , 107 , 106) 1101-1- (111 , 110 , 109 , 108) 11011--

quine-mccluskey method of Next State D_2 (9/10)

Prime Implicants

(67 , 66 , 65 , 64) 10000--
(69 , 68 , 65 , 64) 1000-0-
(73 , 72 , 65 , 64) 100-00-
(81 , 80 , 65 , 64) 10-000-
(97 , 96 , 65 , 64) 1-0000-
(70 , 68 , 66 , 64) 1000--0
(74 , 72 , 66 , 64) 100-0-0
(82 , 80 , 66 , 64) 10-00-0
(98 , 96 , 66 , 64) 1-000-0
(76 , 72 , 68 , 64) 100--00
(84 , 80 , 68 , 64) 10-0-00
(100 , 96 , 68 , 64) 1-00-00
(88 , 80 , 72 , 64) 10--000
(104 , 96 , 72 , 64) 1-0-000
(51 , 50 , 49 , 48) 01100--
(53 , 52 , 49 , 48) 0110-0-
(57 , 56 , 49 , 48) 011-00-
(54 , 52 , 50 , 48) 0110--0
(58 , 56 , 50 , 48) 011-0-0
(60 , 56 , 52 , 48) 011--00
(71 , 69 , 67 , 65) 1000--1
(75 , 73 , 67 , 65) 100-0-1
(83 , 81 , 67 , 65) 10-00-1
(99 , 97 , 67 , 65) 1-000-1
(77 , 73 , 69 , 65) 100--01
(85 , 81 , 69 , 65) 10-0-01
(101 , 97 , 69 , 65) 1-00-01
(89 , 81 , 73 , 65) 10--001
(105 , 97 , 73 , 65) 1-0-001
(71 , 70 , 67 , 66) 1000-1-
(75 , 74 , 67 , 66) 100-01-
(83 , 82 , 67 , 66) 10-001-
(99 , 98 , 67 , 66) 1-0001-
(78 , 74 , 70 , 66) 100—10
(86 , 82 , 70 , 66) 10-0-10
(102 , 98 , 70 , 66) 1-00-10
(90 , 82 , 74 , 66) 10--010
(106 , 98 , 74 , 66) 1-0-010
(71 , 70 , 69 , 68) 10001--
(77 , 76 , 69 , 68) 100-10-
(85 , 84 , 69 , 68) 10-010-
(101 , 100 , 69 , 68) 1-0010-
(78 , 76 , 70 , 68) 100-1-0
(86 , 84 , 70 , 68) 10-01-0
(102 , 100 , 70 , 68) 1-001-0
(92 , 84 , 76 , 68) 10--100
(108 , 100 , 76 , 68) 1-0-100
(75 , 74 , 73 , 72) 10010--
(77 , 76 , 73 , 72) 1001-0-
(89 , 88 , 73 , 72) 10-100-
(105 , 104 , 73 , 72) 1-0100-
(78 , 76 , 74 , 72) 1001--0
(90 , 88 , 74 , 72) 10-10-0
(106 , 104 , 74 , 72) 1-010-0
(92 , 88 , 76 , 72) 10-1-00
(108 , 104 , 76 , 72) 1-01-00
(83 , 82 , 81 , 80) 10100--
(85 , 84 , 81 , 80) 1010-0-
(89 , 88 , 81 , 80) 101-00-
(86 , 84 , 82 , 80) 1010--0
(90 , 88 , 82 , 80) 101-0-0
(92 , 88 , 84 , 80) 101--00
(99 , 98 , 97 , 96) 11000--
(101 , 100 , 97 , 96) 1100-0-
(105 , 104 , 97 , 96) 110-00-
(102 , 100 , 98 , 96) 1100--0
(106 , 104 , 98 , 96) 110-0-0
(108 , 104 , 100 , 96) 110--00
(55 , 53 , 51 , 49) 0110--1
(59 , 57 , 51 , 49) 011-0-1
(61 , 57 , 53 , 49) 011--01
(55 , 54 , 51 , 50) 0110-1-
(59 , 58 , 51 , 50) 011-01-
(62 , 58 , 54 , 50) 011--10
(55 , 54 , 53 , 52) 01101--
(61 , 60 , 53 , 52) 011-10-
(62 , 60 , 54 , 52) 011-1-0
(59 , 58 , 57 , 56) 01110--
(61 , 60 , 57 , 56) 0111-0-
(62 , 60 , 58 , 56) 0111--0
(79 , 75 , 71 , 67) 100--11
(87 , 83 , 71 , 67) 10-0-11
(103 , 99 , 71 , 67) 1-00-11
(91 , 83 , 75 , 67) 10--011
(107 , 99 , 75 , 67) 1-0-011
(79 , 77 , 71 , 69) 100-1-1
(87 , 85 , 71 , 69) 10-01-1
(103 , 101 , 71 , 69) 1-001-1
(93 , 85 , 77 , 69) 10--101
(109 , 101 , 77 , 69) 1-0-101
(79 , 78 , 71 , 70) 100-11-
(87 , 86 , 71 , 70) 10-011-
(103 , 102 , 71 , 70) 1-0011-
(94 , 86 , 78 , 70) 10--110
(110 , 102 , 78 , 70) 1-0-110
(79 , 77 , 75 , 73) 1001--1
(91 , 89 , 75 , 73) 10-10-1
(107 , 105 , 75 , 73) 1-010-1
(93 , 89 , 77 , 73) 10-1-01
(109 , 105 , 77 , 73) 1-01-01
(79 , 78 , 75 , 74) 1001-1-
(91 , 90 , 75 , 74) 10-101-
(107 , 106 , 75 , 74) 1-0101-
(94 , 90 , 78 , 74) 10-1-10
(110 , 106 , 78 , 74) 1-01-10
(79 , 78 , 77 , 76) 10011--
(93 , 92 , 77 , 76) 10-110-
(109 , 108 , 77 , 76) 1-0110-
(94 , 92 , 78 , 76) 10-11-0
(110 , 108 , 78 , 76) 1-011-0
(87 , 85 , 83 , 81) 1010--1
(91 , 89 , 83 , 81) 101-0-1
(93 , 89 , 85 , 81) 101--01
(87 , 86 , 83 , 82) 1010-1-
(91 , 90 , 83 , 82) 101-01-
(94 , 90 , 86 , 82) 101--10
(87 , 86 , 85 , 84) 10101--
(93 , 92 , 85 , 84) 101-10-
(94 , 92 , 86 , 84) 101-1-0
(91 , 90 , 89 , 88) 10110--
(93 , 92 , 89 , 88) 1011-0-
(94 , 92 , 90 , 88) 1011--0
(103 , 101 , 99 , 97) 1100--1
(107 , 105 , 99 , 97) 110-0-1
(109 , 105 , 101 , 97) 110--01
(103 , 102 , 99 , 98) 1100-1-
(107 , 106 , 99 , 98) 110-01-
(110 , 106 , 102 , 98) 110--10
(103 , 102 , 101 , 100) 11001--
(109 , 108 , 101 , 100) 110-10-
(110 , 108 , 102 , 100) 110-1-0
(107 , 106 , 105 , 104) 11010--
(109 , 108 , 105 , 104) 1101-0-
(110 , 108 , 106 , 104) 1101--0
(63 , 59 , 55 , 51) 011--11
(63 , 61 , 55 , 53) 011-1-1
(63 , 62 , 55 , 54) 011-11-
(63 , 61 , 59 , 57) 0111--1
(63 , 62 , 59 , 58) 0111-1-
(63 , 62 , 61 , 60) 01111--
(95 , 87 , 79 , 71) 10--111
(111 , 103 , 79 , 71) 1-0-111
(95 , 91 , 79 , 75) 10-1-11
(111 , 107 , 79 , 75) 1-01-11
(95 , 93 , 79 , 77) 10-11-1
(111 , 109 , 79 , 77) 1-011-1
(95 , 94 , 79 , 78) 10-111-
(111 , 110 , 79 , 78) 1-0111-
(95 , 91 , 87 , 83) 101--11
(95 , 93 , 87 , 85) 101-1-1
(95 , 94 , 87 , 86) 101-11-
(95 , 93 , 91 , 89) 1011--1
(95 , 94 , 91 , 90) 1011-1-
(95 , 94 , 93 , 92) 10111--
(111 , 107 , 103 , 99) 110--11
(111 , 109 , 103 , 101) 110-1-1
(111 , 110 , 103 , 102) 110-11-
(111 , 109 , 107 , 105) 1101--1
(111 , 110 , 107 , 106) 1101-1-
(111 , 110 , 109 , 108) 11011--

quine-mccluskey method of Next State D_2 (10/10)

part of table

	01100--	0110-0-	011-00-	0110--0	011-0-0	011--00	0110--1	011-0-1	011--01	0110-1-	011-01-	011--10	01101--	011-10-	011-1-0	011--11	011-1-1	011-11-
48	X	X	X	X	X	X												
49	X	X	X				X	X	X									
50	X			X	X					X	X	X						
51	X						X	X		X	X					X		
52		X		X		X							X	X	X			
53		X					X		X				X	X			X	
54				X						X		X	X		X			X

$$\vdots$$

$$D_2 = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1} + Q_2Q_1\overline{Q_0}$$

$$D1, D0 = ?$$

Output Table

State	L_A	L_B
S0	Green	Red
S1	Yellow	Red
S2	Left	Red
S3	Yellow	Red
S4	Red	Green
S5	Red	Yellow
S6	Red	Left
S7	Red	Yellow

Color	Code
Green	00
Yellow	01
Left	10
Red	11

Output Encoded Table

Q_2	Q_1	Q_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}
0	0	0	0	0	1	1
0	0	1	0	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	1	1	0	0
1	0	1	1	1	0	1
1	1	0	1	1	1	0
1	1	1	1	1	0	1

$L_{A1} =$
$L_{A0} =$
$L_{B1} =$
$L_{B0} =$

Karnaugh Map of Output Light L_{A1}

Q_2	Q_1	Q_0	L_{A1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$L_{A1} =$ 

	00	01	11	10
0	0	0	0	1
1	1	1	1	1

가로는 각각 Q_1, Q_0타내며, 세로는 Q_2를 나타낸다.

Karnaugh Map of Output Light L_{A1}

Q_2	Q_1	Q_0	L_{A0}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$L_{A0} =$ 

	00	01	11	10
0	0	1	1	0
1	1	1	1	1

가로는 각각 Q_1, Q_0타내며, 세로는 Q_2를 나타낸다.

Karnaugh Map of Output Light L_{A1}

Q_2	Q_1	Q_0	L_{B1}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$L_{B1} =$ 

	00	01	11	10
0	1	1	1	1
1	0	0	0	1

가로는 각각 Q_1, Q_0타내며, 세로는 Q_2를 나타낸다.

Karnaugh Map of Output Light L_{A1}

Q_2	Q_1	Q_0	L_{B0}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$L_{B0} =$ 

	00	01	11	10
0	1	1	1	1
1	0	1	1	0

가로는 각각 Q_1, Q_0타내며, 세로는 Q_2를 나타낸다.

Module Configuration

구분	이름	설명
Top module	tl_cntr_w_left	Traffic light controller의 top module
Sub module	ns_logic	Traffic light controller의 next state를 결정하는 combinational logic
Sub module	_register3_r	3-bit resettable register with active low asynchronous reset module(내부에 d_ff_r_async를 instance) - 현재의 state 값을 저장
Sub module	_dff_r	Resettable D flip-flop with active low asynchronous reset
Sub module	o_logic	현재 state의 값에 기반하여 output 값을 결정하는 combinational logic

I/O Configuration

구분	이름	비트 수	설명
input	clk	1-bit	Clock
	reset_n	1-bit	Active low에 동작하는 reset 신호로 state를 초기화
	Ta	1-bit	Traffic sensor A('Academic Ave.'에 위치하여 직진 감지)
	Tal	1-bit	Traffic sensor AL('Academic Ave.'에 위치하여 좌회전 감지)
	Tb	1-bit	Traffic sensor B('Bravado Blvd.'에 위치하여 직진 감지)
	Tbl	1-bit	Traffic sensor BL('Bravado Blvd.'에 위치하여 좌회전 감지)
output	La	2-bit	신호등 값 출력 A('Academic Ave'에 위치)
	Lb	2-bit	신호등 값 출력 B('Bravado Blvd.'에 위치)

Assignment 5

- Report
  - ✓ 자세한 사항은 lab document 참고
- Submission
  - ✓ Soft copy
    - 기한 : 강의 당일부터 2주 (KLAS 과제란 참고)
    - 실습 미수강은 디지털 논리2 조교 공지에 따름
    - 늦은 숙제는 이틀 후 까지만 받음(20% 감점)

채점기준

세부사항		점수	최상	상	중	하	최하
소스코드	Source code가 잘 작성 되었는가? (Structural design으로 작성되었는가?)	10	10	8	5	3	0
	주석을 적절히 달았는가?	20	20	15	10	5	0
설계검증 (보고서)	보고서를 성실히 작성하였는가? (보고서 형식에 맞추어 작성)	30	30	20	10	5	0
	합성결과를 설명하였는가?	10	10	8	5	3	0
	검증을 제대로 수행하였는가? (모든 입력 조합, waveform 설명)	30	30	20	10	5	0
총점		100					

References

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Q&A

Thank you