VIETNAM NATIONAL UNIVERSITY - HCM

Ho Chi Minh City University of Technology

Faculty of Computer Science and Engineering

LOGIC DESIGN WITH VERILOG HDL

Mini Project:

DOOR LOCK

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Ho Chi Minh, November,2019

CONTENT

REPORT

INTRODUCTION:

Implement a door lock control design (using FSM is compulsory) with the features below:

• The password consists of three numeric digits from 0 to 9;

• To simplify the design, numeric digits are inputted by using BCD code and SWs are used to generate the input signal.

• There is only 1 digit that is inputted each time, a KEY is used to confirm an input value (assume KEY1). Input value must be showed on 7-segment LED.

• There are 2 modes that can be applied:

– Set modes: users set password.

– Verify modes: users enter a password and system check it.

Modes are switched by using KEY (assume KEY2)

• In Verify mode:

– If user enter a correct password: a GREEN led blink with a 5Hz frequency.

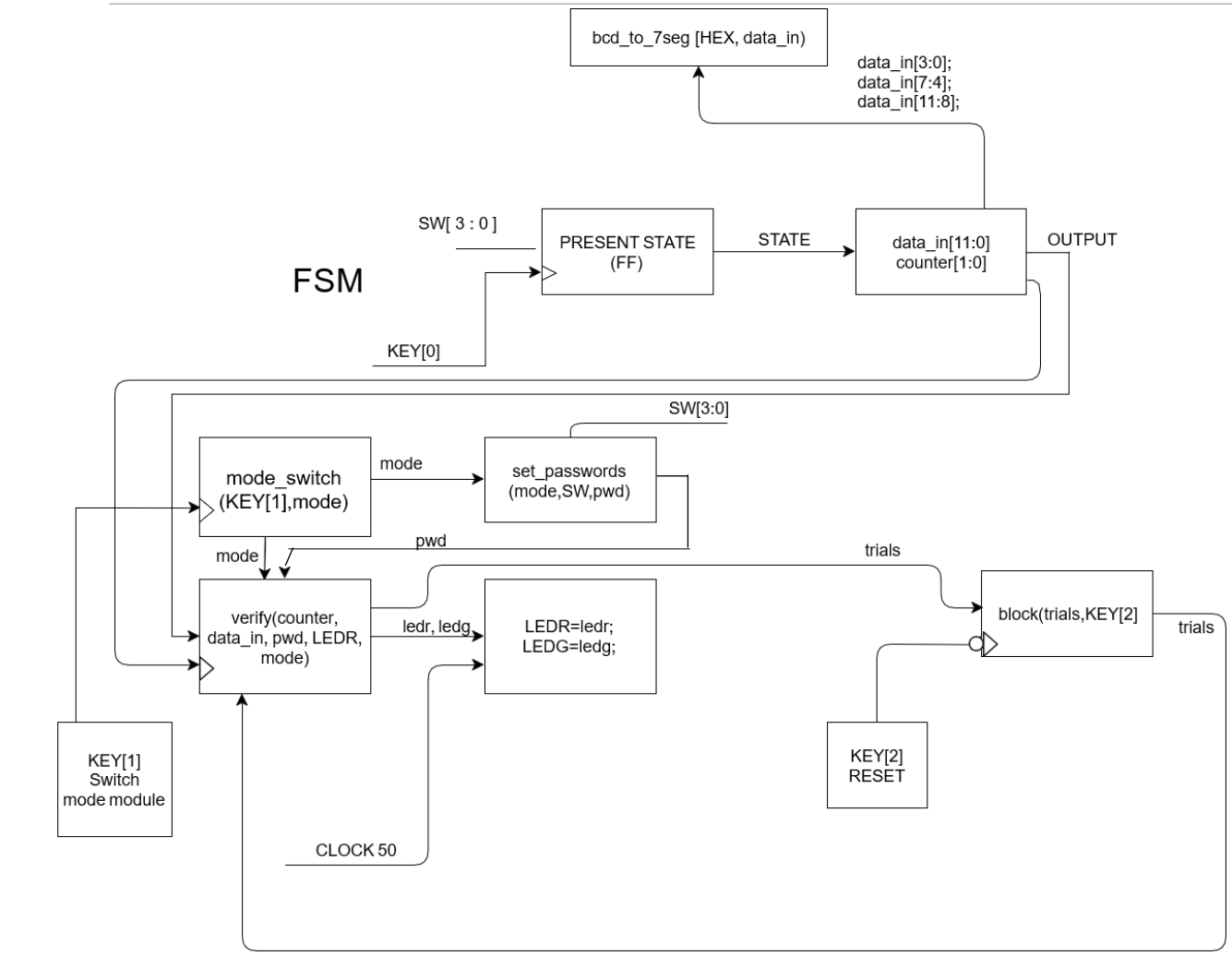
– If user enter a false password: a RED led blink with a 1Hz frequency.

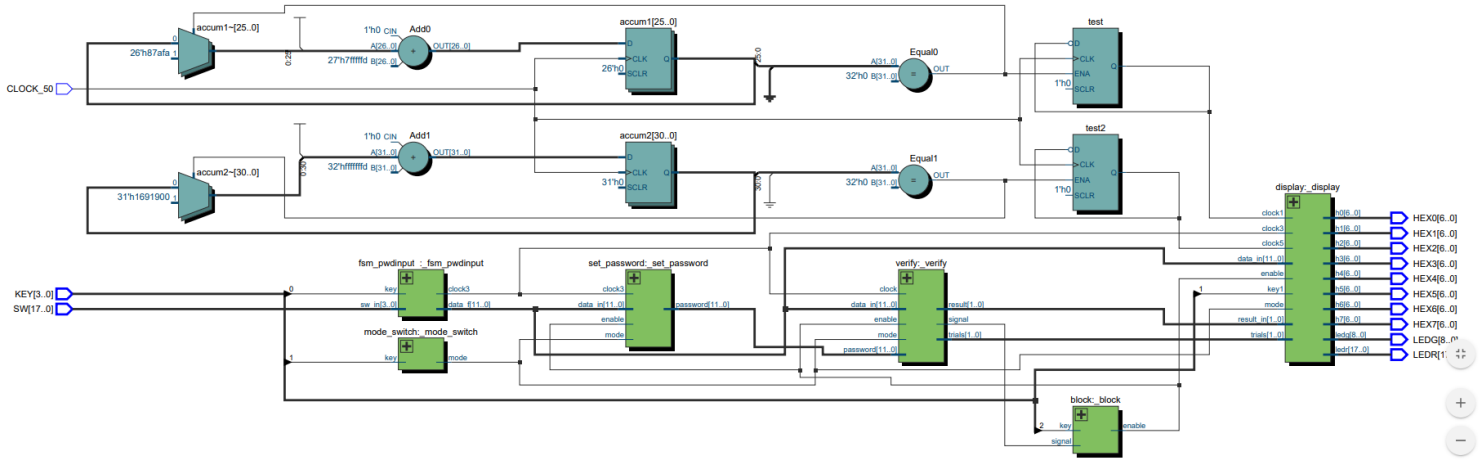
After that, user has more 2 trials. With these trials, if user enter a correct password, her/his number of trials will be resetted. On the contrary side, the system is blocked and only be reactivated by using RESET KEY (assume KEY3).

LIST OF MODULES:

1. Set_password
2. Fsm_pwdinput
3. Mode_switch
4. Verify
5. Block
6. Display
7. BCD_to_HEX_delay
8. Debounce
9. Debounce_display

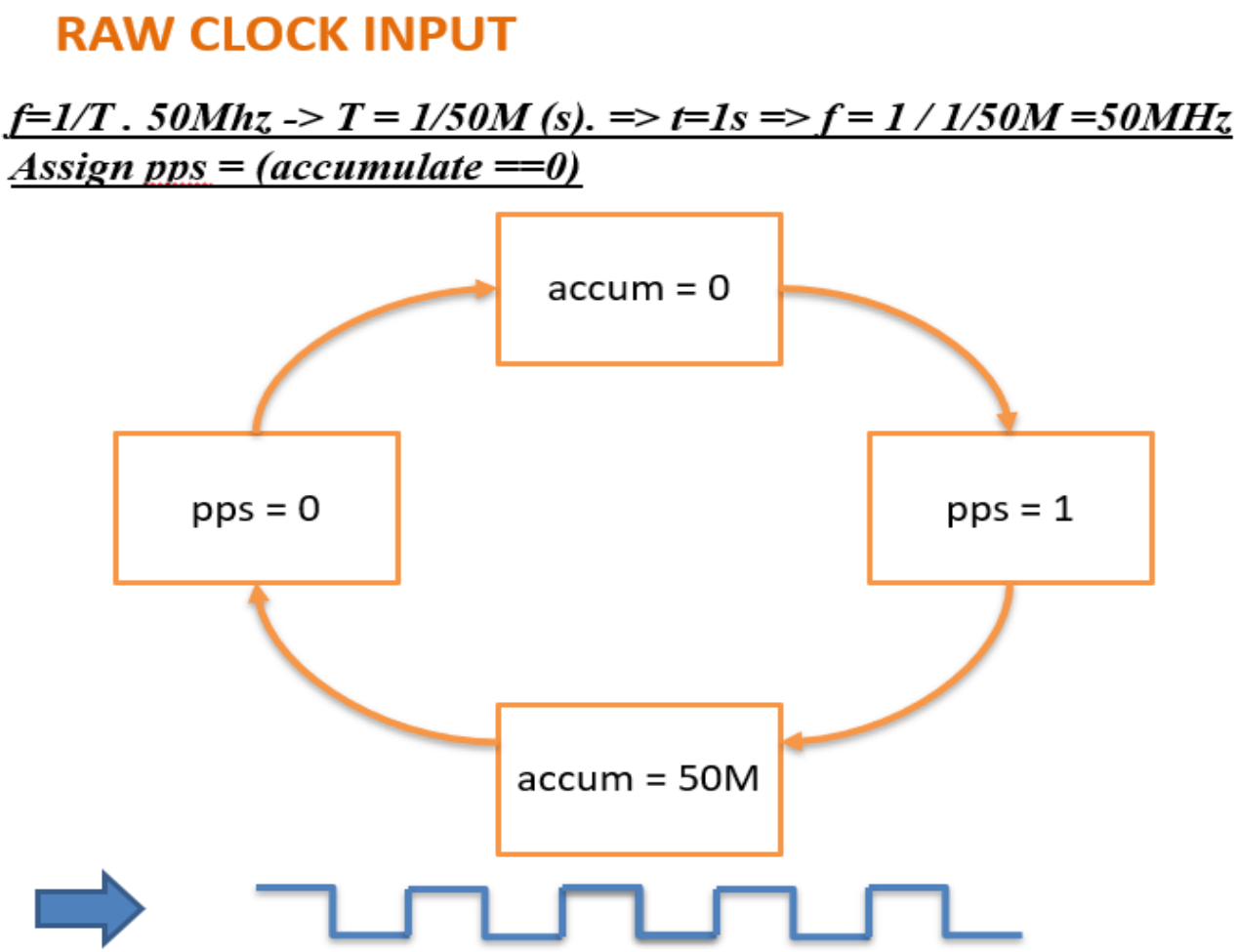
GENERAL VIEW:





DESIGN AND IMPLEMENTATION:

1. Clock Devider:



2. Mode_switch:

input: key

output: mode

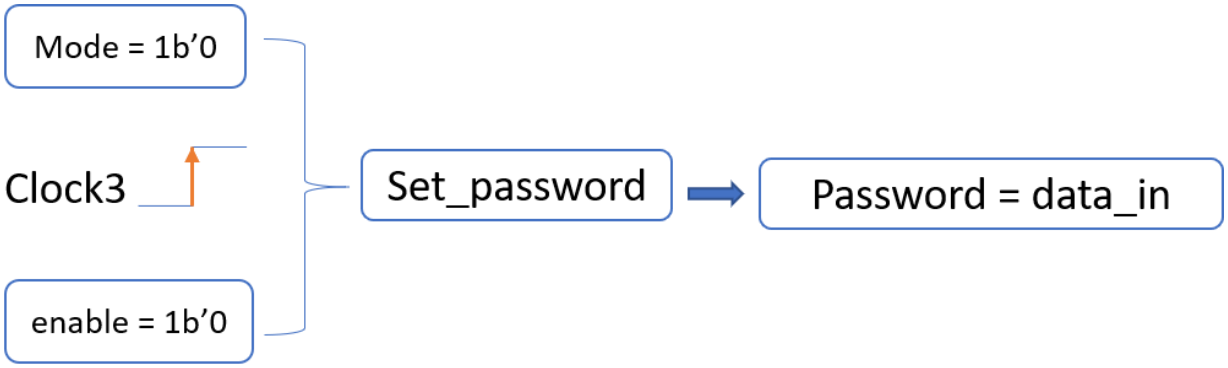
At beginning mode take the value of 0 which mean users are in the set mode, but when user press KEY[0] then the input key received the value of 1. This create a positive edge and the mode now is 1(verify mode).

3. Set_password:

Input: mode, clock3, enable.

Output: password.

When clock3 (from fsm module) change from 0 to 1, mode variable (from mode switch) is 0 and enable (block module) is 0. Then user's inputs are assigned to password

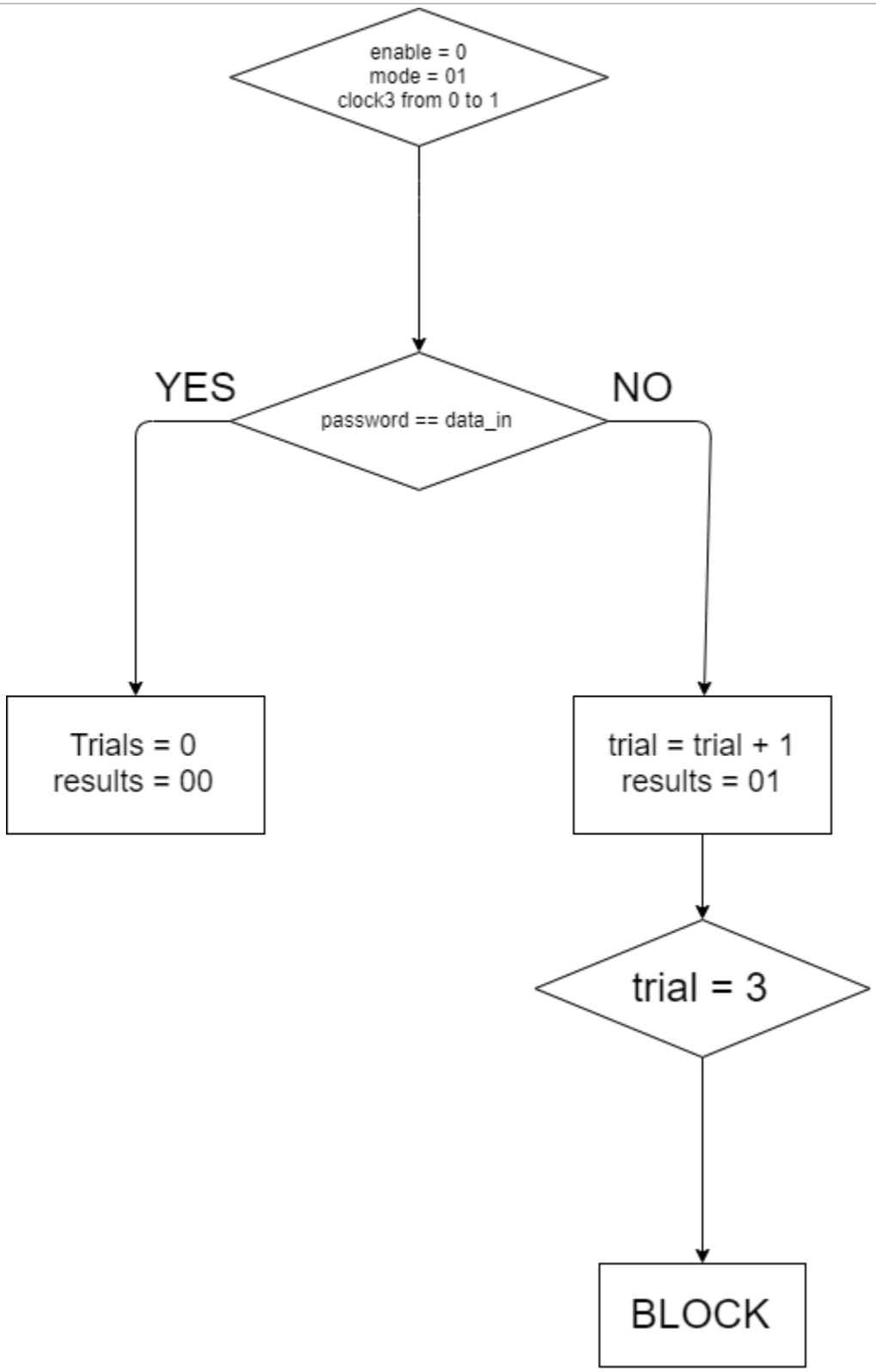


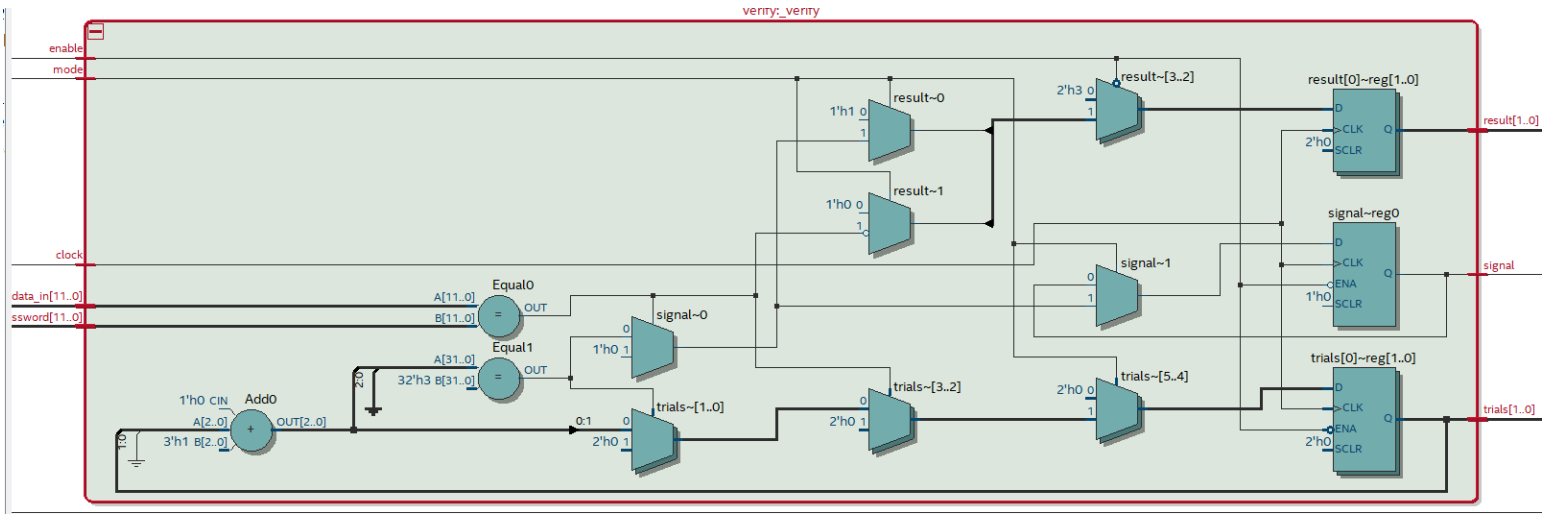
4. Verify:

Input: mode, enable, password, data_in, clock.

- Trials = 2'b00;
- Signal = 1'b0;

Output: trials, result, signal.

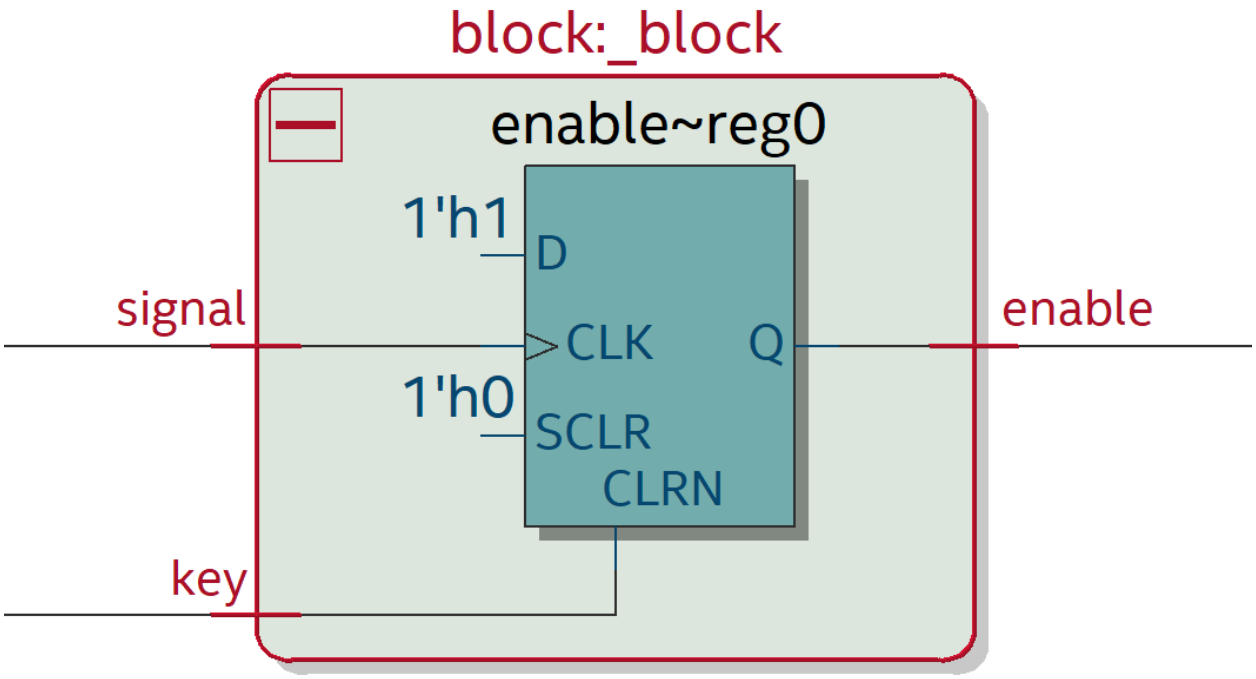

enable = 0
mode = 01
clock3 from 0 to 1
YES
password == data_in
NO
Trials = 0
results = 00
trial = trial + 1
results = 01
trial = 3
BLOCK



5. Block:

Input: key, signal.

Output: enable.



6. Fsm_pwdinput:

-count:

Base on D Flip-Flop count variable run from 0 -2 and turn back to 0 when reach 2

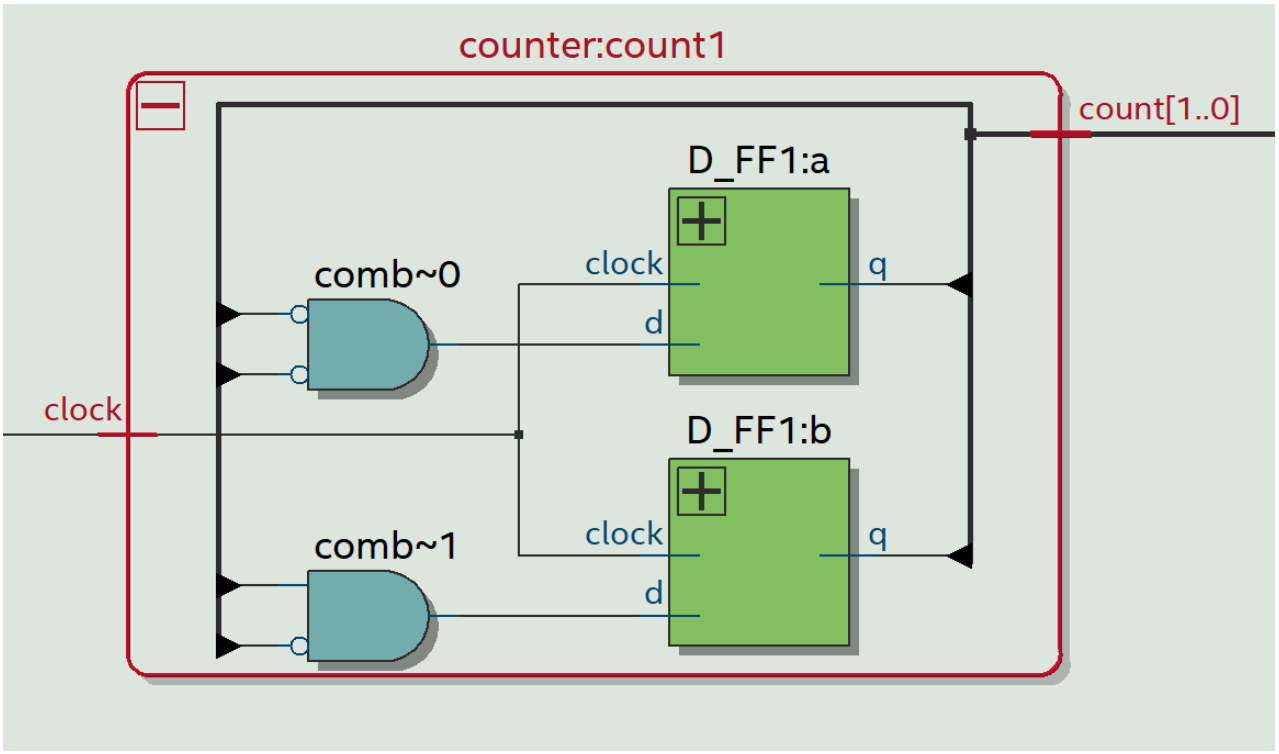
Present state		Next state		Control input	
Qb	Qa	Qb	Qa	D Qb	D Qa
0	0	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0
1	1	0	0	0	0

	$\overline{Qa}$	Qa
$\overline{Qb}$	1	0
Qb	0	0

D Qa = $\overline{Qa}\overline{Qb}$

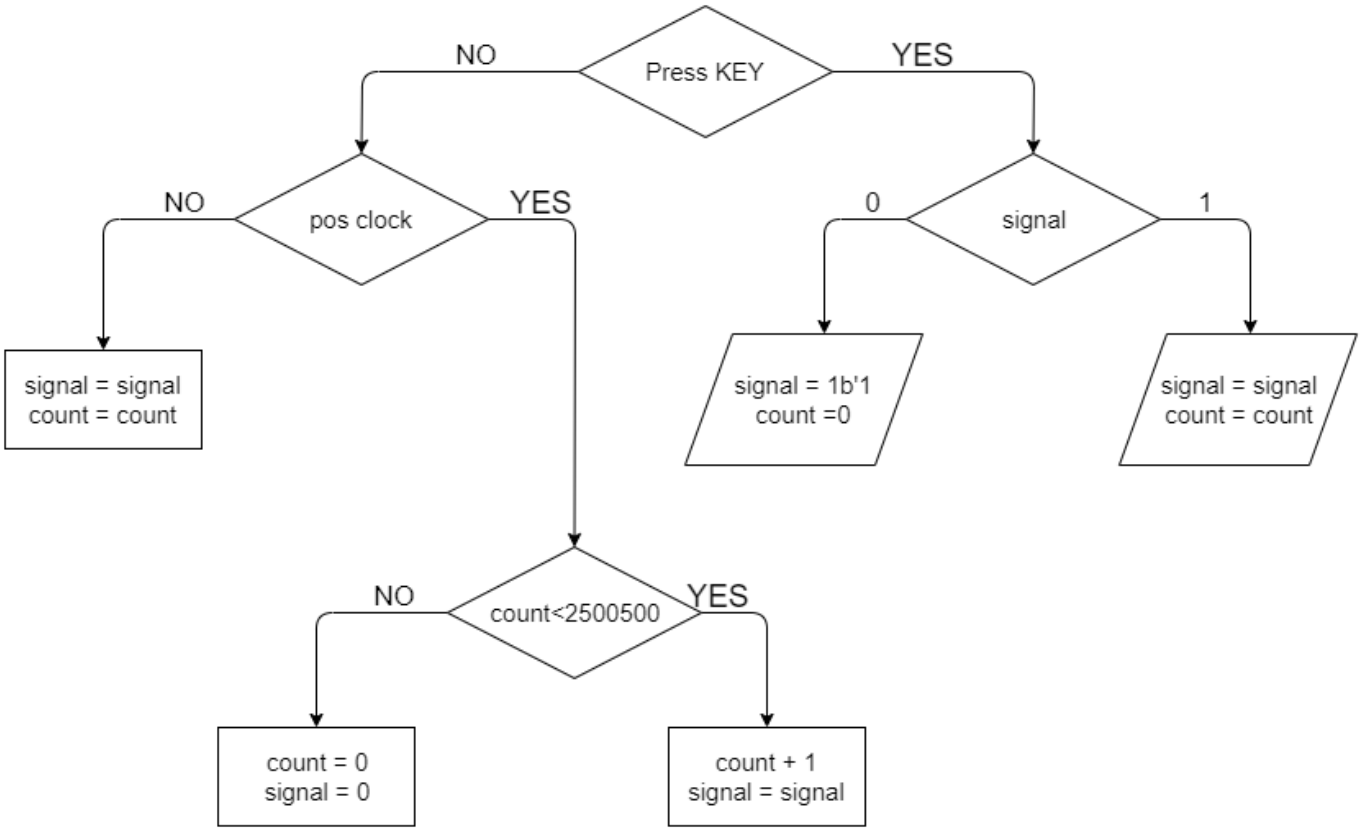
	$\overline{Qa}$	Qa
$\overline{Qb}$	0	1
Qb	0	0

D Qb = $Qa\overline{Qb}$

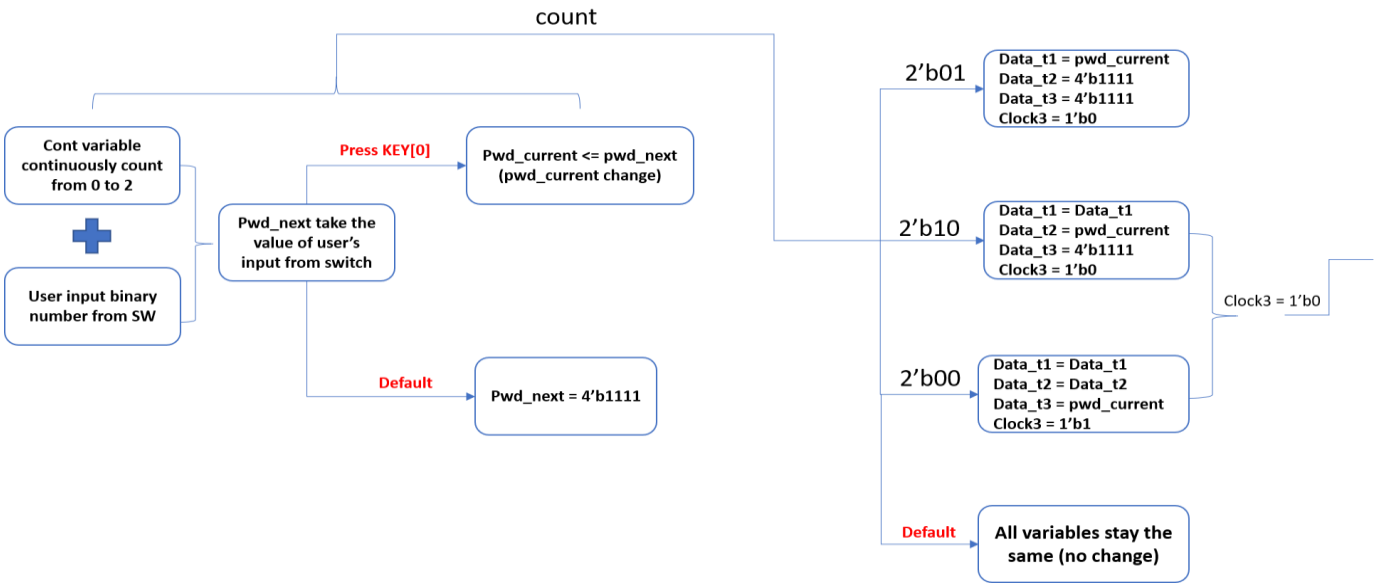


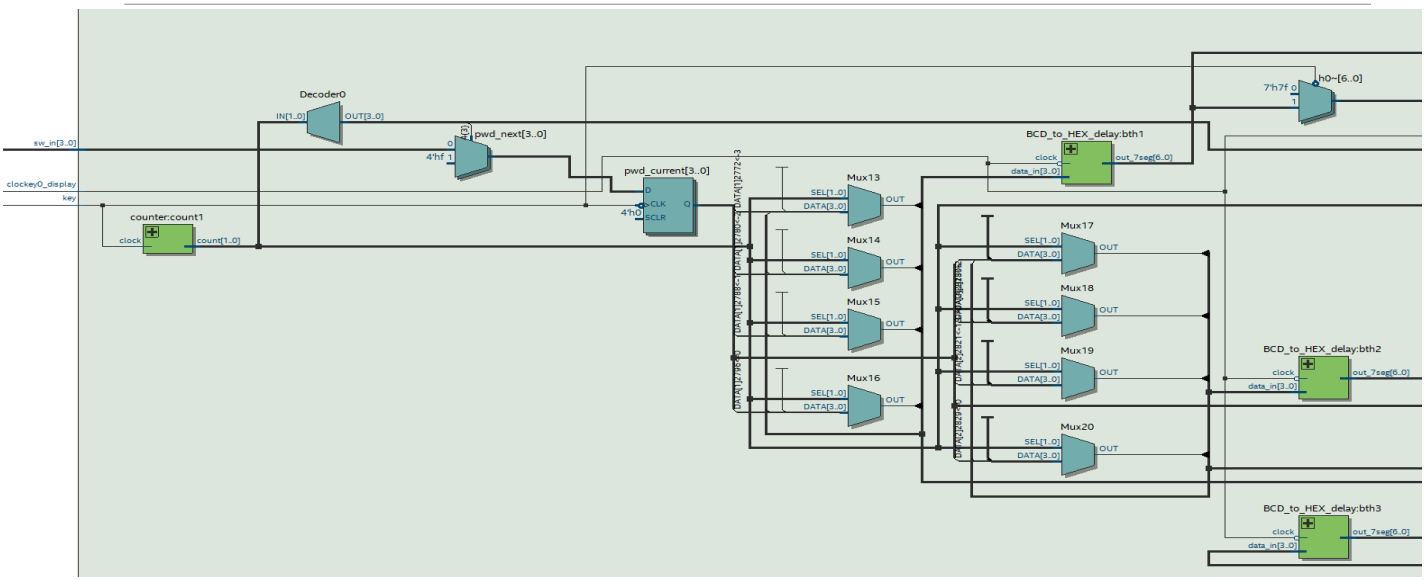
-Debounce_display:

When display the inputs to 7 segments LEDs, we have a problem that the 7 segments don't display the new inputs. So we make an debounce display to solve this problem.



-fsm_pwdinput:





7. Display:

When input right in verify mode:

Right inputs display to LEDG

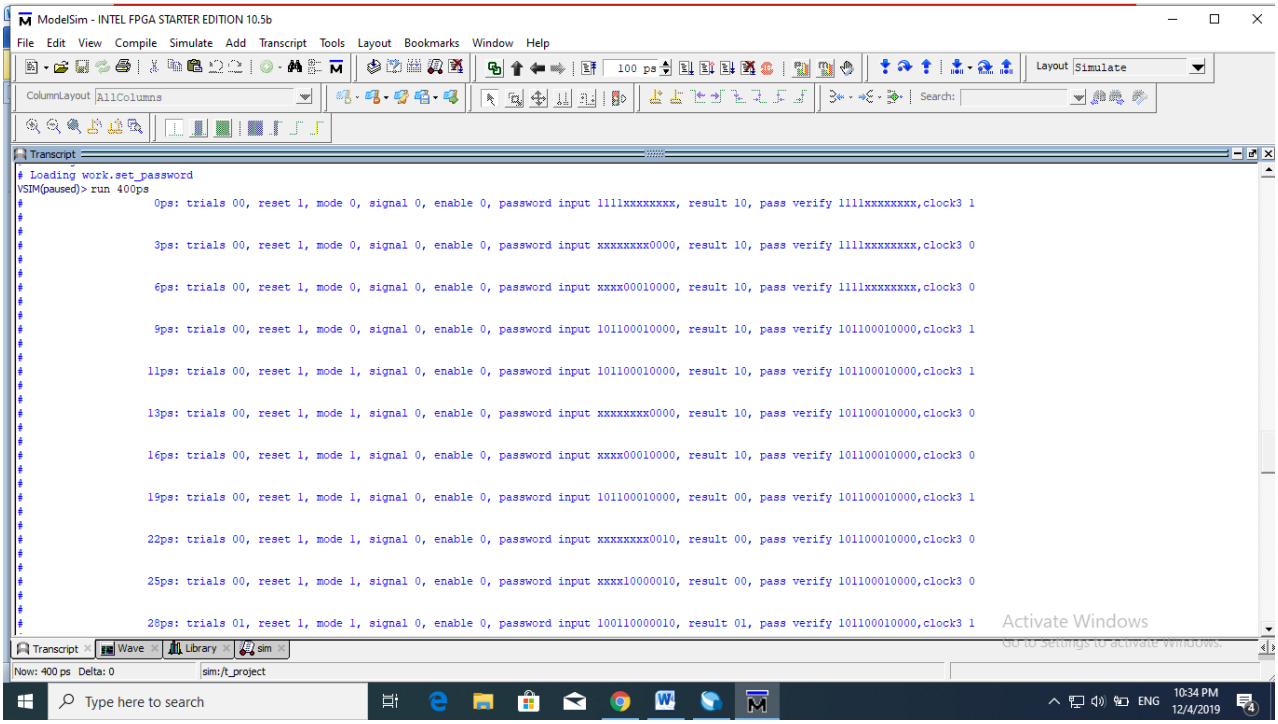
When input wrong in verify mode:

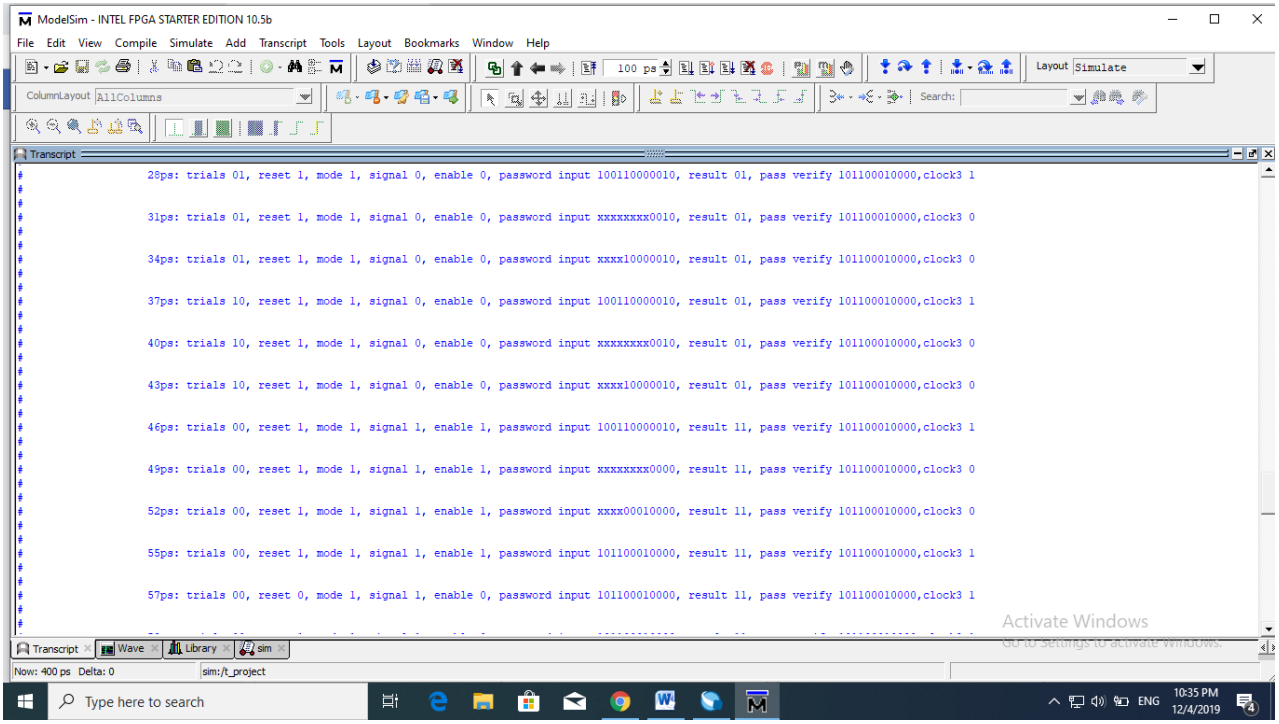
wrong input display to LEDR

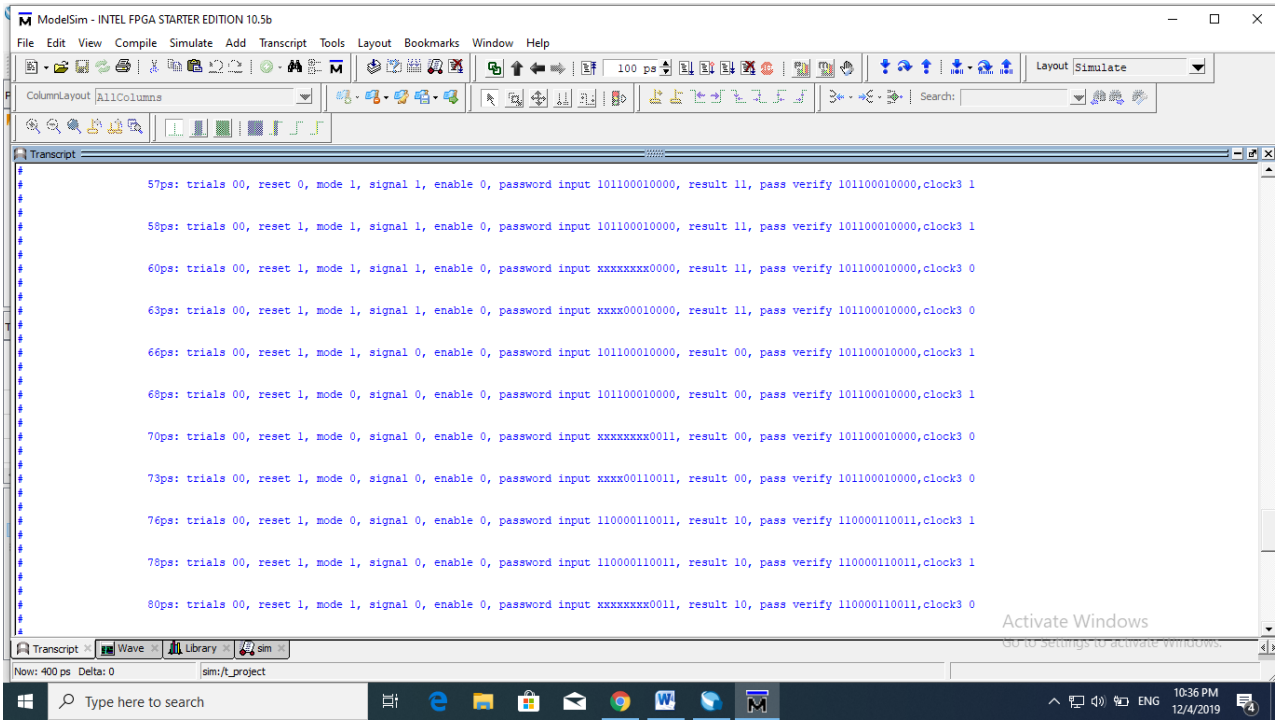
When input wrong 3 times and block:

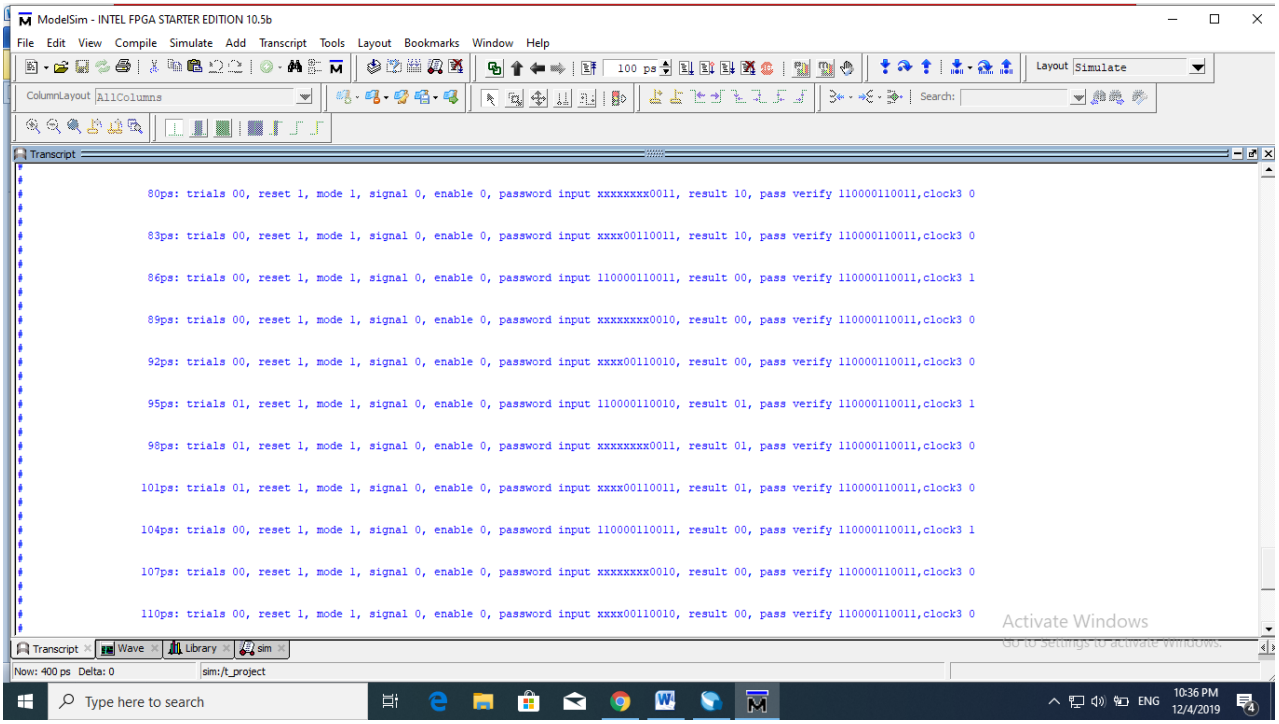
Block display to LEDR LEDG

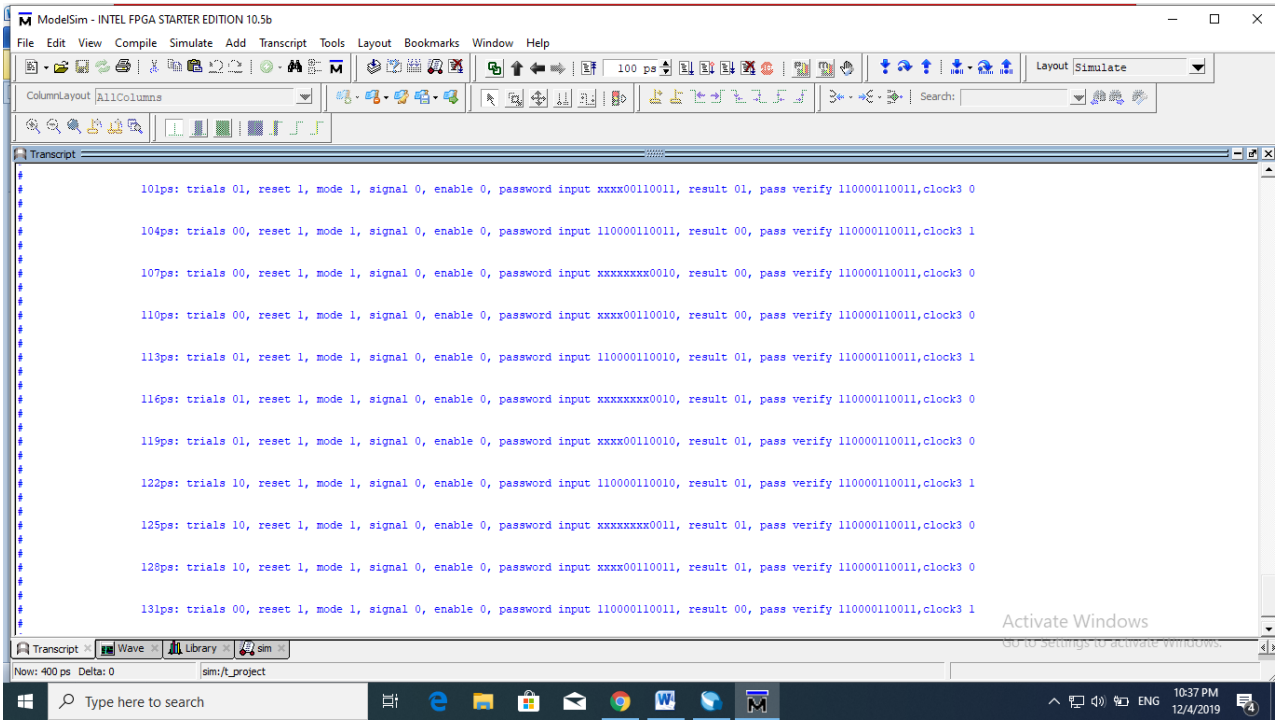
TESTBENCH AND ON-BOARD TEXT:


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
Loading work.set_password
VSIM(paused)> run 400ps
0ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input 1111xxxxxxxx, result 10, pass verify 1111xxxxxxxx,clock3 1
3ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input xxxxxxxx0000, result 10, pass verify 1111xxxxxxxx,clock3 0
6ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input xxxx00010000, result 10, pass verify 1111xxxxxxxx,clock3 0
9ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input 101100010000, result 10, pass verify 101100010000,clock3 1
11ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 101100010000, result 10, pass verify 101100010000,clock3 1
13ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0000, result 10, pass verify 101100010000,clock3 0
16ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx00010000, result 10, pass verify 101100010000,clock3 0
19ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 101100010000, result 00, pass verify 101100010000,clock3 1
22ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 00, pass verify 101100010000,clock3 0
25ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx10000010, result 00, pass verify 101100010000,clock3 0
28ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input 100110000010, result 01, pass verify 101100010000,clock3 1
Activate Windows
Transcript Wave Library sim
Now: 400 ps Delta: 0
sim:/t_project
Type here to search
ENG
10:34 PM
12/4/2019


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
28ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input 100110000010, result 01, pass verify 101100010000,clock3 1
31ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 01, pass verify 101100010000,clock3 0
34ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxx10000010, result 01, pass verify 101100010000,clock3 0
37ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input 100110000010, result 01, pass verify 101100010000,clock3 1
40ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 01, pass verify 101100010000,clock3 0
43ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input xxxx10000010, result 01, pass verify 101100010000,clock3 0
46ps: trials 00, reset 1, mode 1, signal 1, enable 1, password input 100110000010, result 11, pass verify 101100010000,clock3 1
49ps: trials 00, reset 1, mode 1, signal 1, enable 1, password input xxxxxxxx0000, result 11, pass verify 101100010000,clock3 0
52ps: trials 00, reset 1, mode 1, signal 1, enable 1, password input xxxx00010000, result 11, pass verify 101100010000,clock3 0
55ps: trials 00, reset 1, mode 1, signal 1, enable 1, password input 101100010000, result 11, pass verify 101100010000,clock3 1
57ps: trials 00, reset 0, mode 1, signal 1, enable 0, password input 101100010000, result 11, pass verify 101100010000,clock3 1
Activate Windows
Transcript Wave Library sim
Now: 400 ps Delta: 0
sim:/t_project
Type here to search
ENG
10:35 PM
12/4/2019


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Transcript
57ps: trials 00, reset 0, mode 1, signal 1, enable 0, password input 101100010000, result 11, pass verify 101100010000,clock3 1
58ps: trials 00, reset 1, mode 1, signal 1, enable 0, password input 101100010000, result 11, pass verify 101100010000,clock3 1
60ps: trials 00, reset 1, mode 1, signal 1, enable 0, password input xxxxxxxx0000, result 11, pass verify 101100010000,clock3 0
63ps: trials 00, reset 1, mode 1, signal 1, enable 0, password input xxxx00010000, result 11, pass verify 101100010000,clock3 0
66ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 101100010000, result 00, pass verify 101100010000,clock3 1
68ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input 101100010000, result 00, pass verify 101100010000,clock3 1
70ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input xxxxxxxx0011, result 00, pass verify 101100010000,clock3 0
73ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input xxxx00110011, result 00, pass verify 101100010000,clock3 0
76ps: trials 00, reset 1, mode 0, signal 0, enable 0, password input 110000110011, result 10, pass verify 110000110011,clock3 1
78ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 110000110011, result 10, pass verify 110000110011,clock3 1
80ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0011, result 10, pass verify 110000110011,clock3 0
Activate Windows
Transcript Wave Library sim
Now: 400 ps Delta: 0
sim:/t_project
Type here to search
ENG
10:36 PM
12/4/2019


ModelSim - INTEL FPGA STARTER EDITION 10.5b
80ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0011, result 10, pass verify 110000110011,clock3 0
83ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx00110011, result 10, pass verify 110000110011,clock3 0
86ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 110000110011, result 00, pass verify 110000110011,clock3 1
89ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 00, pass verify 110000110011,clock3 0
92ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx00110010, result 00, pass verify 110000110011,clock3 0
95ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input 110000110010, result 01, pass verify 110000110011,clock3 1
98ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0011, result 01, pass verify 110000110011,clock3 0
101ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxx00110011, result 01, pass verify 110000110011,clock3 0
104ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 110000110011, result 00, pass verify 110000110011,clock3 1
107ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 00, pass verify 110000110011,clock3 0
110ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx00110010, result 00, pass verify 110000110011,clock3 0
Activate Windows
Transcript
Wave
Library
sim
Now: 400 ps Delta: 0
sim:/t_project
Type here to search
ENG
10:36 PM
12/4/2019


ModelSim - INTEL FPGA STARTER EDITION 10.5b
101ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxx00110011, result 01, pass verify 110000110011,clock3 0
104ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 110000110011, result 00, pass verify 110000110011,clock3 1
107ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 00, pass verify 110000110011,clock3 0
110ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input xxxx00110010, result 00, pass verify 110000110011,clock3 0
113ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input 110000110010, result 01, pass verify 110000110011,clock3 1
116ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0010, result 01, pass verify 110000110011,clock3 0
119ps: trials 01, reset 1, mode 1, signal 0, enable 0, password input xxxx00110010, result 01, pass verify 110000110011,clock3 0
122ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input 110000110010, result 01, pass verify 110000110011,clock3 1
125ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input xxxxxxxx0011, result 01, pass verify 110000110011,clock3 0
128ps: trials 10, reset 1, mode 1, signal 0, enable 0, password input xxxx00110011, result 01, pass verify 110000110011,clock3 0
131ps: trials 00, reset 1, mode 1, signal 0, enable 0, password input 110000110011, result 00, pass verify 110000110011,clock3 1
Activate Windows
Transcript
Wave
Library
sim
Now: 400 ps Delta: 0
sim:/t_project
Type here to search
ENG
10:37 PM
12/4/2019

Test on board De2i-150:

test on board first time

test on board second time

CONCLUSION:

Advantage and disadvantage:

-Advantage:

Had already learn how to make a program with HDL

Had experience on working with De2i-150 board

-Disadvantage:

Having problem when using FSM

Debounce the noise signal

Phạm Thanh Danh	FSM Password Input De2i-150 Implementation Set_Password module Switch_Mode module Debounce_display module
Trần Nhựt Quang	Verify module Block module Display module Debounce module Testbench Simulation
Hồ Anh Tài	Slide Designer Report writer Design BCD_to_HEX_delay module
Lê Trần Minh Đức	Tester Basic concepts References