Houxuan Guo

hoesenguo@gmail.com | Chicago, IL

Education

- **Northwestern University** *Jan. 2024 – Present*
  Ph.D. Candidate, Computer Engineering Evanston, IL
  - Research focus: ASIC/FPGA Design for ML, Radiation-Hardened Electronics, Chip Design and Verification
- **Northwestern University** *Sep. 2022 – Dec. 2023*
  M.S., Electrical Engineering Evanston, IL
- **University of Shanghai for Science and Technology** *Sep. 2018 – Jun. 2022*
  B.E., Electrical Engineering Shanghai, China

Experience

- **Fermilab** *Jul. 2023 – Present*
  Visiting Researcher Batavia, IL
  - **Chip Bring-up & Validation:** Execute post-silicon bring-up and functional validation of the Cryo-AI ASIC's core logic and I/O subsystems for subsequent deployment in cryogenic environments.
  - **Framework Integration:** Architect a unified design and scalable verification platform, integrating hls4ml and ESP frameworks for scientific hardware accelerators.
  - **Physical Design:** Implement backend digital design flow for a photonic transmitter block, optimizing layout for signal integrity and area efficiency in a mixed-signal environment.

Research Projects

- **Stable On-Chip Backpropagation Framework** *Jun. 2024 – Present*
  - Developed "ENABOL", a C++ HLS flow to automate Python-to-RTL on-chip training, supporting gradient computation and weight updates for custom neural networks.
  - Implemented per-layer operator-norm projection under a global Lipschitz budget, ensuring fixed-point training stability.
  - Achieved stable on-chip training capabilities in hardware simulation while maintaining resource efficiency, allowing deployment on the same FPGA target (Paper submitted).
- **Fault-Tolerant Reconfigurable Design and Bitwise Reliability Analysis** *Jun. 2024 – May 2025*
  - Developed an automated Python toolchain that integrates Partial Triple Modular Redundancy (TMR) into the digital design flow to enhance circuit reliability without manual intervention.
  - Quantified the impact of redundancy on Power, Performance, and Area (PPA) through comprehensive synthesis and implementation trade-off analysis.
  - Developed a bitwise susceptibility analysis toolchain for neural network weights to mitigate Single Event Upsets (SEUs) in high-radiation environments (e.g., CERN LHC).
- **UVM Verification of Image Processing Accelerator and UDP Packet Parser** *Feb. 2024 – Mar. 2024*
  - Designed a Sobel edge detection module with grayscale conversion and a high-speed UDP packet parser (FIFO/FSM) for processing raw PCAP streams.
  - Built UVM testbench from the ground up, achieving 100% functional and code coverage for the Sobel edge detection module and the UDP parser.

Publications

C=Conference

[C.1] **H. Guo**, M. B. Valentín, X. He and S. Ogrenci, **"Toward Reconfigurable In-Pixel Computing: A Fault-Tolerant Design Flow for Machine Learning Accelerators,"** *2025 IEEE 33rd Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Fayetteville, AR, USA, 2025.

Skills

- **Hardware Design & Verification:** ASIC/SoC Design (RTL to GDSII), FPGA (Vivado/Vitis), HLS, UVM, SystemVerilog, Verilog
- **Languages & Scripting:** C/C++, Python, CUDA, Tcl, Embedded C, Bash, MATLAB
- **Machine Learning:** Deep Learning Architectures (CNNs, Transformers), Model Compression (Quantization, Pruning), PyTorch
- **EDA Tools:** Cadence (Genus, Innovus, Xcelium, Virtuoso), Synopsys (VCS, Design Compiler), Siemens (Catapult, Questa)
- **Languages:** English, French, Shanghainese, Mandarin