ALAN GUO

Evanston, IL | hoesenguo@gmail.com

EDUCATION

Northwestern University — Evanston, USA
- Doctor of Philosophy in Computer Engineering — Jan. 2024 – Present

Northwestern University — Evanston, USA
- Master of Science in Electrical Engineering — Sep. 2022 – Dec. 2023

University of Shanghai for Science and Technology — Shanghai, China
- Bachelor of Engineering in Electrical Engineering — Sep. 2018 – Jun. 2022

EXPERIENCE

ASIC Design and Test Engineer — Jul. 2023 – Present
Fermilab (Fermi National Accelerator Laboratory) — Batavia, USA
- Perform testing on Cryo-AI chip by ESP with Columbia University
- Design of SPROCKET3 ASIC chip with Fermilab ASIC Design Group
- Back-end digital flow for Photonic Transmitter block of including RTL, implementing floorplan and P&R

Research Assistant — Apr. 2023 – Present
Northwestern University (Seda Ogrenci Lab) — Evanston, USA
- Research on fault protection for bit-flips induced by radiations for neural network hardware accelerators, verifying, floorplanning, and P&R as full stack hardware design

Hardware Test Engineer — Jul. 2021 – Aug. 2021
Shanghai STEP Electric Corporation — Shanghai, China
- Tested various data against the diagrams of circuit boards and provided suggestions for the R&D department
- Designed schematic diagrams, conducted PCB reviews and component changes, and assisted in handling production and after-sales quality issues for future works

Software Engineering — Jul. 2020 – Aug. 2020
COMAC Software Co., Ltd. from Commercial Aircraft Corporation of China — Chengdu, China
- Development of an interview system in Java, solved permissions problems, and questioned banks accessing

RESEARCH

Fault-Tolerant Reconfigurable In-Pixel AI Computing Design Flow — Jun. 2024 – Present
- Develop TMR (modular redundancy) workflow scripts for backend design tools,

NetSuRF: Bitwise Susceptibility Ranking for Edge Neural Networks — Jun. 2024 – Nov. 2024
- Develop algorithms for ranking weights in ASIC based on-edge neural networks for radiation induced environments like LHC at CERN
- Integrate the algorithms with ASIC related hardware and go through back-end digital flow, ready for tape-out

UTV (Utility Task Vehicle) Design — Mar. 2021 – Jun. 2022
Shanghai University Student Innovation and Entrepreneurship Project, Team Leader
- Design and solder H-bridge PCB circuit, program embedded C in STM32 for controlling the vehicle and motor
- Combine STM32 with a self-designed DC brush drive board and a high-power motor to assemble the vehicle

ADDITIONAL

Skills: Linux, HLS, Digital Logic Design, Analog Circuit Design, (System) Verilog RTL, UVM Verification, Computer Architecture, CUDA, Machine Learning, Python, C, C++, PCB Design, Web Design

Languages: English, Mandarin, Shanghainese

Hobbies: Violin (at Northwestern University Philharmonia and played for over 20 years)