Laboratory Project 1

32-bit ALU

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Objective

The purpose of this laboratory project is to implement a 32-bit arithmetic and logic unit (ALU) using behaviorally modelled VHDL. Figure 1 illustrates the objective.

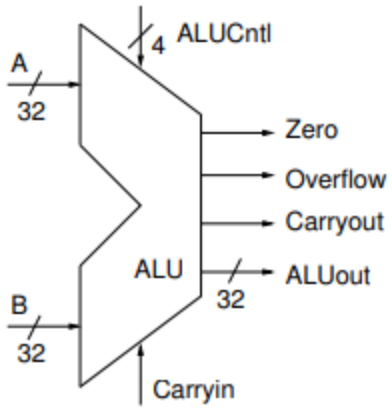


Figure 1: Objective arithmetic and logic unit

The ALU is to implement operations AND, OR, XOR, addition, subtraction, and NOR corresponding to the control signals defined in Table 1.

ALUCntrl	Function
0000	AND
0001	OR
0011	XOR
0010	Add
0110	Subtract
1100	NOR

Table 1: ALU control signals and corresponding operations

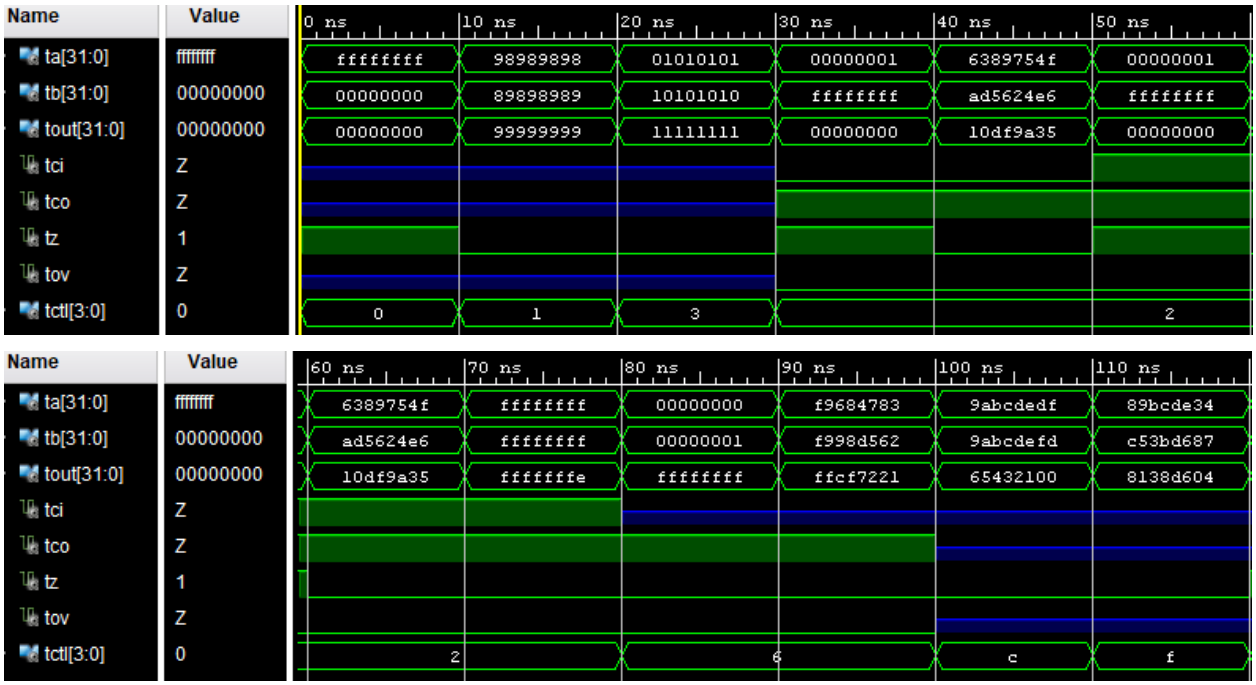
Calculations

Given the twelve test cases in Table 2, the ALU simulation ought to produce the calculated values. Note the ALU specification includes a carry-in, but this value is never used and affects neither arithmetic nor logic.

A_{16}	B_{16}	Carryin	ALUCntl	$ALUout_{16}$	Zero	Overflow	Carryout
FFFFFFFF	00000000	0	0000	00000000	1	Z	Z
98989898	89898989	0	0001	99999999	0	Z	Z
01010101	10101010	0	0011	11111111	0	Z	Z
00000001	FFFFFFFF	0	0010	00000000	1	0	1
6389754F	AD5624E6	0	0010	10DF9A35	0	0	1
00000001	FFFFFFFF	1	0010	00000000	1	0	1
6389754F	AD5624E6	1	0010	10DF9A35	0	0	1
FFFFFFFF	FFFFFFFF	1	0010	FFFFFFFE	0	0	1
00000000	00000001	0	0110	FFFFFFFF	0	0	1
F9684783	F998D562	0	0110	FFCF7221	0	0	1
9ABCDEDF	9ABCDEFD	0	1100	65432100	0	Z	Z
89BCDE34	C53BD687	0	1111	8138D604	0	Z	Z

Table 2: Test vectors and calculated expectations

Simulation



Figures 3 and 4: Simulated waveform of the ALU under the test conditions specified in Table 2

Results

The ALU was implemented to specifications and the simulation waveforms match the calculated results for the port ALUout and flags for zero, carryout, and overflow.