CORTEX NXP1769: HOJAS DE DATOS PARA LA REALIZACIÓN DE EXÁMENES DE INFO II

Acceso a Hardware

PINSEL0 to PINSEL9 Values	Function
00	Primary (default) function, typically GPIO port
01	First alternate function
10	Second alternate function
11	Third alternate function

PINMODE_OD0 to PINMODE_OD4 Values	Function
0	Pin is in the normal (not open drain) mode.
1	Pin is in the open drain mode.

PINMODE0 to PINMODE9 Values	Function
00	Pin has an on-chip pull-up resistor enabled.
01	Repeater mode
10	Pin has neither pull-up nor pull-down resistor enabled.
11	Pin has an on-chip pull-down resistor enabled.

Register	Controls	
PINSEL0	P0[15:0]	
PINSEL1	P0 [31:16]	
PINSEL2	P1 [15:0] (Ethernet)	
PINSEL3	P1 [31:16]	
PINSEL4	P2 [15:0]	
PINSEL5	P2 [31:16]	not used
PINSEL6	P3 [15:0]	not used
PINSEL7	P3 [31:16]	
PINSEL8	P4 [15:0]	not used
PINSEL9	P4 [31:16]	
PINSEL10	Trace port enable	

Name	Description	Access	Reset Value[1]	Address
PINSEL0	Pin function select register 0.	R/W	0	0x4002 C000
PINSEL1	Pin function select register 1.	R/W	0	0x4002 C004
PINSEL2	Pin function select register 2.	R/W	0	0x4002 C008
PINSEL3	Pin function select register 3.	R/W	0	0x4002 C00C
PINSEL4	Pin function select register 4	R/W	0	0x4002 C010
PINSEL7	Pin function select register 7	R/W	0	0x4002 C01C
PINSEL8	Pin function select register 8	R/W	0	0x4002 C020
PINSEL9	Pin function select register 9	R/W	0	0x4002 C024
PINSEL10	Pin function select register 10	R/W	0	0x4002 C028
PINMODE0	Pin mode select register 0	R/W	0	0x4002 C040
PINMODE1	Pin mode select register 1	R/W	0	0x4002 C044
PINMODE2	Pin mode select register 2	R/W	0	0x4002 C048
PINMODE3	Pin mode select register 3.	R/W	0	0x4002 C04C
PINMODE4	Pin mode select register 4	R/W	0	0x4002 C050
PINMODE5	Pin mode select register 5	R/W	0	0x4002 C054
PINMODE6	Pin mode select register 6	R/W	0	0x4002 C058
PINMODE7	Pin mode select register 7	R/W	0	0x4002 C05C
PINMODE9	Pin mode select register 9	R/W	0	0x4002 C064
PINMODE_OD0	Open drain mode control register 0	R/W	0	0x4002 C068
PINMODE_OD1	Open drain mode control register 1	R/W	0	0x4002 C06C
PINMODE_OD2	Open drain mode control register 2	R/W	0	0x4002 C070
PINMODE_OD3	Open drain mode control register 3	R/W	0	0x4002 C074
PINMODE_OD4	Open drain mode control register 4	R/W	0	0x4002 C078
I2CPADCFG	I2C Pin Configuration register	R/W	0	0x4002 C07C

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

- void   SetPINSEL (uint8_t puerto, uint8_t pin, uint8_t modo)
- void   SetPINMODE(uint8_t port, uint8_t pin, uint8_t modo)
- void   SetDIR(uint32_t* puerto, uint8_t pin, uint8_t direccion)
- void   SetPIN(uint32_t* puerto, uint8_t pin, uint8_t estado)
- uint8_t GetPIN(uint8_t puerto, uint8_t pin, uint8_t actividad)

Mapa de las G PIO del LPC1769

Table 101. GPIO register map (local bus accessible registers - enhanced GPIO features)

	Generic Name	Description	Access	Reset value[1]	PORTn Register Name & Address
Establezco Dirección (0 = entrada 1 = salida)	FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
máscara (0 = enable)	FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090
Lectura/escritura de pin (FIOMASK = 0, todo habilitado)	FIOPIN	Fast Port Pin value register using FIOMASK. The current state of digital port pins can be read from this register, regardless of pin direction or alternate function selection (as long as pins are not configured as an input to ADC). The value read is masked by ANDing with inverted FIOMASK. Writing to this register places corresponding values in all bits enabled by zeros in FIOMASK. **Important:** if an FIOPIN register is read, its bit(s) masked with 1 in the FIOMASK register will be read as 0 regardless of the physical pin state.	R/W	0	FIO0PIN - 0x2009 C014 FIO1PIN - 0x2009 C034 FIO2PIN - 0x2009 C054 FIO3PIN - 0x2009 C074 FIO4PIN - 0x2009 C094
Con un "1" Escribo un 1	FIOSET	Fast Port Output Set register using FIOMASK. This register controls the state of output pins. Writing 1s produces highs at the corresponding port pins. Writing 0s has no effect. Reading this register returns the current contents of the port output register. Only bits enabled by 0 in FIOMASK can be altered.	R/W	0	FIO0SET - 0x2009 C018 FIO1SET - 0x2009 C038 FIO2SET - 0x2009 C058 FIO3SET - 0x2009 C078 FIO4SET - 0x2009 C098
Con un "1" escribo un 0	FIOCLR	Fast Port Output Clear register using FIOMASK. This register controls the state of output pins. Writing 1s produces lows at the corresponding port pins. Writing 0s has no effect. Only bits enabled by 0 in FIOMASK can be altered.	WO	0	FIO0CLR - 0x2009 C01C FIO1CLR - 0x2009 C03C FIO2CLR - 0x2009 C05C FIO3CLR - 0x2009 C07C FIO4CLR - 0x2009 C09C

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Registros PINSEL

Table 79.   Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	AD0.7	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	AD0.6	Reserved	00
9:8	P0.4[1]	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5[1]	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00
29:24	-	Reserved	Reserved	Reserved	Reserved	0
31:30	P0.15	GPIO Port 0.15	TXD1	SCK0	SCK	00

Table 80.   Pin function select register 1 (PINSEL1 - address 0x4002 C004) bit description

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.16	GPIO Port 0.16	RXD1	SSEL0	SSEL	00
3:2	P0.17	GPIO Port 0.17	CTS1	MISO0	MISO	00
5:4	P0.18	GPIO Port 0.18	DCD1	MOSI0	MOSI	00
7:6	P0.19[1]	GPIO Port 0.19	DSR1	Reserved	SDA1	00
9:8	P0.20[1]	GPIO Port 0.20	DTR1	Reserved	SCL1	00
11:10	P0.21[1]	GPIO Port 0.21	RI1	Reserved	RD1	00
13:12	P0.22	GPIO Port 0.22	RTS1	Reserved	TD1	00
15:14	P0.23[1]	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24[1]	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00
19:18	P0.25	GPIO Port 0.25	AD0.2	I2SRX_SDA	TXD3	00
21:20	P0.26	GPIO Port 0.26	AD0.3	AOUT	RXD3	00
23:22	P0.27[1][2]	GPIO Port 0.27	SDA0	USB_SDA	Reserved	00
25:24	P0.28[1][2]	GPIO Port 0.28	SCL0	USB_SCL	Reserved	00
27:26	P0.29	GPIO Port 0.29	USB_D+	Reserved	Reserved	00
29:28	P0.30	GPIO Port 0.30	USB_D-	Reserved	Reserved	00
31:30	-	Reserved	Reserved	Reserved	Reserved	00

Table 81.   Pin function select register 2 (PINSEL2 - address 0x4002 C008) bit description

PINSEL2	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.0	GPIO Port 1.0	ENET_TXD0	Reserved	Reserved	00
3:2	P1.1	GPIO Port 1.1	ENET_TXD1	Reserved	Reserved	00
7:4	-	Reserved	Reserved	Reserved	Reserved	0
9:8	P1.4	GPIO Port 1.4	ENET_TX_EN	Reserved	Reserved	00
15:10	-	Reserved	Reserved	Reserved	Reserved	0
17:16	P1.8	GPIO Port 1.8	ENET_CRS	Reserved	Reserved	00
19:18	P1.9	GPIO Port 1.9	ENET_RXD0	Reserved	Reserved	00
21:20	P1.10	GPIO Port 1.10	ENET_RXD1	Reserved	Reserved	00
27:22	-	Reserved	Reserved	Reserved	Reserved	0
29:28	P1.14	GPIO Port 1.14	ENET_RX_ER	Reserved	Reserved	00
31:30	P1.15	GPIO Port 1.15	ENET_REF_CLK	Reserved	Reserved	00

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Table 82. Pin function select register 3 (PINSEL3 - address 0x4002 C00C) bit description

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.16[1]	GPIO Port 1.16	ENET_MDC	Reserved	Reserved	00
3:2	P1.17[1]	GPIO Port 1.17	ENET_MDIO	Reserved	Reserved	00
5:4	P1.18	GPIO Port 1.18	USB_UP_LED	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	MCOA0	USB_PPWR	CAP1.1	00
9:8	P1.20	GPIO Port 1.20	MCI0	PWM1.2	SCK0	00
11:10	P1.21[1]	GPIO Port 1.21	MCABORT	PWM1.3	SSEL0	00
13:12	P1.22	GPIO Port 1.22	MCOB0	USB_PWRD	MAT1.0	00
15:14	P1.23	GPIO Port 1.23	MCI1	PWM1.4	MISO0	00
17:16	P1.24	GPIO Port 1.24	MCI2	PWM1.5	MOSI0	00
19:18	P1.25	GPIO Port 1.25	MCOA1	Reserved	MAT1.1	00
21:20	P1.26	GPIO Port 1.26	MCOB1	PWM1.6	CAP0.0	00
23:22	P1.27[1]	GPIO Port 1.27	CLKOUT	USB_OVRCR	CAP0.1	00
25:24	P1.28	GPIO Port 1.28	MCOA2	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	MCOB2	PCAP1.1	MAT0.1	00
29:28	P1.30	GPIO Port 1.30	Reserved	V_{BUS}	AD0.4	00
31:30	P1.31	GPIO Port 1.31	Reserved	SCK1	AD0.5	00

Table 83. Pin function select register 4 (PINSEL4 - address 0x4002 C010) bit description

PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.0	GPIO Port 2.0	PWM1.1	TXD1	Reserved	00
3:2	P2.1	GPIO Port 2.1	PWM1.2	RXD1	Reserved	00
5:4	P2.2	GPIO Port 2.2	PWM1.3	CTS1	Reserved [2]	00
7:6	P2.3	GPIO Port 2.3	PWM1.4	DCD1	Reserved [2]	00
9:8	P2.4	GPIO Port 2.4	PWM1.5	DSR1	Reserved [2]	00
11:10	P2.5	GPIO Port 2.5	PWM1.6	DTR1	Reserved [2]	00
13:12	P2.6	GPIO Port 2.6	PCAP1.0	RI1	Reserved [2]	00
15:14	P2.7	GPIO Port 2.7	RD2	RTS1	Reserved	00
17:16	P2.8	GPIO Port 2.8	TD2	TXD2	ENET_MDC	00
19:18	P2.9	GPIO Port 2.9	USB_CONNECT	RXD2	ENET_MDIO	00
21:20	P2.10	GPIO Port 2.10	EINT0	NMI	Reserved	00
23:22	P2.11[1]	GPIO Port 2.11	EINT1	Reserved	I2STX_CLK	00
25:24	P2.12[1]	GPIO Port 2.12	EINT2	Reserved	I2STX_WS	00
27:26	P2.13[1]	GPIO Port 2.13	EINT3	Reserved	I2STX_SDA	00
31:28	-	Reserved	Reserved	Reserved	Reserved	0

Table 84. Pin function select register 7 (PINSEL7 - address 0x4002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
17:0	-	Reserved	Reserved	Reserved	Reserved	0
19:18	P3.25[1]	GPIO Port 3.25	Reserved	MAT0.0	PWM1.2	00
21:20	P3.26[1]	GPIO Port 3.26	STCLK	MAT0.1	PWM1.3	00
31:22	-	Reserved	Reserved	Reserved	Reserved	0

Table 85. Pin function select register 9 (PINSEL9 - address 0x4002 C024) bit description

PINSEL9	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
23:0	-	Reserved	Reserved	Reserved	Reserved	00
25:24	P4.28	GPIO Port 4.28	RX_MCLK	MAT2.0	TXD3	00
27:26	P4.29	GPIO Port 4.29	TX_MCLK	MAT2.1	RXD3	00
31:28	-	Reserved	Reserved	Reserved	Reserved	00

Interrupciones: NVIC

Table 51. NVIC register map

Name	Description	Access	Reset value	Address
ISER0 to ISER1	Interrupt Set-Enable Registers. These 2 registers allow enabling interrupts and reading back the interrupt enables for specific peripheral functions.	RW	0	ISER0 - 0xE000 E100 ISER1 - 0xE000 E104
ICER0 to ICER1	Interrupt Clear-Enable Registers. These 2 registers allow disabling interrupts and reading back the interrupt enables for specific peripheral functions.	RW	0	ICER0 - 0xE000 E180 ICER1 - 0xE000 E184
ISPR0 to ISPR1	Interrupt Set-Pending Registers. These 2 registers allow changing the interrupt state to pending and reading back the interrupt pending state for specific peripheral functions.	RW	0	ISPR0 - 0xE000 E200 ISPR1 - 0xE000 E204
ICPR0 to ICPR1	Interrupt Clear-Pending Registers. These 2 registers allow changing the interrupt state to not pending and reading back the interrupt pending state for specific peripheral functions.	RW	0	ICPR0 - 0xE000 E280 ICPR1 - 0xE000 E284
IABR0 to IABR1	Interrupt Active Bit Registers. These 2 registers allow reading the current interrupt active state for specific peripheral functions.	RO	0	IABR0 - 0xE000 E300 IABR1 - 0xE000 E304

Table 52. Interrupt Set-Enable Register 0 register (ISER0 - 0xE000 E100)

Bit	Name	Function
0	ISE_WDT	Watchdog Timer Interrupt Enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.
1	ISE_TIMER0	Timer 0 Interrupt Enable. See functional description for bit 0.
2	ISE_TIMER1	Timer 1. Interrupt Enable. See functional description for bit 0.
3	ISE_TIMER2	Timer 2 Interrupt Enable. See functional description for bit 0.
4	ISE_TIMER3	Timer 3 Interrupt Enable. See functional description for bit 0.
5	ISE_UART0	UART0 Interrupt Enable. See functional description for bit 0.
6	ISE_UART1	UART1 Interrupt Enable. See functional description for bit 0.
7	ISE_UART2	UART2 Interrupt Enable. See functional description for bit 0.
8	ISE_UART3	UART3 Interrupt Enable. See functional description for bit 0.
9	ISE_PWM	PWM1 Interrupt Enable. See functional description for bit 0.
10	ISE_I2C0	I2C0 Interrupt Enable. See functional description for bit 0.
11	ISE_I2C1	I2C1 Interrupt Enable. See functional description for bit 0.
12	ISE_I2C2	I2C2 Interrupt Enable. See functional description for bit 0.
13	ISE_SPI	SPI Interrupt Enable. See functional description for bit 0.
14	ISE_SSP0	SSP0 Interrupt Enable. See functional description for bit 0.
15	ISE_SSP1	SSP1 Interrupt Enable. See functional description for bit 0.
16	ISE_PLL0	PLL0 (Main PLL) Interrupt Enable. See functional description for bit 0.
17	ISE_RTC	Real Time Clock (RTC) Interrupt Enable. See functional description for bit 0.
18	ISE_EINT0	External Interrupt 0 Interrupt Enable. See functional description for bit 0.
19	ISE_EINT1	External Interrupt 1 Interrupt Enable. See functional description for bit 0.
20	ISE_EINT2	External Interrupt 2 Interrupt Enable. See functional description for bit 0.
21	ISE_EINT3	External Interrupt 3 Interrupt Enable. See functional description for bit 0.
22	ISE_ADC	ADC Interrupt Enable. See functional description for bit 0.
23	ISE_BOD	BOD Interrupt Enable. See functional description for bit 0.
24	ISE_USB	USB Interrupt Enable. See functional description for bit 0.
25	ISE_CAN	CAN Interrupt Enable. See functional description for bit 0.
26	ISE_DMA	GPDMA Interrupt Enable. See functional description for bit 0.
27	ISE_I2S	I2S Interrupt Enable. See functional description for bit 0.
28	ISE_ENET	Ethernet Interrupt Enable. See functional description for bit 0.
29	ISE_RIT	Repetitive Interrupt Timer Interrupt Enable. See functional description for bit 0.
30	ISE_MCPWM	Motor Control PWM Interrupt Enable. See functional description for bit 0.
31	ISE_QEI	Quadrature Encoder Interface Interrupt Enable. See functional description for bit 0.

```
         void ResetISR(void);
WEAK void NMI_Handler(void);
WEAK void HardFault_Handler(void);
WEAK void MemManage_Handler(void);
WEAK void BusFault_Handler(void);
WEAK void UsageFault_Handler(void);
WEAK void SVCall_Handler(void);
WEAK void DebugMon_Handler(void);
WEAK void PendSV_Handler(void);
WEAK void SysTick_Handler(void);
WEAK void IntDefaultHandler(void);
```

```
void TIMER0_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER1_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER2_IRQHandler(void) ALIAS(IntDefaultHandler);
void TIMER3_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART0_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART1_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART2_IRQHandler(void) ALIAS(IntDefaultHandler);
void UART3_IRQHandler(void) ALIAS(IntDefaultHandler);
void PWM1_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C0_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C1_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2C2_IRQHandler(void) ALIAS(IntDefaultHandler);
void SPI_IRQHandler(void) ALIAS(IntDefaultHandler);
void SSP0_IRQHandler(void) ALIAS(IntDefaultHandler);
void SSP1_IRQHandler(void) ALIAS(IntDefaultHandler);
void PLL0_IRQHandler(void) ALIAS(IntDefaultHandler);
void RTC_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT0_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT1_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT2_IRQHandler(void) ALIAS(IntDefaultHandler);
void EINT3_IRQHandler(void) ALIAS(IntDefaultHandler);
void ADC_IRQHandler(void) ALIAS(IntDefaultHandler);
void BOD_IRQHandler(void) ALIAS(IntDefaultHandler);
void USB_IRQHandler(void) ALIAS(IntDefaultHandler);
void CAN_IRQHandler(void) ALIAS(IntDefaultHandler);
void DMA_IRQHandler(void) ALIAS(IntDefaultHandler);
void I2S_IRQHandler(void) ALIAS(IntDefaultHandler);
void ENET_IRQHandler(void) ALIAS(IntDefaultHandler);
void RIT_IRQHandler(void) ALIAS(IntDefaultHandler);
void MCPWM_IRQHandler(void) ALIAS(IntDefaultHandler);
void QEI_IRQHandler(void) ALIAS(IntDefaultHandler);
void PLL1_IRQHandler(void) ALIAS(IntDefaultHandler);
void USBActivity_IRQHandler(void) ALIAS(IntDefaultHand
```

Interrupciones. Externas

Table 9. External Interrupt registers

Name	Description	Access	Reset value[1]
EXTINT	The External Interrupt Flag Register contains interrupt flags for EINT0, EINT1, EINT2 and EINT3. See Table 10.	R/W	0x00
EXTMODE	The External Interrupt Mode Register controls whether each pin is edge- or level-sensitive. See Table 11.	R/W	0x00
EXTPOLAR	The External Interrupt Polarity Register controls which level or edge on each pin will cause an interrupt. See Table 12.	R/W	0x00

Table 11. External Interrupt Mode register (EXTMODE - address description

Bit	Symbol	Value	Description
0	EXTMODE0	0	Level-sensitivity is selected for $\overline{EINT0}$.
		1	$\overline{EINT0}$ is edge sensitive.
1	EXTMODE1	0	Level-sensitivity is selected for $\overline{EINT1}$.
		1	$\overline{EINT1}$ is edge sensitive.
2	EXTMODE2	0	Level-sensitivity is selected for $\overline{EINT2}$.
		1	$\overline{EINT2}$ is edge sensitive.
3	EXTMODE3	0	Level-sensitivity is selected for $\overline{EINT3}$.
		1	$\overline{EINT3}$ is edge sensitive.
31:4	-	-	Reserved, user software should not write bits. The value read from a reserved bit i

**Table 10. External Interrupt Flag register (EXTINT - address 0x400F C140) bit description**

Bit	Symbol	Description	Reset value
0	EINT0	In level-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
1	EINT1	In level-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
2	EINT2	In level-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
3	EINT3	In level-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the selected edge occurs on the pin. This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 12. External Interrupt Polarity register (EXTPOLAR - address 0x400F C14C) bit description

Bit	Symbol	Value	Description	Reset value
0	EXTPOLAR0	0	EINT0 is low-active or falling-edge sensitive (depending on EXTMODE0).	0
		1	EINT0 is high-active or rising-edge sensitive (depending on EXTMODE0).	
1	EXTPOLAR1	0	EINT1 is low-active or falling-edge sensitive (depending on EXTMODE1).	0
		1	EINT1 is high-active or rising-edge sensitive (depending on EXTMODE1).	
2	EXTPOLAR2	0	EINT2 is low-active or falling-edge sensitive (depending on EXTMODE2).	0
		1	EINT2 is high-active or rising-edge sensitive (depending on EXTMODE2).	
3	EXTPOLAR3	0	EINT3 is low-active or falling-edge sensitive (depending on EXTMODE3).	0
		1	EINT3 is high-active or rising-edge sensitive (depending on EXTMODE3).	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Interrupciones Externas en Infotronic
Implementación

Interrupción EXTERNA	Puerto	Infotronic	Función
EINT0	P210	SW1	KEY0
EINT1	P211	ENT.DIG2	BORNERA
EINT2	P212	EXPANSION 17	DIP2_2
EINT3	P213	SW4	KEY3

Systick

Timer descendente de 24 bits

STCTRL

COUNTFLAG CLKSOURCE TICKINT ENABLE
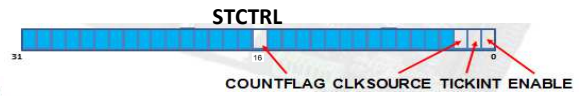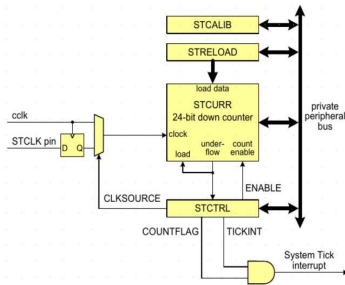
Table 438. System Tick Timer register map

Name	Description	Access	Reset value[1]	Address
STCTRL	System Timer Control and status register	R/W	0x4	0xE000 E010
STRELOAD	System Timer Reload value register	R/W	0	0xE000 E014
STCURR	System Timer Current value register	R/W	0	0xE000 E018
STCALIB	System Timer Calibration value register	R/W	0x000F 423F	0xE000 E01C

Clock por defecto: Interno (CCLK)
Si se elige clock externo: STCLK (P3.26) => Seleccionar al pin STCLK en el registro pinMode

STRELOAD = (STCALIB / N) - 1 ☞ Si N=1 ➔ tick cada 10ms. (si clock=100Mhz)

Power Control for Periphericals

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

PCONP

Bit	Symbol	Description	Reset value
0	-	Reserved.	NA
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Reserved.	NA
6	PCPWM1	PWM1 power/clock control bit.	1
7	PCI2C0	The I2C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP 1 interface power/clock control bit.	1
11	-	Reserved.	NA
12	PCADC	A/D converter (ADC) power/clock control bit. Note: Clear the PDN bit in the AD0CR before clearing this bit, and set this bit before setting PDN.	0
13	PCCAN1	CAN Controller 1 power/clock control bit.	0
14	PCCAN2	CAN Controller 2 power/clock control bit.	0
15	PCGPIO	Power/clock control bit for IOCON, GPIO, and GPIO interrupts.	1
16	PCRIT	Repetitive Interrupt Timer power/clock control bit.	0

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

PCONP

Bit	Symbol	Description	Reset value
17	PCMCPWM	Motor Control PWM	0
18	PCQEI	Quadrature Encoder Interface power/clock control bit.	0
19	PCI2C1	The I2C1 interface power/clock control bit.	1
20	-	Reserved.	NA
21	PCSSP0	The SSP0 interface power/clock control bit.	1
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I2C interface 2 power/clock control bit.	1
27	PCI2S	I2S interface power/clock control bit.	0
28	-	Reserved.	NA
29	PCGPDMA	GPDMA function power/clock control bit.	0
30	PCENET	Ethernet block power/clock control bit.	0
31	PCUSB	USB interface power/clock control bit.	0

Peripherical Clock Seleccion Register

Table 40. Peripheral Clock Selection register 0 (PCLKSEL0 - address 0x400F C1A8) bit description

PCLKSEL0

Bit	Symbol	Description	Reset value
1:0	PCLK_WDT	Peripheral clock selection for WDT.	00
3:2	PCLK_TIMER0	Peripheral clock selection for TIMER0.	00
5:4	PCLK_TIMER1	Peripheral clock selection for TIMER1.	00
7:6	PCLK_UART0	Peripheral clock selection for UART0.	00
9:8	PCLK_UART1	Peripheral clock selection for UART1.	00
11:10	-	Reserved.	NA
13:12	PCLK_PWM1	Peripheral clock selection for PWM1.	00
15:14	PCLK_I2C0	Peripheral clock selection for I2C0.	00
17:16	PCLK_SPI	Peripheral clock selection for SPI.	00
19:18	-	Reserved.	NA
21:20	PCLK_SSP1	Peripheral clock selection for SSP1.	00
23:22	PCLK_DAC	Peripheral clock selection for DAC.	00
25:24	PCLK_ADC	Peripheral clock selection for ADC.	00

Table 42. Peripheral Clock Selection register bit values

PCLKSEL0 and PCLKSEL1 individual peripheral's clock select options	Function	Reset value
00	PCLK_peripheral = CCLK/4	00
01	PCLK_peripheral = CCLK	
10	PCLK_peripheral = CCLK/2	
11	PCLK_peripheral = CCLK/8, except for CAN1, CAN2, and CAN filtering when "11" selects = CCLK/6.	
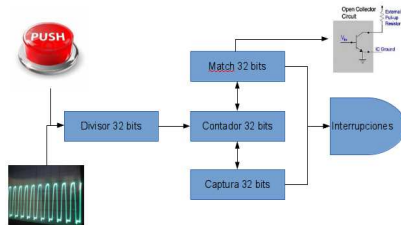
Timers

• 2 canales de captura, que sacan una foto del timer ante una transición de una entrada. Puede generar, en forma opcional, una interrupción.

• Cuatro registros de match de 32-bit que permiten:

– Operación contínua con generación opcional de interrupción on match.

– Frena timer on match con interrupción opcional.

– Reset timer on match interrupción opcional.

• Hasta cuatro salidas externas correspondientes a los registros de match con las siguientes capacidades:

– Set low on match.

– Set high on match.

– Toggle on match.

– No hace nada on match.

Mapa de Registros ///resumen\\\

Table 425. TIMER/COUNTER0-3 register map

Generic Name	Description	Access	Reset Value[1]	TIMERn Register/ Name & Address
IR	Interrupt Register. The IR can be written to clear interrupts. The IR can be read to identify which of eight possible interrupt sources are pending.	R/W	0	T0IR - 0x4000 4000 T1IR - 0x4000 8000 T2IR - 0x4009 0000 T3IR - 0x4009 4000
TCR	Timer Control Register. The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	R/W	0	T0TCR - 0x4000 4004 T1TCR - 0x4000 8004 T2TCR - 0x4009 0004 T3TCR - 0x4009 4004
TC	Timer Counter. The 32-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	R/W	0	T0TC - 0x4000 4008 T1TC - 0x4000 8008 T2TC - 0x4009 0008 T3TC - 0x4009 4008
MCR	Match Control Register. The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	R/W	0	T0MCR - 0x4000 4014 T1MCR - 0x4000 8014 T2MCR - 0x4009 0014 T3MCR - 0x4009 4014
MR0	Match Register 0. MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	R/W	0	T0MR0 - 0x4000 4018 T1MR0 - 0x4000 8018 T2MR0 - 0x4009 0018 T3MR0 - 0x4009 4018
MR1	Match Register 1. See MR0 description.	R/W	0	T0MR1 - 0x4000 401C T1MR1 - 0x4000 801C T2MR1 - 0x4009 001C T3MR1 - 0x4009 401C
MR2	Match Register 2. See MR0 description.	R/W	0	T0MR2 - 0x4000 4020 T1MR2 - 0x4000 8020 T2MR2 - 0x4009 0020 T3MR2 - 0x4009 4020
MR3	Match Register 3. See MR0 description.	R/W	0	T0MR3 - 0x4000 4024 T1MR3 - 0x4000 8024 T2MR3 - 0x4009 0024 T3MR3 - 0x4009 4024
CCR	Capture Control Register. The CCR controls which edges of the capture inputs are used to load the Capture Registers and whether or not an interrupt is generated when a capture takes place.	R/W	0	T0CCR - 0x4000 4028 T1CCR - 0x4000 8028 T2CCR - 0x4009 0028 T3CCR - 0x4009 4028
EMR	External Match Register. The EMR controls the external match pins MATn.0-3 (MAT0.0-3 and MAT1.0-3 respectively).	R/W	0	T0EMR - 0x4000 403C T1EMR - 0x4000 803C T2EMR - 0x4009 003C T3EMR - 0x4009 403C
CTCR	Count Control Register. The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	R/W	0	T0CTCR - 0x4000 4070 T1CTCR - 0x4000 8070 T2CTCR - 0x4009 0070 T3CTCR - 0x4009 4070

TxIR (TIMERx[0])

Bit	Symbol	Description
0	MR0 Interrupt	Interrupt flag for match channel 0.
1	MR1 Interrupt	Interrupt flag for match channel 1.
2	MR2 Interrupt	Interrupt flag for match channel 2.
3	MR3 Interrupt	Interrupt flag for match channel 3.
4	CR0 Interrupt	Interrupt flag for capture channel 0 event.
5	CR1 Interrupt	Interrupt flag for capture channel 1 event.
31:6	-	Reserved

Table 426. Interrupt Register (T[0/1/2/3]IR - addresses 0x4000 4000,
0x4000 8000, 0x4009 0000, 0x4009 4000) bitdescription

Bit	Symbol	Description	Reset Value
0	Counter Enable	When one, the Timer Counter and Prescale Counter are enabled for counting. When 1, the counters are disabled.	0
1	Counter Reset	When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 427. Timer Control Register (TCR, TIMERn: TnTCR - addresses 0x4000 4004, 0x4000 8004, 0x4009 0004,0x4009 4004) bit description

Timers como match

	Table 429. Match Control Register (T[0/1/2/3]MCR - addresses 0x4000 4014, 0x4000 8014, 0x4009 0014, 0x4009 4014) bit description			
Bit	Symbol	Value	Description	Reset Value

TxMCR (TIMERx[5])

Bit	Symbol	Value	Description	Reset Value
0	MR0I	1	Interrupt on MR0: an interrupt is generated when MR0 matches the value in the TC.	0
		0	This interrupt is disabled	
1	MR0R	1	Reset on MR0: the TC will be reset if MR0 matches it.	0
		0	Feature disabled.	
2	MR0S	1	Stop on MR0: the TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC.	0
		0	Feature disabled.	
3	MR1I	1	Interrupt on MR1: an interrupt is generated when MR1 matches the value in the TC.	0
		0	This interrupt is disabled	
4	MR1R	1	Reset on MR1: the TC will be reset if MR1 matches it.	0
		0	Feature disabled.	
5	MR1S	1	Stop on MR1: the TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC.	0
		0	Feature disabled.	

y sigue con el Timer 2 y el Timer 3.........

Table 431. External Match Register (T[0/1/2/3]EMR - addresses 0x4000 403C, 0x4000 803C, 0x4009 003C, 0x4009 403C) bit description

TxEMR (no está en posiciones contigüas)

#define TxEMR (* ((__RWuint32_t *) 0x[ver direccion]UL))

Bit	Symbol	Description	Reset Value
0	EM0	External Match 0. When a match occurs between the TC and MR0, this bit can either toggle, go low, go high, or do nothing, depending on bits 5:4 of this register. This bit can be driven onto a MATn.0 pin, in a positive-logic manner (0 = low, 1 = high).	0
1	EM1	External Match 1. When a match occurs between the TC and MR1, this bit can either toggle, go low, go high, or do nothing, depending on bits 7:6 of this register. This bit can be driven onto a MATn.1 pin, in a positive-logic manner (0 = low, 1 = high).	0
2	EM2	External Match 2. When a match occurs between the TC and MR2, this bit can either toggle, go low, go high, or do nothing, depending on bits 9:8 of this register. This bit can be driven onto a MATn.2 pin, in a positive-logic manner (0 = low, 1 = high).	0
3	EM3	External Match 3. When a match occurs between the TC and MR3, this bit can either toggle, go low, go high, or do nothing, depending on bits 11:10 of this register. This bit can be driven onto a MATn.3 pin, in a positive-logic manner (0 = low, 1 = high).	0
5:4	EMC0	External Match Control 0. Determines the functionality of External Match 0. Table 432 shows the encoding of these bits.	00
7:6	EMC1	External Match Control 1. Determines the functionality of External Match 1. Table 432 shows the encoding of these bits.	00
9:8	EMC2	External Match Control 2. Determines the functionality of External Match 2. Table 432 shows the encoding of these bits.	00
11:10	EMC3	External Match Control 3. Determines the functionality of External Match 3. Table 432 shows the encoding of these bits.	00
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 432. External Match Control

EMR[11:10], EMR[9:8], EMR[7:6], or EMR[5:4]	Function
00	Do Nothing.
01	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).
10	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).
11	Toggle the corresponding External Match bit/output.

Timers como captura

Table 428. Count Control Register (T[0/1/2/3]CTCR - addresses 0x4000 4070, 0x4000 8070, 0x4009 0070, 0x4009 4070) bit description

TxCTCR (no está en posiciones contigüas)
#define TxCTCR (*(__RWuint32_t *) 0x[ver direccion]UL)))

Bit	Symbol	Value	Description	Reset Value
1:0	Counter/Timer Mode		This field selects which rising PCLK edges can increment the Timer's Prescale Counter (PC), or clear the PC and increment the Timer Counter (TC).	00
		00	Timer Mode: the TC is incremented when the Prescale Counter matches the Prescale Register. The Prescale Counter is incremented on every rising PCLK edge.	
		01	Counter Mode: TC is incremented on rising edges on the CAP input selected by bits 3:2.	
		10	Counter Mode: TC is incremented on falling edges on the CAP input selected by bits 3:2.	
		11	Counter Mode: TC is incremented on both edges on the CAP input selected by bits 3:2.	
3:2	Count Input Select		When bits 1:0 in this register are not 00, these bits select which CAP pin is sampled for clocking.	00
		00	CAPn.0 for TIMERn	
		01	CAPn.1 for TIMERn	
		10	Reserved	
		11	Reserved	
			Note: If Counter mode is selected for a particular CAPn input in the TnCTCR, the 3 bits for that input in the Capture Control Register (TnCCR) must be programmed as 000. However, capture and/or interrupt can be selected for the other 3 CAPn inputs in the same timer.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 430. Capture Control Register (T[0/1/2/3]CCR - addresses 0x4000 4028, 0x4000 8020, 0x4009 0028, 0x4009 4028) bit description

TxCCR (TIMERx[9])

Bit	Symbol	Value	Description	Reset Value
0	CAP0RE	1	Capture on CAPn.0 rising edge: a sequence of 0 then 1 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
1	CAP0FE	1	Capture on CAPn.0 falling edge: a sequence of 1 then 0 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
2	CAP0I	1	Interrupt on CAPn.0 event: a CR0 load due to a CAPn.0 event will generate an interrupt.	0
		0	This feature is disabled.	
3	CAP1RE	1	Capture on CAPn.1 rising edge: a sequence of 0 then 1 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
4	CAP1FE	1	Capture on CAPn.1 falling edge: a sequence of 1 then 0 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	0
		0	This feature is disabled.	
5	CAP1I	1	Interrupt on CAPn.1 event: a CR1 load due to a CAPn.1 event will generate an interrupt.	0
		0	This feature is disabled.	
31:6	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

¿Cuáles pines pueden ser salidas de match?

Table 79.   Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00

Table 82.   Pin function select register 3 (PINSEL3 - address 0x4002 C00C) bit description

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
13:12	P1.22	GPIO Port 1.22	MCOB0	USB_PWRD	MAT1.0	00
19:18	P1.25	GPIO Port 1.25	MCOA1	Reserved	MAT1.1	00
25:24	P1.28	GPIO Port 1.28	MCOA2	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	MCOB2	PCAP1.1	MAT0.1	00

Table 84.   Pin function select register 7 (PINSEL7 - address 0x4002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
19:18	P3.25[1]	GPIO Port 3.25	Reserved	MAT0.0	PWM1.2	00
21:20	P3.26[1]	GPIO Port 3.26	STCLK	MAT0.1	PWM1.3	00

Table 85.   Pin function select register 9 (PINSEL9 - address 0x4002 C024) bit description

PINSEL9	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
25:24	P4.28	GPIO Port 4.28	RX_MCLK	MAT2.0	TXD3	00
27:26	P4.29	GPIO Port 4.29	TX_MCLK	MAT2.1	RXD3	00

¿Cuáles pines pueden ser entrada de captura?

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
9:8	P0.4[1]	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5[1]	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
15:14	P0.23[1]	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24[1]	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
5:4	P1.18	GPIO Port 1.18	USB_UP_LED	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	MCOA0	USB_PPWR	CAP1.1	00
21:20	P1.26	GPIO Port 1.26	MCOB1 KEY4_RC	PWM1.6	CAP0.0	00
23:22	P1.27[1]	GPIO Port 1.27	CLKOUT	USB_OVRCR	CAP0.1	00

Puerto Serie

$$UART1_{baudrate} = \frac{PCLK}{16 \times (256 \times U1DLM + U1DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)}$$

#define	DIR_UART0	((volatile uint32_t *) 0x4000C000UL)
#define	DIR_UART1	((volatile uint32_t *) 0x40010000UL)

PUERTO SERIE: La dirección de los puertos serie del sistema, se encuentra a partir de la dirección 0x0400 de memoria

Line Control Register: LCR – BASE + 3 (activo alto)

B7	B6	B5	B4	B3	B2	B1	B0

Word Length (WLS0 – WLS1)

B1	B0	Character length
0	0	5
0	1	6
1	0	7
1	1	8

Number of Stop Bits (STB)

B2	Word length	Stop bits
0	5,6,7 o 8	1
1	5	1,5
1	6,7 o 8	2

Party Enable (PEN)

B3	Paridad
0	OFF
1	ON

Even Parity Select (EPS)

B4	Parity
0	Odd
1	Even

Stick Parity

B5	B4	B3	Logic of parity bit
1	1	1	Logic 0
1	0	1	Logic 1
0	X	X	Disable

Set Break

B6	Causes break conditions (SOUT)
0	Disable
1	Enable

Divisor Latch Access Bit (DLAB)

B7	Access
0	Receiver Buffer and Interrupt Enable Register
1	Divisor Latches of the Baud Generator

Registros: RBR, THR, IER, IIR, FCR, LCR, MCR, LSR, MSR, SCR / DLL, DLM

Line Status Register: LSR – BASE + 5 (activo alto)

0	TEMT	THRE	BI	FE	PE	OE	DR
7	6	5	4	3	2	1	0

Transmitter Empty · Transmitter Holding Register Empty · Break Interrupt · Framing Error · Parity Error · Overrun Error · Data Ready

Reset by HW: Por el solo hecho de leerlo se resetea.

INICIALIZACION DEL PUERTO TRANSMISION - REGISTROS

(2)	Serializador
(1)	Registro Tx

Cuando pasa de (1) a (2) se activa THRE (BASE+5, bit 5)
Cuando sale de (2) se activa TEMT (BASE + 5 , bit 6)

INICIALIZACION DEL PUERTO RECEPCION - REGISTROS

(2)	Paralelizador
(1)	Registro Rx

Cuando pasa de (2) a (1) se activa DR (BASE + 5 , bit 0)

Interrupt Enable Register: IER– BASE + 1 (activo alto)

				EDSSI	ELSI	ETBEI	ERBFI
0	0	0	0	IER(3)	IER(2)	IER(1)	IER(0)
7	6	5	4	3	2	1	0

Reset by HW: Por el solo hecho de leerlo se resetea.

IER0: A 1 si habilitar interrupción de dato disponible.
IER1: A 1 si habilitar interrupción de registro de retención de transmisión vacío.
IER2: A 1 si habilitar interrupción de error de recepción (bits 1 al 4 del LSR).
IER3: A 1 si habilitar interrupción ante el cambio del MSR (Registro de estado del modem).

Interrupt Ident Register: IIR– BASE + 2 (activo alto)

		0	0	b2	b1	b0

Entrada a la función de Int. → Análisis de cuál fue → proceso → Investigo b0 → Salida de la función de Int.

Interrupt Pending

b0 = 0 => Hay una interrupción pendiente de atención
b0 = 1 => No hay una interrupción pendiente

b2	b1	Descripción
1	1	Errores y break (>)
1	0	Dato disponible
0	1	THR disponible
0	0	Estado del MODEM (<)

Nro de Pin Stick LPCXpresso1769	Nombre de la conexión en Hoja 4 (LPCXpresso1769)	Se conecta a: Nro de Hoja del esquemático - Nombre	Descripción	Nro de Puerto y Pin del LPC1769
1	GND	2 - FUENTE	GND	
2	VCC_3V3	2 - FUENTE	Alimentación del LPCXpresso (~5Vcc)	
54	GND	2 - FUENTE	GND	
49	Expansion0	3 - CONEXIÓN A EXPANSIONES	Expansion 0	P2.7
58	Expansion1	3 - CONEXIÓN A EXPANSIONES	Expansion 1	P1.29
57	Expansion2	3 - CONEXIÓN A EXPANSIONES	Expansion 2	P4.28
60	Expansion3	3 - CONEXIÓN A EXPANSIONES	Expansion 3	P1.23
61	Expansion4	3 - CONEXIÓN A EXPANSIONES	Expansion 4	P1.20
62	Expansion5	3 - CONEXIÓN A EXPANSIONES	Expansion 5	P0.19
63	Expansion6	3 - CONEXIÓN A EXPANSIONES	Expansion 6	P3.26
65	Expansion7	3 - CONEXIÓN A EXPANSIONES	Expansion 7	P1.25
66	Expansion8	3 - CONEXIÓN A EXPANSIONES	Expansion 8	P1.22
67	Expansion9	3 - CONEXIÓN A EXPANSIONES	Expansion 9	P1.19
56	Expansion10	3 - CONEXIÓN A EXPANSIONES	Expansion 10	P0.20
69	Expansion11	3 - CONEXIÓN A EXPANSIONES	Expansion 11	P3.25
70	Expansion12	3 - CONEXIÓN A EXPANSIONES	Expansion 12	P1.27
71	Expansion13	3 - CONEXIÓN A EXPANSIONES	Expansion 13	P1.24
72	Expansion14	3 - CONEXIÓN A EXPANSIONES	Expansion 14	P1.21
73	Expansion15	3 - CONEXIÓN A EXPANSIONES	Expansion 15	P1.18
50	Expansion16	3 - CONEXIÓN A EXPANSIONES	Expansion 16	P2.8
53	Expansion17	3 - CONEXIÓN A EXPANSIONES	Expansion 17	P2.12
3	VB	4 - LPCXPRESSO1769	Batería de 3V para RTC	
4	Reset	4 - LPCXPRESSO1769	Señal de Reset del microcontrolador	
28	3V3Externos	4 - LPCXPRESSO1769	Jumper de Alimentación Externa	
29	Sin conexión	4 - LPCXPRESSO1769	Sin conexión	
30	Sin conexión	4 - LPCXPRESSO1769	Sin conexión	
31	Sin conexión	4 - LPCXPRESSO1769	Sin conexión	
55	Sin conexión	4 - LPCXPRESSO1769	Sin conexión	P2.9
51	Teclado5x1_0	5 - TECLADO	Tecla SW1	P2.10
11	Teclado5x1_1	5 - TECLADO	Tecla SW2	P0.18
41	Teclado5x1_2	5 - TECLADO	Tecla SW3	P0.11
27	Teclado5x1_3	5 - TECLADO	Tecla SW4	P2.13
59	Teclado5x1_4	5 - TECLADO	Tecla SW5 (También es Entrada Digital 0)	P1.26
59	ED0	6 - ENTRADAS DIGITALES	Entrada Digital 0 (También es Tecla SW5)	P1.26
68	ED1	6 - ENTRADAS DIGITALES	Entrada Digital 1	P4.29
52	ED2	6 - ENTRADAS DIGITALES	Entrada Digital 2	P2.11
20	EA0	7 - ENTRADAS ANALÓGICAS	Entrada Analógica 0	P1.31

16	EA1	7 - ENTRADAS ANALÓGICAS	Entrada Analógica 1	P0.24
17	EA2	7 - ENTRADAS ANALÓGICAS	Entrada Analógica 2	P0.25
42	SD0	8 - SALIDAS DIGITALES	Salida Digital 0 / Relay 0 / Led 0	P2.0
15	SD1	8 - SALIDAS DIGITALES	Salida Digital 1 / Relay 1 / Led 1	P0.23
23	SD2	8 - SALIDAS DIGITALES	Salida Digital 2 / Relay 2 / Led 2	P0.21
25	SD3	8 - SALIDAS DIGITALES	Salida Digital 3 / Relay 3 / Led 3	P0.27
26	SD4	8 - SALIDAS DIGITALES	Salida Digital 4 / Buzzer / Led 4	P0.28
18	SA	9 - SALIDA ANALÓGICA	Salida DAC / Amplificador de Audio	P0.26
43	PWM2	10 - SALIDAS DE PWM	Led RGB - (B) Azul	P2.1
45	PWM0	10 - SALIDAS DE PWM	Led RGB - (G) Verde	P2.3
44	PWM1	10 - SALIDAS DE PWM	Led RGB - (R) Rojo	P2.2
64	PWM3	10 - SALIDAS DE PWM	No usado	P1.28
39	LCD_D4	11 - LCD	Display de caracteres - Señal D4	P0.5
40	LCD_D5	11 - LCD	Display de caracteres - Señal D5	P0.10
46	LCD_D6	11 - LCD	Display de caracteres - Señal D6	P2.4
47	LCD_D7	11 - LCD	Display de caracteres - Señal D7	P2.5
38	LCD_E	11 - LCD	Display de caracteres - Señal E	P0.4
48	LCD_RST	11 - LCD	Display de caracteres - Señal RST	P2.6
12	CTS1	12 - COMUNICACIÓN SERIE	Señal CTS	P0.17
24	RTS1	12 - COMUNICACIÓN SERIE	Señal RTS	P0.22
14	Rx1	12 - COMUNICACIÓN SERIE	Señal Rx	P0.16
13	Tx1	12 - COMUNICACIÓN SERIE	Señal Tx	P0.15
21	Tx0	13 - USB	USB a Serie - Señal Rx	P0.2
22	Rx0	13 - USB	USB a Serie - Señal Tx	P0.3
19	VBUS	13 - USB	USB Device - Señal de VBUS	P1.30
36	USB D-	13 - USB	USB Host / USB Device - Señal D-	P0.29, P0.30 (Ver Nota 1)
37	USB D+	13 - USB	USB Host / USB Device - Señal D+	
32	ETH_RXN	14 - ETHERNET	Ethernet - Señal RXN	P1.0, P1.1, P1.4, P1.8, P1.9, P1.10, P1.14, P1.15, P1.16, P1.17 (Ver Nota 2)
33	ETH_RXP	14 - ETHERNET	Ethernet - Señal RXP	
34	ETH_TXN	14 - ETHERNET	Ethernet - Señal TXN	
35	ETH_TXP	14 - ETHERNET	Ethernet - Señal TXP	
10	SCL	15 - MEMORIAS	Memoria EEPROM I2C - Señal SCL	P0.1
9	SDA	15 - MEMORIAS	Memoria EEPROM I2C - Señal SDA	P0.0
6	MISO	15 - MEMORIAS	Micro SD Card / SD Card - Señal MISO	P0.8
5	MOSI	15 - MEMORIAS	Micro SD Card / SD Card - Señal MOSI	P0.9
7	SCK	15 - MEMORIAS	Micro SD Card / SD Card - Señal SCK	P0.7
8	SSEL	15 - MEMORIAS	Micro SD Card / SD Card - Señal SSEL	P0.6

PinOut BaseBoard

GPIO	Pin Stick	Funcion	Sal. Micro Exp	PLACA EXPANSION Num 2	Num 3	Num 1	Num 4	Mother
P0.0	9							I2C - Señal SDA
P0.1	10							I2C - Señal SCL
P0.2	21							USB a Serie - Señal Rx
P0.3	22							USB a Serie - Señal Tx
P0.4	38	E lcd						LCD: E
P0.5	39	D4 lcd						LCD: D4
P0.6	8							SD Card - Señal SSEL
P0.7	7							SD Card - Señal SCK
P0.8	6							SD Card - Señal MISO
P0.9	5							SD Card - Señal MOSI
P0.10	40	D5 lcd						LCD: D5
P0.11			Tec.Fijo2					SW3 (ex 7)
P0.12		NC						
P0.13		NC						
P0.14		NC						
P0.15	13							Serie: Señal Tx
P0.16	14							Serie: Señal Rx
P0.17	12							Serie: Señal CTS
P0.18	11		Tec.Fijo1					SW2 (ex 4)
P0.19	62	d0	5	DIG6	CLK	Led 6		Expansión
P0.20	56		10	seg_g	Fila3	DP1- 3		Expansión
P0.21	23	0ut 2						Led 2/Rel1
P0.22	24							Serie: Señal RTS
P0.23	15	0ut 1						Led 3/Rel4
P0.24	16							IN Analógica 1
P0.25	17							IN Analógica 2
P0.26								Salida DAC / Amplificador de Audio
P0.27	25	0ut 3						Led 4/Rel3
P0.28	26							BUZZER
P0.29								
P0.30								USB Device - Señal de VBUS
P0.31		NC						

GPIO	Pin Stick	Funcion	Sal. Micro Exp	PLACA EXPANSION Num 2	Num 3	Num 1	Num 4	Mother
P1.0								
P1.1								
P1.2		NC						
P1.3		NC						
P1.4								
P1.5		NC						
P1.6		NC						
P1.7		NC						
P1.8								
P1.9								
P1.10								
P1.11								
P1.12								
P1.13								
P1.14								
P1.15								
P1.16								
P1.17								
P1.18	73	b	15	seg_b		DP1 - 8		Expansión
P1.19	67		9	seg_dp	Fila2	DP1 - 2		Expansión
P1.20	61	d1	4	DIG5	dp	Led 5		Expansión
P1.21	72	c	14	seg_c		DP1 - 7		
P1.22	66		8		Fila1	DP1 - 1		Expansión
P1.23	60	d2	3	DIG4	D BCD	Led 4		Expansión
P1.24	71		13	seg_d		DP1 - 6		Expansión
P1.25	65		7		Fila0	Led 8		Expansión
P1.26	59	I0 / ED0						SW5 (ex 13) y ED0
P1.27	70		12	seg_e	Col1	DP1 - 5		Expansión
P1.28	64	BF lcd						BF
P1.29	58	d4	1	DIG2	B BCD	Led 2		Expansión
P1.30	19							USB Device - Señal de VBUS
P1.31	20							IN Analógica 0

PinOut BaseBoard

GPIO	Pin Stick	Funcion	Exp	Num 2	Num 3	Num 1	Num 4	Mother
P2.0	42	0ut 0						Led 1/ Rel 2
P2.1	43							RGB Rojo
P2.2	44							RGB Verde
P2.3	45							RGB Azul
P2.4	46	D6 lcd						LCD: D6
P2.5	47	D7 lcd						LCD: D7
P2.6	48	RS lcd						LCD: RS
P2.7	49	d5	0	DIG1	A BCD	Led 1		Expansión
P2.8	50		16			DP2 - 1		Expansión
P2.9	55							NC
P2.10	51		Tec.Fijo0					SW1 EINT0
P2.11	52	ED2						ED2 EINT1
P2.12	53		17			DP2 - 2		Expansión EINT2
P2.13	27		Tec.Fijo3					SW4 (ex10) EINT3

GPIO	Pin Stick	Funcion	Exp	Num 2	Num 3	Num 1	Num 4	Mother
P3.25	69		11	seg_f	Col0	DP1 - 4		Expansión
P3.26	63	a	6	Seg_a	RST	Led 7		Expansión
P4.28	57	d3	2	DIG3	C BCD	Led 3		Expansión
P4.29	68	ED1						

FALTA EXP 18 que va a DP2 -3 en placa EXP 1

EXPANSION 1

FUNCION	GPIO
Led 1	P2.7
Led 2	P1.29
Led 3	P4.28
Led 4	P1.23
Led 5	P1.20
Led 6	P0.19
Led 7	P3.26
Led 8	P1.25
DP1-1	P1.22
DP1-2	P1.19
DP1-3	P0.20
DP1-4	P3.25
DP1-5	P1.27
DP1-6	P1.24
DP1-7	P1.21
DP1-8	P1-18
DP2-1	P2.8
DP2-2	P2.12
DP2-3	P0.16

EXPANSION 2

FUNCION	GPIO
P2.7	DIG1
P1.29	DIG2
P4.28	DIG3
P1.23	DIG4
P1.20	DIG5
P0.19	DIG6
P3.26	seg_a
P1.18	seg_b
P1.21	seg_c
P1.24	seg_d
P1.27	seg_e
P3.25	seg_f
P0.20	seg_g
P1.19	seg_dp

EXPANSION 3

FUNCION	GPIO
Fila0	P1.25
Fila1	P1.22
Fila2	P1.19
Fila3	P0.20
Col0	P3.25
Col1	P1.27
CLK	P0.19
RST	P3.26
A BCD	P2.7
B BCD	P1.29
C BCD	P4.28
D BCD	P1.23
dp	P1.20

Los switch de la placa base deben estar en:
S1[2] = OFF
S2[2] = OFF
S3[2] = ON

PLACA BASE

FUNCION	GPIO
P2.0	Led 1/ Rel 2
P0.21	Led 2/Rel1
P0.23	Led 3/Rel4
P0.27	Led 4/Rel3
P2.1	RGB Rojo
P2.2	RGB Verde
P2.3	RGB Azul
P1.26	SW5 (ex 13) // ED0
P0.11	SW7
P0.18	SW4
P2.10	SW1 EINT0
P2.11	ED2 EINT1
P2.12	Expansion 17 EINT2
P2.13	SW4 (ex10) EINT3
P4.29	ED1
P0.28	BUZZER
P0.4	E LCD
P1.28	BF
P0.5	D4
P0.10	D5
P2.4	D6
P2.5	D7
P2.6	RS