

第一次作业

Hollow Man

本次作业根据：https://blog.csdn.net/weixin_35433448/article/details/112102416 所述方法进行 FPGA 并行单精度浮点数运算能力的计算，结合 DSP/LUT/DFF 资源综合计算，其计算公式为：

$$FPGA\ FLOPS = DSP\ 个数 \times DSP\ 频率 + 逻辑单元个数 \times 逻辑单元频率$$

参考 Xilinx Spartan-6 系列 FPGA 官方介绍文档：

https://china.xilinx.com/support/documentation/data_sheets/ds160.pdf，以包含 DSP 数目最多的 XC6SLX150T 为例，其包含 DSP48A1 180 个，Logic Cells 147443 个，抛去估算的用于 I/O 设备的 14000 个，并且 1 个基于 DSP48 的加法器需要 2 个 DSP slices 和 289LUT-FF pairs 组成，1 个基于 Logic cell 的加法器需要 517 Logic Cells 组成。（具体见问题(2)中所示文档），FPGA 频率最大为 390MHz，且可以在每个时钟周期可以做 2 个单精度浮点计算(乘和加)。则算式为：

$[180/2 + (147443 - 14000 - 90 \times 289)/517] \times 390\ MHz = 116.142\ GFLOPs$ ，远低于 Intel i7 6900K 和 6700K，因而 i7 的浮点数处理能力更强。

Table 1: Spartan-6 FPGA Feature Summary by Device

Device	Logic Cells ⁽¹⁾	Configurable Logic Blocks (CLBs)			DSP48A1 Slices ⁽³⁾	Block RAM Blocks		CMTs ⁽⁵⁾	Memory Controller Blocks (Max) ⁽⁶⁾	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices ⁽²⁾	Flip-Flops	Max Distributed RAM (Kb)		18 Kb ⁽⁴⁾	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

Digital Signal Processing—DSP48A1 Slice

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All Spartan-6 FPGAs have many dedicated, full-custom, low-power DSP slices, combining high speed with small size, while retaining system design flexibility.

Each DSP48A1 slice consists of a dedicated 18×18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating at up to 390 MHz. The DSP48A1 slice provides extensive pipelining and extension capabilities that enhance speed and efficiency of many applications, even beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter. The multiplier can perform barrel shifting.

- (1) 打开 Xilinx 官网，可看到目前 Xilinx 最高端的 FPGA 是 Zynq UltraScale+ RFSoc ZU49DR，参考其官方介绍文档：
https://china.xilinx.com/support/documentation/data_sheets/ds890-ultrascale-overview.pdf，Zynq UltraScale+ ZU49DR 拥有的资源列表，我们可以看到它有 930300 个 Logic cell, 4272 个 DSP slices。

Zynq UltraScale+ RFSoc: Device Feature Summary

Table 19: Zynq UltraScale+ RFSoc Feature Summary

		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
12-bit RF-ADC w/ DDC	# of ADCs	0	8	8	8	16	16	-	-	-	-	-	-
	Max Rate (GSPS)	-	4.096	4.096	4.096	2.058	2.220	-	-	-	-	-	-
14-bit RF-ADC w/ DDC	# of ADCs	-	-	-	-	-	-	8	2	4	8	8	16
	Max Rate (GSPS)	-	-	-	-	-	-	2.5	5.0	5.0	2.5	5.0	2.5
14-bit RF-DAC w/ DUC	# of DACs	0	8	8	8	16	16	8	4	12	8	8	16
	Max Rate (GSPS)	-	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0	10.0
SD-FEC		8	0	0	8	0	0	0	0	0	8	8	0
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight™; NEON and Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache												
Real-Time Processing Unit	Dual-core Arm Cortex-RSF with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM												
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC												
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; Watchdog Timers; Triple Timer Counters												
High-Speed Connectivity	4 PS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII												
System Logic Cells		930,300	678,318	930,300	930,300	930,300	930,300	489,300	930,300	930,300	930,300	930,300	930,300
CLB Flip-Flops		850,560	620,176	850,560	850,560	850,560	850,560	447,360	850,560	850,560	850,560	850,560	850,560
CLB LUTs		425,280	310,088	425,280	425,280	425,280	425,280	223,680	425,280	425,280	425,280	425,280	425,280
Distributed RAM (Mb)		13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0
Block RAM Blocks		1,080	792	1,080	1,080	1,080	1,080	648	1,080	1,080	1,080	1,080	1,080
Block RAM (Mb)		38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0
UltraRAM Blocks		80	48	80	80	80	80	160	80	80	80	80	80
UltraRAM (Mb)		22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5
DSP Slices		4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272
CMTs		8	6	8	8	8	8	5	8	8	8	8	8
Maximum HP I/O		208	299	299	299	312	312	128	299	312	299	299	312
Maximum HD I/O		72	48	48	48	96	96	24	48	48	48	48	96
System Monitor		1	1	1	1	1	1	1	1	1	1	1	1
GTY Transceivers		16	8	16	16	16	16	8	16	16	16	16	16
Transceivers Fractional PLLs		8	4	8	8	8	8	4	8	8	8	8	8
PCIe4 (PCIe Gen3 x16)		2	1	2	2	2	2	-	-	-	-	-	-
PCIe4C (PCIe Gen3 x16 / Gen4 x8 / CCIX) ⁽¹⁾		-	-	-	-	-	-	0	2	2	2	2	2
150G Interlaken		1	1	1	1	1	1	0	1	1	1	1	1
100G Ethernet w/ RS-FEC		2	1	2	2	2	2	0	2	2	2	2	2

Notes:

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. Go to [PG213](#), UltraScale+ Devices Integrated Block for PCI Express Product Guide, for details on compatibility mode.

1 个基于 DSP48 的加法器需要 2 个 DSP slices 和 289LUT-FF pairs 组成。

1 个基于 Logic cell 的加法器需要 517 Logic Cells 组成。

Table 32: Characterization of Single-Precision Format on Kintex-7 FPGAs (Part = XC7K70T-1)

Operation	Resources					Maximum Frequency (MHz) ⁽¹⁾⁽²⁾
	Embedded		Fabric			
	Type	Number	LUT-FF Pairs	LUTs	FFs	-1 Speed Grade
Multiply	DSP48E1 (max usage)	3	125	99	105	463
	DSP48E1 (full usage)	2	170	117	160	463
	DSP48E1 (medium usage)	1	334	285	331	462
	Logic	0	666	629	669	449
Add/Subtract	DSP48E1 (speed optimized, full usage)	2	289	230	327	419
	Logic (speed optimized, no usage)	0	517	403	541	438
	Logic (low latency)	0	587	482	610	464

由于实现相关的 I/O 设备，必须占用掉一定数量的 Logic Cell,这里我们假设用掉 14000 个 Logic Cell. 也即：Logic Cell 剩下总数 = 930300 - 14000 = 916300.

由于要计算出最大值，我们需要假设尽可能多的使用所有资源，这样可以得出：

DSP48 based adder amount = 4272 / 2 = 2136 (个)

LC based Adder amount = (916300 - 2136*289) / 517 = 578(个)


基于 DSP48 的加法器的 clock 范围在： 600 Mhz(slow) - 891Mhz (fastest)

DSP48 Slice Switching Characteristics

Table 83: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V ¹		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	With all registers used	891	775	645	644	600	MHz
F _{MAX_PATDET}	With pattern detector	794	687	571	562	524	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	635	544	456	440	413	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	577	492	410	395	371	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG	655	565	468	453	423	MHz
F _{MAX_NOPIELINEREG}	Without pipeline registers (MREG, ADREG)	483	410	338	323	304	MHz
F _{MAX_NOPIELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	448	379	314	299	280	MHz



Notes:

- For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross the clock region  the specified F_{MAX}.

基于 Logic cell 的加法器的 clock 范围在：667 Mhz(slow) - 891Mhz (fastest)

Clock Buffers and Networks

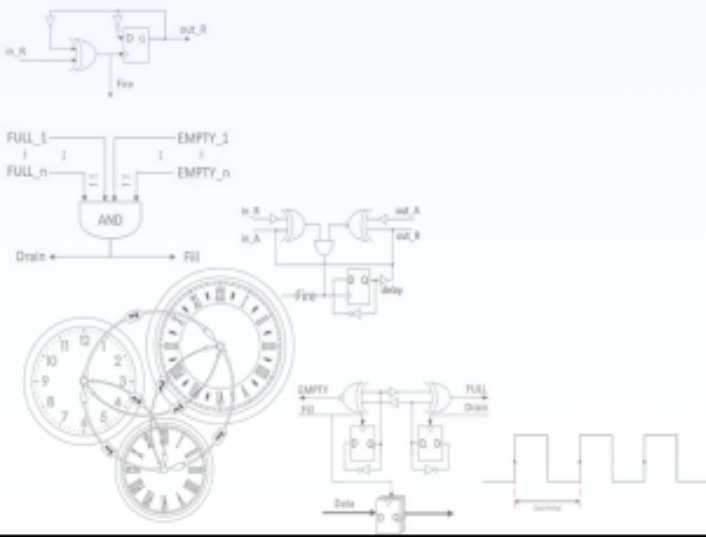
Table 84: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F _{MAX}	Maximum frequency of a global clock tree (BUFG)	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F _{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F _{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512			MHz

所以(2136+578)*891MHz = 2418.174 GFLOPs



第一次作业



第一次作业

**Intel I7 6900K 的单精度浮点数运算能力为 1024GFlops，
6700K 为 511.3GFlops。**

**(1)请估算，如果用低端的 Xilinx Spartan-6 系列 FPGA 来实现
并行的单精度浮点数，可以达到多少 GFlops?与 I7 的浮点 数
处理能力比起来那种强？**

**(2)当前 Xilinx 最高端的 FPGA 是那种?估算这种 FPGA 芯片的
浮点数性能。**

