

Appendix A Combinations of Initial Mapping and Adjustment Algorithms

In order to visualize the difference between the four initial mapping algorithms from ZPW, FiDLS, SABRE, and TSA, we plot the data in Table 2. The five rows in the table correspond to Figs.A 1(a)–1(e). The lower the y -axis of the bar graph means the fewer additional gates are inserted. The smaller the range on the x -axis means the smaller the circuit scale it can handle. In the figures, the yellow (resp. blue) color indicates the performance of TSA (resp. ZPW) as the initial mapping. In terms of different adjustment algorithms, the initial mapping algorithms of SABRE (red) and FiDLS (green) are not absolutely good or bad, but overall, the initial mapping of TSA has the fewest number of additional gates inserted in each adjustment algorithm, and the number of additional gates inserted in the initial mapping of ZPW is the most.

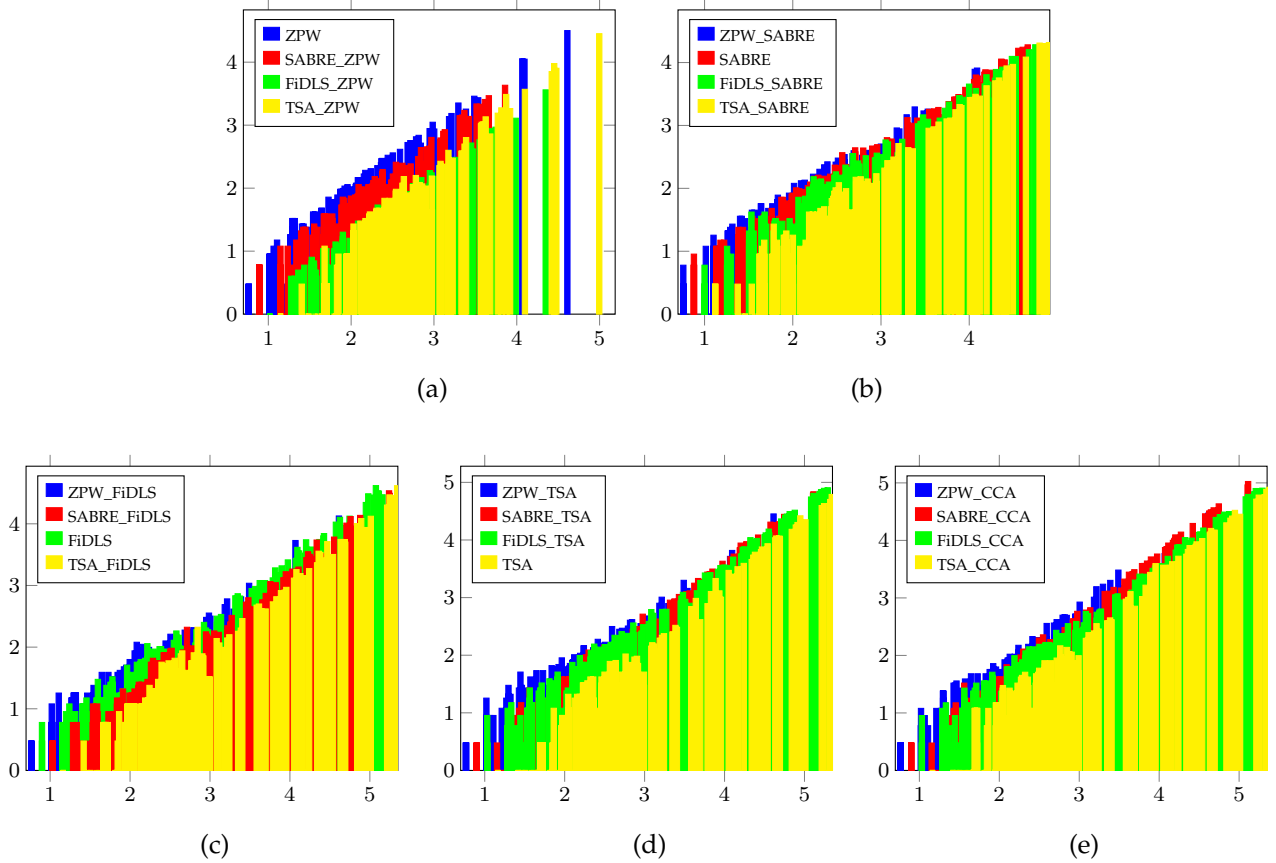
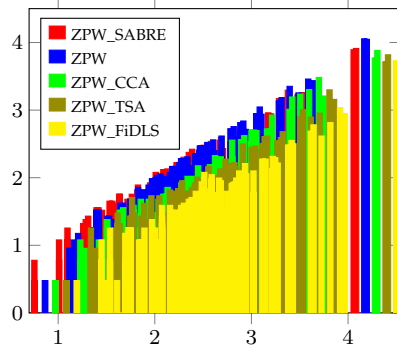
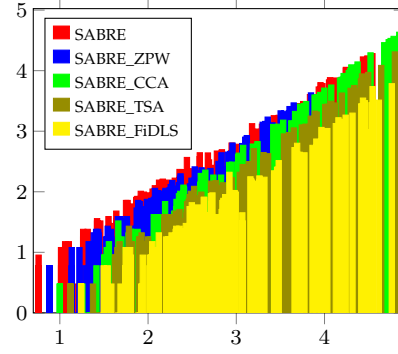


Fig.A1. Comparison of the initial mapping algorithms of ZPW, SABRE, FiDLS, and TSA, using the adjustment algorithm of (a) ZPW, (b) SABRE, (c) FiDLS, (d) TSA_{num}, and (e) TSA_{cca}, respectively. The x -axis represents the number of 2-qubit gates in the benchmark, and the y -axis represents the number of additional gates.

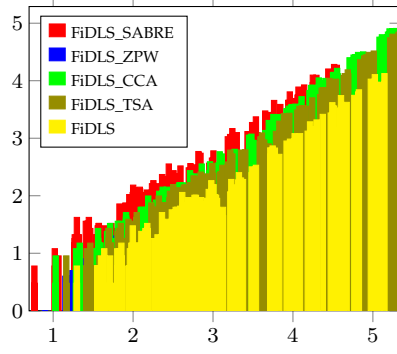
We then compare the five adjustment algorithms ZPW, SABRE, FiDLS, TSA_{num}, and TSA_{cca} under specific initial mapping algorithms. The four rows in Table 3 correspond to Figs.A 2(a)–2(d). As we can see, yellow bars (FiDLS) are the lowest. Red bars (SABRE) are the highest. The second-lowest are olive bars (TSA_{num}), which can handle all benchmarks. TSA_{num} has fewer gates and shorter running time than ZPW in all initial mapping algorithms.



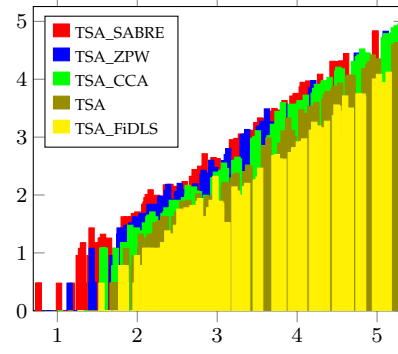
(a)



(b)



(c)



(d)

Fig.A2. Comparison of the adjustment algorithms of ZPW, SABRE, FiDLS, TSA_{num} , and TSA_{cca} , using the initial mapping algorithm of (a) ZPW, (b) SABRE, (c) FiDLS, and (d) TSA, respectively. The x -axis represents the number of 2-qubit gates in the benchmark, and the y -axis represents the number of additional gates.