TEXAS INSTRUMENTS

VinMin = 48.0V
VinMax = 51.6V
Vout = 5.0V
Iout = 1.0A

Device = LMR36510FADDAR
Topology = Buck
Created = 2024-10-18 20:21:32.724
BOM Cost = $2.41
BOM Count = 12
Total Pd = 0.8W

WEBENCH ® Design Report

Design : 15 LMR36510FADDAR
LMR36510FADDAR ***FINAL*** 48V-51.6V to 5.00V @ 1A
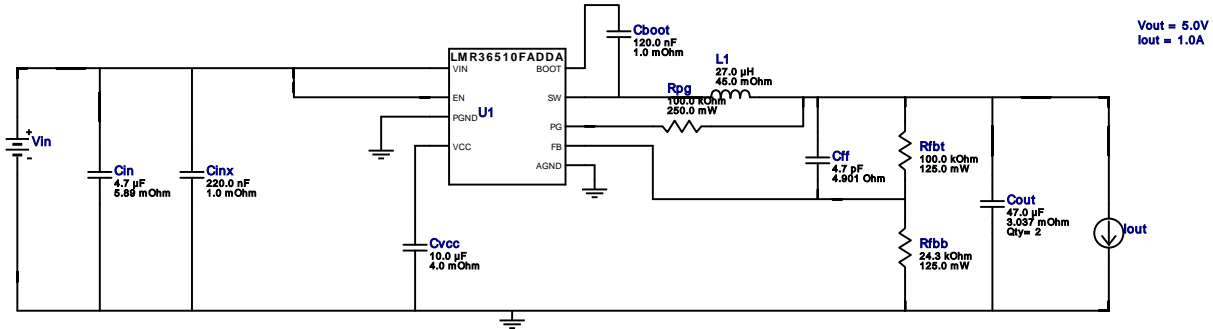
Electrical BOM

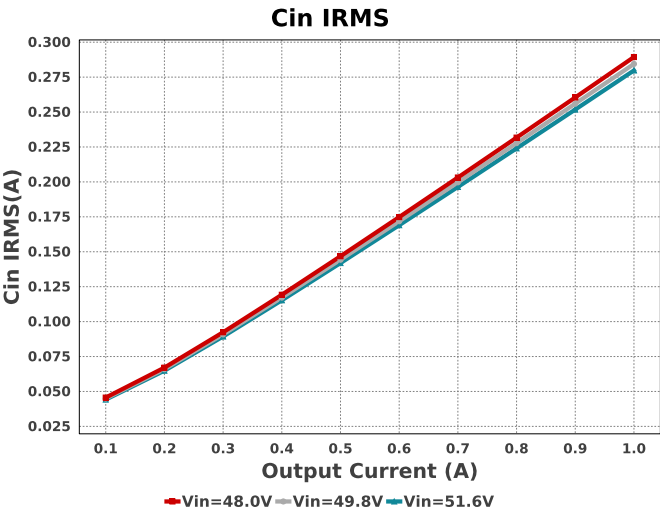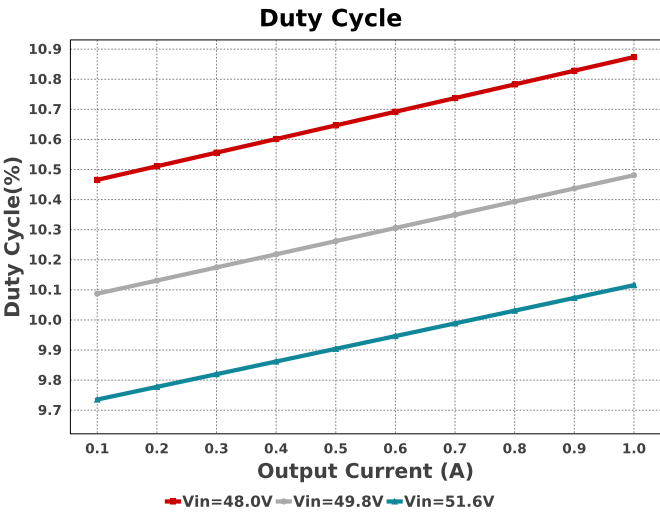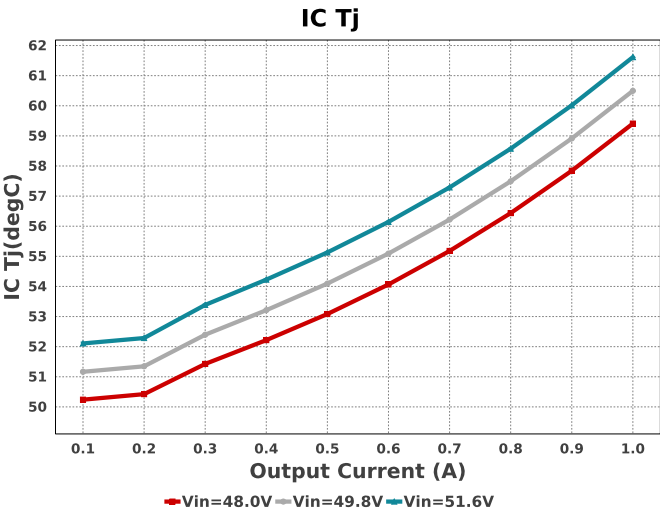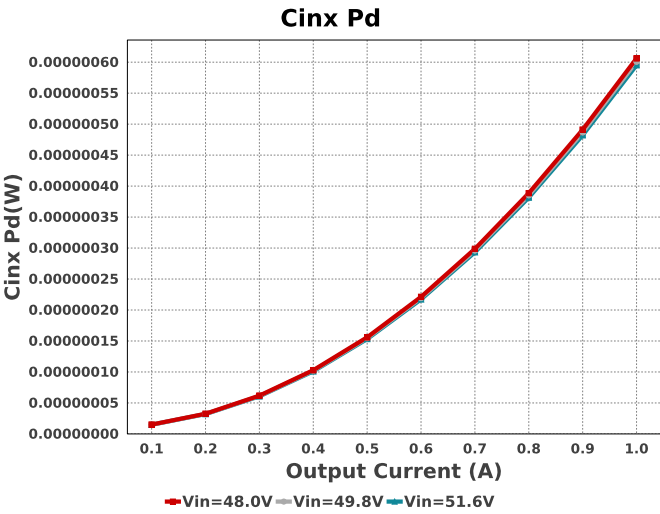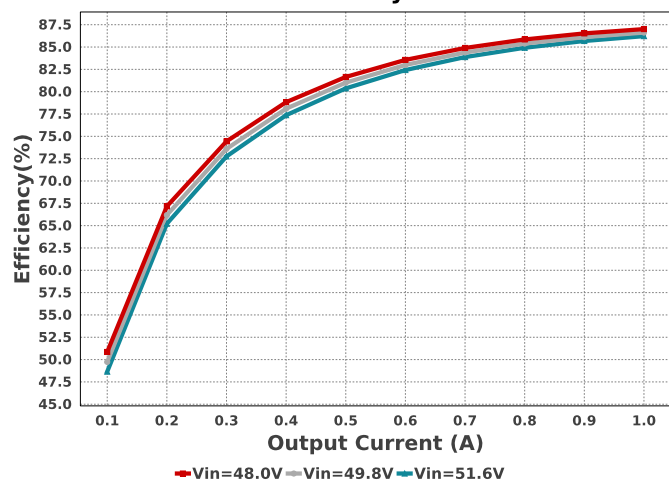| Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cboot	MuRata	GRM21BR71C124KA01L Series= X7R	Cap= 120.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	$0.04	0805 7 mm²
Cff	AVX	12065A4R7CAT2A Series= C0G/NP0	Cap= 4.7 pF ESR= 4.901 Ohm VDC= 50.0 V IRMS= 0.0 A	1	$0.07	1206 11 mm²
Cin	TDK	C3225X7S2A475M200AB Series= X7S	Cap= 4.7 uF ESR= 5.89 mOhm VDC= 100.0 V IRMS= 6.7739 A	1	$0.45	1210 15 mm²
Cinx	MuRata	GRM31MR72A224KA01L Series= X7R	Cap= 220.0 nF ESR= 1.0 mOhm VDC= 100.0 V IRMS= 0.0 A	1	$0.09	1206 11 mm²
Cout	MuRata	GRM32ER61C476KE15L Series= X5R	Cap= 47.0 uF ESR= 3.037 mOhm VDC= 16.0 V IRMS= 4.59346 A	2	$0.17	1210_280 15 mm²
Cvcc	MuRata	GRM21BR61E106MA73L Series= X5R	Cap= 10.0 uF ESR= 4.0 mOhm VDC= 25.0 V IRMS= 2.8 A	1	$0.04	0805 7 mm²
L1	Bourns	SRR1260-270M	L= 27.0 µH 45.0 mOhm	1	$0.60	SRR1260 210 mm²
Rfbb	Vishay-Dale	CRCW080524K3FKEA Series= CRCW..e3	Res= 24.3 kOhm Power= 125.0 mW Tolerance= 1.0%	1	$0.01	0805 7 mm²
Rfbt	Vishay-Dale	CRCW0805100KFKEA Series= CRCW..e3	Res= 100.0 kOhm Power= 125.0 mW Tolerance= 1.0%	1	$0.01	0805 7 mm²
Rpg	Vishay-Dale	CRCW1206100KFKEA Series= CRCW..e3	Res= 100.0 kOhm Power= 250.0 mW Tolerance= 1.0%	1	$0.01	1206 11 mm²

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WEBENCH® Design Report   LMR36510FADDAR : LMR36510FADDAR
FINAL 48V-51.6V to 5.00V @ 1A   November 13, 2024 10:12:12 GMT-06:00

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
U1	Texas Instruments	LMR36510FADDAR	Switcher	1	$0.75	

DDA0008J 55 mm²

Cinx Pd

IC Tj

Duty Cycle

Cin IRMS

IC Ipk

L Pd
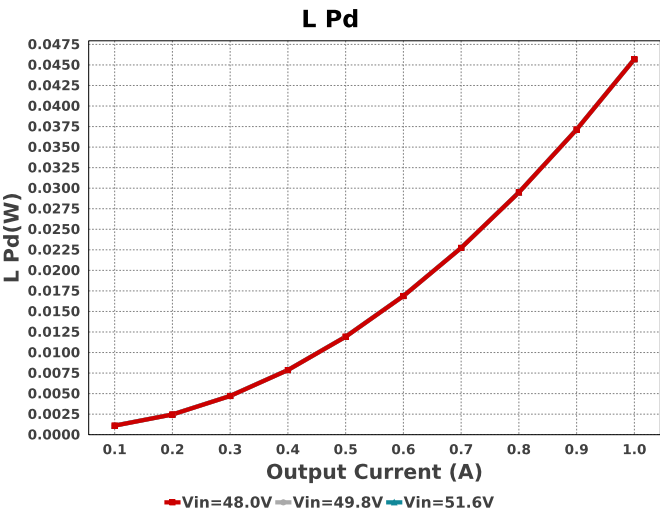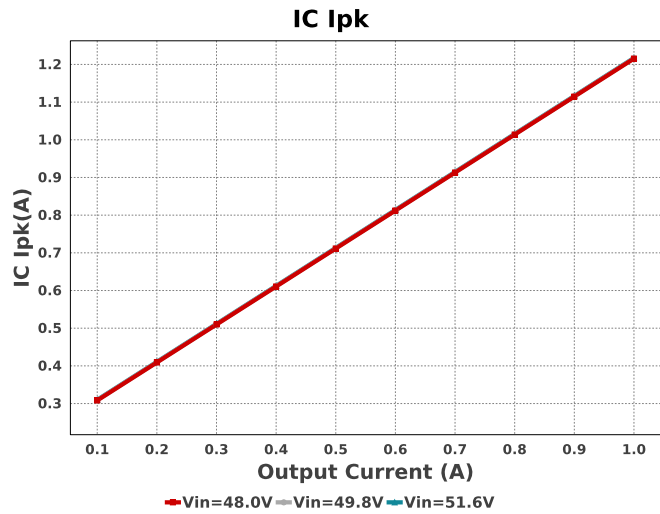
Efficiency

Vin p-p
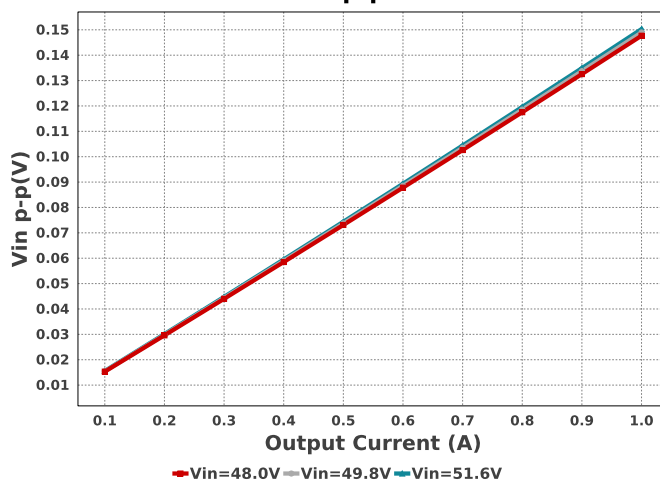
Vout p-p
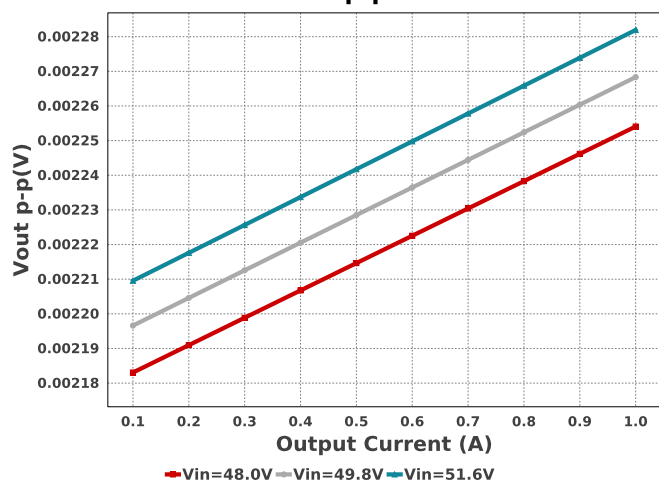
Cin Pd

Cout Pd

Ipp percentage

WEBENCH® Design Report   LMR36510FADDAR : LMR36510FADDAR
FINAL 48V-51.6V to 5.00V @ 1A   November 13, 2024 10:12:12 GMT-06:00

Pout

Iin Avg

Cinx IRMS

Total Pd

Cout IRMS

L Ipp

WEBENCH® Design Report   LMR36510FADDAR : LMR36510FADDAR
FINAL 48V-51.6V to 5.00V @ 1A   November 13, 2024 10:12:12 GMT-06:00

IC Pd

Vin=48.0V ▬ Vin=49.8V ▬ Vin=51.6V

Loop Response

Gain ▬ Phase + 180
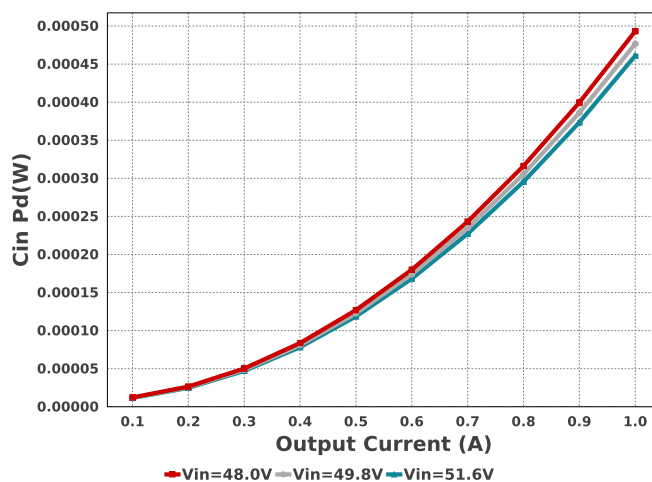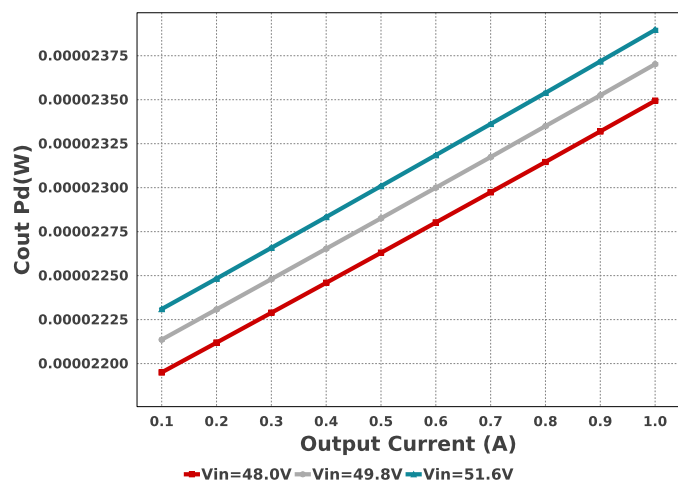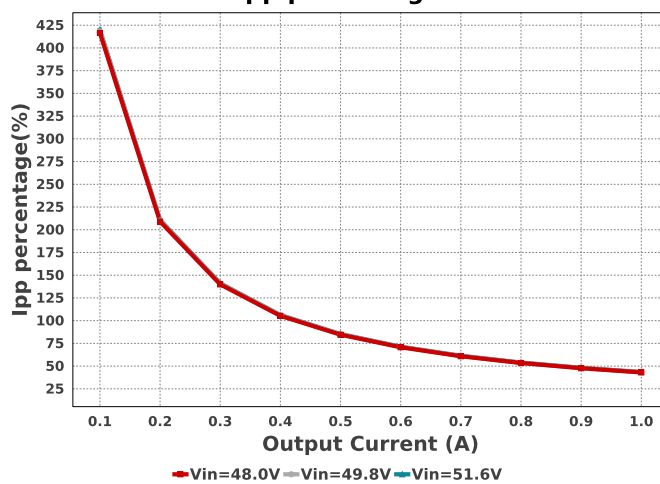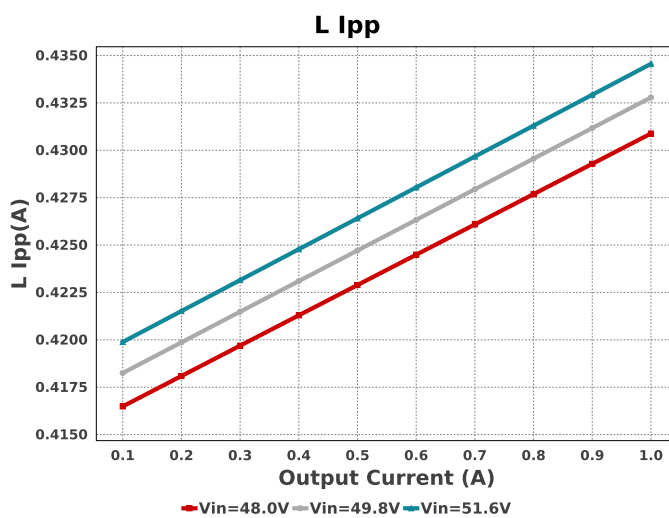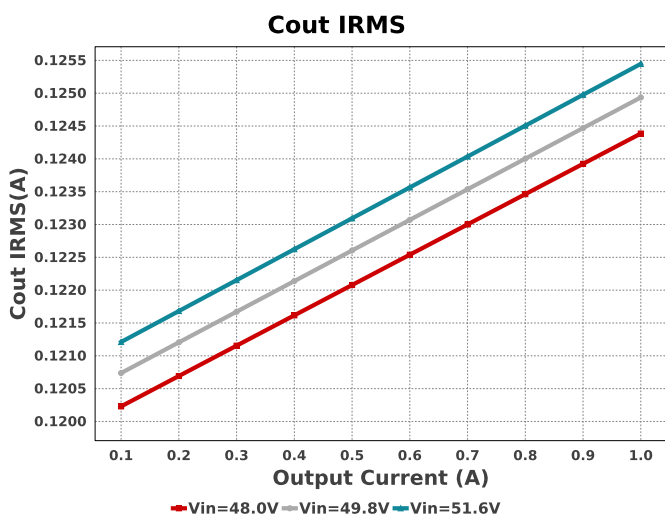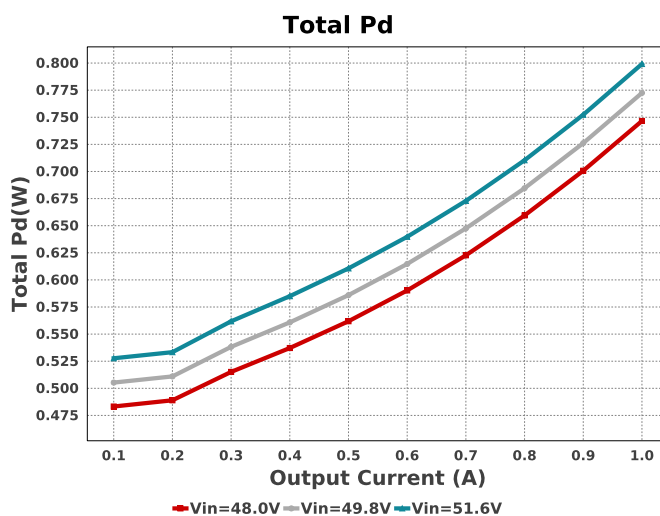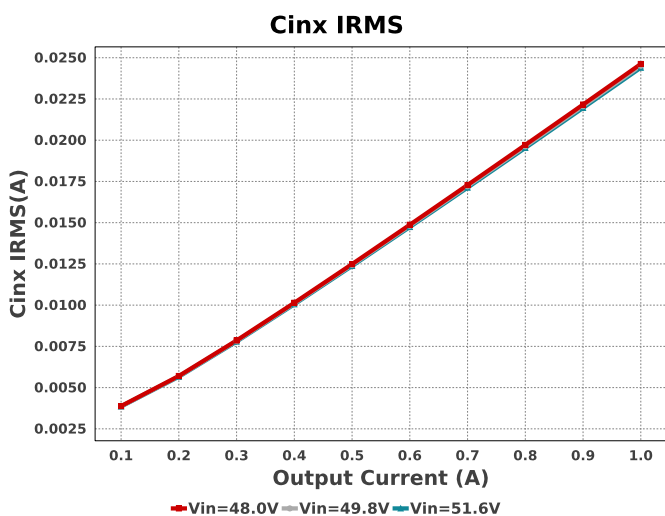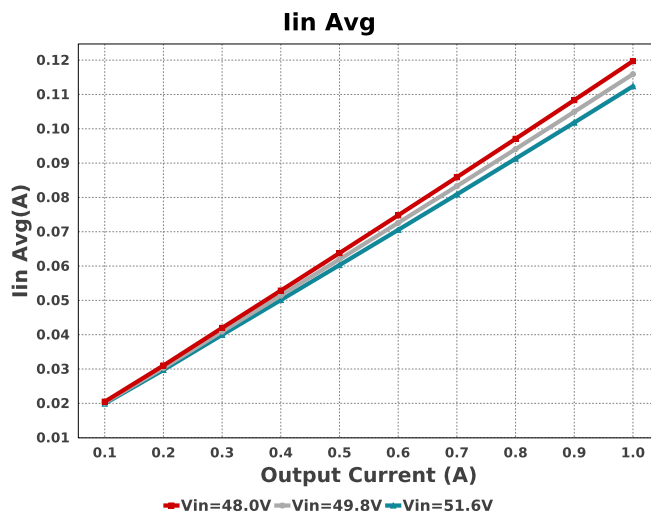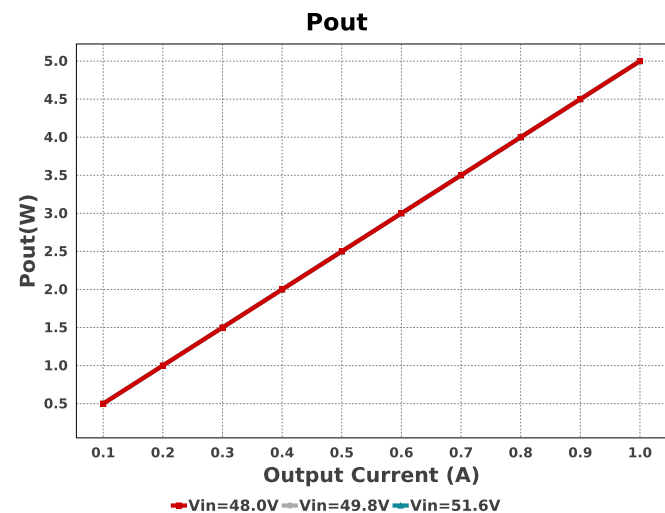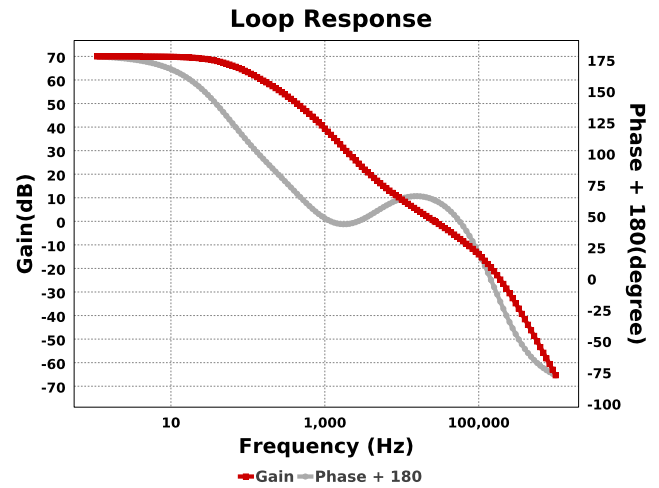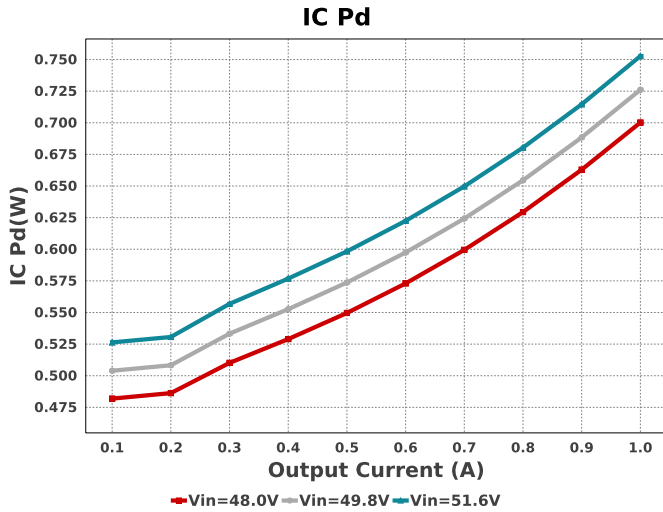
Operating Values

#	Name	Value	Category	Description
1.	BOM Count	12		Total Design BOM count
2.	Total BOM	$2.407		Total BOM Cost
3.	Cin IRMS	279.769 mA	Capacitor	Input capacitor RMS ripple current
4.	Cin Pd	461.01 µW	Capacitor	Input capacitor power dissipation
5.	Cinx IRMS	24.395 mA	Capacitor	Bulk capacitor RMS ripple current
6.	Cinx Pd	595.13 nW	Capacitor	Bulk capacitor power dissipation
7.	Cout IRMS	125.447 mA	Capacitor	Output capacitor RMS ripple current
8.	Cout Pd	23.897 µW	Capacitor	Output capacitor power dissipation
9.	IC Ipk	1.217 A	IC	Peak switch current in IC
10.	IC Pd	752.72 mW	IC	IC power dissipation
11.	IC Tj	61.614 degC	IC	IC junction temperature
12.	IC Tolerance	15.0 mV	IC	IC Feedback Tolerance
13.	ICThetaJA Effective	42.0 degC/W	IC	Effective IC Junction-to-Ambient Thermal Resistance
14.	Iin Avg	112.39 mA	IC	Average input current
15.	Ipp percentage	43.456 %	Inductor	Inductor ripple current percentage (with respect to average inductor current)
16.	L Ipp	434.561 mA	Inductor	Peak-to-peak inductor ripple current
17.	L Pd	45.708 mW	Inductor	Inductor power dissipation
18.	Cin Pd	461.01 µW	Power	Input capacitor power dissipation
19.	Cinx Pd	595.13 nW	Power	Bulk capacitor power dissipation
20.	Cout Pd	23.897 µW	Power	Output capacitor power dissipation
21.	IC Pd	752.72 mW	Power	IC power dissipation
22.	L Pd	45.708 mW	Power	Inductor power dissipation
23.	Total Pd	799.147 mW	Power	Total Power Dissipation
24.	Cross Freq	26.724 kHz	System Information	Bode plot crossover frequency
25.	Duty Cycle	10.116 %	System Information	Duty cycle
26.	Efficiency	86.22 %	System Information	Steady state efficiency
27.	FootPrint	369.0 mm^2	System Information	Total Foot Print Area of BOM components
28.	Frequency	400.0 kHz	System Information	Switching frequency
29.	Gain Marg	-19.596 dB	System Information	Bode Plot Gain Margin
30.	Iout	1.0 A	System Information	Iout operating point
31.	Low Freq Gain	69.99 dB	System Information	Gain at 1Hz
32.	Mode	FCCM	System Information	Conduction Mode
33.	Phase Marg	63.705 deg	System Information	Bode Plot Phase Margin
34.	Pout	5.0 W	System Information	Total output power
35.	Vin	51.6 V	System Information	Vin operating point
36.	Vin p-p	150.282 mV	System Information	Peak-to-peak input voltage
37.	Vout	5.0 V	System Information	Operational Output Voltage

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#	Name	Value	Category	Description
38.	Vout Actual	5.115 V	System Information	Vout Actual calculated based on selected voltage divider resistors
39.	Vout Tolerance	3.15 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
40.	Vout p-p	2.282 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	1.0	Maximum Output Current
VinMax	51.6	Maximum input voltage
VinMin	48.0	Minimum input voltage
Vout	5.0	Output Voltage
base_pn	LMR36510FA	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 48.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

Design Assistance

1. Master key : 8D46410E296FCE97B33F99C6313555A5[v1]

2. **LMR36510FA** Product Folder : http://www.ti.com/product/LMR36510 : contains the data sheet and other resources.

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