CSE240A HW2

Xinhao Luo

TOTAL POINTS

75 / 75

QUESTION 1

Pipelining 35 pts

1.1 MIPS 5 Stage 10 / 10

✓ **- 0 pts Correct**

- 1 pts wrong total cycles

- 1 pts For each instruction with misplaced pipline stage

- 0.5 pts one wrong/missing/extra bypasssing arrow

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- 1 pts For each instruction with misplaced pipline stage

- 0 pts Correct

1.2 MIPS 6 Stage 15 / 15

✓ **- 0 pts Correct**

- 1 pts wrong total cycles

- 1 pts For each instruction with misplaced pipeline stage

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- 0.5 pts one wrong/missing/extra bypasssing arrow

- 0 pts Correct

1.3 Latency and Throughput 10 / 10

✓ **- 0 pts Correct**

- 0 pts incorrect calculation due to previous errors but correct approach

- 2 pts incorrect/missing conclusion on which is better

- 2 pts incorrect/missing latency calculation on 5 stage

- 2 pts incorrect/missing throughput calculation on 6 stage

- 2 pts incorrect/missing latency calculation on 5 stage

- 2 pts incorrect/missing throughput calculation on 6 stage

- 10 pts missing solution

QUESTION 2

MIPS ISA 10 pts

2.1 MIPS Instruction 7 / 7

✓ **- 0 pts Correct**

- 7 pts wrong answer

- 3 pts partially correct

- 2 pts partially wrong

- 1 pts partially wrong

2.2 Hazards 3 / 3

✓ **- 0 pts Correct**

- 3 pts incorrect

- 1 pts partially wrong

- 2 pts partially correct

QUESTION 3

Cache and Memory Hierarchy 30 pts

3.1 Physical Memory 10 / 10

✓ **- 0 pts Correct**

- 2 pts wrong/miss with Mm per DIMM

- 2 pts wrong/miss system mem

- 2 pts wrong meme pre chip

- 10 pts totally wrong / empty

- 1 pts wrong/missing unit or wrong/missing number

- 2 pts wrong with mem pre chip

- **2 pts** No / wrong result

3.2 CPI 10 / 10

✓ **- 0 pts Correct**

- **2 pts** Cycle time incorrectly calculated
- **3 pts** Wrong CPI with only L1 cache
- **5 pts** Wrong CPI with L2 cache added

3.3 10 / 10

✓ **- 0 pts Correct**

- **3 pts** Total no of address bits = 17
- **2 pts** Total no of offset bits = 5
- **2 pts** Total cache blocks = 8
- **1 pts** Incorrect approach

CSE 240A Homework 2

Pipeline and Memory

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Due November 29, 2022 11:59 PM

Instructions

- Submit typed answers to the following questions as a PDF via Gradescope.
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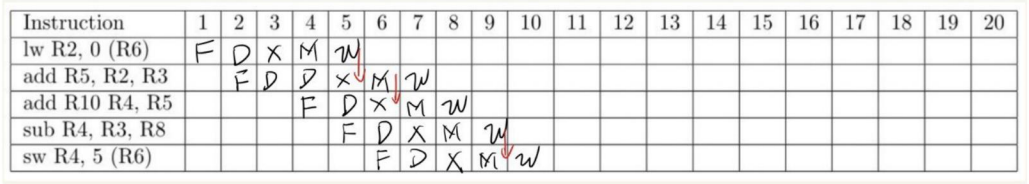
- Homework is to be done individually.
- There are three questions for a total of 75 points (7.5% of your total grade).
- It would be great if you can finish the HW by typing rather than handwriting.

1 Pipelining(35 pts)

1. Fill in the pipline diagram below, assuming it is running on a MIPS 5-stage pipline with stalls done in decode and forwarding whenever needed. Please clearly show pipeline stalls and forwarding with arrows.
   Note: You may not need to fill in all the sycles in the diagram below.



Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
lw R2, 0 (R6)	F	D	X	M	W															
add R5, R2, R3		F	D	D	X	M	W													
add R10 R4, R5				F	D	X	M	W												
sub R4, R3, R8					F	D	X	M	W											
sw R4, 5 (R6)						F	D	X	M	W										

2. A modified 6 stage pipelined processor has been created with the Execute state being split into 2 stages of X1, X2. The Add/Sub values are available after X2 stage

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
lw R2, 0 (R6)	F	D	X_1	X_2	M	W														
add R5, R2, R3		F	D	D	D	X	X_2	M	W											
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sub R4, R3, R8							F	D	X_1	X_2	M	W								
sw R4, 5 (R6)								F	D	X_1	X_2	M	W							

3. If the 5 stage processor has a cycle time of 2 ns and the 6 stage processor has a cycle time of 1.4 ns, which processor design is faster at executing the above code? Compute the Latency, and Throughput of each processor to explain your reasoning. State any assumptions made.

   Cycles for 5 stage CPU: 10
   Latency = 10 * 2ns / 5 = 4ns/inst
   Throughput = 5 / 20 = 1 / 4 inst/ns
   Cycles for 6 stage CPU: 13

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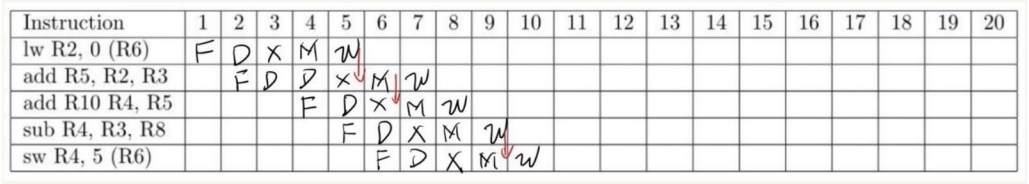

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1.2 MIPS 6 Stage **15 / 15**

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- 0 pts Correct

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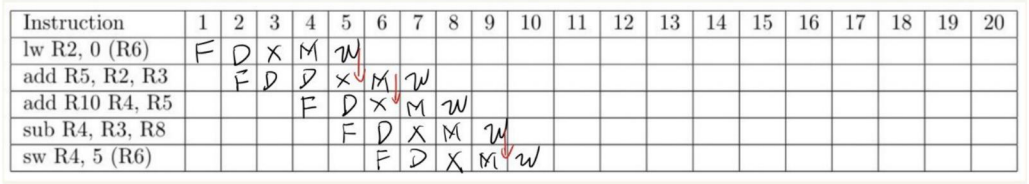

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1.3 Latency and Throughput 10 / 10

✓ **- 0 pts** **Correct**

- 0 pts incorrect calculation due to previous errors but correct approach

- 2 pts incorrect/missing conclusion on which is better

- 2 pts incorrect/missing latency calculation on 5 stage

- 2 pts incorrect/missing throughput calculation on 6 stage

- 2 pts incorrect/missing latency calculation on 5 stage

- 2 pts incorrect/missing throughput calculation on 6 stage

- 10 pts missing solution

Latency = 13 * 1.4ns / 5 = 3.64 ns/inst
Throughput = 5 / 18.2 = 0.275 inst/ns

The second processor could finish the fixed task faster.

2 MIPS ISA (10 pts)

1. Write the MIPS instructions for the following psuedo code. The values of a,b,x and y need to be in R5, R6, R7 and R8 registers respectively at the end of the code.

   a=1
   b=1
   x = a+b
   y = 1+x
   x = y-a
   a = x
   b = y

```
li R5, 1
li R6, 1
add R7, R5, R6
addi R8, R7, 1
sub R7, R8, R5
move R5, R7
move R6, R8
```

2. Mention the hazards that would occur in the above question if no stalls were present. Explain why it would be a hazard?

   There would be data hazards occurred if no stalls were present. There would be read after write dependency within the add, sub and move instructions since the later instructions required registers from the previous instruction's result, which haven't yet write back.

3 Cache and Memory Hierarchy (30 pts)

1. Given a system with:

   - 4 memory channels
   - 4 DRAM DIMMS (1 DIMM per channel)

   Each DIMM has the following:

   - Rank: 4
   - Chips per rank: 8
   - Column size: 8
   - Banks per chip: 16
   - Rows per bank: 32768
   - Columns per bank:1024

   What is the total amount of physical memory in the system?

2.1 MIPS Instruction 7 / 7

✓ **- 0 pts** **Correct**

- 7 pts wrong answer

- 3 pts partially correct

- 2 pts partially wrong

- 1 pts partially wrong

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   What is the total amount of physical memory in the system?

2.2 Hazards 3 / 3

✓ **- 0 pts** **Correct**

- 3 pts incorrect

- 1 pts partially wrong

- 2 pts partially correct

The system has total of 4 DIMMS, each DIMM has:

$$4 \times 8 \times 8 \times 16 \times 32768 \times 1024 = 128Gib = 16GiB \tag{1}$$

So the total would be $16 \times 4 = 64GiB$

2. Given a system :
   The clock frequency of the Processor is 2 Ghz. Assume a CPU base CPI as 1
   With L1 Cache which has a cache miss of 5% and the main memory access time of 200 ns.

   - Calculate the effective new CPI.

$$\text{main memeory miss cycles} = 2 \times 200 = 400cycles \tag{2}$$

$$CPI = 1 + (5\% \times 400) = 21 \tag{3}$$

   - Now consider the system has an L2 cache added which has 0.5% miss rate and an access time of 10ns. Calculate the effective new CPI.

$$\text{L2 miss cycles} = 2 \times 10 = 20cycles \tag{4}$$

$$CPI = 1 + (5\% \times 20) + (0.5\% \times 5\% \times 400) = 2.1 \tag{5}$$

3. Consider a system which is Byte Addressable with
   Main Memory Size : 128 KB
   Cache Size : 256 Bytes
   Cache Block Size : 32 Bytes
   Cache Tag Size : 10 bits
   Find the set associativity of the cache

$$\text{byte offset} = log_2(32) = 5bit \tag{6}$$

$$\text{Address bit} = log_2(128) + 10 = 17bit \tag{7}$$

$$\text{set bit} = 17 - 5 - 10 = 2bit \tag{8}$$

   2 bit means we would have 4 set

$$\text{cache line} = 256/32 = 8 \tag{9}$$

   So set $8/4 = 2$ two-way set associative cache

3.1 Physical Memory 10 / 10

✓ **- 0 pts** **Correct**

- 2 pts wrong/miss with Mm per DIMM

- 2 pts wrong/miss system mem

- 2 pts wrong meme pre chip

- 10 pts totally wrong / empty

- 1 pts wrong/missing unit or wrong/missing number

- 2 pts wrong with mem pre chip

- 2 pts No / wrong result

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3.2 CPI **10 / 10**

✓ **- 0 pts Correct**

- 2 pts Cycle time incorrectly calculated

- 3 pts Wrong CPI with only L1 cache

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3.3 10 / 10

✓ **- 0 pts** **Correct**

- 3 pts Total no of address bits = 17

- 2 pts Total no of offset bits = 5

- 2 pts Total cache blocks = 8

- 1 pts Incorrect approach