♢ CSCI 2500 — Computer Organization ♢
Fall 2019 Optional Make-up Quiz (December 4, 2019)

Please silence and put away all laptops, notes, books, phones, electronic devices, etc. This quiz is designed to take 50 minutes; therefore, for 50% extra time, the expected time is 1 hour and 15 minutes and 100% extra time is 1 hour and 40 minutes. Questions will not be answered except when there is a glaring mistake or ambiguity in the statement of a question. Please do your best to interpret and answer each question.

1. **(12 POINTS)** Given a magnetic disk with 4 KiB disk sectors, 6,000 rpm, 5 ms average seek time, 100 MiB/s transfer rate, 100 µs controller overhead delay, and assuming the disk was initially idling, compute the average time to read 1024 sequential sectors from a single track. Make sure to specify time units. You answers have to be correct to at least 3 significant digits:

   Rotational latency: ____

   Transfer time: ____

   Average read time: ____

2. **(8 POINTS)** Given a 32-bit architecture with byte-addressed main memory, consider a direct-mapped cache with 64 blocks and an 8-word block size. What is the tag and index for address: `0xdecaf1ca`? Present each answer in **hexadecimal**.

   Tag: ____

   Index: ____

3. **(15 POINTS)** Consider a scenario in which die size constraints limited CPU designers to only 64 Kib (i.e., 65,536 bits, not bytes) of space left for the on-chip cache. Given that you want the cache to be write-back, write on allocate, 8-way set-associative with a 2-word block size (and the machine word size is 32 bits), what is the maximum number of sets this cache can have? In other words, how large (in bits) can the index field be? Be sure to account for all required fields, not just the block data. Assume main memory is byte-addressed.

4. **(30 POINTS)** Given a 32-bit architecture with byte-addressed main memory you designed a 2-way set-associative, LRU, write-back, write on allocate primary cache that has a total of 512 blocks with 4 words per block.

   Part a: (14/30 points) Consider the sequence of memory accesses given below and write "hit", "cold miss" ("cold"), "capacity miss" ("cap"), or "conflict miss" ("conf") next to each instruction. Compute the miss rate and express it either as a percentage or as a fraction of the form m/n.

```
load from 0xf00d0020
store  to 0xf00d0020
load from 0xf00d0021
load from 0xf00d1024
load from 0xf00d2029
load from 0xf00d0021
load from 0xf00d1024
store  to 0xf00d0020
```

   Miss rate: [ ]

   Part b: (5/30 points) For this cache configuration, indicate a single change that would lead to fewer cold misses (or write "None" if nothing could be done to decrease cold misses). Assume you cannot increase the total size of your cache (i.e., the total number of bits the cache occupies on the die). Be specific in describing the parameters of this change.

[ ]

   Part c: (5/30 points) For this cache configuration, indicate a single change that would lead to fewer conflict misses (or write "None" if nothing could be done to decrease conflict misses). Assume you cannot increase the total size of your cache (i.e., the total number of bits the cache occupies on the die). Be specific in describing the parameters of this change.

[ ]

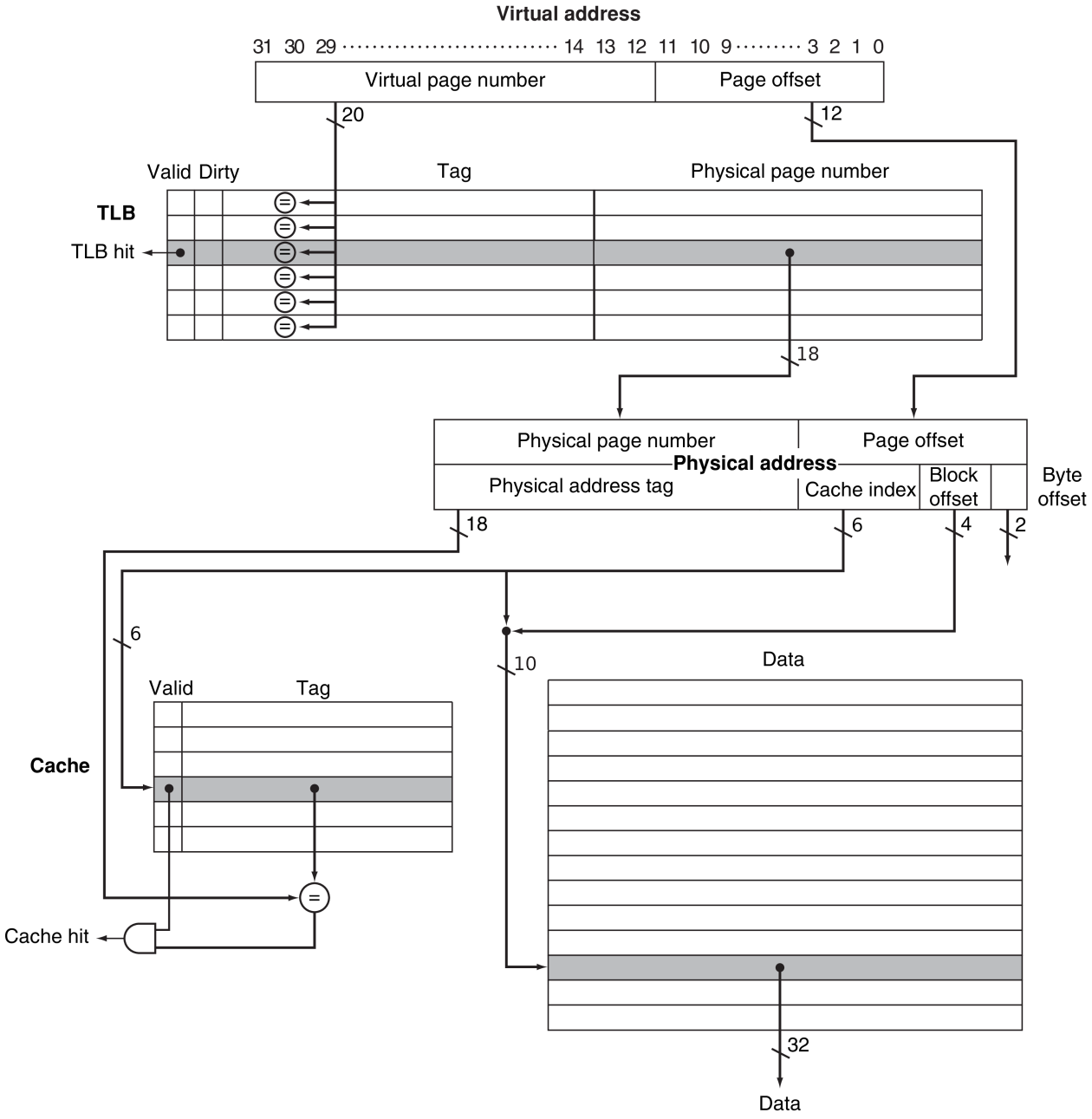
Part d: (3/30 points) In the list of instructions above, use asterisks ("*") to mark at least two instructions that exhibit temporal locality. If there are none, clearly circle the statement below:

There are no instructions in the list above which exhibit temporal locality.

Part e: (3/30 points) In the list of instructions above, use hash signs ("#") to mark at least two instructions that exhibit spatial locality. If there are none, clearly circle the statement below:

There are no instructions in the list above which exhibit spatial locality.

5. **(20 POINTS)** Consider a virtual memory system shown below:



Part a: (2/20 points) This system has which of the following? Clearly circle the **best** answer:

(a) Data cache is virtually indexed and physically tagged
(b) Data cache is virtually indexed and virtually tagged
(c) Data cache is physically indexed and physically tagged
(d) Data cache is physically indexed and virtually tagged
(e) There is no data cache

Part b: (4/20 points) What is the page size in this system, in bytes? [ ]

Part c: (4/20 points) What is the associativity of the TLB?

[ ]

Part d: (5/20 points) What is the associativity of the data cache?

[ ]

Part e: (5/20 points) What is the maximum size of physical memory? Write the value in the box below and clearly circle the corresponding unit of measurement.

[ ] MiB GiB

6. **(15 POINTS)** Consider a virtual memory system with the following parameters:

Virtual address (bits)	Physical DRAM installed	Page size	PTE size (bytes)
43	16 GiB	4 KiB	4

Part a: (7/15 points) How many page table entries (PTEs) are needed? (You may leave your answer in the form 2^n.) [ ]

Part b: (8/15 points) How much physical memory is needed for storing the page table? Write the value in the box below and clearly circle the corresponding unit of measurement.

[ ] MiB GiB