ASSIGNMENT 5

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1 Problem 4.3

1) Improvement

- Without Improvement

$$\begin{aligned} T &= \text{I-Mem} + Mux + ALU + Regs + \text{D-Mem} + Mux \\ &= 400ps + 30ps + 120ps + 200ps + 350ps \\ &= 1130ps \end{aligned} \tag{1}$$

- With Improvement: No MUL, ALU latency is $300ps + 120ps = 420ps$

$$\begin{aligned} T &= \text{I-Mem} + Mux + ALU + Regs + \text{D-Mem} + Mux \\ &= 400ps + 30ps + 420ps + 200ps + 350ps + 30ps \\ &= 1430ps \end{aligned} \tag{2}$$

2) Speed-up: It actually seems like a slow-down

$$\frac{1}{0.95} \times \frac{1130}{1430} = 0.83 \tag{3}$$

3) Cost

Total Cost $1000 + (2 \times 30) + (3 \times 10) + 100 + 200 + 2000 + 500 = 3890$

New Cost $3890 + 600 = 4490$

Relative Cost $3890/4490 = 1.15$

Cost/Performance Ratio $ratio = \frac{\text{Relative Cost}}{\text{Speed-up}} = \frac{1.15}{0.83} = 1.39$

The result suggest that the basic processor is better.

2 Problem 4.4

1) 200ps

2) $200ps + 15ps + 10ps + 70ps + 20ps = 315ps$

3) $200ps + 90ps + 20ps + 90ps + 20ps = 420ps$

4) PC-relative branches instructions, like beq, etc.

5) PC-relative unconditional branches

6) Affected sections

   beq $15 + 10 + 70 = 95$
   add $90 + 20 + 90 = 200$

   In order to affect the latency, shift left 2 has to increase by $200 - 95 = 105ps$.

3 Problem 4.7

1) i) Instruction 0-15: 0000000000010100
After Extended: 00000000000000000000000000010100

ii) Instruction 0-25: 00011000100000000000010100
Shift left 2: 01100010000000000001010000

2) i) Instruction [5-0]: 010100

ii) Instruction [31-26]: 101011
Corresponded to Instruction sw

iii) ALUOp when opcode is sw: 00

iv) Source will be 010100 and 00

3) From part 2, we know that OPcode is sw, which means address will only increase by 4 as normal.
Path: $PC \rightarrow PC + 4 \rightarrow BranchMux \rightarrow JumpMux \rightarrow PC$

4) i) As this is instruction sw, the Mux outputing the address will be PC+4

ii) For sw instruction, the value of RegDst could be 1, the output of this Mux could be [15-11] 00000

iii) Alusrc will be 1 for store and load, which corresponded to the sign extended. The Mux here will be from instruction [0-15] and extended to 00000000000000000000000000010100

iv) SW has nothing to do with data memory, the MemtoReg here will be don't care. The possible output will be 10001 from ALU or the data from address corresponded to 10001 in data memory.

5) i) ALU:

source 1
- Instruction [25-21] 00011
- corresponded to r3 = -3

source 2
- From Q4, we know that Mux here will give 10100

ii) Add (PC+4)

i. PC

ii. 4

iii) Add (Branch)

i. PC+4

ii. From Q4, we know that the extend is 10100, so after left shift it would be 1010000

6) (a) Instruction[25-21] 00011

(b) Instruction[20-16] 00010

(c) From Q4, the regDst for sw is 1, so the value will be 00000

(d) Since it is sw instruction, Reg write here will receive from output from Mux controlled by MemToReg, which is don't care. From Q4, the possible input from mux will be 10001 or data in address of 10001

(e) RegWrite will be 0

4 Problem 4.8

1)
- pipeline: 350ps (largest one)
- non-pipeline: $250ps + 350ps + 150ps + 300ps + 200ps = 1250ps$

2)
- pipeline: $350ps * 5 = 1750ps$
- non-pipeline: $250ps + 350ps + 150ps + 300ps + 200ps = 1250ps$

3) Split the one with the longest latency, ID, and the new clock cycle will be 300ps as MEM become the longest one.

4) Data memory will be used when doing lw and sw, so the rate will be $20\% + 15\% = 35\%$

5) write register will be used when doing lw and alu, so the rate will be $45\% + 20\% = 65\%$