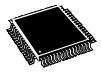
STM32L4S5xx STM32L4S7xx STM32L4S9xx

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 150DMIPS, up to 2MB Flash, 640KB SRAM, LCD-TFT & MIPI DSI, AES+HASH

Datasheet- production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/125 °C temperature range
  - Batch acquisition mode (BAM)
  - 305 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
  - 33 nA Shutdown mode (5 wakeup pins)
  - 125 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - 2.8 µA Stop 2 with RTC
  - 110 µA/MHz Run mode
  - 5 µs wakeup from Stop mode
  - Brownout reset (BOR) in all modes except Shutdown
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 120 MHz, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 409.20 CoreMark® (3.41 CoreMark/MHz @120 MHz)
- Energy benchmark
  - 233 ULPMark™CP score
  - 56.5 ULPMark™PP score
- Clock sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery



LQFP144 (20 × 20)
LQFP100 (14 x 14)
UFBGA169 (7 x 7)
UFBGA144 (10 x 10)
UFBGA132 (7 × 7)
WLCSP144 (pitch 0.4 mm)

  - 3 PLLs for system clock, USB, audio, ADC
- RTC with hardware calendar, alarms and calibration
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- Advanced graphics features
  - Chrom-ART Accelerator (DMA2D) for enhanced graphic content creation
  - Chrom-GRC (GFXMMU) allowing up to 20% of graphic resources optimization
  - MIPI® DSI Host controller with two DSI lanes running at up to 500 Mbit/s each
  - LCD-TFT controller
- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
- Memories
  - 2-Mbyte Flash, 2 banks read-while-write, proprietary code readout protection
  - 640 Kbytes of SRAM including 64 Kbytes with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR, NAND and FRAM memories
  - 2 x Octo-SPI memory interface
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)
  - 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps

  - 2x 12-bit DAC, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x SAIs (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (5x SPIs with the dual Octo-SPI)
  - CAN (2.0B Active) and SDMMC
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- 8- to 14-bit camera interface up to 32 MHz (black and white) or 10 MHz (color)
- Encryption hardware accelerator: AES (128/256-bit key), HASH (SHA-256)
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

Table 1. Device summary

Reference	Part numbers
STM32L4S5xx	STM32L4S5VI, STM32L4S5QI, STM32L4S5ZI, STM32L4S5AI
STM32L4S7xx	STM32L4S7VI, STM32L4S7ZI, STM32L4S7AI
STM32L4S9xx	STM32L4S9VI, STM32L4S9ZI, STM32L4S9AI

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L4Sxxx microcontrollers.

This document should be read in conjunction with the STM32L4Sxxx reference manual (RM0432). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices are an ultra-low-power microcontrollers family (STM32L4+ Series) based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 120 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex-M4 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (2 Mbytes of Flash memory and 640 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), two OctoSPI Flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L4Sxxx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and a firewall.

These devices offer a fast 12-bit ADC (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM). In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one low-power UART
- Two SAIs
- One SDMMC
- One CAN
- One USB OTG full-speed
- Camera interface
- DMA2D controller

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices embed an AES and a HASH hardware accelerator.

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows to backup the RTC and backup the registers.

The STM32L4Sxxx family offers six packages from 100-pin to 169-pin.

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts

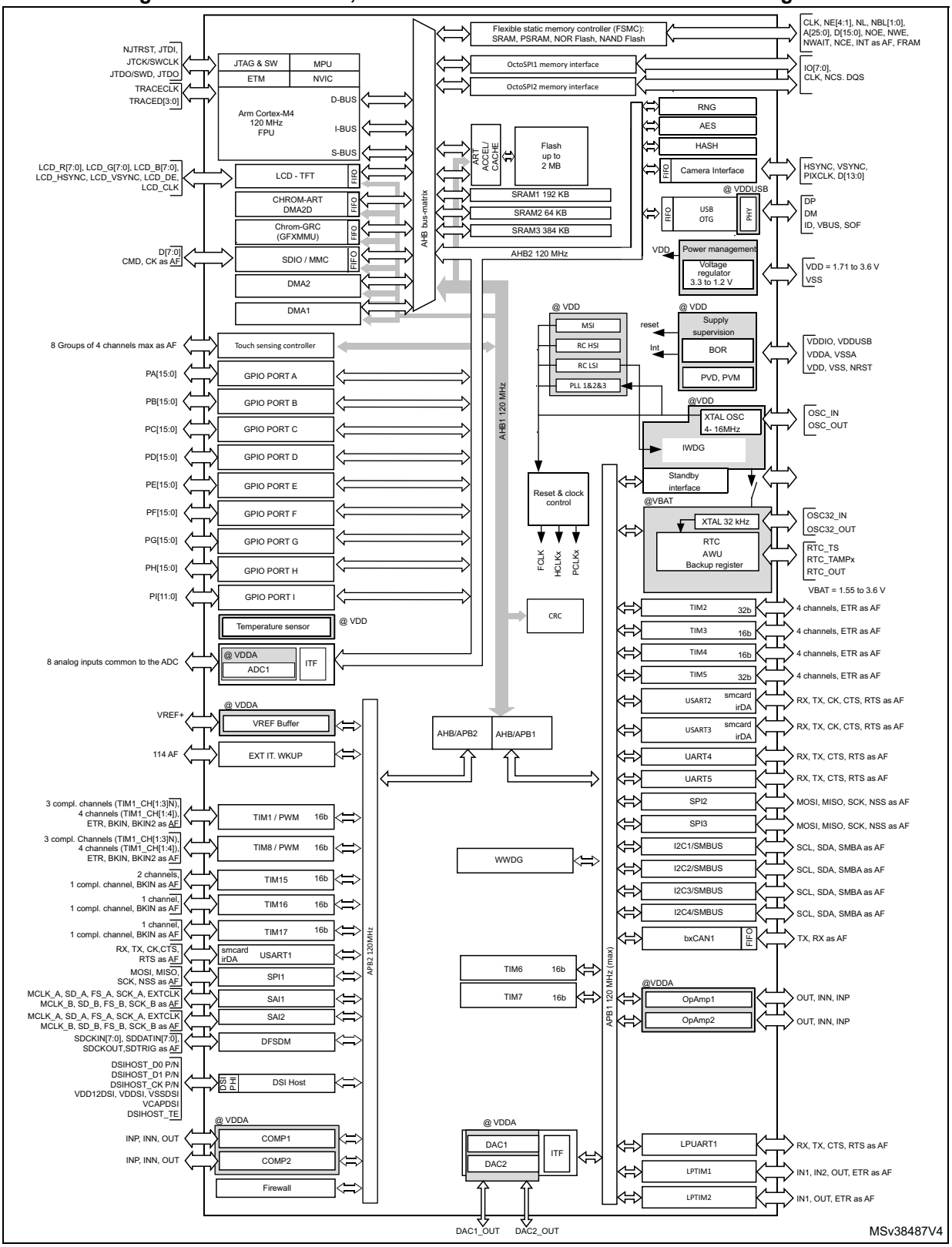
Peripheral		S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
Flash memory		2 Mbytes									
SRAM	System	640 (192 + 64 + 384) Kbytes									
	Backup	128 bytes									
External memory controller for static memories (FSMC)		Yes(1)			Yes						
OctoSPI		1			2						
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low-power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
Comm. interfaces	SPI	3									
	I^2C	4									
	USART/UART UART LPUART	3 2 1									
	SAI	2									
	CAN	1									
	USB OTG FS	Yes									
	SDMMC	Yes									
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes									
Chrom-ART Accelerator		Yes									
Chrom-GRC™		No	Yes		No		Yes		No	Yes	
LCD - TFT		No	Yes	No	No		Yes		No	Yes	
MIPI DSI Host(2)		No		Yes	No			Yes	No		Yes

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts (continued)

Peripheral	S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
Random number generator	Yes									
AES + HASH	Yes									
GPIOs Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112(3) 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1 16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage	1.71 to 3.6 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA 132	LQFP 144 WLCSP144	LQFP 144	LQFP 144, UFBGA 144 WLCSP 144	UFBGA169		
Bootloader	USART 1	USART 2	USART 3	SPI1	SPI2	I2C1	I2C2	I2C3	CAN1	USB through DFU

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4S9xx sales types.
3. 110 GPIOs available for WLCSP144 and LQFP144 packages.

Figure 1. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm® core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm® core, the STM32L4Sxxx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L4Sxxx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator that is optimized for the STM32 industry-standard Arm®Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 150 DMIPS performance at 120 MHz, the accelerator implements an instruction prefetch queue and a branch cache, which increases the program's execution speed from the Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from the Flash memory at a CPU frequency of up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided in up into eight subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32L4Sxxx devices feature 2 Mbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 4 or 8 Kbytes (depending on the read access width).

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 8-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 4-Kbyte granularity.

- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  – In single bank mode, two areas can be selected with 128-bit granularity.
  – In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

3.5 Embedded SRAM

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices feature 640 Kbytes of embedded SRAM. This SRAM is split into three blocks:

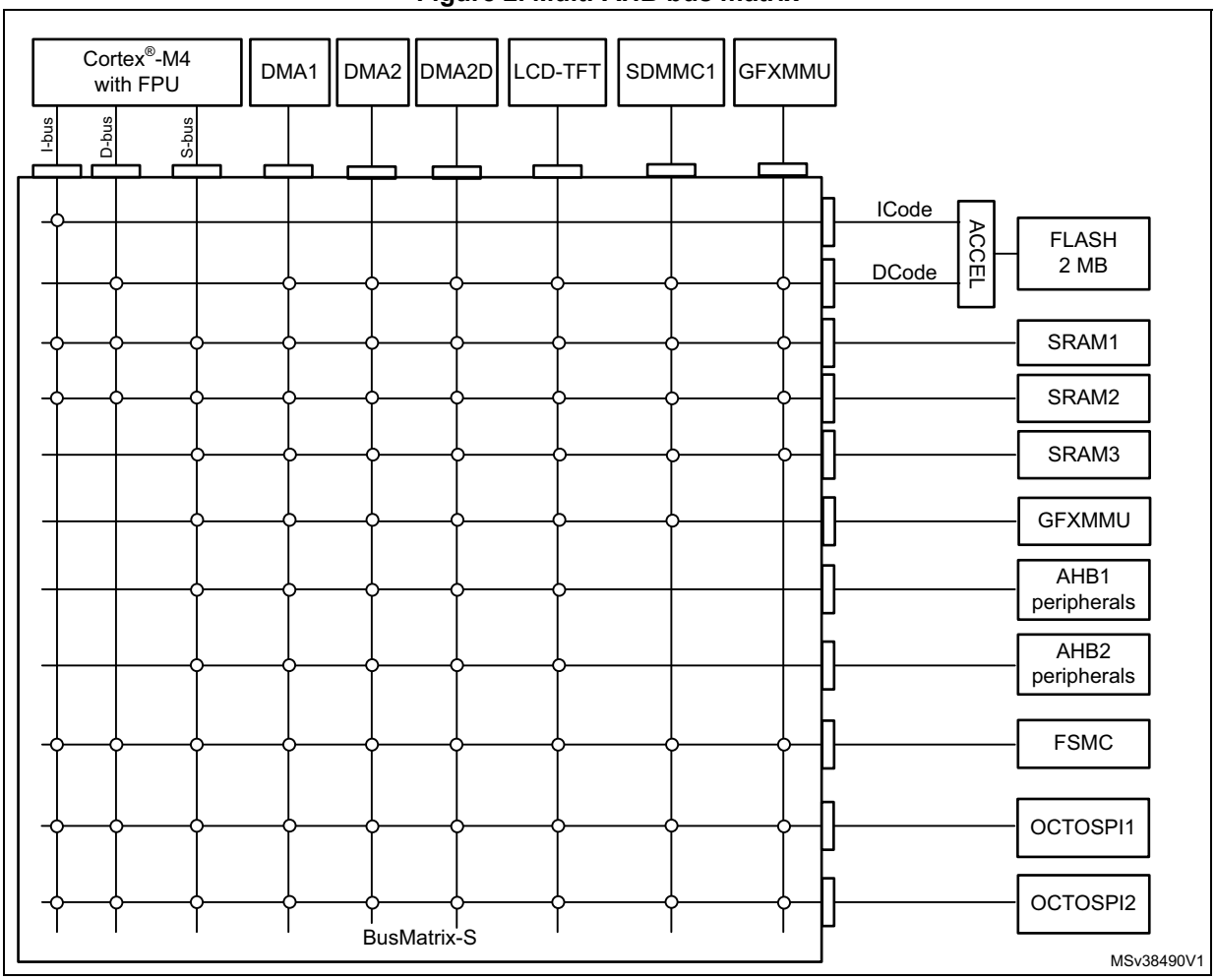
- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.
  These 64 Kbytes SRAM can also be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.
- 384 Kbytes mapped at address 0x2004 0000 - (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, DMA2D, SDMMC1, LCD-TFT and GFXMMU) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Firewall

These devices embed a firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 2048 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 2048 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 192 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.10 Power supply management

3.10.1 Power supply schemes

The STM32L4x devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.

-

  V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- VDDUSB = 3.0 V to 3.6 V
  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.
- VDDIO2 = 1.08 V to 3.6 V
- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.
- VDDDSI is an independent DSI power supply dedicated for is used to supply the DSI regulator and MIPI D-PHY. This supply must be connected to the global VDD.
- VCAPDSI pin is the output of DSI regulator (1.2 V) which must be connected externally to VDD12DSI.
- VDD12DSI pin is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the VDD12DSI pin.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.

  – V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for

packages pinout description).
V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1, SRAM2 and SRAM3. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 3. STM32L4S5xx and STM32L4S7xx power supply overview

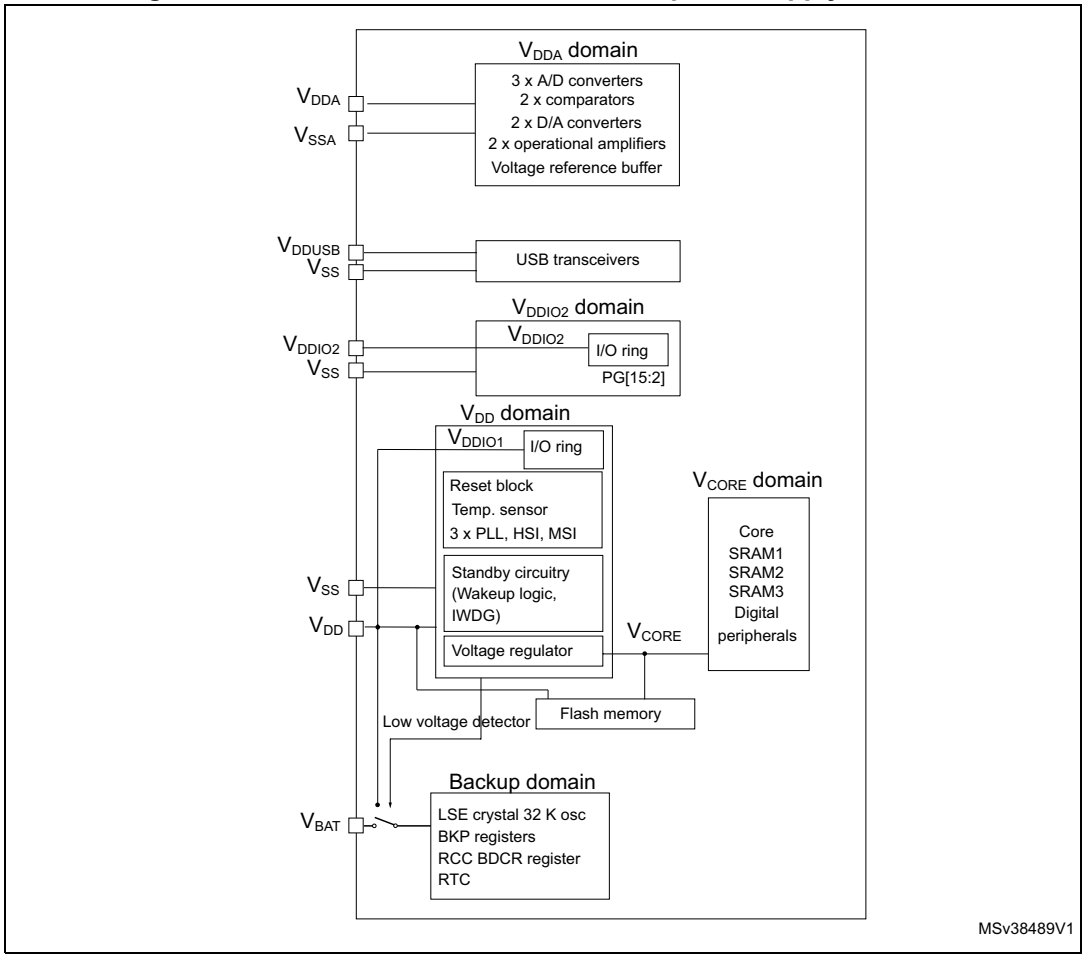
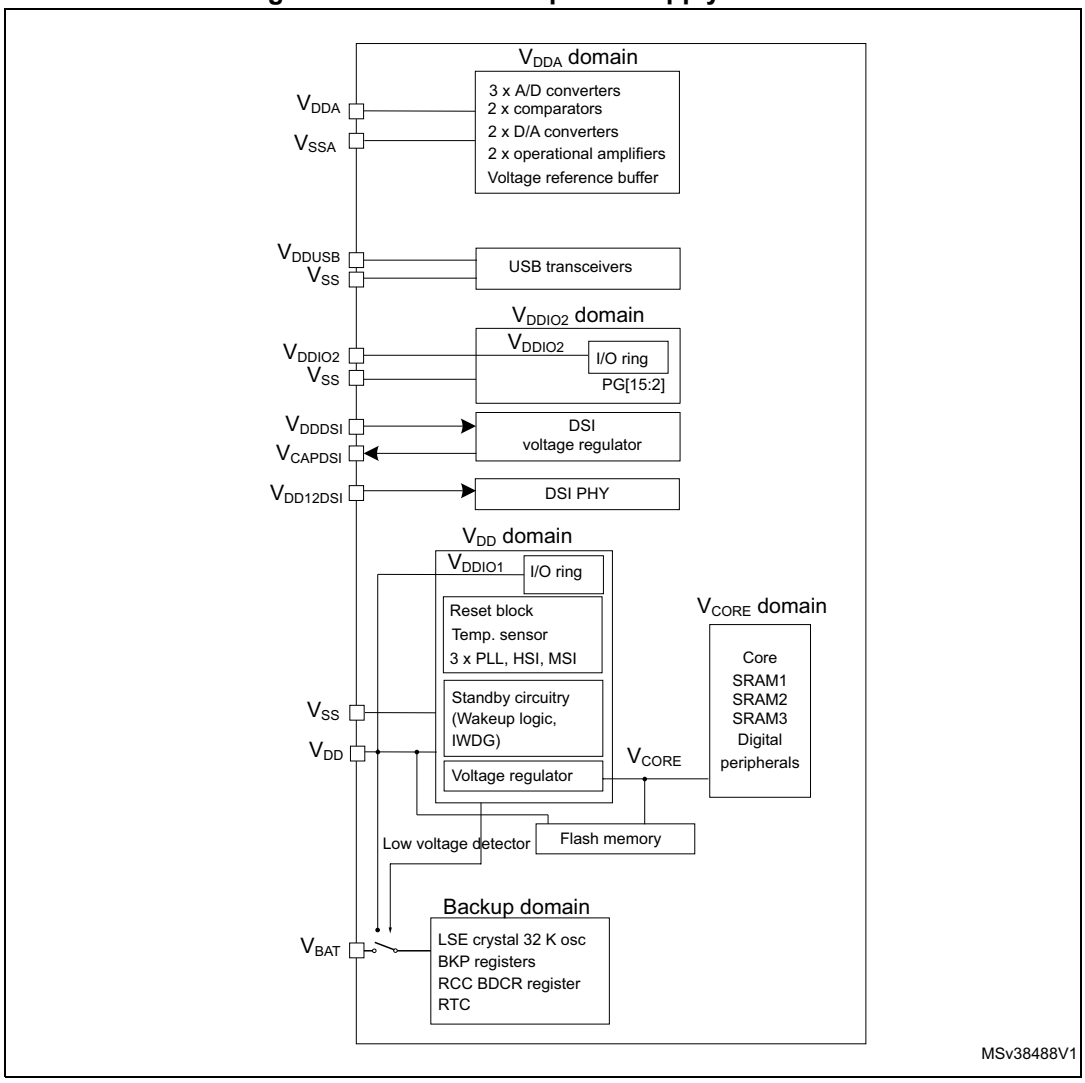


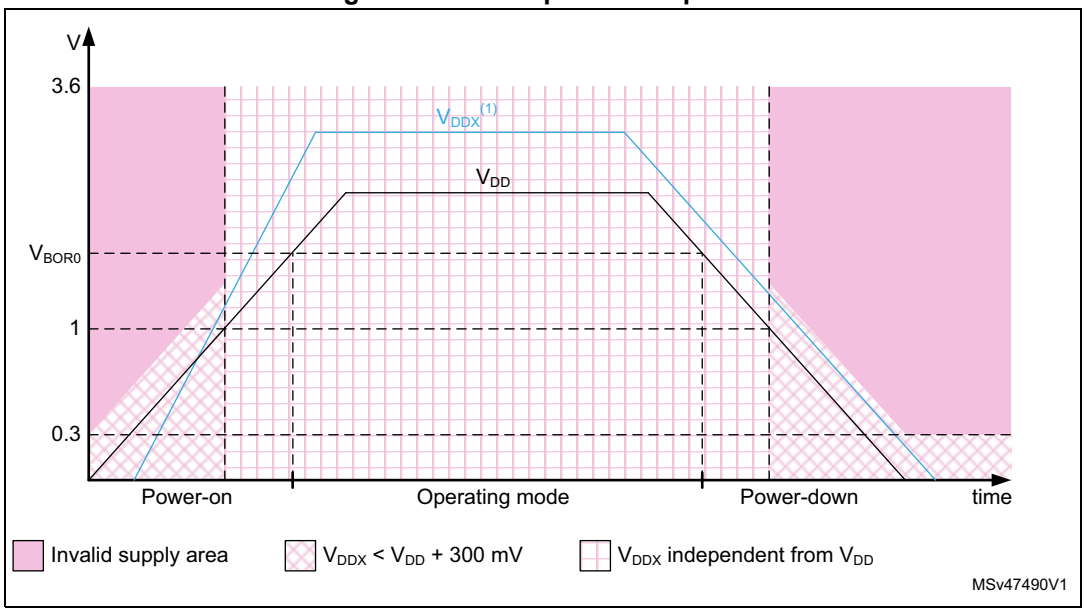
Figure 4. STM32L4S9xx power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}.

3.10.2 Power supply supervisor

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold.

An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes SRAM2 in standby with RAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultra-low-power STM32L4Sxxx devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 boost mode with the CPU running at up to 120 MHz.
- Range 1 normal mode with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by the HSI16.

Note: The USB and DSIHOST can only be used when the main regulator is in range1 boost mode.

3.10.4 Low-power modes

The ultra-low-power STM32L4Sxxx devices support seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources. *Table 4* shows the related STM32L4Sxxx modes overview.

Table 4. STM32L4S5xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range2					All except OTG_FS, RNG, LCD-TFT	
LPRun	LPR	Yes	ON[3]	ON	Any except PLL	All except OTG_FS, RNG, LCD-TFT	N/A
Sleep	Range 1	No	ON[3]	ON[4]	Any	All	Any interrupt or event
	Range 2					All except OTG_FS, RNG, LCD-TFT	
LPSleep	LPR	No	ON[3]	ON[4]	Any except PLL	All except OTG_FS, RNG, LCD-TFT	Any interrupt or event
Stop 0	Range 1	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) OTG_FS[7]
	Range 2						

Table 4. STM32L4S5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) OTG_FS[7]
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[6] LPUART1[5] LPTIM1 *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[6] LPUART1[5] LPTIM1
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[8] BOR, RTC, IWDG
	OFF			Powered Off			
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down[9]	Reset pin 5 I/Os (WKUPx)[8] RTC

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1, SRAM2 and SRAM3 clocks can be gated on or off independently.
5. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
6. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
7. OTG_FS wakeup by resume from suspend and attach detection protocol event.
8. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
9. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM3 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be

retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2, SRAM3 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 5. Functionalities depending on the working mode(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (2 Mbytes)	O(2)	O(2)	O(2)	O(2)	-	-	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	O(4)	-	-	-	-
SRAM3 (384 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y(3)	-	-	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OctoSPIs	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
DMA2D	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-

Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
Camera interface	O	O	O	O	-	-	-	-	-	-	-	-	-
LCD-TFT	O	O	-	-	-	-	-	-	-	-	-	-	-
GFXMMU	O	O	O	O	-	-	-	-	-	-	-	-	-
DSIHOST	O	O	-	-	-	-	-	-	-	-	-	-	-
USB OTG FS	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN(x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
HASH hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off. In Stop 2 mode, the content of SRAM3 is preserved or not depending on the RRSTP bit in PWR_CR1 register.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.10.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.10.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.11 Interconnect matrix

Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 6* for more details.

Table 6. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC DACx DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

Table 6. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADC DACx DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.12 Clocks and startup

The clock controller (see *Figure 6*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

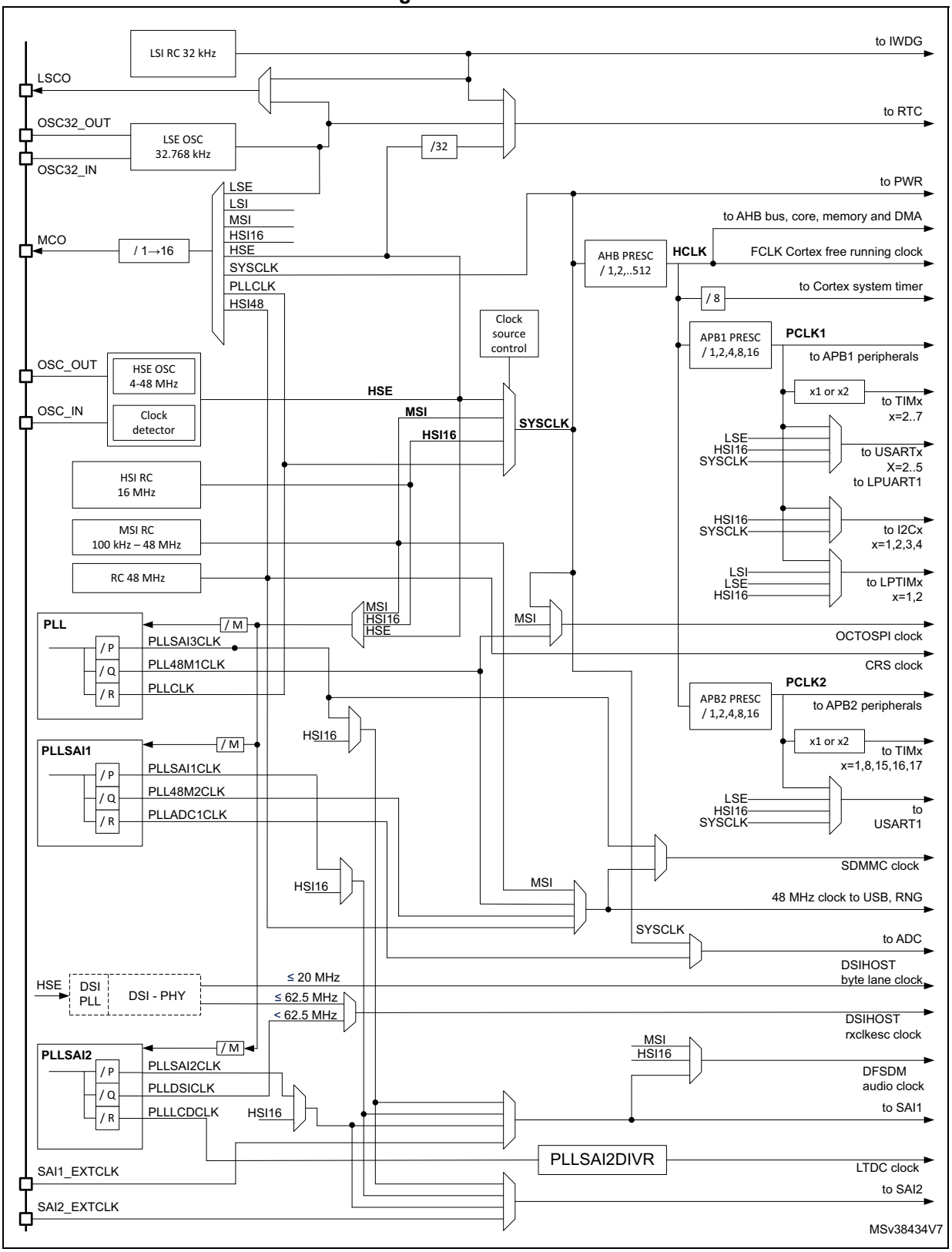
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 120 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG, the two SAIs, LCD-TFT and DSI-HOST. When using DSI-HOST peripheral, the high-speed external crystal (HSE) must be available.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 120 MHz.

Figure 6. Clock tree



3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.15 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

3.16 Chrom-ART Accelerator (DMA2D)

Chrom-ART Accelerator (DMA2D) is a graphic accelerator that offers an advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4 bpp color mode up to 32 bpp direct color. It embeds a dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.17 Chrom-GRC (GFXMMU)

The Chrom-GRC (GFXMMU) is a graphical oriented memory management unit aimed to:

- Optimize memory usage according to the display shape
- Manage packing/unpacking for 24 bpp frame buffers

The Chrom-GRC features:

- Fully programmable display shape to physically store only the visible pixel
- Up to four virtual buffers
- Each virtual buffer have 4096 bytes per line and 1024 lines
- Each virtual buffer can be physically mapped to any system memory
- 24 bpp packing unit to store unpacked 24bpp data in a packed 24 bpp
- Packing/un-packing management per buffer
- Interrupt in case of buffer overflow (1 per buffer)
- Interrupt in case of memory transfer error

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xxdevices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 95 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 36 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.19 Analog-to-digital converter (ADC)

The device embeds a successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.19.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.19.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.19.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.20 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.21 Voltage reference buffer (VREFBUF)

The STM32L4Sxxx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

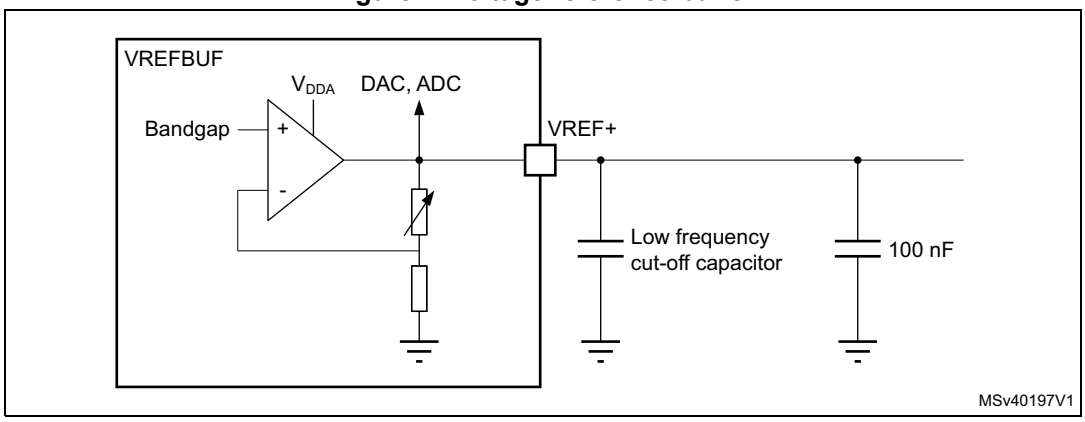
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 7. Voltage reference buffer



3.22 Comparators (COMP)

The STM32L4Sxxx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.23 Operational amplifier (OPAMP)

The STM32L4Sxxx devices embed two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.24 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.25 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- Two displays layers with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

3.26 DSI Host (DSIHOST)

The DSI Host is a dedicated IP that interfaces with the MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

The interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI)
  - Used to transmit information in full bandwidth in the Adapted Command Mode (DBI) through a custom mode
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli

The DSI Host main features are:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted command mode interface through LTDC
- Independently programmable virtual channel ID in
  - Video mode
  - Adapted command mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps

Adapted interface features:

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2 and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

3.27 Digital filter for sigma-delta modulators (DFSDM)

The STM32L4Sxxx devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (pulse density modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16-bit input resolution):
  - Internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high-value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - Monitoring continuously each input serial channel

- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data
  - Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “Regular” or “injected” conversions:
  - “Regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “Injected” conversions for precise timing and with high conversion priority

3.28 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.29 Digital camera interface (DCMI)

The STM32L4Sxxx devices embed a camera interface that can connect with any camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface in order to receive video data.

The camera interface can sustain a data transfer rate up to 54 Mbytes/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication of 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image.

3.30 Advanced encryption standard hardware accelerator (AES)

The STM32L4Sxxx devices embed an AES hardware accelerator that can be used both to encipher and to decipher data using an AES algorithm.

The AES peripheral supports:

- Encryption/decryption using AES Rijndael block cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer
- Register access supporting 32-bit data width only
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data
- Suspend a message if another message with a higher priority needs to be processed.

3.31 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the HMAC (keyed-hash message authentication code) algorithm suitable for a variety of applications.

It computes a message digest (160 bits for the SHA-1 algorithm, 256 bits for the SHA-256 algorithm and 224 bits for the SHA-224 algorithm,128 bits for the MD5 algorithm) for messages of up to (264 - 1) bits, while the HMAC algorithms provide a way of authenticating messages by means of hash functions. The HMAC algorithms consist in calling the SHA-1, SHA-224, SHA-256 or MD5 hash function twice.

3.32 Timers and watchdogs

The STM32L4Sxxx devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

The *Table 10* below compares the features of the advanced control, general-purpose and basic timers.

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.32.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.32.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.32.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L4Sxxx devices (see *Table 10* for differences).
Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.32.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.32.4 Low-power timer (LPTIM1 and LPTIM2)

The STM32L4Sxxx devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only).

3.32.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.32.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.32.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.33 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (alarm, wake-up timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.34 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to *Table 11: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 6: Clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

3.35 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L4Sxxx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

3.36 Low-power universal asynchronous receiver transmitter (LPUART)

The STM32L4Sxxx devices embed one low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.37 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.38 Serial audio interfaces (SAI)

The STM32L4Sxxx devices embed two SAI. Refer to *Table 13: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.

- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 13. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 Word)	X (8 Word)
SPDIF	X	X
PDM	X	-

1. X: supported

3.39 Controller area network (CAN)

The CAN is compliant with the 2.0A and B (active) specifications with a bit rate of up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN has three transmit mailboxes, two receive FIFOS with three stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated.

The CAN peripheral supports:

- CAN protocol version 2.0 A, B Active
- Bit rates of up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - Scalable filter banks: 28 filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.40 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

3.41 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume.

The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

The major features are:

- Combined Rx and Tx FIFO size of 1.25 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- One bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- Eight host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery charging specification revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.42 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.43 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (four memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.44 OctoSPI interface (OctoSPI)

The OctoSPI is a specialized communication interface targetting single, dual, quad or octal SPI memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OctoSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation

The OctoSPI supports two frame formats:

- Classical frame format with command, address, alternate byte, dummy cycles and data phase over 1, 2, 4 or 8 data pins
- HyperBus™ frame format

The OctoSPI offers the following features:

- Three functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where 8 bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR and DTR support
- Data strobe support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode

- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- HyperBus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.45 OctoSPI IO manager (OctoSPIIOM)

The OctoSPI IO Manager is a low level interface allowing:

- Efficient OctoSPI pin assignment with a full IO Matrix (before alternate function map)
- Multiplexing single/dual/quad/octal SPI interface over the same bus

The OctoSPI IO Manager has the following features:

- Support up to two single/dual/quad/octal SPI Interface
- Support up to eight ports for pin assignment
- Fully programmable IO matrix for pin assignment by function (data/control/clock)
- Muxer for Single/Dual/Quad/Octal SPI interface multiplexing over the same bus

3.46 Development support

3.46.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.46.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L4Sxxx devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

Figure 8. STM32L4S5xx and STM32L4S7xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv38036V4

1. The above figure shows the package top view.

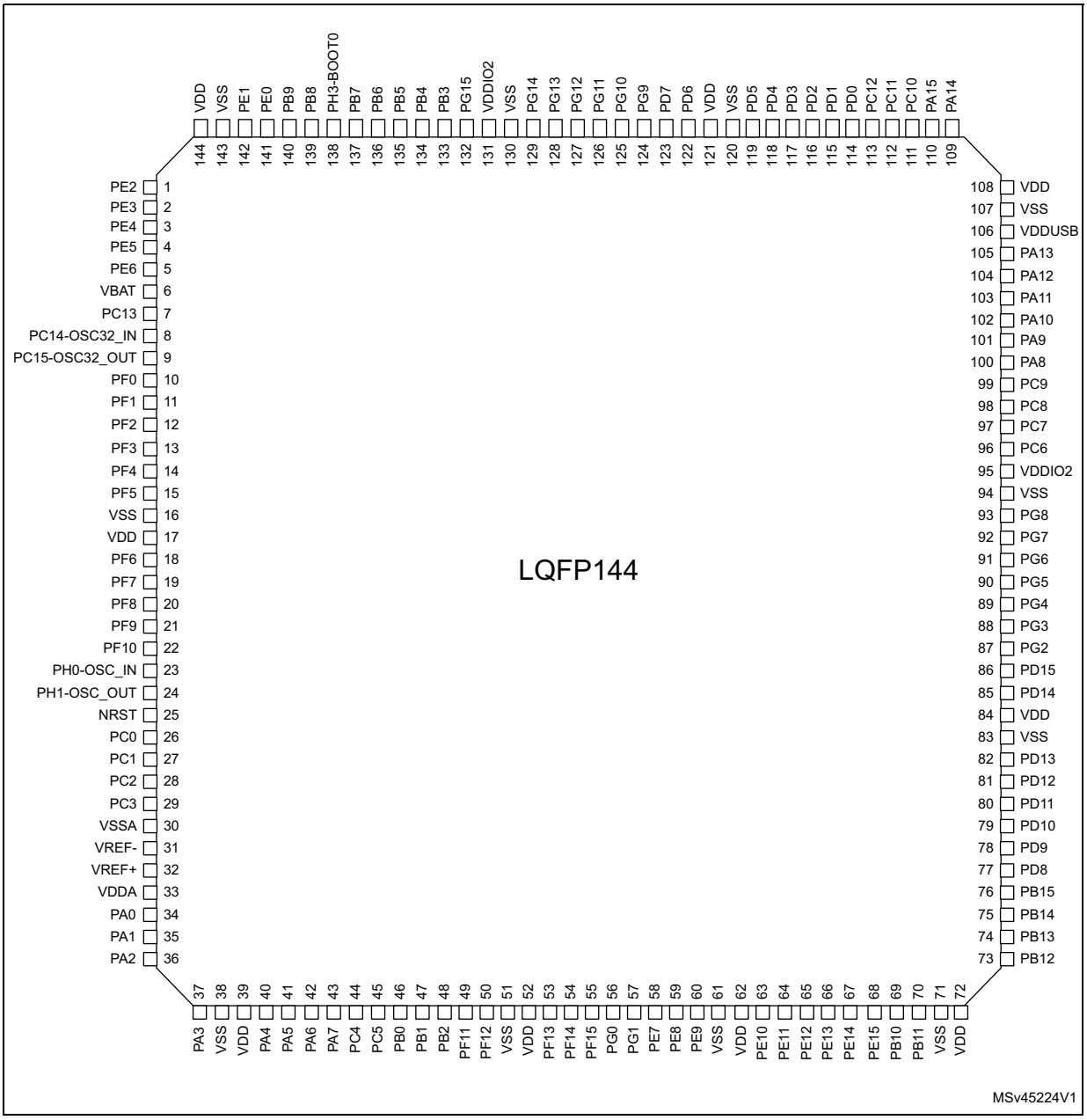
Figure 9. STM32L4S9xx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PH9	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PA10	VDDUSB	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PA8	PA9	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PC8	PG8	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG13	PG4	PG3	PG5	PG7	PC7	PG6	PC9
H	PH0-OSC_IN	VSS	NRST	PF10	PG1	PE10	PB11	PD13	PG2	PD15	PD14	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PG0	PE9	PE15	PD12	PD11	PD10	DSI_D1P	DSI_D1N	VSSDSI
K	PC3	VSSA/VREF-	PA0	PC4	PF15	PE8	PE14	PH4	PD9	PD8	DSI_CKP	DSI_CKN	VSSDSI
L	VREF+	VDDA	PA5	PA6	PB1	PF14	PE7	PE13	PH5	PB15	DSI_D0P	DSI_D0N	VCAPDSI
M	PA1	PA3	VSS	PA7	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB14	VDDDSI
N	PA2	PA4	VDD	PB0	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv45223V2

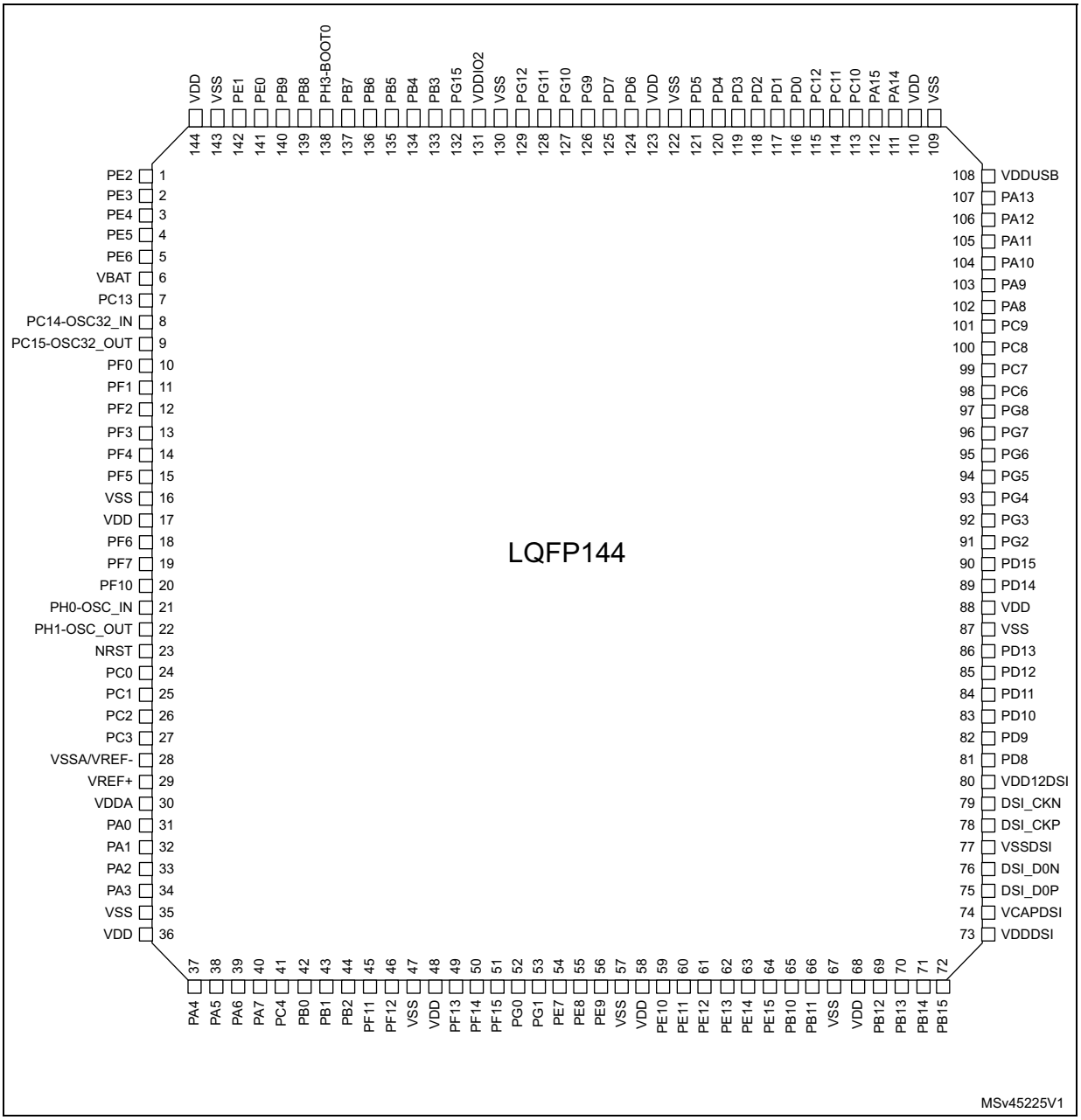
1. The above figure shows the package top view.

Figure 10. STM32L4S5xx and STM32L4S7xx LQFP144 pinout(1)



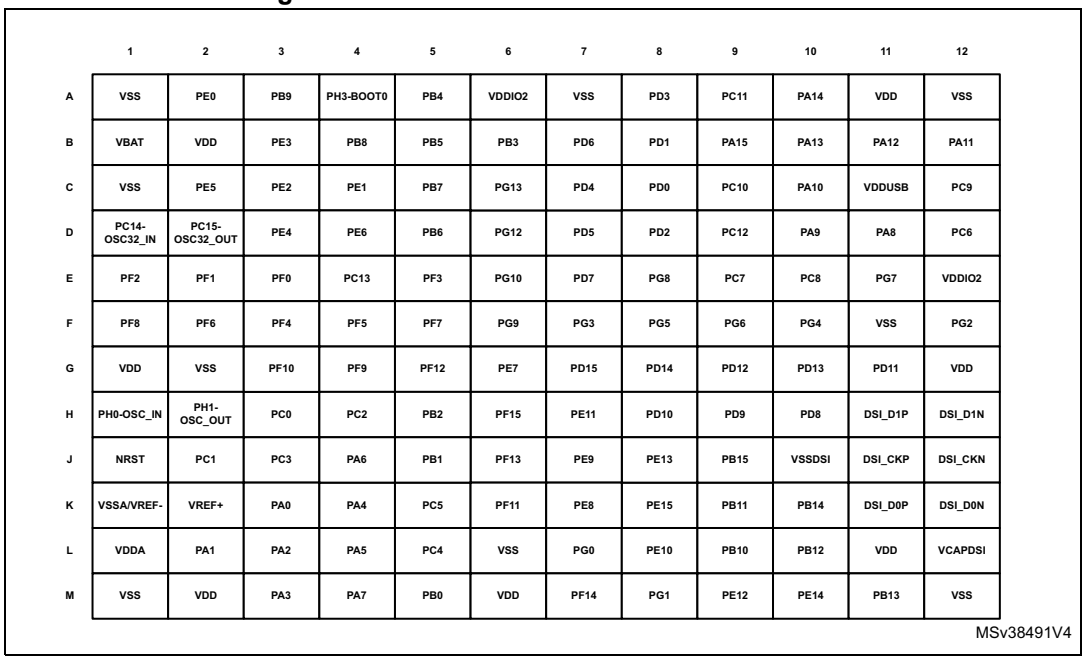
1. The above figure shows the package top view.

Figure 11. STM32L4S9xx LQFP144 pinout(1)



1. The above figure shows the package top view.

Figure 12. STM32L4S9xx UFBGA144 ballout(1)

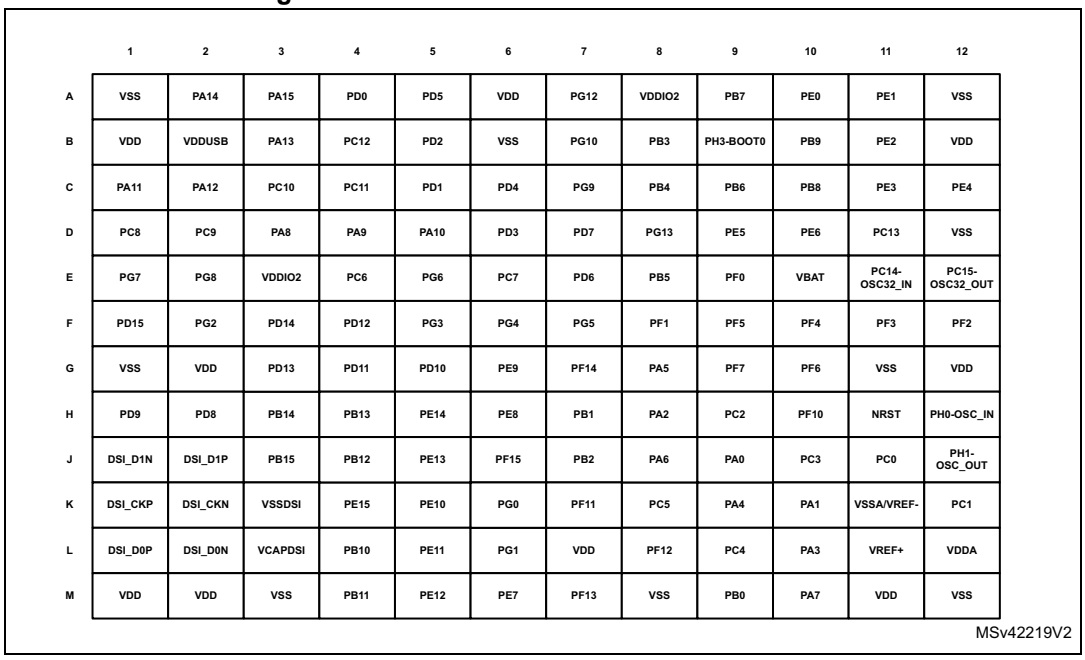


	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PE0	PB9	PH3-BOOT0	PB4	VDDIO2	VSS	PD3	PC11	PA14	VDD	VSS
B	VBAT	VDD	PE3	PB8	PB5	PB3	PD6	PD1	PA15	PA13	PA12	PA11
C	VSS	PE5	PE2	PE1	PB7	PG13	PD4	PD0	PC10	PA10	VDDUSB	PC9
D	PC14-OSC32_IN	PC15-OSC32_OUT	PE4	PE6	PB6	PG12	PD5	PD2	PC12	PA9	PA8	PC6
E	PF2	PF1	PF0	PC13	PF3	PG10	PD7	PG8	PC7	PC8	PG7	VDDIO2
F	PF8	PF6	PF4	PF5	PF7	PG9	PG3	PG5	PG6	PG4	VSS	PG2
G	VDD	VSS	PF10	PF9	PF12	PE7	PD15	PD14	PD12	PD13	PD11	VDD
H	PH0-OSC_IN	PH1-OSC_OUT	PC0	PC2	PB2	PF15	PE11	PD10	PD9	PD8	DSI_D1P	DSI_D1N
J	NRST	PC1	PC3	PA6	PB1	PF13	PE9	PE13	PB15	VSSDSI	DSI_CKP	DSI_CKN
K	VSSA/VREF-	VREF+	PA0	PA4	PC5	PF11	PE8	PE15	PB11	PB14	DSI_D0P	DSI_D0N
L	VDDA	PA1	PA2	PA5	PC4	VSS	PG0	PE10	PB10	PB12	VDD	VCAPDSI
M	VSS	VDD	PA3	PA7	PB0	VDD	PF14	PG1	PE12	PE14	PB13	VSS

MSv38491V4

1. The above figure shows the package top view.

Figure 13. STM32L4S9xx WLCSP144 ballout(1)

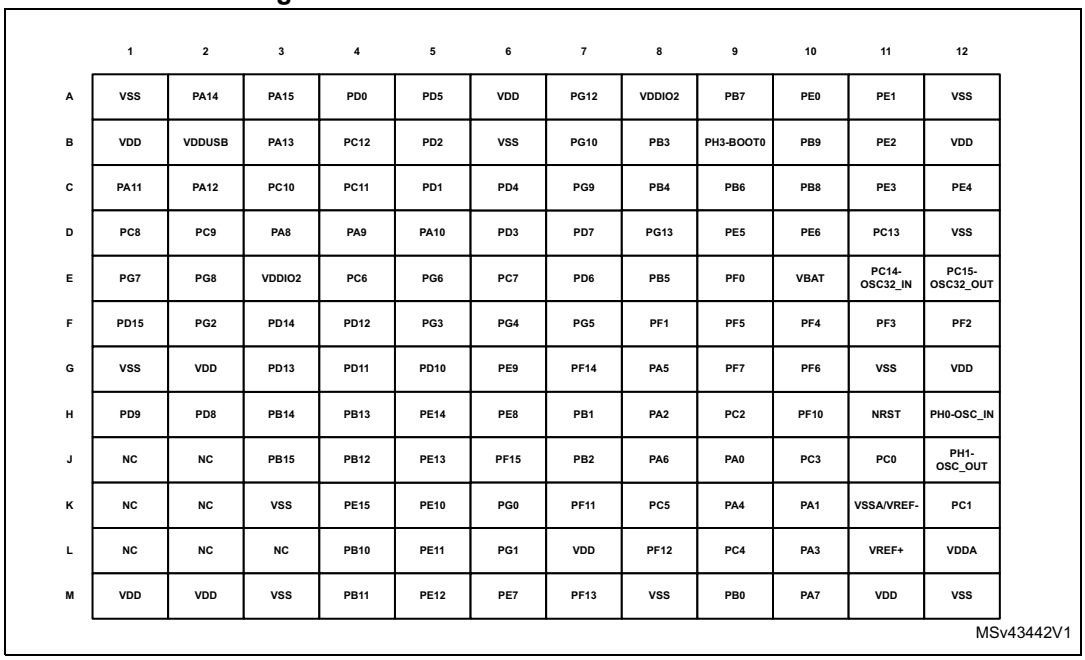


	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	DSI_D1N	DSI_D1P	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	DSI_CKP	DSI_CKN	VSSDSI	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	DSI_D0P	DSI_D0N	VCAPDSI	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv42219V2

1. The above figure shows the package top view

Figure 14. STM32L4S5xx WLCSP144 ballout(1)

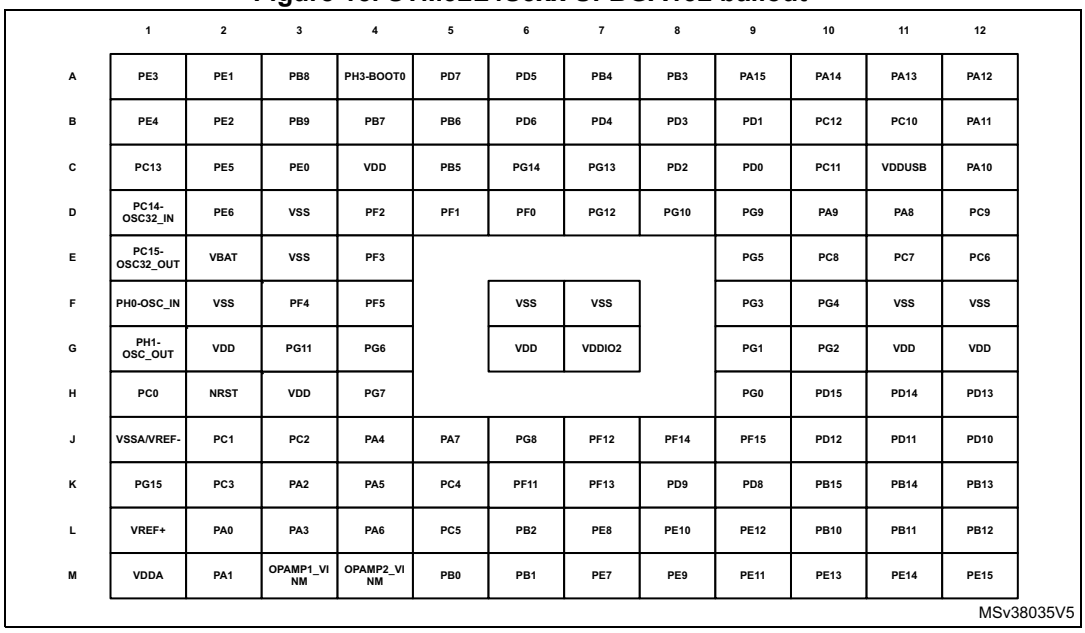


	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PA14	PA15	PD0	PD5	VDD	PG12	VDDIO2	PB7	PE0	PE1	VSS
B	VDD	VDDUSB	PA13	PC12	PD2	VSS	PG10	PB3	PH3-BOOT0	PB9	PE2	VDD
C	PA11	PA12	PC10	PC11	PD1	PD4	PG9	PB4	PB6	PB8	PE3	PE4
D	PC8	PC9	PA8	PA9	PA10	PD3	PD7	PG13	PE5	PE6	PC13	VSS
E	PG7	PG8	VDDIO2	PC6	PG6	PC7	PD6	PB5	PF0	VBAT	PC14-OSC32_IN	PC15-OSC32_OUT
F	PD15	PG2	PD14	PD12	PG3	PG4	PG5	PF1	PF5	PF4	PF3	PF2
G	VSS	VDD	PD13	PD11	PD10	PE9	PF14	PA5	PF7	PF6	VSS	VDD
H	PD9	PD8	PB14	PB13	PE14	PE8	PB1	PA2	PC2	PF10	NRST	PH0-OSC_IN
J	NC	NC	PB15	PB12	PE13	PF15	PB2	PA6	PA0	PC3	PC0	PH1-OSC_OUT
K	NC	NC	VSS	PE15	PE10	PG0	PF11	PC5	PA4	PA1	VSSA/VREF-	PC1
L	NC	NC	NC	PB10	PE11	PG1	VDD	PF12	PC4	PA3	VREF+	VDDA
M	VDD	VDD	VSS	PB11	PE12	PE7	PF13	VSS	PB0	PA7	VDD	VSS

MSv43442V1

1. The above figure shows the package top view.
   NC (not-connected) balls must be left unconnected.

Figure 15. STM32L4S5xx UFBGA132 ballout(1)

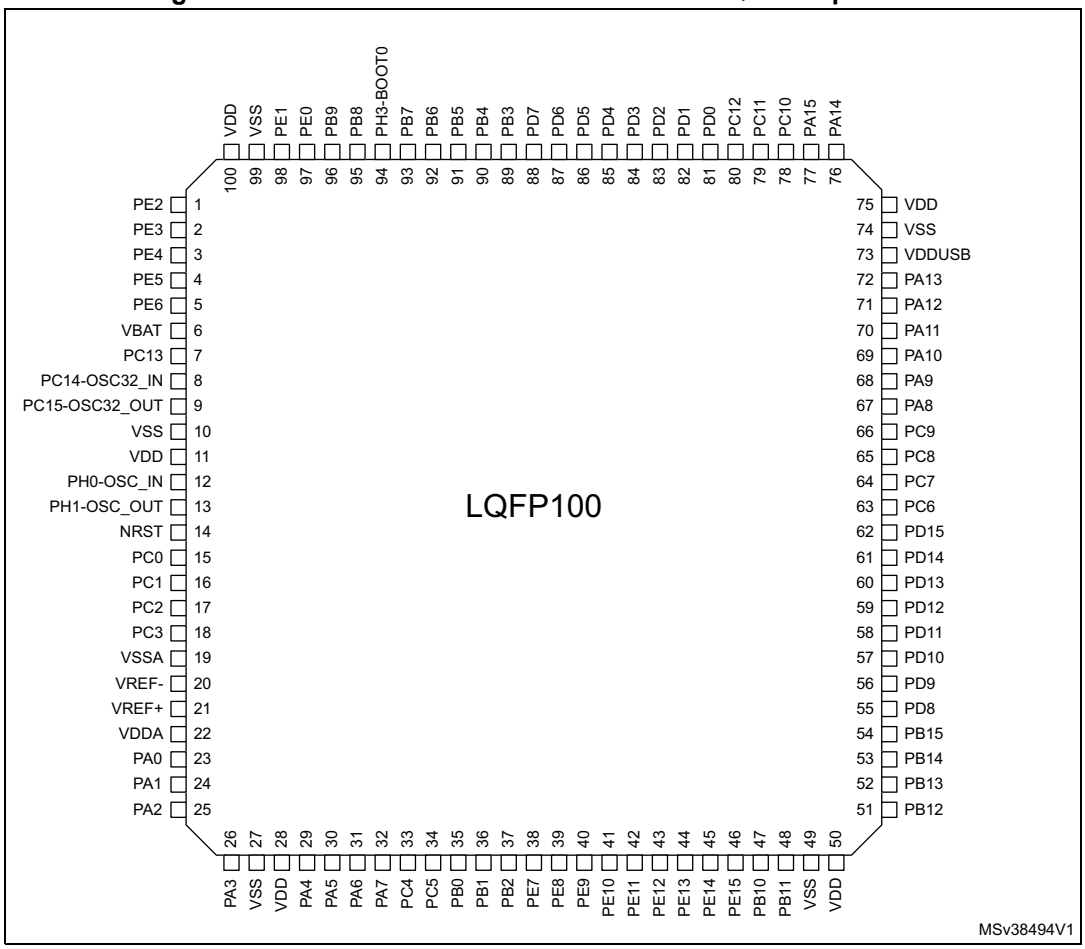


	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv38035V5

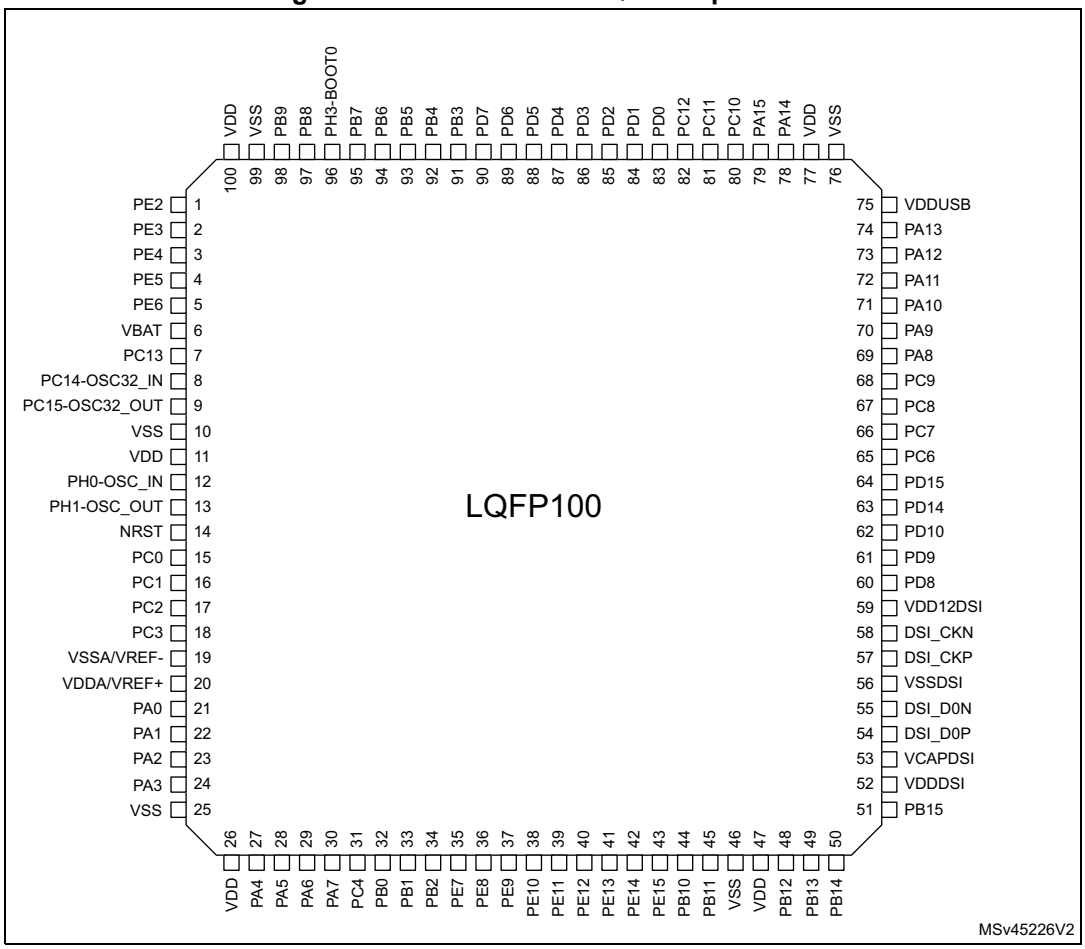
1. The above figure shows the package top view.

Figure 16. STM32L4S5xx and STM32L4S7xx LQFP100 pinout(1)



1. The above figure shows the package top view.

Figure 17. STM32L4S9xx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 14. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_l (2)	I/O, with LCD function supplied by V_{LCD}
		_u (3)	I/O, with USB function supplied by V_{DDUSB}
		_a (4)	I/O, with Analog switch function supplied by V_{DDA}
		_s (5)	I/O supplied only by V_{DDIO2}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 15* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 15* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 15* are: FT_u, FT_lu.
4. The related I/O structures in *Table 15* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Table 15. STM32L4Sxxx pin definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	-	-	-	M11	-	-	-	-	M11	VSS	S	-	-	-	-
-	-	-	-	C1	-	-	-	-	C1	VDD	S	-	-	-	-
-	-	-	-	C3	-	-	-	-	C3	PI11	I/O	FT	-	OCTOSPIM_P2_IO0, EVENTOUT	-
1	B2	1	B11	D3	1	1	C3	B11	D3	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, LCD_R0, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
2	A1	2	C11	D2	2	2	B3	C11	D2	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, OCTOSPIM_P1_DQS, TSC_G7_IO2, LCD_R1, FMC_A19, SAI1_SD_B, EVENTOUT	-
3	B1	3	C12	D1	3	3	D3	C12	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, LCD_B0, FMC_A20, SAI1_FS_A, EVENTOUT	-
4	C2	4	D9	E4	4	4	C2	D9	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, LCD_G0, FMC_A21, SAI1_SCK_A, EVENTOUT	-
5	D2	5	D10	E3	5	5	D4	D10	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7, LCD_G1, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3, WKUP3
6	E2	6	E10	E2	6	6	B1	E10	E2	VBAT	S	-	-	-	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
7	C1	7	D11	E1	7	7	E4	D11	E1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT,WKUP2
8	D1	8	E11	F1	8	8	D1	E11	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
9	E1	9	E12	G1	9	9	D2	E12	G1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	D6	10	E9	F5	-	10	E3	E9	F5	PF0	I/O	FT_f	-	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	D5	11	F8	F4	-	11	E2	F8	F4	PF1	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	D4	12	F12	F3	-	12	E1	F12	F3	PF2	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	-
-	E4	13	F11	G3	-	13	E5	F11	G3	PF3	I/O	FT	-	OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-
-	F3	14	F10	G4	-	14	F3	F10	G4	PF4	I/O	FT	-	OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	-
-	F4	15	F9	G5	-	15	F4	F9	G5	PF5	I/O	FT	-	FMC_A5, EVENTOUT	-
10	F2	16	G11	F2	10	16	L6	G11	F2	VSS	S	-	-	-	-
11	G2	17	G12	G2	11	17	G1	G12	G2	VDD	S	-	-	-	-
-	-	18	G10	-	-	18	F2	G10	-	PF6	I/O	FT	-	TIM5_ETR, TIM5_CH1, OCTOSPIM_P1_IO3, SAI1_SD_B, EVENTOUT	-
-	-	19	G9	-	-	19	F5	G9	-	PF7	I/O	FT	-	TIM5_CH2, OCTOSPIM_P1_IO2, SAI1_MCLK_B, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	-	20	NC	-	-	-	F1	NC	-	PF8	I/O	FT	(3)	TIM5_CH3, OCTOSPIM_P1_IO0, SAI1_SCK_B, EVENTOUT	-
-	-	21	NC	-	-	-	G4	NC	-	PF9	I/O	FT	(3)	TIM5_CH4, OCTOSPIM_P1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	-
-	-	22	H10	H4	-	20	G3	H10	H4	PF10	I/O	FT	-	OCTOSPIM_P1_CLK, DFSDM1_CKOUT, DCMI_D11, SAI1_D3, TIM15_CH2, EVENTOUT	-
12	F1	23	H12	H1	12	21	H1	H12	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	G1	24	J12	J1	13	22	H2	J12	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
14	H2	25	H11	H3	14	23	J1	H11	H3	NRST	I-O	RST	-	-	-
15	H1	26	J11	J2	15	24	H3	J11	J2	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC1_IN1
16	J2	27	K12	J3	16	25	J2	K12	J3	PC1	I/O	FT_fla	-	TRACED0, LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, DFSDM1_CKIN4, LPUART1_TX, OCTOSPIM_P1_IO4, SAI1_SD_A, EVENTOUT	ADC1_IN2
17	J3	28	H9	J4	17	26	H4	H9	J4	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, OCTOSPIM_P1_IO5, EVENTOUT	ADC1_IN3

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
18	K2	29	J10	K1	18	27	J3	J10	K1	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_D1, SPI2_MOSI, OCTOSPIM_P1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC1_IN4
19	-	30	-	-	-	-	-	-	-	VSSA	S	-	-	-	-
20	-	31	-	-	-	-	-	-	-	VREF-	S	-	-	-	-
-	J1	-	K11	K2	19	28	K1	K11	K2	VSSA/VREF-	S	-	-	-	-
21	L1	32	L11	L1	-	29	K2	L11	L1	VREF+	S	-	-	-	VREFBUF_OUT
22	M1	33	L12	L2	-	30	L1	L12	L2	VDDA	S	-	-	-	-
-	-	-	-	-	20	-	-	-	-	VDDA/VREF+	S	-	-	-	-
23	L2	34	J9	K3	21	31	K3	J9	K3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS_NSS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC1_IN5, RTC_TAMP2, WKUP1
-	M3	-	-	M1	-	-	-	-	-	OPAMP1_VINM	I	TT	-	-	-
24	M2	35	K10	N2	22	32	L2	K10	M1	PA1	I/O	FT_la	-	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, OCTOSPIM_P1_DQS, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC1_IN6
25	K3	36	H8	N1	23	33	L3	H8	N1	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, OCTOSPIM_P1_NCS, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC1_IN7, WKUP4/LSCO

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
26	L3	37	L10	M2	24	34	M3	L10	M2	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI1_CK1, USART2_RX, LPUART1_RX, OCTOSPIM_P1_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC1_IN8
27	E3	38	M12	H2	25	35	G2	M12	H2	VSS	S	-	-	-	-
28	H3	39	M11	N3	26	36	M2	M11	N3	VDD	S	-	-	-	-
29	J4	40	K9	L3	27	37	K4	K9	N2	PA4	I/O	TT_a	-	OCTOSPIM_P1_NCS, SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC1_IN9, DAC1_OUT1
30	K4	41	G8	K4	28	38	L4	G8	L3	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC1_IN10, DAC1_OUT2
31	L4	42	J8	M4	29	39	J4	J8	L4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK, SPI1_MISO, USART3_CTS_NSS, LPUART1_CTS, OCTOSPIM_P1_IO3, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC1_IN11
-	M4	-	-	N4	-	-	-	-	-	OPAMP2_VINM	I	TT	-	-	-
32	J5	43	M10	L4	30	40	M4	M10	M4	PA7	I/O	FT_fla	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPIM_P1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC1_IN12

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
33	K5	44	L9	H5	31	41	L5	L9	K4	PC4	I/O	FT_a	-	USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM, ADC1_IN13
34	L5	45	K8	J5	-	-	K5	K8	-	PC5	I/O	FT_a	-	SAI1_D3, USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
35	M5	46	M9	K5	32	42	M5	M9	N4	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN15
36	M6	47	H7	L5	33	43	J5	H7	L5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, OCTOSPIM_P1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
37	L6	48	J7	N5	34	44	H5	J7	N5	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPIM_P1_DQS, LCD_B1, EVENTOUT	COMP1_INP
-	K6	49	K7	M5	-	45	K6	K7	M5	PF11	I/O	FT	-	LCD_DE, DCMI_D12, DSI_TE, EVENTOUT	-
-	J7	50	L8	N6	-	46	G5	L8	N6	PF12	I/O	FT	-	OCTOSPIM_P2_DQS, LCD_B0, FMC_A6, EVENTOUT	-
-	-	51	M8	-	-	47	M1	M8	-	VSS	S	-	-	-	-
-	-	52	L7	N7	-	48	M6	L7	N7	VDD	S	-	-	-	-
-	K7	53	M7	M6	-	49	J6	M7	M6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, LCD_B1, FMC_A7, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	J8	54	G7	L6	-	50	M7	G7	L6	PF14	I/O	FT_f	-	I2C4_SCL, DFSDM1_CKIN6, TSC_G8_IO1, LCD_G0, FMC_A8, EVENTOUT	-
-	J9	55	J6	K6	-	51	H6	J6	K5	PF15	I/O	FT_f	-	I2C4_SDA, TSC_G8_IO2, LCD_G1, FMC_A9, EVENTOUT	-
-	H9	56	K6	J6	-	52	L7	K6	J5	PG0	I/O	FT	-	OCTOSPIM_P2_IO4, TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	G9	57	L6	H6	-	53	M8	L6	H5	PG1	I/O	FT	-	OCTOSPIM_P2_IO5, TSC_G8_IO4, FMC_A11, EVENTOUT	-
38	M7	58	M6	L7	35	54	G6	M6	L7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, LCD_B6, FMC_D4, SAI1_SD_B, EVENTOUT	-
39	L7	59	H6	K7	36	55	K7	H6	K6	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, LCD_B7, FMC_D5, SAI1_SCK_B, EVENTOUT	-
40	M8	60	G6	J7	37	56	J7	G6	J6	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, LCD_G2, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	F6	61	-	M7	-	57	C1	-	M7	VSS	S	-	-	-	-
-	G6	62	-	-	-	58	-	-	-	VDD	S	-	-	-	-
41	L8	63	K5	H7	38	59	L8	K5	H6	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, OCTOSPIM_P1_CLK, LCD_G3, FMC_D7, SAI1_MCLK_B, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
42	M9	64	L5	N8	39	60	H7	L5	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT	-
43	L9	65	M5	M8	40	61	M9	M5	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, OCTOSPIM_1_IO0, LCD_G5, FMC_D9, EVENTOUT	-
44	M10	66	J5	L8	41	62	J8	J5	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT	-
45	M11	67	H5	K8	42	63	M10	H5	K7	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPIM_P1_IO2, LCD_G7, FMC_D11, EVENTOUT	-
46	M12	68	K4	J8	43	64	K8	K4	J7	PE15	I/O	FT	-	TIM1_BKIN, SPI1_MOSI, OCTOSPIM_P1_IO3, LCD_R2, FMC_D12, EVENTOUT	-
47	L10	69	L4	N9	44	65	L9	L4	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPIM_P1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
48	L11	70	M4	H8	45	66	K9	M4	H7	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, OCTOSPIM_P1_NCS, DSI_TE, COMP2_OUT, EVENTOUT	-
-	-	-	-	K9	-	-	-	-	K8	PH4	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_DQS, EVENTOUT	-
-	-	-	-	L9	-	-	-	-	L9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK, EVENTOUT	-
-	-	-	-	N10	-	-	-	-	N10	PH8	I/O	FT_f	-	I2C3_SDA, OCTOSPIM_P2_IO3, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	M9	-	-	-	-	M9	PH10	I/O	FT	-	TIM5_CH1, OCTOSPIM_P2_IO5, DCMI_D1, EVENTOUT	-
-	-	-	-	M10	-	-	-	-	M10	PH11	I/O	FT	-	TIM5_CH2, OCTOSPIM_P2_IO6, DCMI_D2, EVENTOUT	-
-	-	-	-	C2	-	-	-	-	C2	VSS	S	-	-	-	-
49	F12	71	M3	A7	46	67	M12	M3	A7	VSS	S	-	-	-	-
50	G12	72	M1	N11	47	68	L11	M1	N11	VDD	S	-	-	-	-
51	L12	73	J4	N12	48	69	L10	J4	N12	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
52	K12	74	H4	N13	49	70	M11	H4	N13	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM1_CKIN1, USART3_CTS_NSS, LPUART1_CTS, TSC_G1_IO2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
53	K11	75	H3	M13	50	71	K10	H3	M12	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
54	K10	76	J3	M12	51	72	J9	J3	L10	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	M2	L12	-	-	-	M2	-	VDD	S	-	-	-	-
-	-	-	-	-	52	73	-	-	M13	VDDDSI	S	-	-	-	-
-	-	-	-	L13	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	53	74	L12	L3	L13	VCAPDSI	S	-	-	-	-
-	-	-	-	-	54	75	K11	L1	L11	DSI_D0P	I/O	-	(3)	-	-
-	-	-	-	-	55	76	K12	L2	L12	DSI_D0N	I/O	-	(3)	-	-
-	-	-	-	-	56	77	-	-	J13	VSSDSI	S	-	-	-	-
-	-	-	-	-	57	78	J11	K1	K11	DSI_CKP	I/O	-	(3)	-	-
-	-	-	-	-	58	79	J12	K2	K12	DSI_CKN	I/O	-	(3)	-	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	-	-	-	-	59	80	-	-	-	VDD12DSI	S	-	-	-	-
-	-	-	-	-	-	-	H11	J2	J11	DSI_D1P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	H12	J1	J12	DSI_D1N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	J10	K3	K13	VSSDSI	S	-	-	-	-
-	-	-	K3	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	L3	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	L1	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	L2	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	K1	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	K2	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	J2	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	J1	-	-	-	-	-	-	NC	-	-	-	-	-
55	K9	77	H2	L11	60	81	H10	H2	K10	PD8	I/O	FT	-	USART3_TX, DCMI_HSYNC, LCD_R3, FMC_D13, EVENTOUT	-
56	K8	78	H1	L10	61	82	H9	H1	K9	PD9	I/O	FT	-	USART3_RX, DCMI_PIXCLK, LCD_R4, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
57	J12	79	G5	J13	62	83	H8	G5	J10	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, LCD_R5, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	-	H13	-	-	-	-	-	VDD	S	-	-	-	-
58	J11	80	G4	K12	-	84	G11	G4	J9	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS_NSS, TSC_G6_IO2, LCD_R6, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
59	J10	81	F4	K11	-	85	G9	F4	J8	PD12	I/O	FT_fl	-	TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_R7, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
60	H12	82	G3	K13	-	86	G10	G3	H8	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	83	G1	H12	-	87	-	G1	H12	VSS	S	-	-	-	-
-	-	84	G2	G13	-	88	G12	G2	H13	VDD	S	-	-	-	-
61	H11	85	F3	K10	63	89	G8	F3	H11	PD14	I/O	FT	-	TIM4_CH3, LCD_B2, FMC_D0, EVENTOUT	-
62	H10	86	F1	H11	64	90	G7	F1	H10	PD15	I/O	FT	-	TIM4_CH4, LCD_B3, FMC_D1, EVENTOUT	-
-	G10	87	F2	J12	-	91	F12	F2	H9	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	F9	88	F5	J11	-	92	F7	F5	G8	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	F10	89	F6	J10	-	93	F10	F6	G7	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	E9	90	F7	J9	-	94	F8	F7	G9	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	G4	91	E5	G11	-	95	F9	E5	G12	PG6	I/O	FT_s	-	OCTOSPIM_P1_DQS, I2C3_SMBA, LPUART1_RTS_DE, LCD_R1, DSI_TE, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	H4	92	E1	H10	-	96	E11	E1	G10	PG7	I/O	FT_fs	-	SAI1_CK1, I2C3_SCL, OCTOSPIM_P2_DQS, DFSDM1_CKOUT, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	J6	93	E2	H9	-	97	E8	E2	F10	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	94	D12	F13	-	-	F11	D12	F13	VSS	S	-	-	-	-
-	-	95	E3	F12	-	-	E12	E3	F12	VDDIO2	S	-	-	-	-
63	E12	96	E4	F11	65	98	D12	E4	F11	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, SDMMC1_D0DIR, TSC_G4_IO1, DCMI_D0, LCD_R0, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
64	E11	97	E6	G12	66	99	E9	E6	G11	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, SDMMC1_D123DIR, TSC_G4_IO2, DCMI_D1, LCD_R1, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
65	E10	98	D1	G10	67	100	E10	D1	F9	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2, SDMMC1_D0, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
66	D12	99	D2	G9	68	101	C12	D2	G13	PC9	I/O	FT_fl	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-
67	D11	100	D3	G8	69	102	D11	D3	E11	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, OTG_FS_SOF, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
68	D10	101	D4	F10	70	103	D10	D4	E12	PA9	I/O	FT_flu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
69	C12	102	D5	F9	71	104	C10	D5	D11	PA10	I/O	FT_flu	-	TIM1_CH3, SAI1_D1, DCMI_D1, USART1_RX, OTG_FS_ID, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
70	B12	103	C1	E13	72	105	B12	C1	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
71	A12	104	C2	D13	73	106	B11	C2	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
72	A11	105	B3	A11	74	107	B10	B3	A11	PA13 (JTMS/SWDIO)	I/O	FT	(4)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT	-
73	C11	106	B2	E12	75	108	C11	B2	D12	VDDUSB	S	-	-	-	-
74	F11	107	A1	C12	76	109	A12	A1	C12	VSS	S	-	-	-	-
75	G11	108	B1	C13	77	110	A11	B1	C13	VDD	S	-	-	-	-
-	-	-	-	E11	-	-	-	-	-	PH6	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8, EVENTOUT	-
-	-	-	-	D12	-	-	-	-	-	PH7	I/O	FT_f	-	I2C3_SCL, DCMI_D9, EVENTOUT	-
-	-	-	-	D11	-	-	-	-	C11	PH9	I/O	FT	-	I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0, EVENTOUT	-
-	-	-	-	B13	-	-	-	-	B13	PH12	I/O	FT	-	TIM5_CH3, OCTOSPIM_P2_IO7, DCMI_D3, EVENTOUT	-
-	-	-	-	A13	-	-	-	-	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-
-	-	-	-	B12	-	-	-	-	B12	PH15	I/O	FT	-	TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11, EVENTOUT	-
-	-	-	-	A12	-	-	-	-	A12	PI0	I/O	FT	-	TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13, EVENTOUT	-
-	-	-	-	C11	-	-	-	-	-	PI8	I/O	FT	-	OCTOSPIM_P2_NCS, DCMI_D12, EVENTOUT	-
-	-	-	-	B11	-	-	-	-	B11	PI1	I/O	FT	-	SPI2_SCK, DCMI_D8, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	-	-	-	B10	-	-	-	-	B10	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, DCMI_D9, EVENTOUT	-
-	-	-	-	C10	-	-	-	-	C10	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, DCMI_D10, EVENTOUT	-
-	-	-	-	D10	-	-	-	-	D10	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	E10	-	-	-	-	E10	PI5	I/O	FT	-	TIM8_CH1, OCTOSPIM_P2_NCS, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	C9	-	-	-	-	C9	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	B9	-	-	-	-	B9	PI6	I/O	FT	-	TIM8_CH2, OCTOSPIM_P2_CLK, DCMI_D6, EVENTOUT	-
76	A10	109	A2	A10	78	111	A10	A2	A10	PA14 (JTCK/SWCLK)	I/O	FT	(4)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, OTG_FS_SOF, SAI1_FS_B, EVENTOUT	-
77	A9	110	A3	A9	79	112	B9	A3	A9	PA15 (JTDI)	I/O	FT	(4)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, SAI2_FS_B, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
78	B11	111	C3	D9	80	113	C9	C3	D9	PC10	I/O	FT	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, DCMI_D8, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
79	C10	112	C4	E9	81	114	A9	C4	E9	PC11	I/O	FT	-	DCMI_D2, OCTOSPIM_P1_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
80	B10	113	B4	F8	82	115	D9	B4	F8	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
81	C9	114	A4	B8	83	116	C8	A4	B8	PD0	I/O	FT	-	SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, LCD_B4, FMC_D2, EVENTOUT	-
82	B9	115	C5	C8	84	117	B8	C5	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, LCD_B5, FMC_D3, EVENTOUT	-
83	C8	116	B5	D8	85	118	D8	B5	D8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, SDMMC1_CMD, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
84	B8	117	D6	E8	86	119	A8	D6	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS_NSS, OCTOSPIM_P2_NCS, LCD_CLK, FMC_CLK, EVENTOUT	-
85	B7	118	C6	C7	87	120	C7	C6	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-
86	A6	119	A5	D7	88	121	D7	A5	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	120	B6	M3	-	122	-	B6	M3	VSS	S	-	-	-	-
-	-	121	A6	A8	-	123	-	A6	A8	VDD	S	-	-	-	-
87	B6	122	E7	E7	89	124	B7	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
88	A5	123	D7	F7	90	125	E7	D7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-
-	D9	124	C7	B7	-	126	F6	C7	B7	PG9	I/O	FT_s	-	OCTOSPIM_P2_IO6, SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
-	D8	125	B7	D6	-	127	E6	B7	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	G3	126	-	E6	-	128	-	-	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS_NSS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	D7	127	A7	F6	-	129	D6	A7	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, OCTOSPIM_P2_NCS, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	C7	128	D8	G7	-	-	C6	D8	G6	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, LCD_R0, FMC_A24, EVENTOUT	-
-	C6	129	-	G6	-	-	-	-	-	PG14	I/O	FT_fs	-	I2C1_SCL, LCD_R1, FMC_A25, EVENTOUT	-
-	F7	130	-	-	-	130	A7	-	-	VSS	S	-	-	-	-
-	G7	131	A8	B6	-	131	A6	A8	B6	VDDIO2	S	-	-	-	-
-	K1	132	-	C6	-	132	-	-	C6	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, OCTOSPIM_P2_DQS, DCMI_D13, EVENTOUT	-
89	A8	133	B8	A6	91	133	B6	B8	A6	PB3 (JTDO/TRACESWO)	I/O	FT_la	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, OTG_FS_CRS_SYNC, SAI1_SCK_B, EVENTOUT	COMP2_INM

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
90	A7	134	C8	A5	92	134	A5	C8	A5	PB4 (NJTRST)	I/O	FT_fa	(4)	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS_NSS, UART5_RTS_DE, TSC_G2_IO1, DCMI_D12, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP
91	C5	135	E8	B5	93	135	B5	E8	B5	PB5	I/O	FT_la	-	LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
92	B5	136	C9	C5	94	136	D5	C9	C5	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, DFSDM1_DATIN5, USART1_TX, TSC_G2_IO3, DCMI_D5, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
93	B4	137	A9	D5	95	137	C5	A9	D5	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, I2C4_SDA, DFSDM1_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, DCMI_VSYNC, DSI_TE, FMC_NL, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
94	A4	138	B9	E5	96	138	A4	B9	E5	PH3-BOOT0	I/O	FT	-	EVENTOUT	-
95	A3	139	C10	C4	97	139	B4	C10	C4	PB8	I/O	FT_fl	-	TIM4_CH3, SAI1_CK1, I2C1_SCL, DFSDM1_CKOUT, DFSDM1_DATIN6, SDMMC1_CKIN, CAN1_RX, DCMI_D6, LCD_B1, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
96	B3	140	B10	D4	98	140	A3	B10	D4	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, SAI1_D2, I2C1_SDA, SPI2_NSS, DFSDM1_CKIN6, SDMMC1_CDIR, CAN1_TX, DCMI_D7, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
97	C3	141	A10	A4	-	141	A2	A10	A4	PE0	I/O	FT	-	TIM4_ETR, DCMI_D2, LCD_HSYNC, FMC_NBL0, TIM16_CH1, EVENTOUT	-

Table 15. STM32L4Sxxx pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4S5xx STM32L4S7xx					STM32L4S9xx										
LQFP100	UBGA132	LQFP144	WLCSP144	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144	UFBGA169						
98	A2	142	A11	B4	-	142	C4	A11	B4	PE1	I/O	FT	-	DCMI_D3, LCD_VSYNC, FMC_NBL1, TIM17_CH1, EVENTOUT	-
99	D3	143	A12	B3	99	143	A1	A12	B3	VSS	S	-	-	-	-
100	C4	144	B12	A3	100	144	B2	B12	A3	VDD	S	-	-	-	-
-	-	-	-	A2	-	-	-	-	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	B2	-	-	-	-	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	B1	-	-	-	-	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT	-
-	-	-	-	A1	-	-	-	-	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, PF8 and PF9 NC' IOs are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS_NSS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_RX
	PA4	-	-	-	OCTOSPIM_P1_NCS	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK	SPI1_MISO	-	USART3_CTS_NSS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	DCMI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	SAI1_D1	-	DCMI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS_NSS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_DE

Table 16. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	DFSDM1_DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM1_DATIN4	-
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_CKOUT	-
	PC3	-	LPTIM1_ETR	-	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	SAI1_D3	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	DCMI_D2	OCTOSPIM_P1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port D	PD0	-	-	-	-	-	SPI2_NSS	DFSDM1_DATIN7	-
	PD1	-	-	-	-	-	SPI2_SCK	DFSDM1_CKIN7	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	SPI2_SCK	DCMI_D5	SPI2_MISO	DFSDM1_DATIN0	USART2_CTS_NSS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_CKIN0	USART2_RTS_DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	SAI1_D1	DCMI_D10	SPI3_MOSI	DFSDM1_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS_NSS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_RTS_DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPIM_P1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	DFSDM1_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM1_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM1_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM1_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPIM_P1_CLK	-	-	DFSDM1_CKOUT	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_P1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_P2_DQS	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_P1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_P2_NCS	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	OCTOSPIM_P2_DQS	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	-	-	OCTOSPIM_P1_IO4	-	-	-	-
	PH3	-	-	-	-	-	-	-	-
	PH4	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_DQS	-	-
	PH5	-	-	-	-	I2C2_SDA	-	-	-
	PH6	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_CLK	-	-
	PH7	-	-	-	-	I2C3_SCL	-	-	-
	PH8	-	-	-	-	I2C3_SDA	OCTOSPIM_P2_IO3	-	-
	PH9	-	-	-	-	I2C3_SMBA	OCTOSPIM_P2_IO4	-	-
	PH10	-	-	TIM5_CH1	-	-	OCTOSPIM_P2_IO5	-	-
	PH11	-	-	TIM5_CH2	-	-	OCTOSPIM_P2_IO6	-	-
	PH12	-	-	TIM5_CH3	-	-	OCTOSPIM_P2_IO7	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-
	PH15	-	-	-	TIM8_CH3N	-	OCTOSPIM_P2_IO6	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/ SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	OCTOSPIM_P2_NCS	-	-
	PI9	-	-	-	-	-	OCTOSPIM_P2_IO2	-	-
	PI10	-	-	-	-	-	OCTOSPIM_P2_IO1	-	-
	PI11	-	-	-	-	-	OCTOSPIM_P2_IO0	-	-

1. Refer to *Table 17* for AF8 to AF15.

Table 17. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	OCTOSPIM_P1_DQS	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	OCTOSPIM_P1_NCS	-	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	OCTOSPIM_P1_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	OCTOSPIM_P1_IO3	-	TIM1_BKIN	TIM8_BKIN	TIM16_CH1	EVENTOUT
	PA7	-	-	OCTOSPIM_P1_IO2	-	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	-	-	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	-	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	-	TIM1_BKIN2	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_DE	TSC_G3_IO1	-	-	-	SAI2_FS_B	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port B	PB0	-	-	OCTOSPIM_P1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_ RTS_DE	-	OCTOSPIM_P1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPIM_P1_DQS	LCD_B1	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRS_SYNC	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_ DE	TSC_G2_IO1	DCMI_D12	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	DCMI_D5	-	TIM8_BKIN2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC	DSI_TE	FMC_NL	TIM8_BKIN	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_ CKIN	CAN1_RX	DCMI_D6	LCD_B1	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_ CDIR	CAN1_TX	DCMI_D7	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPIM_P1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPIM_P1_NCS	DSI_TE	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RT S_DE	TSC_G1_IO1	-	-	-	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CT S	TSC_G1_IO2	-	-	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	-	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	-	-	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	-	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_ D0DIR	TSC_G4_IO1	DCMI_D0	LCD_R0	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_ D123DIR	TSC_G4_IO2	DCMI_D1	LCD_R1	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port D	PD0	-	CAN1_RX	-	LCD_B4	FMC_D2	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	LCD_B5	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	DCMI_D11	-	SDMMC1_CMD	-	-	EVENTOUT
	PD3	-	-	OCTOSPIM_P2_NCS	LCD_CLK	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	OCTOSPIM_P1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	OCTOSPIM_P1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	OCTOSPIM_P1_IO6	LCD_DE	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	OCTOSPIM_P1_IO7	-	FMC_NCE/FMC_NE1	-	-	EVENTOUT
	PD8	-	-	DCMI_HSYNC	LCD_R3	FMC_D13	-	-	EVENTOUT
	PD9	-	-	DCMI_PIXCLK	LCD_R4	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	LCD_R5	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	LCD_R6	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	LCD_R7	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	LCD_B2	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	LCD_B3	FMC_D1	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port E	PE0	-	-	DCMI_D2	LCD_HSYNC	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	DCMI_D3	LCD_VSYNC	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	LCD_R0	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	LCD_R1	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	DCMI_D4	LCD_B0	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	DCMI_D6	LCD_G0	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	DCMI_D7	LCD_G1	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	LCD_B6	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	LCD_B7	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	LCD_G2	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	OCTOSPIM_P1_CLK	LCD_G3	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	OCTOSPIM_P1_NCS	LCD_G4	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	OCTOSPIM_1_IO0	LCD_G5	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	OCTOSPIM_P1_IO1	LCD_G6	FMC_D10	-	-	EVENTOUT
	PE14	-	-	OCTOSPIM_P1_IO2	LCD_G7	FMC_D11	-	-	EVENTOUT
	PE15	-	-	OCTOSPIM_P1_IO3	LCD_R2	FMC_D12	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPIM_P1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	OCTOSPIM_P1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	OCTOSPIM_P1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	OCTOSPIM_P1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11	-	-	SAI1_D3	TIM15_CH2	EVENTOUT
	PF11	-	LCD_DE	DCMI_D12	DSI_TE	-	-	-	EVENTOUT
	PF12	-	-	-	LCD_B0	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	LCD_B1	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	LCD_G0	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	LCD_G1	FMC_A9	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS_DE	LCD_R1	-	DSI_TE	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE/FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	LCD_R0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	LCD_R1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	DCMI_D13	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	-	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3	-	-	-	-	EVENTOUT
	PH13	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	DCMI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

1. Refer to *Table 16* for AF0 to AF7.

5 Memory mapping

For memory map and peripheral register boundary addresses refer to the corresponding section of reference manual RM0432.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 18*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 19*.

Figure 18. Pin loading conditions

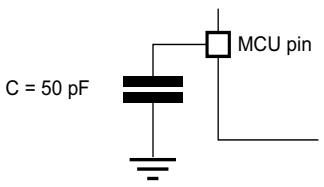
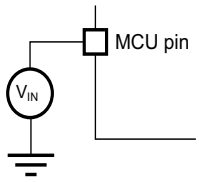
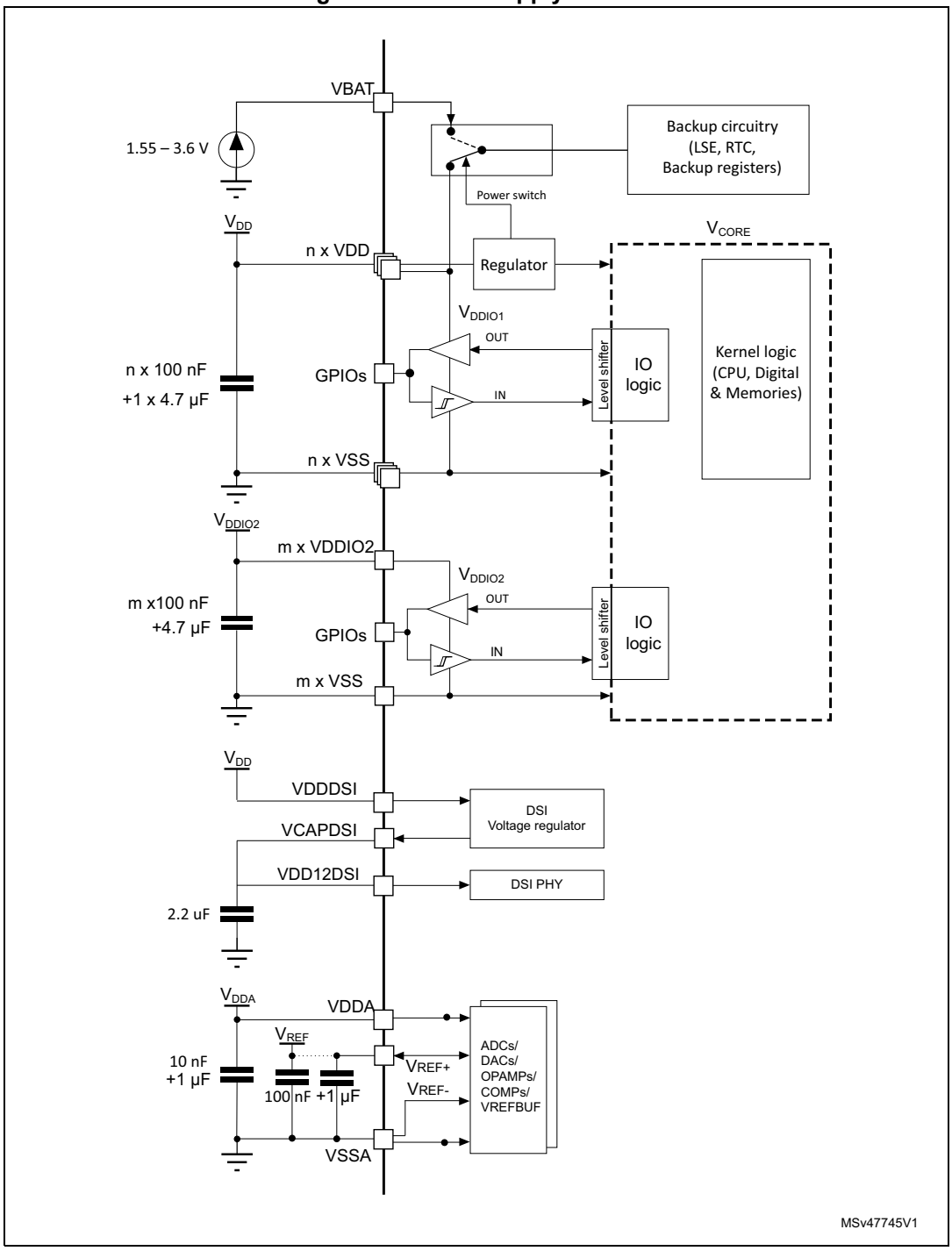


Figure 19. Pin input voltage



6.1.6 Power supply scheme

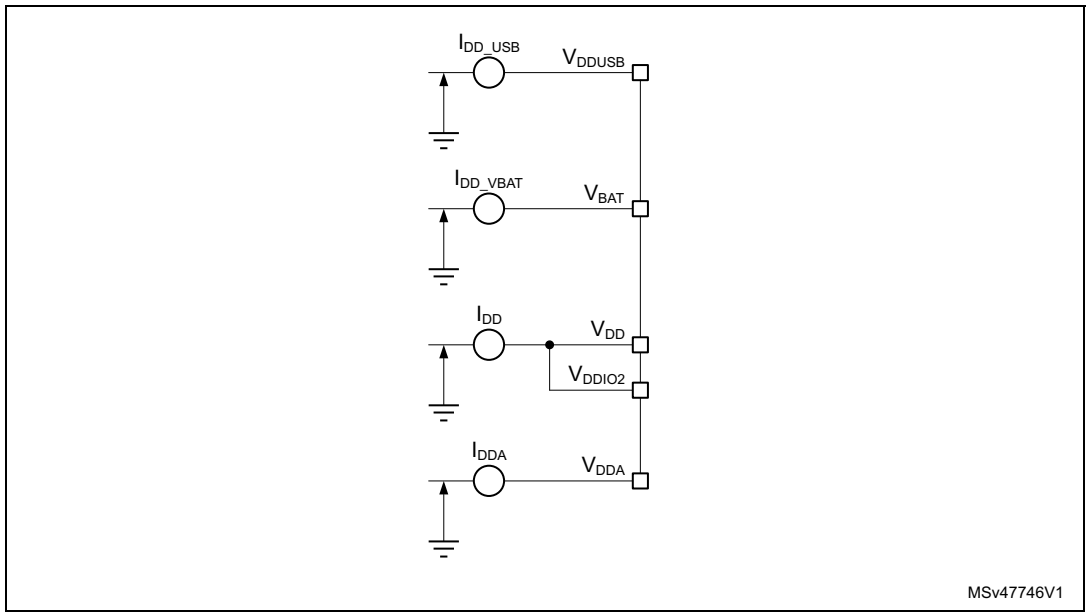
Figure 20. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 21. Current consumption measurement



The I_{DD_ALL} parameters given in *Table 25* to *Table 32* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB} and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) + 4.0(3)(4)	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	

Table 18. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
$\sum I_{VSS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(4)	
	Injected current on PA4, PA5	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 18: Voltage characteristics* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	120	
f_{PCLK2}	Internal APB2 clock frequency	-	0	120	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	V
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	V_{DDIOx}+0.3	
		BOOT0	0	9	
		All I/O except BOOT0 and TT_xx	-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V, 5.5 V)(2)(3)	

Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6(4)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		UFBGA169	-	-	385	
		UFBGA132	-	-	364	
		WLCSP144	-	-	664	
P_D	Power dissipation at T_A = 125 °C for suffix 3(4)	LQFP144	-	-	156	mW
		LQFP100	-	-	119	
		UFBGA169	-	-	96	
		UFBGA132	-	-	91	
		WLCSP144	-	-	831	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(5)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	µs/V
	V_{DDIO2} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}[2]	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	

Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.4 Embedded voltage reference

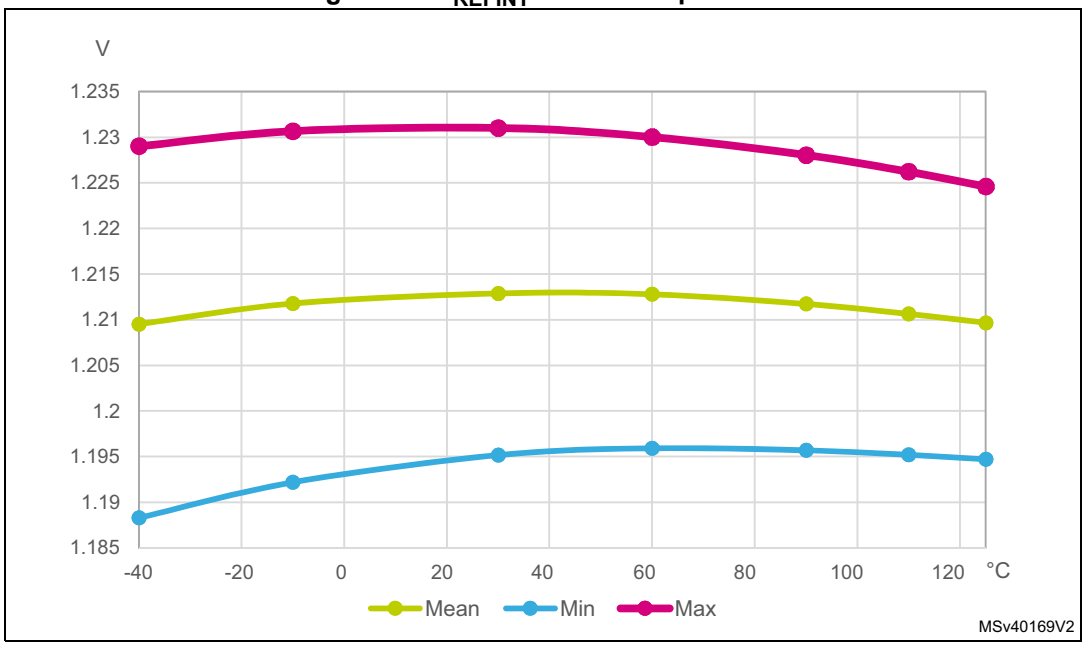
The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 22. V_{REFINT} versus temperature



6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in *Figure 21: Current consumption measurement*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0432 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 1 Boost mode for 80 MHz < f_{HCLK} <= 120 MHz
  - Voltage Range 1 Normal mode for 26 MHz < f_{HCLK} <= 80 MHz

The parameters given in *Table 25* to *Table 32* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.40	3.80	4.90	6.55	9.45	3.9	4.8	6.8	11.0	17.0	mA
				16 MHz	2.20	2.55	3.70	5.30	8.20	2.6	3.4	5.4	8.7	15.0	
				8 MHz	1.25	1.60	2.70	4.30	7.20	1.6	2.3	4.3	7.6	14.0	
				4 MHz	0.740	1.10	2.20	3.80	6.70	1.0	1.8	3.8	7.1	13.0	
				2 MHz	0.495	0.860	1.95	3.55	6.45	0.7	1.5	3.5	6.8	13.0	
				1 MHz	0.370	0.740	1.85	3.45	6.35	0.6	1.4	3.4	6.6	13.0	
				100 KHz	0.265	0.630	1.75	3.35	6.25	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.5	19.5	21.0	23.0	27.0	21.0	23.0	26.0	30.0	38.0	
			Range 1 Normal Mode	80 MHz	11.5	12.0	13.5	15.5	19.0	13.0	14.0	17.0	21.0	28.0	
				72 MHz	10.5	11.0	12.5	14.5	18.0	12.0	13.0	16.0	20.0	27.0	
				64 MHz	9.25	9.75	11.0	13.5	17.0	11.0	12.0	14.0	18.0	26.0	
				48 MHz	7.35	7.85	9.30	11.5	15.0	8.3	9.3	12.0	16.0	23.0	
				32 MHz	5.00	5.50	6.95	8.95	12.5	5.7	6.7	9.2	14.0	21.0	
				24 MHz	3.85	4.35	5.75	7.75	11.5	4.4	5.4	7.9	12.0	19.0	
				16 MHz	2.65	3.15	4.55	6.55	10.0	3.1	4.1	6.6	11.0	18.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	490	910	2200	4050	7250	690	1600	4000	7700	14000	µA
				1 MHz	305	770	2050	3900	7100	490	1500	3900	7500	14000	
				400 KHz	250	695	2000	3800	7000	430	1400	3800	7500	14000	
				100 KHz	210	645	1950	3750	7000	380	1400	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.60	3.95	5.05	6.65	9.55	4.2	5.0	7.1	11.0	17.0	mA
				16 MHz	2.30	2.65	3.75	5.35	8.20	2.7	3.6	5.6	8.9	15.0	
				8 MHz	1.30	1.65	2.70	4.30	7.15	1.6	2.4	4.4	7.7	14.0	
				4 MHz	0.770	1.10	2.20	3.75	6.60	1.0	1.8	3.8	7.1	14.0	
				2 MHz	0.515	0.865	1.95	3.50	6.35	0.7	1.5	3.5	6.8	13.0	
				1 MHz	0.380	0.735	1.80	3.35	6.20	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.620	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.0	18.0	19.5	21.5	25.5	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	12.5	13.0	14.0	16.0	19.5	14.0	15.0	18.0	22.0	29.0	
				72 MHz	11.0	11.5	13.0	15.0	18.5	13.0	14.0	17.0	21.0	28.0	
				64 MHz	9.90	10.5	12.0	14.0	17.5	12.0	13.0	15.0	19.0	26.0	
				48 MHz	7.85	8.30	9.75	11.5	15.0	8.7	9.9	13.0	17.0	24.0	
				32 MHz	5.35	5.80	7.20	9.20	12.5	6.1	7.1	9.6	14.0	21.0	
				24 MHz	4.10	4.55	5.95	7.90	11.5	4.7	5.7	8.2	13.0	20.0	
				16 MHz	2.80	3.30	4.65	6.60	10.0	3.3	4.3	6.8	11.0	18.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	460	905	2150	3950	7100	660	1700	4100	7700	15000	µA
				1 MHz	355	760	2000	3800	6950	540	1500	3900	7600	14000	
				400 KHz	240	685	1950	3700	6850	410	1400	3800	7500	14000	
				100 KHz	200	635	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.00	4.40	5.55	7.20	10.0	4.60	5.5	7.5	11.0	17.0	mA
				16 MHz	2.65	3.05	4.15	5.80	8.75	3.10	4.0	6.0	9.3	16.0	
				8 MHz	1.50	1.85	2.90	4.45	7.25	1.80	2.6	4.6	7.9	14.0	
				4 MHz	0.875	1.25	2.35	3.95	6.90	1.20	1.9	3.9	7.2	14.0	
				2 MHz	0.565	0.925	2.05	3.65	6.55	0.77	1.6	3.6	6.8	13.0	
				1 MHz	0.405	0.770	1.90	3.50	6.40	0.60	1.4	3.4	6.7	13.0	
				100 KHz	0.265	0.635	1.75	3.35	6.25	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.5	19.5	21.0	23.5	27.0	21.00	23.0	26.0	30.0	38.0	
			Range 1 Normal Mode	80 MHz	13.0	13.5	15.5	17.5	21.0	15.00	17.0	19.0	23.0	30.0	
				72 MHz	12.0	12.5	14.0	16.0	20.0	14.00	15.0	18.0	22.0	29.0	
				64 MHz	10.5	11.0	12.5	15.0	18.5	12.00	14.0	16.0	20.0	28.0	
				48 MHz	8.75	9.30	11.0	13.0	16.5	9.80	12.0	14.0	18.0	25.0	
				32 MHz	6.20	6.70	8.20	10.0	14.0	7.00	8.2	11.0	15.0	22.0	
				24 MHz	4.70	5.20	6.70	10.5	12.5	5.40	6.5	9.0	13.0	20.0	
				16 MHz	3.35	3.85	5.25	7.30	11.0	3.90	4.9	7.4	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	595	1000	2300	4150	7350	810.00	1700	4100	7800	15000	µA
				1 MHz	370	800	2100	3950	7150	560.00	1500	3900	7600	14000	
				400 KHz	245	705	2000	3850	7050	420.00	1400	3800	7500	14000	
				100 KHz	230	655	1950	3800	7000	400.00	1400	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	4.10	4.50	5.60	7.20	10.00	4.7	5.6	7.6	11.0	17.0	mA
				16 MHz	2.75	3.10	4.25	5.85	8.70	3.2	4.1	6.1	9.4	16.0	
				8 MHz	1.25	1.90	2.95	4.55	7.35	1.7	2.7	4.7	8.0	14.0	
				4 MHz	0.91	1.25	2.35	3.90	6.75	1.2	2.0	4.0	7.3	14.0	
				2 MHz	0.59	0.94	2.00	3.60	6.40	0.8	1.6	3.6	6.9	13.0	
				1 MHz	0.42	0.77	1.85	3.40	6.25	0.6	1.4	3.4	6.7	13.0	
				100 KHz	0.27	0.63	1.70	3.25	6.10	0.4	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	17.00	18.00	19.50	21.50	25.50	19.0	21.0	24.0	28.0	36.0	
			Range 1 Normal Mode	80 MHz	13.00	13.50	15.00	17.00	20.50	15.0	16.0	19.0	23.0	30.0	
				72 MHz	11.50	12.00	14.00	16.00	19.50	13.0	15.0	18.0	22.0	29.0	
				64 MHz	10.50	11.00	12.50	14.50	18.00	12.0	13.0	16.0	20.0	27.0	
				48 MHz	9.00	9.50	11.00	13.00	16.50	11.0	12.0	15.0	19.0	26.0	
				32 MHz	6.45	6.95	8.40	10.50	14.00	7.3	8.5	12.0	16.0	23.0	
				24 MHz	4.90	5.40	6.85	8.80	12.50	5.6	6.7	9.3	14.0	21.0	
				16 MHz	3.55	4.00	5.40	7.40	11.00	4.1	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	590	1000	2300	4050	7200	800.0	1800	4200	7800	15000	µA
				1 MHz	390	805	2100	3850	7000	580.0	1600	4000	7600	14000	
				400 KHz	245	655	1950	3750	6900	420.0	1400	3800	7500	14000	
				100 KHz	195	610	1900	3700	6850	370.0	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 29. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.75	4.85	6.45	9.30	4.70	5.6	7.6	11.0	17.0	mA
				16 MHz	2.20	2.55	3.65	5.20	8.10	3.20	4.1	6.1	9.4	16.0	
				8 MHz	1.20	1.55	2.65	4.25	7.10	1.70	2.7	4.7	8.0	14.0	
				4 MHz	0.74	1.10	2.15	3.75	6.60	1.20	2.0	4.0	7.3	14.0	
				2 MHz	0.49	0.85	1.95	3.50	6.35	0.79	1.6	3.6	6.9	13.0	
				1 MHz	0.37	0.73	1.80	3.40	6.20	0.61	1.4	3.4	6.7	13.0	
				100 KHz	0.26	0.62	1.70	3.25	6.10	0.44	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	18.00	18.50	20.00	22.50	26.50	19.00	21.0	24.0	28.0	36.0(2)	
			Range 1 Normal Mode	80 MHz	11.00	11.50	13.50	15.50	19.00	15.00	16.0	19.0	23.0	30.0(2)	
				72 MHz	10.00	10.50	12.00	14.00	18.00	13.00	15.0	18.0	22.0	29.0	
				64 MHz	9.10	9.60	11.00	13.00	16.50	12.00	13.0	16.0	20.0	27.0	
				48 MHz	7.20	7.70	9.20	11.00	14.50	11.00	12.0	15.0	19.0	26.0	
				32 MHz	4.90	5.40	6.85	8.80	12.50	7.30	8.5	12.0	16.0	23.0	
				24 MHz	3.75	4.25	5.65	7.65	11.00	5.60	6.7	9.3	14.0	21.0	
				16 MHz	2.60	3.10	4.50	6.45	9.90	4.10	5.2	7.7	12.0	19.0	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable FLASH in power-down		2 MHz	435	885	2150	3950	7100	800	1800	4200	7800	15000	µA
				1 MHz	300	745	2000	3800	6950	580	1600	4000	7600	14000	
				400 KHz	225	655	1900	3700	6850	420	1400	3800	7500	14000	
				100 KHz	180	620	1900	3650	6800	370	1400	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	3.40	3.60	mA	131	138	µA/MHz
				Coremark	3.90	3.95		150	152	
				Dhrystone2.1	4.25	4.30		163	165	
				Fibonacci	3.65	3.90		140	150	
				While(1)	3.15	3.15		121	121	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.5	12.5	mA	144	156	µA/MHz
				Coremark	13.5	13.5		169	169	
				Dhrystone2.1	14.5	14.5		181	181	
				Fibonacci	12.5	14.0		156	175	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	21.5	21.5		179	179	
				Dhrystone2.1	22.5	22.5		188	188	
				Fibonacci	20.0	21.0		167	175	
				While(1)	16.5	16.5		138	138	

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2MHz all pripherals disable		Reduced code(1)	490	460	µA	245	230	µA/MHz
				Coremark	520	515		260	258	
				Dhrystone2.1	530	530		265	265	
				Fibonacci	470	495		235	248	
				While(1)	455	515		228	258	

1. Reduced code used for characterization results provided in *Table 25*, *Table 27*, *Table 29*.

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	4.00	4.10	mA	154	158	µA/MHz
				Coremark	4.15	3.80		160	146	
				Dhrystone2.1	4.40	4.00		169	154	
				Fibonacci	3.80	3.60		146	138	
				While(1)	3.15	3.15		121.2	121.2	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	13.0	13.0	mA	163	163	µA/MHz
				Coremark	13.0	12.0		163	150	
				Dhrystone2.1	14.0	12.5		175	156	
				Fibonacci	11.5	11.0		144	138	
				While(1)	10.5	10.5		131	131	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.5	17.0	mA	154	142	µA/MHz
				Coremark	18.0	16.0		150	133	
				Dhrystone2.1	19.0	16.5		158	138	
				Fibonacci	16.0	15.0		133	125	
				While(1)	16.5	16.5		138	138	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	595	590	µA	298	295	µA/MHz
				Coremark	620	580		310	290	
				Dhrystone2.1	645	655		323	328	
				Fibonacci	670	580		335	290	
				While(1)	470	685		235	343	

1. Reduced code used for characterization results provided in *Table 25*, *Table 27*, *Table 29*.

Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	3.35	mA	129	µA/MHz
				Coremark	3.10		119	
				Dhrystone2.1	3.65		140	
				Fibonacci	3.20		123	
				While(1)	2.85		110	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	11.0	mA	138	µA/MHz
				Coremark	10.5		131	
				Dhrystone2.1	12.5		156	
				Fibonacci	10.5		131	
				While(1)	9.40		118	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	18.0	mA	150	µA/MHz
				Coremark	16.5		138	
				Dhrystone2.1	19.5		163	
				Fibonacci	17.5		146	
				While(1)	15.0		125	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	435	µA	218	µA/MHz
				Coremark	395		198	
				Dhrystone2.1	470		235	
				Fibonacci	425		213	
				While(1)	455		228	

1. Reduced code used for characterization results provided in *Table 25*, *Table 27*, *Table 29*.

Table 33. Current consumption in Sleep and Low-power sleep mode, Flash ON

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Sleep)	Supply current in Sleep mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	1.10	1.45	2.55	4.15	7.00	1.40	2.2	4.2	7.5	14.0	mA
				16 MHz	0.78	1.15	2.25	3.80	6.65	1.00	1.8	3.8	7.1	14.0	
				8 MHz	0.52	0.87	1.95	3.55	6.35	0.72	1.5	3.5	6.8	13.0	
				4 MHz	0.38	0.74	1.85	3.40	6.25	0.57	1.4	3.4	6.7	13.0	
				2 MHz	0.32	0.63	1.75	3.35	6.15	0.50	1.3	3.3	6.6	13.0	
				1 MHz	0.29	0.61	1.75	3.30	6.10	0.46	1.3	3.3	6.5	13.0	
				100 KHz	0.26	0.58	1.70	3.25	6.10	0.43	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	4.20	4.70	6.25	8.40	12.00	4.80	6.0	8.7	13.0	21.0	
			Range 1 Normal Mode	80 MHz	2.80	3.25	4.65	6.60	10.00	3.30	4.3	6.8	11.0	18.0	
				72 MHz	2.55	3.00	4.40	6.40	9.85	3.00	4.0	6.5	11.0	18.0	
				64 MHz	2.30	2.75	4.20	6.15	9.60	2.70	3.8	6.3	11.0	18.0	
				48 MHz	2.15	2.60	4.00	6.00	9.45	2.60	3.5	6.0	10.0	18.0	
				32 MHz	1.55	2.00	3.40	5.35	8.80	1.90	2.9	5.4	9.3	17.0	
				24 MHz	1.25	1.70	3.10	5.05	8.50	1.60	2.5	5.0	9.0	16.0	
				16 MHz	0.93	1.40	2.80	4.70	8.20	1.20	2.2	4.7	8.6	16.0	
IDD (LPSleep)	Supply current in Low-power sleep mode	fHCLK = fMSI all peripherals disable		2 MHz	235	625	1950	3750	6900	410	1400	3800	7500	14000	µA
				1 MHz	220	605	1900	3700	6850	390	1400	3700	7500	14000	
				400 KHz	215	595	1900	3700	6850	390	1300	3700	7500	14000	
				100 KHz	210	595	1900	3700	6800	380	1300	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Low-power sleep mode, Flash in power-down

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	255	645	1950	3700	6850	430	1400	3700	7400	14000	µA
				1 MHz	195	620	1900	3700	6850	370	1300	3700	7400	14000	
				400 KHz	180	600	1900	3700	6800	350	1300	3700	7400	14000	
				100 KHz	175	595	1900	3650	6800	340	1300	3700	7400	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 35. Current consumption in Stop 2 mode, SRAM3 disabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	2.50	9.10	36.5	84.0	185	7.70	30.0	120	270	580	µA
			2.4 V	2.50	9.20	37.0	85.0	185	8.00	31.0	120	270	590	
			3 V	2.55	9.30	37.5	87.0	190	8.00	31.0	120	280	600	
			3.6 V	2.60	9.50	38.0	89.0	195	8.30	32.0	130	280	610	
I_{DD}(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	2.75	9.45	36.5	84.5	185	8.30	31.0	120	270	580	
			2.4 V	2.90	9.60	37.0	85.5	185	8.50	32.0	120	270	590	
			3 V	3.05	9.85	38.0	87.0	190	8.60	32.0	120	280	600	
			3.6 V	3.20	10.0	38.5	89.5	195	9.00	33.0	130	280	610	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	2.95	9.65	37.0	84.5	185	7.80	25.0	93.0	220	470	
			2.4 V	3.05	9.85	37.5	86.0	185	7.90	25.0	94.0	220	470	
			3 V	3.25	10.0	38.0	87.5	190	8.10	25.0	95.0	220	480	
			3.6 V	3.55	10.5	39.0	90.0	195	8.50	27.0	98.0	230	490	
		RTC clocked by LSE quartz in low drive mode	1.8 V	2.80	9.30	36.0	84.5	-	7.60	24.0	90.0	220	-	
			2.4 V	2.90	9.45	36.5	85.5	-	7.70	24.0	92.0	220	-	
			3 V	3.05	9.65	37.0	87.0	-	7.90	25.0	93.0	220	-	
			3.6 V	3.15	9.95	38.0	89.0	-	8.00	25.0	95.0	230	-	
I_{DD}(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(2)	3 V	3.55	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(2)	3 V	1.25	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(2)	3 V	2.90	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 43: Low-power mode wakeup timings*.

Table 36. Current consumption in Stop 2 mode, SRAM3 enabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	3.90	15.0	59.5	140	310	13.0	52.0	210	480	1100	µA
			2.4 V	3.95	15.0	60.0	140	310	14.0	53.0	210	480	1100	
			3 V	3.95	15.0	60.5	145	315	14.0	53.0	210	480	1100	
			3.6 V	3.95	15.0	61.5	145	320	14.0	54.0	210	490	1100	
IDD(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	4.10	15.0	60.5	140	310	11.0	53.0	210	480	1100	
			2.4 V	4.25	15.5	60.5	145	315	12.0	54.0	210	480	1100	
			3 V	4.50	15.5	61.5	145	320	12.0	54.0	210	480	1100	
			3.6 V	4.70	16.0	62.5	145	325	12.0	56.0	220	490	1100(2)	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	4.35	15.5	61.0	140	310	9.50	39.0	160	350	780	
			2.4 V	4.50	15.5	61.0	145	315	9.60	39.0	160	370	790	
			3 V	4.70	16.0	62.0	145	320	9.90	40.0	160	370	800	
			3.6 V	4.80	16.5	63.0	145	325	10.0	42.0	160	370	820	
		RTC clocked by LSE quartz in low drive mode	1.8 V	4.30	15.5	63.5	150	-	9.40	39.0	160	380	-	
			2.4 V	4.40	16.0	64.0	150	-	9.50	40.0	160	380	-	
			3 V	4.45	16.0	64.5	150	-	9.60	40.0	170	380	-	
			3.6 V	4.85	16.5	65.5	155	-	11.0	42.0	170	390	-	
IDD(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(3)	3 V	3.80	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(3)	3 V	1.30	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(3)	3 V	2.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 43: Low-power mode wakeup timings*.

Table 37. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	120	430	1400	2750	5050	280	1100	3300	6500	13000	µA
			2.4 V	120	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3.6 V	120	430	1400	2750	5150	280	1100	3300	6600	13000(2)	
IDD (Stop 1 with RTC)	Supply current in STOP 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	120	430	1400	2700	5050	280	1100	3300	6500	13000	
			2.4 V	125	430	1400	2750	5100	280	1100	3300	6500	13000	
			3 V	125	430	1400	2750	5100	280	1100	3300	6600	13000	
			3.6 V	125	435	1400	2750	5150	280	1100	3300	6600	13000	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	120	430	1400	2750	5050	300	1100	3500	6900	13000	
			2.4 V	120	435	1400	2750	5100	300	1100	3500	6900	13000	
			3 V	125	435	1400	2750	5100	320	1100	3500	6900	13000	
			3.6 V	125	435	1400	2750	5150	320	1100	3500	6900	13000	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			2.4 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3 V	120	420	1350	2700	-	300	1100	3400	6800	-	
			3.6 V	120	425	1350	2700	-	300	1100	3400	6800	-	
IDD (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(4)	3 V	2.10	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(4)	3 V	0.70	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(4)	3 V	1.50	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 43: Low-power mode wakeup timings*

Table 38. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	290	735	2050	3800	6950	560	1600	4500	8700	16000	µA
			2.4 V	295	735	2050	3850	6950	560	1600	4500	8700	17000	
			3 V	295	735	2050	3850	7000	570	1600	4500	8800	17000	
			3.6 V	295	740	2050	3850	7000	570	1600	4500	8800	17000 (2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 39. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	125	380	1900	5200	13500	340	1100	5300	15000	41000	nA
			2.4 V	135	440	2200	6050	15500	350	1300	6100	18000	47000	
			3 V	150	535	2700	7500	19500	370	1500	7100	21000	54000	
			3.6 V	190	665	3200	8850	23000	400	1900	8400	24000	62000	
		With independent watchdog	1.8 V	295	-	-	-	-	-	-	-	-	-	
			2.4 V	355	-	-	-	-	-	-	-	-	-	
			3 V	420	-	-	-	-	-	-	-	-	-	
			3.6 V	510	-	-	-	-	-	-	-	-	-	

Table 39. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	370	640	2100	5300	13500	1100	1400	6400	16000	41000	nA
			2.4 V	455	760	2500	6250	15500	1200	1700	6800	18000	47000	
			3 V	560	930	3050	7650	19000	1300	1900	8100	21000	55000	
			3.6 V	690	1150	3700	9200	23000	1400	2400	9000	24000	62000 (2)	
		RTC clocked by LSI, with independent watchdog	1.8 V	420	-	-	-	-	-	-	-	-	-	
			2.4 V	525	-	-	-	-	-	-	-	-	-	
			3 V	645	-	-	-	-	-	-	-	-	-	
			3.6 V	795	-	-	-	-	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	480	750	2200	5400	13500	-	-	-	-	-	nA
			2.4 V	615	930	2650	6400	15500	-	-	-	-	-	
			3 V	770	1150	3250	7900	19500	-	-	-	-	-	
			3.6 V	975	1450	3950	9500	23000	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	420	685	2150	5400	13500	-	-	-	-	-	
			2.4 V	520	830	2550	6400	15500	-	-	-	-	-	
			3 V	650	1000	3100	7800	19500	-	-	-	-	-	
			3.6 V	825	1300	3800	9400	23000	-	-	-	-	-	
I_{DD} (SRAM2)(4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	380	1420	5600	13300	28500	-	-	-	-	-	nA
			2.4 V	380	1410	5650	12950	29000	-	-	-	-	-	
			3 V	385	1415	5600	13000	28500	-	-	-	-	-	
			3.6 V	400	1435	5700	13150	29000	-	-	-	-	-	

Table 39. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz(5)	3 V	2.0	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: I_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 43: Low-power mode wakeup timings*.

Table 40. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	33.0	205	1250	3650	10500	150	620	3800	12000	35000	nA
			2.4 V	43.0	250	1450	4300	12000	170	740	4400	14000	39000	
			3 V	60.0	320	1850	5450	15500	190	920	5200	16000	45000	
			3.6 V	92.0	430	2300	6700	18500	270	1200	6200	19000	51000	

Table 40. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	245	420	1450	3850	10500	-	-	-	-	-	nA
			2.4 V	340	555	1750	4600	12500	-	-	-	-	-	
			3 V	465	730	2250	5900	15500	-	-	-	-	-	
			3.6 V	615	945	2850	7250	19000	-	-	-	-	-	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	335	520	1550	4000	-	-	-	-	-	-	
			2.4 V	435	650	1850	4750	-	-	-	-	-	-	
			3 V	560	830	2350	6050	-	-	-	-	-	-	
			3.6 V	730	1050	2950	7400	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz(3)	3 V	0.5	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 43: Low-power mode wakeup timings*.

Table 41. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(VBAT)	Backup domain supply current	RTC disabled	1.8 V	3.00	27.0	165	495	1350	8.0	67.0	390	1200	3000	nA
			2.4 V	4.00	31.0	190	560	1550	10.0	76.0	440	1300	3300	
			3 V	6.00	43.0	255	750	2000	13.0	91.0	510	1500	3800	
			3.6 V	14.0	83.0	485	1450	4050	34.0	200	1100	3100	8300	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	215	240	390	730	-	-	-	-	-	-	
			2.4 V	305	340	510	900	-	-	-	-	-	-	
			3 V	415	455	680	1200	-	-	-	-	-	-	
			3.6 V	540	595	925	1900	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	305	345	510	865	1600	-	-	-	-	-	
			2.4 V	395	440	625	1050	1800	-	-	-	-	-	
			3 V	510	565	805	1350	2300	-	-	-	-	-	
			3.6 V	650	740	1200	2200	4450	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 66: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 43: Low-power mode wakeup timings*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 43*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 43*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 42. Peripheral current consumption

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix	10.5	9.65	7.7	9	µA/MHz
	ADC independent clock domain	0.25	0.25	0.125	0.5	
	ADC AHB clock domain	3	2.75	2.6	3.5	
	AES	3	2.75	2.15	3	
	CRC	0.835	0.875	0.835	0.5	
	DCMI	7.15	6.65	5.5	7	
	DMA1	3.15	2.9	2.5	2.5	
	DMA2	2.85	2.65	2.5	2.5	
	DMA2D	29.5	27.5	22.5	26	
	DMAMUX	5.35	5.15	4.15	4.5	
	FLASH	7.75	7.25	6.25	6.5	
	FMC	10.5	9.65	8.35	9.5	
	GFXMMU	5.6	5.25	4.6	4.5	
	GPIOA	1.85	1.75	1.4	1	
	GPIOB	1.75	1.65	1.35	1.5	
	GPIOC	2.4	2.25	1.9	2.5	
	GPIOD	1.85	1.75	1.45	2	
	GPIOE	1.85	1.75	1.45	1.5	
	GPIOF	2	1.75	1.55	2	
	GPIOG	2.25	2.15	1.8	2.5	
	GPIOH	2.35	2.15	1.8	2.5	

Table 42. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
AHB (Cont.)	GPIOI	1.6	1.4	1.25	2	µA/MHz
	HASH1	2.6	2.4	2	3	
	OTG_FS independent clock domain	25.5	28	NA	NA	
	OTG_FS AHB clock domain	18	16.5	NA	NA	
	OSPIM independent clock domain	0.15	0.115	0.084	0.5	
	OSPIM AHB clock domain	0.665	0.625	0.54	1	
	OSPI1 independent clock domain	2.5	2.4	2.1	2.5	
	OSPI1 AHB clock domain	6.15	5.75	4.6	5.5	
	OSPI2 independent clock domain	1.9	1.65	1.25	1	
	OSPI2 AHB clock domain	5.5	5.25	4.15	5.5	
	RNG independent clock domain	3.9	4.25	NA	NA	
	RNG AHB clock domain	2.65	2.5	NA	NA	
	SDMMC1 independent clock domain	24.5	23.5	NA	NA	
	SDMMC1 AHB clock domain	23.5	22	NA	NA	
	SRAM1	2.65	2.65	2.1	2	
	SRAM2	2.25	2	1.75	2	
	SRAM3	5.35	5	4.25	5.5	
	TSC	1.85	1.75	1.65	1	
	All AHB Peripherals	165	150	125	145	
APB1	AHB to APB1 bridge	0.084	0.25	0.165	0.5	µA/MHz
	CAN1	4.85	4.5	3.75	4.5	
	CRS	0.335	0.25	0.415	0.5	
	DAC1	2.75	2.5	2.1	2.5	
	I2C1 independent clock domain	3.75	3.4	2.9	2.5	

Table 42. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	I2C1 APB clock domain	1.4	1.4	1.25	2	µA/MHz
	I2C2 independent clock domain	3.5	3.4	2.5	3.5	
	I2C2 APB clock domain	1.4	1.25	1.25	1	
	I2C3 independent clock domain	3.25	3.15	2.9	3	
	I2C3 APB clock domain	1.15	1	0.835	1	
	I2C4 independent clock domain	3.5	3.25	2.75	3	
	I2C4 APB clock domain	1.35	1.25	1	1.5	
	LPUART1 independent clock domain	3.15	3	2.45	3	
	LPUART1 APB clock domain	1.65	1.5	1.3	1.5	
	LPTIM1 independent clock domain	3.6	3.5	2.9	3	
	LPTIM1 APB clock domain	1	0.875	0.835	1	
	LPTIM2 independent clock domain	3.4	3.25	2.55	3.5	
	LPTIM2 APB clock domain	1.1	1	0.79	1	
	OPAMP	0.415	0.375	0.415	0.5	
	PWR	0.5	0.375	0.415	0.5	
	RTCAPB	1.25	1.15	1.25	1	
	SPI2	2.6	2.4	2.1	2.5	
	SPI3	3	2.75	2.5	3	
	TIM2	6.15	5.75	4.65	4.5	
	TIM3	5.25	4.9	4.15	5	
	TIM4	5.15	4.75	4.15	5	
	TIM5	6.5	6	5	6	
	TIM6	1.35	1.15	1.25	1	
	TIM7	1.25	1.15	0.835	1	

Table 42. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	USART2 independent clock domain	5.35	5	4.15	4.5	µA/MHz
	USART2 APB clock domain	3	2.75	2.5	2.5	
	USART3 independent clock domain	6.35	6	5	5.5	
	USART3 APB clock domain	2.6	2.4	2.1	2.5	
	UART4 independent clock domain	5.15	4.9	3.75	4.5	
	UART4 APB clock domain	2.5	2.25	2.1	2.5	
	UART5 independent clock domain	5.4	5	4.15	5	
	UART5 APB clock domain	2.4	2.25	2.1	2	
	WWDG	0.75	0.625	0.835	0.5	
	All APB1 on	110	100	84	97	
APB2	AHB to APB2 bridge	0.185	0.15	0.125	0.5	µA/MHz
	DFSDM	9.5	9	7.5	8.5	
	DSI independent clock domain	33	34.5	29.5	NA	
	DSI APB clock domain	13	7.15	29	NA	
	FW	0.665	0.625	0.5	0.5	
	LTDC independent clock domain	35.5	34.5	40	NA	
	LTDC APB clock domain	18	17	14	NA	
	SAI1 independent clock domain	3.1	2.9	2.5	3	
	SAI1 APB clock domain	2.6	2.4	1.9	2	
	SAI2 independent clock domain	3.15	3	2.55	3	
	SAI2 APB clock domain	2.6	2.4	1.9	2.5	
	SPI1	2.25	2.15	1.75	1	
	SYSCFG/VREFBUF/COMP	0.565	0.6	0.5	0.5	

Table 42. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB2 (Cont.)	TIM1	8.25	7.75	6.25	6.5	µA/MHz
	TIM8	8.4	8	6.65	6.5	
	TIM15	4	3.9	3.35	2.5	
	TIM16	2.9	2.9	2.35	1.5	
	TIM17	3.15	3	2.5	2	
	USART1 independent clock domain	6.5	6.15	5.25	6	
	USART1 APB clock domain	2.9	2.75	2.25	2	
	All APB2 on	80	75	62.5	72	
ALL		340	320	265	310	

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 43* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 43. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	9.1	9.8	µs
			Wakeup clock HSI16 = 16 MHz	8.5	9.0	
		Range 2	Wakeup clock MSI = 24 MHz	18.8	19.7	
			Wakeup clock HSI16 = 16 MHz	17.6	18.3	
			Wakeup clock MSI = 4 MHz	23.9	25.7	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	1.9	2.5	
			Wakeup clock HSI16 = 16 MHz	2.6	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	2.6	3.1	
			Wakeup clock HSI16 = 16 MHz	2.6	3.0	
			Wakeup clock MSI = 4 MHz	10.0	11.5	

Table 43. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	12.6	14.5	µs
			Wakeup clock HSI16 = 16 MHz	12.2	14.0	
		Range 2	Wakeup clock MSI = 24 MHz	22.1	24.1	
			Wakeup clock HSI16 = 16 MHz	21.3	23.3	
			Wakeup clock MSI = 4 MHz	25.1	27.1	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.3	7.0	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
		Range 2	Wakeup clock MSI = 24 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.2	8.0	
			Wakeup clock MSI = 4 MHz	10.9	12.6	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	20.4	22.4	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			16.8	19.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	13.1	14.8	µs
			Wakeup clock HSI16 = 16 MHz	12.6	14.4	
		Range 2	Wakeup clock MSI = 24 MHz	22.6	24.6	
			Wakeup clock HSI16 = 16 MHz	21.7	23.7	
			Wakeup clock MSI = 4 MHz	25.8	27.9	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.8	7.5	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
		Range 2	Wakeup clock MSI = 24 MHz	6.4	8.0	
			Wakeup clock HSI16 = 16 MHz	6.9	8.5	
			Wakeup clock MSI = 4 MHz	11.9	13.6	

Table 43. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	30.7	47.8	µs
			Wakeup clock MSI = 4 MHz	40.4	55.6	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	32.1	49.1	
			Wakeup clock MSI = 4 MHz	41.5	55.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	265.0	339.4	

1. Guaranteed by characterization results.

Table 44. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 45. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by characterization results.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

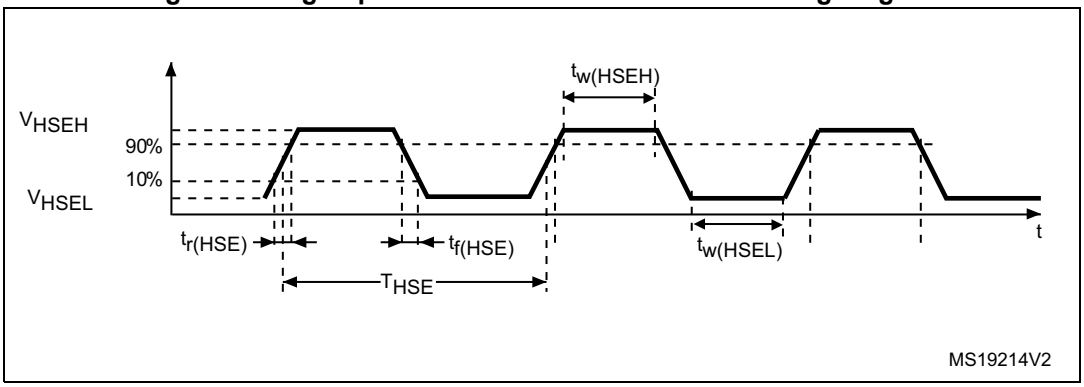
The external clock signal has to respect the I/O characteristics in *Section 6.3.17*. However, the recommended clock input waveform is shown in *Figure 23: High-speed external clock source AC timing diagram*.

Table 46. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 23. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

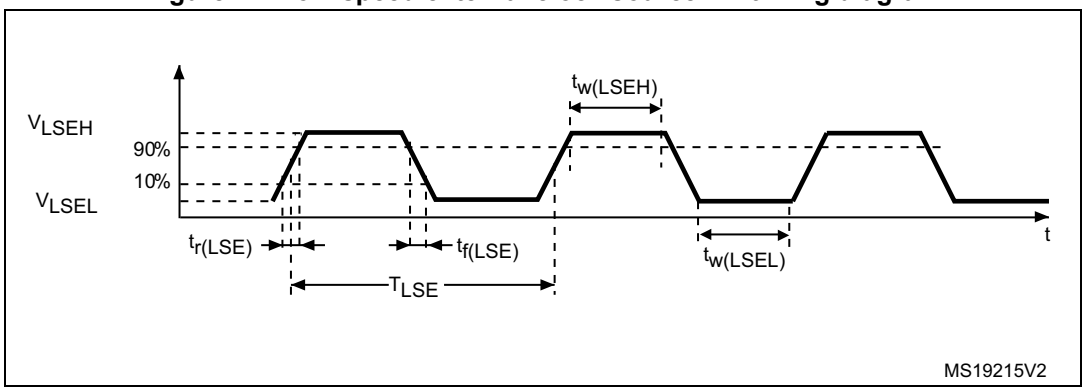
The external clock signal has to respect the I/O characteristics in *Section 6.3.17*. However, the recommended clock input waveform is shown in *Figure 24*.

Table 47. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 24. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 48*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 48. HSE oscillator characteristics(1)

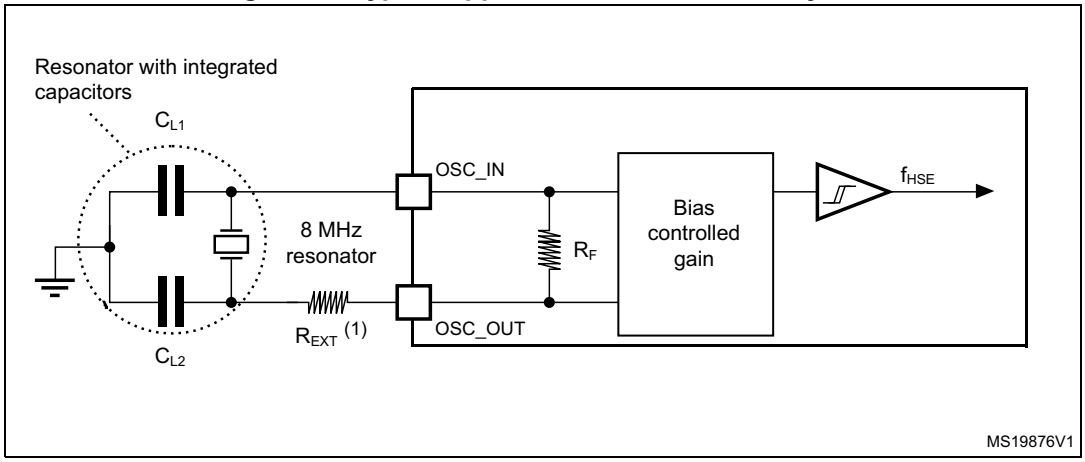
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 25*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 25. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 49*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

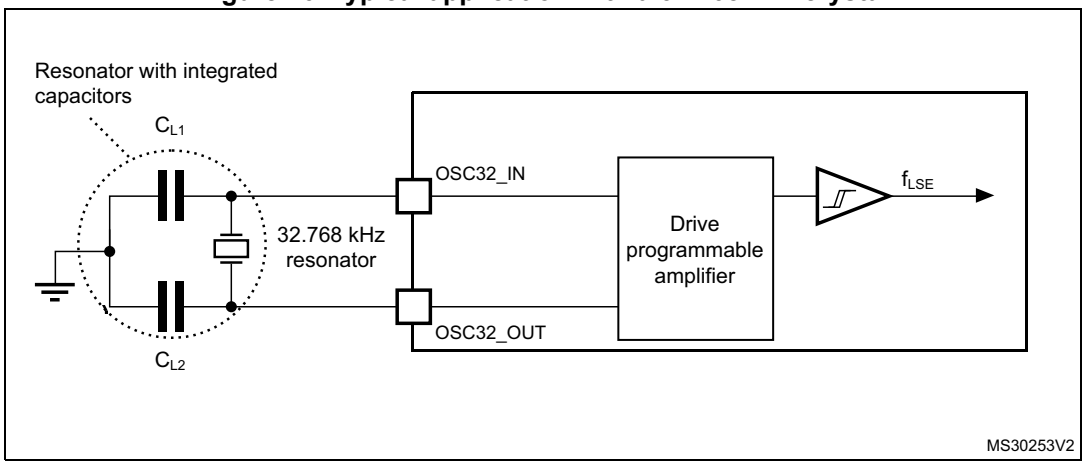
Table 49. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 26. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 50* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

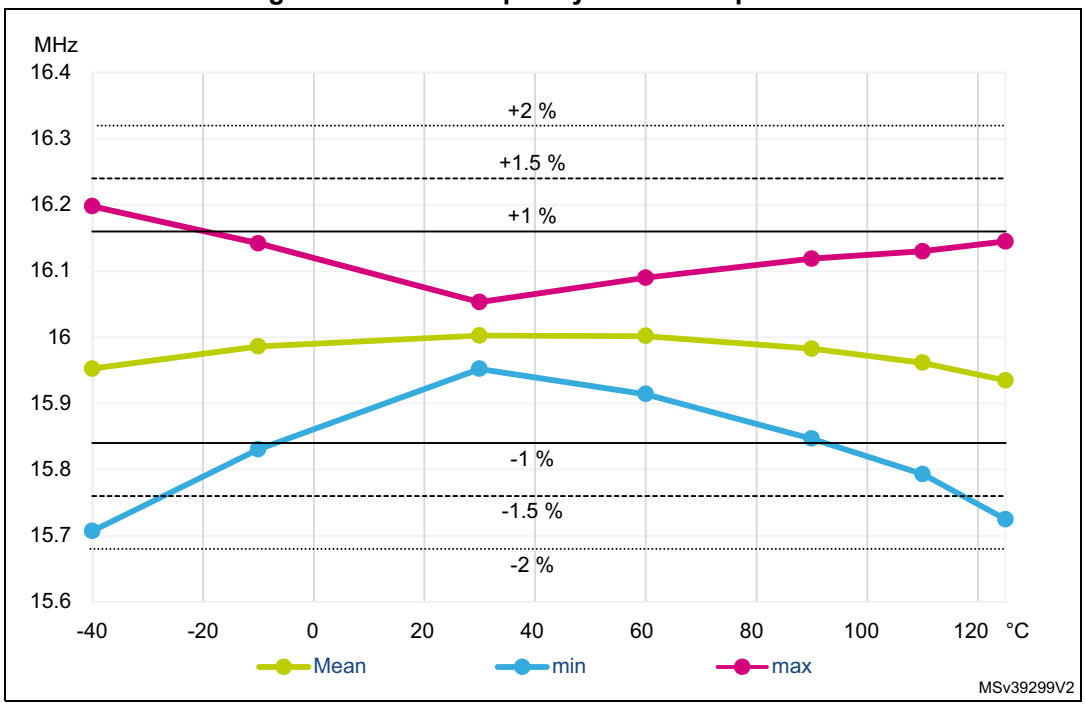
High-speed internal (HSI16) RC oscillator

Table 50. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 27. HSI16 frequency versus temperature



Multi-speed internal (MSI) RC oscillator

Table 51. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	7896	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 51. MSI oscillator characteristics(1) (continued)

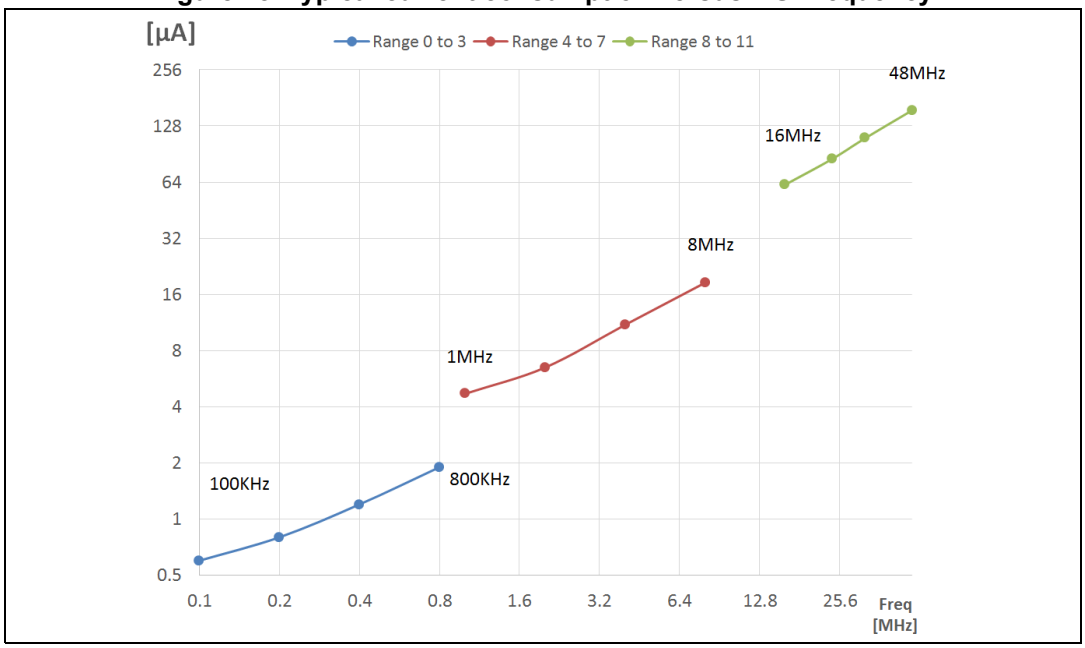
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 51. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.
5. Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.
   For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.
   For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Figure 28. Typical current consumption versus MSI frequency



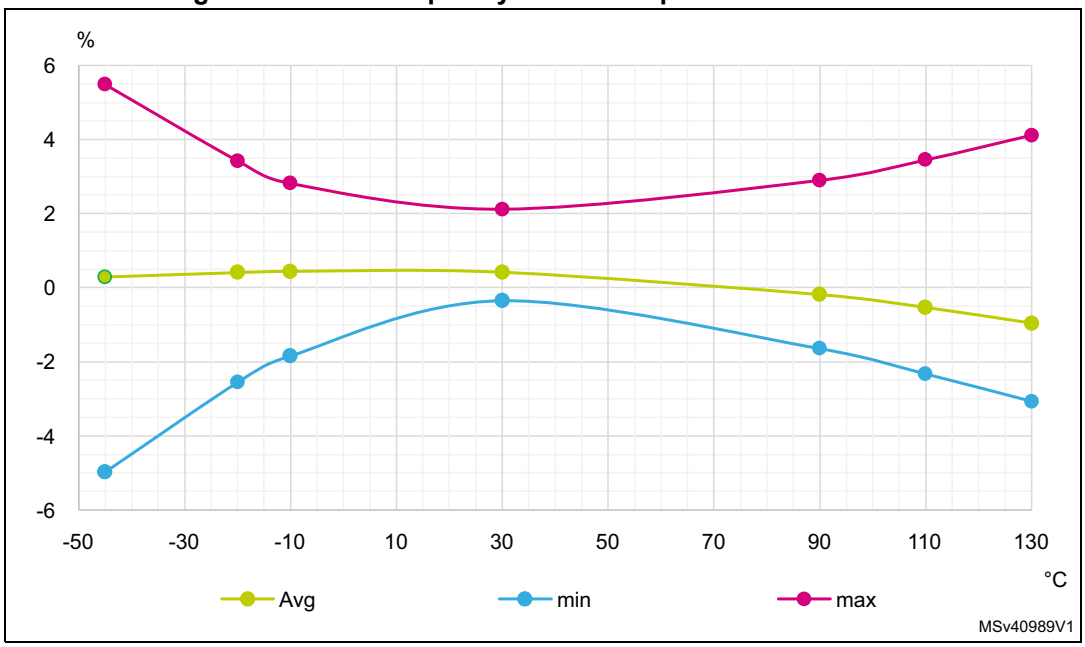
High-speed internal 48 MHz (HSI48) RC oscillator

Table 52. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 29. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 53. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)^{(2)}$	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)^{(2)}$	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)^{(2)}$	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 54* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 54. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1 Normal mode	2.0645	-	80	MHz
		Voltage scaling Range 1 Boost mode	2.0645	-	120	
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1 Normal mode	8	-	80	
		Voltage scaling Range 1 Boost mode	8	-	120	
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1 Normal mode	8	-	80	
		Voltage scaling Range 1 Boost mode	8	-	120	
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

6.3.10 MIPI D-PHY characteristics

The parameters given in *Table 55* and *Table 56* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21*.

Table 55. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-speed input/output characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns
V_{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	-	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V_{OHHS}	HS output high voltage	-	-	-	360	
Z_{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	-	10	%
t_{HSr} & t_{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP receiver input characteristics						
V_{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	-	300	
V_{IH}	Input high level voltage	-	880	-	-	
V_{hys}	Voltage hysteresis	-	25	-	-	
LP emitter output characteristics						
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP contention detector characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

1. Guaranteed by characterization results.

Table 56. MIPI D-PHY AC characteristics LP mode and HS/LP transitions(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LPX}	Transmitted length of any Low-Power state period	-	50	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	38	-	95	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the clock.	-	300	-	-	
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	-	8	-	-	UI
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	-	62+52*UI	-	-	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of an HS transmission burst.	-	60	-	-	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	-	40+4*UI	-	85+6*UI	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE+}$ Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	-	145+10*UI	-	-	
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	-	Max (n*8*UI, 60+n*4*UI)	-	-	
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	-	100	-	-	
T_{REOT}	30%-85% rise time and fall time	-	-	-	35	
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.	-	-	-	105+ n*12UI	

1. Guaranteed by characterization results.

Figure 30. MIPI D-PHY HS/LP clock lane transition timing diagram

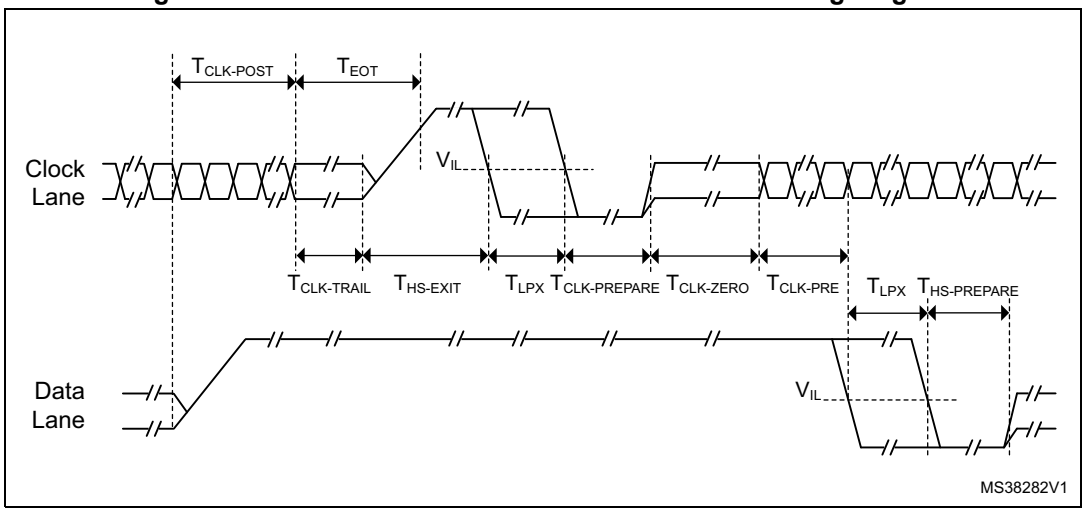
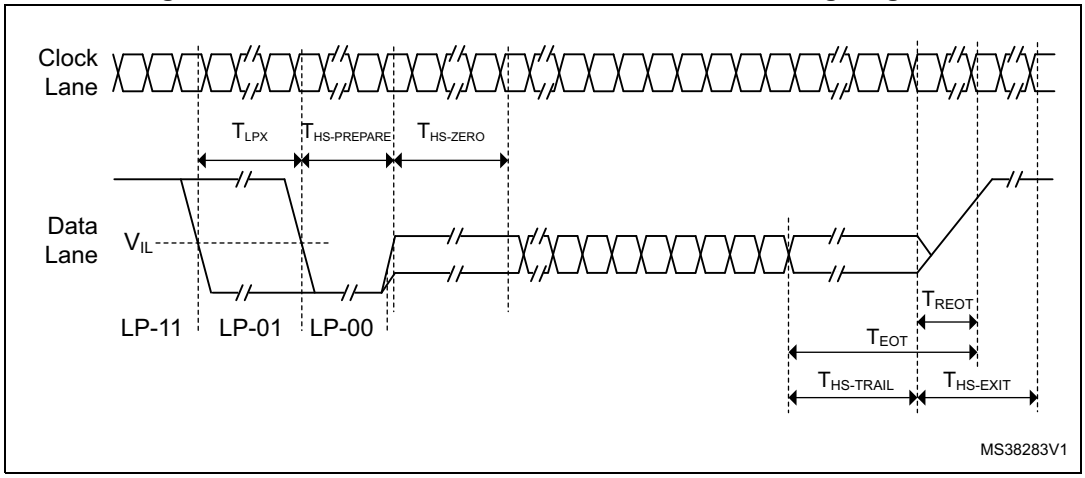


Figure 31. MIPI D-PHY HS/LP data lane transition timing diagram



6.3.11 MIPI D-PHY PLL characteristics

The parameters given in *Table 57* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21*.

Table 57. DSI-PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	100	MHz
f_{PLL_INFIN}	PFD input clock	-	4	-	25	
f_{PLL_OUT}	PLL multiplier output clock	-	31.25	-	500	
f_{VCO_OUT}	PLL VCO output	-	500	-	1000	
t_{LOCK}	PLL lock time	-	-	-	200	µs

Table 57. DSI-PLL characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLL)}$	PLL power consumption on V_{DD12}	f_{VCO_OUT} = 500 MHz	-	0.55	0.70	mA
		f_{VCO_OUT} = 600 MHz	-	0.65	0.80	
		f_{VCO_OUT} = 1000 MHz	-	0.95	1.20	

1. Guaranteed by characterization results.

6.3.12 MIPI D-PHY regulator characteristics

The parameters given in *Table 58* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21*.

Table 58. DSI regulator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD12DSI}$	1.2 V internal voltage on $V_{DD12DSI}$	-	1.15	1.20	1.30	V
C_{EXT}	External capacitor on V_{CAPDSI}	-	1.1	2.2	3.3	µF
ESR	External Serial Resistor	-	0	25	600	mΩ
$I_{DDDSIREG}$	Regulator power consumption	-	100	120	125	µA
I_{DDDSI}	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI}	Ultra Low Power Mode (Reg. ON + PLL OFF)	-	290	600	µA
		Stop State (Reg. ON + PLL OFF)	-	290	600	
$I_{DDDSILP}$	DSI system current consumption on V_{DDDSI} in LP mode communication(2)	10 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	mA
		20 MHz escape clock (Reg. ON + PLL OFF)	-	4.3	5.0	
$I_{DDDSIHS}$	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode communication(3)	300 Mbps - 1 data lane (Reg. ON + PLL ON)	-	8.0	8.8	mA
		300 Mbps - 2data lane (Reg. ON + PLL ON)	-	11.4	12.5	
		500 Mbps - 1 data lane (Reg. ON + PLL ON)	-	13.5	14.7	
		500 Mbps - 2data lane (Reg. ON + PLL ON)	-	18.0	19.6	
	DSI system (regulator, PLL and D-PHY) current consumption on V_{DDDSI} in HS mode with CLK like payload	500 Mbps - 2data lane (Reg. ON + PLL ON)	-	21.4	23.3	
t_{WAKEUP}	Startup delay	C_{EXT} = 2.2 µF	-	110	-	µs
		C_{EXT} = 3.3 µF	-	-	160	
I_{INRUSH}	Inrush current on V_{DDDSI}	External capacitor load at start	-	60	200	mA

1. Guaranteed by characterization results.
2. Values based on an average traffic in LP Command Mode.
3. Values based on an average traffic (3/4 HS traffic & 1/4 LP) in Video Mode.

6.3.13 Flash memory characteristics

Table 59. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	41.8	43	
		Fast programming	30.4	31	
t_{ERASE}	Page (4 Kbytes) erase time	-	22	24.5	
t_{prog_bank}	One bank (1 Mbyte) programming time	Normal programming	10.7	11	s
		Fast programming	7.7	8	
t_{ME}	Mass erase time (one or two banks)	-	22.1	25	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 60. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 61*. They are based on the EMS levels and classes defined in application note AN1709.

Table 61. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 62. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 120 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA169 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-2	dBµV
			30 MHz to 130 MHz	3	
			130 MHz to 1 GHz	10	
			1 GHz to 2 GHz	8	
			EMI Level	3	-

6.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 63. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 64. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 65*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 65. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except PA4, PA5, PB0, PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0, OPAMP1_V1NM, OPAMP2_V1NM	-5	NA	mA
	Injected current on pins PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0	0	NA	
	Injected current on pins OPAMP1_V1NM, OPAMP2_V1NM	0	0	
	Injected current on PA4, PA5, PB0 pins	-5	0	

1. Guaranteed by characterization.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 66. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3xV_{DDIOx}$(2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.39xV_{DDIOx}$-0.06(3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	$0.43xV_{DDIOx}$-0.1(3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.17xV_{DDIOx}$(3)	

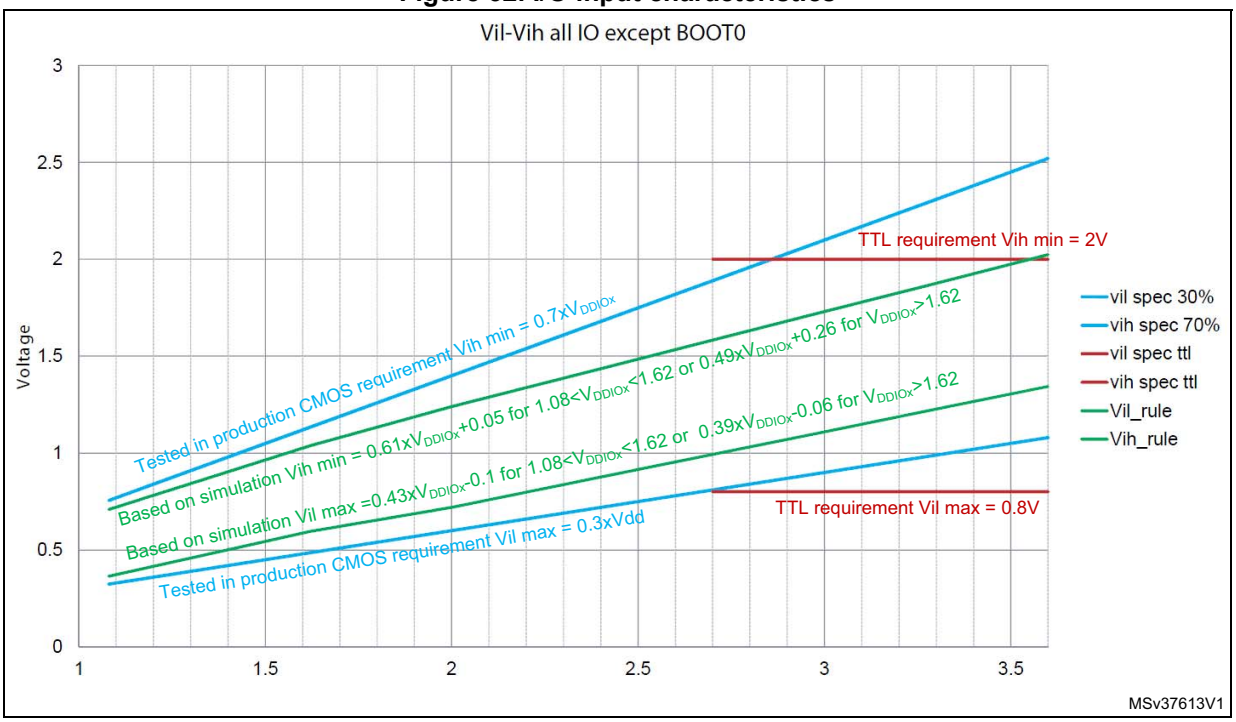
Table 66. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u, PB2 and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 32: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.
5. All TX_xx IO except FT_lu, FT_u, PB2 and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:
   $I_{Total\_lleak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 82: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 32* for standard I/Os, and in *Figure 32* for 5 V tolerant I/Os.

Figure 32. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 67. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.35 x V_{DDIOx}	
V_{OH}(3)	Output high level voltage for an I/O pin		0.65xV_{DDIOx}	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 33* and *Table 68*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 68. I/O AC characteristics(1)(2)

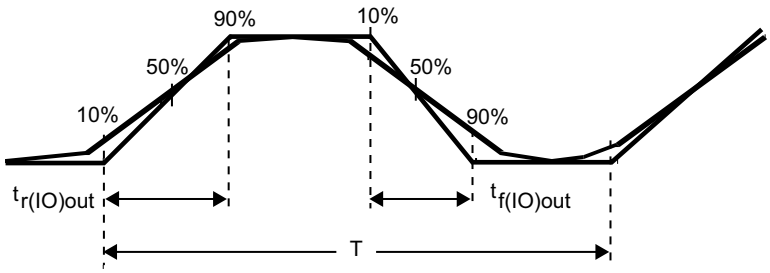
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 68. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0432 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Figure 33. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 68: I/O AC characteristics*.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

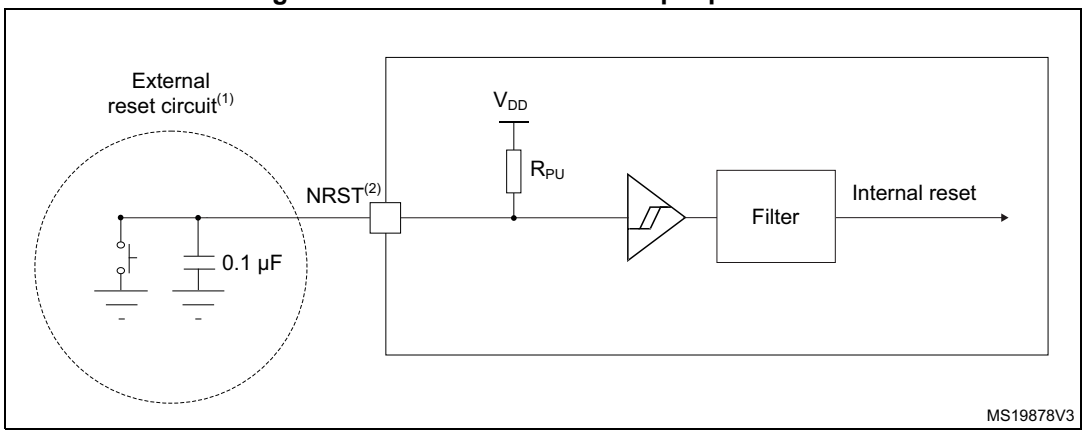
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 69. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 34. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 69: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 70. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.20 Analog switches booster

Table 71. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

6.3.21 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 72* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 72. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

Table 72. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
   Refer to *Section 4: Pinouts and pin description* for further details.

The maximum value of R_{AIN} can be found in *Table 73: Maximum ADC RAIN*.

Table 73. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

Table 74. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 74. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 75. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 75. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 76. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 76. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 77. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 77. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 35. ADC accuracy characteristics

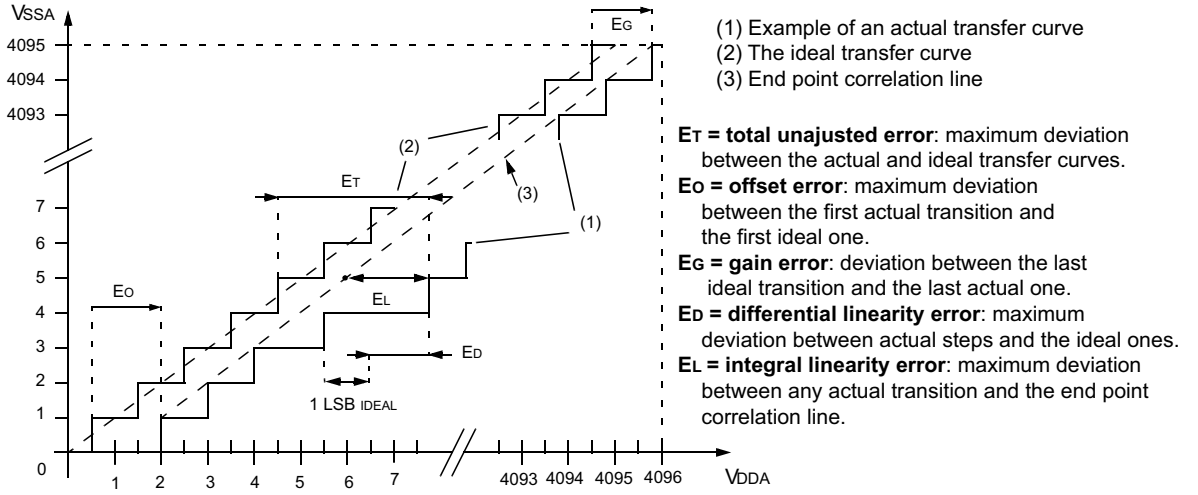
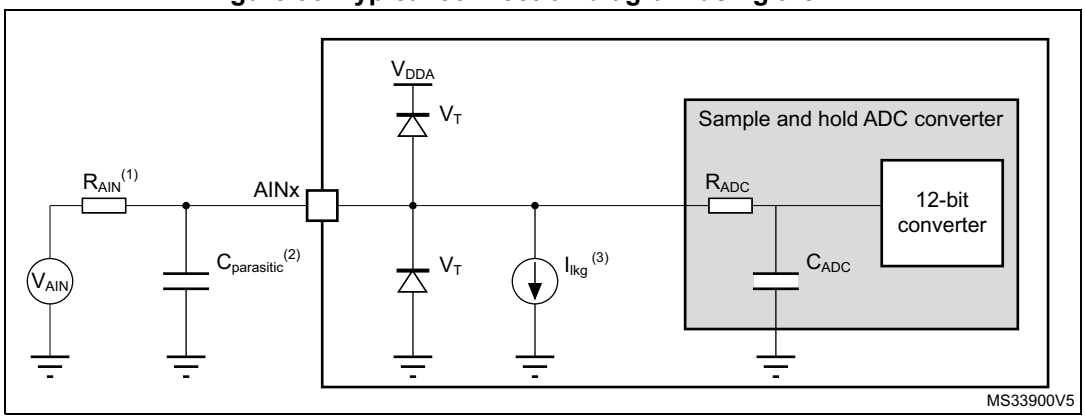


Figure 36. Typical connection diagram using the ADC



1. Refer to *Table 72: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 66: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 66: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 20: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.22 Digital-to-Analog converter characteristics

Table 78. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 78. DAC characteristics(1) (continued)

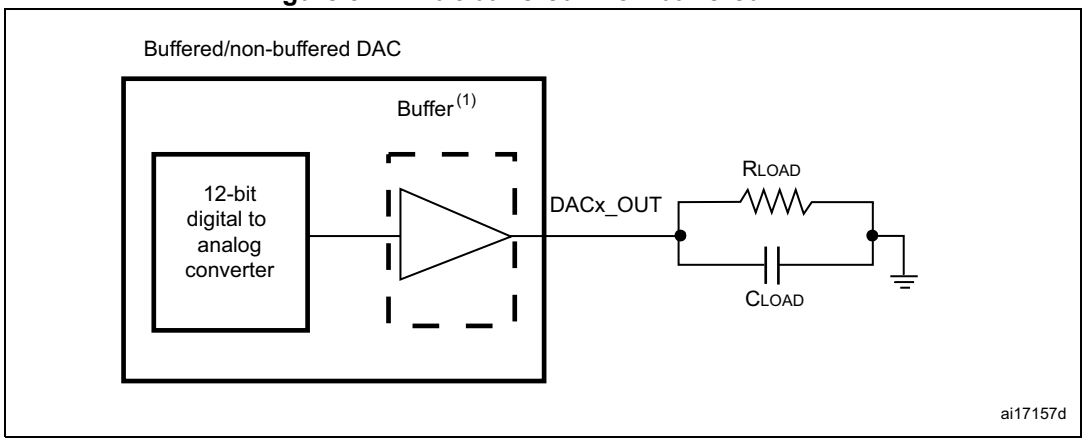
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 78. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 66: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0432 reference manual for more details.

Figure 37. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 79. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 79. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

6.3.23 Voltage reference buffer characteristics

Table 80. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.037	2.042	2.047	
			V_{RS} = 1	2.494	2.5	2.506	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(3)		-	300	350	µs
		CL = 1.1 µF(3)		-	500	650	
		CL = 1.5 µF(3)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (4)	-	-	-	8	-	mA

Table 80. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.24 Comparator characteristics

Table 81. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 81. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-(4)	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 24: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 66: I/O static characteristics*.

6.3.25 Operational amplifiers characteristics

Table 82. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.	-	-	±1.5	mV
		All voltage/Temp.	-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	±5	-	µV/°C
		Low-power mode	-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	-	1	1.35	

Table 82. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Table 82. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132 and UFBGA169 only)		-	-	(3)	nA
		Dedicated input (UFBGA132 and UFBGA169 only)	T_J ≤ 75 °C	-	-	1	
			T_J ≤ 85 °C	-	-	3	
			T_J ≤ 105 °C	-	-	8	
			T_J ≤ 125 °C	-	-	15	
PGA gain(2)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode(4)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	

Table 82. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.
3. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in *Table 66: I/O static characteristics*.
4. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

6.3.26 Temperature sensor characteristics

Table 83. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.27 V_{BAT} monitoring characteristics

Table 84. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 85. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.28 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 86* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

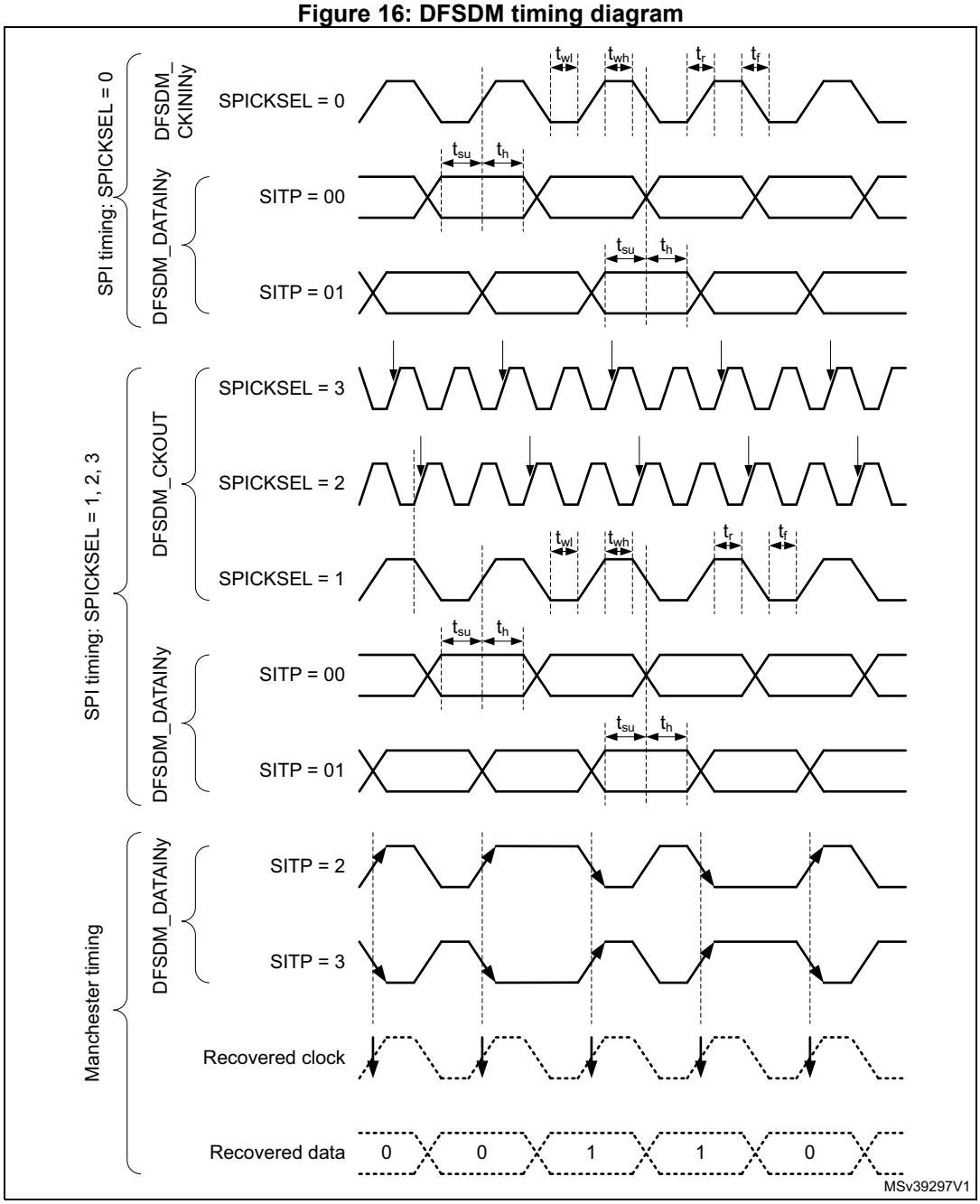
Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINy, DFSDM1_DATINy, DFSDM1_CKOUT for DFSDM).

Table 86. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20	
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	45	50	55	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2$-0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	0	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 16: DFSDM timing diagram



6.3.29 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.17: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 87. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	8.33	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 120 MHz	0	60	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	0.00833	546.13	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	-	35.77	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 88. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 89. WWDG min/max timeout value at 120 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0341	2.1845	ms
2	1	0.0683	4.3691	
4	2	0.1356	8.7381	
8	3	0.2731	17.4763	

6.3.30 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0432 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 90* below for the analog filter characteristics:

Table 90. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 91* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 91. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	-	60	MHz
		Master mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			46	
		Master transmitter mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			60	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			60	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range V1			33	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range V1			21	
		1.71 V < V_{DD} < 3.6 V Voltage Range V2			13	
		1.08 V < V_{DD} < 1.32 V(3)			12	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4xT_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2xT_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-1	T_{PCLK}	T_{PCLK}+1	ns
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6	-	-	ns
$t_{h(SI)}$		Slave mode	5.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns

Table 91. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	13	15	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1	-	10	23	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V2	-	13	25	
		Slave mode 1.08 V < V_{DD} < 1.32 V(3)	-	29	39	
$t_{v(MO)}$		Master mode	-	2	4	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
		Slave mode 1.08 < V_{DD} < 1.32 V(3)	26	-	-	
$t_{h(MO)}$		Master mode	1	-	-	

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.
3. SPI mapped on Port G.

Figure 38. SPI timing diagram - slave mode and CPHA = 0

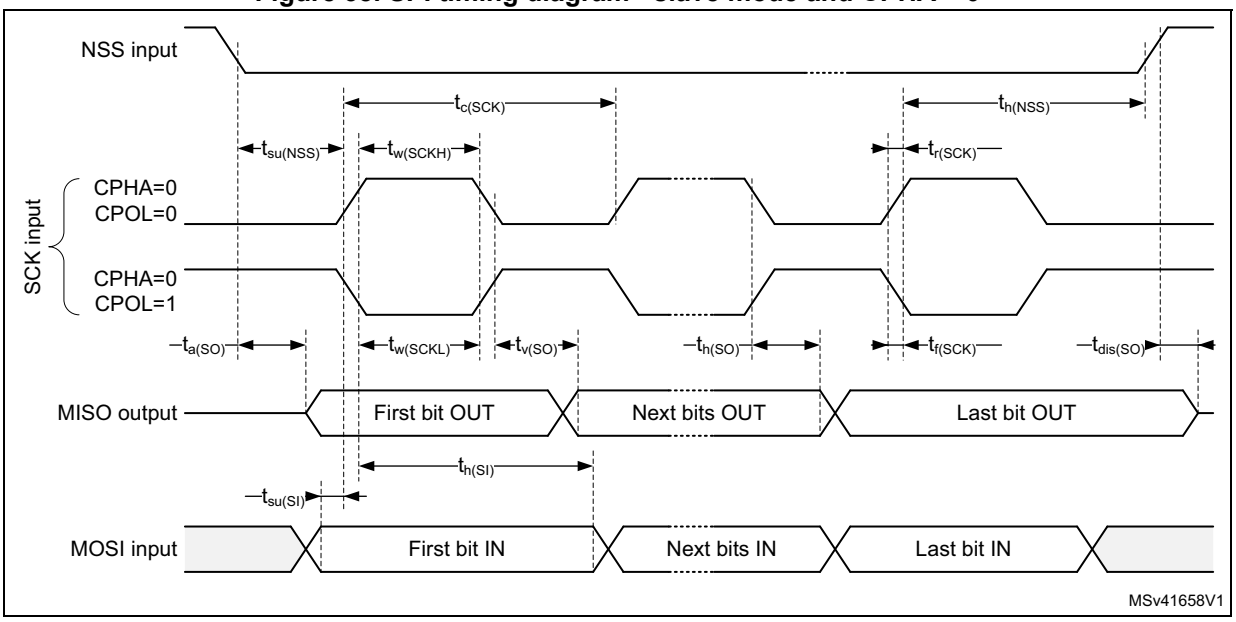
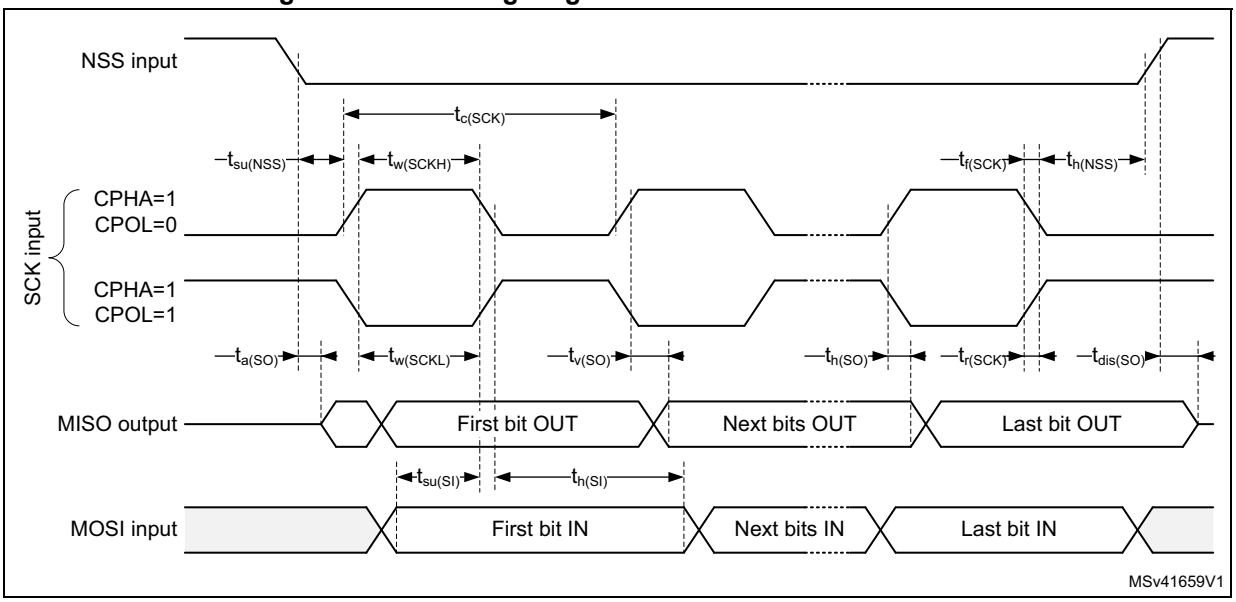
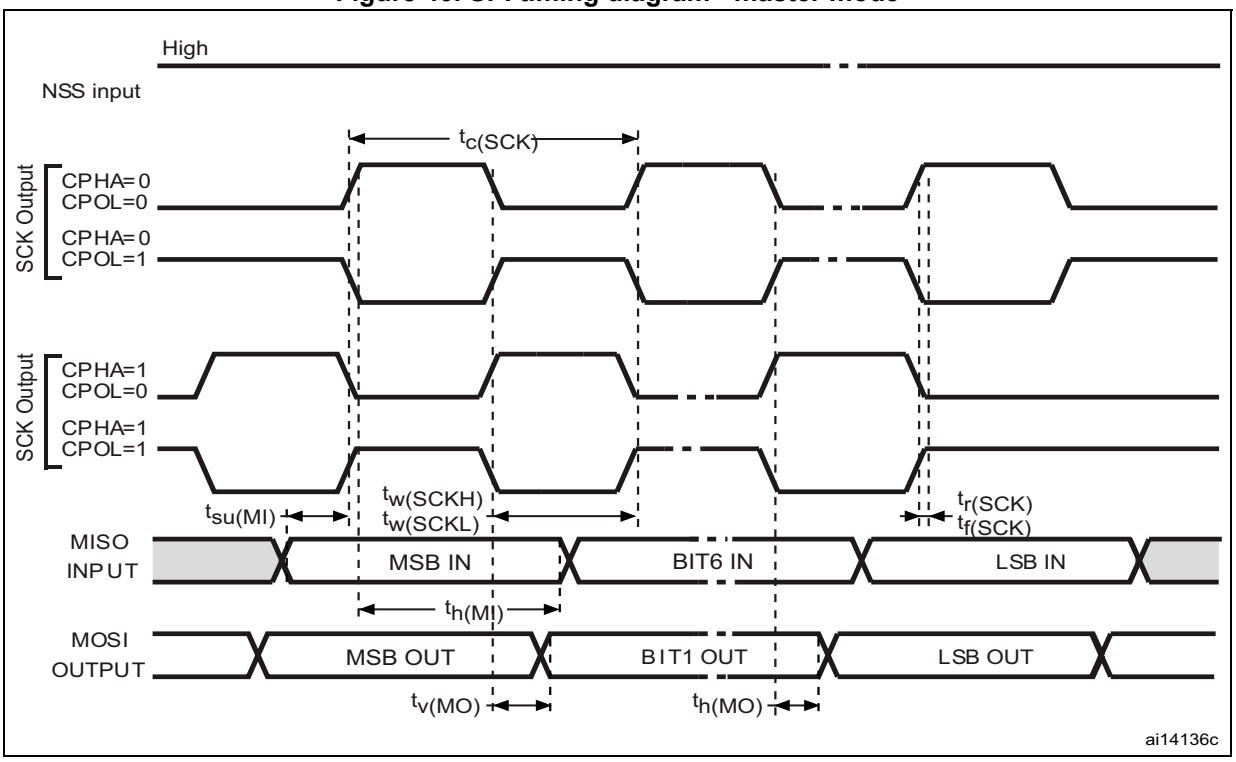


Figure 39. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 40. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 92* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in*Table 21: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 92. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	13	
		1.08 V ≤ V_{DD} ≤ 1.32 V	-	9	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2.5	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	6.5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	25	
		Slave transmitter (after enable edge) 1.08 V < V_{DD} <1.32 V	-	50	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns

Table 92. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	25	
		Master transmitter (after enable edge) 1.08 V ≤ V_{DD} ≤ 1.32 V	-	52	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 41. SAI master timing waveforms

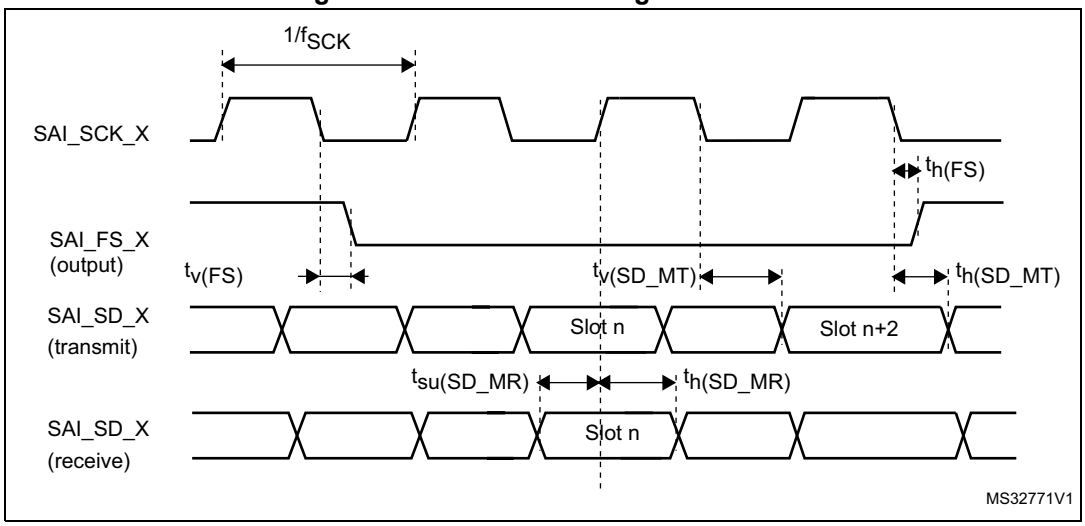
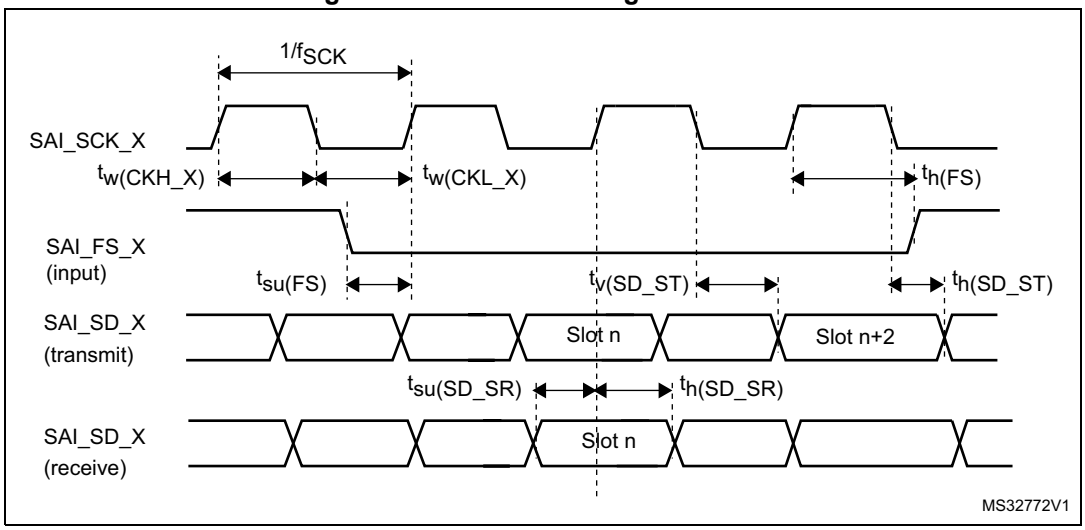


Figure 42. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

The device's USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 93. USB electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	
V_{OH}	Static output level high	R_L of 15 kΩ to 3.6 V(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_FS_DP/DM)	$V_{IN} = V_{DD}$	14.25	-	24.8	kΩ
R_{PU}(3)	Pull Up Resistor on PA12 (USB_FS_DP)	$V_{IN} = V_{SS}$ during idle	0.9	1.25	1.575	
	Pull Up Resistor on PA12 (USB_FS_DP)	$V_{IN} = V_{SS}$ during reception	1.425	2.25	3.09	
	Pull Up Resistor on PA10 (OTG_FS_ID)	-	-	-	14.5	

1. All the voltages are measured from the local ground potential.
2. The STM32L4S5xx USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at its default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 43. USB OTG timings – definition of data signal rise and fall time

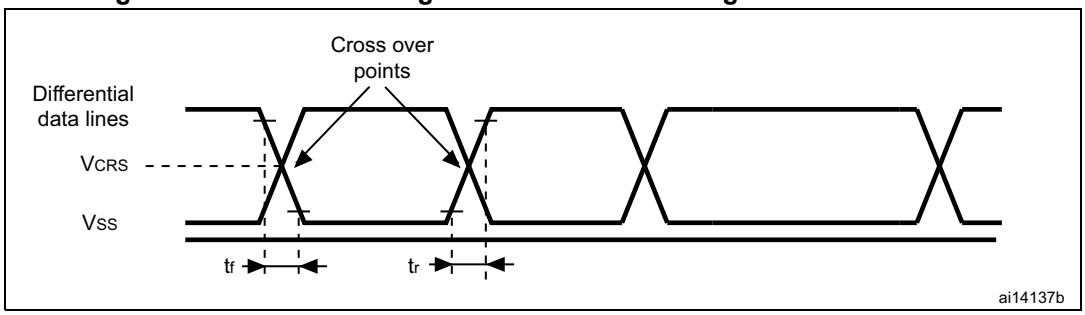


Table 94. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF			
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 95. USB BCD DC electrical characteristics(1)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-		
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V

Table 95. USB BCD DC electrical characteristics(1) (continued)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
VLGC	Logic threshold	-	0.8	-	2.0	V
VDAT_REF	Data detect voltage	-	0.25	-	0.4	V
VDP_SRC	D+ source voltage	-	0.5	-	0.7	V
VDM_SRC	D- source voltage	-	0.5	-	0.7	V
IDP_SINK	D+ sink current	-	25	-	175	µA
IDM_SINK	D- sink current	-	25	-	175	µA

1. Guaranteed by design

CAN (controller area network) interface

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.31 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 96* to *Table 109* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 21*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 44 through *Figure 47* represent asynchronous waveforms and *Table 96* through *Table 103* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Figure 44. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

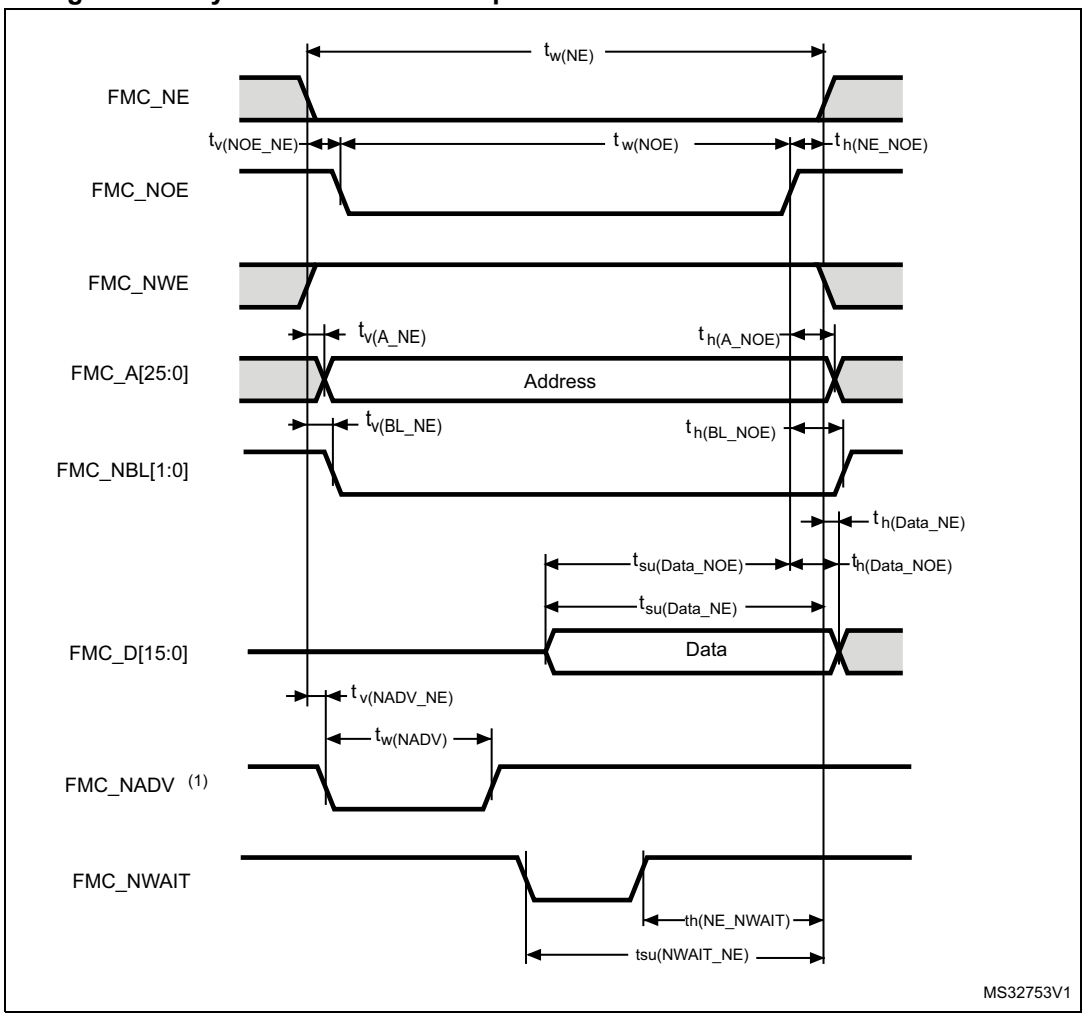


Table 96. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-0.5	$3T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$2T_{HCLK}$-1	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}+14	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	14	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 97. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$-0.5	$8T_{HCLK}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$7T_{HCLK}$-0.5	$7T_{HCLK}$+0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+12.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+12	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

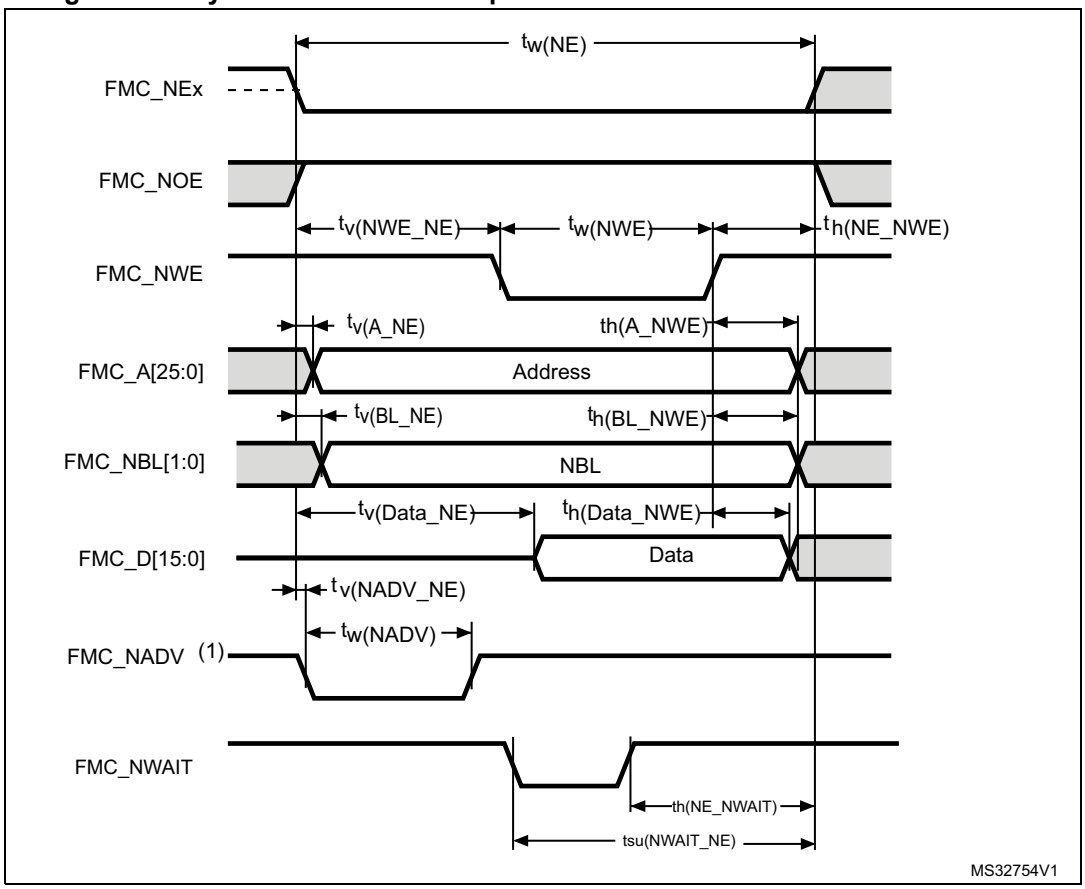


Table 98. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$2T_{HCLK}$-1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+1	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 99. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+1.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}$-0.5	$6T_{HCLK}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{HCLK}$-13	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{HCLK}$+13	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 46. Asynchronous multiplexed PSRAM/NOR read waveforms

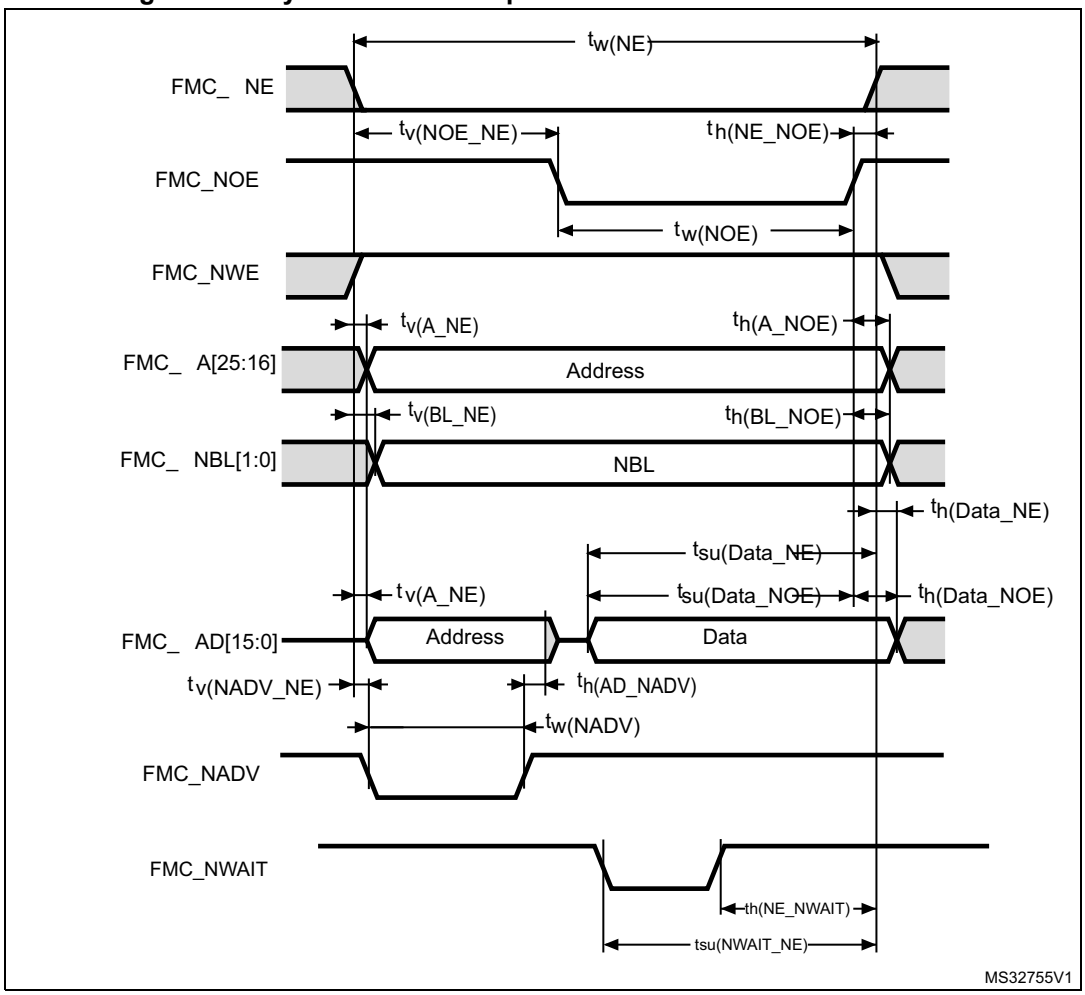


Table 100. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$-0.5	$2T_{HCLK}$+1	
$t_{w(NOE)}$	FMC_NOE low time	T_{HCLK}-0.5	T_{HCLK}+0.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	T_{HCLK}-1	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}	T_{HCLK}+1.5	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	T_{HCLK}-3	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}+14	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	14	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 101. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+ 1	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{HCLK}$-0.5	$6T_{HCLK}$+1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+12	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+11	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 47. Asynchronous multiplexed PSRAM/NOR write waveforms

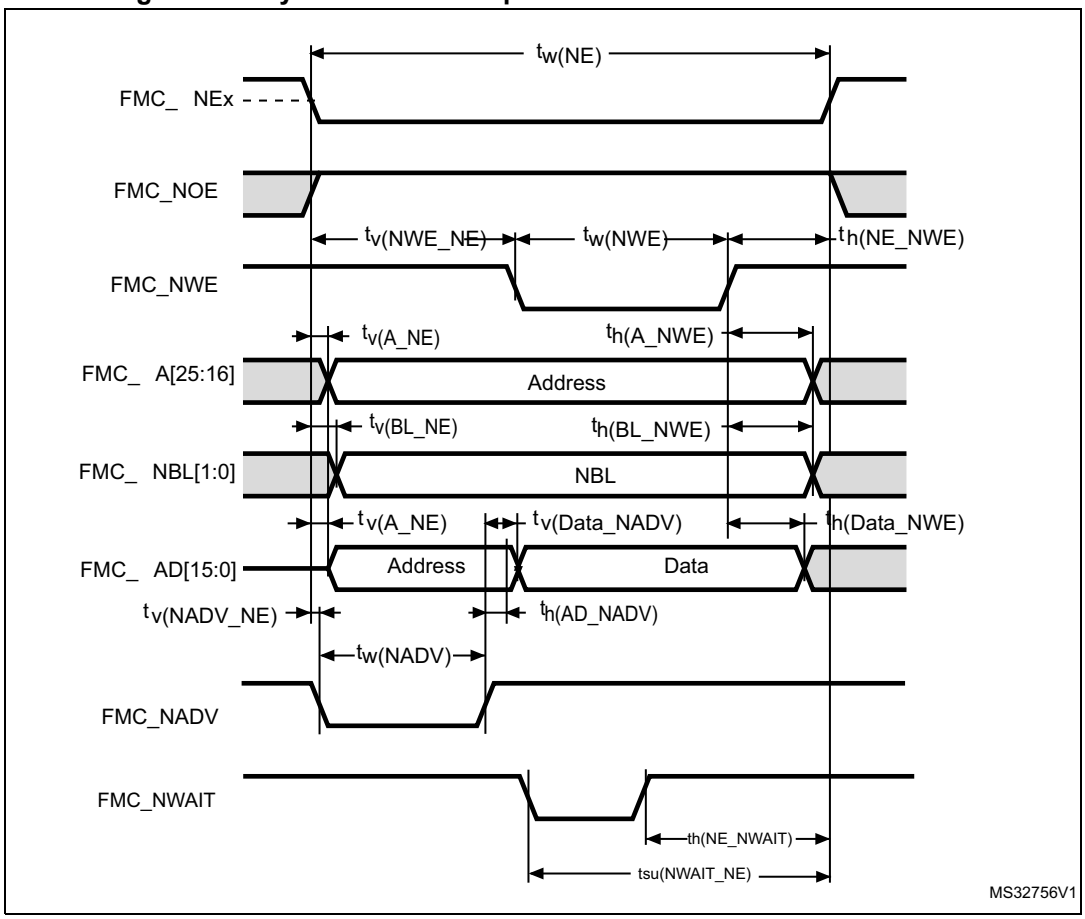


Table 102. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$5T_{HCLK}$-0.5	$5T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}+0.5	T_{HCLK}+1.5	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}-3	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	0	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK}+2	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 103. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$10T_{HCLK}$-0.5	$10T_{HCLK}$+1	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$-0.5	$7T_{HCLK}$+0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7T_{HCLK}$+12.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5T_{HCLK}$+13	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 48 through *Figure 51* represent synchronous waveforms and *Table 104* through *Table 107* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V ≤ V_{DD} ≤ 3.6 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 54 MHz for CLKDIV = 0x0 at CL = 30 pF (on FMC_CLK).
- For 1.71 V ≤ V_{DD} ≤ 2.7 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 32 MHz for CLKDIV = 0x0 at CL= 20 pF (on FMC_CLK).

Figure 48. Synchronous multiplexed NOR/PSRAM read timings

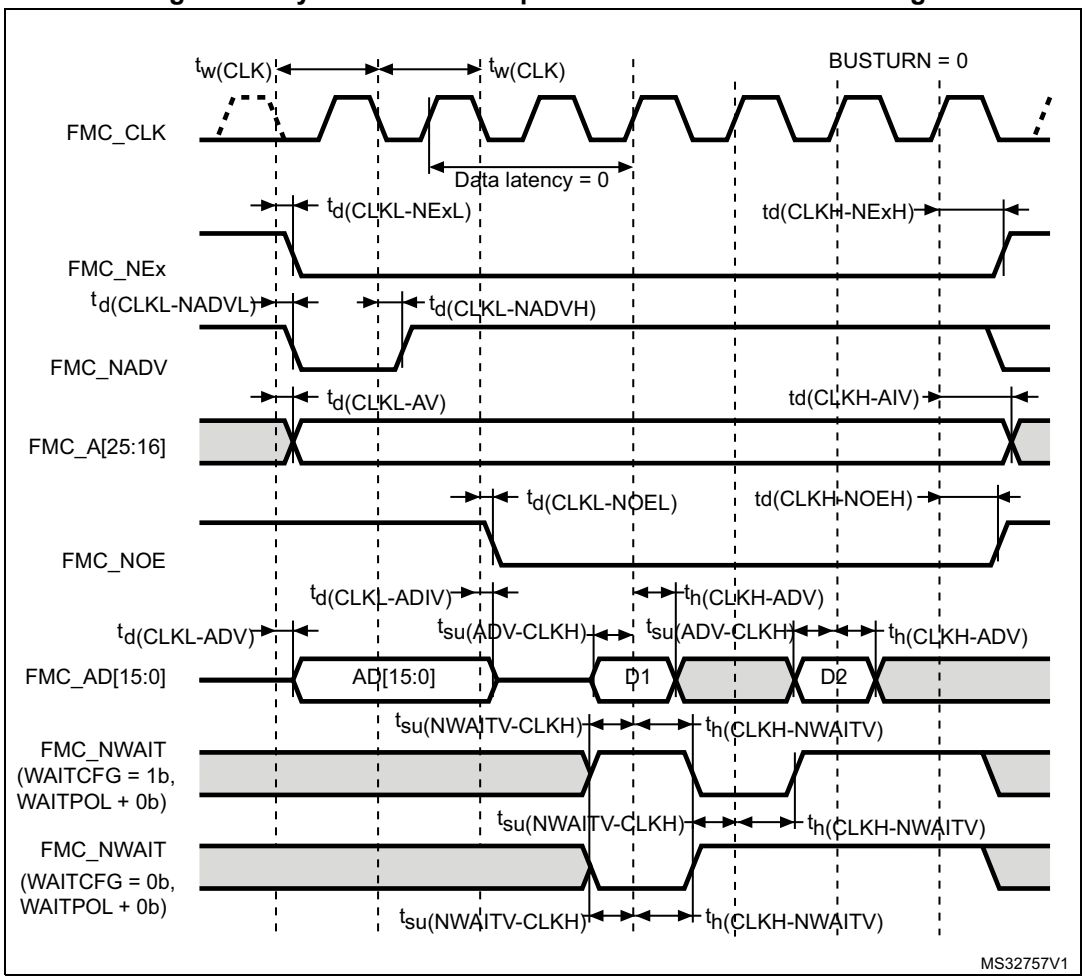


Table 104. Synchronous multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	4	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 49. Synchronous multiplexed PSRAM write timings

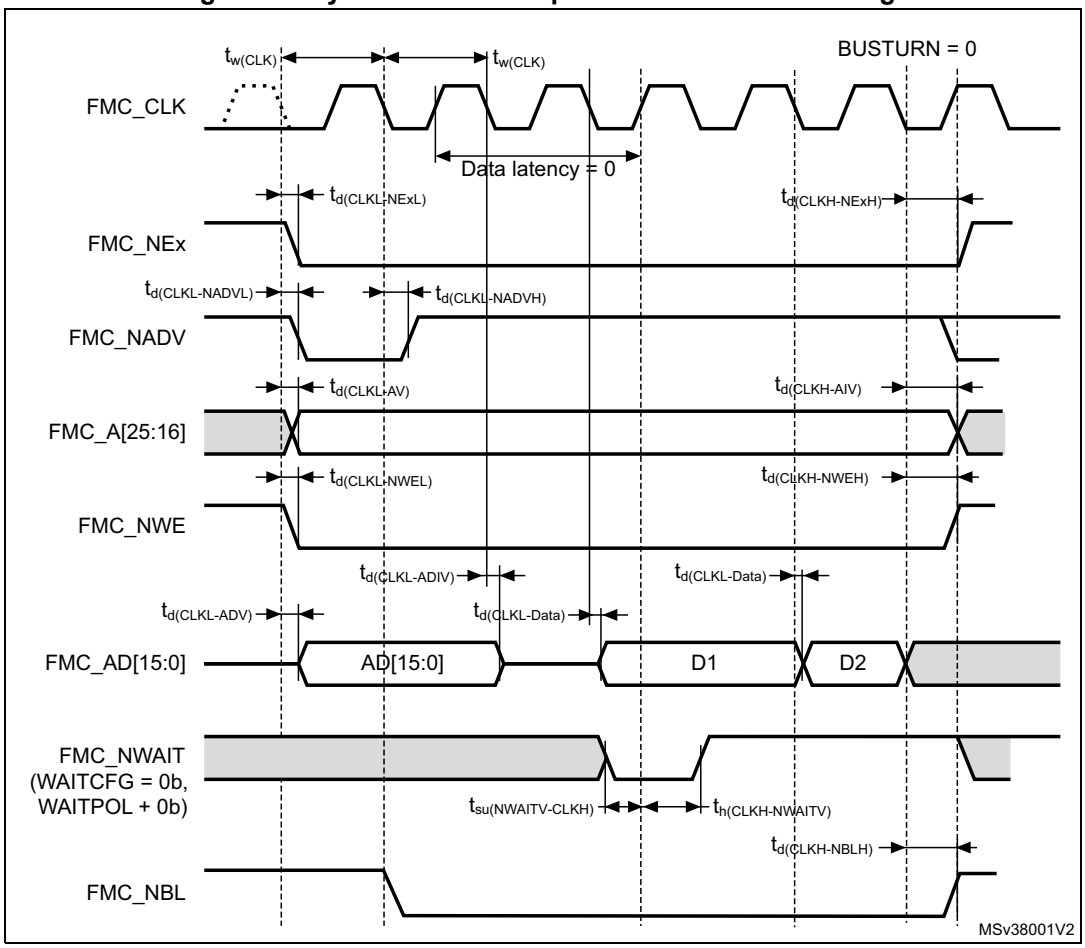


Table 105. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}- 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	RxT_{HCLK}/2 +1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 50. Synchronous non-multiplexed NOR/PSRAM read timings

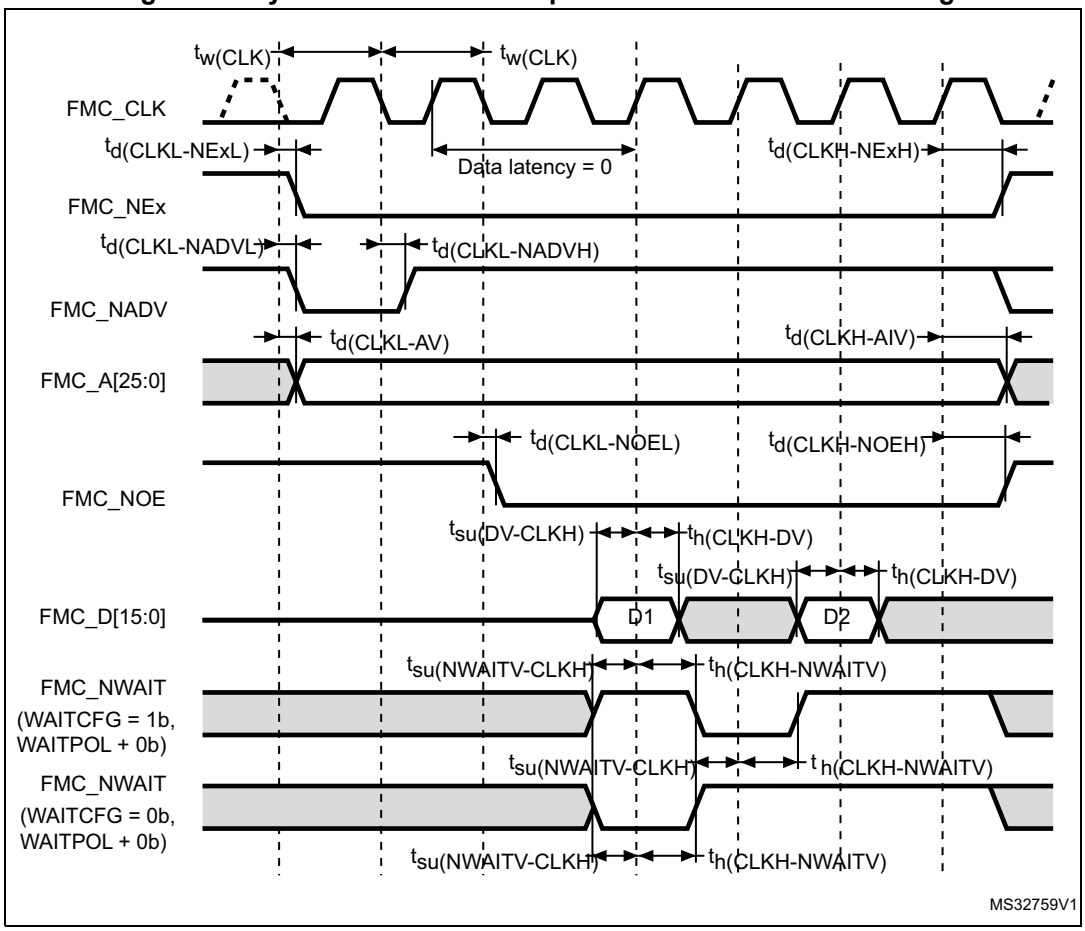


Table 106. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK} -0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +0.5	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	RxT_{HCLK}/2 +1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	4	-	

Table 106. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 51. Synchronous non-multiplexed PSRAM write timings

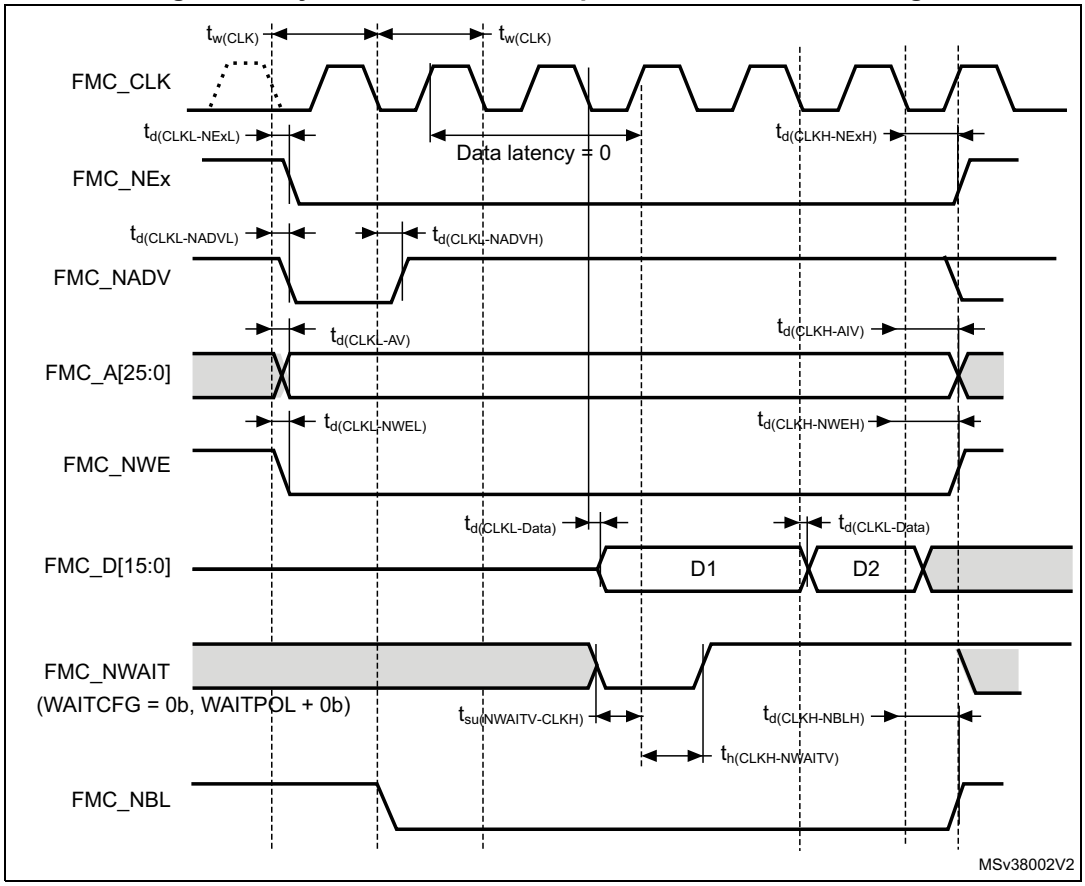


Table 107. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +0.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	RxT_{HCLK}/2 +1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

Figure 52 through *Figure 55* represent synchronous waveforms, and *Table 108* and *Table 109* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 52. NAND controller waveforms for read access

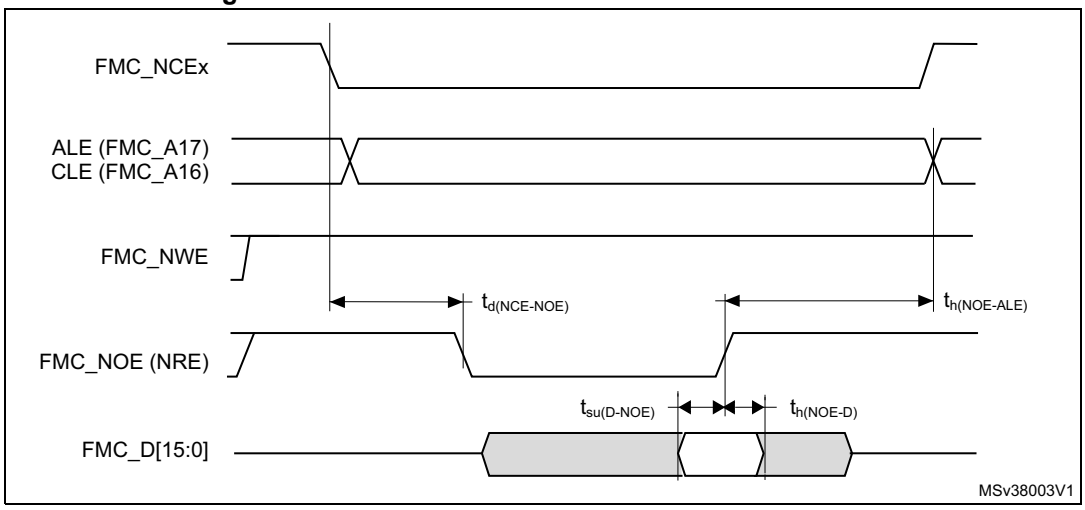


Figure 53. NAND controller waveforms for write access

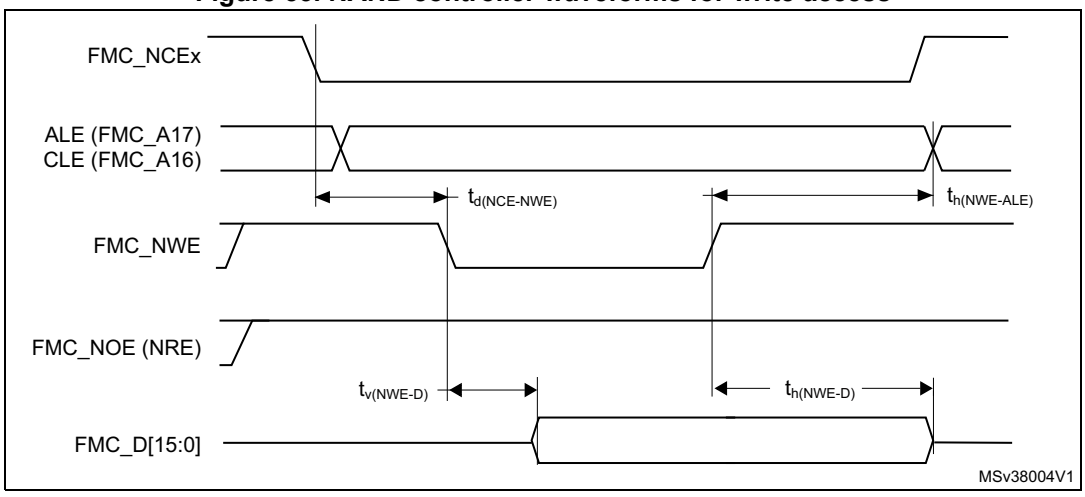


Figure 54. NAND controller waveforms for common memory read access

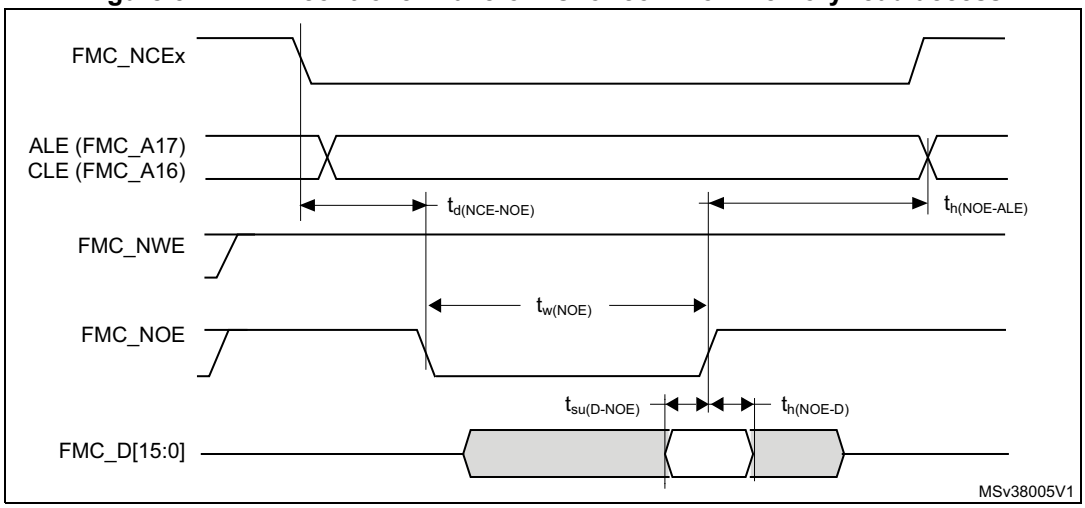


Figure 55. NAND controller waveforms for common memory write access

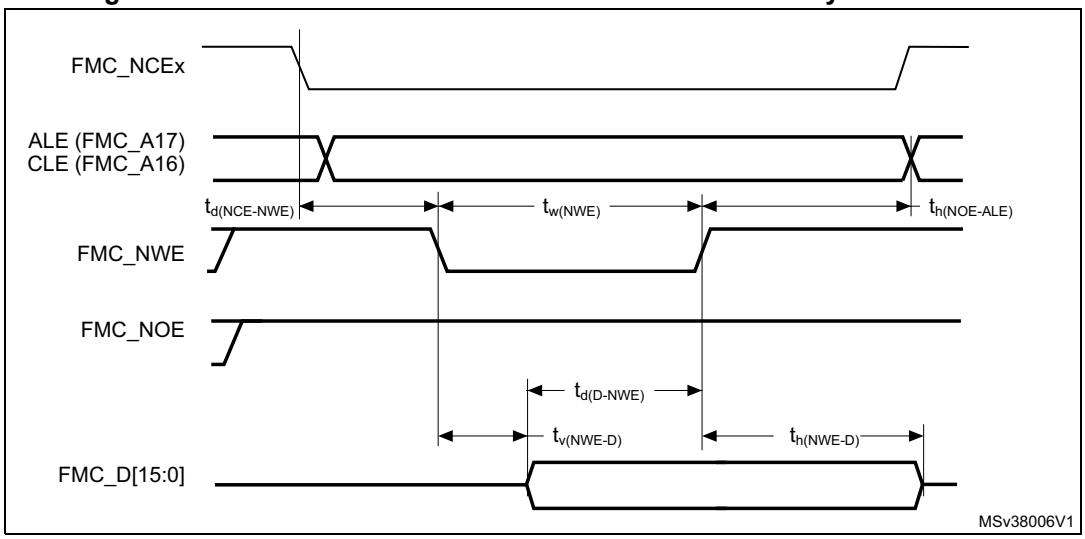


Table 108. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	14	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 109. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$2T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$-1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}$-0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.32 OctoSPI characteristics

Unless otherwise specified, the parameters given in *Table 110*, *Table 111* and *Table 112* for OctoSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 110. OctoSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	OctoSPI clock frequency	1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	58	MHz
		2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	-	-	86	
		1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 15 pF	-	-	66	
		1.71 V < V_{DD}< 3.6 V Voltage Range 2 C_{LOAD} = 20 pF	-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	Prescaler = 0	$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	0.5	-	-	
		Voltage Range 2	0	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	7.75	-	-	
		Voltage Range 2	10.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2	3.5	
		Voltage Range 2	-	4	5.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

Table 111. OctoSPI(1) characteristics in DTR mode (no DQS)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	OctoSPI clock frequency	1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	58	MHz
		2.7 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	60	
		1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 15 pF		-	-	60	
		1.71 V < V_{DD} < 3.6 V Voltage Range 2 C_{LOAD} = 20 pF		-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}$/2-1	-	$t_{(CK)}$/2+0.5	ns
$t_{w(CKL)}$				$t_{(CK)}$/2-1	-	$t_{(CK)}$/2+0.5	
$t_{sf(IN)}$ $t_{sr(IN)}$	Data input setup time	Voltage Range 1		0.5	-	-	
		Voltage Range 2		1	-	-	
$t_{hf(IN)}$ $t_{hr(IN)}$	Data input hold time	Voltage Range 1		7.75	-	-	
		Voltage Range 2		10.75	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	
			DHQC = 1 Pres=1,2 ...		tpclk/4+1	tpclk/4+3	
		Voltage Range 2	DHQC = 0		8.5	12	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	1	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-2	-	-	
		Voltage Range 2	DHQC = 0	3.5	-	-	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

Table 112. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and HyperBus™

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
F_{CK} $1/t_{(CK)}$	OctoSPI clock frequency (Octal Flash and HyperFlash™)	1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	60	MHz
		2.7 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	64	
		1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 15 pF		-	-	60	
		1.71 V < V_{DD} < 3.6 V Voltage Range 2 C_{LOAD} = 20 pF		-	-	26	
	OctoSPI clock frequency (HyperRAM™)	1.71 < V_{DD} < 3.6 V Voltage Range V1 C_{LOAD} = 20 pF t_{CKDS} = 9ns	Prescaler = 0,1,3,5...	-	-	18	
			Prescaler = 2,4,6...	-	-	25	
		2.7 < V_{DD} < 3.6 V Voltage Range V1 C_{LOAD} = 20 pF t_{CKDS} = 9ns	Prescaler = 0,1,3,5...	-	-	22	
			Prescaler = 2,4,6...	-	-	29	
		1.71 < V_{DD} < 3.6 V Voltage Range V2 C_{LOAD} = 20 pF t_{CKDS} = 9ns	-	-	-	17	

Table 112. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and HyperBus™ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+0.5$	
$t_{v(CK)}$	Clock valid time	-		-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-		$t_{(CK)}/2-0.5$	-	-	
$t_{w(CS)}$	Chip select high time	-		3 x $t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-		0	-	-	
$t_{v(DS)}$	Data storbe input valid time	-		0	-	-	
$t_{h(DS)}$	Data storbe input hold time	-		0	-	-	
$t_{v(RWDS)}$	Data storbe output valid time	-		-	-	3 x $t_{(CK)}$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		-3.5	-	$t_{(CK)}/2-5.75$(3)	
		Voltage Range 2		-5.5	-	$t_{(CK)}/2-9$(3)	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		5.75	-	-	
		Voltage Range 2		9	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	ns
			DHQC = 1 Pres=1,2 ...		tpclk/4+1.5	tpclk/4+2.25	
		Voltage Range 2	DHQC = 0		8	11	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	0.5	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-1.75	-	-	
		Voltage Range 2	DHQC = 0	0.75	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Data input setup time maximum does not take into account Data level switching duration.

Figure 56. OctoSPI timing diagram - SDR mode

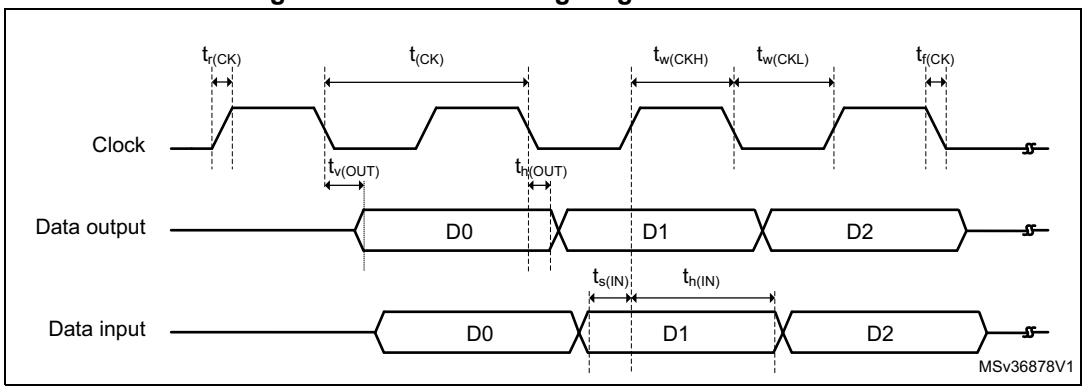


Figure 57. OctoSPI timing diagram - DDR mode

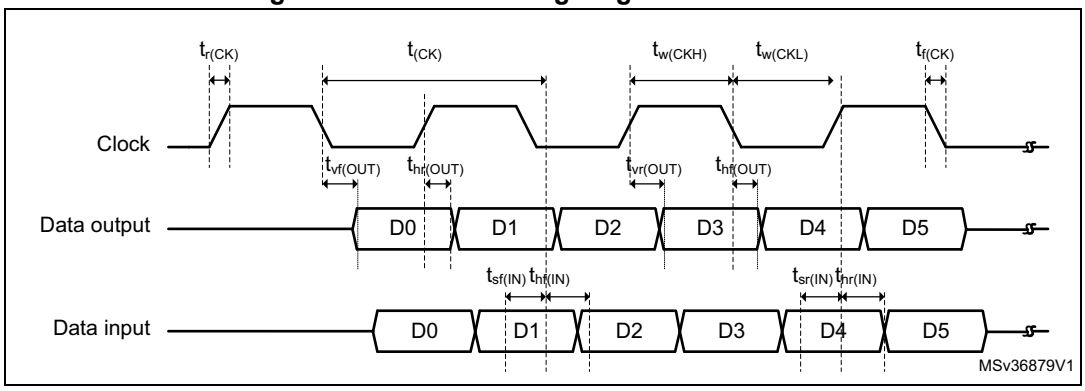


Figure 58. OctoSPI HyperBus™ clock

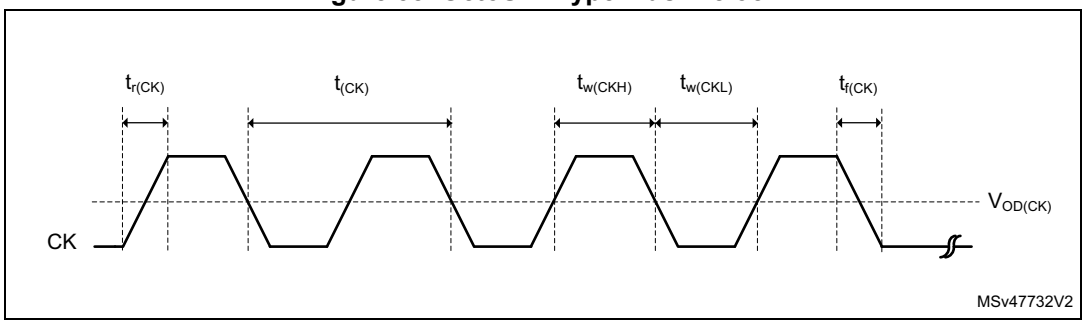


Figure 59. OctoSPI HyperBus™ read

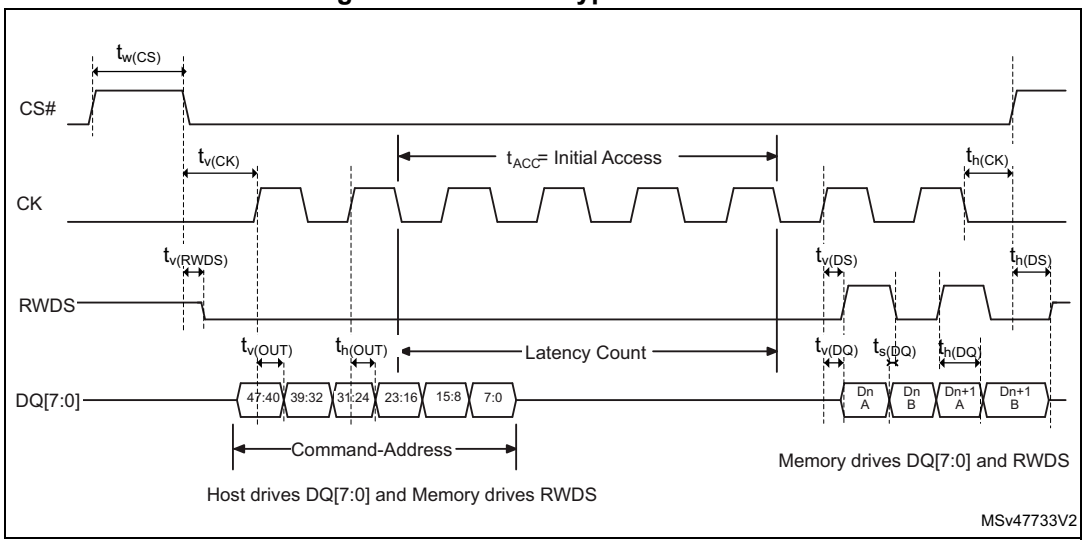


Figure 60. OctoSPI HyperBus™ read with double latency

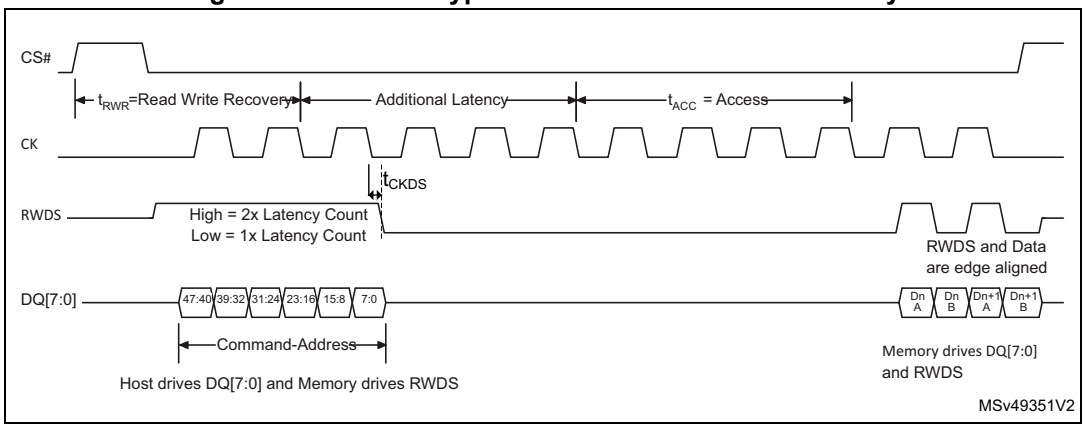
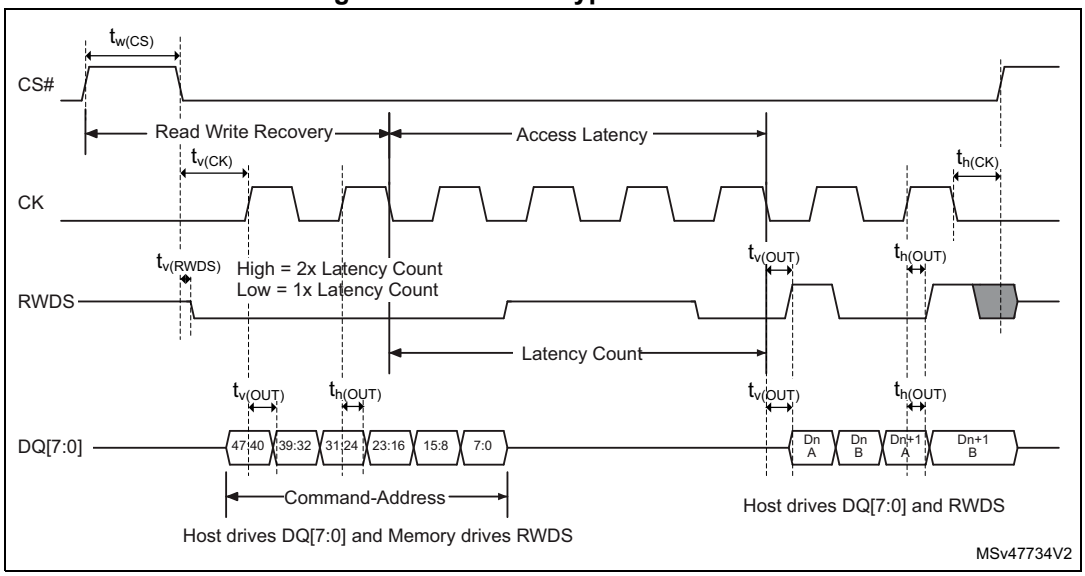


Figure 61. OctoSPI HyperBus™ write



6.3.33 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 113* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 62. DCMI timing diagram

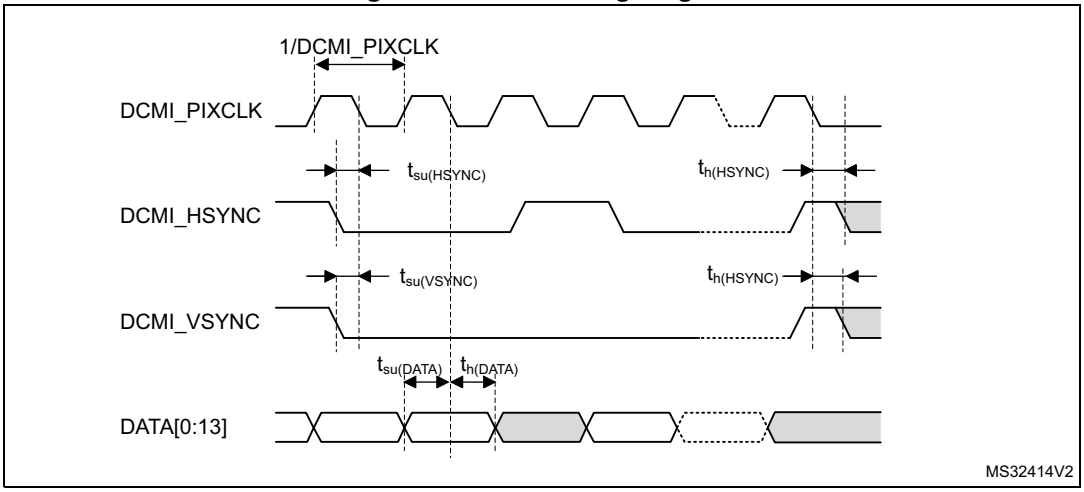


Table 113. DCMI characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	-	48	MHz
		1.71 < VDD < 3.6 Voltage range V2	-	10	
D_{pixel}	Pixel clock input duty cycle	-	30	70	%

Table 113. DCMI characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	1.71 < VDD < 3.6 Voltage range V1	5.5	-	ns
		1.71 < VDD < 3.6 Voltage range V2	8	-	
$t_{h(DATA)}$	Data hold time	1.71 < VDD < 3.6 Voltage range V1	0	-	
		1.71 < VDD < 3.6 Voltage range V2	0	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	1.71 < VDD < 3.6 Voltage range V1	6	-	
		1.71 < VDD < 3.6 Voltage range V2	9	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1.71 < VDD < 3.6 Voltage range V1	0	-	
		1.71 < VDD < 3.6 Voltage range V2	0	-	

1. Data based on characterization results, not tested in production.

6.3.34 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 114* for LCD-TFT are derived from tests performed under the ambient temperature, fHCLK frequency and VDD supply voltage summarized in *Table 21*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 114. LTDC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK} D_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V	-	83	MHz
		1.71 V < V_{DD} < 3.6 V	-	50	
	LTDC clock output duty cycle	-	45	55	%
tw(CLKH) tw(CLKL)	Clock high time Clock low time	-	tw(CLK)/2-0.5	tw(CLK)/2+0.5	-
t_v(DATA)	Data output valid time	-	-	6	
t_h(DATA)	Data output hold time	-	0	-	
t_v(HSYNC) t_v(VSYNC) t_v(DE)	HSYNC/VSYNC/DE output valid time	-	-	3	
t_h(HSYNC) t_h(VSYNC) t_h(DE)	HSYNC/VSYNC/DE output hold time	-	0	-	

1. Guaranteed by characterization results.

6.3.35 SD/SDIO/MMC card host interfaces (SDMMC)

Unless otherwise specified, the parameters given in Table xx for SDIO are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 21: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD} Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Table 115. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	66	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	

Table 115. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tISU	Input setup time HS	-	1.5	-	-	ns
tIHD	Input hold time HS	-	2	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tOV	Output valid time HS	-	-	5	6.5	ns
tOH	Output hold time HS	-	4	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	-	1.5	-	-	ns
tIHD	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	-	-	1	2.5	ns
tOHD	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. For SD 1.8 V support, an external voltage converter is needed.

Table 116. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	52	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp = 52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
tISU	Input setup time HS	-	0.5	-	-	ns
tIH	Input hold time HS	-	4.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
tOV	Output valid time HS	-	-	6	7.4	ns
tOH	Output hold time HS	-	4	-	-	

1. Guaranteed by characterization results.
2. Cload = 20 pF.

See the different SDMMC diagrams in *Figure 63*, *Figure 64* and *Figure 65* below.

Figure 63. SDIO high-speed mode

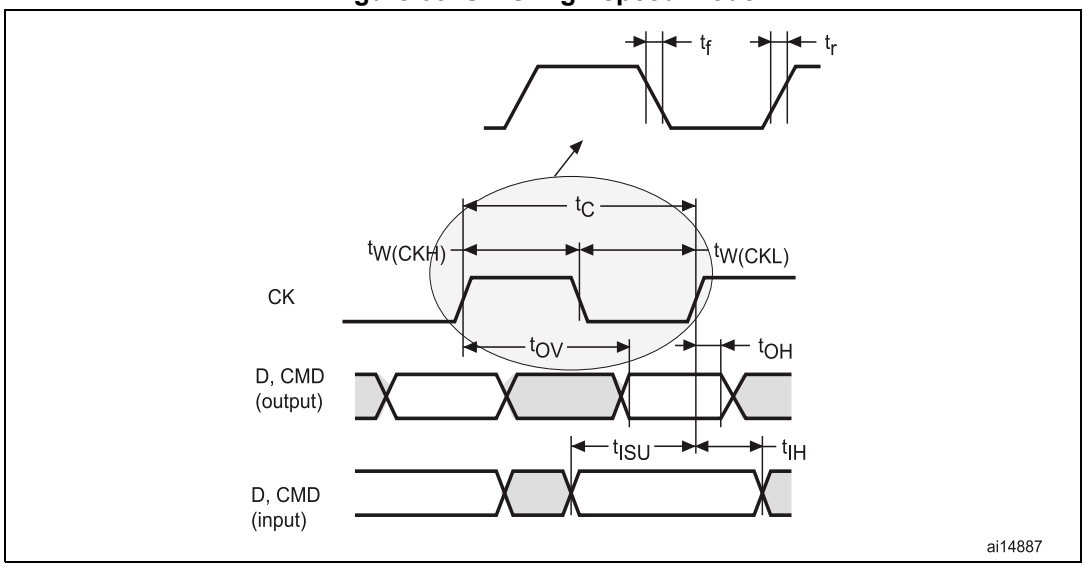


Figure 64. SD default mode

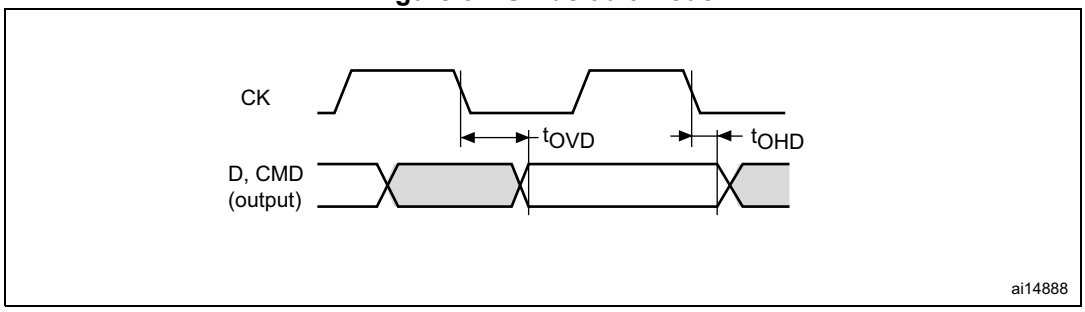
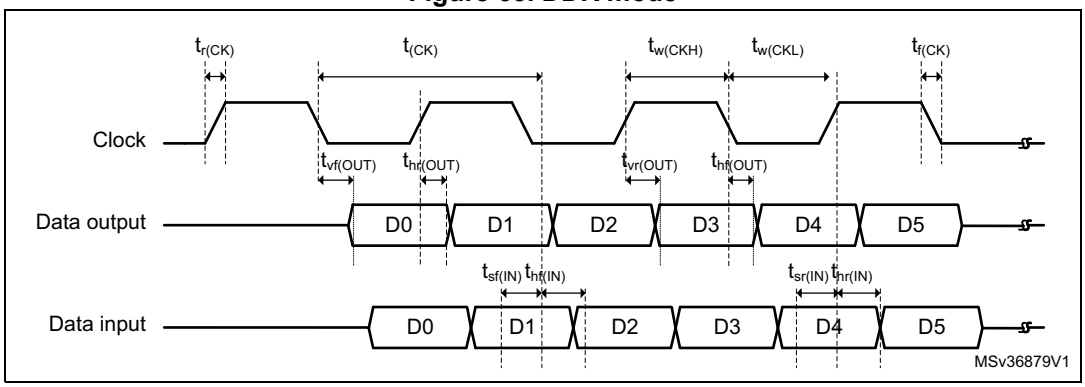


Figure 65. DDR mode



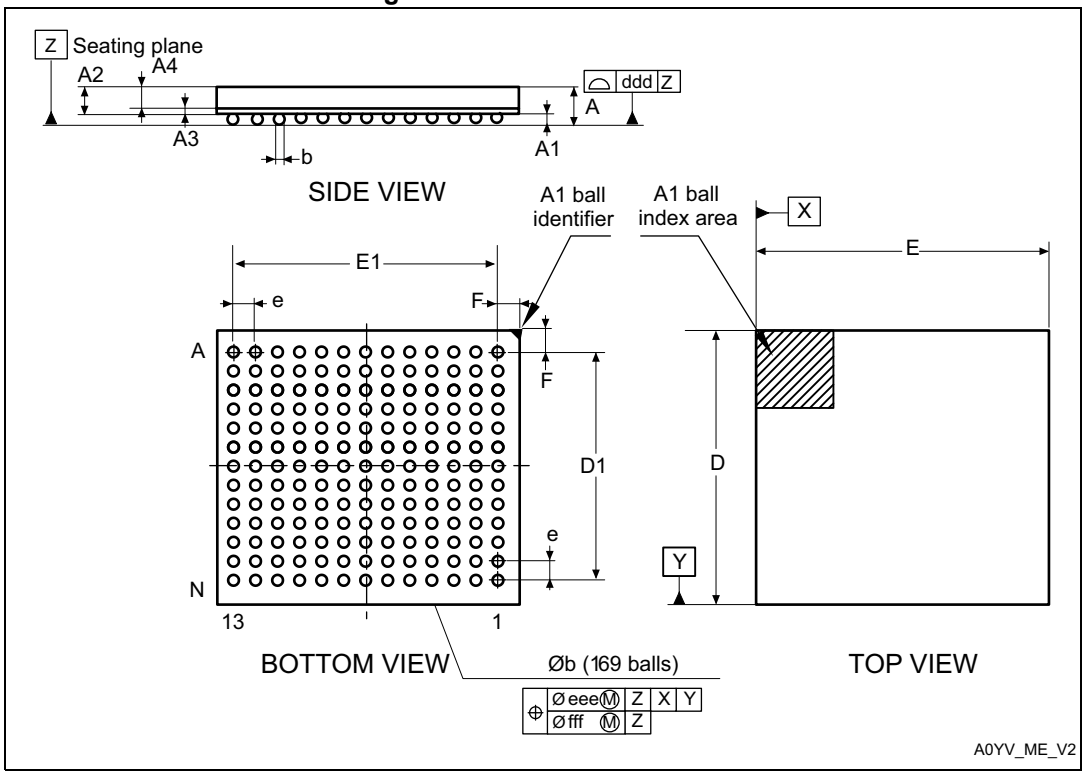
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 UFBGA169 package information

UFBGA169 is a 169-ball, 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 66. UFBGA169 outline



1. Drawing is not to scale.

Table 117. UFBGA169 mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146

Table 117. UFBGA169 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. UFBGA169 recommended footprint

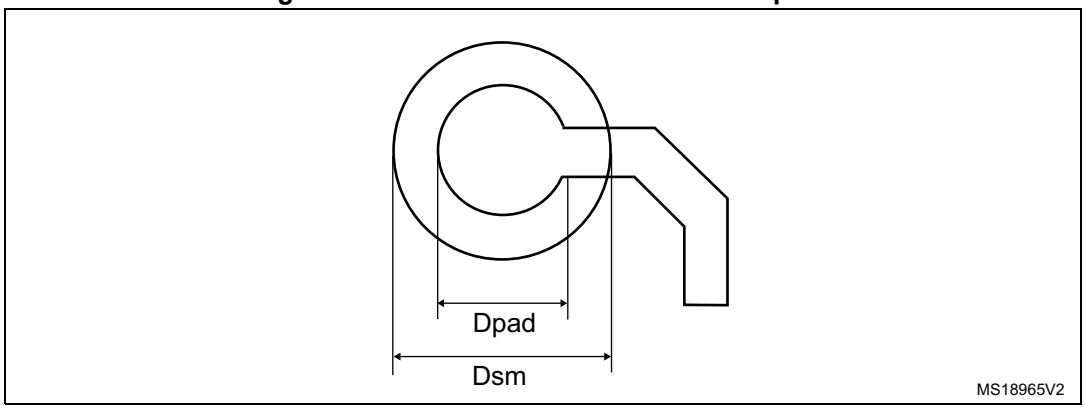


Table 118. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

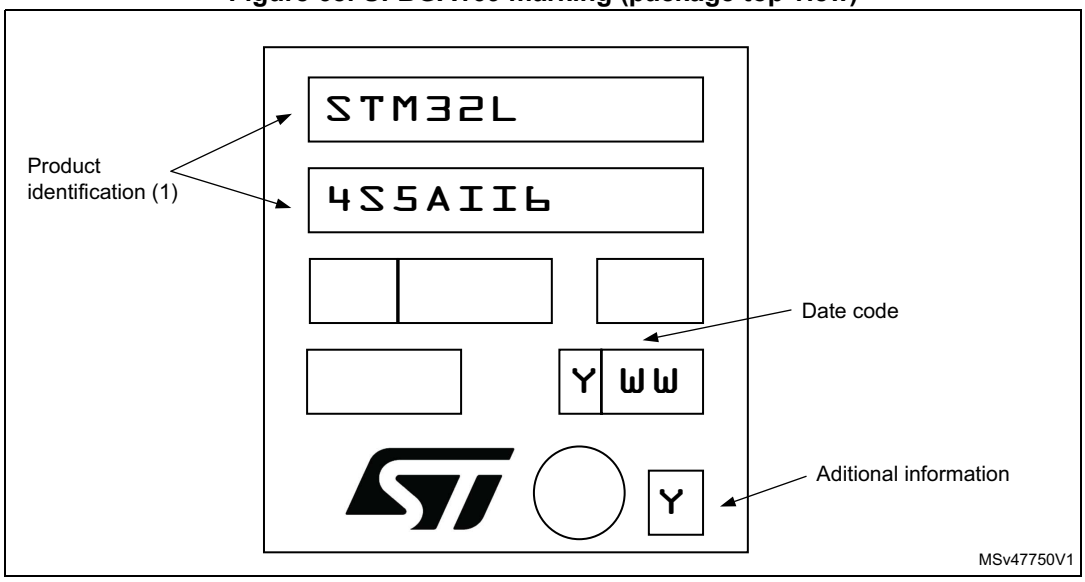
UFBGA169 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 68. UFBGA169 marking (package top view)

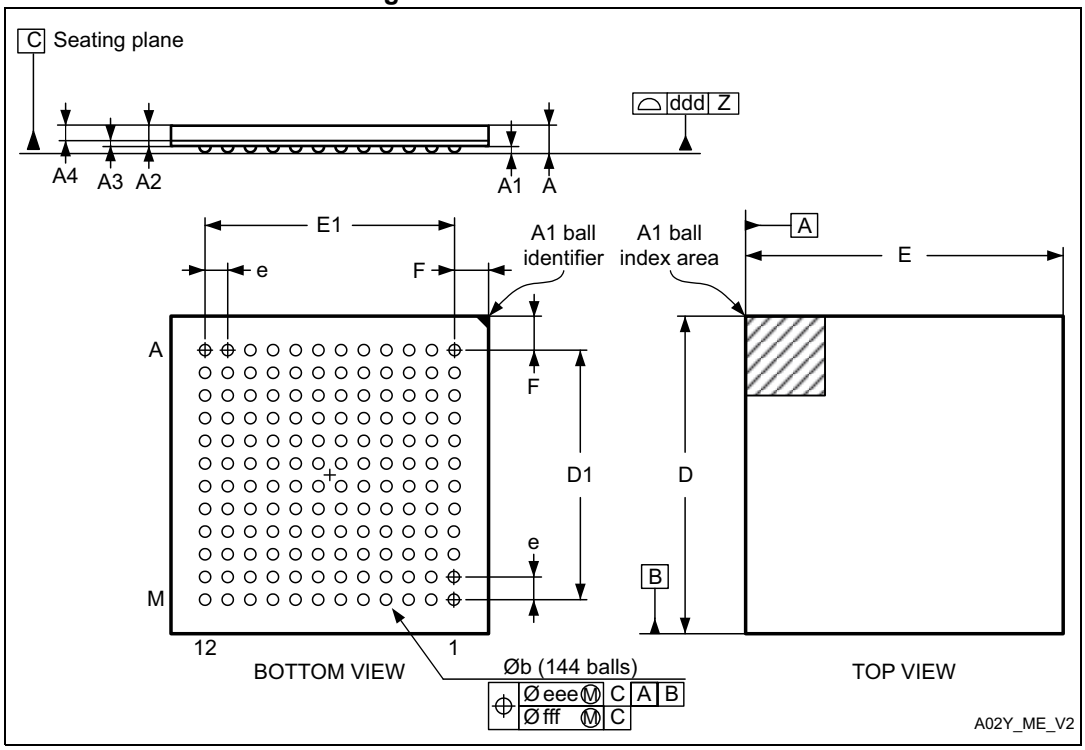


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 UFBGA144 package information

UFBGA144 is a 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package.

Figure 69. UFBGA144 outline



1. Drawing is not to scale.

Table 119. UFBGA144 mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.360	0.400	0.440	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.2736	0.2756	0.2776
D1	8.750	8.800	8.850	0.2343	0.2362	0.2382
E	9.950	10.000	10.050	0.2736	0.2756	0.2776
E1	8.750	8.800	8.850	0.2343	0.2362	0.2382
e	0.750	0.800	0.850	-	0.0197	-
F	0.550	0.600	0.650	0.0177	0.0197	0.0217

Table 119. UFBGA144 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. UFBGA144 recommended footprint

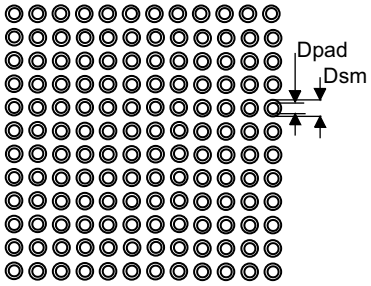


Table 120. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

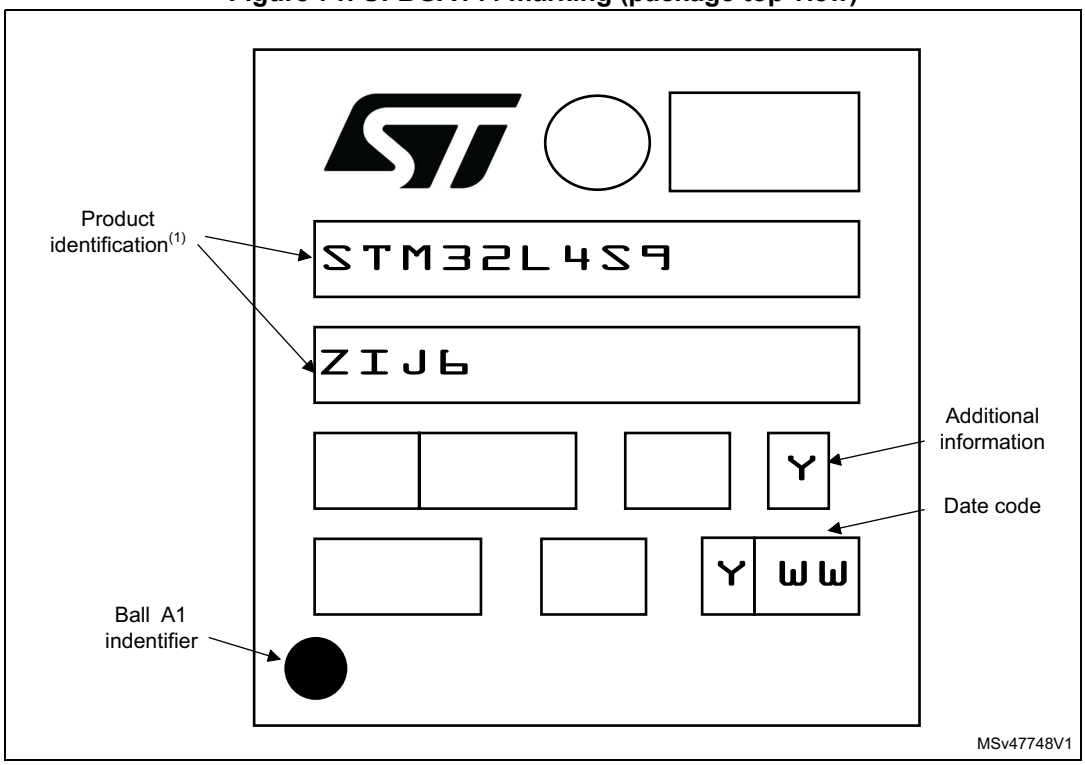
UFBGA144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 71. UFBGA144 marking (package top view)

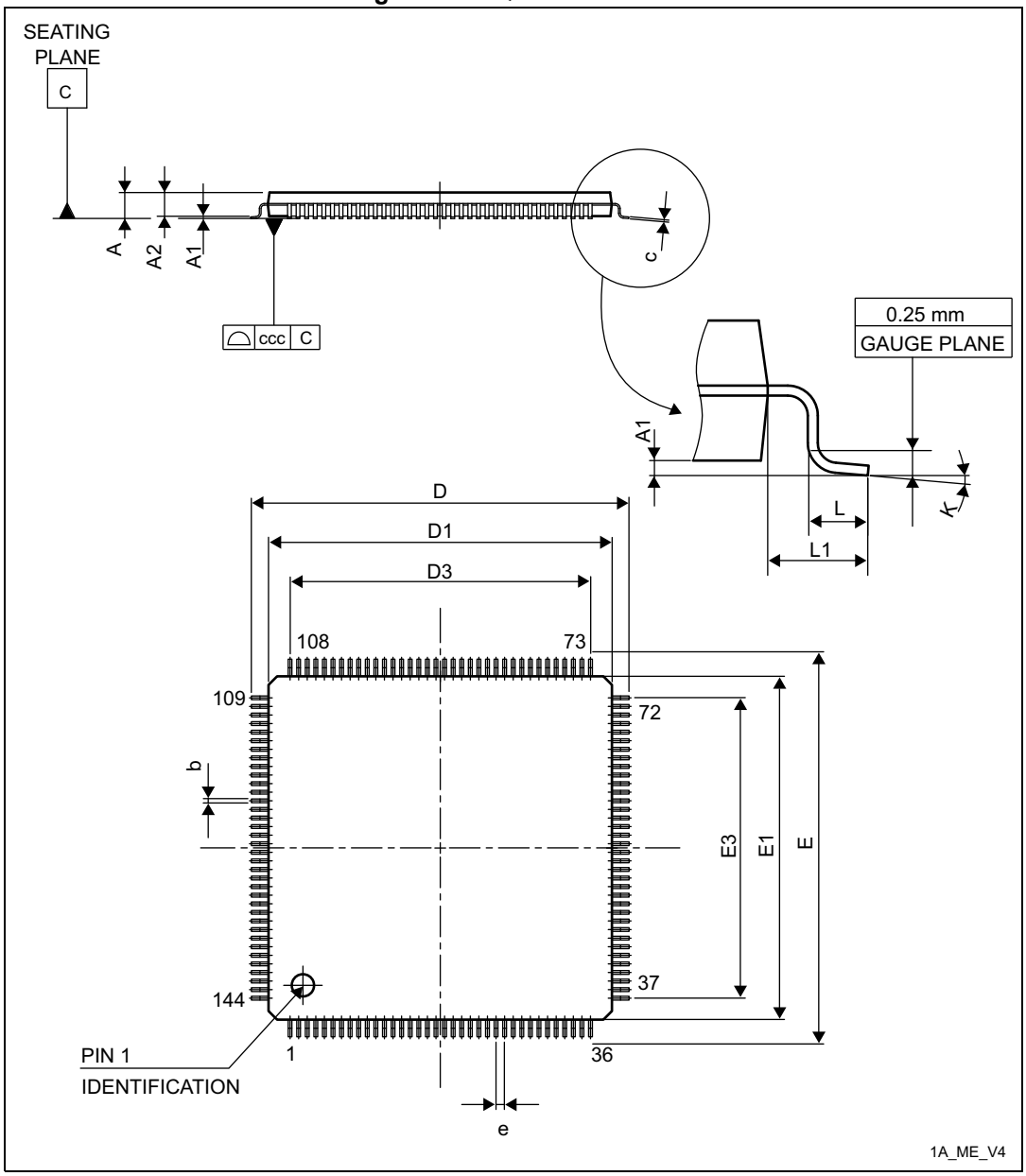


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP144 package information

LQFP144 is a 144-pin, 20 x 20 mm, low-profile quad flat package.

Figure 72. LQFP144 outline



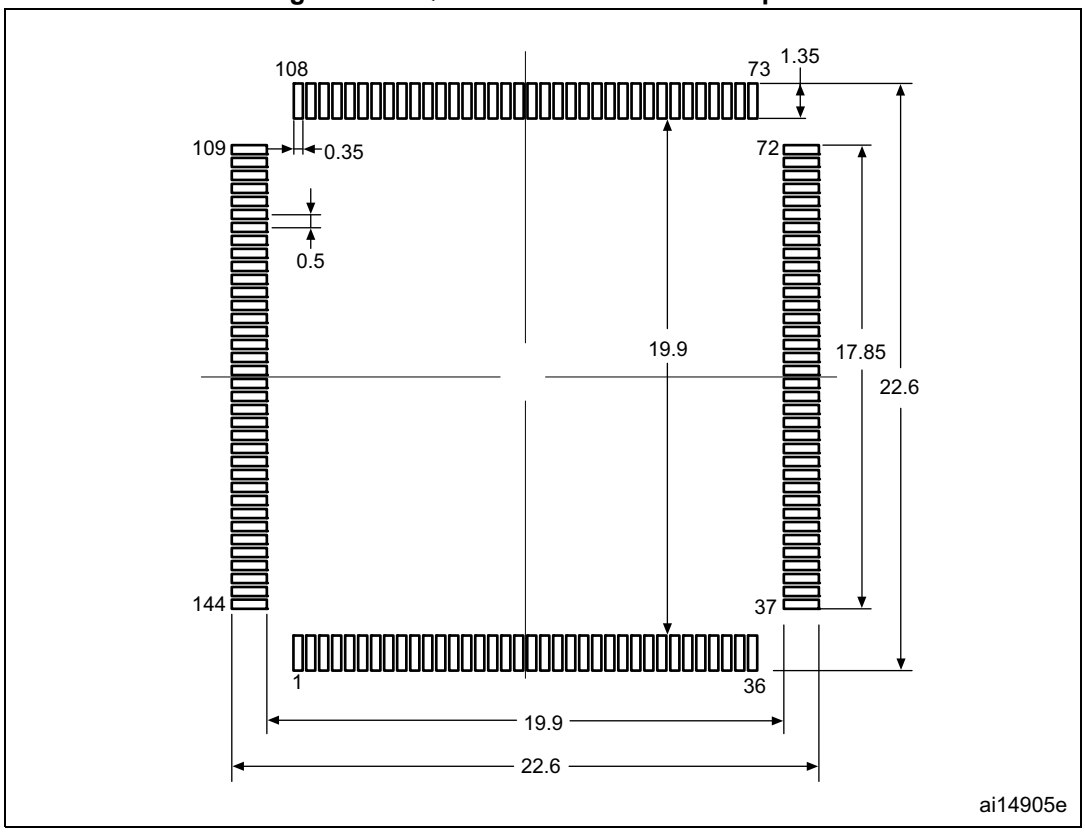
1. Drawing is not to scale.

Table 121. LQFP144 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 73. LQFP144 recommended footprint



1. Dimensions are expressed in millimeters.

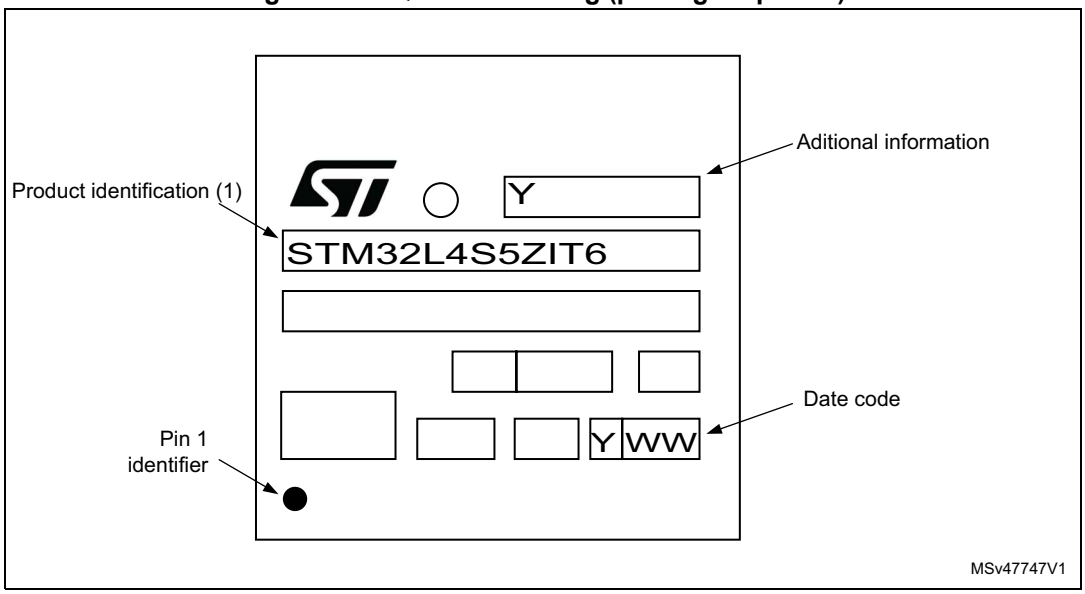
LQFP144 device marking

The following figures gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 74. LQFP144 marking (package top view)

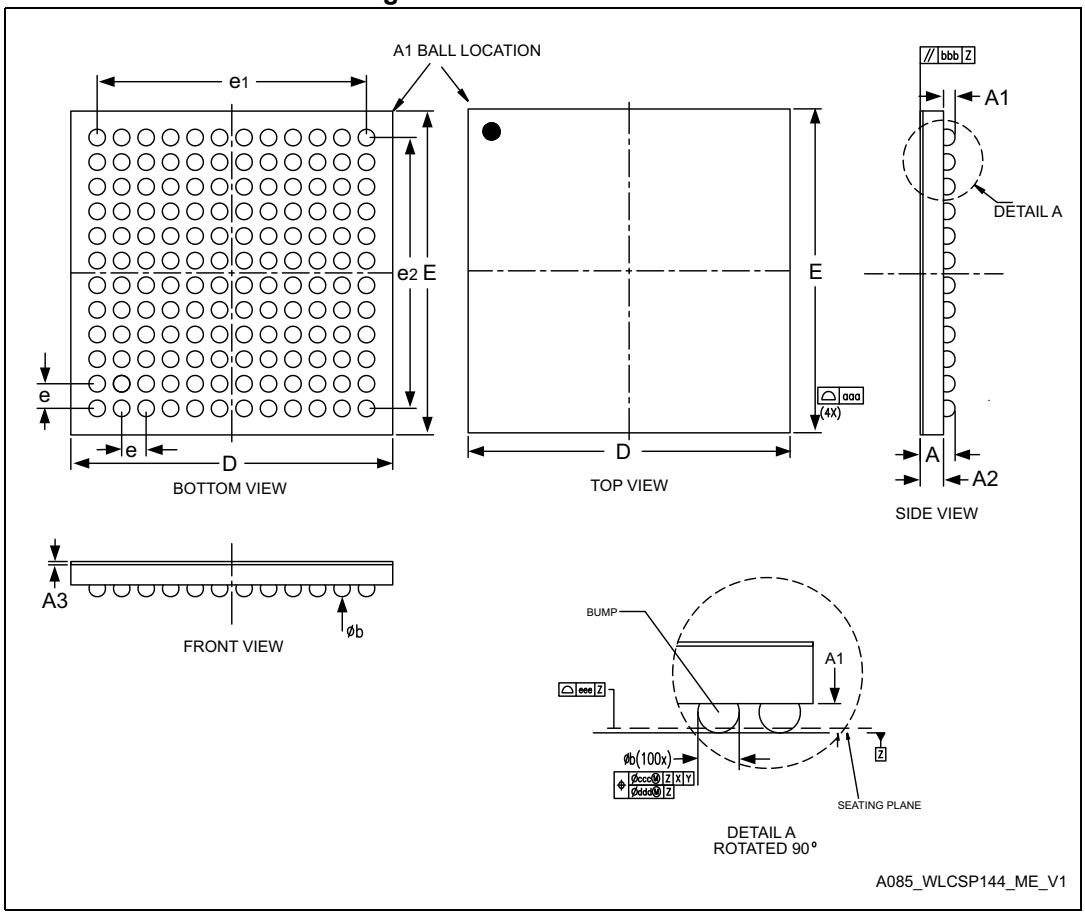


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 WLCSP144 package information

WLCSP144 is a 144-bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale package.

Figure 75. WLCSP144 outline



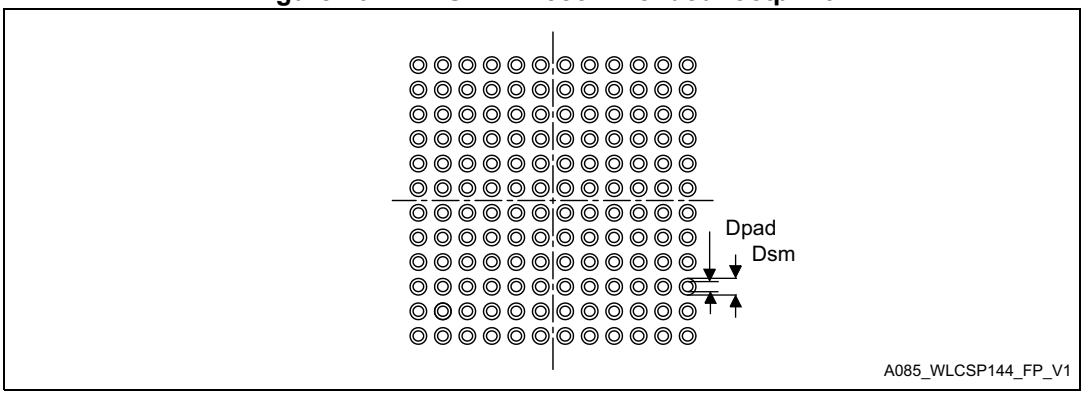
1. Drawing is not to scale.

Table 122. WLCSP144 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.0010	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	5.22	5.24	5.26	0.205	0.206	0.207
E	5.22	5.24	5.26	0.205	0.206	0.207
e	-	0.40	-	-	0.016	-
e1	-	4.40	-	-	0.173	-
e2	-	4.40	-	-	0.173	-
F	-	0.420[3]	-	-	0.0165	-
G	-	0.420[4]	-	-	0.0165	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. A3 value is guaranteed by technology design value.
3. This value is calculated from over value D and e1.
4. This value is calculated from over value E and e2.

Figure 76. WLCSP144 recommended footprint



1. Dimensions are expressed in millimeters.

Table 123. WLCSP144 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

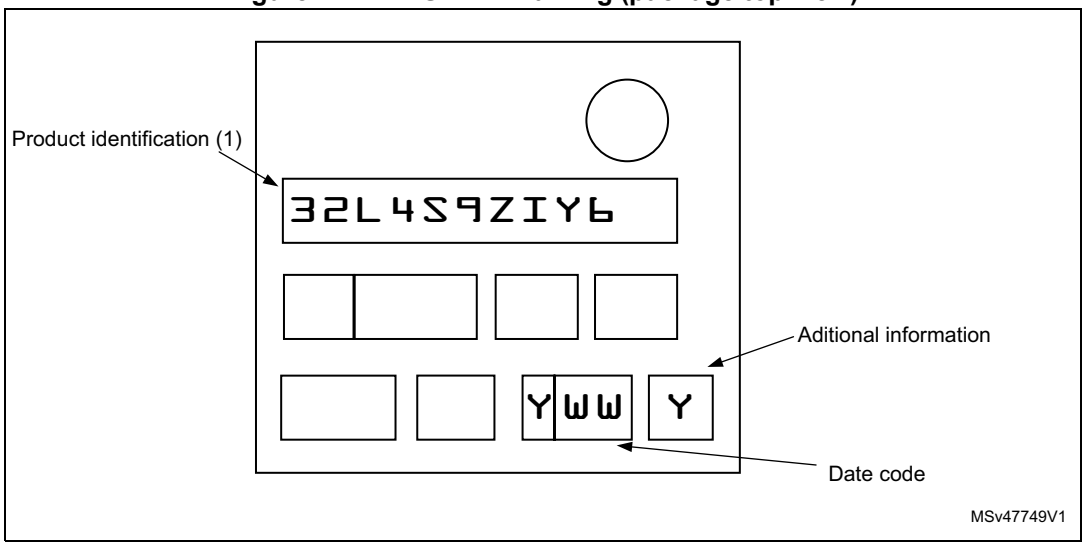
WLCSP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 77. WLCSP144 marking (package top view)

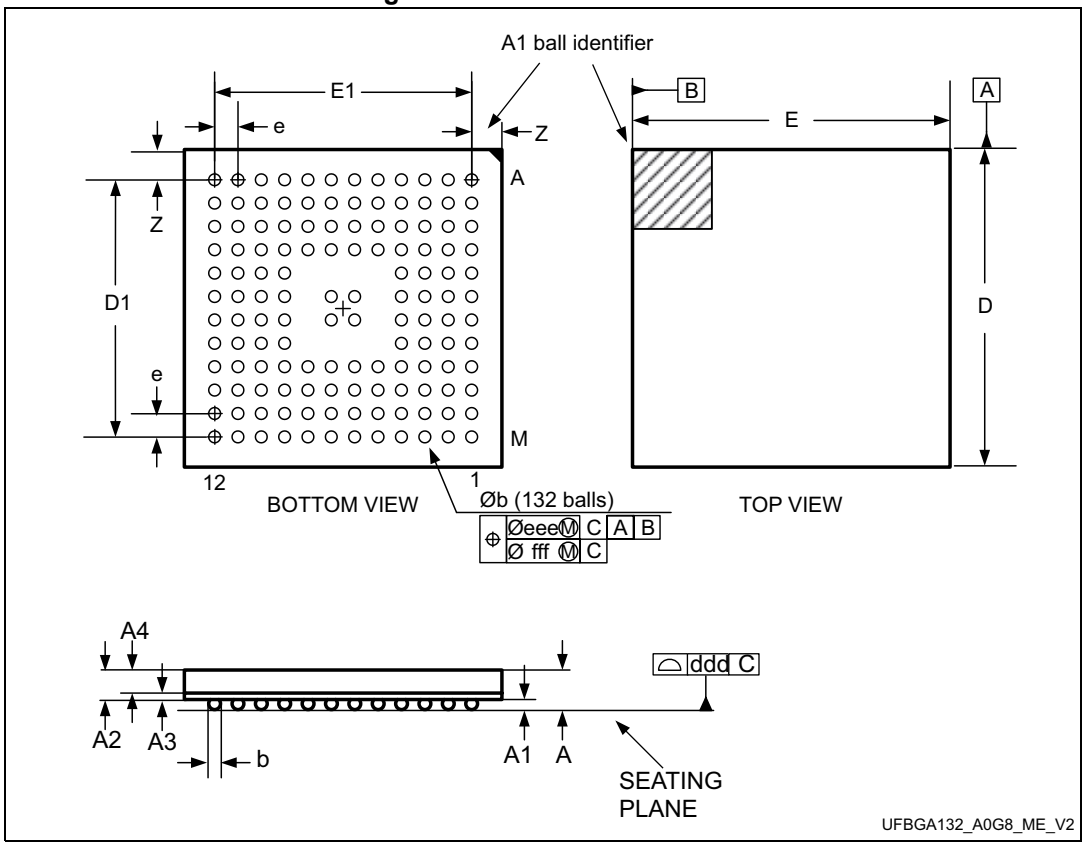


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 UFBGA132 package information

UFBGA132 is a 132-ball, 7 x 7 mm, ultra thin fine pitch ball grid array package.

Figure 78. UFBGA132 outline



1. Drawing is not to scale.

Table 124. UFBGA132 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Table 124. UFBGA132 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 79. UFBGA132 recommended footprint

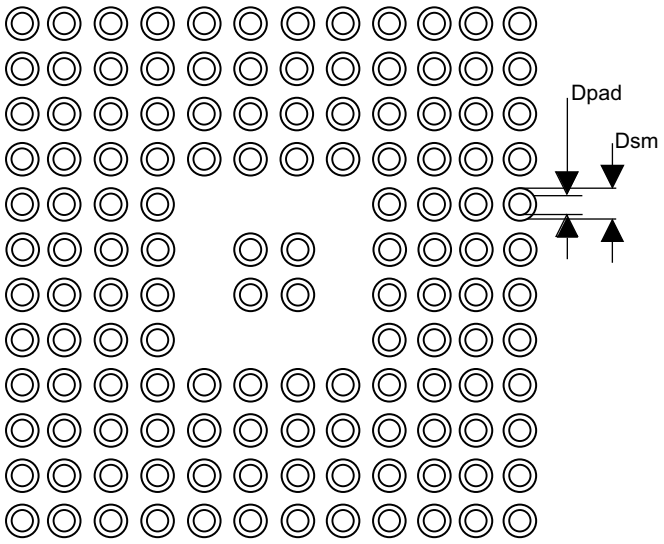


Table 125. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

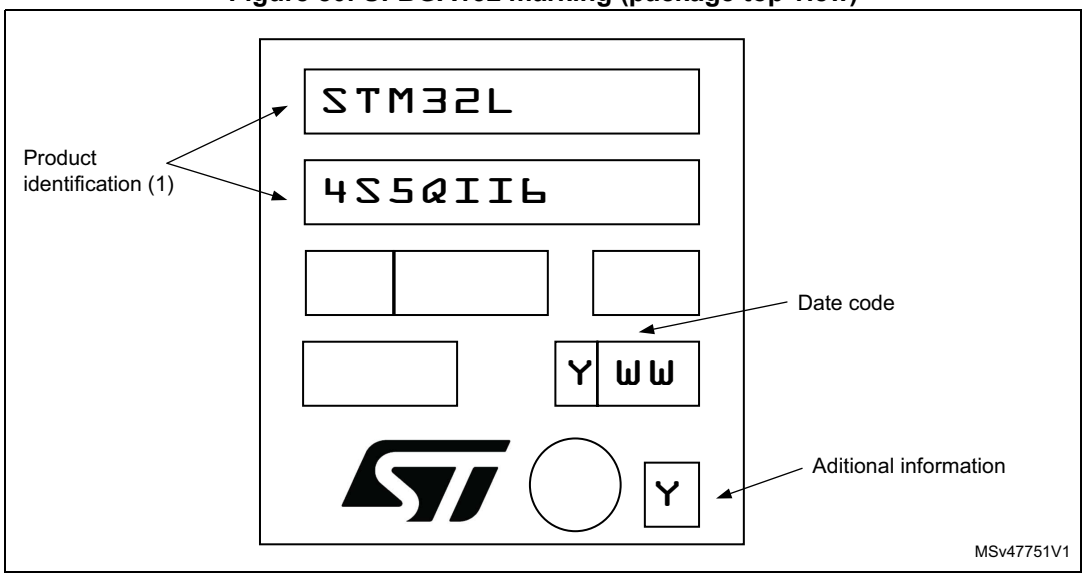
UFBGA132 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 80. UFBGA132 marking (package top view)

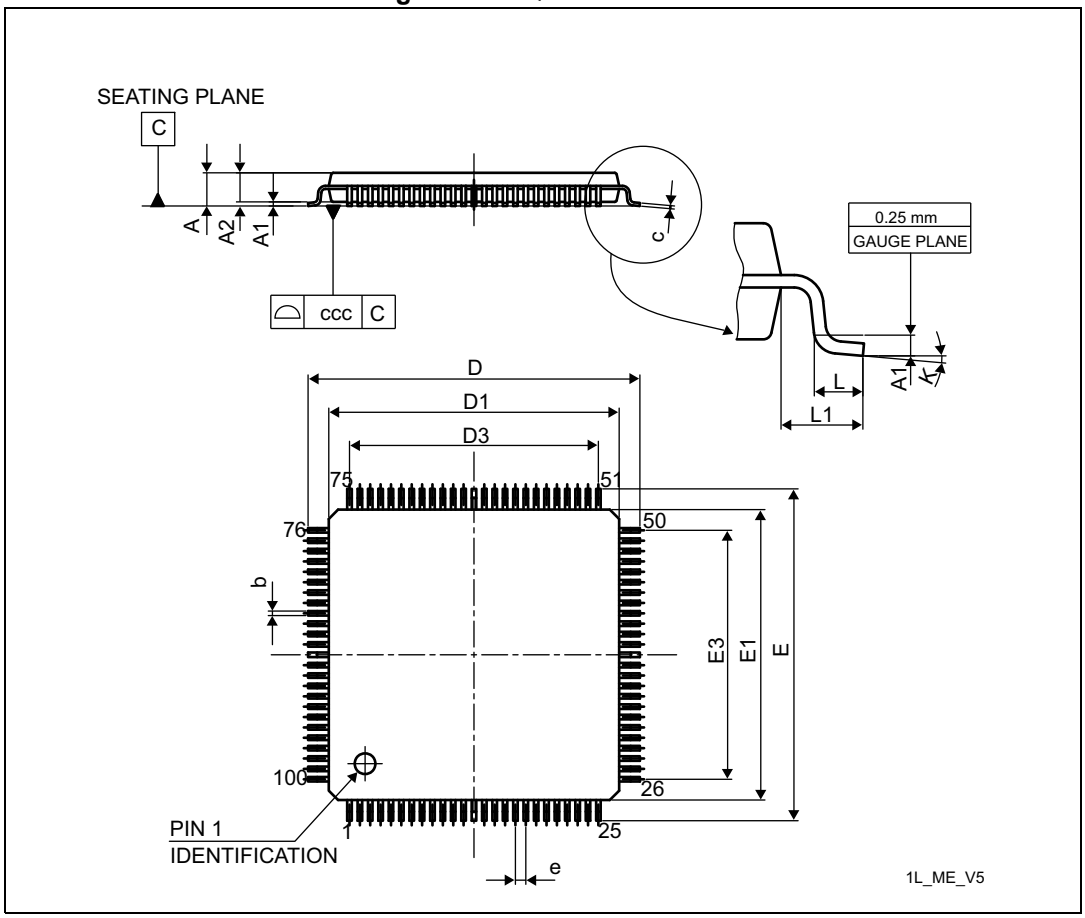


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm, low-profile quad flat package.

Figure 81. LQFP100 outline



1. Drawing is not to scale.

Table 126. LQPF100 mechanical data

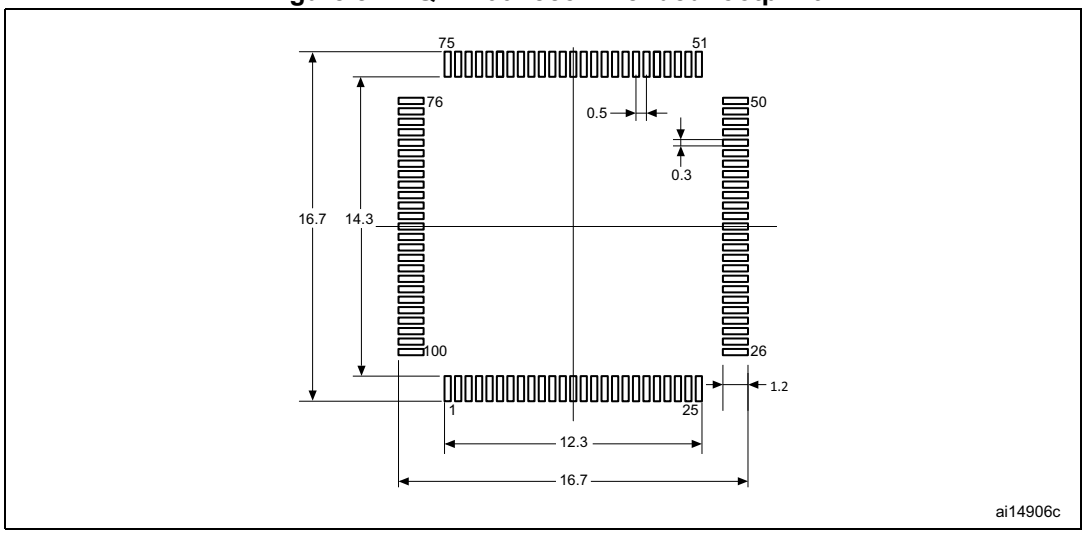
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 126. LQPF100 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 recommended footprint



1. Dimensions are expressed in millimeters.

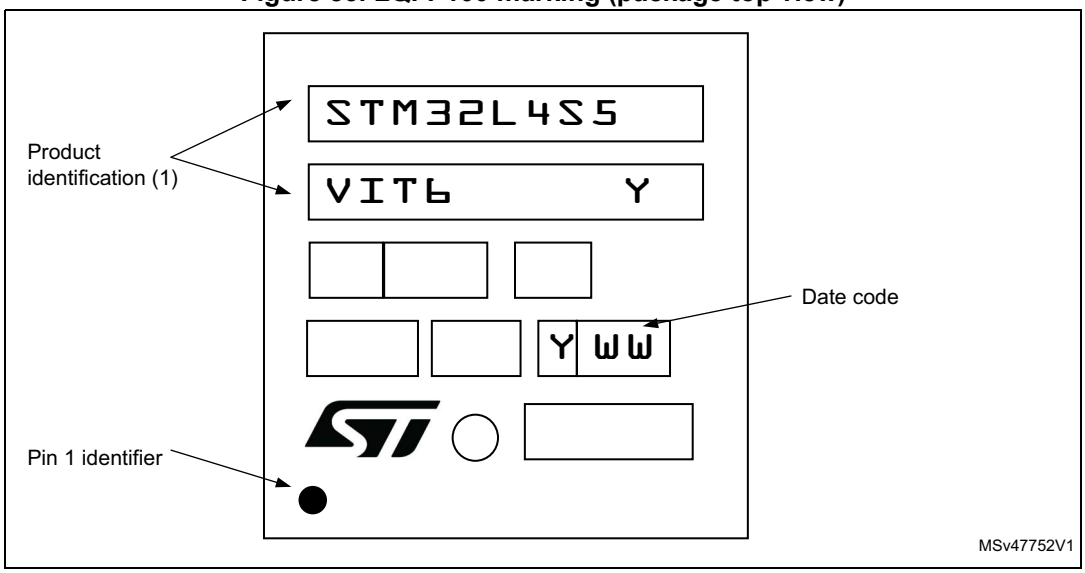
LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 83. LQFP100 marking (package top view)



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 127. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14mm	42	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA144 -10 x 10 mm	53	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7 mm	52	
	Thermal resistance junction-ambient WLCSP144	30.1	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L4Sxxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 127* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 3: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 130-18.774 = 111.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 127* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

8 Ordering information

Table 128. STM32L4Sxxx ordering information scheme

Example: STM32 L 4Sx V I T 6 S TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

4S5 = STM32L4S5xx
4S7 = STM32L4S7xx, LCD-TFT, Chrom-GRC
4S9 = STM32L4S9xx, LCD-TFT Chrom-GRC and DSI Host

Pin count

V = 100 pins
Q = 132 balls
Z = 144 pins/balls
A = 169 balls

Flash memory size

I = 2 Mbytes of Flash memory

Package

T = LQFP
I = UFBGA (7 x 7 mm)
J = UFBGA (10 x 10 mm)
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
3 = Industrial temperature range, -40 to 125 °C (130°C junction)

Option

S = new sawing

Packing

TR = tape and reel
xxx = programmed parts

9 Revision history

Table 129. Document revision history

Date	Revision	Changes
10-Oct-2017	1	Initial release.
28-Nov-2017	2	Added: – *Section 6.3.10: MIPI D-PHY characteristics* – *Section 6.3.11: MIPI D-PHY PLL characteristics* – *Section 6.3.12: MIPI D-PHY regulator characteristics* Updated: – Cover page *Features* (Performance benchmark and Energy benchmark) – *Table 4: STM32L4S5xx modes overview* – *Section 3.12: Clocks and startup* – *Figure 14: STM32L4S5xx WLCSP144 ballout*(1) – *Table 15: STM32L4Sxxx pin definitions*
30-Apr-2018	3	Added: – *Figure 5: Power-up/down sequence* – *Figure 60: OctoSPI HyperBus™ read with double latency* Updated: – *Section 1: Introduction* – *Section 3.10.1: Power supply schemes* – *Table 8: Temperature sensor calibration values* – Values on column “Parameter”’ on *Table :* – Title of *Table 34: Current consumption in Low-power sleep mode, Flash in power-down*
31-Mar-2020	4	Updated: – *Table 2: STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts*. – *Figure 1: STM32L4S5xx, STM32L4S7xx and STM32L4S9xx block diagram*. – *Section 5: Memory mapping* removing tables and figure, which are put in the reference manual. – *Table 18: Voltage characteristics*. – *Table 66: I/O static characteristics* note 4. – *Table 80: VREFBUF characteristics*. – *Table 112: OctoSPI characteristics in DTR mode (with DQS)/Octal and HyperBus™*. – *Figure 58: OctoSPI HyperBus™ clock*., *Figure 59: OctoSPI HyperBus™ read*, *Figure 60: OctoSPI HyperBus™ read with double latency*, *Figure 61: OctoSPI HyperBus™ write* removing any reference to CK#. – *Table 128: STM32L4Sxxx ordering information scheme*. – *Section 7: Package information*. – *Section 8: Ordering information*.

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STM32L4S5ZIT6 STM32L4S9ZIJ6 STM32L4S9ZIT6 STM32L4S5AII6 STM32L4S7ZIT6 STM32L4S9AII6 STM32L4S5QII6 STM32L4S7VIT6 STM32L4S5ZIY6TR STM32L4S5VIT6 STM32L4S7AII6 STM32L4S9VIT6 STM32L4S5QII3P STM32L4S9ZIY6TR STM32L4S9ZIJ6TR