Wei Minyi

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Education

2020.09-2024.06

UESTC (Bachelor Degree) **Microelectronics**

Score Ranking: top 30%

GPA: 3.6

Major Courses: Microelectronic Systems (99); Embedded Processors (95); Semiconductor Physics (93); Team Design Project (92); Electronic Devices (89); Circuit Analysis and Design (86); Integrated Circuit Design

Academic

2023.09-2024.06

The implementation of a multi-phase DPD on FPGA **designer**

The performance of a digital pre-distortion (DPD) was validated using a closed-loop direct learning structure on an FPGA. The DPD employed a memory polynomial model estimated through the least squares method to alleviate the inherent nonlinearities and memory effects in the PA. The effectiveness of the implemented DPD algorithm was confirmed through testing on the FPGA platform. The results indicated a significant improvement in the ACPR by more than 25 dBc under operating bandwidths of 20 MHz and 40 MHz.

2023.03-2023.06

Comprehensive Experiment of Modern Electronic Techno.. **Experimenter**

In this experiment, an in-depth exploration of the circuit design and layout implementation of operational amplifiers was undertaken. The core objective of the experiment was to utilize Empyrean to perform parameter simulation and layout design of a two-stage operational amplifier circuit, ensuring that the design met specific technical specifications. The experiment was divided into four key parts, each building upon the previous one, advancing step by step.

Firstly, the characteristics of NMOS were analyzed using Empyrean, and an NMOS bias circuit was constructed. Simulations were conducted to obtain the IV characteristic curves under various process corners. Following that, a current source loaded common source amplifier circuit was designed. By adjusting the size ratio of NMOS and PMOS, an amplification of over 100 times was achieved, and simulations were carried out across five process corners to ensure the robustness.

2022.09-2023.06

CPU Design and FPGA Implementation Based on RISC-V **Designer**

This was a challenging course aimed at further improving my Verilog HDL skills, with the entire process carried out in Vivado. We used the RISC-V instruction set to build a basic CPU, employing a five-stage pipeline architecture to enhance the overall efficiency of the CPU. Finally, I wrote a 'running LED program' that successfully ran on the FPGA.

Award

2022.11

Gold award of China College Students' Innovation Competition

Skill/Language

Verilog :
Competent

Vivado :
Competent

Linux :
Familiar

C :
Competent

Empyrean :
Familiar