# SIT111 - Task 3.1P Implement the Full Adder in HDL

## Overview

Adders are important not only in computers, but also in many types of digital systems in which numerical data are processed.

The Full Adder accepts two input bits and an input carry and generates a sum output and an output carry. The main difference between a full adder and a half adder is that the full adder accepts an input carry.

Your task is to implement a Full Adder using Hardware Description Language (HDL).

### Task requirements

a. Go through week 3 class materials on Google Classroom & complete the practice problems in week 3

b. Read the task instructions

## Task Instructions

1. Using your knowledge gained from the learning materials and learning sessions in week 3, write and program to implement the Full Adder.

   You may refer to the truth table and logic diagram of the Full Adder discussed in the active learning session.

2. Note that you can only use the following chips: AND, OR, NOT, NAND, XOR, NOR, Mux, Half Adder.
3. Use the provided test scripts in task resources to test your implementation.
4. Upload the script to the Hardware Simulator tool.
5. Run and validate your HDL program with the test script.
6. Upload Your HDL program (a .hdl file) and a document (up to 1 page) describing how you arrived at the solution to Google Classroom.

## Reference

Nisan, Noam, and Shimon Schocken. *The Elements of Computing Systems : Building a Modern Computer from First Principles* MIT Press, 2005

Floyd, L., Thomas. *Digital Fundamentals*. Prentice-Hall International, 2003