SIT111 - Task 2.1P Implement and Test the Mux in HDL

Overview

A simple multiplexor (Mux) is a three-input gate that uses one of the inputs, called 'selection bit', to select and output one of the other two inputs, called 'data bits'. In this task, you are given the design of a Mux using a collection of primitive Nand gates. Nand gate is called a 'universal gate' because it can be used to build all other gates.

Your task is to implement the given design using Hardware Description Language (HDL).

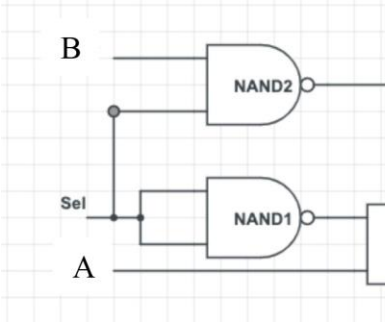
Task requirements

a. Go through week 2 class materials on Google Classroom & complete the practice problems.

b. Read the task instructions

Task Instructions

1. Using your knowledge gained from the learning materials and learning sessions in week 2, write an HDL program to implement the given Mux design in Figure 1 below. The truth table is also given below.



Sel	A	B	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Figure 1: Diagram of Mux designed from NAND gates and Truth Table

2. Upload the script to the Hardware Simulator tool that is provided.
3. Run and validate your HDL program with the test scripts provided in this task, to test your implementation. (refer to the learning materials on how to do this)
4. Your submission is the HDL program (a .hdl file).

Reference

Nisan, Noam, and Shimon Schocken. The *Elements of Computing Systems : Building a Modern Computer from First Principles* MIT Press, 2005.