1.6

	clock rate	A	B	C	D
P_1	2.5	1	2	3	3
P_2	3	2	2	2	2

(a) 10^6 Instruction divided

⇒ A: $0.1 \times 10^6 = 10^5$

B: $0.2 \times 10^6 = 2 \times 10^5$

C: $0.5 \times 10^6 = 5 \times 10^5$

D: $0.2 \times 10^6 = 2 \times 10^5$

$$\text{시간} = \frac{\text{Instruction 개수} \times \text{CPI}}{\text{clock rate}}$$

$$P1: \frac{(10^5 + 2 \cdot 2 \cdot 10^5 + 3 \cdot 5 \cdot 10^5 + 3 \cdot 2 \cdot 10^5)}{2.5 \times 10^9}$$

$$= 0.4 \times 10^{-4}\,s$$

$$P2: \frac{(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)}{3 \times 10^9}$$

$$= 6.66 \times 10^{-4}\,s$$

∴ P2 is faster than P1

b)

$$CPI = \frac{\text{time} \times \text{clock rate}}{\text{instruction no}}$$

$$CPI \text{ of } P1 = \frac{10.4 \times 10^{-4} \times 2.5 \times 10^9}{10^6}$$

$$= \frac{10.4 \times 2.5}{10} = 2.6$$

$$CPI \text{ of } P2 = \frac{6.66 \times 10^{-4} \times 3 \times 10^9}{10^6}$$

$$= \frac{6.66 \times 3}{10} = 1.998$$

c)

Clock Cycles of P1

$$= 10^5 + 2 \cdot 2 \cdot 10^5 + 3 \cdot 5 \cdot 10^5 + 3 \cdot 2 \cdot 10^5$$

$$= 26 \cdot 10^5$$

Clock Cycles of P2

$$= 2 \cdot 10^5 + 2 \cdot 2 \cdot 10^5 + 2 \cdot 5 \cdot 10^5 + 2 \cdot 2 \cdot 10^5$$

$$= 20 \cdot 10^5$$

1.8.1

P power $= \frac{1}{2} \cdot$ Capacitive load $\times$ Votage$^2 \times$ Frequency switched

$$C = \frac{2 \cdot P}{V^2 \cdot F}$$

(pentium 4)

$$C = \frac{2 \cdot 90}{(1.25)^2 \cdot 3.6 \times 10^9} = 3.2 \times 10^{-8}$$

(Core i5 Ivy Bridge)

$$C = \frac{2.40}{(0.9)^2 \cdot 3.4 \cdot 10^9} \simeq 2.9 \times 10^{-8}$$

1.8.2

(pentium 4)

$10/100 \times 100(\%) = 10\%$

((ore i5 Ivy Bridge)

$30/70 \times 100(\%) \simeq 42.86\%$

1.8.3

(pentium 4)

$10 = 1.25 \times \underline{I}$ (I = leakage current)

$\therefore I = 8$

$$(DP_{new} + SP_{new}) / (DP_{old} + SP_{old}) = 0.9$$

$$\Leftrightarrow \frac{DP_{new} + SP_{new}}{100} = 0.9, \quad DP_{new} + SP_{new} = 90$$

$$DP_{new} = \frac{1}{2} C V_{new}^2 F = \frac{1}{2} \times 3.2 \times 10^{-8} \times 3.6 \times 10^9 \times V_{new}^2$$

$$= 57.6 \times V_{new}^2$$

$$SP_{new} = V_{new} \times 8$$

$$\therefore 57.6 V_{new}^2 + 8 V_{new} = 90$$

$$\therefore V_{new} \simeq 1.18 V$$

(Core I5 IVY Bridge)

$$30 = 0.9\,I, \quad I = \frac{100}{3}$$

$$DP_{new} + SP_{new} = 63$$

$$DP_{new} = \frac{1}{2} \times 2.9 \times 10^{-8} \times V_{new}^{2} \times 3.4 \times 10^{9}$$

$$= 49.3\,V_{new}^{2}$$

$$SP_{new} = V_{new} \times \frac{100}{3}$$

$$\therefore 49.3\,V_{new}^{2} + \frac{100}{3} V_{new} = 63$$

$$\therefore V_{new} \simeq 0.84\,V$$

1.11.1

$$CPI = \text{clock rate} \times CPU\ \text{time} / IC \quad (IC = \text{instruction counts})$$

$$\text{clock rate} = 1/\text{clock cycle time} = 3\text{GHz}$$

$$\therefore CPI = 3 \cdot 10^9 \times 750 / 2.389 \times 10^{12}$$

$$\simeq 0.94$$

1.11.2

$$SPEC\ ratio = \frac{\text{reference time}}{\text{execution time}}$$

$$= \frac{9650}{750} \simeq 12.87$$

1.11.4

$$CPU\ time = \frac{IC \cdot CPI}{\text{clock rate}}$$

IC↑ 10%, CPI↑ 5%

$$CPU\ time_{new} = (1.1 \times 1.05) \frac{IC \cdot CPI}{\text{clock rate}}$$

$$= \frac{IC \cdot CPI}{\text{clock rate}} \times 1.155, \therefore 15.5\%\ \text{증가}$$

1.11.6

clock rate → 4GHz

num of Instructions → 15% 감소

Execution time → 700 s

spec ratio new → 13.7

$$CPI_{new} = 100 \times 4 \times 10^9 / 2.389 \times 10^{12} \times 0.85$$

$$\simeq 1.38$$

1.12.1

	clock rate	CPI	execution
P1	4GHz	0.9	5×10^9
P2	3GHz	0.75	1×10^9

$$\text{CPU time} = \frac{\text{IC} \cdot \text{CPI}}{\text{clock rate}}$$

$$\text{time}(P1) = \frac{5\times10^9 \times 0.9}{4\times10^9} = 1.125\text{s}$$

$$\text{time}(P2) = \frac{10^9 \times 0.75}{3\times10^9} = 0.25\text{s}$$

clock rate : $P1 > P2$

performance : $P1 < P2$

∴ It is false.

1.12.2

$$time(p1) = \frac{10^9 \times 0.9}{4 \times 10^9} = 0.225$$

$$time(p2) = 0.225 = \frac{n \times 0.75}{3 \times 10^9}$$

$$n = 9 \times 10^8$$

∴ 같은 시간에 p2는 9×10^8 만큼의 instructions 실행 가능.

1.12.3

$$MIPS = \frac{Clock\ rate}{CPI \times 10^6}$$

$$MIPS(p1) = \frac{4 \times 10^9}{0.9 \times 10^6} \approx 4.44 \times 10^3$$

$$MIPS(p2) = \frac{3 \times 10^9}{0.75 \times 10^6} = 4 \times 10^3$$

MIPS : p1 > p2

performance : p1 < p2

(1.21.1)

∴ it is false.

1.12.4

$$MFLOPS = \frac{\text{No. FP operations}}{\text{execution time} \times 10^6}$$

$$MFLOPS(P1) = \frac{0.4 \times 5 \times 10^9}{1.125 \times 10^6} \simeq 1.78 \times 10^3$$

$$MFLOPS(P2) = \frac{0.4 \times 10^9}{0.25 \times 10^6} = 1.6 \times 10^3$$

MFLOPS : P1 > P2

performance : P1 < P2

1.13.1

running a program : 250s

FP instructions : 10s

L/S " : 85s

Branch " : 40s

int " : 55s

time(FP) = 15 x 0.8 = 56s

time(new) = 56 + 85 + 40 + 55 = 236s

$14/250 \times 100(\%) = 5.6\%$

∴ total time reduced 5.6%

1.13.2

time(total) = 250 x 0.8 = 200 s

time(FP) + time(L/S) + time(branch)

= 40 + 85 + 40 = 165

$\frac{55-5}{55} \times 100 \simeq 90.9$ ∴ INT operation → 90.9% reduced

1.C3.3

time(total) = 250 · 0.8 = 200 s

time(FP) + time(LIS) + time(int)

= 10 + 85 + 55 = 210 s > 200 s

∴ It can't reduce total time to 80% by reducing only the time for branch instructions.

2.4

array A and B.

addi $t2, $t0, 4 ⇒ index 1증가

lw $t0, 0($t2) ⇒ $t0에 A[1]

add $t0, $t0, $s0

⇒ $t0 = A[f] + A[f+1]

sw $t0, 0($t1) ⇒ B[g] = $t0

---

in C code

B[g] = A[f] + A[f+1];

2.15

sw $t1, 32($t2)

⇒ I-format,

101011 10010 01001 0000 0000 0010 00

A D 4 9 0 0 2 0

⇒ 0xAD490020

2.24

0x20000000

= 0010 0000 0000 0000 0000 0000

0000 0000

0x40000000

= 0100 0000 0000 0000 0000 0000

0000 0000

jump는 pc에서 26bit의 LSB만 변경

가능하므로 0x20000000에서 0x40000000

으로 j는 사용하여 변경할 수 없다.

branch는 offset으로 16bits를 가질 수 있는데

0x20000000을 16bits로 표현이 되지 않는다.

∴ j와 beq 둘 다 0x4000 0000으로

pc를 옮기도록 불가능하다.

2.25.1

loop는 label로 레지스터가 아닌 constant로 볼 수 있다.

∴ I-format이 적절하다.

2.25.2

if(R[rs] > 0) R[rs] = R[rs] - 1

PC = PC + 4 + BranchAddr.

⇓

addi $t2, $t2, -1

beq $t2, $0, loop