5.3.1

Cache block size = $2^{\text{offset bits}} = 2^5$ bytes

in words, 2^5 bytes = 8 words

5.3.2

entries = $2^{\text{index bits}} = 2^5 = 32$

5.3.3

total bits = $2^{\text{index}} \times$ (block size + tag size + valid field size)

$= 2^5 \times (256 + 22 + 1)$

$= 32$ blocks $\times$ 279 bits

data storage size = $2^{\text{index}} \times$ block size

$= 32$ blocks $\times$ 256 bits

ratio = $279 / 256 \approx 1.0898$

5.3.4

Address	binary	Hit / Miss	Replacement
0	0000 0000 0000 0000	Miss	X
4	0000 0000 0000 0100	Hit	X
16	0000 0010 0001 0000	Hit	X.
132	0000 0010 0001 0100	Miss	X
232	0000 0011 1010 1000	Miss	X
160	0000 0010 1010 0000	Miss	X
1024	0100 0000 0000 0000	Miss	O
30	0000 0001 0001 1110	Miss	O
140	0000 0010 0001 1100	Hit	X
3100	0000 1100 0011 1100	Miss	O
180	0000 0010 1101 0100	Hit	X
2180	0000 1000 1000 0100	Miss	O

- block (index 0) : 3번
- block (index 4) : 1번

⇒ 2개의 block에서 총 4번의 replacements가 있었다.

5.3.5

Hit ratio = num of hits / num of references

= 4/12 ≈ 0.33

5.3.6

<Index, tag, data> 3

Index	tag	data (offset)
0	3	mem[3100 - 28] ⇒ mem[3072]
4	2	mem[2180 - 4] ⇒ mem[2176]
5	0	mem[160 - 0] ⇒ mem[160]
7	0	mem[232 - 8] ⇒ mem[226]

∴

$<00000_2, 0011_2,$ mem[3072] ~ mem[3103]>

$<00100_2, 0010_2,$ mem[2176] ~ mem[2207]>

$<00101_2, 0000_2,$ mem[160] ~ mem[192]>

$<00111_2, 0000_2,$ mem[224] ~ mem[255]>

§.6.1

clock rate = 1/cycle time.

L_1's hit time for P1 = 1/0.66ns ≈ 1.5/GHz

L_1's hit time for P2 = 1/0.90ns ≈ 1.11GHz

§.6.2

AMAT = Time for a hit + Miss rate × Miss penalty.

AMAT for P1 = 0.66ns + (8.0% × 10ns)

= 0.66 + (0.08 × 10)

= 0.66 + 5.6

= 6.26ns

AMAT for P2 = 0.90ns + (6.0% × 10ns)

= 0.90 + (0.06 × 10)

= 0.90 + 4.2

= 5.1ns

5.6.3

(P1)

miss penalty = 110 / 0.66 ≈ 167 cycles.

miss cycles per Instructions

I-cache : 0.08 × 167 = 8.56

D-cache : 0.08 × 0.36 × 167 = 3.0816

∴ total CPI of P1 = 1 + 8.56 + 3.0816 = 12.6416 Cycles

(P2)

miss penalty = 110 / 0.9 ≈ 118 cycles

miss cycles per Instructions

I-cache : 0.06 × 118 = 4.68

D-cache : 0.06 × 0.36 × 118 = 1.6848

∴ total CPI of P2 = 1 + 4.68 + 1.6848 = 7.3648 Cycles

∴ P2 is faster than P1.

5.6.4

AMAT = Time for a hit + Miss rate x Miss penalty

AMAT with L2 = (L1 hit time) +

(L1 miss rate) x ((L2 hit time) +

(L2 miss rate) x (L2 miss penalty))

(p1)

AMAT with L2 = 0.66ns + 0.08 x (5.62ns +

0.95 x 100)

= 0.66 + 0.08 x (5.62 + 66.5)

= 0.66 + 0.08 x 72.12

= 0.16 + 5.7696

= 6.4296ns

(cycle 단위 계산)

AMAT with L2 = 0.66 x (1 + 0.08 x (9 + 0.95 x 100))

= 0.66 x 9.852 = 6.5023ns

∴ AMAT worse with L2 cache.

5.6.5

(1)

total CPI : $CPI_{base} + CPI_{I\text{-}cache} + CPI_{D\text{-}cache}$

$= 1.0 + 0.08 \times (9 + 0.95 \times 10^{n}) + 0.36 \times$

$0.08 \times (9 + 0.95 \times 10^{n})$

$= 1.0 + 8.852 + 3.186^{n}2$

$= 13.038^{n}2$

5.6.6

(P1)

AMAT = 6.5023 ns

(P2)

AMAT = 0.90 + (0.06 × 10) = 5.1 ns

∴ P2 is faster than P1

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to match, make P1 with L_2 cache faster.

⇒ reduce miss rate.

0.66 × (1 + miss rate × (9 + 0.95 × 100)) = 5.1

$$\text{miss rate} = \frac{(5.1/0.66) - 1}{9 + 0.95 \times 100} \simeq \frac{6.73}{110.65} \simeq 0.06$$

∴ L1 miss rate for P1 should be reduced to 6 %.