Comparative Performance Evaluation of Orthogonal-Signal-Generators-Based Single-Phase PLL Algorithms—A Survey

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***Abstract*—The orthogonal-signal-generator-based phase-locked loops (OSG-PLLs) are among the most popular single-phase PLLs within the areas of power electronics and power systems, mainly because they are often easy to be implemented and offer a robust performance against the grid disturbances. The main aim of this paper is to present a survey of the comparative performance evaluation among the state-of-the-art OSG-PLLs (include Delay-PLL, Deri-PLL, Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL) under different grid disturbances such as voltage sags, phase, and frequency jumps, and in the presence of dc offset, harmonic components, and white noise in their input. This analysis provides a useful insight about the advantages and disadvantages of these PLLs. The performance enhancement of Delay-PLL, Deri-PLL, and CCF-PLL by including a moving average filter into their structure is another goal of this paper.**

***Index Terms*—Frequency estimation, orthogonal signal generator (OSG), phase estimation, phase-locked loop (PLL), single phase, synchronization.**

I. Introduction

THE accurate extraction of the grid voltage phase angle and frequency is of vital importance to ensure stable operation of grid-connected power-electronic-based equipment such as active power filters, uninterruptible power supplies, dynamic voltage restores, etc. [1]–[3]. However, the power quality issues caused by ever increasing penetration of the renewable energy sources such as the photovoltaic (PV) and wind power into the utility grid, as well as the proliferation of power-electronics-based loads in power systems has made this task more challenging than before. To tackle this problem, many advanced synchronization techniques have been proposed in recent years [1]–[13].

The Fourier-transform-based techniques such as the discrete Fourier transform [4], [5] and the fast Fourier transform [6] are the basic methods for the spectrum analysis of power signals and extraction of the grid voltage phase, frequency, and amplitude. However, these techniques often assume that the grid voltage waveform is periodic and repetitive, which may lead to spectrum leakage problem due to unsynchronized sampling effect, causing errors for frequency and phase angle detection [7]. The Kalman filter (KF) and the extended KF methods are alternative techniques for instantaneous tracking of grid voltage parameters [8]. However, the KF method is computationally demanding [9], some other techniques, such as the methods based on an adaptive notch filter [10], the zero-crossing detection method [11] and the frequency-locked loop (FLL) [12], [13] were also presented in the recent literature to analyze the grid voltage phase angle.

The PLL algorithms are probably the most popular synchronization techniques for the grid-connected inverters applications owing to their ease of implementation and robustness [14]–[21]. Generally, a PLL is composed of three parts: phase detector (PD), loop filter (LF), and voltage-controlled oscillator (VCO) [22]. The LF normally is a proportional-integral (PI) controller that results in a type-2 control system (a control system of type-N has N poles at the origin in its open-loop transfer function) [23]. In most cases, a first-order low-pass filter (LPF) is also cascaded with the PI controller to improve the PLL filtering capability. The first-order LPF, however, has a limited ability to suppress the grid disturbances. Therefore, under some scenarios, it may be useful to use higher order LPFs in the PLL control loop [24].

From the PD point of view, the simplest PLL is a power-based PLL (pPLL), which uses a sinusoidal multiplier as the PD [25]. The pPLL, however, suffers from remarkable double-frequency oscillations in their estimated quantities. A dynamic analysis and performance evaluation of the pPLL can be found in [26]. To overcome this drawback of the pPLL, some modifications have been suggested. In [27], a method based on peak voltage detection was proposed by Thacker *et al*., and in [28], a modified pPLL with double frequency and amplitude compensation method was presented by Golestan *et al*. Another approach to deal with the aforementioned problem of pPLLs is using an orthogonal-signal-generation (OSG)-based PD in the PLL structure. These PDs use an OSG unit to create a fictitious orthogonal signal from the original single-phase signal [29]–[32].

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In retrospect, the delay-based PLL (here named as Delay-PLL) is regarded as the earliest and simplest OSG-PLL method and its performance analysis was presented in [32]. Another simple method to generate an orthogonal signal is used a derivator (here named as Deri-PLL), however, this kind of PLL is rarely used in practical application due to the high sensitivity under distorted grid voltage conditions.

In recently years, some new OSGs schemes have been presented, such as the PD based on the second-order generalized integrator (corresponding to the SOGI-PLL) and inverse-park transform (corresponding to the Park-PLL), which show a relatively fast transient response, high disturbance rejection capability, and a robust performance [7], [22]. The SOGI scheme was first proposed in 2006 by Ciobotaru *et al*. [33]. In [34], a multiple SOGI plus an FLL scheme was proposed by Rodriguez *et al*., in which the dual SOGI acts as the basic module called MSOGI-FLL, which can be used to detect the different harmonic components of the input signal. A modified SOGI-based OSG was proposed by Karimi-Ghartemani *et al*. [18], in which an integrator is added to the SOGI structure to deal with the problem of dc offset. The Park-PLL also shows satisfactory performance under various grid voltage disturbance scenarios. In [35], the Park-PLL was used in a single-phase PV-power generation system to make the system more robust. In [22], a detailed mathematical analysis about the Park-PLL and SOGI-PLL was proposed by Golestan *et al*. and it is shown that these two PLL structures are equivalent to each other, from the control point of view.

On the other hand, the complex-coefficient filter (CCF) also has drawn much attention. In [36], a detail analysis about the CCF and multiple-CCF was presented, and in [37], the design oriented of the MCCF-PLL was suggested. In [38], the CCF-PLL based on the z-domain was introduced, in which the negative frequency component can be effectively removed by using the CCF block. Therefore, the CCF shown in [38] can be considered as another kind of OSG. In [39], the PLL using the dc offset error compensation (DOEC-PLL) was proposed, which is capable of eliminating dc component effectively. The variable time-delay PLL (VTD-PLL) was presented in [40], which is a software-PLL (SPLL) and can achieve a fast transient response with low computational burden. The PD of the VTD-PLL consists of a sinusoidal multiplier, thus, VTD-PLL can be seen as an extension of the *p*PLL. Further, in [41], a three-phase frequency-adaptive PLL (TPFA-PLL) was presented for single-phase applications, in which the input signal of the PLL was enhanced and the moving-average filter (MAF) was used to improve the filtering performance [42].

In this paper, a survey of some OSG-based PLLs is presented, and a detailed comparison among the Delay-PLL, Deri-PLL, Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL algorithms are carried out to gain a deep insight about their advantages and disadvantages. The evaluation is conducted under different grid disturbances such as voltage sags, phase and frequency jumps, and in the presence of harmonics, dc offset, and noise in the PLLs input. The results of this analysis can be very helpful for researcher and designers in the areas of single-phase grid-connected inverters and distributed generators (DGs).

The rest of this paper is organized as follows. Section II presents the overview of the aforementioned OSG-PLLs. The LF parameters design in s-domain is presented in Section III. In Section IV, the comparison of the experimental results under different grid voltage disturbance scenarios are presented. In Section V, the MAF method is presented to improve steady state and dynamic performance of Delay-PLL, Deri-PLL, and CCF-PLL. Finally, Section VI concludes this paper.

II. Overview of the Different PLL Algorithms

In this Section, eight different PLL algorithms mode are introduced and a generic mathematical model is also derived. Moreover, considering the practical implementation, all of the algorithms are conceived in the z-domain, and the following assumptions are considered: 1) the sampling frequency ($f_s = 1/T_s$) is fixed to 10 kHz, and the fundamental angular frequency ($\omega_{\rm ff}$) is set to be $2\pi 50$ rad/s and 2) the forward Euler method is used to discretize the LP and VCO except for the SOGI block, which is discretized by using the Tustin method in order to avoid the algebraic loop [38], [40].

The grid voltage is presented in the discrete form as

$$v = V_g \sin(\theta_g) = V_g \sin(\omega_g k T_s + \phi_g) \tag{1}$$

where V_g, θ_g, ω_g, and ϕ_g are amplitude, phase angle, angular frequency and initial phase of the grid voltage, respectively, and k denotes the kth sampling interval by the digital processor, and $k = 0, 1, 2, \ldots$,etc.

A. Conventional OSG-PLL

Fig. 1(a) shows the general structure of a conventional OSG-PLL. Fig. 1(b) illustrates the delay-based OSG, in which the orthogonal signal is created by *T*/4 (*T* is the grid fundamental period, and in discrete domain with a sample frequency $f_s = 10$ kHz, the delay block is expressed as z^{-50}) cycle delaying the original single-phase signal.

When the *T*/4 delay algorithm is used as the OSG shown in Fig. 1(a), the mathematical expressions for v_α and v_β are

$$\begin{cases} v_\alpha = V_g \sin(\theta_g) \\ \phi(\omega_g) = -\dfrac{(\omega_g - \omega_{\rm ff})\, T}{4} \\ v_\beta = -V_g \cos[\theta_g + \phi(\omega_g)] \end{cases} \tag{2}$$

where $\omega_{\rm ff}$ is the nominal frequency ($2\pi 50$ rad/s). By using Park's transformation, the mathematical expressions for *v*Delay *q* is

$$v_q^{\rm Delay} = V_g \sin(\theta_g)\cos(\hat{\theta}) - V_g \sin(\hat{\theta})\cos[\theta_g + \phi(\omega_g)] \tag{3}$$

where $\hat{\theta}$ is the estimated value of the phase angle. From (3), as expected, only when the grid voltage frequency is at its normal value, $\phi(\omega_g)$ will equal to zero, and the Delay-PLL can track the grid frequency without steady-state error, and vice versa.

The derivative-based OSG is shown in Fig. 1(c), in which the orthogonal signals are produced by the differential operation.

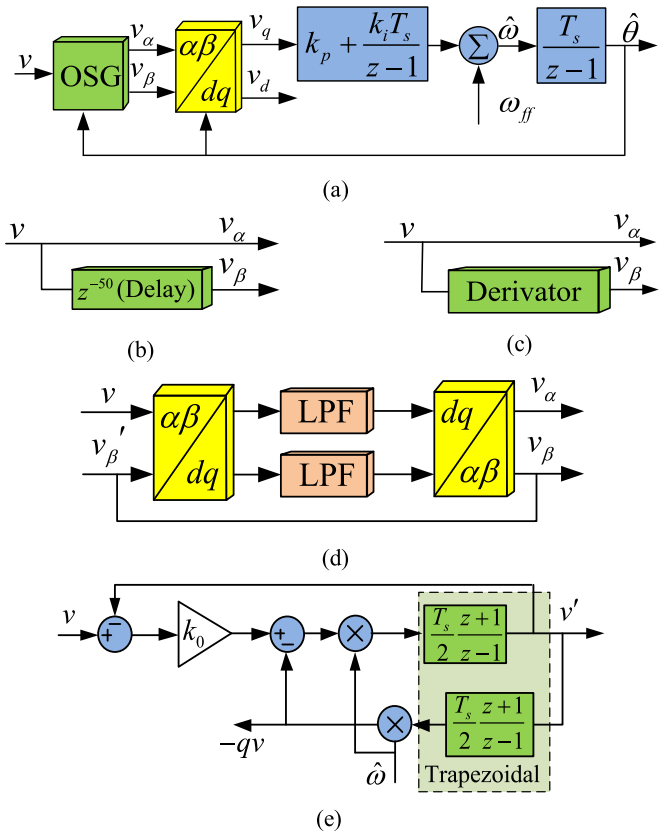

Fig. 1. Conventional OSG-PLL and different OSGs. (a) Block diagram of a typical OSG-PLL. (b) Delay-based OSG. (c) Derivative-based OSG. (d) Park-transform-based OSG. (e) SOGI-based OSG.

However, the differential operation will introduce high frequency noise and numerical errors. With the derivative-based OSG, the mathematical expressions of $v\mathrm{Deri}q$ can be expressed as

$$v_q^{\mathrm{Deri}} = V_g\left(1+\frac{\omega_g}{\omega_{\mathrm{ff}}}\right)\sin(\theta_g-\hat{\theta})+\left(1+\frac{\omega_g}{\omega_{\mathrm{ff}}}\right) V_g\sin(\hat{\theta})\cos(\theta_g). \tag{4}$$

As expected, (4) shows similar fluctuations characteristic as (3) when the grid frequency deviates from its nominal value. Moreover, if the gird voltage contains harmonics, the second term of (4) will increase with the increase of the order of harmonics. Especially in the condition of high-order harmonic and noise, the result of the estimated phase/frequency might be erroneous.

The Park-based PD is shown in Fig. 1(d), where the Park transform is used typically as a tool to project an input voltage vector, defined by in-quadrature signal in $\alpha\beta$ stationary reference frame, on the orthogonal axes of the *dq* synchronous reference frame [43]. The SOGI-based PD and the integrator discretized by the Tustin method is shown in Fig. 1(e). The equivalence of the Park and SOGI blocks was proved in [21], hence, the transfer function of the OSG can be derived as

$$\begin{cases} G_\alpha(z) = \dfrac{v_\alpha(z)}{v(z)} \\ \qquad = \dfrac{2k_0\hat{\omega}T_s(z^2-1)}{4(z-1)^2+2k_0\hat{\omega}T_s(z-1)+(\hat{\omega}T_s)^2(z+1)^2} \\ G_\beta(z) = \dfrac{v_\beta(z)}{v(z)} \\ \qquad = \dfrac{k_0\hat{\omega}^2T_S^2(z+1)^2}{4(z-1)^2+2k_0\hat{\omega}T_s(z-1)+(\hat{\omega}T_s)^2(z+1)^2}. \end{cases} \tag{5}$$

With the previous assumption, the output of the OSG block can be expressed as

$$\begin{cases} v_\alpha^{P,S} = V_g\sin(\theta_g)+g(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \\ v_\beta^{P,S} = -V_g\cos(\theta_g)+h(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \end{cases} \tag{6}$$

where the superscript *P* and *S* represents the Park-PLL and SOGI-PLL, $g(k)$ and $h(k)$ are the function of k, which can be expressed as [43]

$$\begin{cases} g(k) = -\dfrac{V_g}{\sqrt{1-(k_0/2)^2}}\sin(\omega_g\sqrt{1-(k_0/2)^2}kT_s) \\ h(k) = -\dfrac{V_g}{\sqrt{1-(k_0/2)^2}}\cos(\omega_g\sqrt{1-(k_0/2)^2}kT_s-\varphi) \\ \varphi = \arctan\left(\dfrac{k_0/2}{\sqrt{1-(k_0/2)^2}}\right). \end{cases} \tag{7}$$

It is worth noting that a gain $k_0 = 1.414$ implies the damping factor of (5) $\xi_G = 0.7$ (ξ_G indicate the damping ratio of (5) and depends the dynamic performance of the OSG block), which results in an optimal relationship between the setting time and overshoot in the dynamic response [35]. Thus, substituting $k_0 = 1.414$ into (7), the expressions for v_q is

$$\begin{cases} v_q^{P,S} = V_g\sin(\theta_g-\hat{\theta})+f(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \\ f(k) = -\sqrt{2}V_g\sin\left(\frac{\sqrt{2}}{2}\omega_gkT_s\right)\cos(\hat{\theta}) \\ \qquad -\sqrt{2}V_g\cos\left(\frac{\sqrt{2}}{2}\omega_gkT_s-\frac{\pi}{4}\right)\sin(\hat{\theta}) \end{cases} \tag{8}$$

where $f(k)$ is the fluctuating terms, which decays to zero with a time constant of $\tau_p = k_0/\sqrt{2}\omega_g = \sqrt{2}/\omega_g$ and vP,Sq converges to $\theta_g-\hat{\theta}$ in the steady-state conditions, which represents the steady-state error.

Then, v_q shown in (3), (4), and (8) is regulated to be zero and the phase angle of OSG output signal can be obtained. However, whether the phase angle of the input is equal to that of the output of the OSG is the key point to evaluate the performance of the OSG-PLL. Next, four recent OSG-PLLs are presented, namely, DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL.

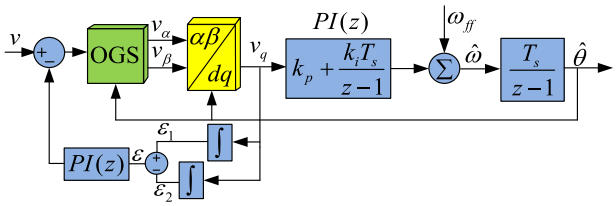

Fig. 2. Block diagram of the DOEC-PLL [39].

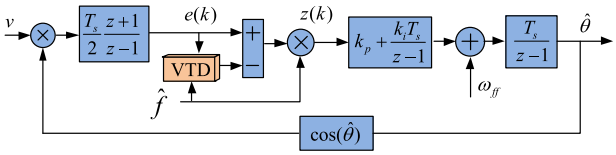

Fig. 3. Block diagram of the VTD-PLL [40].

B. DOEC-PLL

Fig. 2 shows the general structure of the DOEC-PLL presented by Hwang *et al.* [39]. In this paper, the inverse-park transform is used to generate a virtual voltage (v_β), which is delayed by 90° from the measured grid voltage v_α.

The grid voltage including the dc offset can be derived as

$$v = V_g \sin(\theta_g) + \Delta \tag{9}$$

where Δ is the amplitude of the dc offset.

Using the OSG technology and the Park's transformation, in the steady state, the following equations can be obtained:

$$\begin{cases} v_{d,\mathrm{dc}} = -1 - \Delta \sin\hat{\theta} + \Delta \cos\hat{\theta} \\ v_{q,\mathrm{dc}} = \Delta \sin\hat{\theta} + \Delta \cos\hat{\theta}. \end{cases} \tag{10}$$

To obtain the dc offset, the following expression is defined:

$$\begin{cases} \varepsilon_1 = \int_0^{\pi} (\Delta \sin\hat{\theta} + \Delta \cos\hat{\theta}) d\hat{\theta} = 2\Delta \\ \varepsilon_2 = \int_{\pi}^{2\pi} (\Delta \sin\hat{\theta} + \Delta \cos\hat{\theta}) d\hat{\theta} = -2\Delta. \end{cases} \tag{11}$$

The difference between ε_1 and ε_2 can be obtained as follows:

$$\varepsilon = \varepsilon_1 - \varepsilon_2 = 4\Delta. \tag{12}$$

Applying the integral operation at a specific interval in q-axis voltage, the dc offset can be separated as shown in (12). The PI controller is used to remove the dc offset error Δ.

C. VTD-PLL

Fig. 3 illustrates the block diagram of the VTD-PLL presented by A. Ozdemir *et al.* [40]. This algorithm adopts the variable time-delay algorithm, which reduces the computation load remarkably. From Fig. 3, the error signal $e(k)$ can be denoted as

$$e(k) = V_g \sin(\Delta\theta) \tag{13}$$

where $\Delta\theta = \theta_g - \hat{\theta} = (\omega_g - \hat{\omega})kT_s = \Delta\omega kT_s$.

After calculation of the VTD block, $z(k)$ is expressed as

$$z(k) = [e(k) - e(k-1)\hat{T}]\hat{f} \tag{14}$$

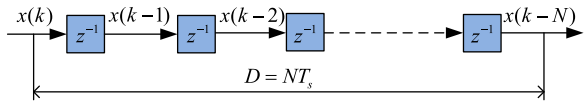

Fig. 4. Classical variable time-delay (VTD) structure [40].

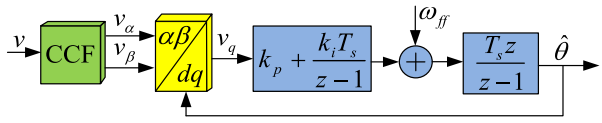

Fig. 5. Block diagram of the CCF-PLL [38].

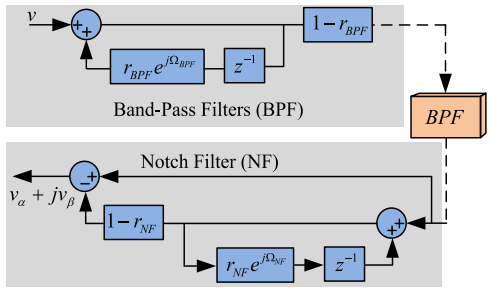

Fig. 6. Block diagram of complex-coefficient filters [38].

where $\hat{T}$ is the estimated period of input voltage and $e((k-1)\hat{T})$ is the delayed signal by $\hat{T}$, thus, (14) can be considered as derivative of $e(k)$ with respect to $\hat{T}$, which is derived as

$$z(k) = \frac{de(k)}{d\hat{T}} = \Delta\omega V_g \cos(\Delta\omega kT_s). \tag{15}$$

Fig. 4 shows the block diagram of the classical variable time-delay structure. In EN 50160 standard, the frequency range is considered 47–52 Hz, and IEC considered 42.5–57.5 Hz. To consider a more adverse scenario, in this study, locking frequency range for the PLL is 40 Hz $\leq f_{\mathrm{lock}} \leq$ 60 Hz, sampling period is $T_s = 100\ \mu$s. Accordingly, the range of N is calculated as $165 \leq N \leq 250$ [40].

Then, after convergence of the algorithm, $z(k)$ is regulated to be zero, which yields $\Delta\omega = 0$, and the estimated frequency is controlled to be the preset value.

D. CCF-PLL

Fig. 5 shows the lock diagram of the CCF-PLL presented by Ohoriet *et al.* [38]. In this algorithm, the complex-coefficient filter is configured as a first-order IIR filter and is composed of two complex-coefficient band-pass filters (BPFs) and one notch filter (NF), which are shown in Fig. 6.

The input voltage can be rewritten as

$$v = V_g \sin(\theta_g) = \frac{V_g}{2j}\left(e^{j\theta_g} - e^{-j\theta_g}\right). \tag{16}$$

The negative frequency component $(-\theta_g)$ is removed by the complex-coefficient filter, the output of the CCF block can be

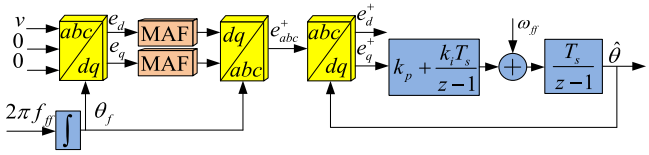

Fig. 7. Block diagram of the TPFA-PLL [41].

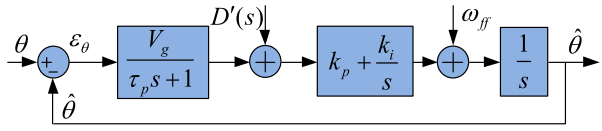

Fig. 8. Generic linearized model of the PLL.

expressed as

$$v_{\mathrm{CCF}} = \frac{V_g}{2j}e^{j\theta_g} = \frac{1}{2}V_g\sin(\theta_g) - \frac{j}{2}V_g\cos(\theta_g) = v_r + jv_i. \tag{17}$$

The magnitude of (17) is normalized as follows:

$$\frac{1}{\sqrt{v_r^2+v_i^2}}(v_r + jv_i) = \sin(\theta_g) - j\cos(\theta_g). \tag{18}$$

By extracting the real and imaginary parts of (18), which are represented by v_α and v_β, respectively, a pair of orthogonal voltage vector can be obtained. Therefore, notice that the CCF can be seen as a special OSG.

E. TPFA-PLL

Fig. 7 shows a three-phase PLL to estimate the phase, frequency, and amplitude of a single-phase system [41]. The *abc* input of the TPFA-PLL is assumed to be (v, 0, 0). If the window width of the MAF ($T\omega$) is equal *T*/2 all the second-order oscillation produced by unbalanced input voltage can be removed.

By applying the Park's transformation, e_d and e_q can be obtained as

$$\begin{cases} e_d = -\dfrac{V_g}{\sqrt{6}}[\cos(\theta_g+\theta_f) - \cos(\theta_g-\theta_f)] \\ e_q = \dfrac{V_g}{\sqrt{6}}[\sin(\theta_g+\theta_f) + \sin(\theta_g-\theta_f)] \end{cases} \tag{19}$$

where θ_f is an arbitrary angle at the grid frequency (ω_{ff}).If $T\omega = T/2$, the terms with $\theta_g + \theta_f$ in (19) are filtered by an MAF. Applying inverse Park's transformation to (19), the positive sequence is obtained in a stationary *abc* frame, as follows:

$$e^+_{abc} = \frac{1}{3}V_g\left[\sin(\theta_g), \sin\left(\theta_g - \frac{2\pi}{3}\right), \sin\left(\theta_g - \frac{4\pi}{3}\right)\right]^T. \tag{20}$$

Then, the output angle of the TPFA-PLL $\hat{\theta}$ (the estimated phase angle) is used in the *dq* transformation to transform the set of voltage in (20). The following expression can be obtained:

$$e_d^+ = \frac{V_g}{3}\cos(\theta_g - \hat{\theta}), e_q^+ = \frac{V_g}{3}\sin(\theta_g - \hat{\theta}). \tag{21}$$

Therefore, by controlling $e_{\mathrm{q}}+$ to be zero, the estimated frequency can be obtained. Unlike OGS-PLL, it is unnecessary for the TPFA-PLL to produce a pair of orthogonal signals hence the additional numerical error can be avoided.

III. Parameter Design Guidelines

Since the PLL model is set up in z-domain, it seems to be more accurate to perform the LF parameters tuning in the z-domain instead of the s-domain. It should be noticed that the PLL bandwidth is much lower than its sampling frequency. Therefore, the s-domain analysis/tuning can provide an accuracy as good as that achievable in z-domain. In addition, the analysis/tuning in the Laplace domain is more convenient and straightforward than that in the z-domain [42]. For these reasons, in this section, the generic linearized model of the PLL is presented in s-domain, which is shown in Fig. 8.

For the sake of simplicity, in the PLL linearized model, the input voltage amplitude V_g is assumed to be unity. This assumption can be simply realized by dividing the PD output signal by an estimation of the input voltage amplitude before it was fed into the LF [22]. In this case, the open-loop transfer function of the PLL can be expressed as

$$G_{\mathrm{ol}}(s) = \frac{k_p s + k_i}{s^2(\tau_p s+1)} = \frac{k_i(\tau_i s+1)}{s^2(\tau_p s+1)} \tag{22}$$

where $\tau_i = k_p/k_i$. It can be seen that (22) is a typical open-loop transfer function of the type-II system. In the recent literature, many parameters design methods based on such transfer function have been presented. In this paper, a systemic way called symmetrical optimum method is introduced to design the parameters [44]. The core insight of the symmetrical optimum method is to obtain the maximum phase margin (PM) at the crossover frequency ω_c. Therefore, from (22), the amplitude and phase frequency characteristics can be written

$$|G_{\mathrm{ol}}(j\omega)| = \frac{k_i}{\omega^2}\sqrt{\frac{(\tau_i\omega)^2+1}{(\tau_p\omega)^2+1}} \tag{23}$$

$$\angle G_{\mathrm{ol}}(j\omega) = \arctan(\tau_i\omega) - 180^\circ - \arctan(\tau_p\omega). \tag{24}$$

Therefore, the PM can be expressed

$$\gamma = \angle G_{ol}(j\omega_c) + 180^\circ = \arctan(\tau_i\omega_c) - \arctan(\tau_p\omega_c). \tag{25}$$

In order to obtain the ω_c when $\gamma = \gamma_{\max}$, take the derivative of (25) with respect to ω_c, and equate the result to zero, gives

$$\omega_c = \frac{1}{\sqrt{\tau_i\tau_p}}. \tag{26}$$

Thus, $\lg(\omega_c) = [\lg(\tau_i) + \lg(\tau_p)]/2$, which means in the bode diagram, $\lg(\tau_i)$ and $\lg(\tau_p)$ are symmetrical about $\lg(\omega_c)$. Then, $\gamma_{\max}$ can be expressed as

$$\gamma_{\max} = \arctan(\sqrt{\tau_i/\tau_p}) - \arctan(\sqrt{\tau_p/\tau_i}). \tag{27}$$

According to trigonometric function operation

$$\sin(\gamma_{\max}) = \frac{\tau_i - \tau_p}{\tau_i + \tau_p}. \tag{28}$$

TABLE I
SUMMARY OF RESULTS FOR THE EIGHT PLL ALGORITHMS

	Delay-PLL	Deri-PLL	Park-PLL	SOGI-PLL	DOEC-PLL	VTD-PLL	CCF-PLL	TPFA-PLL
Voltage Sag of –0.4 p.u.								
Settling time (5%)	22 ms	0	60 ms	55 ms	16 ms	20 ms	30 ms	15 ms
Frequency overshoot	2.9 Hz	0	2.5 Hz	2.5 Hz	0.7 Hz	0.7 Hz	10.0 Hz	1.5 Hz
Peak phase error	3.3°	0	6.7°	6.0°	2.0°	2.5°	5.5°	3.5°
Phase-Angle Jump of pi/2								
Settling time (5%)	40 ms	40 ms	81 ms	70 ms	82 ms	71 ms	104 ms	105 ms
Frequency overshoot	17.0 Hz	17.0 Hz	18.9 Hz	22.0 Hz	18.9 Hz	12.4 Hz	16.6 Hz	17.1 Hz
Peak phase error	16.2°	16.0°	37.0°	25.0°	40.5°	10.8°	17.8°	28.8°
Frequency Step of +5Hz								
Settling time (5%)	70 ms	70 ms	72 ms	53 ms	72 ms	90 ms	75 ms	90 ms
Frequency overshoot	2.2 Hz	2.0 Hz	2.5 Hz	2.1 Hz	2.5 Hz	3.5 Hz	8.1 Hz	2.6 Hz
Peak phase error	16.0°	12.5°	17.0°	15.5°	17.0°	25.0°	21.0°	25.0°
Harmonics								
Peak–peak frequency error	3.8 Hz	8.7 Hz	1.1 Hz	1.2 Hz	0.9 Hz	0	1.5 Hz	0
Peak–peak phase error	0.8°	2.2°	0.4°	0.4°	0.3°	0	0.6°	0
DC Offset								
Peak–peak frequency error	1.6 Hz	1.5 Hz	1.5 Hz	1.7 Hz	0	0	3.2 Hz	1.2 Hz
Peak–peak phase error	1.7°	1.5°	1.8°	1.9°	0	0	3.8°	1.2°
White Noise (Power = 0.01 W)								
Peak–peak frequency error	2.30 Hz	120 Hz	0.25 Hz	0.30 Hz	0.23 Hz	0.12 Hz	0.60 Hz	0.13 Hz
Peak–peak phase error	0.4°	3.1°	0.7°	0.8°	0.8°	0.5°	0.5°	0.6°

Then, from (28)

$$\tau_i = \tau_p \frac{1+\sin(\gamma_{\max})}{1-\sin(\gamma_{\max})}. \tag{29}$$

Normally, the PM with a range of $0 < \gamma_{\max} \leq 90$ is considered, thus, the inequality $\tau_i \geq \tau_p$ can be obtained. Supposing that $\lg(1/\tau_p) - \lg(1/\tau_i) = 2\lg\lambda(\lambda \geq 1)$, it can be obtained that

$$\tau_i = \lambda^2 \tau_p. \tag{30}$$

Considering (26) and (30), and assuming the equation (23) equals to 1 when $\omega = \omega_c$, then

$$\begin{cases} k_i = \dfrac{1}{\lambda^3 \tau_p^2} \\ k_p = \tau_i k_i = \dfrac{1}{\lambda \tau_p}. \end{cases} \tag{31}$$

It can be seen that k_p and k_i is the function of λ and τ_p, thus, next step is to determine the value of λ and $\tau_{\rm p}$. From the open-loop transfer function (22), the closed-loop transfer function can be expressed as

$$\begin{aligned} G_{cl}(s) &= \frac{G_{ol}(s)}{1+G_{ol}(s)} = \frac{k_i(\tau_i s+1)}{\tau_p s^3 + s^2 + k_i \tau_i s + k_i} \\ &= \frac{\lambda^2 \tau_p s + 1}{(\lambda \tau_p s+1)[\lambda^2 \tau_p^2 s^2 + \lambda(\lambda-1)\tau_p s + 1]}. \end{aligned} \tag{32}$$

From (32), the oscillating element should be design carefully. The damping ratio $\xi = (\lambda - 1)/2$, thus, ξ must be chosen to provide a fast transient response as well as a stable operation. Since most literature recommend $\xi = 0.7$ for the best damping, this selection yield $\lambda = 2.4$. Substituting $\lambda = 2.4$ and (30) into (28), the value of $\gamma_{\max}$ can be derived as

$$\gamma_{\max} \approx 45^\circ \tag{33}$$

which can be interpreted as a perfect PM.

Then, the disturbance rejection capability of the system is taken into consideration. The proper attenuation at $2\omega_{\rm ff}$ (which is generated by the harmonic) is selected to be 25 dB in this paper. Substituting $\lambda = 2.4$, (30), and (31) into (23), and assuming (23) equals to –25 dB when $\omega = 2\omega_{\rm ff}$, an approximate value of $\tau_p = 0.004$ can be calculated. Then, the LF parameter can be calculated as $k_i = 4521$ and $k_p = 104$.

With the parameter designed, the PM of the PLL is about 44.8°, the crossover frequency $\omega_{\rm c} = 2\pi 16.6$ rad/s and the attenuation at $2\omega_{\rm ff}$ is 24.3 dB. Thus, the PLL shows a high disturbance rejection capability and fast transient response.

IV. EXPERIMENTAL RESULTS

The aim of this section is to evaluate the performance of the eight PLLs under different grid scenarios, such as voltage sag, phase jump, frequency step, harmonics, dc offset and noise. To validate the analysis, the presented algorithms are tested in the Microgrid Research Lab, Aalborg University [45], and the experimental prototype was based on the 2.2-kW Danfoss inverter controlled in voltage control mode (VCM) using an *LCL* output filter with resistive load, the capacitor voltage of the *LCL* filter was controlled to synthesize the virtual grid conditions. The inverter PWM frequency was set to be 10 kHz in order to evaluate the PLL algorithms with a discrete time step of 100 μs, as analyzed in this paper. The dSPACE1006 platform was utilized to implement the Simulink-based control algorithms and the compiled executable file was downloaded to the dSPACE1006 controller to extract the real-time grid-synchronization signals.

The binary word size was only several kilobytes (kB) when the VCM was adopted for inverter control and the eight PLL algorithms were implemented, which facilities the practical implementation in both fixed point and floating point digital signal

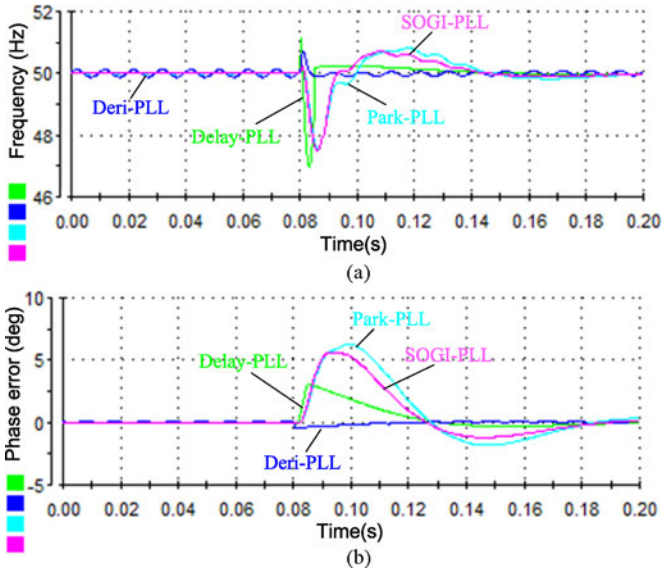

Fig. 9. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL under 0.4 p.u. voltage sag in grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

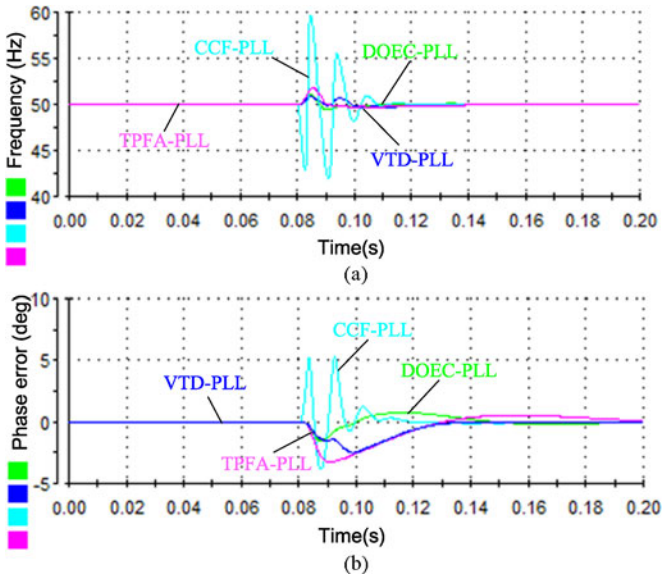

Fig. 10. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL under 0.4 p.u. voltage sag in grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

processors (DSPs). The phase and frequency step were set to be 90° and 5 Hz, respectively. Throughout the experimental studies, the sampling frequency is fixed to be 10 kHz and the nominal angular frequency is set to $2\pi 50$ rad/s. The detailed comparison of eight PLL algorithms under different grid disturbance scenarios is shown in Table I.

A. Performance Comparison Under Voltage Sag

Figs. 9 and 10 show the experimental results of the estimated frequency and the phase estimation error when the grid is subjected to 0.4 per unit (p.u.) voltage sag. It can be observed that Deri-PLL presents a ripple of 0.1 Hz in the estimated frequency with a slight overshoot. The Park-PLL, SOGI-PLL have similar dynamic performance, having all of them a respond time of about three cycles and an overshoot of 2.5 Hz. The Delay-PLL shows an overshoot of 3 Hz, but a smaller overshoot in phase error compared to the Park-PLL and the SOGI-PLL ones. The CCF-PLL shows a high frequency overshoot (10 Hz), and a relatively slow dynamic response with a respond time of 1.5 cycles. By comparison, VTD-PLL, DOEC-PLL, and TPFA-PLL show a relatively fast overshoot compared to other grid synchronization schemes, with a transient overshoot of 0.7, 0.7, and 1.5 Hz, respectively.

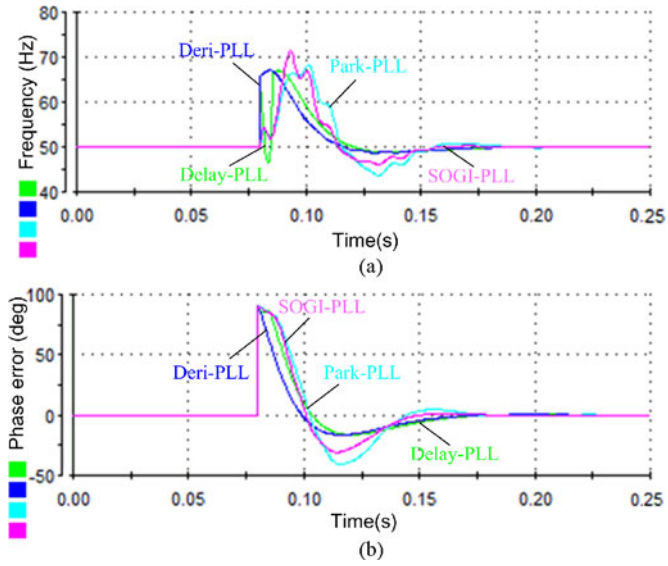

Fig. 11. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL under 90° phase jump in grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

B. Performance Comparison Under Phase-Angle Jump

Figs. 11 and Fig. 12 show the experimental results of the estimated frequency and the phase estimation error when the grid is subjected to 90° phase-angle jump. Among the OGS-based PLLs, the Delay-PLL and Deri-PLL show better performance than the Park-PLL and SOGI-PLL with a response time of about two cycles. A similar performance can be observed between Park-PLL and DOEC-PLL, due to the equivalence of the OSG block, with a response time of four cycles. The SOGI-PLL and VTD-PLL show a response time of 3.5 cycles. But for CCF-PLL and TPFA-PLL, the response time is about five cycles. Therefore, optimal dynamic performance can be obtained by using the Delay-PLL under grid voltage phase-angle jumps.

C. Performance Comparison Under Frequency Steps

Figs. 13 and 14 show the experimental results of the estimated frequency and the phase estimation error when a sudden frequency jump of 5 Hz occurs in the grid voltage. The Delay-PLL and Deri-PLL show similar steady-state fluctuation, and in

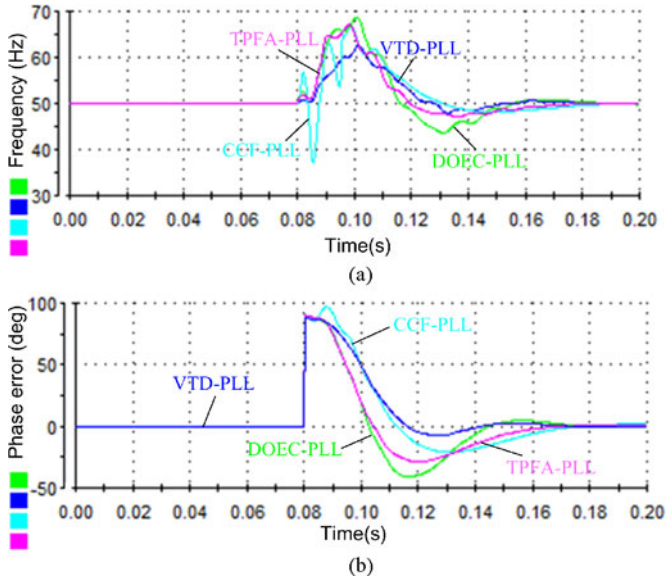

Fig. 12. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL under 90° phase jump in grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

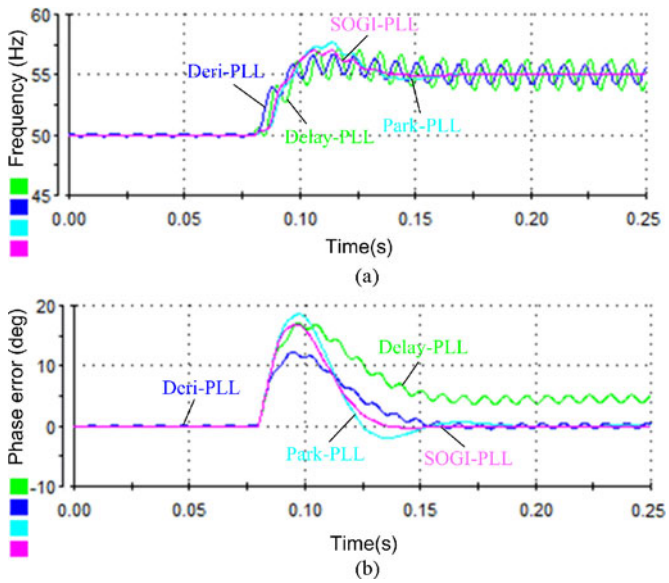

Fig. 13. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL under a sudden frequency jump of +5 Hz. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

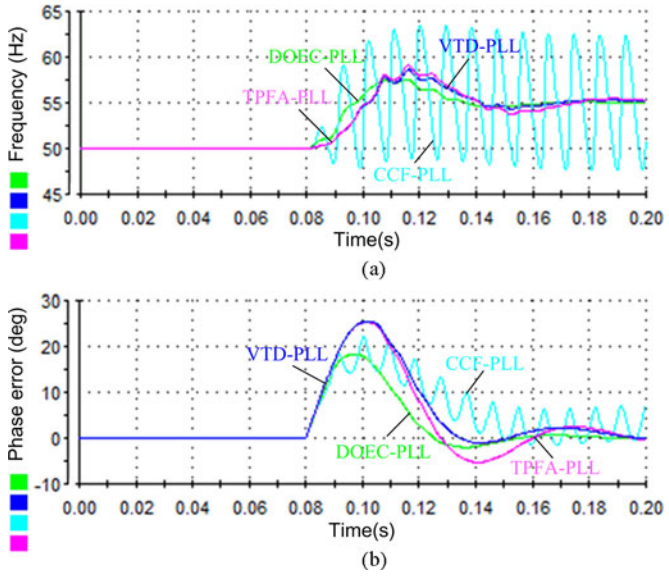

Fig. 14. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL under a sudden frequency jump of +5 Hz. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

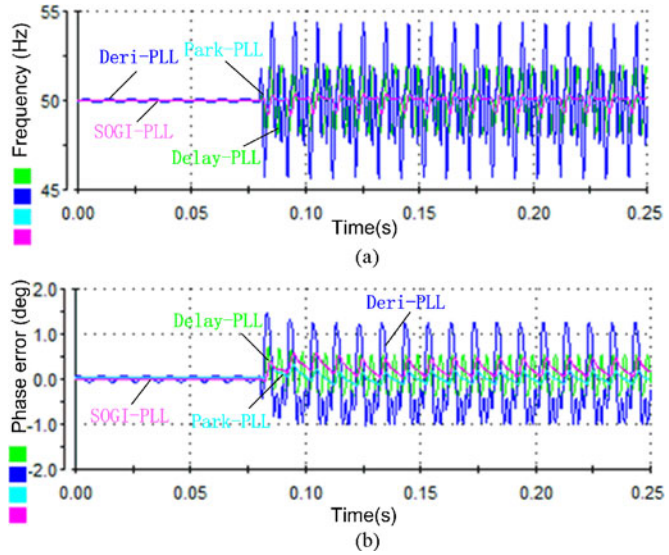

Fig. 15. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL under 0.05-p.u. third-order, 0.05-p.u. fifth-order, and 0.04-p.u. seventh-order harmonics. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

particular, the Delay-PLL shows steady-state error (about 5°) in phase estimation because of the fix time delay. The CCF-PLL shows a higher fluctuation of about 15 Hz due to the adoption of the BPF, which has a narrow pass band. Because of the integral link in VTD-PLL, and the frequency-adaptive MAF in TPFA-PLL, the two PLLs show a slow dynamic response, both with a response time of about 4.5 cycles. For Park-PLL and DOEC-PLL, similar results are achieved, the estimated frequency is locked to the rated value in about 3.5 cycles, and for Deri-PLL and SOGI-PLL, the response time is around 2.5 cycles. Through the comprehensive comparison, the Park-PLL and SOGI-PLL show the relatively satisfactory performance when frequency step occurs.

D. Performance Comparison Under Grid Voltage Harmonics

According to EN 50160 Standard [46], the maximum allowed total harmonic distortion is 8%; 0.05-p.u. third-, 0.05-p.u. fifth-, and 0.04-p.u. seventh-order harmonics components are applied to the grid voltage to test these algorithms. Figs. 15 and 16 show the experimental results of the estimated frequency and

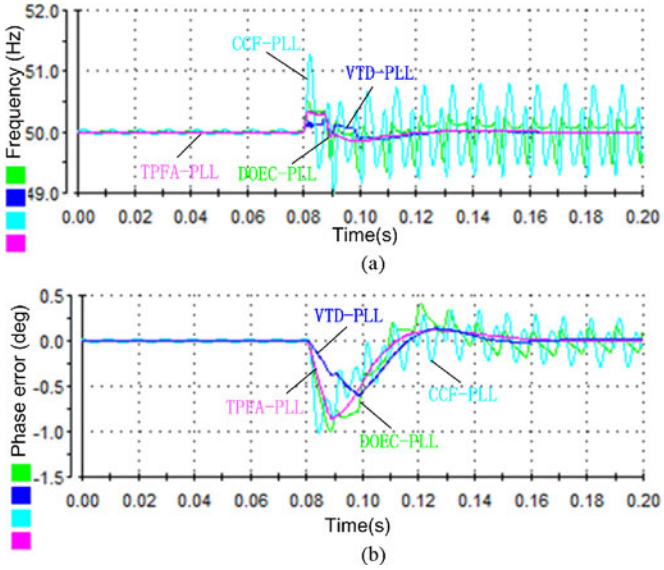

Fig. 16. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL under 0.05-p.u. third-order, 0.05-p.u. fifth-order, and 0.04-p.u. seventh-order harmonics. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

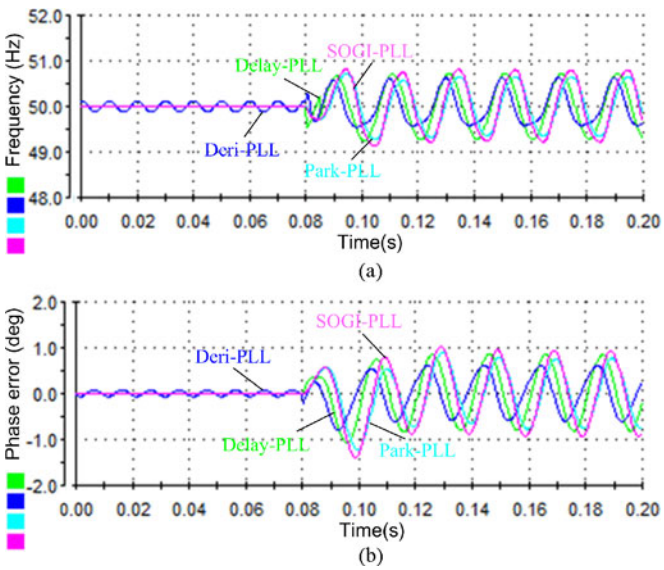

Fig. 17. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL under a sudden dc offset of 10 V. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

the phase estimation error. The Delay-PLL and Deri-PLL show noticeable oscillations in the estimated frequency due to the lack of filter. By comparison, the oscillations of Park-PLL, SOGI-PLL, and DOEC-PLL are much smaller, with a frequency error of about 1 Hz. The CCF-PLL shows a frequency error of about 1.5Hz. However, the VTD-PLL and TPFA-PLL show the lowest frequency oscillations with nearly zero steady-state errors compared to other PLL algorithms.

E. Performance Comparison Under DC Offset

Figs. 17 and 18 show the experimental results of the estimated frequency and the phase estimation error when a sudden dc

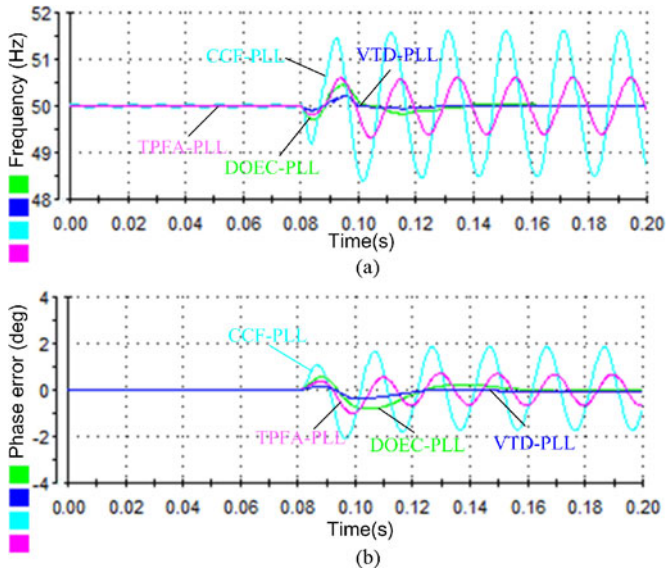

Fig. 18. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL under a sudden dc offset of 10 V. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

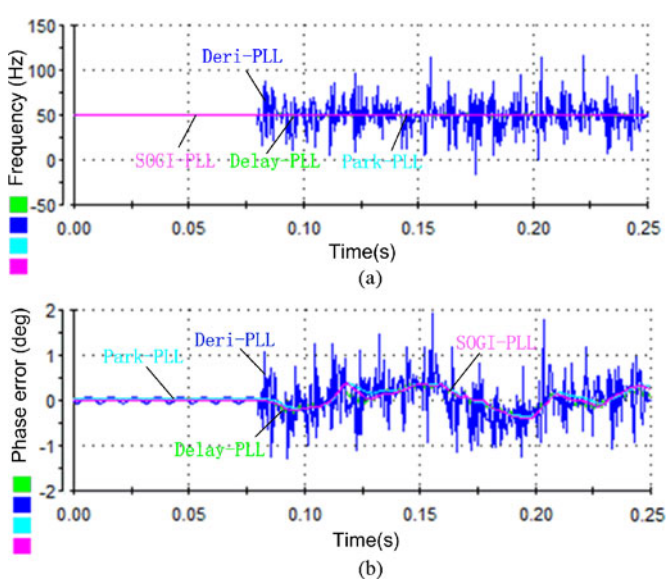

Fig. 19. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL, and SOGI-PLL when the noise (variance $\sigma^2 = 0.01$) is suddenly applied in the grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

offset of 0.04 p.u. occurs in the grid voltage. In this case, the four OGS-based PLLs have the similar steady-state oscillations with the peak–peak frequency error of nearly 1.5 Hz. However, the CCF-PLL undergoes the biggest steady-state oscillations of 3.2 Hz. The TPFA-PLL shows the estimation error of about 1.3 Hz in the estimation frequency. Because of the dc offset error compensator, the DOEC-PLL can acquire the zero steady-state error of both estimated frequency and phase. It is interesting to notice that the VTD-PLL also shows similar dynamic response to DOEC-PLL. Therefore, the best performance under dc offset scenario is achieved by DOEC-PLL and VTD-PLL.

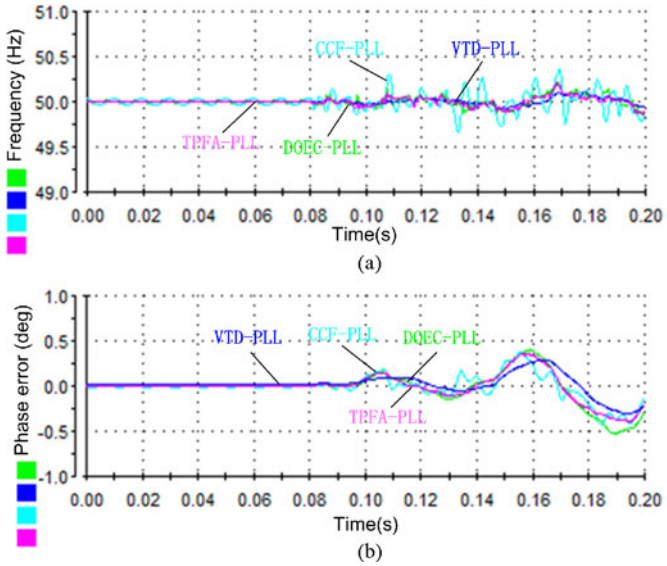

Fig. 20. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL when the noise (variance $\sigma^2 = 0.01$) is suddenly applied in the grid voltage. (a) Estimated grid fundamental frequency. (b) Estimation error of phase angle.

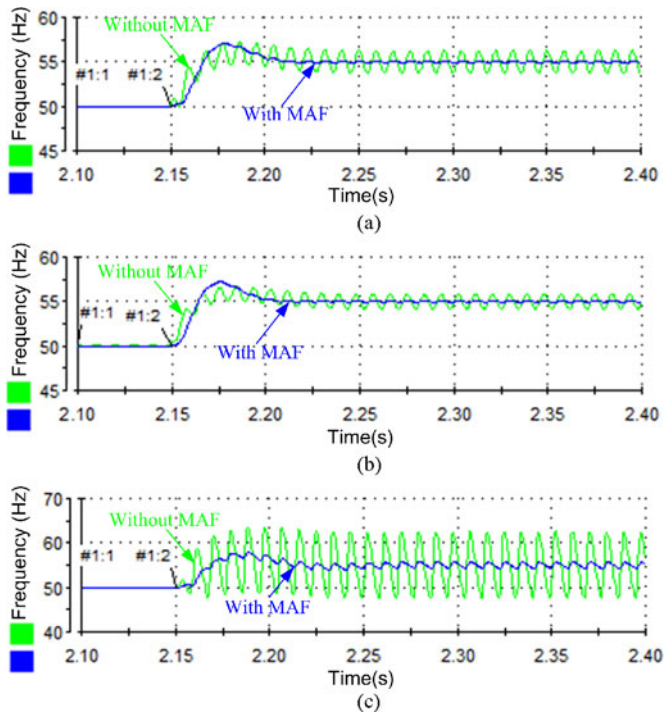

Fig. 21. Obtained results with and/or without MAF when the grid voltage undergoes a frequency of +5 Hz. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

F. Performance Comparison Under White Gaussian Noise

To evaluate the electromagnetic interference (EMI) noise immunity of the PLLs, a white Gaussian noise of variance $\sigma^2 = 0.01$ is added to the grid voltage. The signal-to-noise ratio (SNR) in the PLL input is $SNR = 10 \log (1/2\sigma^2) = 17$ dB. The noisy waveform is sampled at a rate of 100 kHz, and is then fed to a digital antialiasing. This high sampling rate is to avoid the

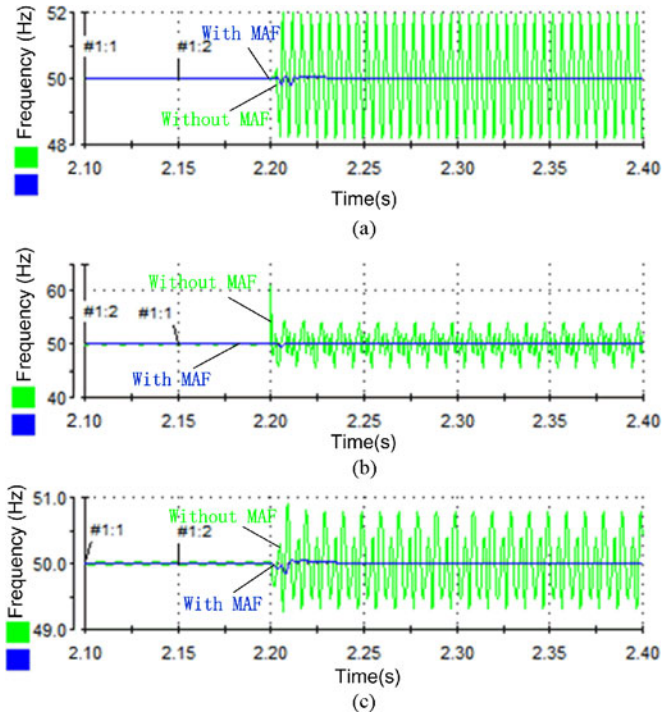

Fig. 22. Experimental results with and without MAF when the grid voltage undergoes 0.05-p.u. third-order, 0.05-p.u. fifth-order, and 0.04-p.u. seventh-order harmonics. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

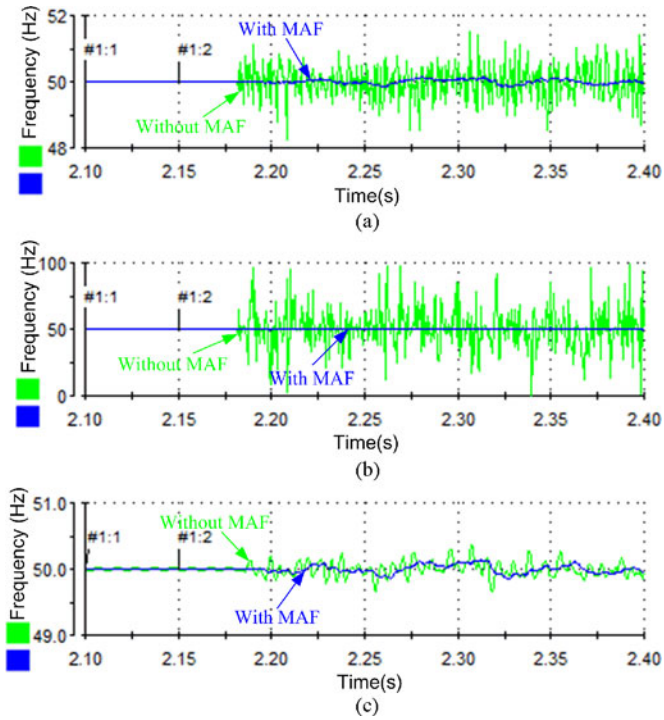

Fig. 23. Experimental results with and without MAF when the noise (variance $\sigma^2 = 0.01$) is suddenly applied in the grid voltage. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

TABLE II
COMPARISON OF DELAY-PLL, DERI-PLL, AND CCF-PLL WITH OR WITHOUT MAF

	Delay-PLL		Deri-PLL		CCF-PLL	
With (w) or Without (w/o) MAF	w/o-MAF	w-MAF	w/o-MAF	w-MAF	w/o-MAF	w-MAF
Frequency Step of +5Hz						
Steady-state oscillations	2.50 Hz	0.22 Hz	1.62 Hz	0.10 Hz	14.72 Hz	1.27 Hz
Harmonics						
Peak–peak frequency error						
Peak–peak phase error	3.8 Hz	0	8.7 Hz	0	1.5 Hz	0
	0.8°	0	2.2°	0	0.6°	0
White Noise (Power = 0.01 W)						
Peak–peak frequency error	2.3 Hz	0.22 Hz	120 Hz	0.92 Hz	0.60 Hz	0.30 Hz
Peak–peak phase error	0.4°	0.3°	1.5°	0.4°	0.5°	0.3°

aliasing effects and increase the accuracy of simulations. A digital first-order LPF with cutoff frequency of 4 kHz is considered as the antialiasing filter. The output of antialiasing filter is down sampled to 10 kHz and is fed to the PLL [42].

Figs. 19 and 20 show the experimental results of the estimated frequency and the phase estimation error. Similar to the case of harmonic contamination, the Delay-PLL and Deri-PLL show noticeable oscillations in the estimated frequency with the amplitude of about 2.3 Hz and more than 100 Hz, respectively. The Park-PLL and DOEC-PLL show the estimation error of about 0.25 Hz. The VTD-PLL and TPFA-PLL show the lowest steady-state oscillations of about 0.12 Hz. For CCF-PLL, the peak-to-peak frequency error is about 0.6 Hz, which is bigger than SOGI-PLL (0.30 Hz).

V. PERFORMANCE IMPROVEMENT USING MAF

From experimental results presented in the last section, the Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL, and TPFA-PLL show relatively satisfactory performance. However, the performance of Delay-PLL, Deri-PLL, and CCF-PLL under grid frequency variations, harmonics, and white noise scenarios is still unsatisfactory. In order to optimize the performance of Delay-PLL, Deri-PLL, and CCF-PLL, the MAF is presented to achieve this propose as an inner-loop filter. It should be noted that the application of an MAF may reduce the open-loop bandwidth due to the large phase shift of the MAF [47].

The experimental results under grid frequency variations, harmonics, and white noise scenarios are shown in Figs. 21, 22, and 23, respectively. The detailed comparisons of Delay-PLL, Deri-PLL, and CCF-PLL with and without MAF are shown in Table II.

Fig. 21 shows the comparative results between with and/or without MAF when the grid voltage undergoes a frequency jump of 5 Hz. It is obvious that the steady-state oscillations have been mitigated by the use of the MAF. For the Delay-PLL, the estimation error in frequency is reduced from 2.5 to 0.2 Hz. For the Deri-PLL, the estimation error is reduced from 1.6 to 0.1 Hz and for the CCF-PLL, the error is reduced from 14.7 to 1.2 Hz.

Fig. 22 shows the comparative results between with and/or without MAF when the grid voltage undergoes 0.05-p.u. third-order, 0.05-p.u. fifth-order, and 0.04-p.u. seventh-order harmonics. Similarly as in the previous analysis, the estimation error in the frequency has been reduced to zero, which means MAF almost eliminates the harmonics completely.

Fig. 23 shows the comparative results between with and/or without MAF when the white Gaussian noise (variance $\sigma^2 = 0.01$) is suddenly applied in the grid voltage. For Delay-PLL and Deri-PLL, it shows that the steady-state errors are eliminated effectively. As for the CCF-PLL, it is interesting to notice that the fluctuation ripple of about 0.2 Hz in the estimated frequency is also suppressed.

VI. CONCLUSION

A detailed analysis and performance comparison of eight single-phase PLLs is presented in this paper. From the presented comprehensive comparison, it is found that Delay-PLL, Deri-PLL, and VTD-PLL show relatively desired dynamic performance under voltage sag and phase-angle jump scenarios. When grid voltage undergoes frequency step, Park-PLL and SOGI-PLL may be a good choice. When grid voltage undergoes harmonic contamination scenario, TPFA-PLL can achieve zero steady-state error due to the use of an MAF, and for dc offset scenario, DOEC-PLL and VTD-PLL show the best performance. When grid voltage undergoes random noise contamination scenario, all PLLs show some noise immunity capability except for Delay-PLL and Deri-PLL due to the lack of filter in their control structures. However, under a wide range of grid disturbance conditions, Park-PLL, SOGI-PLL, and TPFA-PLL show satisfactory performance for achieving a tradeoff between steady-state accuracy and dynamic response.

Finally, the MAF is applied to effectively attenuate steady-state oscillation of the Delay-PLL, Deri-PLL, and CCF-PLL under grid frequency step, harmonics, and noise scenarios. The presented results provide useful guidelines for choosing and designing the proper grid synchronization schemes for single-phase grid-connected inverters and DGs.

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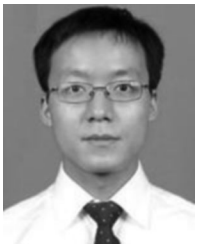

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