Offset rejection for PLL based synchronization in grid-connected converters

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***Abstract* - Grid-connected converters rely on fast and accurate detection of the phase angle, amplitude and frequency of the utility voltage to guarantee the correct generation of the reference signals. An important issue associated with accurate grid voltage monitoring is the presence of an offset in the measured grid voltage. This voltage offset is typically introduced by the measurements and data conversion processes and causes errors for the estimated parameters of the grid voltage. Accordingly, this paper presents an offset rejection method for grid-connected converters based on a Phase-Locked-Loop (PLL) technique. The offset rejection method relies on the Second Order Generalized Integrator (SOGI) having the advantages of a simple implementation independent of the grid frequency and avoidance of filtering delays due to its resonance at the fundamental frequency. Selected experimental results validate the performance and robustness of the proposed offset rejection method.**

***Keywords* - Offset Rejection, PLL, Inverters, Grid Connected Systems, Distributed Generation, Grid Voltage Monitoring.**

I. INTRODUCTION

Phase, amplitude and frequency of the utility voltage are critical information for the operation of the grid-connected inverter systems. In such applications, an accurate and fast detection of the phase angle, amplitude and frequency of the utility voltage is essential to assure the correct generation of the reference signals and to cope with the standard requirements for the grid-connected converters, such as [1] and [2].

An important issue associated with accurate grid voltage monitoring is the presence of an offset in the measured grid voltage. This voltage offset is typically introduced by the measurements and data conversion processes and causes errors for the estimated parameters of the grid voltage. For instance, the grid-connected converters based on fixed-point DSP require a manual setting of an offset before the Analogue to Digital (A/D) conversion in order to deliver a positive signal (e.g. 0 to +3V signal) to the A/D converter input of the fixed-point DSP. After the A/D conversion the signal data type is `uint` (unsigned integer) and has to be converted to `int` (integer) in accordance with the offset applied before the A/D conversion. Therefore, a perfect matching between the offset value applied before the A/D conversion and the signal data type conversion from `uint` to `int` is difficult to obtain.

As concluded in [3], the error caused by the voltage offset has the same frequency as the utility voltage. Since the frequency of the error is relatively low, the low pass filtering effect of the loop filter cannot be expected. The extremely low band-width can provide the filtering effect. However, this degrades the dynamic performances and is not acceptable. Therefore, more attention has to be considered for the voltage offset.

This paper presents an effective offset rejection method for grid-connected converters based on a PLL technique. The proposed method is suitable for both, grid-connected systems (e.g. Photovoltaics, Wind Turbines, etc) and power condition equipments (e.g. Uninterruptible Power Supply (UPS), active filters, etc) which rely on PLL based synchronization.

II. SYSTEM DESCRIPTION

A single-phase Distributed Power Generation System (DPGS) based on a PLL technique has been chosen in order to test the proposed method. The general structure of the single-phase DPGS including the power circuit and the control diagram is presented in Fig. 1.

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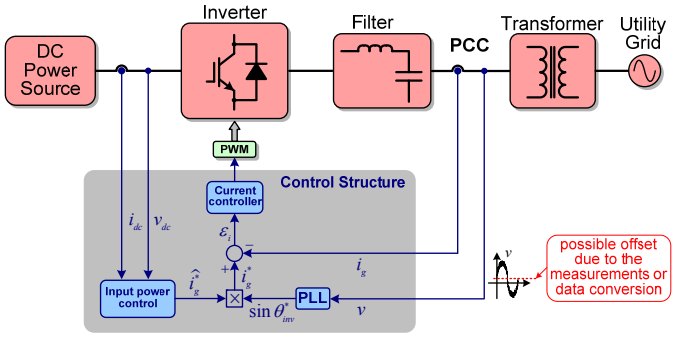


Fig. 1. Single-phase DPGS based on PLL technique.

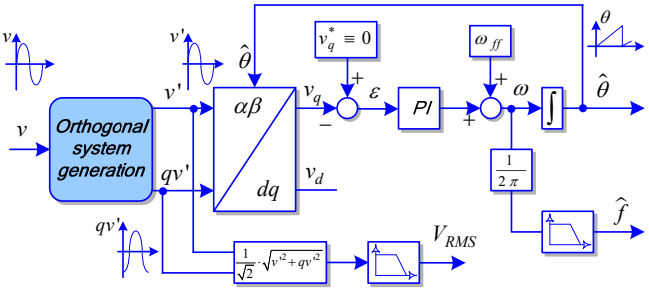


Fig. 2. General structure of a single-phase PLL.

Fig. 2 shows the general structure of a single-phase PLL including the grid voltage monitoring. Usually, the main difference among different single-phase PLL topologies is the orthogonal voltage system generation technique.

There are different ways of generating the orthogonal voltage system for a single-phase system. The common methods used in the technical literature make use of the transport delay block, Hilbert transformation, inverse Park transformation as presented in [4]-[9]. However, these methods have one or more of the following shortcomings: frequency dependency, high complexity, nonlinearity, poor or no filtering. Therefore, more attention should be paid on single-phase PLL systems.

III. OFFSET REJECTION METHOD

An alternative of creating an orthogonal voltage system for a single-phase PLL is presented in [10]. The proposed Orthogonal Signal Generator (OSG) method relies on the Second Order Generalized Integrator (SOGI). The advantages of the proposed approach include simple implementation independent of the grid frequency and avoidance of filtering delays due to its resonance at the fundamental frequency.

The offset rejection method presented in this paper is based on the OSG-SOGI (OSG based on SOGI) structure. The method of creating the orthogonal voltage system for a single-phase PLL including the offset rejection feature is further presented.

A. Orthogonal system generation

The OSG-SOGI structure is depicted in Fig. 3. The input signal v is the grid voltage. As output signals, two sine waves (v' and qv') with a phase shift of 90° are generated. The component v' has the same phase and magnitude as the fundamental of the input signal (v) [11].

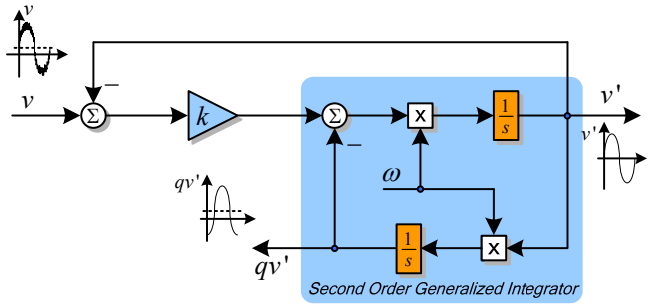


Fig. 3. Standard OSG-SOGI structure [10].

The SOGI structure is defined in (1) [10]-[14]. The closed-loop transfer functions ($H_d = \frac{v'}{v}$ and $H_q = \frac{qv'}{v}$) of the structure presented in Fig. 3 are defined in (2) and (3).

$$H_{SOGI}(s) = \frac{\omega s}{s^2 + \omega^2} \quad (1)$$

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \quad (2)$$

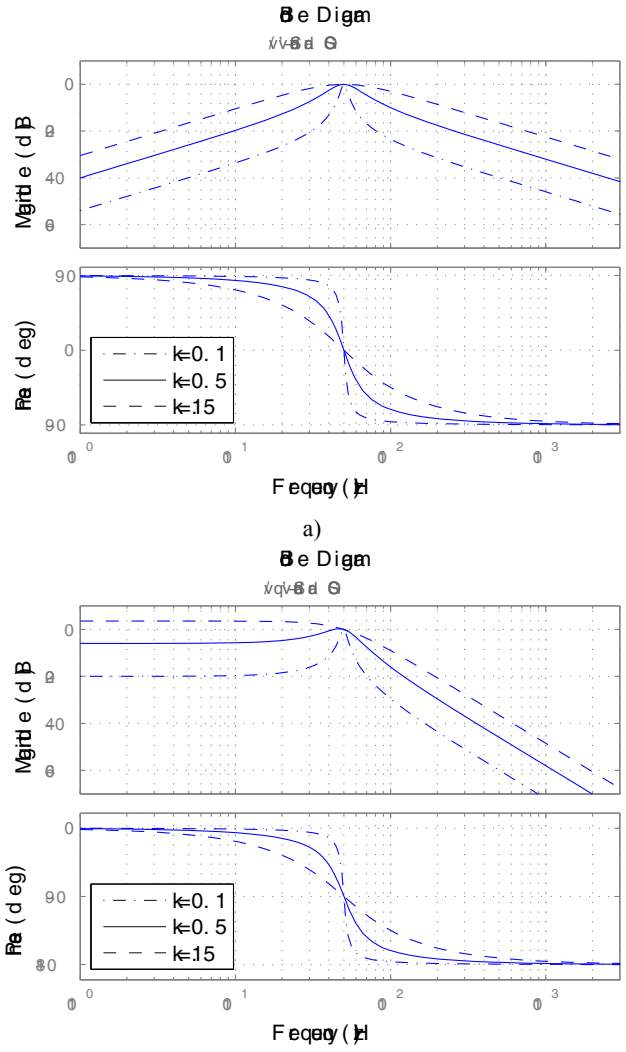
$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \quad (3)$$

- where ω represents the resonance frequency of the SOGI;
- k is the gain which affects the bandwidth of the OSG-SOGI structure.

The Bode representations of the closed-loop transfer functions $H_d = \frac{v}{v'}$ and $H_q = \frac{qv'}{v}$, for the proposed OSG-SOGI at different values of gain k, are shown in Fig. 4a and Fig. 4b. The tuning of the proposed structure is frequency dependent, thus problems can occur when grid frequency has fluctuations. As a consequence, an adaptive tuning of the structure with respect to its resonance frequency is required. Therefore, the resonance frequency of the SOGI is adjusted online using the frequency provided by the PLL structure.

Using the OSG-SOGI structure the input signal v (grid voltage) is filtered resulting two clean orthogonal voltage waveforms v' and qv', due to the resonance frequency of the SOGI at ω (grid frequency).

The single-phase PLL based on the SOGI combines all the advantages of other known methods such as Transport-Delay, Hilbert Transformation, and Inverse Park Transformation [4]-[8]. Specifically, by using the OSG-SOGI structure shown in Fig. 3, the following three main tasks can be accomplished: - generation of the orthogonal voltage system; - filtering of the orthogonal voltage system without delay; - making the OSG structure frequency adaptive. However, the OSG-SOGI structure, as it is presented in Fig. 3, has a common drawback specific to all methods presented in [4]-[8]. Namely, all OSG methods are sensible at voltage offset. As it can be seen from Fig. 4, the OSG-SOGI structure rejects the DC component only for the component v'. The orthogonal component qv' is directly affected by the presence of any voltage offset. Therefore, an improved OSG-SOGI structure is proposed and presented in the next section.



a)

b)

Fig. 4. Bode plots of the closed-loop transfer functions: a) $H_d = v/v'$ and b) $H_d = v/qv'$ for different values of gain k.

B. Offset rejection of the measured voltage

The improved OSG-SOGI structure is shown in Fig. 5. As it can be seen from Fig. 4a, the component v' does not contain any DC component. In the case of any offset in the voltage signal v, the signal ε will contain that offset due to the subtraction $v - v' = \varepsilon$. Therefore, the improvement over the structure presented in Fig. 3 consists in subtracting $k\varepsilon$ from qv_i' (green dotted [----] structure including the Low Pass Filter (LPF) from Fig. 5). Furthermore, a LPF is required in order to filter out the harmonics which can be present in the voltage signal (v). From Fig. 6a and Fig. 6b it can be noticed the effectiveness of the proposed method for the offset rejection. The solid lines are obtained using the standard OSG-SOGI presented in Fig. 3 and the dashed, dotted and dashdot lines are obtained for three different cut-off frequencies of the LPF using the improved structure presented in Fig. 5. A gain k of 0.7 has been used for the plots presented in Fig. 6a and Fig. 6b.

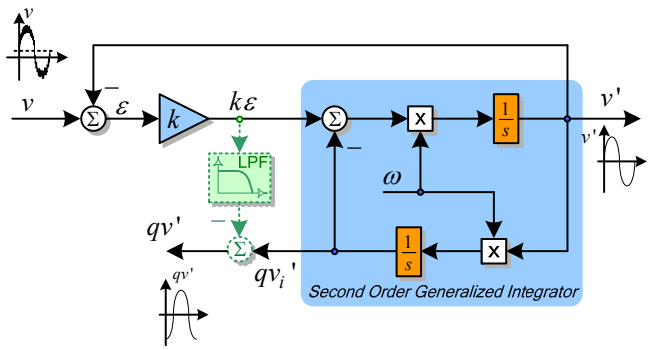
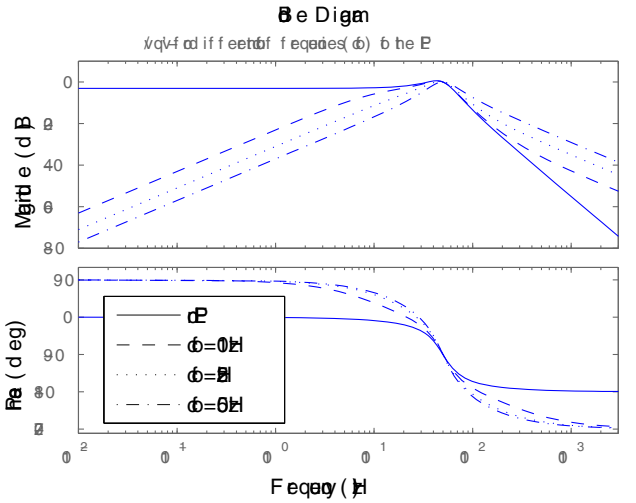
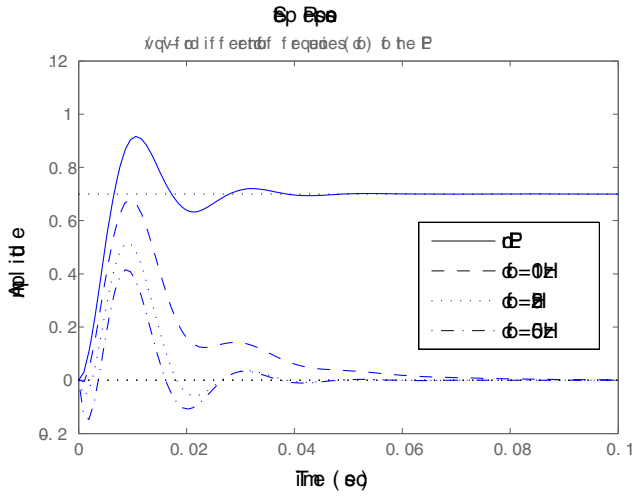


Fig. 5. Improved OSG-SOGI structure.



a)



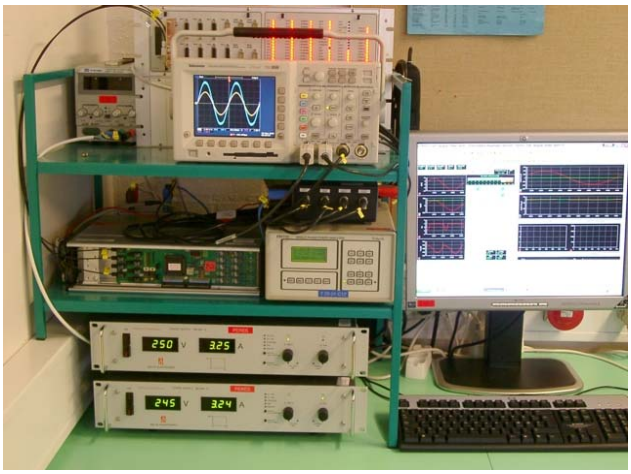
b)

Fig. 6. Bode plot (a) and step response (b) of the closed-loop transfer function $H_d = v/qv'$ for k=0.7.

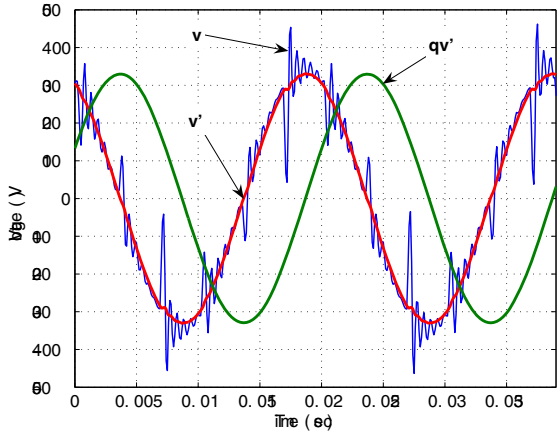
IV. Results

The PLL structure based on OSG-SOGI has been implemented using a setup based on dSPACE 1103 (Fig. 7a). The voltage waveforms were generated by an AC source. Fig. 7b shows how the OSG-SOGI structure is able to generate a

clean orthogonal voltage system (represented by v' and qv') using a highly distorted grid voltage waveform (v) containing notches.



a)

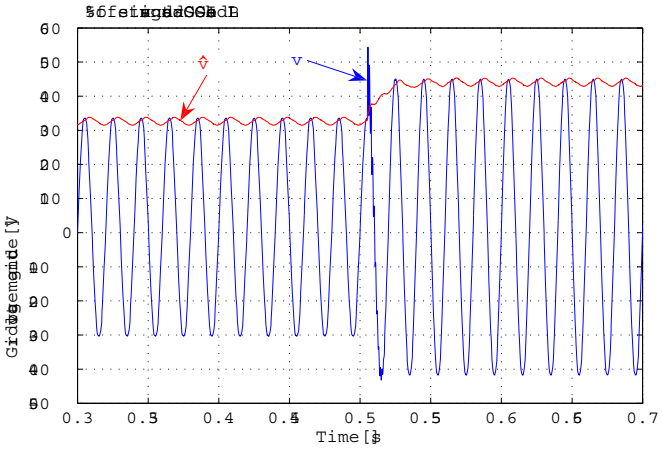


b)

Fig. 7. a) Experimental setup; b) Distorted grid voltage v and the generated orthogonal voltage system (v' and its quadrature qv').

Two cases have been analyzed in order to test the effectiveness of the proposed method for offset rejection. In the first case a 5% (of voltage amplitude) offset has been introduced in the measured voltage (Fig. 8 and Fig. 9). For the second case a 25% offset has been introduced in order to test the robustness of the proposed method (Fig. 10 and Fig. 11). The plots (a) of the Fig. 8 - Fig. 11 show the voltage waveform and its amplitude, estimated by the OSG-SOGI. The plots (b) of the Fig. 8 - Fig. 11 contain the orthogonal voltage system (v' and qv'), generated by the OSG-SOGI. The plots (c) of the Fig. 8 - Fig. 11 represent the estimated frequency of the voltage signal using the PLL based on OSG-SOGI.

The Fig. 8 and Fig. 10 show the results obtained using the standard OSG-SOGI structure presented in Fig. 3, while the Fig. 9 and Fig. 11 show the results obtained using the improved OSG-SOGI structure as drown in Fig. 5. As it can be noticed from Fig. 8 (standard OSG-SOGI), a 5% offset in the voltage highly affects the estimation of the frequency and amplitude of the voltage (2 Hz ripple in the estimated frequency and 25 V ripple in the estimated amplitude). On the contrary, using the offset rejection method as presented in Fig. 5, the estimated frequency and amplitude of the voltage is not affected by the 5% voltage offset (Fig. 9). Moreover, the offset rejection method proved to be very efficient and robust even when using a 25% offset in the voltage as presented in Fig. 11.



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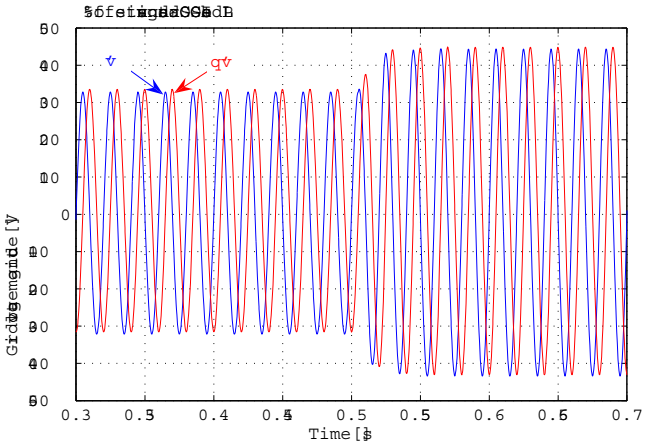

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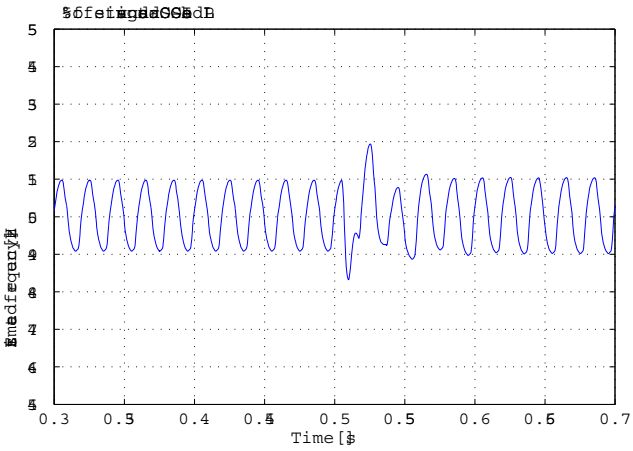
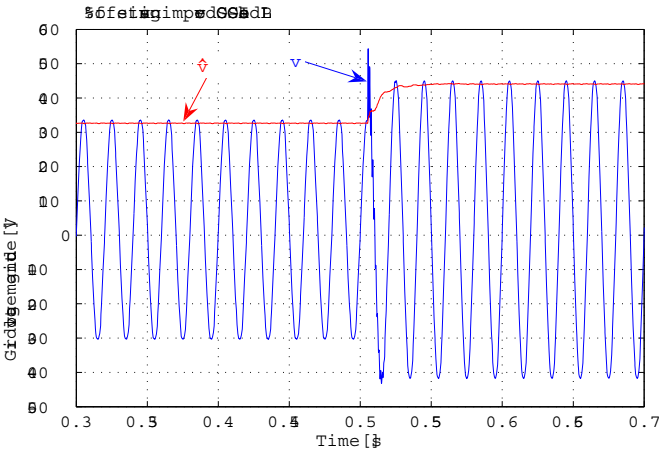
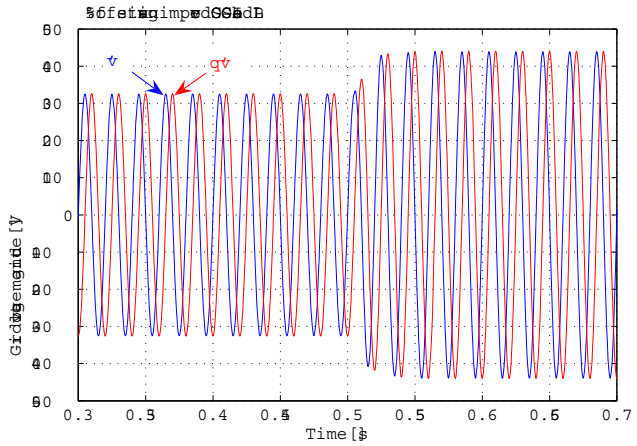


c)

Fig. 8. Obtained results using standard OSG-SOGI structure (Fig. 3) under a 5% voltage offset: a) amplitude estimation; b) generated orthogonal voltage system; c) frequency estimation.



a)



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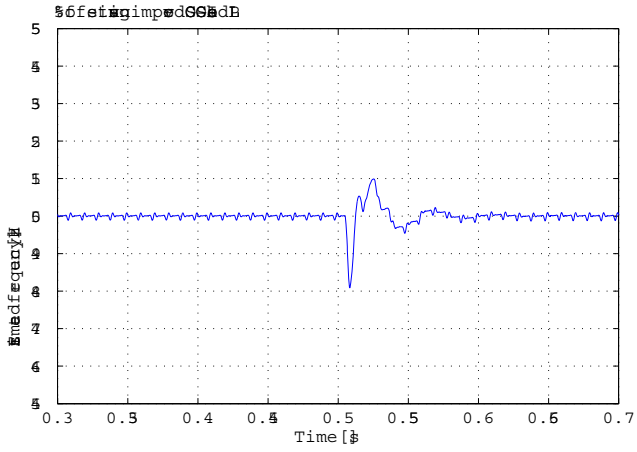
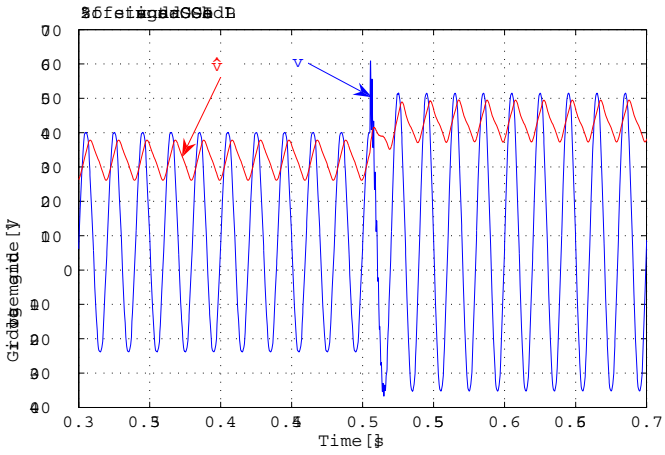


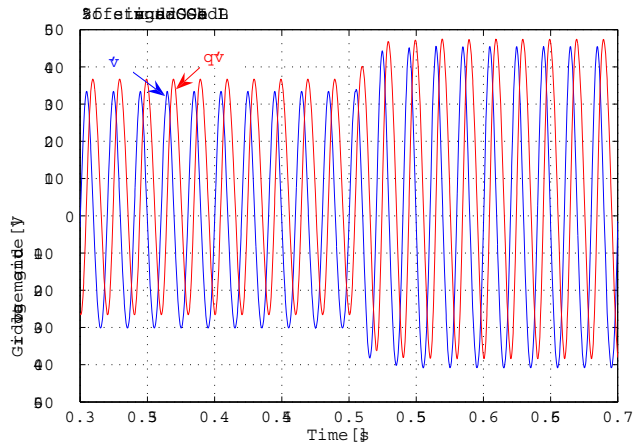
c)

Fig. 9. Obtained results using improved OSG-SOGI structure (Fig. 5) under a 5% voltage offset: a) amplitude estimation; b) generated orthogonal voltage system; c) frequency estimation.

As it can clearly be seen from Fig. 10, the error generated by the voltage offset has the same frequency with the fundamental frequency of the voltage, thus being very difficult to filter it out using an extremely low band-width PI controller for the PLL, as mentioned in [3].



a)



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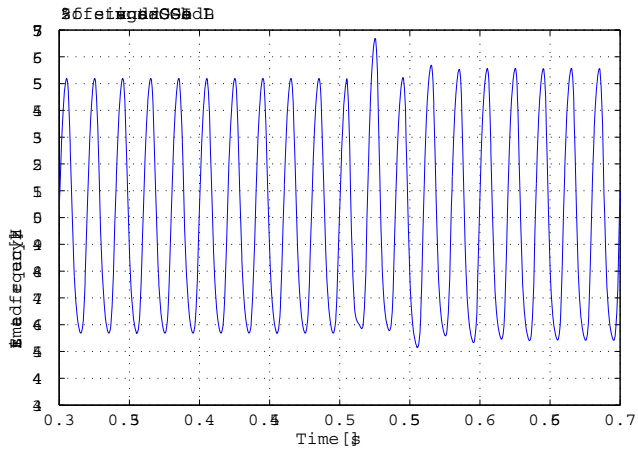
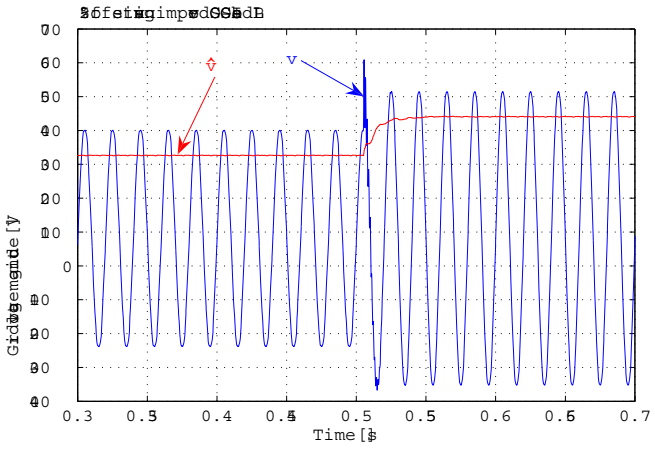


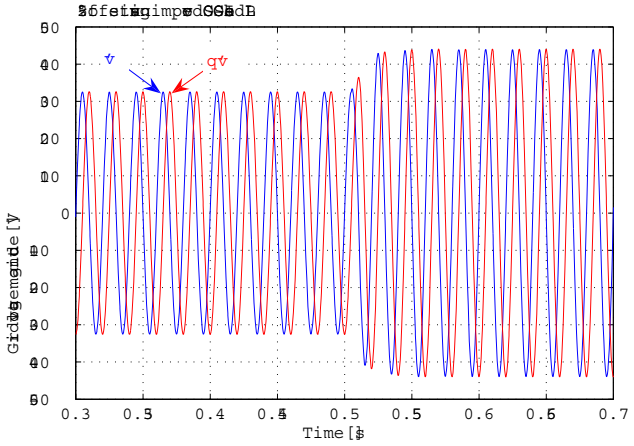
c)

Fig. 10. Obtained results using standard OSG-SOGI structure (Fig. 3) under a 25% voltage offset: a) amplitude estimation; b) generated orthogonal voltage system; c) frequency estimation.

A voltage swell of 35% has been deliberately created in order to show that the dynamic of the OSG-SOGI structure is not affected by the offset rejection method proposed in Fig. 5. A 2.5% voltage Total Harmonic Distortion (THD) was used for the experimental results presented in Fig. 8 - Fig. 11.



a)



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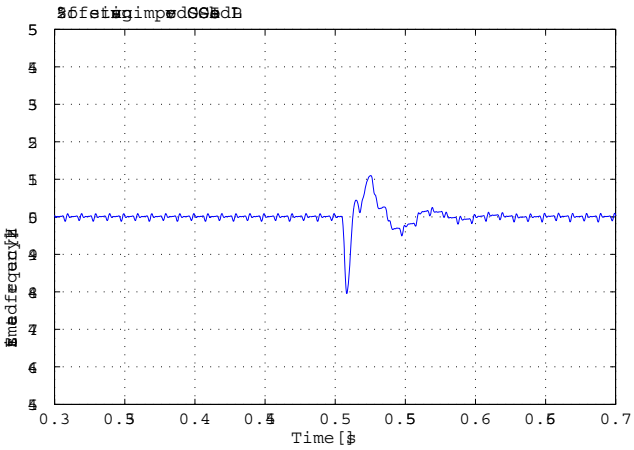

c)

Fig. 11. Obtained results using improved OSG-SOGI structure (Fig. 5) under a 25% voltage offset: a) amplitude estimation; b) generated orthogonal voltage system; c) frequency estimation.

V. Conclusions

An important issue associated with accurate grid voltage monitoring is the presence of an offset in the measured grid voltage. The majority of the PLL based synchronization systems are not able to reject the voltage offset which is typically introduced by the measurements and data conversion processes. Therefore, this paper presents an effective offset rejection method for grid-connected converters based on a Phase-Locked-Loop (PLL) technique. The proposed method is suitable for both, grid-connected systems (e.g. Photovoltaics, Wind Turbines) and power condition equipments (e.g. Uninterruptible Power Supply (UPS), active filters) which rely on PLL based synchronization.

The presented results proved the performances and robustness of the proposed offset rejection method.

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