Letters

DC Offset Error Compensation for Synchronous Reference Frame PLL in Single-Phase Grid-Connected Converters

Seon-Hwan Hwang, Liming Liu, Hui Li, and Jang-Mok Kim

***Abstract*—This letter proposes a dc offset error compensation algorithm for synchronous reference frame phase-locked loop (PLL) in single-phase grid-connected converters. The errors generated from the grid voltage measurement circuits can be divided into dc offset and scaling errors. These errors may cause the undesirable periodic ripples with grid frequency in the synchronous reference frame PLL. As a result, the performance of the power conversion systems is degraded. In this letter, the effects of the dc offset and scaling errors are comprehensively analyzed based on the synchronous *dq* frame PLL. In particular, the dc offset error can be estimated and compensated by controlling the synchronous *d*-axis voltage in a PLL system to be zero. The proposed algorithm does not require any additional hardware and can be implemented by a simple proportional-integral controller and an integral operation. Experimental results are presented to demonstrate the effectiveness of the proposed dc offset error compensation algorithm.**

***Index Terms*—DC offset error, integral operation, phase-locked loop (PLL), scaling error, single-phase grid-connected converter (SPGC), synchronous *d*-axis voltage.**

I. Introduction

THE single-phase grid-connected converter (SPGC) is very important for renewable energy conversion systems such as photovoltaic, fuel cells, and batteries, especially in residential applications [1]–[3]. The phase-locked loop (PLL) as a key component in grid-connected systems will impact the power quality, stability, and reliability of power conversion systems [4]–[16].

Previous studies mostly deal with the performance improvements of PLL systems under distortions and transients such as harmonics, frequency variations, and phase shifts in the grid voltage [4]–[13]. However, the errors caused by the measurement path of the grid voltage also seriously influence the performance of PLL [14]–[16]. Due to the inherent issues in the PLL, the dynamic performance of the SPGC systems may be degraded. In general, the grid voltage is measured through voltage sensors, low-pass filters to remove switching noise, and A/D converters. Because of the nonlinearity of the voltage sensors, the thermal drift of the analog elements, and the nonlinearity of the A/D converters, these errors from the grid voltage measurement circuits are inevitably generated even if the system may be well designed.

In this letter, only primary errors including dc offset and scaling errors are considered. Correspondingly, a novel dc offset error compensation algorithm of the measured grid voltage is proposed. The effects of the dc offset and scaling errors are comprehensively analyzed based on the PLL in synchronous *dq* frame. Accordingly, the effect of the scaling errors is verified to be negligible in the synchronous *dq* frame PLL, whereas the dc offset error results in the sine and cosine ripple components with grid frequency in the synchronous *dq*-axis voltages of the PLL. In the proposed algorithm, the dc offset error is readily estimated by using an integral operation according to the grid angle and is compensated by suppressing the ripples in the synchronous *d*-axis voltage to be zero. The PLL with the proposed algorithm, which is inherently suitable for the digital control for SPGC, generates good static and dynamic performance. Experimental results were given to verify the validity of the proposed dc offset error compensation algorithm.

II. Effects of DC Offset and Scaling Errors in Grid Voltage Measurement

A. System Description

Fig. 1 describes the system configuration of the SPGC including power circuits and control algorithm [3], [4], which is used to implement the proposed algorithm in this letter.

Fig. 2 shows the block diagram of a traditional single-phase PLL based on the *dq* transformation. As shown in Fig. 2, the PLL is used to synchronize the output voltage of SPGC to the grid voltage so that the desired control can be achieved. A phase angle detection algorithm applied to a single-phase system is similar to the *dq* transformation of the three-phase variables [5], [7], [10], [11], [13], as shown in Fig. 2.

In this letter, the PLL for a single-phase system is implemented by generating a virtual voltage, which is delayed by 90° from the measured grid voltage and it can be achieved by using an all-pass filter as shown in Fig. 2 [5]. The measured

Manuscript received October 19, 2011; revised January 10, 2012; accepted February 24, 2012. Date of current version April 20, 2012. This work was supported by the National Science Foundation under Grant 1124658. Recommended for publication by Associate Editor C. (Letters AE) C. Mi.

S.-H. Hwang is with the Department of Electrical Engineering, Kyungnam University, Gyeongnam 631-701, Korea (e-mail: seonhwan@kyungnam.ac.kr).

L. Liu and H. Li are with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL 32310 USA (e-mail: liming@caps.fsu.edu; hli@caps.fsu.edu).

J.-M. Kim is with the School of Electrical Engineering, Pusan National University, Busan 609-735, Korea (e-mail: jmok@pusan.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2012.2190425

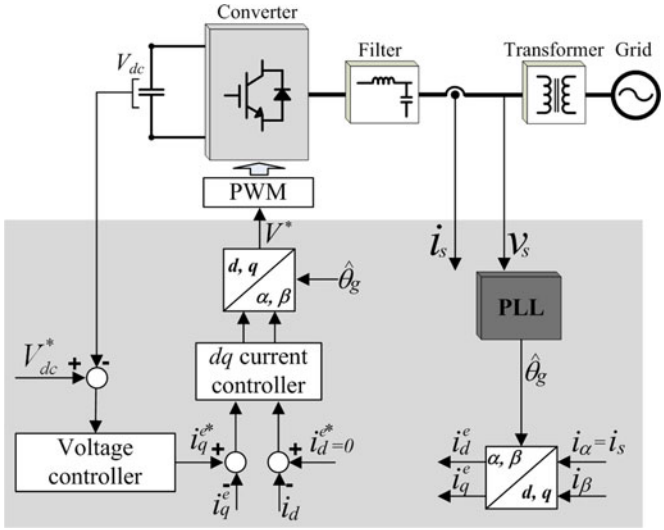

Fig. 1. Control block diagram of SPGCs.

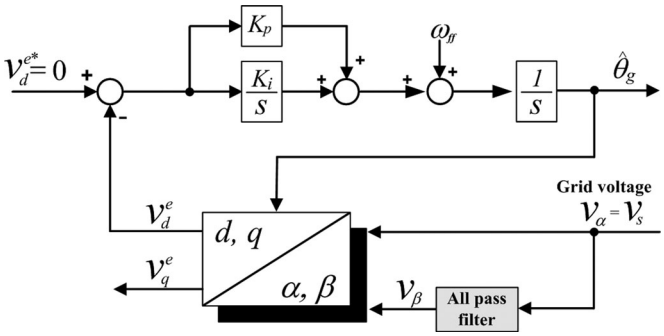

Fig. 2. Structure of a single-phase PLL based on *dq* transformation.

grid voltage v_s is set to be v_α and v_β is the virtual voltage through the all-pass filter. v_α and v_β are converted to v_d^e and v_q^e in the synchronous reference frame. ω_{ff} is the feed-forward grid frequency.

B. Effect of DC Offset and Scaling Errors

Ideally, the grid voltage without the dc offset and scaling errors can be defined by

$$v_s = -V_m \sin \omega_g t \tag{1}$$

where V_m is the peak value of the grid voltage. ω_g is the grid angular frequency.

However, the measured grid voltage includes the errors caused by the grid voltage measurement circuit as shown in Fig. 3. Fig. 3 represents the error factors in the grid voltage measurement path. Typically, the measured grid voltage is digitalized through matching circuits including voltage sensor, low-pass filter, and A/D converter. As a result, the dc offset and scaling errors may be generated from the voltage sensor itself and the nonlinear characteristics of the analog devices and A/D converters [15], [16].

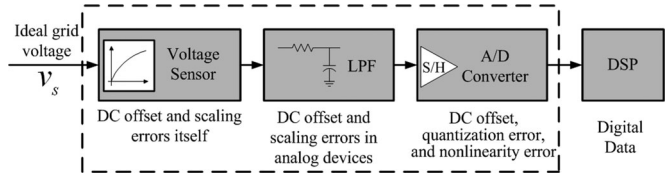

Fig. 3. Error factors in grid voltage measurement circuit.

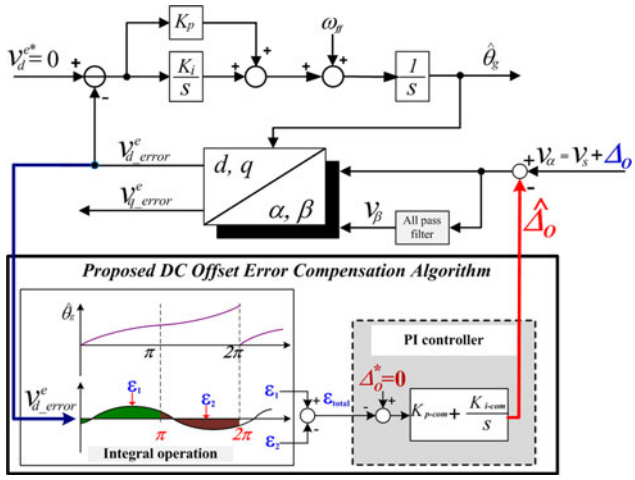

Fig. 4. Block diagram of the proposed dc offset error compensation algorithm.

Therefore, the measured grid voltage v_{s_error} including the dc offset and scaling errors can be derived by

$$v_{s\_error} = -(1+\Delta_S) V_m \sin \omega_g t + \Delta_O \tag{2}$$

where Δ_O and Δ_S are the amplitude of the dc offset and scaling errors, respectively.

Considering the aforementioned errors, the α-axis and β-axis voltages of the stationary reference frame in the PLL as shown in Fig. 4 can be given as

$$\begin{cases} v^s_{d\_error} = -(1+\Delta_S) V_m \sin \omega_g t + \Delta_O \\ v^s_{q\_error} = \quad (1+\Delta_S) V_m \cos \omega_g t + \Delta_O \end{cases} \tag{3}$$

where $v^s_{d\_error}$ is v_α and $v^s_{q\_error}$ is v_β as shown in Fig. 4.

In order to obtain the estimated grid angle, frequency, and amplitude, the stationary *dq*-axis voltages are transformed by using $\alpha\beta$ to *dq* transformation matrix as shown in Fig. 4. The transformation matrix with the estimated grid angle can be obtained as follows:

$$\begin{bmatrix} v^e_{d\_error} \\ v^e_{q\_error} \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \begin{bmatrix} v^s_{d\_error} \\ v^s_{q\_error} \end{bmatrix}$$
$$= \begin{bmatrix} \cos\hat{\theta}_g & \sin\hat{\theta}_g \\ -\sin\hat{\theta}_g & \cos\hat{\theta}_g \end{bmatrix} \begin{bmatrix} -(1+\Delta_S) V_m \sin \omega_g t + \Delta_O \\ (1+\Delta_S) V_m \cos \omega_g t + \Delta_O \end{bmatrix} \tag{4}$$

where $\hat{\theta}_g$ is the estimated grid angle and $\theta_g = \omega_g t$ is the real grid angle.

The synchronous dq-axis voltages including the dc offset and scaling errors can be calculated as

$$\begin{cases} v^e_{d\_\text{error}} = -(1+\Delta_S)V_m \sin\left(\theta_g - \hat{\theta}_g\right) \\ \qquad\qquad +\Delta_O \cos\hat{\theta}_g + \Delta_O \sin\hat{\theta}_g \\ v^e_{q\_\text{error}} = (1+\Delta_S)V_m \cos\left(\theta_g - \hat{\theta}_g\right) \\ \qquad\qquad -\Delta_O \sin\hat{\theta}_g + \Delta_O \cos\hat{\theta}_g. \end{cases} \tag{5}$$

It can be seen from (5) that when the grid angle error between θ_g and $\hat{\theta}_g$ is small, the synchronous dq-axis voltages including the dc offset and scaling errors can be rewritten as

$$\begin{cases} v^e_{d\_\text{error}} = \Delta_O \cos\hat{\theta}_g + \Delta_O \sin\hat{\theta}_g \\ v^e_{q\_\text{error}} = V_m + \Delta_S V_m - \Delta_O \sin\hat{\theta}_g + \Delta_O \cos\hat{\theta}_g. \end{cases} \tag{6}$$

From (6), the synchronous d- and q-axis voltages have the same frequency components compared with the grid frequency. In addition, the ripple components in the synchronous dq-axis voltages basically are determined by sine and cosine terms with the estimated grid frequency and the dc offset error. In particular, the distorted synchronous d-axis voltage causes the distorted grid angle and grid frequency in the PLL system. Moreover, the synchronous d-axis voltage does not include the ripple components related to the scaling error as shown in (6). In other words, the scaling error does not cause the distortion in the estimated grid angle and estimated grid frequency but affects the estimated grid voltage amplitude related to the synchronous q-axis voltage. It only relates to the feed-forward term at the output of the current controller [3]. Therefore, the only dc offset error is considered to reduce the distortion of the estimated grid angle and grid frequency in this letter.

III. Proposed DC Offset Error Compensation Method

From (6), the synchronous d-axis voltage is composed of the sine and cosine terms with the dc offset error. Especially, the frequency component of the synchronous d-axis voltage is the same as the grid frequency. Therefore, the dc offset error can be easily estimated by using integral operation according to specific grid angle. As a result, the dc offset error can be compensated by reducing the ripple components of the synchronous d-axis voltage in a PLL.

Fig. 4 shows the block diagram of the proposed dc offset error compensation method. The synchronous d-axis voltage is directly used for the input signal of the proposed method as shown in Fig. 4. The integral values ε_1 and ε_2 can be obtained by the integral operation of the synchronous d-axis voltage according to the estimated grid angle which divides into two parts $[0, \pi]$ and $[\pi, 2\pi]$, respectively. The integrated results according to the specific grid angle can be given by

$$\begin{cases} \varepsilon_1 = \displaystyle\int_0^{\pi} v^e_{d\_\text{error}} d\hat{\theta}_g = \int_0^{\pi} \left(\Delta_O \cos\hat{\theta}_g + \Delta_O \sin\hat{\theta}_g\right) d\hat{\theta}_g \\ \qquad\qquad = -2\Delta_O \\ \varepsilon_2 = \displaystyle\int_{\pi}^{2\pi} v^e_{d\_\text{error}} d\hat{\theta}_g = \int_0^{\pi} \left(\Delta_O \cos\hat{\theta}_g + \Delta_O \sin\hat{\theta}_g\right) d\hat{\theta}_g \\ \qquad\qquad = 2\Delta_O. \end{cases} \tag{7}$$

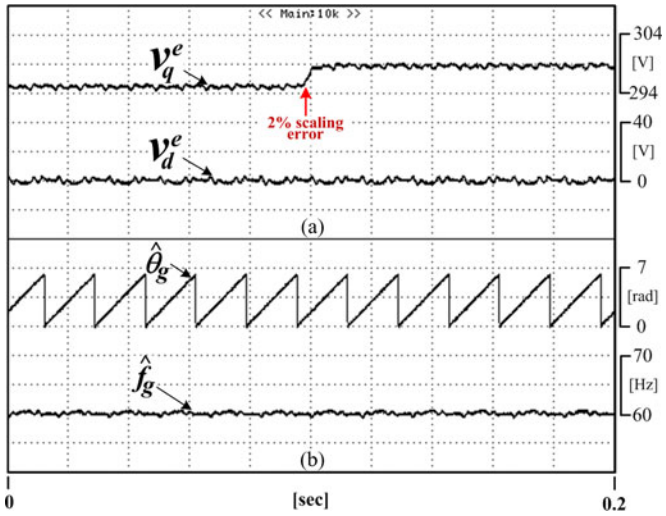

Fig. 5. Experimental results under a 2% scaling error of grid voltage. (a) Synchronous dq-axis voltages. (b) Estimated grid angle and frequency.

The difference ε_{total} between ε_1 and ε_2 can be obtained as follows:

$$\varepsilon_{\text{total}} = \varepsilon_1 - \varepsilon_2 = -4\Delta_O. \tag{8}$$

Applying the integral operation at the synchronous d-axis voltage, the cosine term in the synchronous d-axis voltage is automatically removed as shown in (7). The proposed compensator consists of two parts as shown in Fig. 4. The first part is the integrator used for estimating the dc offset error from the synchronous d-axis voltage according to the estimated grid angle $\hat{\theta}_g$. The other is the proportional-integral (PI) controller to remove the dc offset error Δ_O. The PI gains of the proposed method affect the convergence rate of the estimated dc offset error $\hat{\Delta}_O$. In addition, the output of the proposed PI controller is continuously updated to get the constant of the exact dc offset error Δ_O.

IV. Experimental Results

The proposed dc offset error compensation method was verified on a 1-kW SPGC operating at 10 kHz with a DSP-based control system.

Fig. 5 shows the experimental results considering the variation of the scaling error. As shown in Fig. 5, despite a change of 2% scaling error in the grid voltage, the synchronous dq-axis voltages and the estimated grid angle and grid frequency do not have any ripple components. Therefore, the scaling error does not affect the PLL system as can be seen from (6).

Figs. 6 and 7 show the synchronous dq-axis voltages, estimated grid angle, and grid frequency from the PLL under a 2% dc offset error of the grid voltage without and with the proposed method, respectively. Without the compensation algorithm, the estimated grid frequency and synchronous dq-axis voltages have the same ripples with the grid frequency as shown in Fig. 6. It is very difficult to filter them out using an extremely low bandwidth [3].

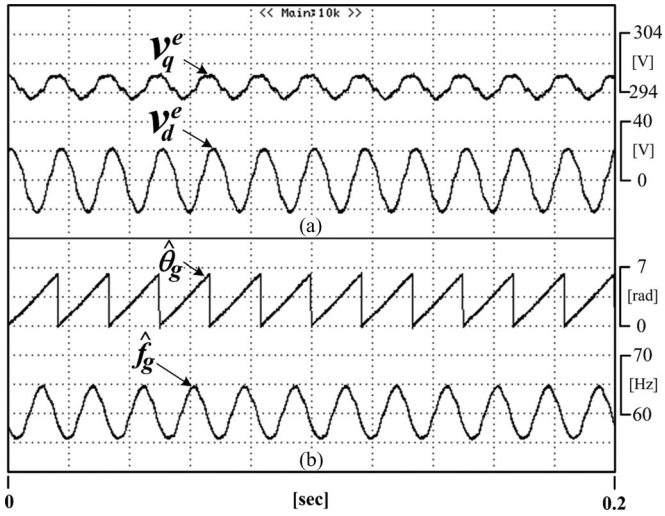

Fig. 6. Experimental results without the proposed method under a 2% dc offset error of grid voltage. (a) Synchronous *dq*-axis voltages. (b) Estimated grid angle and frequency.

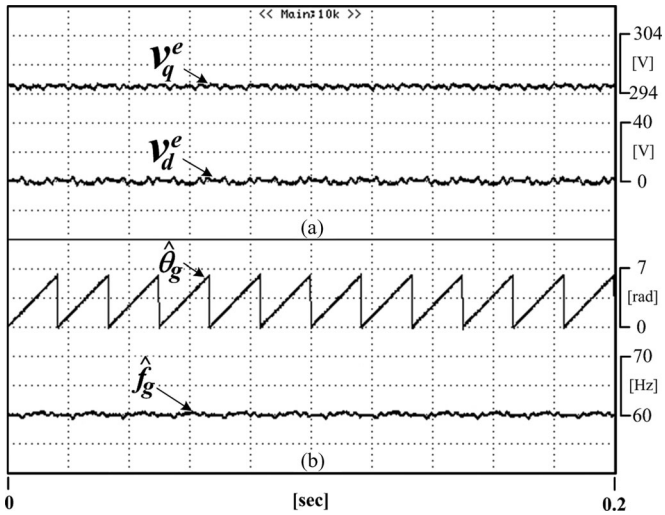

Fig. 7. Experimental results with the proposed method under a 2% dc offset error of grid voltage. (a) Synchronous *dq*-axis voltages. (b) Estimated grid angle and frequency.

However, the ripples of the estimated grid frequency and synchronous *dq*-axis voltages are considerably reduced by applying the proposed algorithm as shown in Fig. 7.

Fig. 8 illustrates the effectiveness of the proposed dc offset error compensation method according to the variation of the dc offset errors. In Fig. 8, the amplitudes of the synchronous *d*-axis voltage ripple and the estimated grid frequency ripple with and without the proposed method are compared.

As shown in section "a" of Fig. 8, v_{ds}^e and $\hat{f}_g$ have serious ripples when the offset error changes from 0 to 2% without the proposed method. After compensation in section "b" of Fig. 8, the ripples of v_{ds}^e and $\hat{f}_g$ are significantly decreased by subtracting the estimated dc offset value $\hat{\Delta}_o$ from the proposed PI controller as shown in Fig. 4. Moreover, the proposed controller can continuously generate accurate $\hat{\Delta}_o$ to track the change ranging from 2% to 4% and then back to 1%. As a result, the proposed

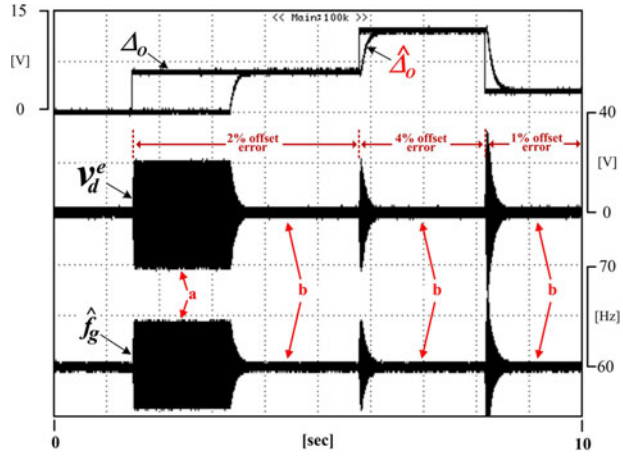

Fig. 8. Experimental results under the change of the dc offset error in grid voltage. (a: without proposed method and b: with proposed method).

algorithm can be effectively applied to both steady and transient states.

V. Conclusion

A new dc offset error compensation algorithm for the synchronous reference frame PLL of the SPGC systems was proposed. The effects of the dc offset and scaling errors caused by the grid voltage measurement circuits were mathematically analyzed based on a synchronous reference frame PLL. Due to the dc offset error, the synchronous *dq*-axis voltages in the PLL based on *dq* transformation had the sine and cosine terms which are fundamental grid frequency. Therefore, the synchronous *d*-axis voltage was directly used for the input signal of the proposed compensator to detect the dc offset error because there is no effect of the scaling error in the synchronous *d*-axis voltage. As a result, the dc offset error was easily estimated by an integral operation of the synchronous *d*-axis voltage. The proposed algorithm provided no additional hardware and reduced the computation burden significantly. The effectiveness of the proposed algorithm was verified through the several experimental results.

References

[1] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[3] U. A. Miranda, M. Aredes, and L. G. B. Rolim, "A *dq* synchronous reference frame control for single-phase converters," in *Proc. Power Electron. Spec. Conf.*, 2005, pp. 1377–1381.

[4] M. Ciobotaru, V. G. Agelidis, R. Teodorescu, and F. Blaabjerg, "Accurate and less-disturbing active antiislanding method based on PLL for grid-connected converter," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1576–1584, Jun. 2010.

[5] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Bosventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," in *Proc. 39th IEEE Ind. Appl. Soc. Annu. Meet. Ind. Appl. Conf.*, 2004, vol. 4, pp. 2259–2263.

[6] S. K. Chung, H. B. Shin, and H. W. Lee, "Precision control of single-phase PWM inverter using PLL compensation," in *Proc. IEE Electr. Power Appl.*, Mar. 2005, vol. 152, no. 2, pp. 429–436.

[7] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.

[8] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008.

[9] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. Power Electron. Spec. Conf.*, 2006, pp. 1–6.

[10] D. Velasco, C. Trujillo, G. Garcera, and E. Figueres, "An active anti-islanding method based on phase-PLL perturbation," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1056–1066, Apr. 2011.

[11] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-locked loops noise reduction via phase detector implementation for single-phase systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2482–2490, Jun. 2011.

[12] S. Shinnaka, "A novel fast-tracking D-estimation method for single-phase signals," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1081–1088, Apr. 2011.

[13] S. J. Lee, J. K. Kim, and S. K. Sul, "A new phase detecting method for power conversion systems considering distorted conditions in power system," in *Proc. 34th IEEE Ind. Appl. Soc. Annu. Meet. Ind. Appl. Conf.*, 1999, vol. 4, pp. 2167–2172.

[14] S. K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431–438, May 2000.

[15] M. Ciobotaru, R. Teodorescu, and V. G. Agelidis, "Offset rejection for PLL based synchronization in grid-connected converters," in *Proc. 23rd Annu. IEEE Appl. Power Energy Conf. Expo.*, 2008, pp. 1611–1617.

[16] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 78–86, Jan. 2012.