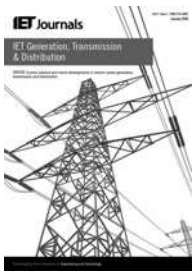
Published in IET Generation, Transmission & Distribution
Received on 22nd January 2013
Revised on 12th April 2013
Accepted on 5th May 2013
doi: 10.1049/iet-gtd.2013.0041



ISSN 1751-8687

Fast and robust software-based digital phase-locked loop for power electronics applications

Ayhan Özdemir[1], İrfan Yazici[1], Cabir Vural[2]

[1]*Department of Electrical–Electronics Engineering 54187, Sakarya University, Esentepe, Sakarya 54187, Turkey*
[2]*Department of Electrical–Electronics Engineering, Marmara University, Göztepe, İstanbul 34722, Turkey*
E-mail: iyazici@sakarya.edu.tr

Abstract: In this study, a fast and fully software-based algorithm for digital phase-locked loop (PLL) is proposed via a new hybrid approach in software and hardware by using an advanced digital signal processor architecture. The proposed algorithm is robust against line disturbances such as phase-angle jump, voltage sag, third harmonic injection, multi-zero crossing and step change in frequency at the input voltage. Performance and robustness of the proposed method are investigated through experimental studies. Furthermore, it is compared with three different PLL algorithms in detail to show its superiority over existing methods.

1 Introduction

The number of distributed generation units such as wind generation unit, photovoltaic generation unit, microturbine generation unit and power conditioning equipments such as static VAR compensator, active power filters, uninterruptible power supplies (UPSs) etc. in the electric power systems are growing rapidly. The accurate information about phase angle and frequency of the utility voltage has crucial importance for proper operations of all these equipments in grid-connected condition [1–11].

Existing methods used to synchronise the above-mentioned equipment to the grid can be broadly categorised into open-loop and closed-loop methods [2]. Open-loop methods based on space vector filters, Kalman filters, fast Fourier transform, recursive weighted least-square estimation are affected under the distorted conditions of the input signal [5].

The phase-locked loop (PLL), closed-loop method, is the most commonly preferred technique in synchronisation of the grid-connected systems under distorted conditions owing to its hardware (analogue) and software (digital) -based implementations [5, 6, 12]. Owing to some drawbacks of analogue implementation such as steady-state phase error caused by the leakage current of the low-pass filter (LPF) [13] and inflexibility seen in hardware-based implementation, digital implementation is more preferred and many valuable studies have contributed to the literature in recent years [1–11, 14, 15].

Digital PLL-based synchronisation structures generally present good performance even if the synchronisation signal is affected by harmonics, voltage sags and swells, noise and commutation notches [2, 5]. Therefore digital PLL can be considered as one of the key blocks of the modern power electronics-based systems as stated above.

In study [12], a robust PLL structure based on the instantaneous real and imaginary power theory (pq theory) under distorted utility conditions was presented. A modified synchronous reference frame (SRF) -based PLL was discussed in [1] to overcome traditional SRF's degeneracy. In reference [7], a decoupled double SRF-based PLL that eliminates detection errors of conventional SRF was introduced. An enhanced PLL (EPLL) structure that increases the immunity and insensitivity of the system to noise and harmonics was employed in [2]. In [4], a lead compensation and selective band-stop filtering-based PLL having a fast transient response was developed. In reference [6], another PLL structure having fast transient response based on modulating functions and orthogonal system generator was proposed. A modified power-based PLL (pPLL) structure was proposed in [8] to overcome the drawbacks associated with the pPLL. Multiple delayed signal cancellation (DSC) operator was discussed in [9] to eliminate undesired harmonics of input signal. However, increasing loop time as a result of cascaded DSC operators affects the stability and dynamics of the whole PLL structure negatively. A PLL topology with reduced number of calculations having adaptive structure for polluted single-phase grids was devised in [10]. In [11], park-PLL and second-order generalised integrator-PLL structures were analysed and a systematic design approach for tuning of the PLL parameters were proposed. Performance of the three single-phase PLL structures designed for UPS applications, pPLL, park PLL and EPLL were investigated comparatively in [3].

In this study, a software-based digital PLL algorithm is proposed based on the work of Giroux and Sybille [16], which is available under the name single-phase PLL block in MATLAB/Simulink 6.5/ SimPowerSystems Toolbox.

The PLL block in [16], which is preferred for its superior robustness, has the following disadvantages:

1. It is developed for simulation studies and it has both analogue and digital blocks. Therefore it is impracticable in real-time applications.
2. The classical variable time-delay algorithm in the frequency discriminator block increases computational load significantly. For this reason it cannot be used for many power electronic applications. Consequently, it is not optimised for real-time implementations.
3. The lowest possible running time cannot be obtained even if problems 1 and 2 are solved. This is because the codes are run from flash memory in classical digital signal processor (DSP) architecture. Note that the reading data from random access memory (RAM) is faster than reading data from flash memory.

In this study, these disadvantages have been removed by the following modifications:

1. The digital counterparts of the analogue blocks in the reference PLL in [16] are designed. As a result a fully digital and practicable PLL structure given in Fig. 1 is obtained for real-time implementations.
2. A new algorithm, called fast variable time delay that decreases the computation load dramatically is developed.
3. The DSP used in this study has an architecture that allows running the codes from RAM. The software is created by taking into consideration and all the codes related to Fig. 1 are run from RAM. Hence, the running time is decreased by half.

In summary, a software-based PLL structure that is fully digital, fast, robust and applicable in real-time application is developed in this study. Dynamic performance of the proposed algorithm is investigated through real-time experimental studies for several line disturbances such as phase-angle jump, voltage sag, third harmonic injection, multi-zero crossing and step change in frequency at the input voltage $v_i(t)$. Results show that the proposed PLL algorithm is faster and more robust against distortions compared with the existing methods given in [3]. Studies also show that the proposed algorithm gives the second best performance in case of a +5 Hz step change in frequency in the input signal. Furthermore, the proposed method is also shown to provide a high performance when the input signals have multi-zero crossing, which represent an extreme case in power systems. In addition, computational load of the proposed and the existing algorithms described in [3] were compared in the same DSP family. The results show that the proposed method is the fastest algorithm having 2.35 μs running time.

2 Proposed method

In this study, a fully software-based fast digital PLL algorithm is developed. The algorithm is based on the single-phase discrete PLL structure existing in Simulink V6.5 developed by Giroux and Sybille [16]. Speed of the PLL structure of Giroux and Sybille is significantly increased by a new hybrid approach. The proposed algorithm is suitable for use in real-time applications of power electronic circuits. Block diagram corresponding to the developed digital PLL is given in Fig. 1.

As it is clear from Fig. 1, the reference input voltage $v_i(t)$ is obtained from only one phase in the PLL architecture. Three voltage $V_j(t), j \in a, b, c$ synchronised to the input voltage $v_i(t)$ are generated at the output. The sub-blocks in Fig. 1 are discussed below.

2.1 Phase detector block

The discrete-time reference input signal $v(k)$ and the feedback signal $x(k)$ is given by:

$$v(k) = A\sin(w_1 k + \phi_1) \tag{1}$$

$$x(k) = B\cos(w_2 k + \phi_2) \tag{2}$$

From sub-block A in Fig. 1, we have

$$\begin{aligned} y(k) &= v(k)x(k) \\ y(k) &= AB\sin(w_1\, k + \phi_1)\cos(w_2\, k + \phi_2) \end{aligned} \tag{3}$$

$$\begin{aligned} y(k) = \frac{AB}{2}\{&\sin((w_1 + w_2)k + \phi_1 + \phi_2) \\ &+ \sin((w_1 - w_2)k + \phi_1 - \phi_2)\} \end{aligned} \tag{4}$$

where $k = 0, 1, 2, \ldots$

The high-frequency component in (4) is eliminated by passing $y(k)$ through a LPF. The output of the LPF is

$$e(k) = \frac{AB}{2}\sin((w_1 - w_2)k + \phi_1 - \phi_2) \tag{5}$$

After a sufficiently long time, the transient regime comes to an end and the PLL is nearly locked at the centre frequency, that is, $w_1 = w_2$. Then, (5) can be rewritten as

$$e(k) = \frac{AB}{2}\sin(\Delta\phi) \tag{6}$$

where $\Delta\phi = \phi_1 - \phi_2$. Note that $\Delta\phi(k) = \Delta w k$. Hence, (6)

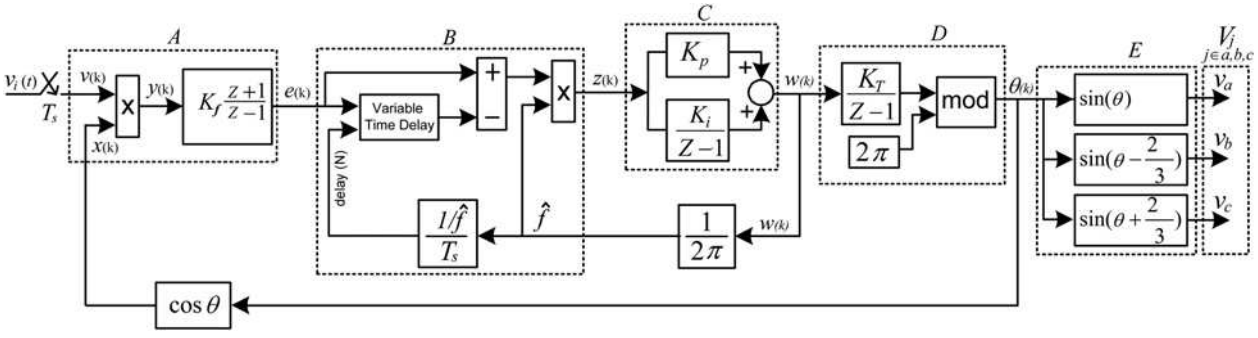


Fig. 1 *Block diagram of the developed PLL structure*

doi: 10.1049/iet-gtd.2013.0041

becomes

$$e(k) = \frac{AB}{2}\sin(\Delta wk) \tag{7}$$

The signal $e(k)$ in (7) is in the form $A_c \sin(\Delta wk)$ and can be considered as a frequency-modulated (FM) signal [17]. On the other hand, an amplitude modulation (AM) signal is preferable with respect to FM in controller design process. Therefore a frequency discriminator is used for FM to AM conversion [17, 18].

2.2 Frequency discriminator block

From sub-block B in Fig. 1, we can write

$$z(k) = \left\{e(k) - e\left((k-1)\hat{T}\right)\right\}\frac{1}{\hat{T}} \tag{8}$$

where $e(k)$ is the current value, $\hat{T}$ is the estimated period of input voltage and $e\left((k-1)\hat{T}\right)$ is the delayed signal by $\hat{T}$. Equation (8) can be considered as derivative $e(k)$ with respect to $\hat{T}$, that is

$$z(k) = \frac{\mathrm{d}e(k)}{\mathrm{d}\hat{T}} \tag{9}$$

Substituting $e(k)$ given in (7) in (9) gives

$$z(k) = AB\frac{\Delta w}{2}\cos(\Delta wk) \tag{10}$$

One of the most important blocks in the PLL architecture given in Fig. 1 is the variable time-delay structure for the frequency discriminator. In the classical variable time-delay structure shown in Fig. 2, $x(k)$, $x(k-1)$ and $x(k-N)$ represent the current, previous and N previous values of the signal, respectively. In this case the total transmission delay is

$$D = NT_s \tag{11}$$

where N is the variable delay coefficient and T_s is the constant sampling period.

The reason for calling it variable time-delay structure is that the coefficient N determining the total delay D changes between N_{min} and N_{max} determined during the design until the PLL is locked to the fundamental component of the input signal $v_i(t)$. Once the PLL is locked to the input signal, N and in turn delay time D take a constant value depending on the input signal frequency. As stated before, N_{min} and N_{max} values are determined during the design process according to the ranges of operating frequency f_{Lock} to which the PLL locks and the sampling period T_s.

The classical variable time-delay structure shown in Fig. 2 is not suitable for use in real-time applications of power electronics-based systems operating at high switching frequencies because of long computation time. For this reason, a new variable time-delay structure is developed in this study. It is discussed in detail in Section 3.

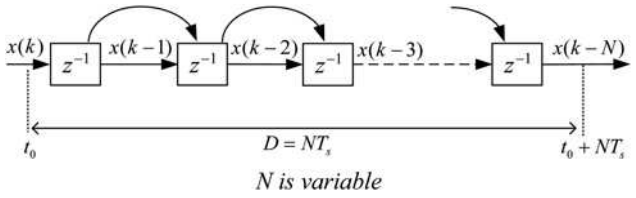


Fig. 2 *Classical variable time-delay structure*

2.3 Proportional-integral (PI) controller block

The discrete-time PI controller denoted by sub-block C in Fig. 1 is described as [19]

$$G_{PI}(z) = K_p + K_i\frac{1}{z-1} \tag{12}$$

The output of the PI gives the angular frequency $w(k)$.

2.4 Voltage controlled oscillator (VCO) block

Recall that

$$\frac{\mathrm{d}\theta(k)}{\mathrm{d}t} = w(k) \text{ or } \theta(k) = \int w(k)\,\mathrm{d}k \tag{13}$$

Therefore VCO can be considered as an integrator [3].

2.5 Output blocks

These blocks used $\theta(k)$ as input and generate the three-phase reference signals $V_j(k), j \in a, b, c$ synchronise to input signal $v(k)$ when phase lock is established.

3 Proposed variable time-delay algorithm

As discussed in Section 2, the new hybrid approach developed to decrease the computation time of the PLL algorithm given in Fig. 1 consists of two parts:

1. Instead of running the PLL codes from program memory (FLASH), the PLL codes are moved to RAM and are run from RAM after power on reset as shown in Fig. 3 by using the TMS320F2810 DSP family architecture property. In this way, the proposed PLL code running time is decreased approximately by half (from 4.56 to 2.35 µs) resulting in significant speed advantage,
2. Variable assignments for the variable time-delay algorithms are made using the new approach developed in this study leading to savings in computation time. Significant decrease in running time allows the PLL algorithm shown in Fig. 1 to be applicable to power electronics, measurement and control systems with high switching/sampling frequencies. Block diagram and flowchart corresponding to the proposed hybrid method are given in Fig. 3.

In this study, locking frequency range for the PLL is 45 Hz $\leq f_{Lock} \leq$ 60 Hz, sampling period is $T_s = 50$ µs. Accordingly, N_{min} and N_{max} are calculated as $N_{min} = 330$, $N_{max} = 440$, that is $3300 < N < 5440$. The initial value of N is determined from the fundamental frequency of the input signal to which the PLL is locked.

4 Experimental studies

In a power system, the voltage signal is distorted mainly by harmonic injection, voltage sag, phase and frequency

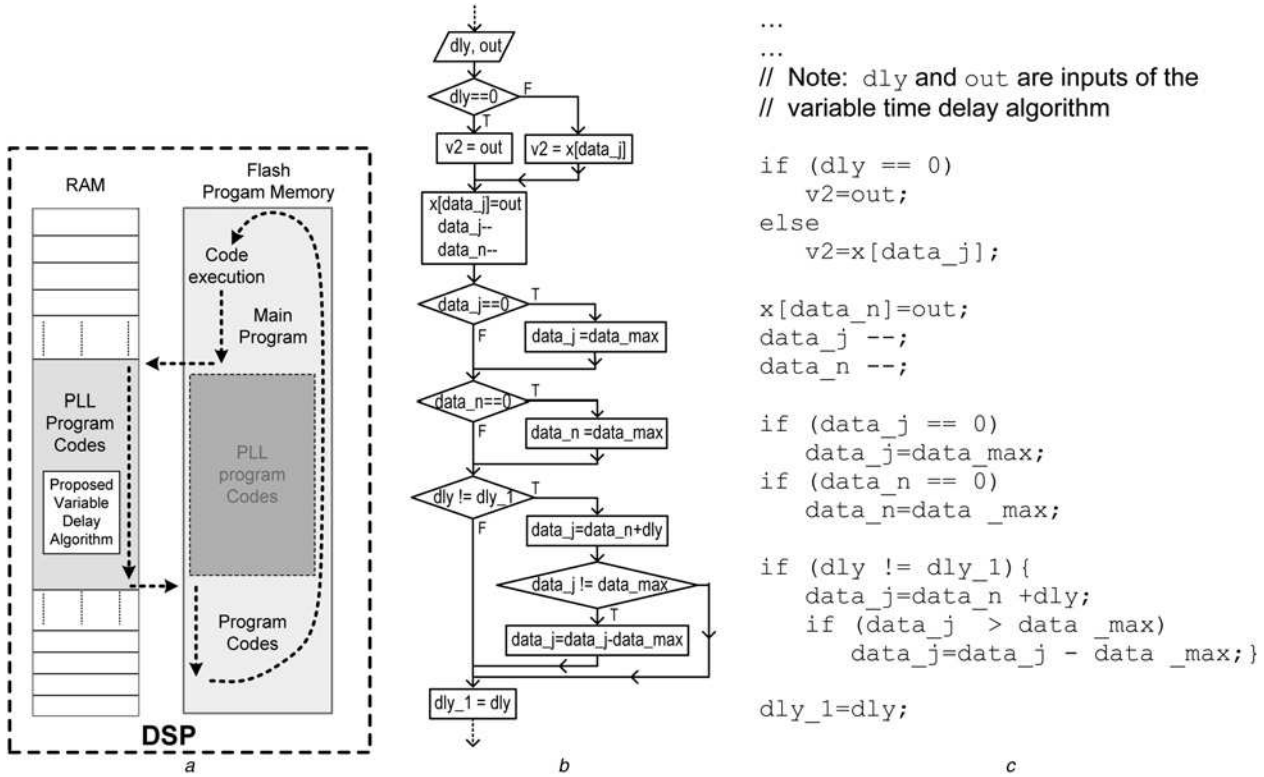


Fig. 3 *Block diagram and flowchart corresponding to the proposed hybrid method*

a Block diagram of proposed hybrid method
b Flowchart
c Program code in C of the proposed variable time-delay algorithm

deviation, noise, swells, notches etc. [5, 13]. Therefore the performance of the PLL designed by the proposed variable time delay is investigated through real-time experimental studies when the input voltage $v_i(t)$ is distorted by some of these conditions such as frequency varying, phase-angle jump, input voltage sag and third harmonic injection. Furthermore, the performance of the proposed method is compared with three different PLL algorithms existing in the literature.

Simplified block diagram and picture of the experimental test bench for the real-time studies is given in Figs. 4*a* and *b*, respectively, and the coefficients used are specified in Table 1.

Table 1 Coefficients for real-time experiments

Coefficient	Value
K_f	3.5×10^{-5}
K_p	58
K_i	9.65
K_T	1
T_s	50 μs

First, the reference PLL structure in [16] modified to be fully digital in this study is implemented on a high-performance DSP (TMS320F2810, 32-bit, 150 MHz)

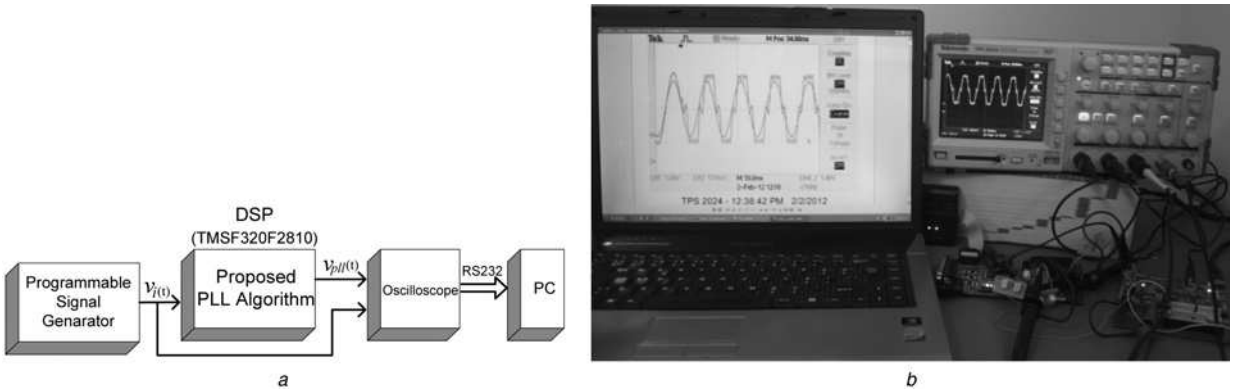


Fig. 4 *Simplified block diagram and picture of the experimental test bench for the real-time studies*

a Simplified block diagram
b Picture of the test bench

doi: 10.1049/iet-gtd.2013.0041

experimentally, having classical variable time-delay algorithm. The execution time of all the algorithms given in Fig. 1 was observed to have ~29 μs computation load on TMS320F2810 DSP.

As stated before, PLL is a crucial complementary circuit for an efficient operation of most power electronics-based systems (UPS, grid synchronised devices, IM drivers etc.). On the other hand, there are various basic tasks (measurement, assessment, running the control algorithm, generation of desired pulse-width modulated signals and etc.) that the DSP used in these systems need to perform during the sampling interval $T_s = 1/f_s$. Hence, 29 μs spent for the classical PLL causes increase of sampling period or equivalently decrease of switching frequency f_s when the other operations are taken into account.

A new variable time-delay algorithm is derived in Section 3 in order to decrease the computational load of the investigated PLL. Furthermore, the program codes are run from RAM instead of the flash memory. As a result, the proposed hybrid method was run on the same DSP in real time and the running time was decreased by 12 times to 2.35 μs compared with the classical PLL structure given in Fig. 1. As such, a software-based PLL algorithm that can be used in real-time applications was constructed.

4.1 Performance and robustness tests

Deviation of the phase angle and the estimated frequency $\hat{w}$ responses to a 40° phase-angle jump, 30% voltage sag, 15% third harmonic injection and a +5 Hz step change in frequency at the input voltage $v_i(t)$ at t_0 are given in Figs. 5–8, respectively.

As seen from Fig. 5, the proposed method locks to the new condition with zero steady-state error within about 2.8 cycles ($\Delta t_1 \cong 56$ ms) response to a 40° phase-angle jump occurring at t_0.

On the other hand, the maximum deviation of the estimated frequency from the reference value (50 Hz) is about $f_{ov} = 3.2$ Hz and it reaches the reference value with zero steady-state error within about 4.1 cycles ($\Delta t_2 \cong 82$ ms).

It is clear from Figs. 6 and 7 that the proposed method is so insensitive to 30% voltage sag and 15% third harmonic injection into input voltage $v_i(t)$. The maximum phase error is about to 0.7° and the frequency deviation is within 49.95–50.05 Hz for both cases. The ±0.05 Hz frequency deviation and a 0.7° phase error are acceptable values for any power system. Also, these values are comparable with those reported in the literature [3]. From the results, it can be concluded that the proposed method is so robust to voltage sag and harmonics.

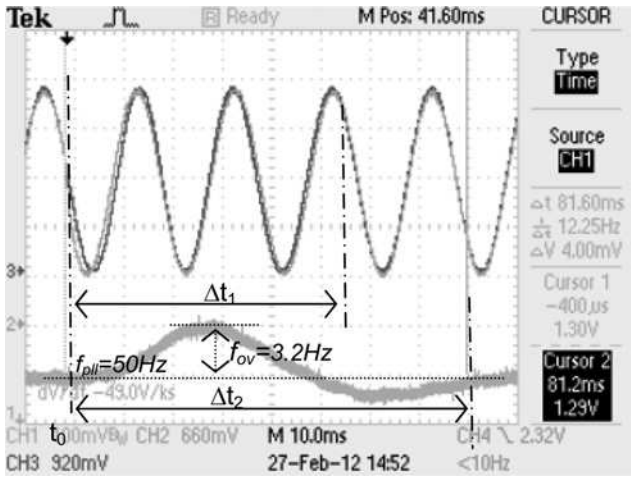


Fig. 5 *Response to a phase-angle jump of 40°*

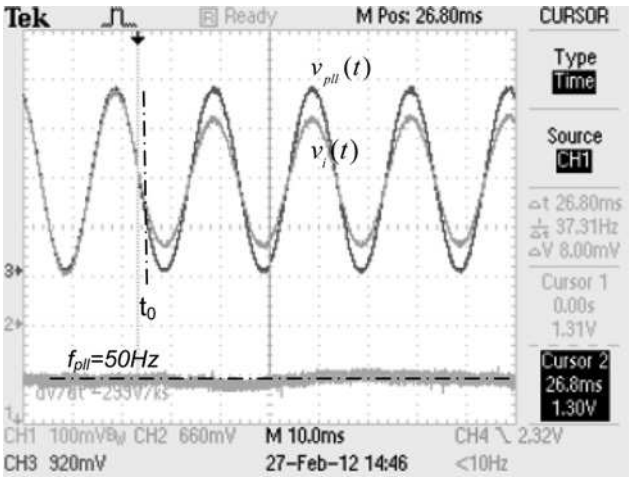


Fig. 6 *Response to a 30% voltage sag*

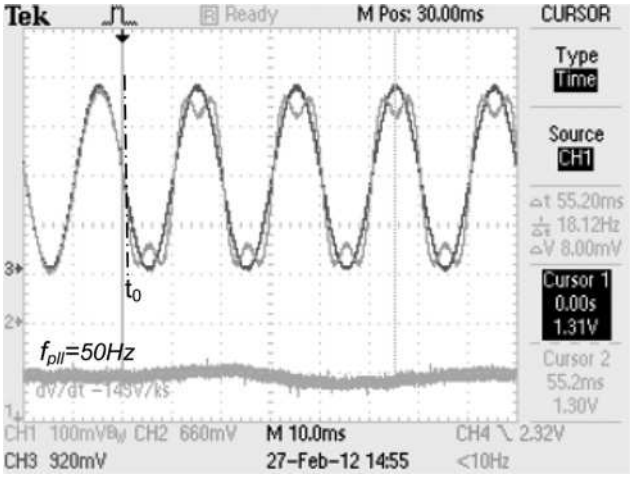


Fig. 7 *Response to a 15% third harmonic injection*

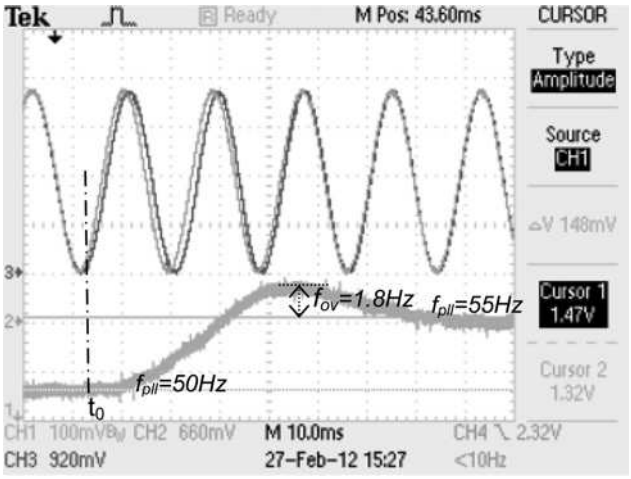


Fig. 8 *Response to a +5 Hz step change in frequency*

It is shown in Fig. 8 that the proposed method locks to the new reference frequency (55 Hz) with zero steady-state error when a +5 Hz step changes in frequency at the input voltage signal. One should keep in mind that a frequency step of +5 Hz corresponds to an extreme situation in a power system. Frequency deviations occur in a much narrower band in a power system. In spite of this, the maximum overshoot is about 1.8 Hz and the settling time is about to 3.5 cycles (70 ms) with the proposed method for this extreme situation.

It is shown in Fig. 9 that the proposed method has a high performance when the input signals have multi-zero crossings, which represent an extreme case in power systems. The maximum overshot in frequency is $f_{ov} = 4.6$ Hz and the settling time is about the 5.8 cycles.

4.2 Literature comparison

Performances of the three selected single-phase PLL algorithms designed specifically for UPS applications were compared and the results were provided in a table clearly in [3]. These PLL structures were pPLL, inverse park transformation-based PLL (park PLL) and adaptive phase detection-based PLL (EPLL). In this study, performance of the proposed method was compared with the mentioned three PLL algorithms by using information provided in [3]. Results are given in Table 2. When examining Table 2, one should keep in mind that real-time applications of the proposed and other three PLL algorithms were performed on the same DSP family (TMSF320F281X, 32-bit, 150 MHz).

It is clear from Fig. 1 that the total number of operations corresponding to the proposed method is more than that of the other three algorithms because of frequency discriminator. However, computational load in real time corresponding to the proposed method is the least as can be seen from Table 2 thanks to the new hybrid approaches in hardware and software solution presented in this study.

From Table 2, the proposed method is seen to have high performance and robustness for common power system failures such as 30% voltage sag and 15% third harmonic injection.

For +40° phase-angle jump, it is superior to the other methods in terms of overshoot in phase and overshoot in frequency. For settling time, it is close to the EPLL method having the best performance.

Application of +5 Hz step change in frequency at the input voltage, except the best EPLL method, the proposed and other methods behaves similarly.

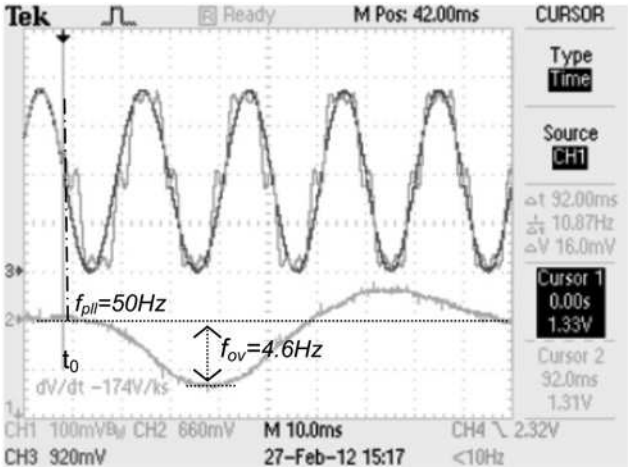


Fig. 9 *Response to multi-zero crossing*

Table 2 Comparison of the proposed method with the existed studies

	pPLL	Park PLL	EPLL	**Proposed PLL**
30% voltage sag				
settling time (cycles)	5	2	2.5	**0.05**
overshoot in phase	2°	4°	3°	**0.7°**
15% third harmonic phase error (in steady state)	0°	3°	5°	**0°**
40° phase-angle jump				
settling time (cycles)	7	3	2.5	**2.8**
overshoot in phase	23°	14°	15°	**3°**
overshoot in frequency (f_{ov})	8 Hz	15 Hz	16 Hz	**3.2** Hz
+5 Hz step in frequency				
settling time (cycles)	7	3	2.5	**3.2**
overshoot in phase	30°	9°	9°	**21°**
overshoot in frequency (f_{ov})	2.5 Hz	2 Hz	1.2 Hz	**1.8** Hz
computational load	68% 2.58 µs	100% 3.80 µs	80% 3.04 µs	**62%** **2.35** µs
multi-zero crossing				
settling time (cycles)	—	—	—	**5.8**
overshoot in phase	—	—	—	**10°**
overshoot in frequency (f_{ov})	—	—	—	**4.6** Hz

The performances of the other three methods when the input signals have multi-zero crossings were not investigated in [16]. On the other hand, as stated in Table 2 the proposed method has a high performance for this extreme case.

In summary, the proposed hybrid method resulting from new approaches in hardware and software has less computational load and is more robust to phase-angle jump, voltage sag and third harmonic injection distortions compared with other methods. This robust characteristic is very important in industrial applications such as active power filters, UPS, connection of alternative energy sources (sun and wind) to power systems. In this study, a fast, robust and easily implementable fully software-based digital PLL algorithm was developed.

5 Conclusions

In this study, a software-based fast digital PLL method was proposed by exploiting new hybrid approaches in hardware and software in an advanced DSP architecture. Its real-time experimental application was performed successfully. Experimental results show that the proposed PLL algorithm is robust to line disturbances such as phase-angle jump, voltage sag, third harmonic injection, multi-zero crossings and step change in frequency at input signal. Furthermore, the proposed method was shown to be superior to the three PLL algorithms existing in the literature. Its computation time is 2.35 µs that is much smaller than that of other methods. It is a fully software-based digital PLL algorithm and can be used in real-time applications of power electronics, measurement and control systems operating at high switching/sampling frequencies.

6 Acknowledgments

This work was supported by The Scientific and Technological Research Council of Turkey (TUBITAK) under project number 107-E-165.

doi: 10.1049/iet-gtd.2013.0041

7 References

1 Silva, C.H., Pereira, R.R., Borges, L.E., Torres, G.L., Bose, B.K.: 'A digital PLL scheme for three-phase system using modified synchronous reference frame', *IEEE Trans. Ind. Electron.*, 2010, **57**, (11), pp. 3814–3821

2 Karimi-Ghartemani, M., Iravani, M.R.: 'A method for synchronization of power electronic converters in polluted and variable-frequency environments', *IEEE Trans. Power Syst.*, 2004, **19**, (3), pp. 1263–1270

3 Santos Filho, R.M., Seixas, P.F., Cortizo, P.C., Torres, L.A.B., Souza, A.F.: 'Comparison of three single-phase PLL algorithms for UPS applications', *Trans. Ind. Electron.*, 2008, **55**, (8), pp. 2923–2932

4 Freijedo, F.D., Yepes, A.G., Lopez, O., Vidal, A., Gandoy, J.D.: 'Three-phase PLLs with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation', *IEEE Trans. Power Electron.*, 2011, **26**, (1), pp. 85–97

5 Liccardo, F., Marino, P., Raimondo, G.: 'Robust and fast three-phase PLL tracking system', *Trans. Ind. Electron.*, 2011, **58**, (1), pp. 221–231

6 Fedele, G., Picardi, C., Sgro, D.: 'A power electrical signal tracking strategy based on the modulating functions method', *IEEE Trans. Ind. Electron.*, 2009, **56**, (10), pp. 4079–4087

7 Rodriguez, P., Pou, J., Bergas, J., *et al.*: 'Decoupled double synchronous reference frame PLL for power converters control', *IEEE Trans. Power Electron.*, 2007, **22**, (2), pp. 584–592

8 Golestan, S., Monfared, M., Freijedo, F.D., Guerrero, J.M.: 'Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems', *IEEE Trans. Power Electron.*, 2012, **27**, (8), pp. 3639–3650

9 Wang, Y.F., Li, Y.W.: 'Grid synchronization PLL based on cascaded delayed signal cancellation', *IEEE Trans. Power Electron.*, 2011, **26**, (7), pp. 1987–1997

10 Carugati, I., Donato, P., Maestri, S., Carrica, D., Benedetti, M.: 'Frequency adaptive PLL for polluted single-phase grids', *IEEE Trans. Power Electron.*, 2012, **27**, (5), pp. 2396–2404

11 Golestan, S., Monfared, M., Freijedo, F.D., Guerrero, J.M.: 'Dynamics assessment of advanced single-phase PLL structures', *IEEE Trans. Ind. Electron.*, 2013, **60**, (6), pp. 2167–2177

12 Barbosa Rolim, L.G., Rodrigues da Costa Jr. D., Aredes, M.: 'Analysis and software implementation of a robust synchronizing PLL circuit based on the pq theory', *IEEE Trans. Ind. Electron.*, 2006, **53**, (6), pp. 1919–1926

13 El-Amawy, A.A., Mirbod, A.: 'An efficient software-controlled PLL for low-frequency applications', *IEEE Trans. Ind. Electron.*, 1988, **35**, (2), pp. 341–344

14 Choi, J.W., Kim, Y.K., Kim, H.G.: 'Digital PLL control for single-phase photovoltaic system', *IEE Proc.-Electr. Power Appl.*, 2006, **153**, (1), pp. 40–46

15 Chung, S.: 'A phase tracking system for three phase utility interface inverters', *IEEE Trans. Power Electron.*, 2000, **15**, (3), pp. 431–438

16 Giroux, P., Sybille, G.: 'MATLAB/simulink Ver 6.5/simpowersystem toolbox' (Mathworks Inc., 2006)

17 Proakis, J.G., Salehi, M.: 'Communication systems engineering' (Prentice-Hall, New Jersey, USA, 2002, 2nd edn.)

18 Haykin, S.: 'Communication systems' (John Wiley & Sons, USA, 1994, 3rd edn.)

19 Ogata, K.: 'Discrete-time control systems' (Prentice-Hall, NJ, USA, 1995)