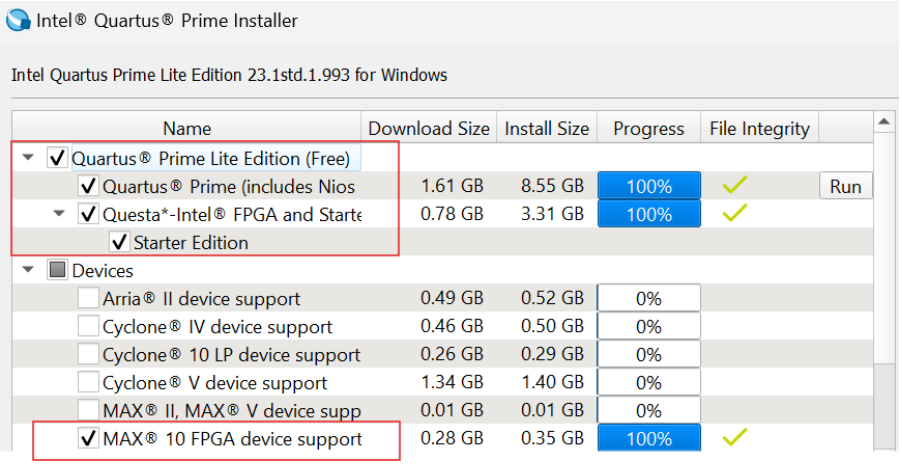
Project Setup Guide

A guide for installing Quartus, setup Questa, setup the initial RISC-V project, and run the simulation.

Install Intel Quartus Prime Lite. Make sure to choose the latest version and the correct OS.

Note: this guide is for Windows OS, other OS might looks similar.

Open the installer, make sure to check these options (Quartus Prime Lite, Questa, MAX 10 FPGA):



When going through the installer, **remember the installed location**. For me, it's C:\intelFPGA_lite\23.1std

Go into the installed location, and open the **questa_fse** folder (path should resemble this: C:\intelFPGA_lite\23.1std\questa_fse

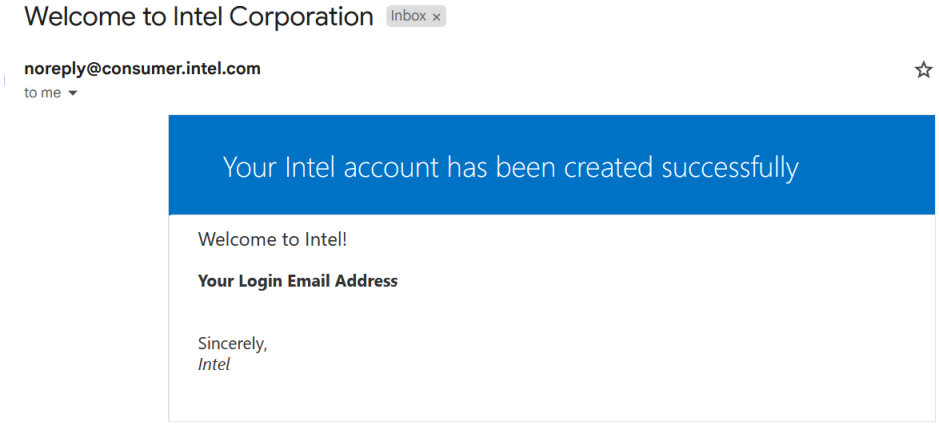
In there, you'll find a **readme.txt** file. It contains the direction on how to obtain the license under the "Licensing Questa-Intel FPGA Edition software" section.

- **DO NOT** skip any line. My mistake was skipping lines and have to do everything again.

If you follow the readme.txt instructions, you should be good. But just to spell out what you need to do briefly, here are the steps:

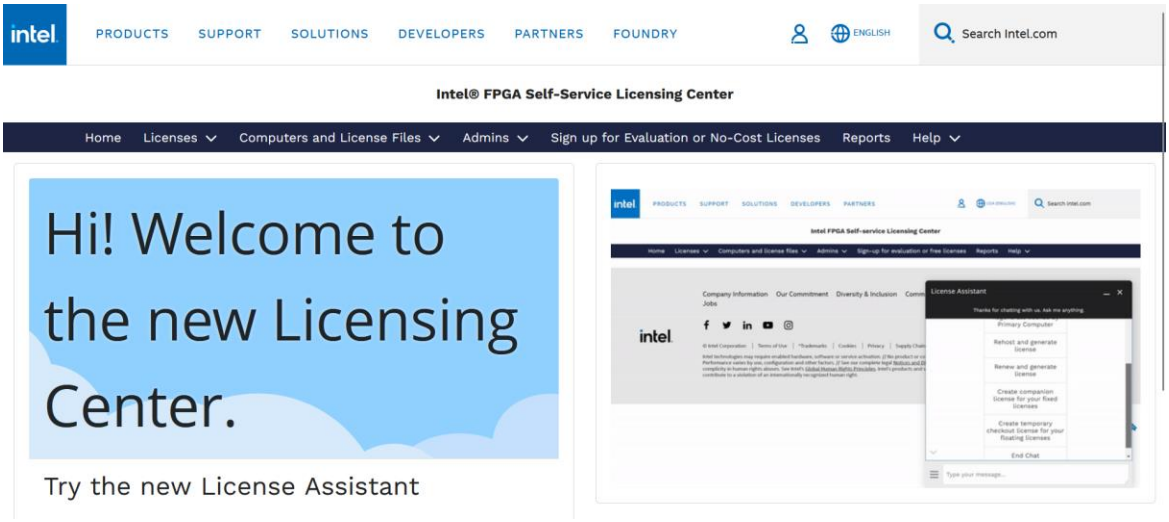
1. Go to: Intel FPGA Licensing Support Center

2. Enroll (or sign-in) if you already have an account.
    a. For **enroll**, after account registration, you need to **wait for the email** from Intel saying your account has done setting up. Else you won't be able to log in. Email looks like this:

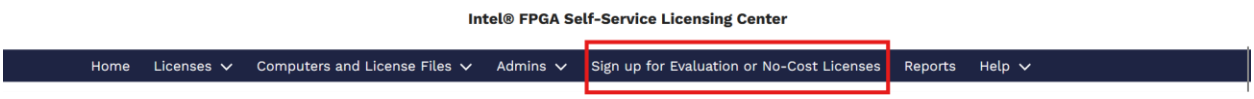


    b. When **logging in**, you'll be redirect to Intel Azure portal. If it shows your UW account, just go back and switch to the account you used to sign up for Intel account.

3. If successful, you screen should look like this, else you did something wrong or skip steps in-between.



4. Click on "Sign up for Evaluation or No-Cost License":



5. Choose Questa Intel FPGA Starter Edition:

6. Next -> Choose existing computer or create a new one.
    a. Create a new one: License type is **FIXED**, for NIC ID or Guard ID, Google how you can get that info from your computer.
7. Read agreements, generate license.

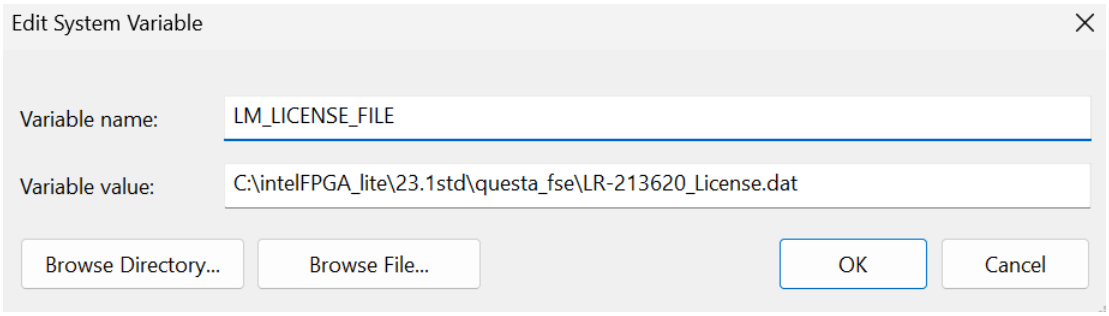
The license should be sent to **your email**.

Save it on you computer as **.dat** file. Remember the save location (I saved it in the same location as the Questa folder).

Follow these steps:

1. Go to **This PC**, right-click, and select **Properties**.
2. Click **Advanced System Setting**.
3. In the **Advanced** tab, select **Environment Variable**.
4. Under **System variables**, create a new variable with the name as `LM_LICENSE_FILE` and value as `<license.dat file path>`.
5. Click **OK** and restart the Questa*-Intel® FPGA Edition software.

- **Note:** again, under **System variables**, NOT user variables!
- **Variable name:** `LM_LICENSE_FILE`
- **Variable value:** the license .dat path

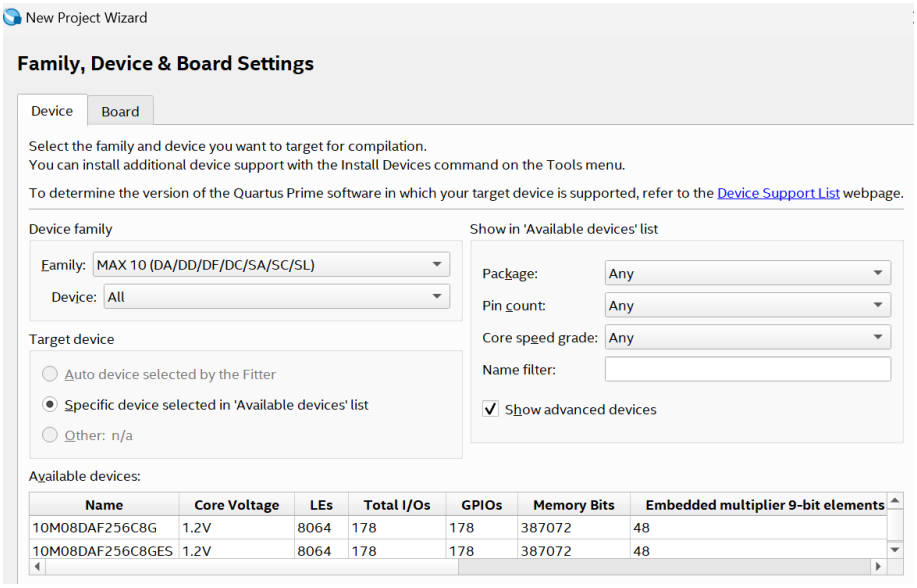


Next is how to set up the project.

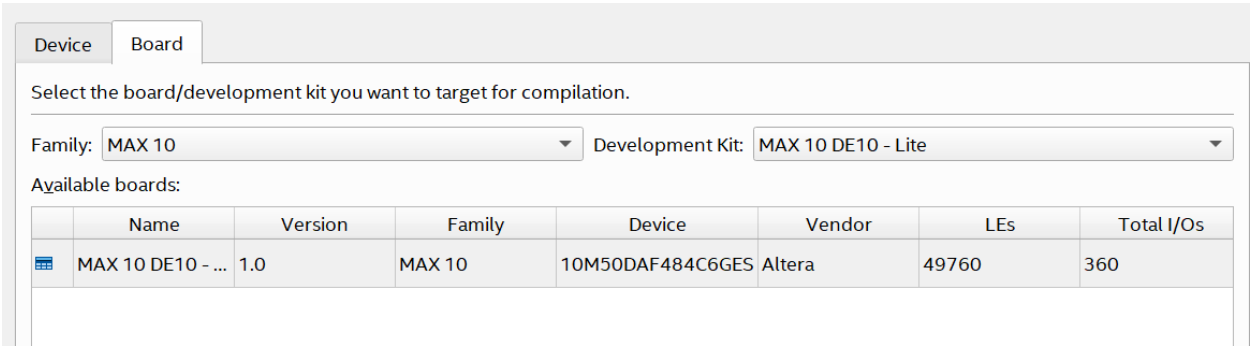
Download the .sv and .txt files this repository.

Open Quartus -> File -> New Project Wizard -> Choose save location & name -> Empty Project -> Next -> Next

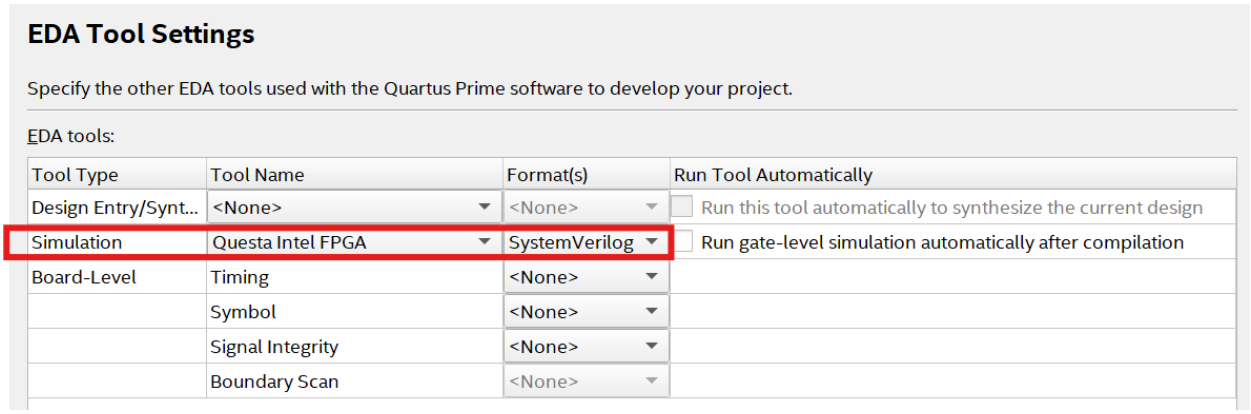
Device: MAX10 family:



Board: Development kit: MAX 10 DE10 - Lite



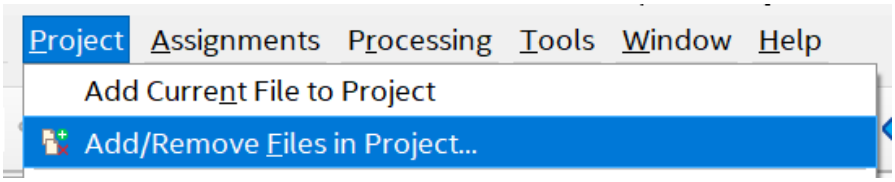
Next -> EDA Tool Settings -> Simulation: Questa Intel FPGA (**NOT QuestaSim**), SystemVerilog



Next -> Finish

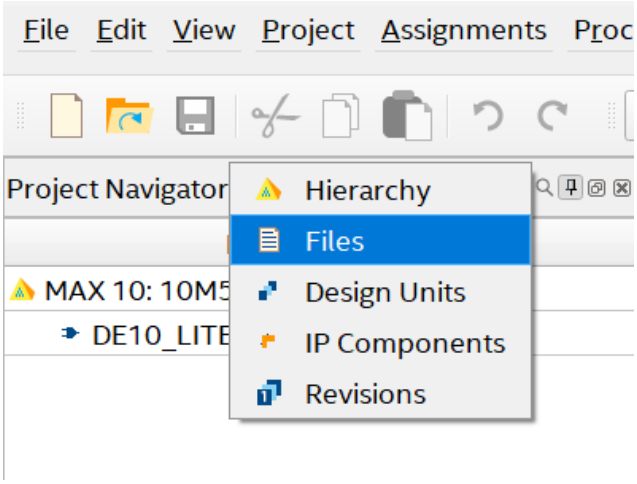
Drag all the **.sv files + riscvtest.txt** to the folder containing the project you just created.

Then:



Choose the "..." -> Select all the **.sv files + riscvtest.txt** you just dragged in -> Apply -> Ok

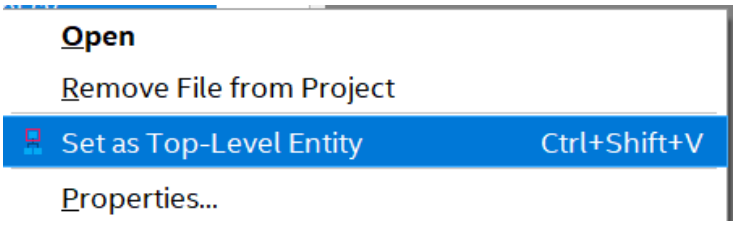
Top left of UI: Project Navigator drop-down, change from Hierarchy to **Files**



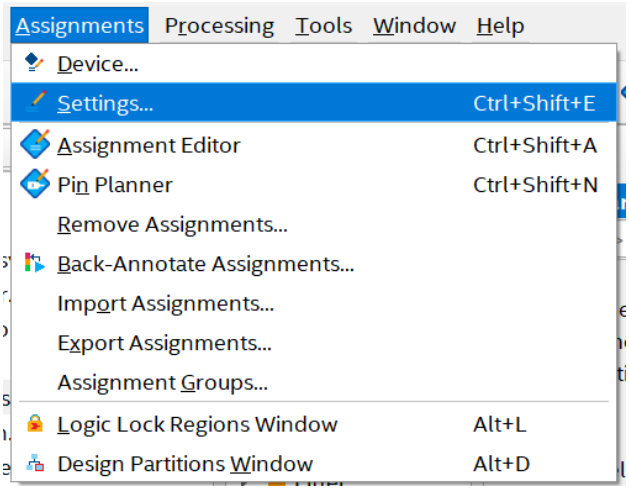
Open the **mem.sv**, change this to the **absolute path** of the riscvtest.txt (line 13):

```
13        $readmemh("D:/path/riscvtest.txt", RAM);
```

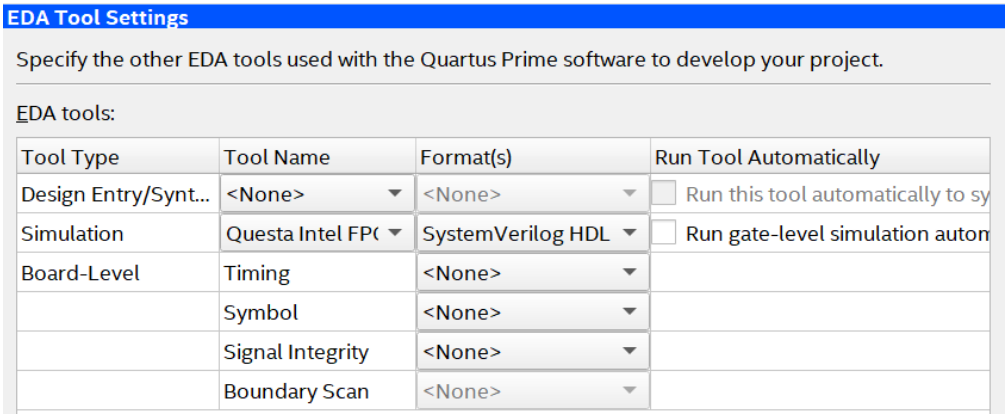
Right-click on **topLevel.sv** -> Set as Top Level Entity



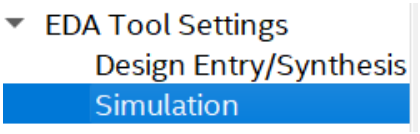
Go to Assignments -> Settings:



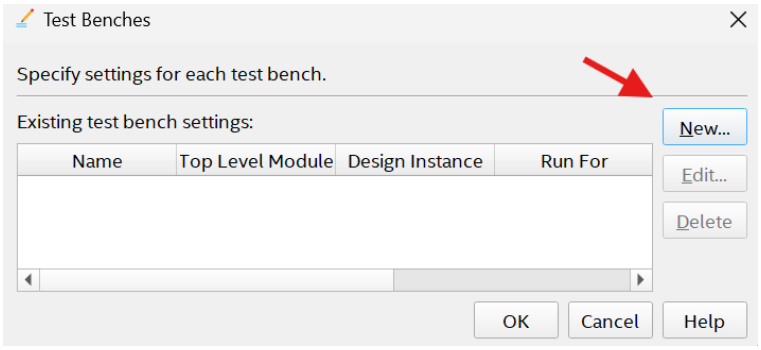
Choose “EDA Tool Settings”, make sure it looks like this:



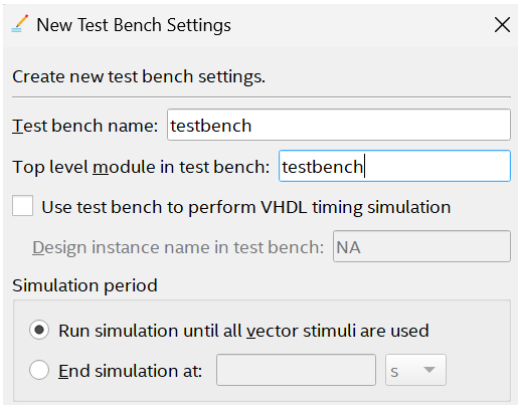
Choose Simulation:



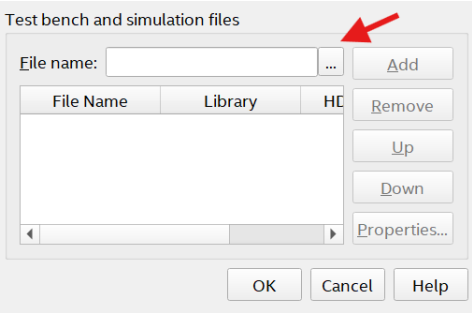
Then choose the compile test bench, click the “Test Benches” box.



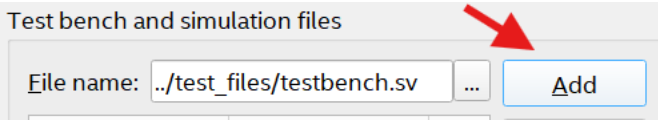
Use these settings:



Click on the “...”, find the “**testbench.sv**” file

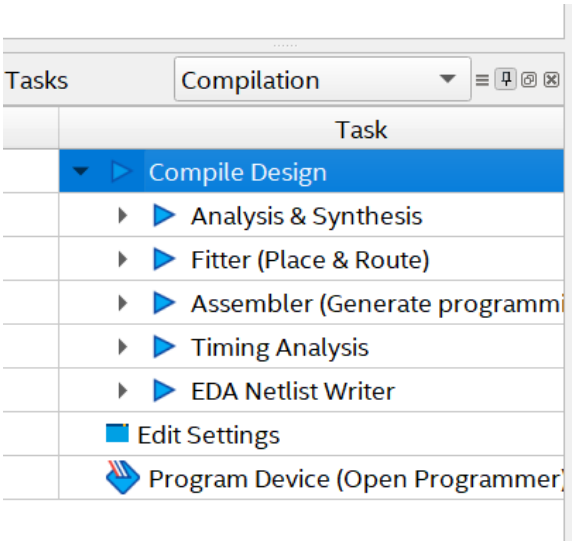


Click **Add**:

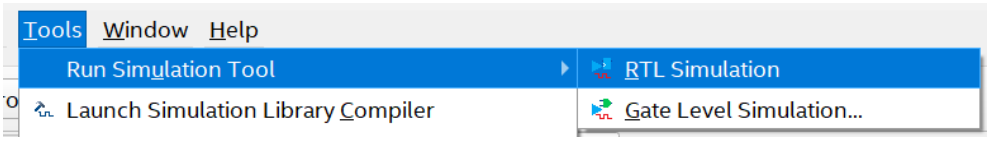


Ok -> Apply -> Ok

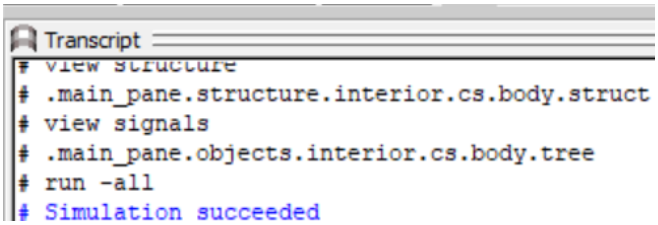
Under Compilation, double click on **Compile Design**. Wait until 100% (mine took around 2 - 5 minutes).

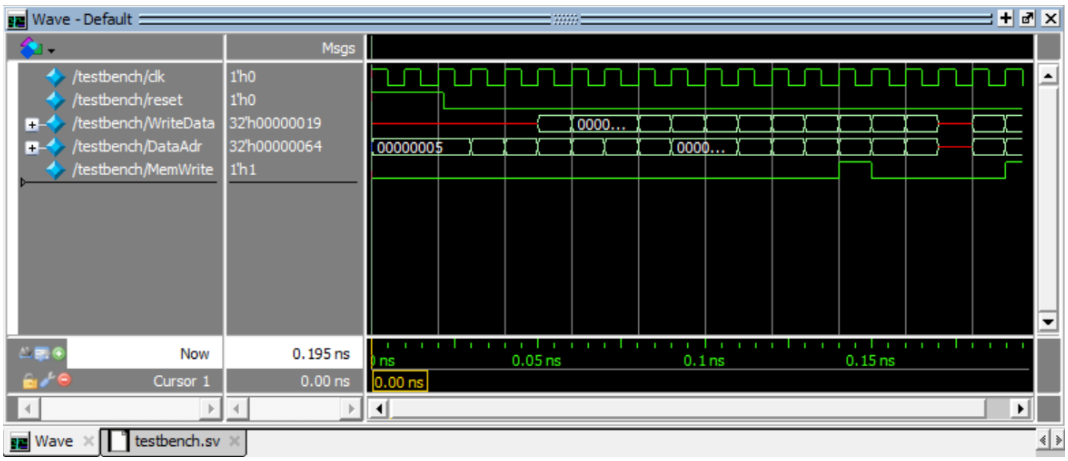


Go to:



Questa should pop up, if you have this line in the terminal and the UI looks like this, good job =]





Bonus: for your amusement, you could also view the RTL diagram of the RISC-V processor.