Bài 2:Chương trình hiển thị led:

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_arith**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

---------------------------------------------------------------------

**entity** hien\_thi\_led **is**

**port** **(**

so **:** **in** integer**;**

out\_7seg**:** **out** std\_logic\_vector **(**6 **downto** 0**)**

**);**

**end** hien\_thi\_led**;**

---------------------------------------------------------------------

**architecture** behavior **of** hien\_thi\_led **is**

**begin**

**process(**so**)**

**begin**

**case** so **is**

**when** 0 **=>** out\_7seg **<=** "1111110"**;**

**when** 1 **=>** out\_7seg **<=** "0110000"**;**

**when** 2 **=>** out\_7seg **<=** "1101101"**;**

**when** 3 **=>** out\_7seg **<=** "1111001"**;**

**when** 4 **=>** out\_7seg **<=** "0110011"**;**

**when** 5 **=>** out\_7seg **<=** "1011011"**;**

**when** 6 **=>** out\_7seg **<=** "1011111"**;**

**when** 7 **=>** out\_7seg **<=** "1110000"**;**

**when** 8 **=>** out\_7seg **<=** "1111111"**;**

**when** 9 **=>** out\_7seg **<=** "1111011"**;**

**when** **others** **=>** out\_7seg**<=** "0000000"**;**

**end** **case;**

**end** **process;**

**end** behavior**;**

Chương trình bộ đếm :

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_arith**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

---------------------------------------------------------------------

**entity** bodem **is**

**port** **(**

reset**,**count **:** **in** std\_logic**;**

led1**,**led2**,**led3 **:** **out** std\_logic\_vector**(**6 **downto** 0**)**

**);**

**end** bodem**;**

---------------------------------------------------------------------

**architecture** behavior **of** bodem **is**

**signal** tram**,**chuc**,**donvi **:** integer**;**

**component** hien\_thi\_led **is**

**port** **(**

so **:** **in** integer**;**

out\_7seg**:** **out** std\_logic\_vector **(**6 **downto** 0**)**

**);**

**end** **component;**

**begin**

**process(**count**,**reset**)**

**variable** t\_donvi**,**t\_chuc**,**t\_tram **:** integer**;**

**begin**

**if** reset **=** '1' **then**

t\_tram **:=** 0**;**

t\_chuc **:=** 0**;**

t\_donvi **:=** 0**;**

**else**

**if** count'**event** and count **=** '1' **then**

t\_donvi **:=** t\_donvi **+** 1**;**

**if** t\_donvi **=** 10 **then**

t\_donvi**:=** 0**;**

t\_chuc **:=** t\_chuc **+** 1**;**

**end** **if;**

**if** t\_chuc **=** 10 **then**

t\_chuc**:=** 0**;**

t\_tram **:=** t\_tram **+** 1**;**

**end** **if;**

**if** t\_tram **=** 10 **then**

t\_tram **:=** 0**;**

**end** **if;**

**end** **if;**

**end** **if;**

tram **<=** t\_tram**;**

chuc **<=** t\_chuc**;**

donvi **<=** t\_donvi**;**

**end** **process;**

u1**:**hien\_thi\_led **port** **map** **(**tram**,**led1**);**

u2:hien\_thi\_led port map (chuc,led2);

u3:hien\_thi\_led port map (donvi,led3);

end behavior;

Bài 3:

Chương trình máy trạng thái:

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** may\_trang\_thai **is**

**port** **(**

inp **:** **in** std\_logic**;**

clk**,**rst **:** **in** std\_logic**;**

outp **:** **out** std\_logic\_vector **(**1 **downto** 0**)**

**);**

**end** may\_trang\_thai**;**

**architecture** behavior **of** may\_trang\_thai **is**

**type** states **is** **(**S1**,**S2**,**S3**,**S4**);**

**signal** current\_state**,**next\_state **:** states**;**

**begin**

-- Phan mach day

**process(**rst**,**inp**,**clk**)**

**begin**

**if** rst **=** '1' **then**

current\_state **<=** S1**;**

**else**

**if** clk'**event** and clk **=** '1' **then**

current\_state **<=** next\_state**;**

**end** **if;**

**end** **if;**

**end** **process;**

-- Phan mach to hop

**process(**current\_state**)**

**begin**

**case** current\_state **is**

**when** S1 **=>**

outp **<=** "00"**;**

**if** inp **=** '1' **then**

next\_state **<=** S2**;**

**else**

next\_state **<=** S1**;**

**end** **if;**

**when** S2 **=>**

outp **<=** "01"**;**

**if** inp **=** '1' **then**

next\_state **<=** S4**;**

**else**

next\_state **<=** S3**;**

**end** **if;**

**when** S3 **=>**

outp **<=** "10"**;**

**if** inp **=** '1' **then**

next\_state **<=** S4**;**

**else**

next\_state <= S3;

end if;

when S4 =>

outp <= "11";

if inp = '1' then

next\_state <= S1;

else

next\_state <= S2;

end if;

end case;

end process;

end behavior;