Synopsys DesignWare IP Support Kick-off Meeting

For Horizon Sigiriya

Zheng Deng, Application Engineer

5th Nov 2021

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Agenda

- Contacts & Project Information
- Project Information (by Horizon)
- IP Support
- IP Training & Integration Reviews
- IP Documentation, Download and Notifications
- Support Resources Available Online
- Other useful info

Contacts and Project Information

Key Contact Information

- **Customer Team**
  - Wei Wang (Key Contact/UFS IP Owner)
    Shanghai (wei04.wang@horizon.ai)
  - Herman Yu (Engineer Manager)
    Shanghai (herman.yu@horizon.ai)
  - Juncheng Shen (DDR/SPI IP owner)
    Shanghai (juncheng.shen@horizon.ai)
  - Yujie Ren (PCIE/ETH/PVT IP owner)
    Shanghai (yujie.ren@horizon.ai)
  - Austin.lin (PCIE/ETH IP owner)
    Hongkong (austin.lin@horizon.ai)
  - Stanley Sha (MIPI IP owner)
    Taiwan (stanley.sha@horizon.ai)
  - Wei Yao (DP/eDP/Uart/Timer/Wdt IP owner)
    Shanghai (wei.yao@horizon.ai)
  - Jianbing Hu (USB/I2S IP owner)
    Shanghai (jianbing.hu@horizon.ai)
  - Zhiwei Liu (USB IP owner)
    Shanghai (zhiwei.liu@horizon.ai)
  - Xuan Dong (I2C IP owner)
    Shanghai (xuan.dong@horizon.ai)
  - Wei Nie (DMA IP owner)
    Shanghai (wei.nie@horizon.ai)
  - Chaoqiang Chu (GPIO IP owner)
    Shanghai (chaoqiang.chu@horizon.ai)

- **Synopsys Team**
- **Post-sales IP Support**
  - Atharva Akolkar (AMBA Post-sales AE)
    Bangalore (atharva@synopsys.com)
  - Jaskaran Singh (AMBA Post-sales AE)
    Bangalore (jasingh@synopsys.com)
  - Lei Cheng (DSC Post-sales AE)
    Shanghai (leic@synopsys.com)
  - Dehuan Meng (DP/eDP controller Post-sales AE)
    Beijing (dehuan@synopsys.com)
  - Di Dai (USB controller Post-sales AE)
    Beijing (did@synopsys.com)
  - Songwei Chen (USB PHY Post-sales AE)
    Shanghai (songweic@synopsys.com)
  - Amy Yang (MIPI CSI/DSI Post-sales AE)
    Shanghai (leiy@synopsys.com)
  - Breeze Shen (MPHY Post-sales AE)
    Shenzhen (ren@synopsys.com)
  - Cara Wang (UFS controller Post-sales AE)
    Shanghai (yangwa@synopsys.com)
  - Jesse Yang (ETH controller Post-sales AE)
    Shenzhen (jessey@synopsys.com)
  - Zhengyi Chen (DDR PHY Post-sales AE)
    Shanghai (zhengyi@synopsys.com)
  - Xiaoqing Wang (DDR controller Post-sales AE)
    Beijing (xiaoqing@synopsys.com)
  - Liang Yin (Multi-PHY Post-sales AE)
    Beijing (liangyin@synopsys.com)
  - Terry Yang (PCIE controller Post-sales AE)
    Beijing (xiaojuny@synopsys.com)

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    Shanghai (chaoqiang.chu@horizon.ai)

- **Synopsys Team**
- **Pre-sales IP Support**
  - Zheng Deng (Presales AE)
    Beijing (zheng.deng@synopsys.com)
- **Program Manager**
  - Michael Yang (Program Manager)
    Shanghai (yangyi@synopsys.com)
- **Sales Team:**
  - Kenny Zhou (IP Product Solution Sales Manager)
    Beijing (kun@synopsys.com)
  - Tao Du (Executive Account Manager)
    Beijing (dutao@synopsys.com)

Product License Information

Note: The correct Project ID and licensed product names are required for core support

- Official Project Name: Sigiriya
- The licenses are hosted at: Horizon (Shanghai) Artificial, Bldg C, No.888, Huanhu West 2nd Rd,, Shanghai, 201306
- Site ID: 42533
- Project ID: Sigiriya (1)

Product code	Licensed products	Support start	Support end	Comments
E094-0	DWC AP LPDDR5/4/4X Controller	3rd Nov 2021	2nd Nov 2023	Config2, Port num TBD
D771-0	dwc_ap_lpddr54_phy_tsmc7ff18	3rd Nov 2021	2nd Nov 2023	
C413-0	DWC UFS G4 HC AND UNIPRO	3rd Nov 2021	2nd Nov 2023	
7270-0	DWC UFS HC SW	3rd Nov 2021	2nd Nov 2023	
C470-0	dwc_mipi_mphy_type1_22_tsmc7ff	3rd Nov 2021	2nd Nov 2023	Cust: Metal, Auto Enhance

(1) used during IP installation

Product License Information

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Product code	Licensed products	Support start	Support end	Comments
F319-0	DWC AC PCIe 4.0 Premium AMBA	1st Mar 2022	28th Feb 2024	EA, subject to change
D936-0	DWC PCIe Software Sample	3rd Nov 2021	2nd Nov 2023	
C118-0	DWC AP Ethernet QOS	3rd Nov 2021	2nd Nov 2023	
C432-0	DWC Ether QOS TSN1 Add-on	3rd Nov 2021	2nd Nov 2023	
C433-0	DWC Ether QOS RxParser Add-on	3rd Nov 2021	2nd Nov 2023	
D473-0	DWC AP Ethernet XGMAC	3rd Nov 2021	2nd Nov 2023	
D475-0	DWC XGMAC TSN1 Add-on	3rd Nov 2021	2nd Nov 2023	
D476-0	DWC XGMAC RxParser Add-on	3rd Nov 2021	2nd Nov 2023	
D474-0	DWC AP Ethernet XPCS	3rd Nov 2021	2nd Nov 2023	
C777-0	DWC Ethernet PCS Multiport Add-on	3rd Nov 2021	2nd Nov 2023	
G539-0	DWC AP2 MP16G LP TSMC N7 X4	25th Jan 2022	24th Jan 2024	EA. Cust: SGMII-1.25G, QSGMII-5G

Product License Information

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Product code	Licensed products	Support start	Support end	Comments
F382-0	DWC AC MIPI CSI2 HP Host Combo	4th Nov 2021	3rd Nov 2023	EA, subject to change
E115-0	DWC AP MIPI CD RX 3T4L 45 TSMC N7 NS	23th Nov 2021	22th Nov 2022	
B915-0	DWC AP MIPI CSI2 Device Ctlr	3rd Nov 2021	2nd Nov 2023	
F985-0	DWC AP MIPI DSI Host Ctrl	3rd Nov 2021	2nd Nov 2023	ConfigB
F983-0	DWC AP MIPI D T4 TSMC N7 NS	3rd Nov 2021	2nd Nov 2023	
9057-0	DWC MIPI DSI Host SW Sample	3rd Nov 2021	2nd Nov 2023	
9058-0	DWC MIPI CSI2 Host SW Sample	3rd Nov 2021	2nd Nov 2023	
B150-0	DWC MIPI CSI2 Device SW Sample	3rd Nov 2021	2nd Nov 2023	

Product License Information

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Product code	Licensed products	Support start	Support end	Comments
E051-0	DWC VESA DSC Encoder ver 1.2a RTL	3rd Nov 2021	2nd Nov 2023	
G260-0	DWC DP-eDP Tx 1.4 with external DSC			
C289-0	DWC DP MultiPixel Mode Add-On	3rd Nov 2021	2nd Nov 2023	
C290-0	DWC DP MultiStrmTrsprt Add-On	3rd Nov 2021	2nd Nov 2023	
56764-0	DP Integration CoStart			
A871-0	DWC USB 3.1 DRD-Single Port	3rd Nov 2021	2nd Nov 2023	
A875-0	DWC USB 3.1 Hibernation Add-On	3rd Nov 2021	2nd Nov 2023	
C391-0	dwc_usbc31dptxphy_tsmc7ffns	3rd Nov 2021	2nd Nov 2023	Cust: Metal, Auto Enhance
C236-0	dwc_usb2_femtophy_otg_tsmc7ff18_x1ns	3rd Nov 2021	2nd Nov 2023	Cust: Metal, Auto Enhance

Product License Information

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Product code	Licensed products	Support start	Support end	Comments
3771-0	DWC APB Peripherals	3rd Nov 2021	2nd Nov 2023	
3768-0	DWC AMBA Fabric	23th Nov 2021	22th Nov 2022	
3772-0	DWC APB Advanced Peripherals	23th Nov 2021	22th Nov 2022	
A415-0	DWC AXI DMAC	3rd Nov 2021	2nd Nov 2023	
3889-0	DWC DMA Controller	23th Nov 2021	22th Nov 2022	
B858-0	DWC SSI	3rd Nov 2021	2nd Nov 2023	
F801-0	DWC SSI Internal DMA	3rd Nov 2021	2nd Nov 2023	
D470-0	DWC SPI to AHB Bridge add-on	3rd Nov 2021	2nd Nov 2023	

Project Information

Item	Description
Project Name	Sigiriya
Application	ADAS
Process Technology	TSMC automotive 7nm
Package	Flip-chip
Metal Stack	13M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2R
RTL Q/A Flow (LINT, CDC etc)	Spyglass
Verification Flow (tools, VIP, methodology)	VCS
Synthesis Flow (tools, methodology)	DC
Physical Design Flow (tools, methodology)	Innovas
System Validation flow (SW, H/W, methodology)	Haps
Project Schedule (start, RTL freeze, ES1 TO, production etc.)	TBD

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

- 384bit total subject to change, may be placed at EW, NS or as L-shape
- Controller follow “LPDDR54_ASILB_Config2” as shown in next page, AXI port number and settings are subject to change

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

set_configuration_parameter DDRCTL_PRODUCT_NAME 2;	DWC-AP-LPDDR54-Controller
set_configuration_parameter MEMC_DRAM_DATA_WIDTH 32	32bit memory datapath
set_configuration_parameter UMCTL2_INCL_ARB 1; # == default value.	AXI Configuration
set_configuration_parameter MEMC_NUM_RANKS 2;	2 ranks system
set_configuration_parameter MEMC_ECC_SUPPORT 1	ECC Support
set_configuration_parameter MEMC_SIDEBAND_ECC 0	No sideband ECC
set_configuration_parameter MEMC_INLINE_ECC 1	Inline ECC
set_configuration_parameter MEMC_USE_RMW 1; # == default value.	RMW Required
set_configuration_parameter UMCTL2_SBR_EN 1	ECC Scrubber
set_configuration_parameter MEMC_NO_OF_ENTRY 64	64 entries per CAM
set_configuration_parameter MEMC_NO_OF_BLK_CHANNEL 16	16 BLK CHANNELS
set_configuration_parameter UMCTL2_VPRW_EN 1	QoS Enabled
set_configuration_parameter UMCTL2_OCPAR_EN 1	On-Chip Parity Enabled
set_configuration_parameter UMCTL2_OCPAR_ADDR_PARITY_WIDTH 1	On-chip parity address width
set_configuration_parameter DDRCTL_OCSAP_EN 1	On-Chip External SRAM Address Protection
set_configuration_parameter UMCTL2_REGPAR_EN 1	Registers Parity Protection
set_configuration_parameter UMCTL2_REGPAR_TYPE 0; # == default value.	1bit parity for every 32bit register for REGPAR
set_configuration_parameter UMCTL2_OCCAP_EN 1	On-Chip Command and Address Path Protection
set_configuration_parameter UMCTL2_HWFFC_EN 0;# ==default value.	No HWFFC support
set_configuration_parameter UMCTL2_FREQUENCY_NUM 1;# ==default value.	1 set of AC reg. No fast frequency support
set_configuration_parameter UMCTL2_WDATA_EXTRAM 1; # == default value.	External write data SRAM
set_configuration_parameter MEMC_PERF_LOG_ON 1	Performance log
set_configuration_parameter UMCTL2_A_NPORTS 2	2 AXI ports config
set_configuration_parameter UMCTL2_XPI_USE_INPUT_RAR 1	XPI read address output retime to aid timing
set_configuration_parameter UMCTL2_XPI_USE_RPR 1	XPI read data/parity retime to aid timing
set_configuration_parameter UMCTL2_EXCL_ACCESS 0; # == default value.	No Exclusive Access support
set_configuration_parameter UMCTL2_EXT_PORTPRIO 1	External Port priority enabled
set_configuration_parameter UMCTL2_A_LENW 8; # ==default value.	AXI AxLen width support up to 8bits
set_configuration_parameter UMCTL2_A_IDW 6	AXI ID width support up to 6bits
set_configuration_parameter UMCTL2_A_ADDRW 33	Max AXI address bit width

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

set_configuration_parameter UMCTL2_A_TYPE_0 3; # == default value.	AXI4
set_configuration_parameter UMCTL2_PORT_DW_0 256; # == default value.	256bit port width for 1st AXI port
set_configuration_parameter UMCTL2_A_SYNC_0 1	1st AXI port SYNC interface
set_configuration_parameter UMCTL2_XPI_USE2RAQ_0 1	QoS uses dual RAQ for 1st AXI port
set_configuration_parameter UMCTL2_ASYNC_FIFO_N_SYNC_0 2;# == default value.	
set_configuration_parameter UMCTL2_STATIC_VIR_CH_0 0;# ==default value.	Disable Static VC support for 1st AXI port
set_configuration_parameter UMCTL2_NUM_VIR_CH_0 32	32 dynamic VC support for 1st AXI port
set_configuration_parameter UMCTL2_RRB_EXTRAM_0 1	External RRB SRAM for 1st AXI port
set_configuration_parameter UMCTL2_READ_DATA_INTERLEAVE_EN_0 1; # == default value.	Read data interleave support for 1st AXI port
set_configuration_parameter UMCTL2_AXI_RAQD_0 32	1st AXI port fifo sizing
set_configuration_parameter UMCTL2_AXI_WAQD_0 32	
set_configuration_parameter UMCTL2_AXI_RDQD_0 128	
set_configuration_parameter UMCTL2_AXI_WDQD_0 128	
set_configuration_parameter UMCTL2_AXI_WRQD_0 32	
set_configuration_parameter UMCTL2_A_TYPE_1 3; # == default value.	AXI4
set_configuration_parameter UMCTL2_PORT_DW_1 128	128bit port width for 2nd AXI port
set_configuration_parameter UMCTL2_A_SYNC_1 1	2nd AXI port SYNC interface
set_configuration_parameter UMCTL2_XPI_USE2RAQ_1 0; # == default value.	QoS uses single RAQ for 2nd AXI port
set_configuration_parameter UMCTL2_ASYNC_FIFO_N_SYNC_1 2;# == default value.	
set_configuration_parameter UMCTL2_STATIC_VIR_CH_1 0;# == default value.	Disable Static VC support for 2nd AXI port
set_configuration_parameter UMCTL2_NUM_VIR_CH_1 32	32 dynamic VC support for 2nd AXI port
set_configuration_parameter UMCTL2_RRB_EXTRAM_1 1	External RRB SRAM for 2nd AXI port
set_configuration_parameter UMCTL2_READ_DATA_INTERLEAVE_EN_1 0	Read data interleave support disabled for 2nd AXI port
set_configuration_parameter UMCTL2_AXI_RAQD_1 8	2nd AXI port fifo sizing
set_configuration_parameter UMCTL2_AXI_WAQD_1 32	
set_configuration_parameter UMCTL2_AXI_RDQD_1 16	
set_configuration_parameter UMCTL2_AXI_WDQD_1 128	
set_configuration_parameter UMCTL2_AXI_WRQD_1 32	
set_configuration_parameter MEMC_ENH_CAM_PTR 1;#== default value.	
set_configuration_parameter MEMC_ENH_RDWR_SWITCH 1; #== default value.	
set_configuration_parameter MEMC_RDWR_SWITCH_POL_SEL 1; #== default value.	

Project Information

AP MIPI DSI Host Controller Configuration

Parameter	B
DSI_HOST_AP	1
DSI_HOST_PHY	1
DSI_HOST_DPHY_NUMBER_OF_LANES	4
DSI_HOST_SNPS_PHY	0
DSI_HOST_DATAINTERFACE	4
DSI_HOST_DFLT_F_SYNC_TYPE	2
DSI_HOST_SNPS_SYNC_RD_FIFOS	1
DSI_HOST_DSC_ENC	0
DSI_HOST_PIXELMEMADDRDEPTH	4096
DSI_HOST_GENERICCMDADDRDEPTH	10
DSI_HOST_GENERICPLDADDRDEPTH	64
DSI_HOST_GENERICPLD_RAM_ADDRDEPTH	66
DSI_HOST_GENREADPLDADDRDEPTH	32
DSI_HOST_GENREADPLD_RAM_ADDRDEPTH	34

Project Information

PHY Customization

- Automotive Enhancement, Metal Stack Change
  - C470-0, dwc_mipi_mphy_type1_22_tsmc7ff
  - C391-0, dwc_usbc31dptxphy_tsmc7ffns
  - C236-0, dwc_usb2_femtophy_otg_tsmc7ff18_x1ns

- Support SGMII-1.25Gbps, QSGMII-5Gbps add-on
  - G539-0, DWC AP2 MP16G LP TSMC N7 X4

Project Information

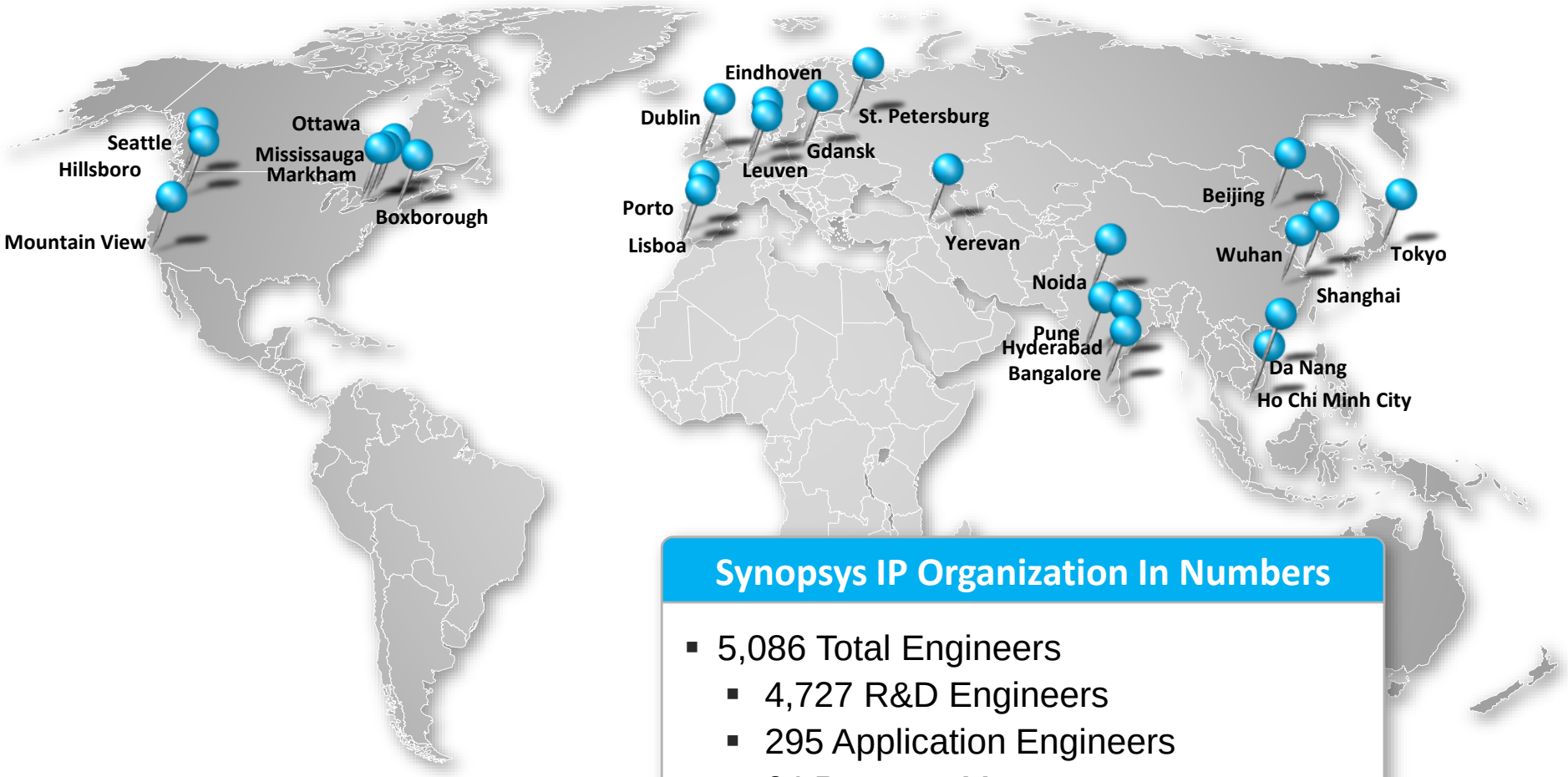
Configuration and Usage Details

- NOTE:

  Horizon’s project milestones are still TBD, SNPS team will continue to actively follow up to ensure that the internal information is consistent with the Horizon project schedule.

IP Support

Global IP Development And Support



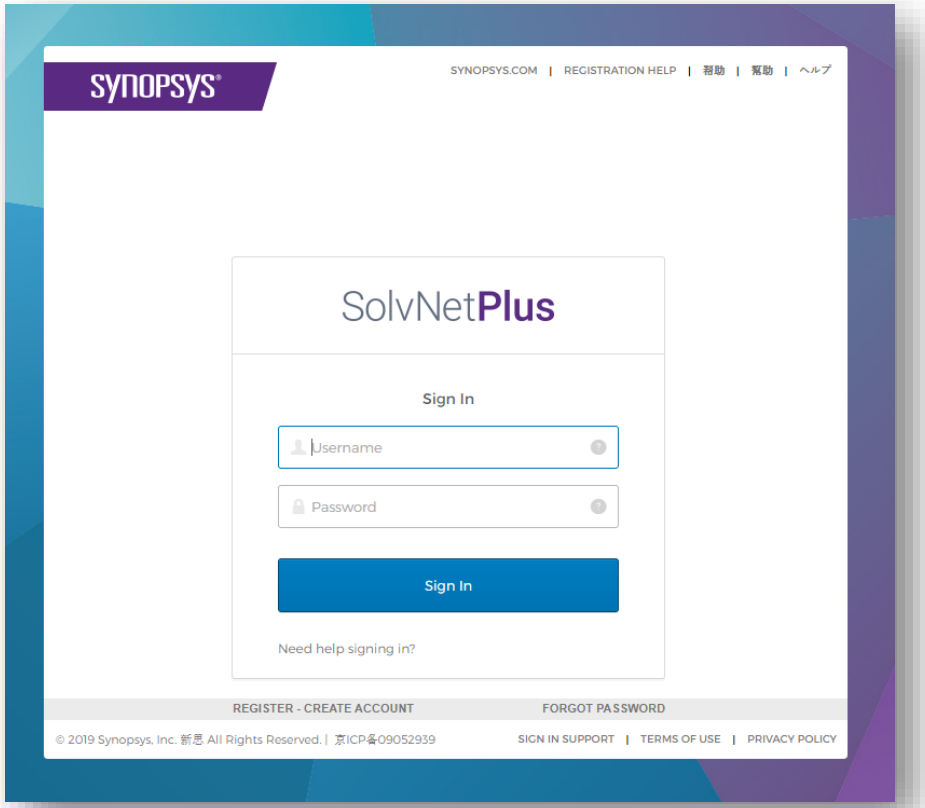
Synopsys IP Organization In Numbers

- 5,086 Total Engineers
  - 4,727 R&D Engineers
  - 295 Application Engineers
  - 64 Program Managers

Technical Support

- Provided by product experts supporting inquiries on
  - Protocol
  - Product architecture, features, specs,
  - Integration, implementation and simulation guidance
  - Silicon bring-up

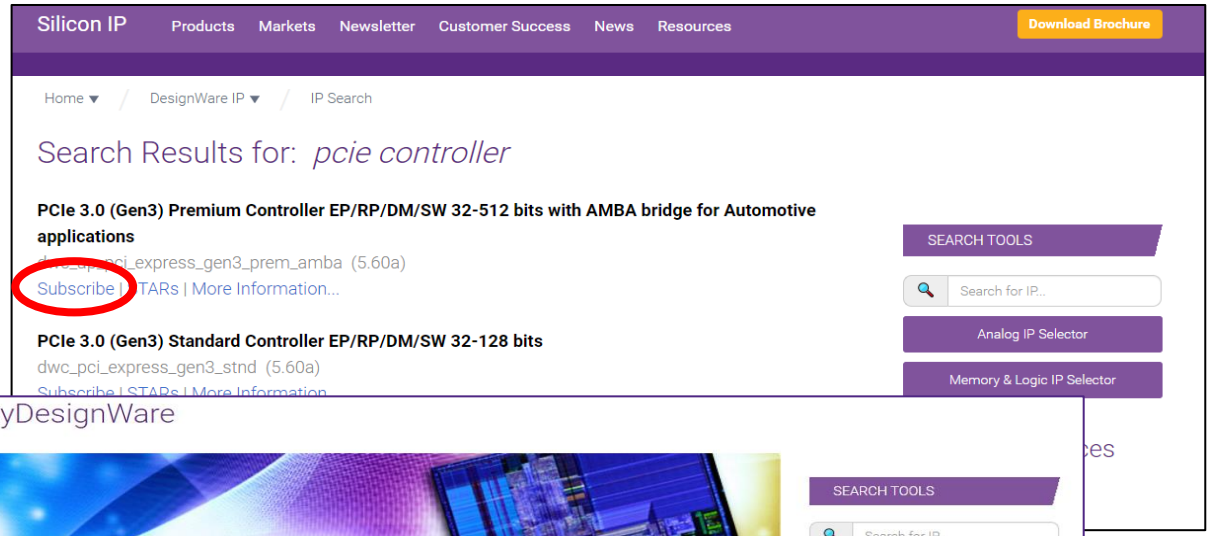
- SolvNetPlus CRM
  - Main support channel
  - Advanced knowledgebase search
  - Conference calls for in-depth discussions
  - Supplemented by IP designers when deeper design know-how required
  - Detailed SolvNetPlus usage instructions are here

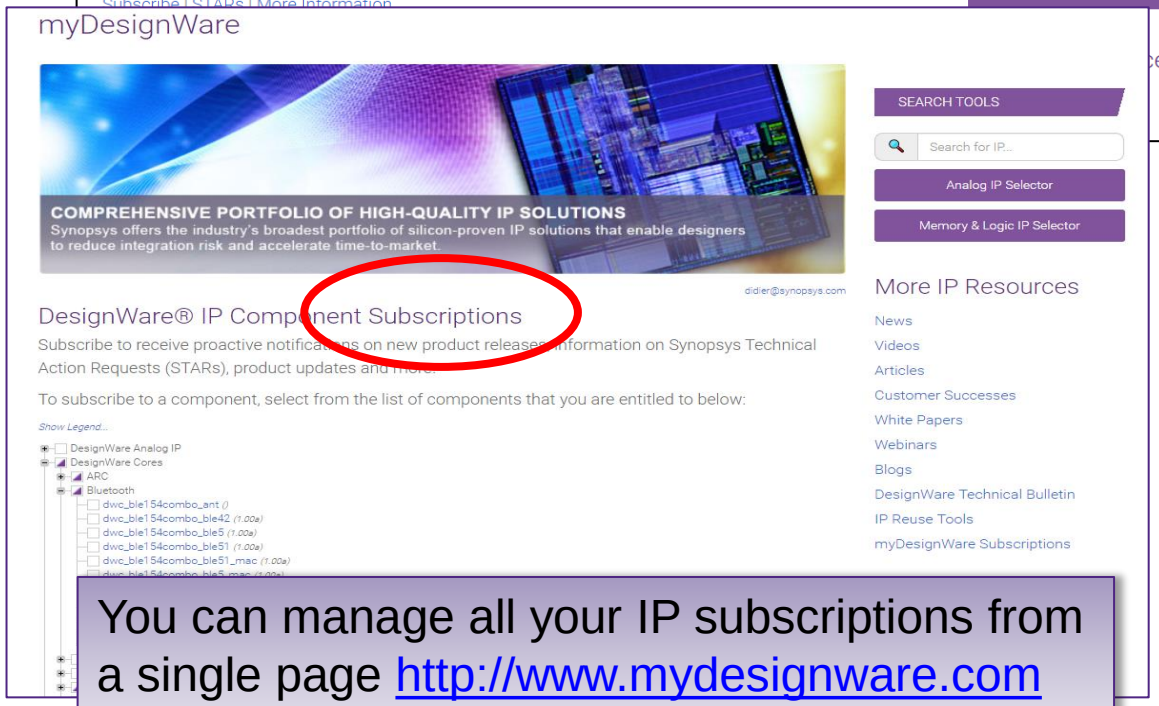


SolvNetPlus
solvnetplus.synopsys.com

Subscribe to IP Notifications

- http://www.mydesignware.com

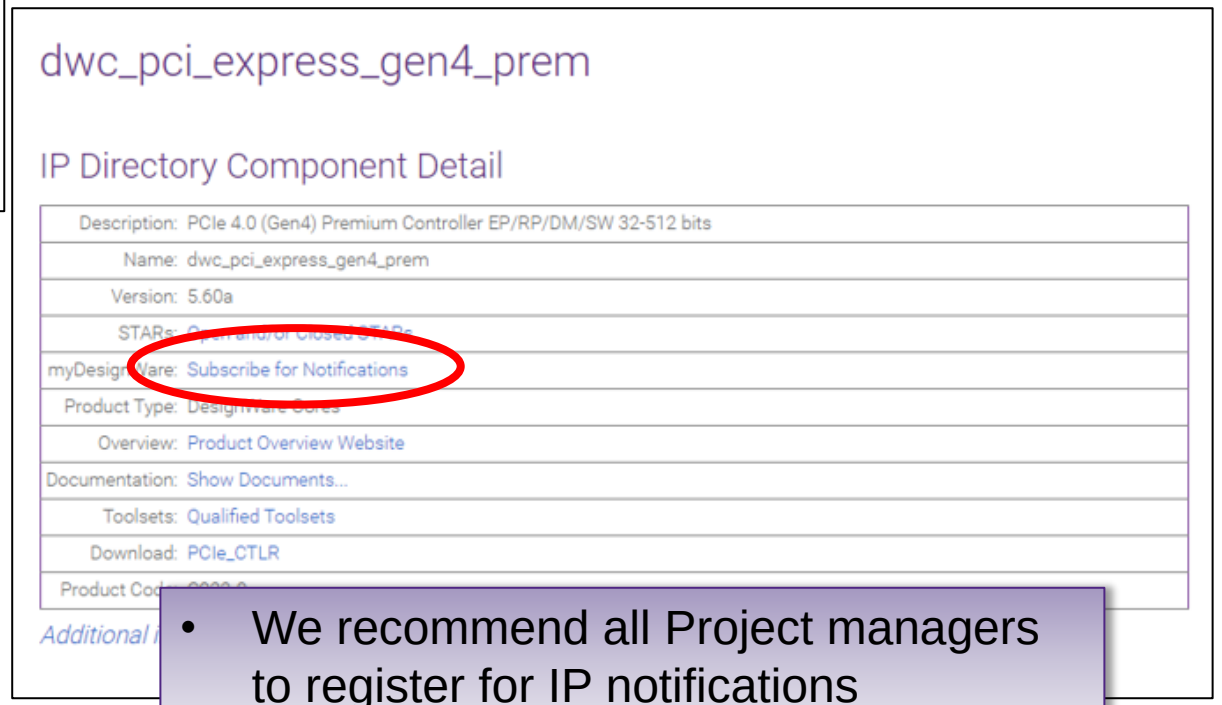




You can manage all your IP subscriptions from a single page http://www.mydesignware.com

Several ways to subscribe …

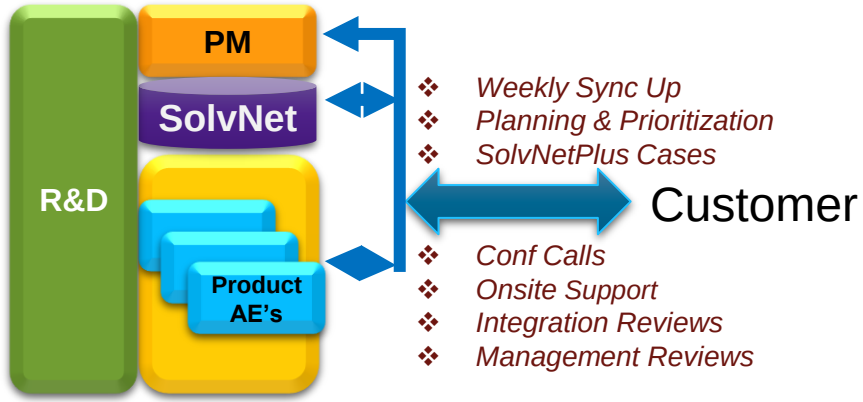
- You will receive notification emails for each event on the selected IP(s), eg a new release was published, or new STAR was found.
- Once subscribed, you will continue to receive notification emails even after your maintenance has expired, … until you unsubscribe



- We recommend all Project managers to register for IP notifications

Program Manager

Michael Yang



- SNPS's official channel for
  - Communicating Plan of Record & Schedule
  - Tracking the development and delivery of commitments in the SOW
  - Communicating internally and to Customer any changes to the plan of record
  - Publishing weekly program tracking reports
  - Change resolution process
- Customer's focal point for
  - Escalating issues & actions
  - Pulling in the designated experts as required
  - Coordinating special-topic technical meetings & reviews
  - Tracking actions and follow up
  - Mitigation plans of identified risks
  - Focusing SNPS teams in alignment with priorities and critical milestones

IP Training & Integration Reviews

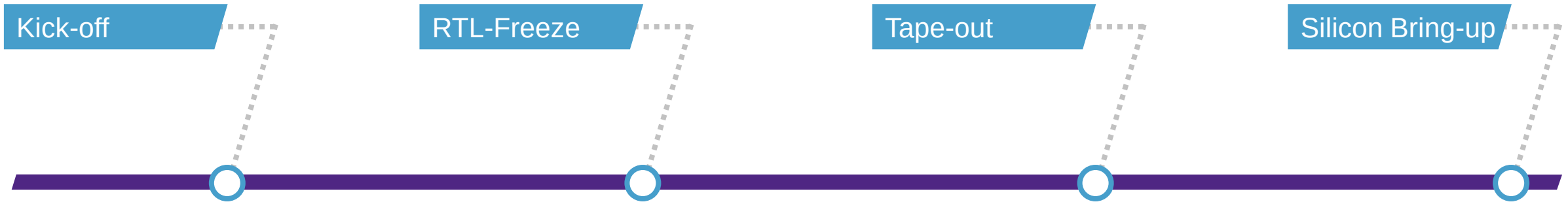
Close Partnership for Success

Align support plan at start & throughout the SOC design, verification & silicon bring-up

Plan & deploy the most effective support solutions by understanding design goals, challenges and risk items

Continuously adapt to project needs by proactive communication of SoC design milestones

Close Partnership for Success



	Kick-off	RTL-Freeze		Tape-out	Silicon Bring-up
IP Solution Support	**I**P Kick-off & Training **C**onfiguration Review **D**FT architecture Review (SMS/SHS)	**L**ogical Review **C**onstraints Review **F**loorplan Review	**S**MS Insertion Review **S**oC level SMS pattern Review	**P**ost P&R STA Review **G**DS/Layout Review **E**SD Review	**P**ackage & PCB Review **S**ignal / Power Integrity Review
IP Accelerated	**I**P Subsystems **I**P Prototyping Kits **S**oC Architecture	**I**P Hardening **S**ignal / Power Integrity Analysis			**S**ilicon Bring-up Services

IP Solution Support

IP TRAINING

- **Part of IP Core Support**
- **Interface IP**: Architecture; Usage & Integration; IP Configuration Guidance – register programming
- **Foundation IP**: Memory Compiler/Library portfolio, features & options; Instance/Library selection choice for optimal QoR; SMS training & customized consulting
- **Getting started on the IP**: Installing and understanding the IP deliverables

IP INTEGRATION REVIEWS

- **Part of IP Core Support**
- **Visual reviews based on detailed checklists** to ensure all IP integration & implementation & verification steps completed successfully
- Offering **timely guidance** in the initial, intermediate and final phases of project
- Avoids lengthy silicon debug cycles and expensive re-spins

Significantly reduce the risk of IP integration issues by including Synopsys reviews in your project plan

IP Training: DDR Signal & Power Integrity

DDR Interface

- Interface overview
- DDR Signal Types
- DDRn Synchronous Signaling

PHY IO ring implementation

- PHY SSTL IO library cell overview
- SSTL IO library Si/Pi features
- Si/Pi design constraints on IO ring
- ESD constraints
- Documentation overview

Implementation challenges

- Signal Integrity issues cause “real” problems
- Timing uncertainty
- Regions of timing uncertainty
- Static vs Dynamic uncertainty
- Sources of dynamic interconnect uncertainty

System Implementation

- PCB
- Package
- Skew
- Crosstalk
- Reflections
- Power delivery
- Decoupling
- Vref and VTT

Timing Budgets Calculation

- Timing Relationships
- Timing Budget
  - Read
  - Write
  - Command & Address (CA)
  - CK/CK# to DQS/DQS#

SI/PI Simulations

- Types of simulations
- Common conditions
- Interface model
- Example

IP programmability to improve SI/PI

- Data training
  - Deskew & Strobe Centering
  - Read/Write Leveling
  - VREF training
- IO related
  - Slew-rate control
  - ODT, Zout
- 2T timing
- Data bus inversion

Training slides are typically provided to customers for offline self-pace review, followed by Q&A either offline and/or live meetings to address follow-on questions

IP Integration Reviews

Collaborate to Succeed

Type Of Review	Applicable To	Purpose	Recommended Timeframe
IP Configuration	Solution: Controller + PHY	Review to ensure chosen configuration is suitable for application and there are no gross errors in selection (e.g., performance related parameters)	Project Start (after configuration has been finalized)
Logical Integration	Solution	Visual review of interconnections between controller, PHY, memories, etc.; connectivity for clocks, resets, debug access, Custom I/O and SoC interface; ensure proper connectivity across critical signals; review simulation results etc.	Minimum 4 weeks prior to RTL Freeze
Constraints	Solution	Review usage of combined PHY + controller SDC, deviations from SNPS provided deliverables, guidance to address violations/errors etc.	Minimum 4 weeks prior to RTL Freeze
SMS Insertion	SMS	Review the MBIST architecture and the insertion of various SMS components i.e. Server, sub-server, processors, wrapper etc.. Ensure that connectivity check patterns are validated successfully.	Minimum 4 weeks prior to RTL Freeze
SoC level SMS Pattern	SMS	Review the MBIST test pattern generation strategy considering factors like test time and peak power, provide guidance to optimize the patterns	Minimum 4 weeks prior to RTL Freeze
Floorplan	Solution	High level review of PHY + controller combined floorplan for improved routability, SI etc.	Minimum 4 weeks prior to RTL Freeze
Post P&R STA	Solution	Review detailed STA reports for the PHY + controller combo, ensure that constraints, and timing slacks are adequate across PVT	Minimum 4 weeks prior to tapeout

Customer owns all tool based Subsystem/SoC integration checks

IP Integration Reviews (cont.)

Collaborate to Succeed

Type Of Review	Applicable To	Purpose	Recommended Timeframe
GDS/Layout	PHY+PADs	Review physical layout for recommended guidelines (e.g.,RDL, supply/gnd isolation, clamps, clock nets, DRC/LVS waivers etc.)	Minimum 2 weeks prior to tapeout
ESD	PHY+PADs	ASIC-level ESD review to check for power/gnd assignments, cross-domain protections, SoC's ESD-ground etc.	Minimum 2 weeks prior to tapeout
Pre-TO	Solution	Final check to verify IP version, access to debug ports, Clk/Rst connectivity, any open STARs and sanity check	Minimum of 1 week prior to tapeout
Package / PCB	SoC	Visual review of customer's interface floorplan, package/PCB physical design, including guidelines for stack-up, signal trace width and impedance, power distribution network, reference clock routing to PHY, crosstalk mitigation, etc. Review floorplan at package/PCB pre-layout stage, follow by preliminary layout review, and a final layout review on improvements	After floorplan review
Signal and Power Integrity	TX/RX IO, Interposer, Package, PCB, RX/TX IOs (as applicable)	Review customer's SI/PI simulation report, assessing simulation coverage, results quality against pass criteria. An initial review of the simulation methodology and coverage, and a final review to verify the improvements	After package, PCB and interposer reviews

Flow for IP Integration Reviews

Customer – Opens a SolvNetPlus case

- Specify project name
- Specify type of review requested
- Provide (upload) info to be reviewed

SNPS

- Communicates through SolvNetPlus case if further information is needed
- Carefully reviews the data & provides feedback through SolvNetPlus case
- Typical duration: 3 to 5 business days

SNPS

- Provides review comments to customer through SolvNetPlus
- Customer may request a WebEx call if desired

Final Review (optional)

- After customer implements review recommendations a final review is carried out, to ensure all items were properly addressed
- Typical duration: 5 to 7 business days

Silicon Bring-up Service

Thorough Pre- to Post- Silicon Package

SI BRING-UP PLAN REVIEW

Align Schedule
Anticipate Needs
Structure Plan by Stages
Test Setup
Test Equipment
Test Sequence

Pre-silicon

PREEMPTIVE ON-SITE EXPERTISE

Synopsys Engr. on-site
Specific location & period
Broad scope of expertise
Short iteration cycles

Post-silicon

SI BRING-UP TECHN. MGMT.

Track & manage progress
Accelerated analysis & resolution

Post-silicon

Synopsys Engineer Offering Broad Expertise

Protocol and Conformance Test Suite

Package and PCB

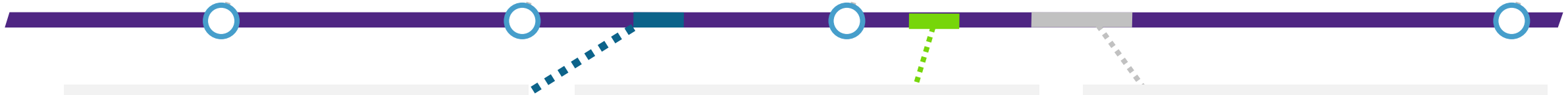
Laboratory and metrology

IP integration and usage requirements (RTL to Silicon)

Direct contact window to the multidisciplinary team designing and supporting the IP Solution

Silicon Bring-up Service - Thorough Pre- to Post- Silicon Package

Kick-off | Tape-out | Silicon Bring-up | Production



SI BRING-UP PLAN REVIEW

Align Schedule
Anticipate Needs
Structure Plan by Stages
Test Setup
Test Equipment
Test Sequence

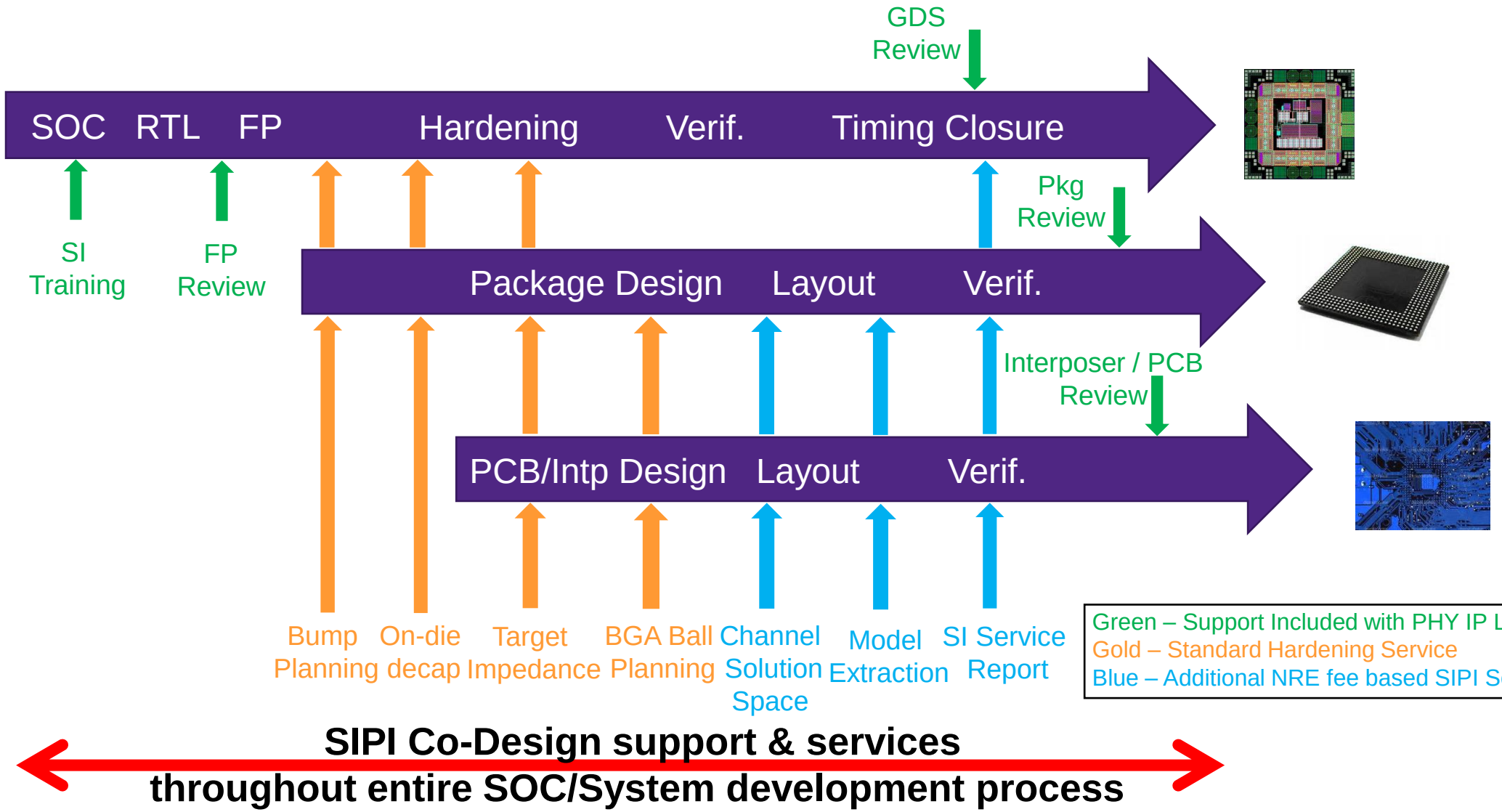
PREEMPTIVE ON-SITE EXPERTISE

Consultant on-site
Specified location & period
Broad scope of expertise
Short iteration cycles

SI BRING-UP TECHN. MGMT.

Track & manage progress
Accelerated analysis & resolution

Signal / Power Integrity Analysis Support & Service



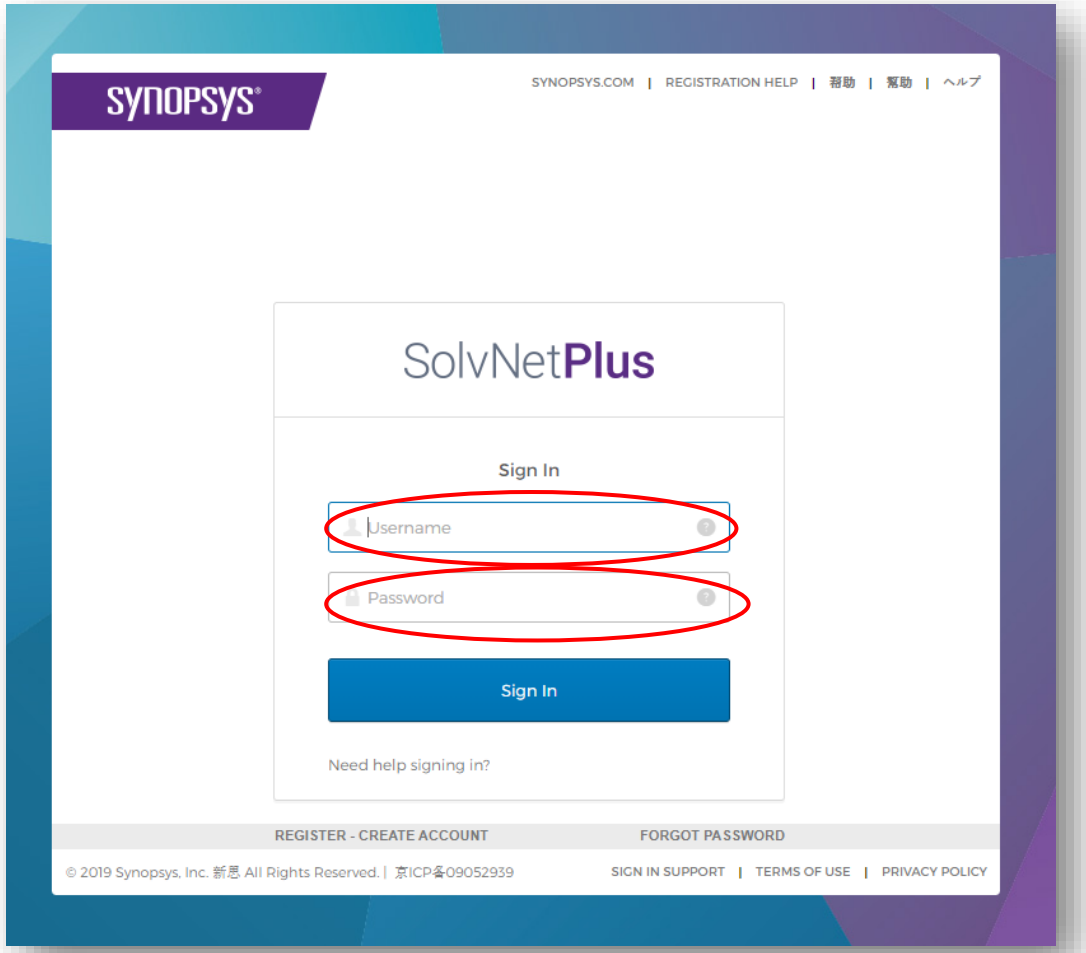
Summary

- Close partnership for success
- Plan & deploy the most effective support solutions by understanding design goals, challenges and risk items
- Continuously adapt to project needs by proactive communication of SoC design milestones
- Quickly get up to speed on new IP usage and integration with IP Training
- Avoid lengthy silicon debugs and respins by taking advantage of offered reviews
- Accelerate IP integration and success through available customizable services

IP Documentation, Download and Notifications

DesignWare IP info Page

http://www.mydesignware.com

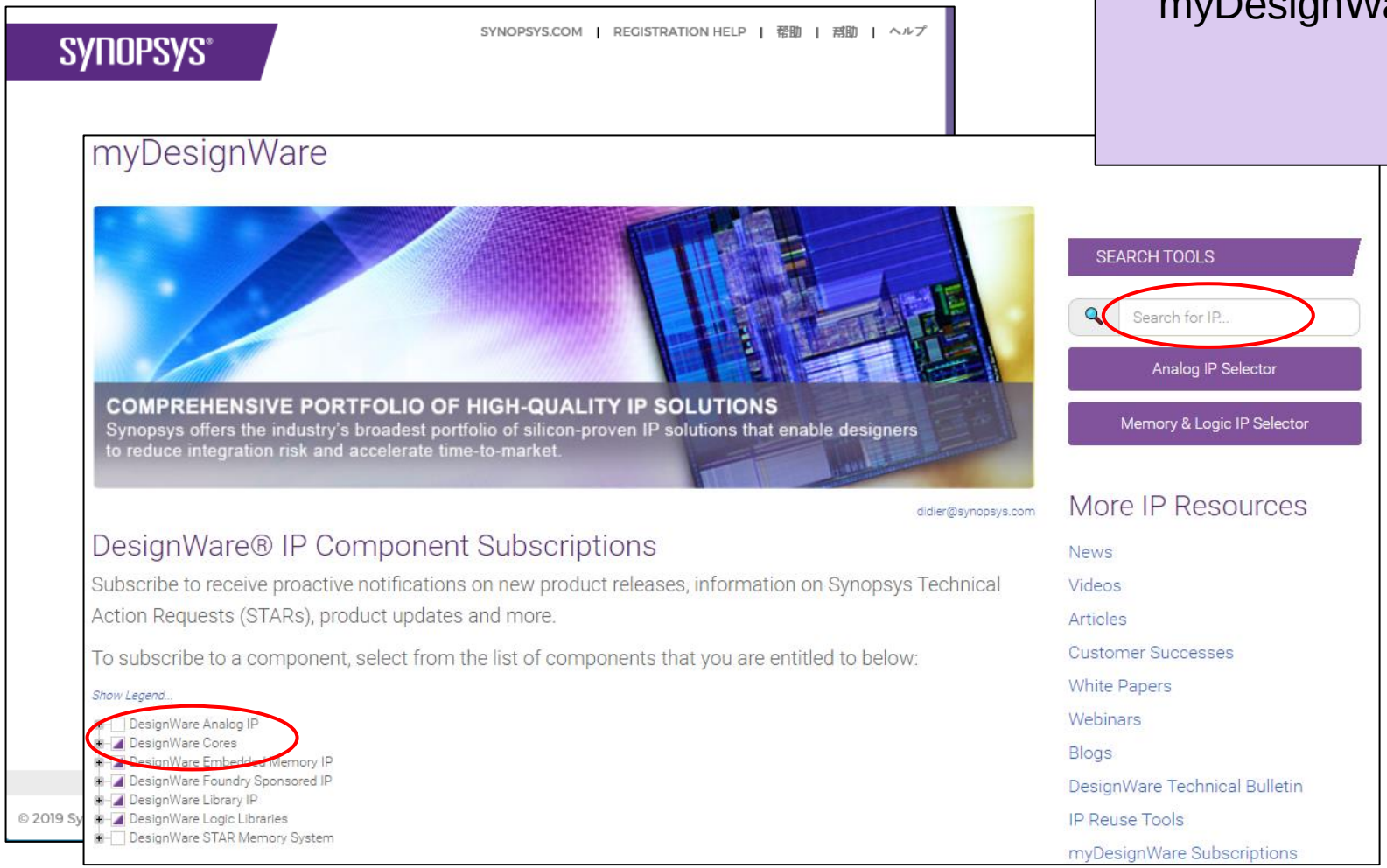


- Login to myDesignWare.com with your SolvNetPlus user ID and password

DesignWare IP info Page

http://www.mydesignware.com

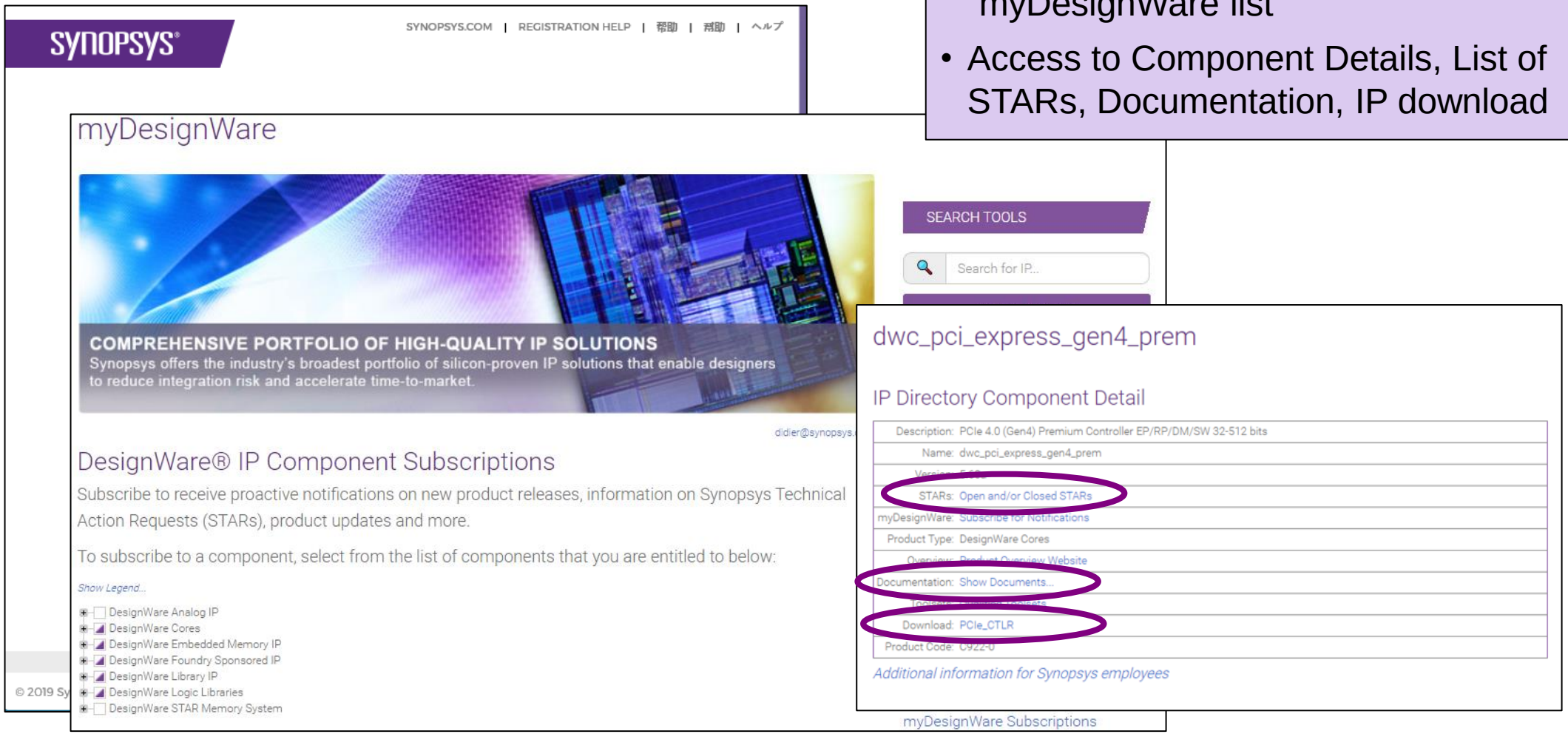
- Login to myDesignWare.com with your SolvNetPlus user ID and password
- Search for your IP or select it from your “myDesignWare list



DesignWare IP info Page

http://www.mydesignware.com

- Login to myDesignWare.com with your SolvNetPlus user ID and password
- Search for your IP or select it from your “myDesignWare list
- Access to Component Details, List of STARs, Documentation, IP download

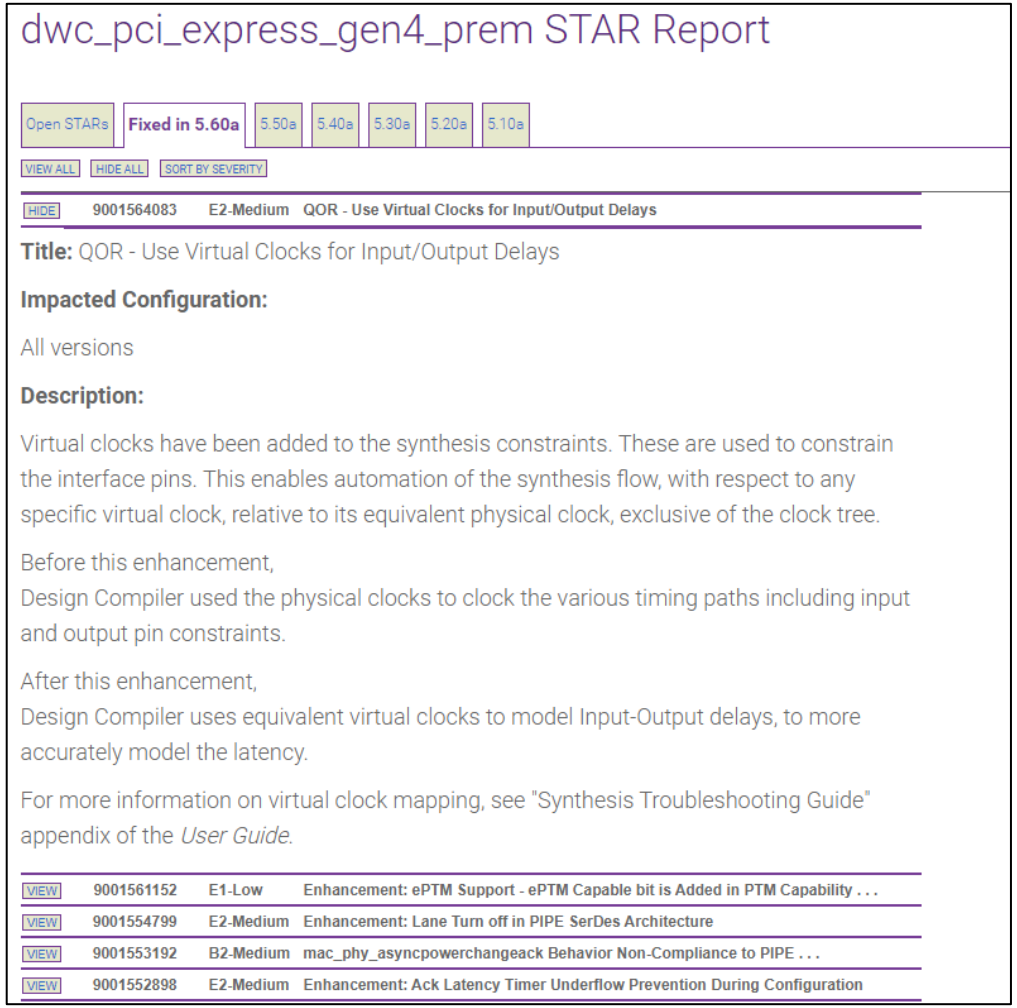


Access to STARs On-The-WEB

- http://www.mydesignware.com

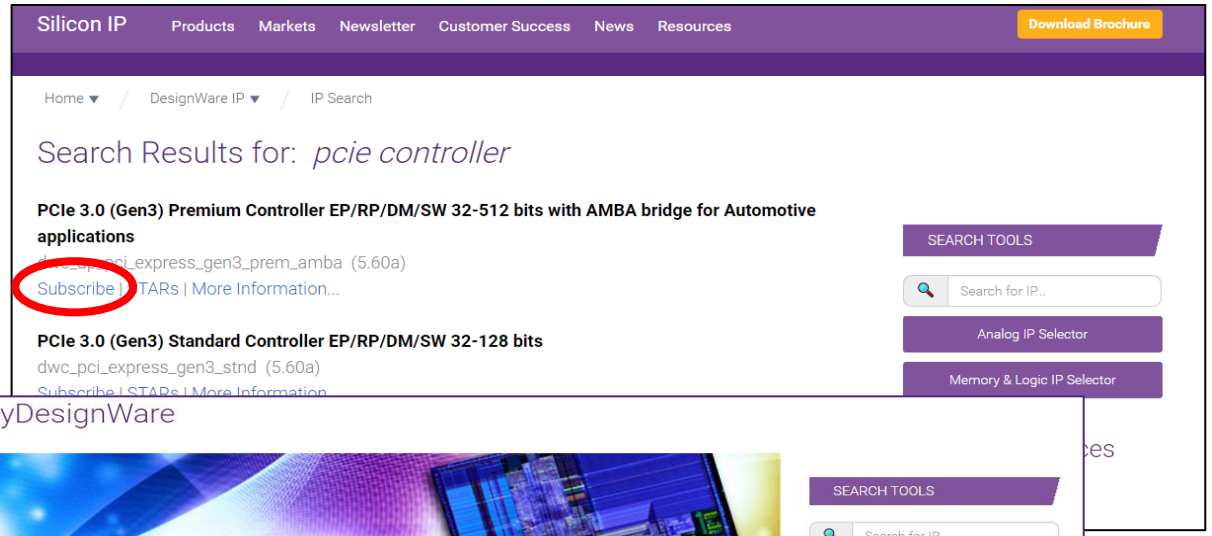
Lists of Open and Fixed STARs

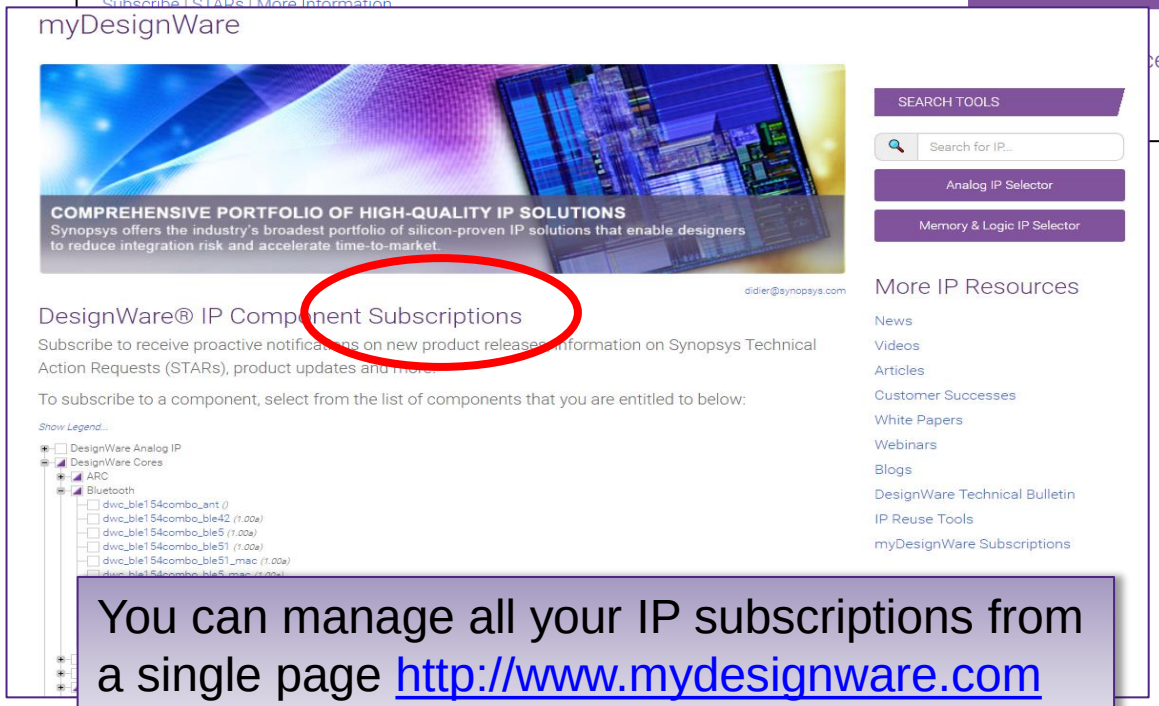
- By release version
- Click to get more details
  - Description
  - Versions
  - Configurations affected
  - Workaround
  - Target Fix
- More details may be available from the Support Team (open a SolvNetPlus case)



Subscribe to IP Notifications

- http://www.mydesignware.com

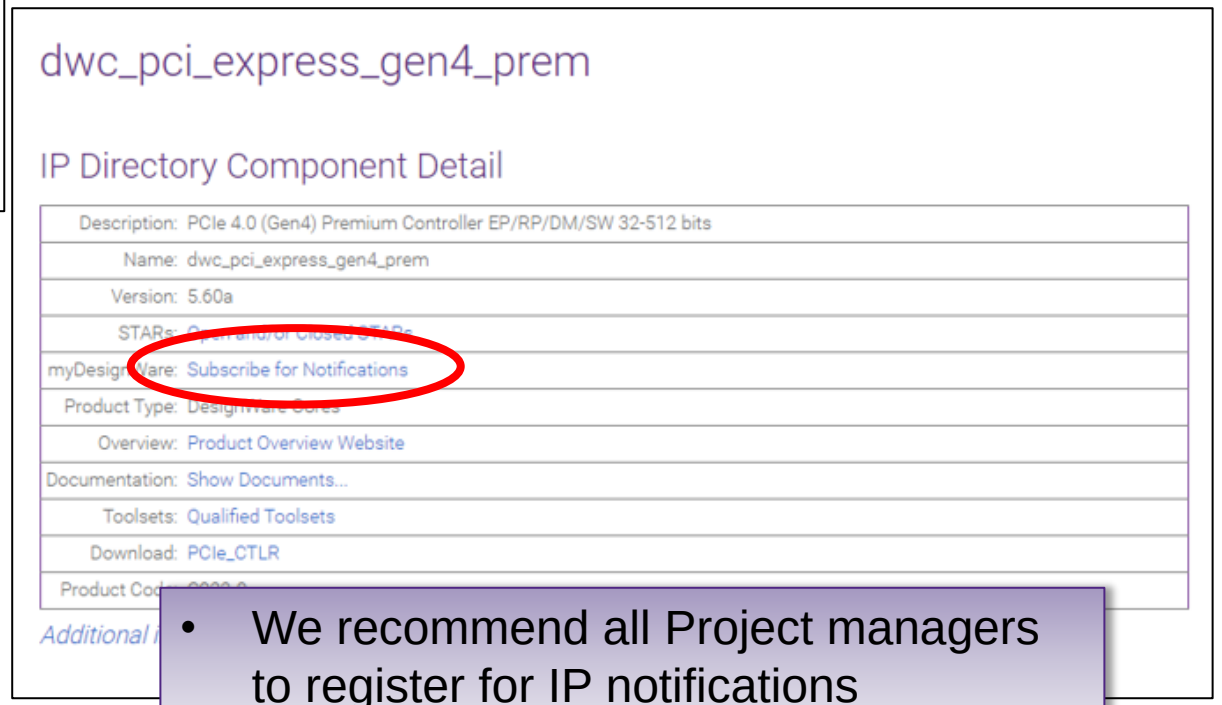




You can manage all your IP subscriptions from a single page http://www.mydesignware.com

Several ways to subscribe …

- You will receive notification emails for each event on the selected IP(s), eg a new release was published, or new STAR was found.
- Once subscribed, you will continue to receive notification emails even after your maintenance has expired, … until you unsubscribe



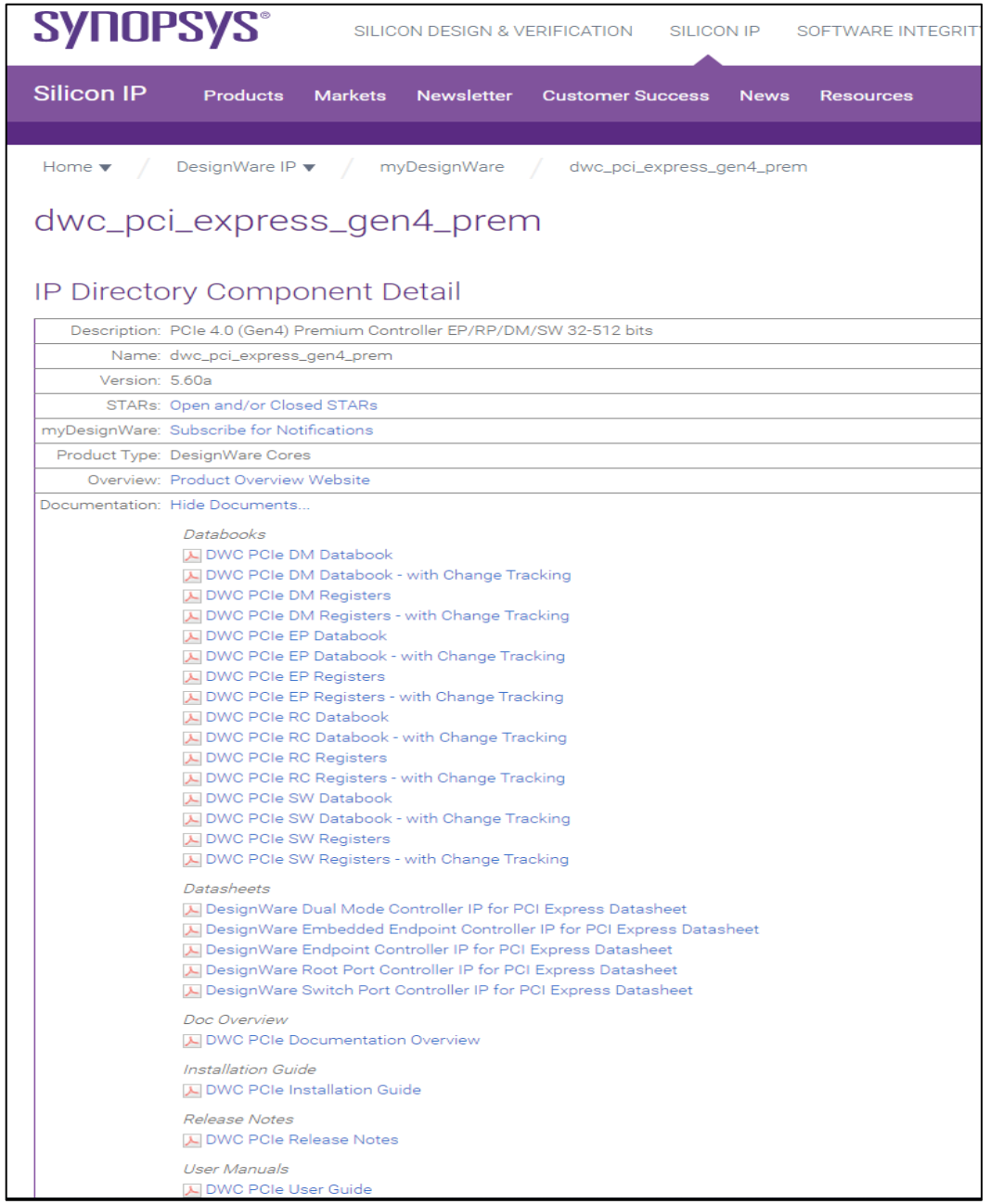
- We recommend all Project managers to register for IP notifications

Access to IP Documentation

- http://www.mydesignware.com

IP Documentation

- Data books
- Users Manual
- Installation guide
- Release Notes
- Application Notes …



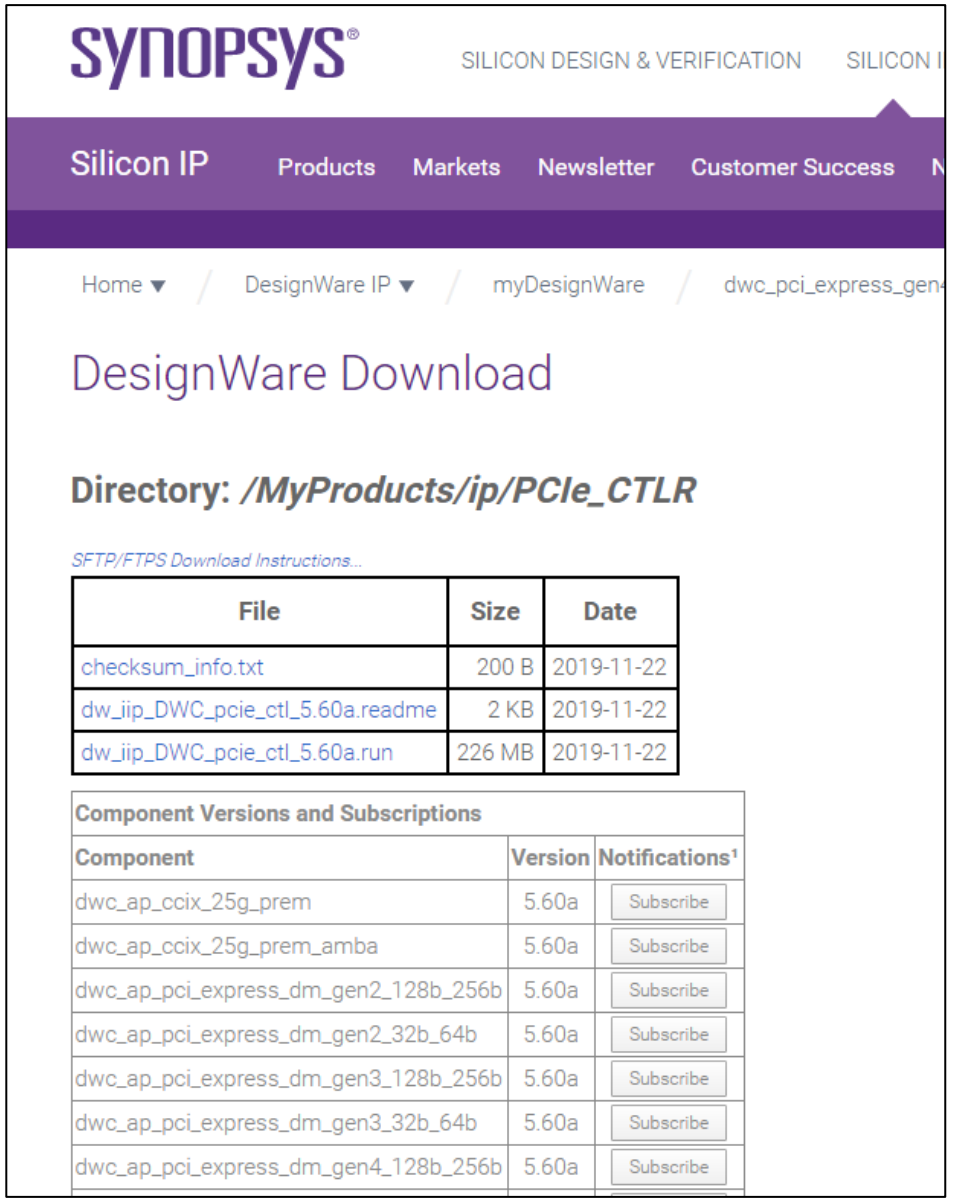
Downloading the IP

- http://www.mydesignware.com

Check Readme file first

```
This directory contains a .run file which is a self-extracting image that
contains a DesignWare IP product. The most recent version of this product
is also always available at the following URL:

  https://www.synopsys.com/dw/dwdl.php?e=PCIe_CTLR

To install this DesignWare IP product, download this file from the above
website or this FTP directory to a UNIX file server:

  dw_iip_DWC_pcie_ctl_5.60a.run

Then issue the following command from a UNIX shell to view information
about .run command syntax:

  % ./dw_iip_DWC_pcie_ctl_5.60a.run --help

Problems?
---------
o If the .run file does not execute properly, check your permissions.
  Some browsers do not set execute permission for downloaded files.

o Did the installation fail asking for a license?  Make sure you have received
  a "project ID" string from your sales representative, a FLEXlm key specific
  to this product, and make sure LM_LICENSE_FILE or SNPSLMD_LICENSE_FILE is
  pointing at the correct license server for that key.
```

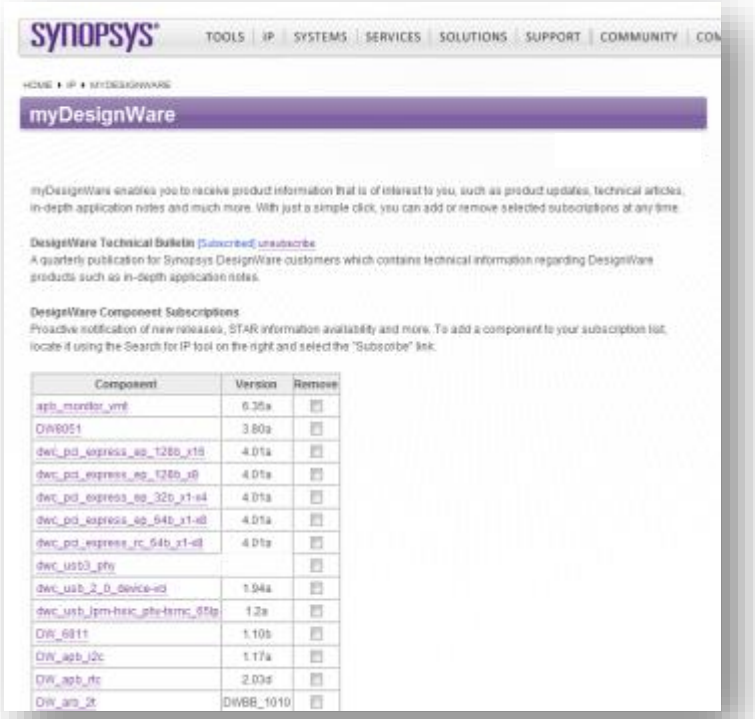
See Back up Slides
For more details on IP
download and installation



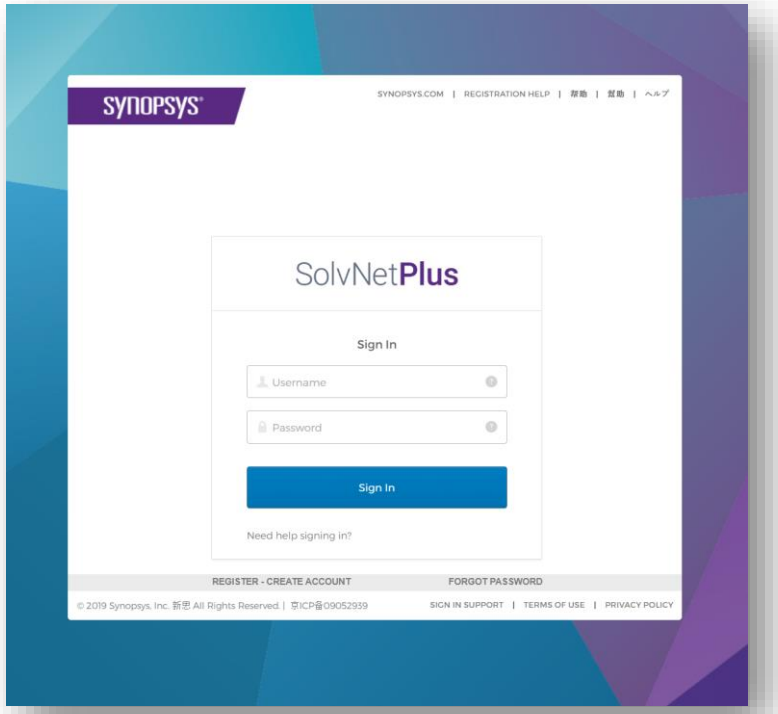
Support Resources Available Online

Comprehensive Online Support

myDesignWare
Subscribe for proactive release and bug fix notifications



SolvNetPlus
Synopsys Support Portal



STARs On-The-Web
Complete Transparency on bugs

DesignWare IP Support

For products under a valid core support agreement

ONLINE

solvnetplus.synopsys.com

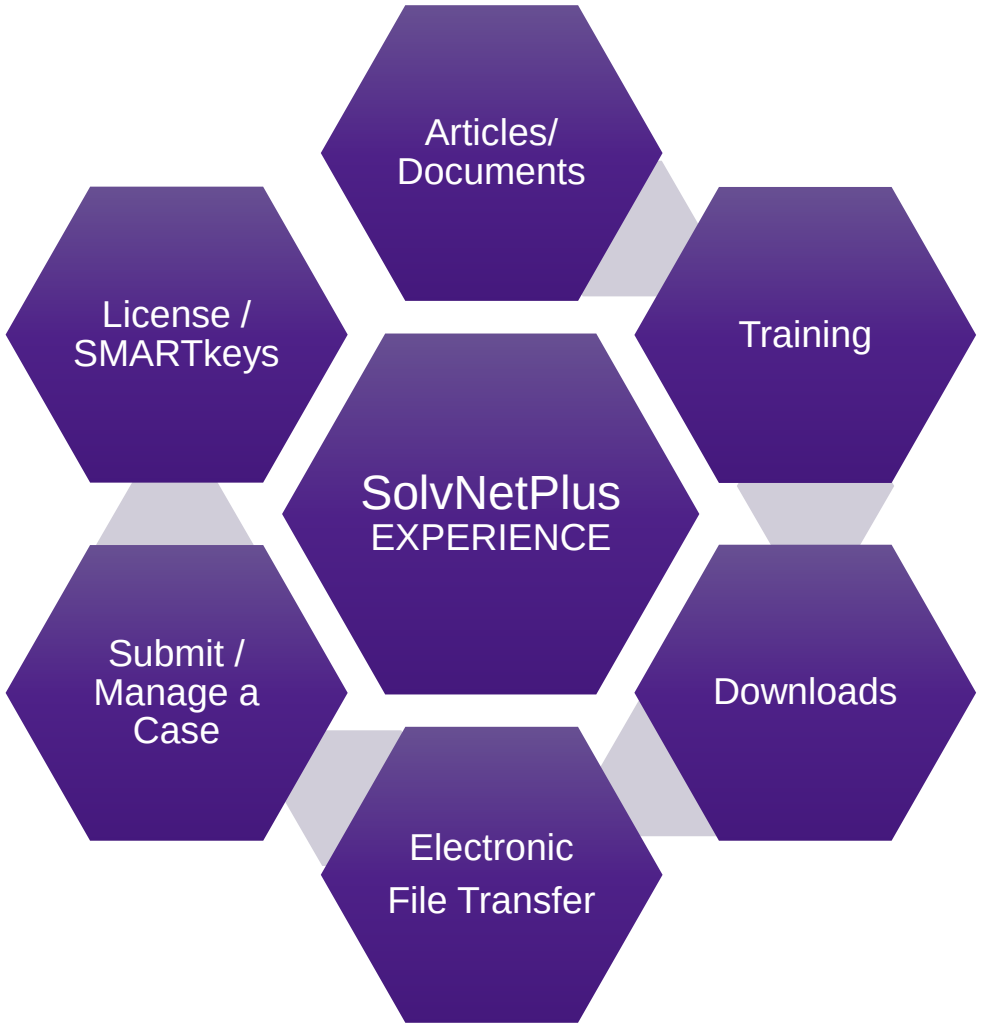
Most efficient method
Extensive Knowledgebase
Support by Worldwide Experts
Acknowledged Within 24hrs

EMAIL

support_center@synopsys.com

Opens SovNetPlus case
Less efficient routing

SolvNetPlus

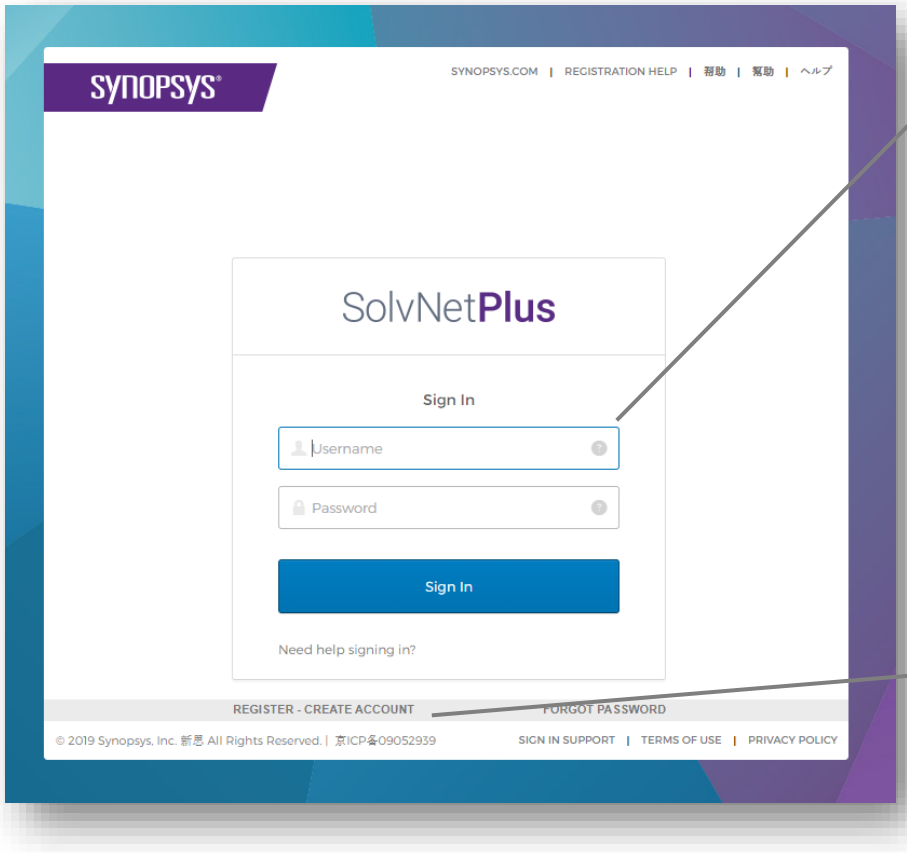


SYNOPSYS®

Integrated Customer Experience Platform

- Enhanced Search Experience
- Curated Technical Content
- Improved Case Self Service
- Intelligent Recommendations
- Secure Access

SolvNetPlus solvnetplus.synopsys.com



Login with SolvNet(Plus) credentials

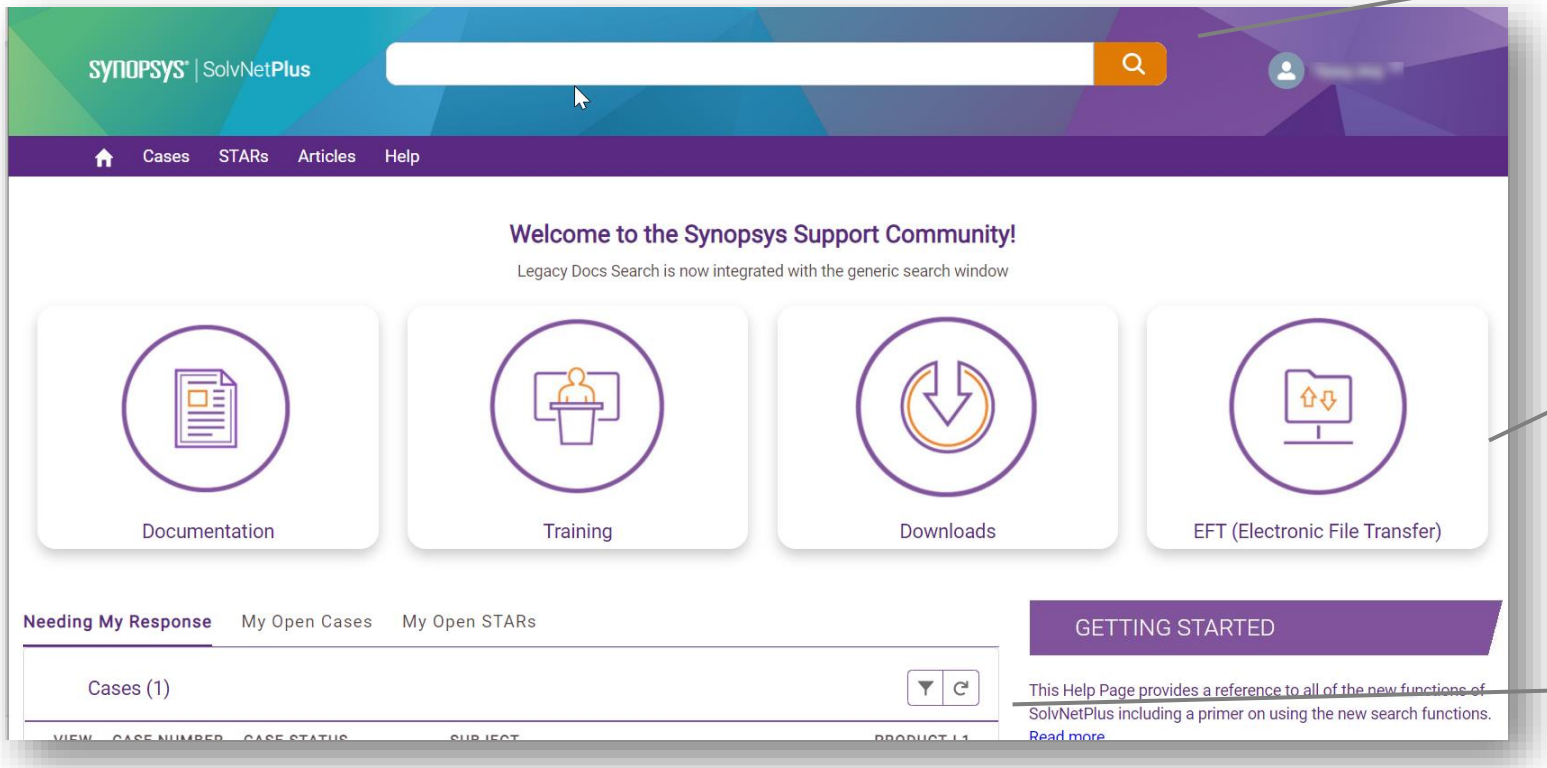
Register if you need an account

SYNOPSYS®

Integrated Customer Experience Platform

- Product support portal
- Search knowledgebase for licensed products
- Initiate a support case
- Manage support cases
- Keep track of STARs

SolvNetPlus Overview

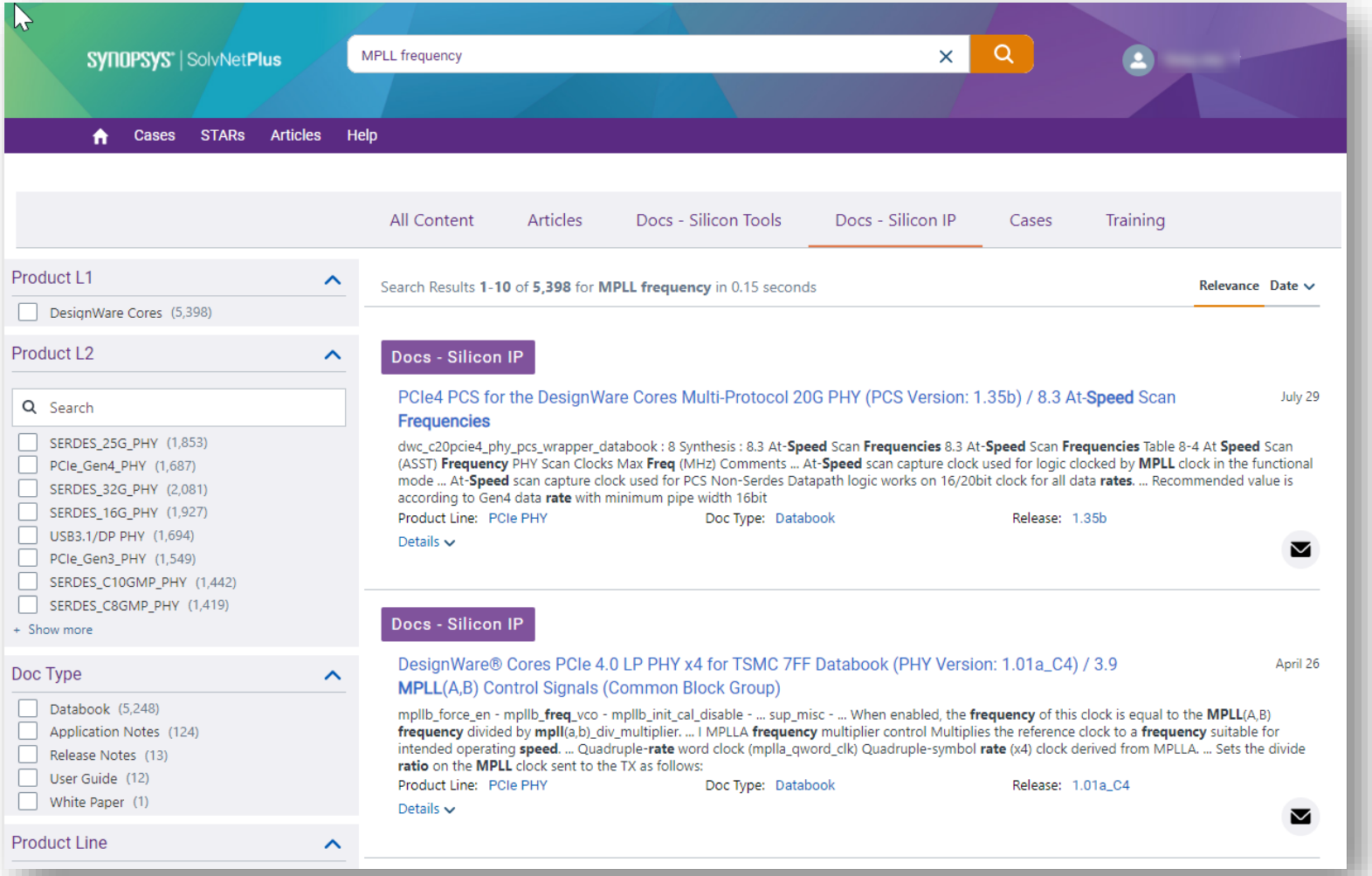


Advanced knowledgebase search

Navigate to resources

View cases and STARs

SolvNetPlus Knowledgebase Search



SYNOPSYS®

Key Highlights

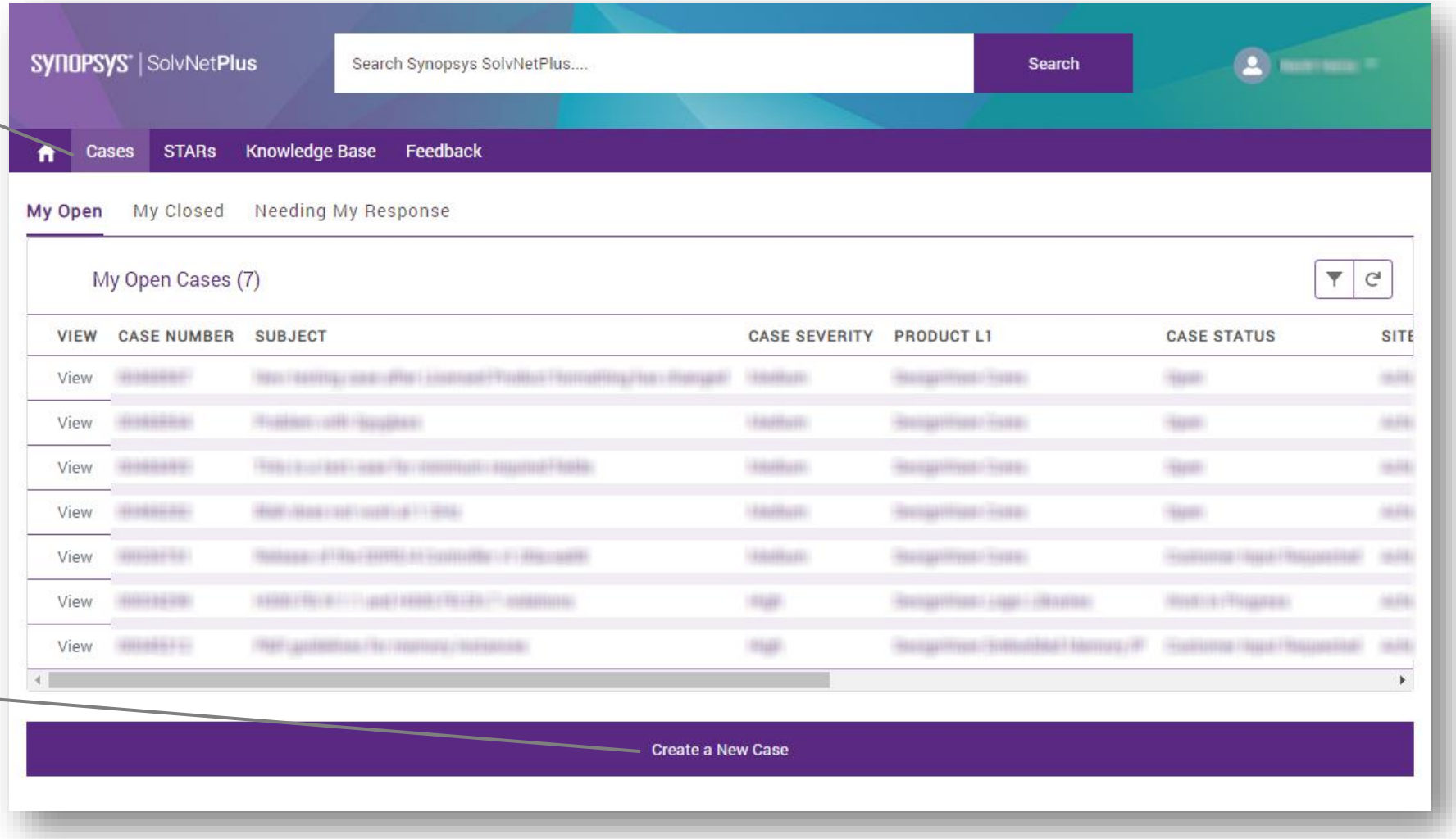
- **Single search interface**
  Aggregates results from multiple sources
  - Knowledge Articles
  - Documentation
  - Training
  - Cases & STARs
- **Filters and facets**
  Narrow down results
- **Case self-service**
  Recommends context-based knowledge solutions
- **Advanced ML capabilities**
  Help improve relevance of results over time

SolvNetPlus Create a New Case (1)

Getting started

Navigate to cases

Click to create a case

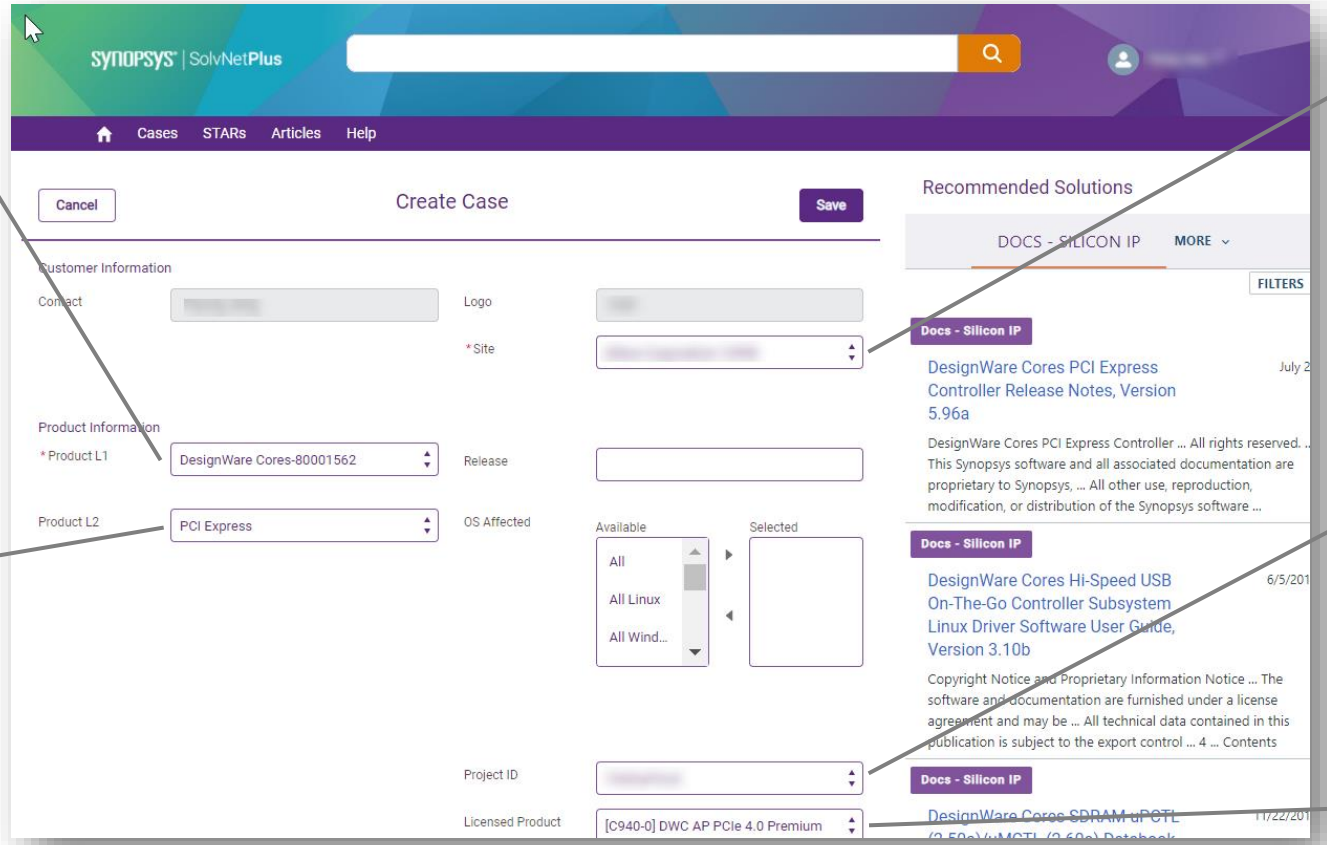


SolvNetPlus Create a New Case (2)

Enter contact, project ID and product information

Select Appropriate Product Category

Select Product Family or Type



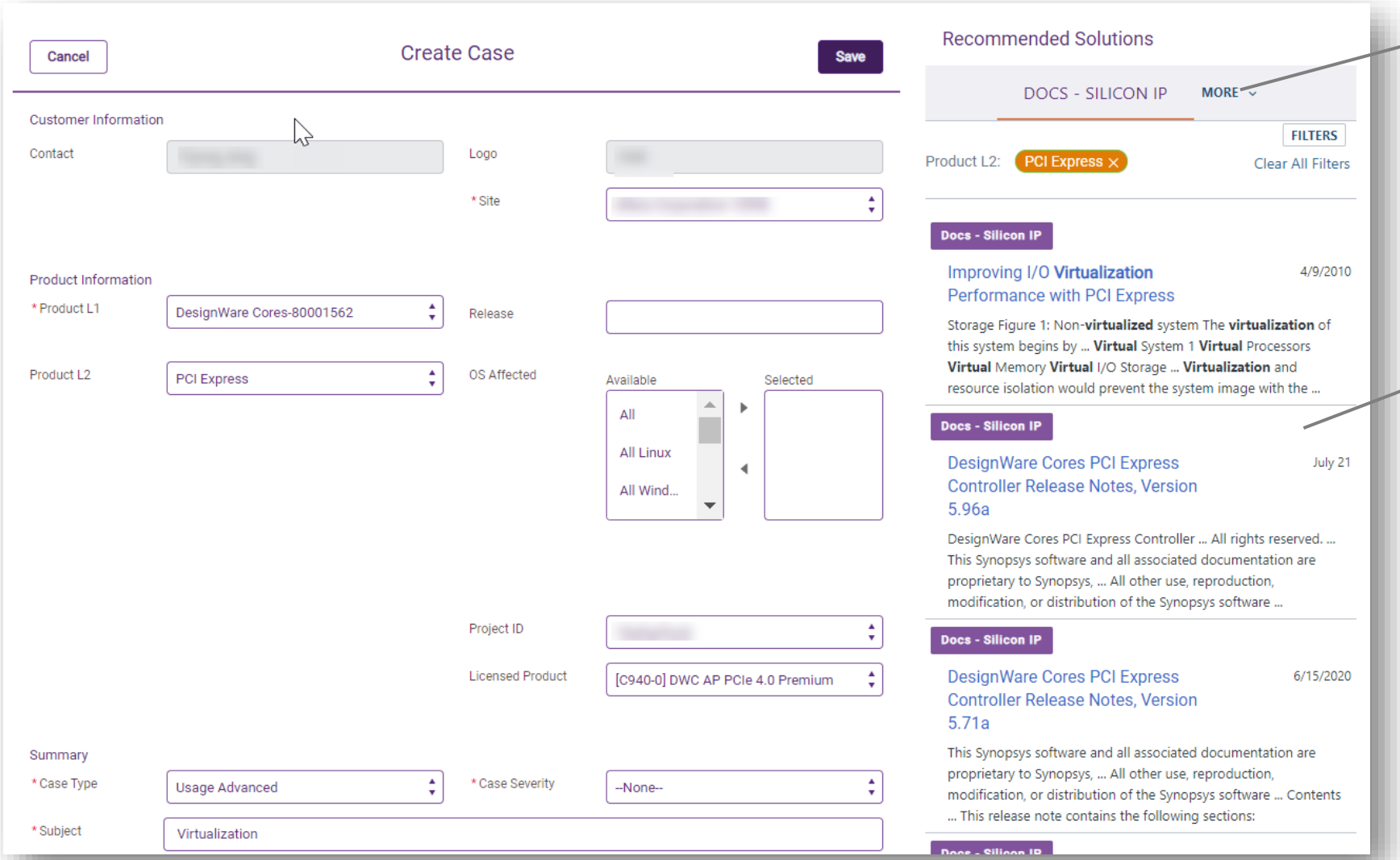
Select Site where IP is licensed

Select your Project ID

Select the Licensed Product

SolvNetPlus Create a New Case (3)

Accelerate Issue Resolution with Knowledge Recommendations



Select Sources and filter with facets

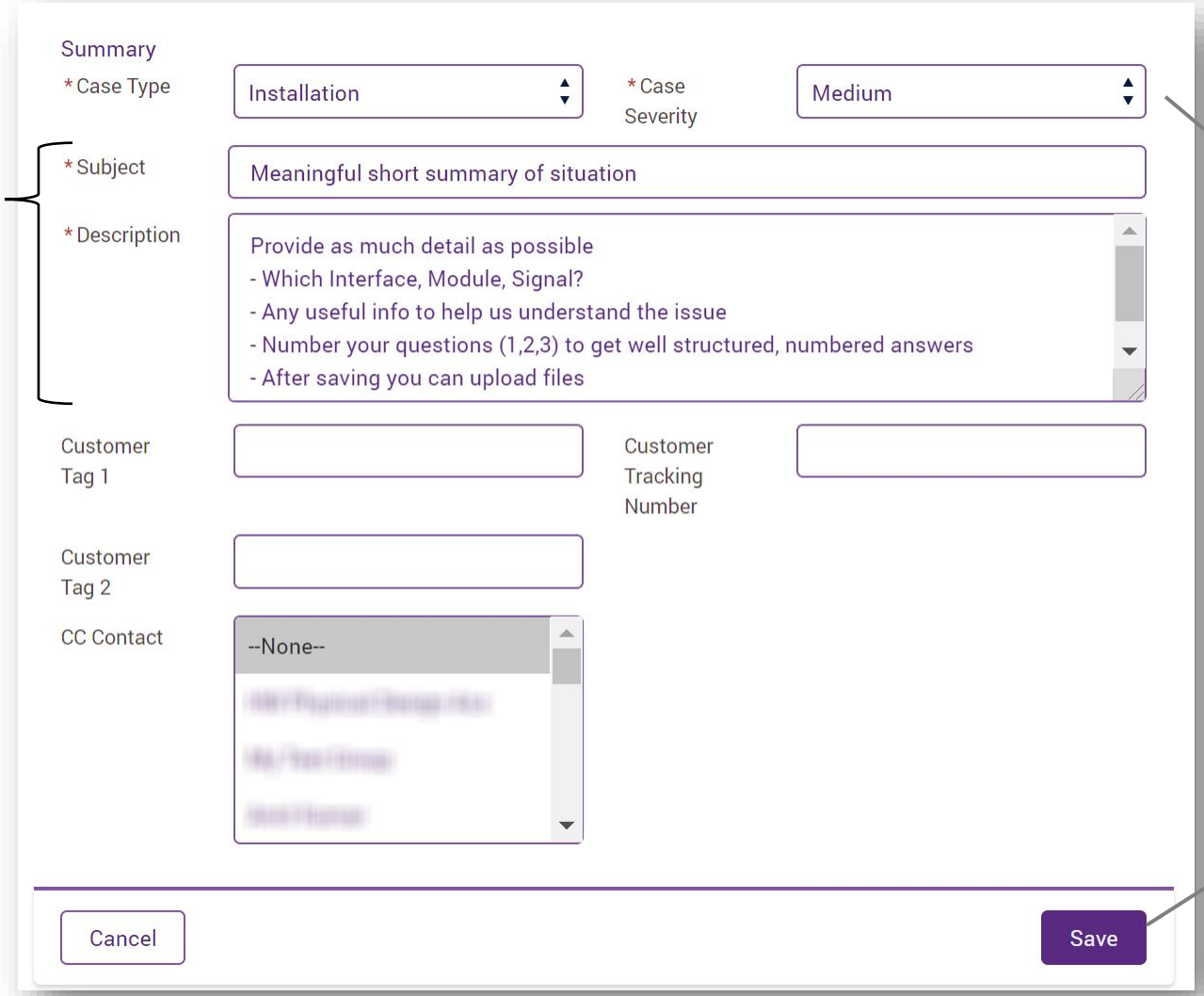
Recommends context based knowledge solutions

Recommendations may avoid the need for a case

SolvNetPlus Create a New Case (4)

Enter case details

Critical for effective issue communication

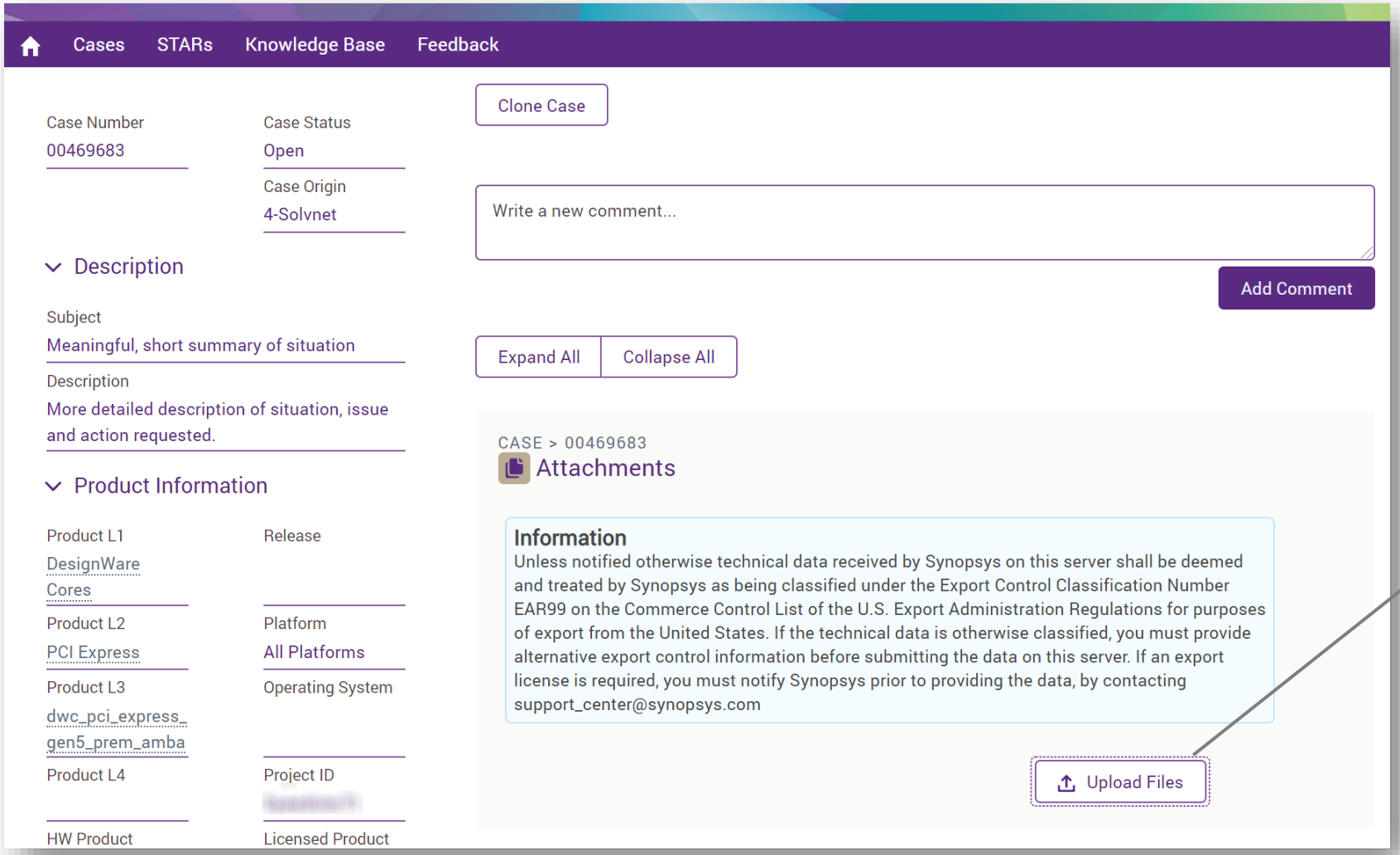


Severity of issue

Save!

SolvNetPlus Create a New Case (4)

Upload files or add more information



Upload any files

- Simulation waveforms
- Testcases
- Block diagrams
- etc.

SolvNetPlus Importance of Site ID, Project ID

- The Site ID is a unique number, that Synopsys uses to identify one specific customer site, a customer can have multiple site IDs.

- For each new project Synopsys and Customer define a unique Project ID
  - IP licenses are cut for one specific Site ID and one specific project ID

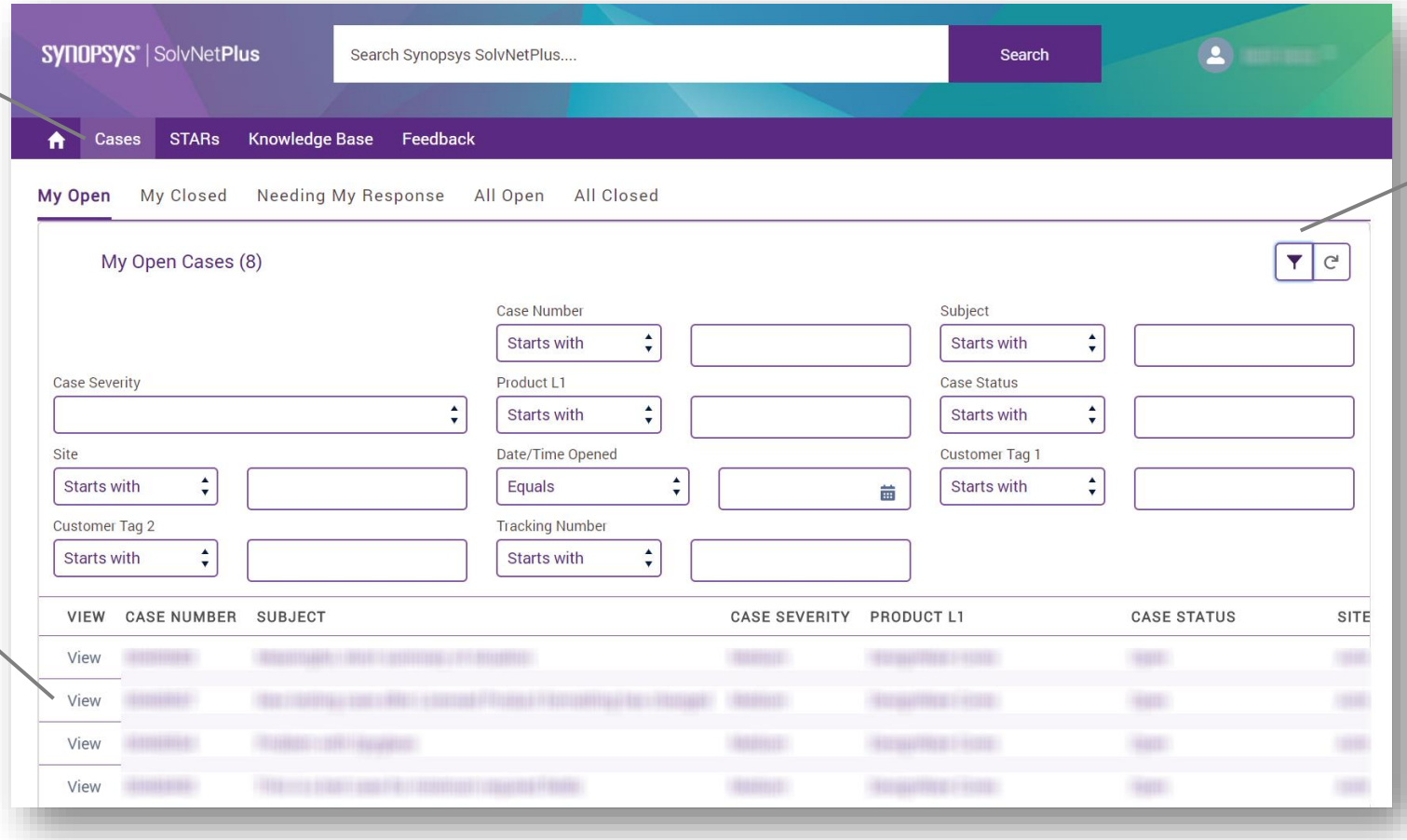
- When entering a new SolvNetPlus ticket, Users must enter their Site ID, a valid Project ID and select the related Licensed product

- The Project ID is also used during IP installation
  - during execution of .run file, when prompted, enter the project ID for source code installation (if no Project ID is entered, then the encrypted IP is installed)

- The Project ID was communicated to you by Synopsys Sales team
  - it does not appear “in clear text” in the license file you have received

SolvNetPlus View and Manage Cases

Navigate to cases



Filter case list

Click to manage case

Escalation Path

Customer Support Escalation Path

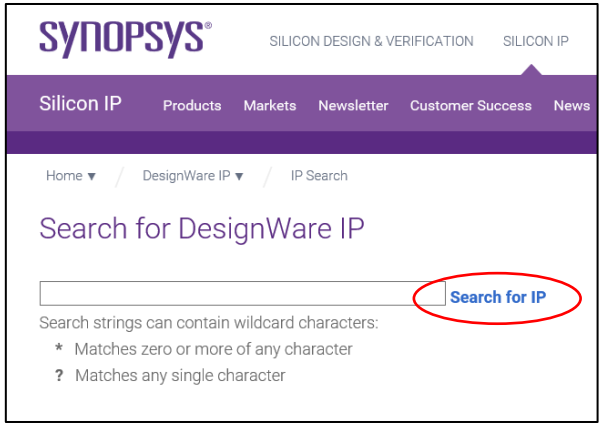
- SolvNetPlus is the primary support channel
- If your support needs aren't being met through SolvNetPlus,
  1. Let the AE assigned to the case know about your dissatisfaction
  2. Follow the escalation path below
  3. Please include the SolvNetPlus CASE number and reason for your escalation

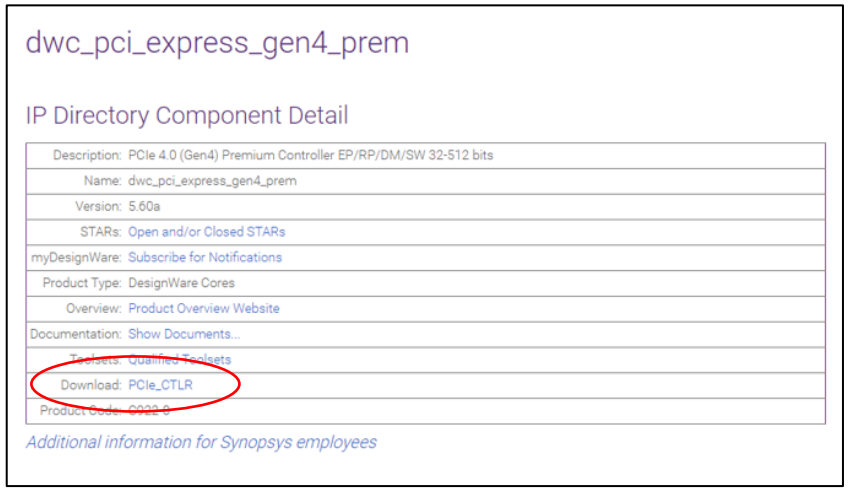
	Interface IP		***Foundation IP***	
			Embedded Memories, IO Libraries	Logic Libraries
Level 1	**Michael Yang, Flora Cheng (Shanghai)** Program Manager			
Level 2	**Rahul Sachdev** Sr Director, Program Management	**William Lau** Group Director, R&D Engineering	**Zeljko Tufekcic** Sr Manager, Applications Engineering	**Sumita Mathai** Sr Manager, Applications Engineering
Level 3	**Jumana Muwafi** SVP Engineering and Customer Support			

Other useful info

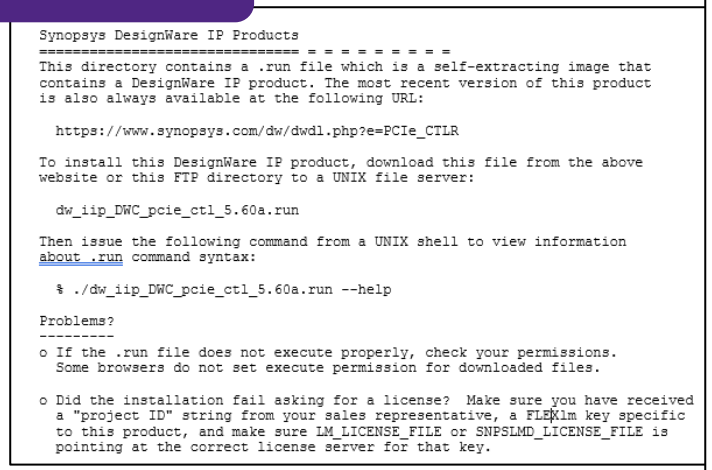
IP installation: Downloading an IP

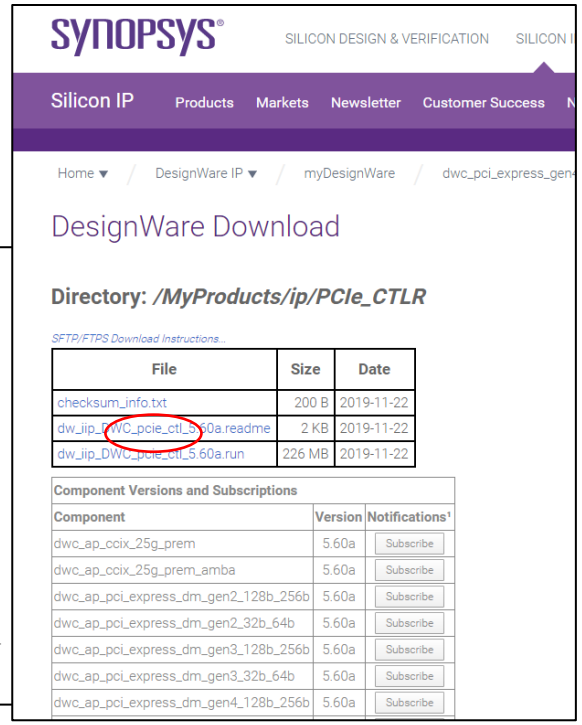
- Download IPs from Synopsys web site
  - You can access the IP directly – if you know the link or
  - if you need to “search for an IP” use this link: https://www.synopsys.com/dw/ipsearch.php
- To Download an IP you will need
  - a valid SolvnetPlus account (containing the site ID where the IP was licensed)
  - a valid license (not expired) for this IP must be installed on your license server
  - We recommend you read the Readme first
  - Download from Linux or UNIX platform





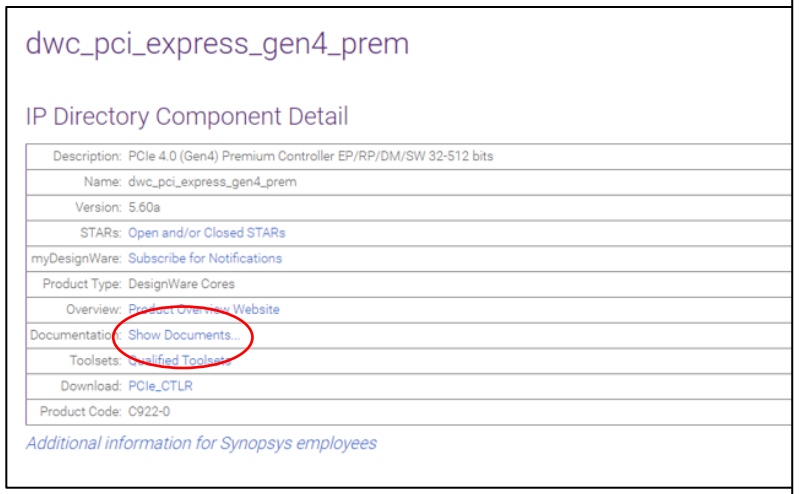
Readme

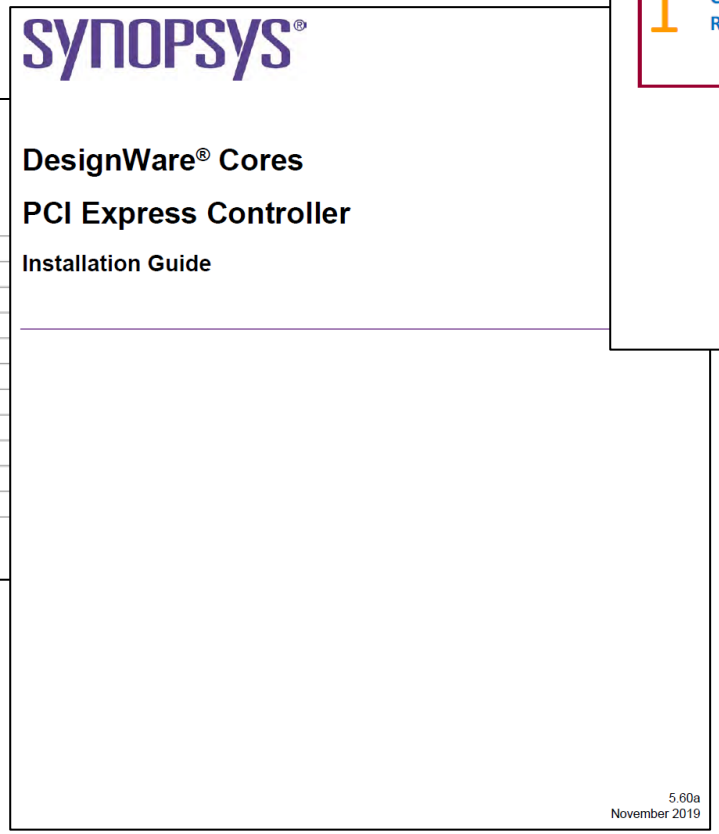


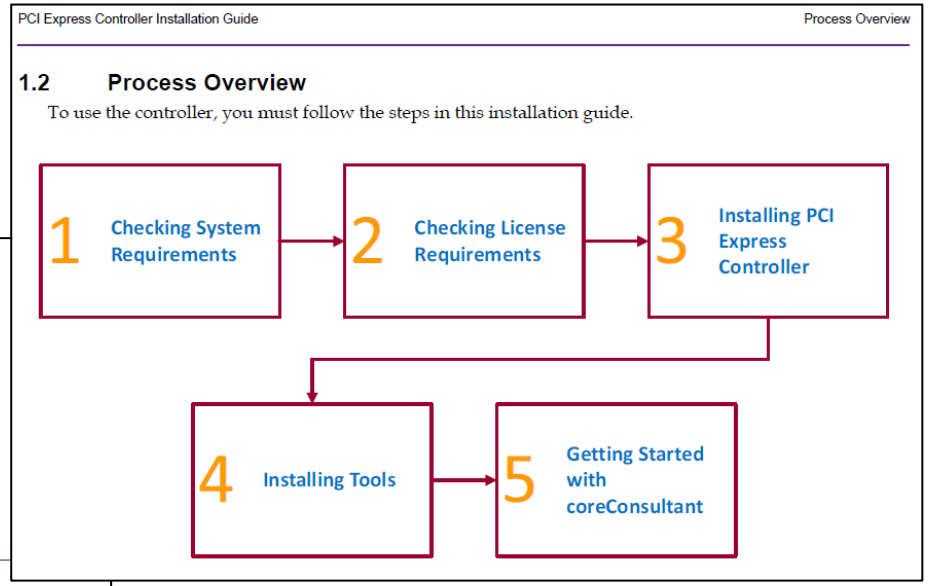


IP installation – Recommended Readings

- Before proceeding to IP installation
  - Read the download README (on each download page)
  - Read the IP install guide (available for each IP title)
  - Several steps are required to install an IP



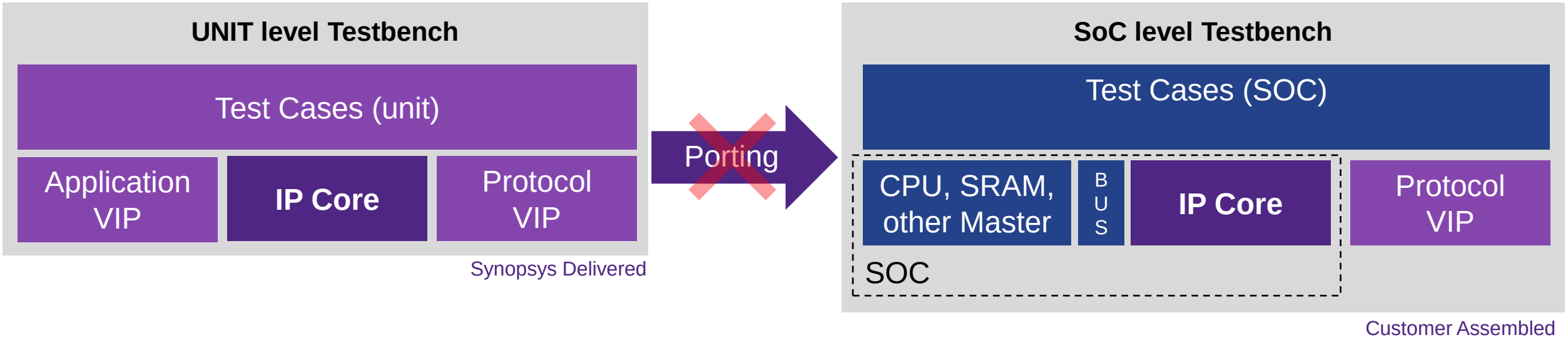




IP installation (install guide extract)

- When you have downloaded a .run file on your UNIX machine.
- Before executing the .run file
- You must set the SNPSLMD_LICENSE_FILE or LM_LICENSE_FILE environment variable to point at your license server that contains your license key.
- If you use both LM_LICENSE_FILE and SNPSLMD_LICENSE_FILE in your environment, ensure they are set to exactly the same value.
- To set environment variable type for example:
  - % setenv SNPSLMD_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
  - % setenv LM_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}
- Talk to your IT department to know the right settings for LM_LICENSE_FILE and SNPSLMD_LICENSE_FILE variables i.e the logic path to your license server(s)

VIP Support in DesignWare Cores



- Selected DesignWare Cores Digital Controller IP include a VIP based UNIT level Testbench
- Purpose is to confirm the IP deliverables meet the requirements by verifying the interface level testing of the specific IP configuration out-of-the-box in coreConsultant
- Synopsys VIP licenses shipped with DesignWare Cores Digital Controller IP do not include Synopsys VIP support
  - To obtain Synopsys VIP support to build your SoC level verification environment you must obtain a separate Synopsys VIP license

IP Evaluation licenses

- Evaluation licenses are for Digital IP only
- Synopsys does not generate evaluation keys for PHY IP

- Evaluation licenses are limited in time (typically few weeks)
- The following actions are limited to the first 7 days of the evaluation period:
  - The access to IP data page (documentation, STARs, IP download)
  - IP download (download of .run file)
  - IP installation (extraction of IP core kit, i.e execution of .run file)
  - Subscribe to IP notifications (you will continue to receive IP notification after the 7 days until you unsubscribe)
- The following actions are allowed until the end of the evaluation period:
  - Configure an IP and Generate RTL source code using CoreConsultant (GUI tool)
  - Simulate the IP in it's standalone testbench (using Synopsys VIP)

EA (Early Adopter) release delivery

What:

- Specific IP product delivery, not (yet) a standard product, draft documentation only
- EA release may be only verified for the customer configuration (see EA release notes for details)
- Subject to Synopsys Sales and Marketing approval

- Why:
  - To enable a customer with an early access to a new IP product or a set of features not yet available or not fully tested

- How:
  - EA Delivery process different from Standard IP downloads (customer will receive specific instructions – ShipPortal)
  - Specific paperwork and licenses key cutting required

- Logistic and Support:
  - Customer to provide: host id, site id, project id, customer contact
  - Tight support provided by Synopsys IP Product Engineering and/or IP support team
  - Technical kick-off meeting organized to train the customer to specific IP usage
  - If no dedicated PM assigned to this project, then the EA delivery is tracked by the Pre-sales AE

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Thank You