Micron Technology

System Level Memory Qualification Testing

CEL (Customer Engineering Labs)

Memory System Qualification

Question

- What are we trying to accomplish with a memory qualification test?

Answer

- Provide the most insightful, comprehensive, & complete system level memory qualification tests and results possible, in a timely manner. To essentially show that our customer's implementation of the whole memory system interface passes with margin when a tuned set of voltage & timing parameters are set by their controller.

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Contents

TSA (Timing & Signal Analysis) & System Level Memory Qualification

- What is “Traditional TSA”
- What is “Virtual TSA”
- What does the industry use for system level memory qualification
- What Micron sees as the future of memory qualification
- What Micron needs help with from our customers
- Summary

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Traditional TSA – What is it?

- TSA is detailed timing and signal analysis of the memory interface signals between a controller (processor) and the memory chip(s) or module(s) on customer systems. The CEL's "Traditional TSA" approach has been to choose a single channel and perform the analysis as measured with test equipment, at room temperature, nominal input, reference, & termination voltages, while running a default application on the system.
  - Requires custom sockets and interposer boards, to access signals for probing… for each memory device pinout variant.
  - Requires high bandwidth oscilloscopes, probes and logic analyzers.
  - Requires BGA re-balling & solder equipment for the memory chips under test.
- Traditional tests can take weeks to complete for one system. Detailed Pass/Fail reports are then generated including all the timing parameters, voltages levels, etc… as compared to the datasheet specifications.

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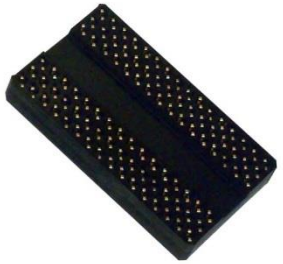
Traditional TSA – Test Equipment

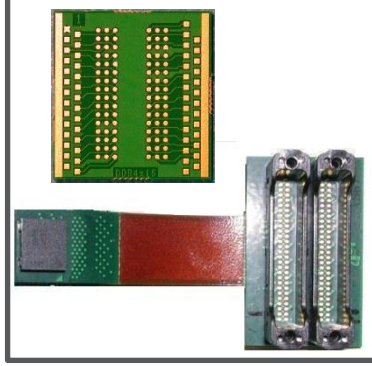
- High bandwidth Scope.

- High bandwidth probes with direct solder attach leads.

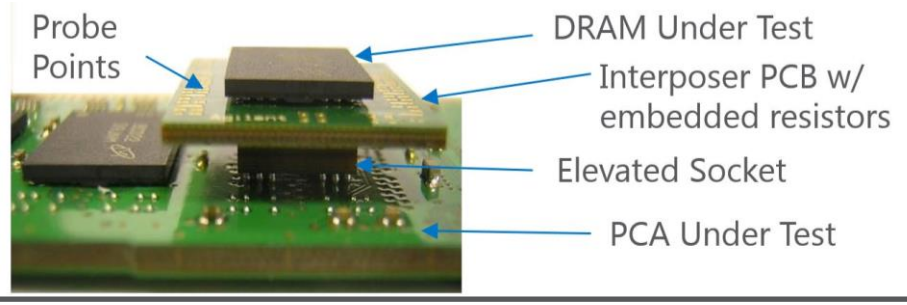
- High bandwidth Logic Analyzer



- Custom, elevated sockets to not interfere with surrounding components, or test additional DRAM.



- Custom interposer PCA's for Scope and Logic Analyzer probe attach.



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Traditional TSA – Sample Data

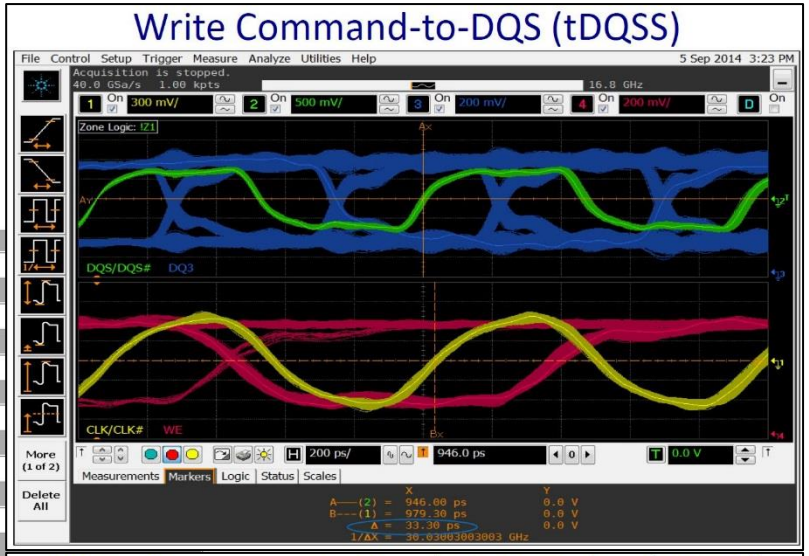
- Reports show measured results of each parameter tested and a comparison to the datasheet specs.
- Reports also include scope & LA waveforms used to capture the measurement.

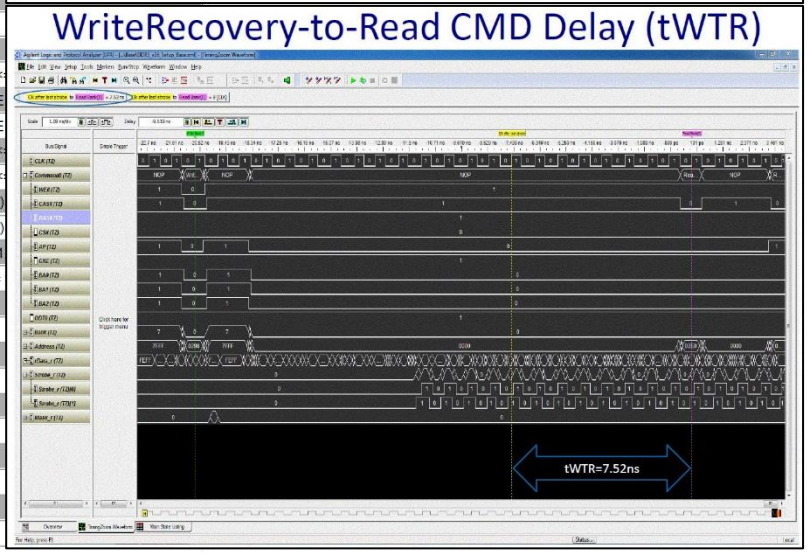
Summary of Results

Test Statistics	
Failed	2
Passed	31
Total	33

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	tjit(CC) Rising Edge Measurements	-30 ps	39.3 %	-140 ps <= VALUE <= 140 ps
✗	1	1	tCK(avg) Rising Edge Measurements	1.249 ns	0.4 %	1.250 ns <= VALUE <= 1.500 ns
✓	0	1	tjit(per) Rising Edge Measurements	24 ps	32.9 %	-70 ps <= VALUE <= 70 ps
✓	0	1	terr(2per) Rising Edge Measurements	39 ps	31.1 %	-103 ps <= VALUE <= 103 ps
✓	0	1	terr(3per) Rising Edge Measurements	50 ps	29.5 %	-122 ps <= VALUE <= 122 ps
✓	0	1	terr(4per) Rising Edge Measurements	55 ps	29.8 %	-136 ps <= VALUE <= 136 ps
✓	0	1	terr(5per) Rising Edge Measurements	58 ps	30.3 %	-147 ps <= VALUE <= 147 ps
✓	0	1	terr(6per) Rising Edge Measurements	55 ps	32.3 %	-155 ps <= VALUE <= 155 ps
✓	0	1	terr(7per) Rising Edge Measurements	53 ps	33.7 %	-163 ps <= VALUE <= 163 ps
✓	0	1	terr(8per) Rising Edge Measurements	54 ps	34.0 %	-169 ps <= VALUE <= 169 ps
✓	0	1	terr(9per) Rising Edge Measurements	56 ps	34.0 %	-175 ps <= VALUE <= 175 ps
✓	0	1	terr(10per) Rising Edge Measurements	57 ps	34.2 %	-180 ps <= VALUE <= 180 ps
✓	0	1	terr(11per) Rising Edge Measurements	59 ps	34.0 %	-184 ps <= VALUE <= 184 ps
✓	0	1	terr(12per) Rising Edge Measurements	63 ps	33.2 %	-188 ps <= VALUE <= 188 ps
✓	0	1	terr(nper) Rising Edge Measurements	-90 ps	50.0 %	-99.000000000000 E36s <= VALUE <=
✓	0	1	tCH Average High Measurements	501.029244903 mtCK(avg)	48.3 %	470.000000000 mtCK(avg) <= VALUE
✓	0	1	tCL Average Low Measurements	498.970755097 mtCK(avg)	48.3 %	470.000000000 mtCK(avg) <= VALUE
✓	0	1	tjit(duty-high) Jitter Average High Measurements	-12 ps	50.0 %	-99.000000000000 E36s <= VALUE <=
✓	0	1	tjit(duty-low) Jitter Average Low Measurements	-15 ps	50.0 %	-99.000000000000 E36s <= VALUE <=
✓	0	1	tCH(abs) Absolute clock HIGH pulse width	490.273677811 mtCK(avg)	14.0 %	VALUE >= 430.000000000 mtCK(avg)
✓	0	1	tCL(abs) Absolute clock LOW pulse width	487.871297030 mtCK(avg)	13.5 %	VALUE >= 430.000000000 mtCK(avg)
✓	0	1	tRPRE	1.078291000000 tCK	26.9 %	900.000000000 mtCK <= VALUE <= 1
✓	0	1	tRPST	468.1686000000 mtCK	23.8 %	300.000000000 mtCK <= VALUE <=
✓	0	1	tDQSCK	196 ps	6.4 %	-225 ps <= VALUE <= 225 ps
ⓘ	0	1	tDVAC(Clock)	549.3 ps		Information Only
✓	0	1	tLZDQS	73.5 ps	22.4 %	-450.0 ps <= VALUE <= 225.0 ps
✗	1	1	tQSH	368.2030000000 mtCK	7.9 %	VALUE >= 400.0000000000 mtCK
✓	0	1	tQSL	502.2864000000 mtCK	25.6 %	VALUE >= 400.0000000000 mtCK
ⓘ	0	1	tDVAC(Strobe)	489.7 ps		Information Only
✓	0	1	Overshoot amplitude (Clock, Data, Strobe, Mask)	184.140000000 mV	54.0 %	VALUE <= 400.000000000 mV
✓	0	1	Overshoot area (Clock, Data, Strobe, Mask)	14.395110000 mV-ns	88.9 %	VALUE <= 130.000000000 mV-ns
✓	0	1	Undershoot amplitude (Clock, Data, Strobe, Mask)	216.780000000 mV	45.8 %	VALUE <= 400.000000000 mV
✓	0	1	Undershoot area (Clock, Data, Strobe, Mask)	16.688500000 mV-ns	87.2 %	VALUE <= 130.000000000 mV-ns





Traditional TSA – Purpose?

- Some may argue the most important reason to perform a Traditional TSA is for signal verification of the memory interface per the datasheet specification.
  - This may be a valid statement if each channel is tested at the voltage & temperature extremes per the datasheet. This process can take months to complete.
  - As described earlier, the CEL team doesn't attach probes and analyze every channel on every memory socket… but only on a single channel on a single chip. So, while the extensive data in the report gives the customer a relative level of confidence that their system has met the design criteria, it realistically isn't a full verification of memory to controller interface and shouldn't be used as the qualification of the full memory system.
- The main reason to perform a Traditional TSA should be to debug a diagnostic failure. Using test equipment to capture a known issue, to help determine what the root cause is.

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Traditional TSA – Pro's/Con's?

Pro's

- Provides detailed parameter analysis with respect to the specifications.
- Can assist in debug of system failures, whether design or manufacturing.

Con's

- Results can't be used to qualify the full system level memory interface.
- It only provides a glimpse of a subset of the memory interface.
  - Narrow window of sampling time.
  - Single DQ (with associated DQS/Addr/Clk, etc…)
- Performing a Traditional TSA rarely if ever captures a memory system failure.
  - Example: may miss byte lane [DQ0:7] mis-alignments even though the DQ[n] we're looking at on a scope or LA is meeting all the timing specs with respect to DQS, etc…
- Despite global Customer Engineering Labs, time on equipment increases time to completion & continues to be a bottleneck for large scale customer support.

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Virtual TSA – What is it?

- Virtual TSA is a more comprehensive, system level, “automated” approach to memory qualification testing.
- Virtual TSA utilizes software like Intel’s MRC (Memory Reference Code) with embedded RMT (Rank Margining Tool), or AMD’s OverDrive™ utility, or other processor supplier’s similar software that performs memory interface “tuning”. The software adjusts timing parameters, voltage levels, ODT settings, etc… and tests the memory for pass/fail functionality in the system at each iteration.
  - This covers every channel of every memory device for a complete system test.
  - Parameters and respective pass/fail results are logged in an off system host via a UART connection (or similar) to the DUT. …allows multiple DUTs to be tested simultaneously.
  - The log files are plotted showing the parameter sweep in test, the respective spec value mask, and the pass/fail results of the tests. Plots will show out of spec conditions, as well as optimal settings for the best margin and stability across operating conditions.

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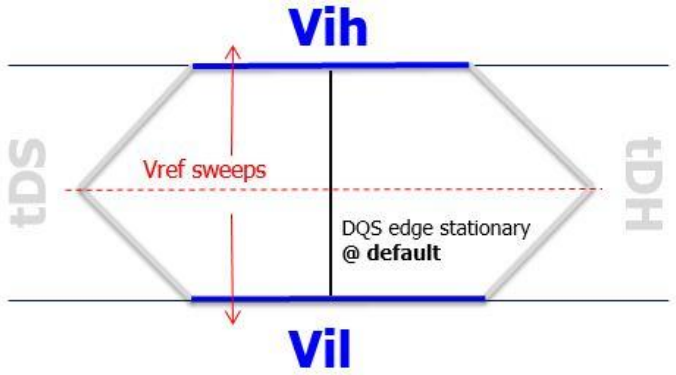
Virtual TSA – Sample Parameter Sweep…

- Using the memory controller interface to sweep each channel from –n to +m of the nominal set points of voltages, timing alignments, etc… provides a detailed matrix of the range of settings that result in a “pass” functionally.

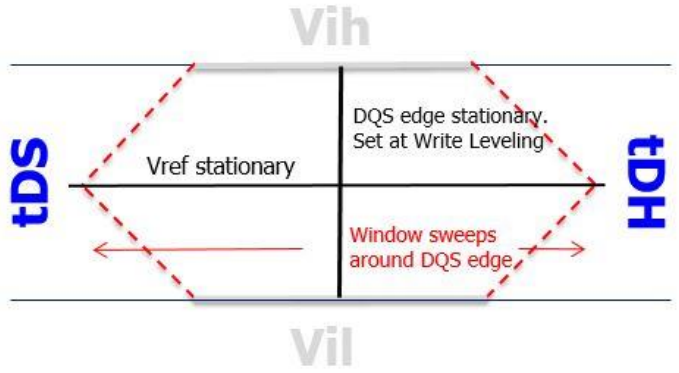
Vih/Vil → TxVHigh/TxVlow

- DQS placement set to ‘default’, obtained from training at nom conditions.
- System sweeps DRAM’s VREF input, to find upper/lower edges write window.



tDS/tDH → TxLeft/TxRight

- System place’s DRAM’s Vref at nominal (1/2Vdd).
- DQS edge placement will sweep relative to data window to find pass/fail



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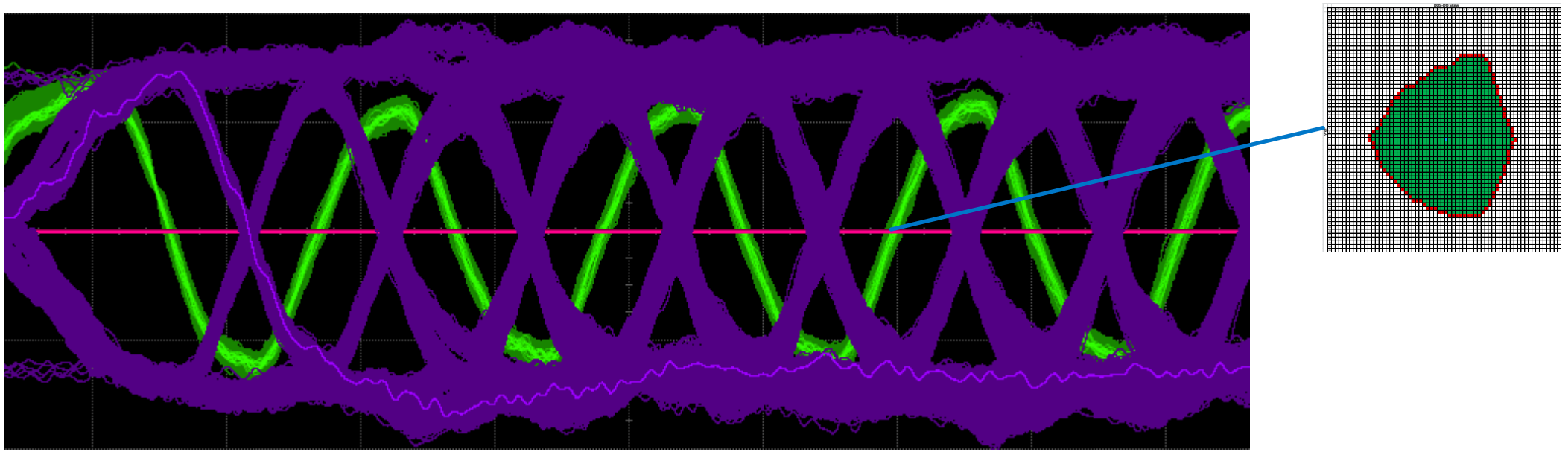
Virtual TSA – Already In Use

- Processors already utilize memory calibration/training code during boot to tune the memory interface to the optimal operating set points.
- Customized parameter sweeps, & logged results for comparison to the datasheet specs, provides the virtual full system level qualification data.



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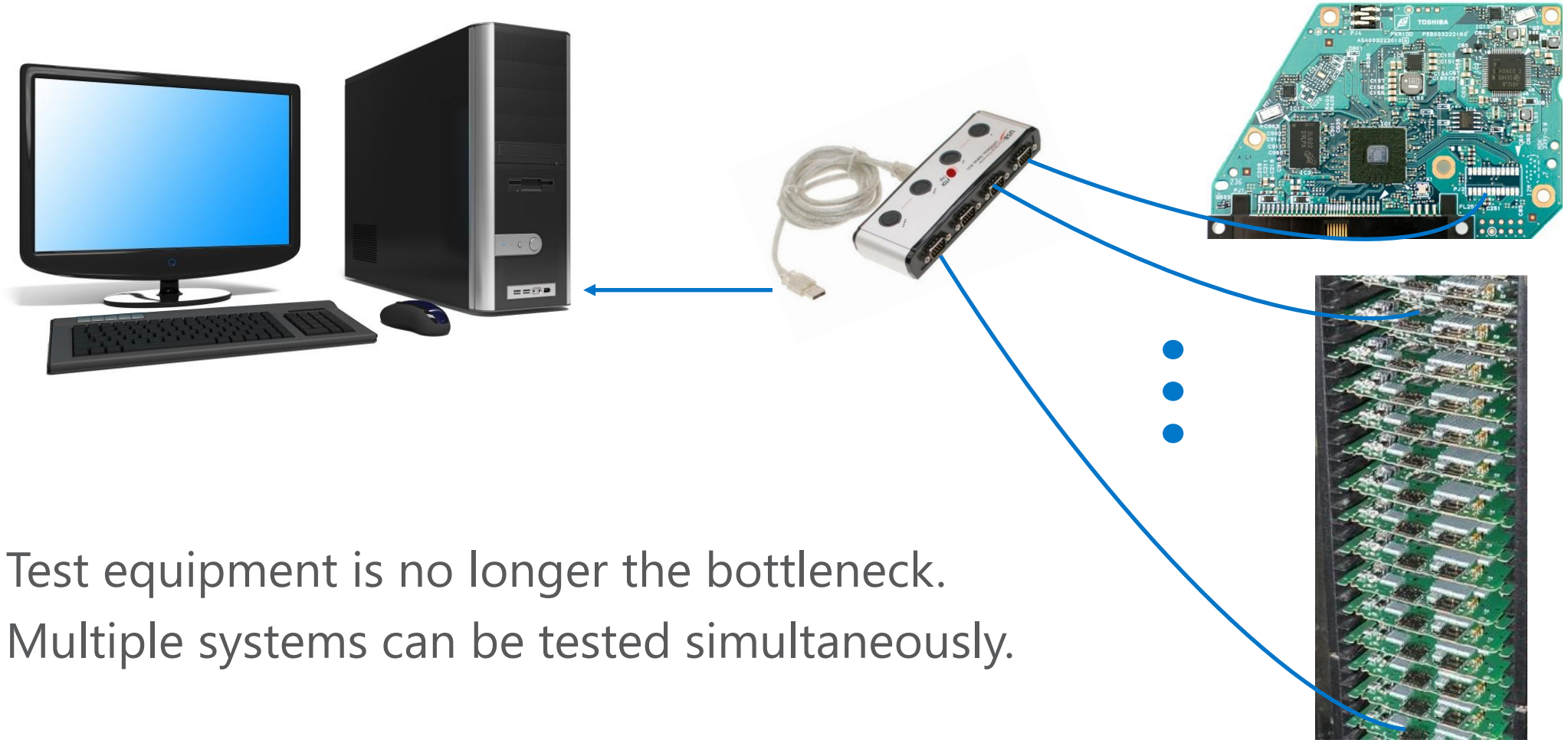
Virtual TSA – Sample Setup for Logging Results

Host PC

USB-UART convertor

DUT(s) w/ UART debug port



- Test equipment is no longer the bottleneck.
- Multiple systems can be tested simultaneously.

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Virtual TSA – Purpose?

- A more complete system level memory analysis is needed than what the "Traditional TSA" provides.
- A missing parameter to a system engineer is the full knowledge of the affect that parameter changes cause to the rest of the memory interface… how much actual functional margin is available after performance tuning settings are implemented? Virtual TSA provides this valuable information.
- Inclusion of guardband testing can be combined to provide an extensive matrix of memory system qualification results. This provides the optimal window of operation across system variances: voltage, temperature, etc…
  - Micron CEL's have custom voltage rail interface circuits for voltage margining tests.
  - Micron CEL's have multiple temperature chambers for use w/ customer memory quals.
  - *This is especially important for controllers that run training only once on first boot, and save the parameters for remaining boots to reduce startup time… they may not have the optimal environmental settings at the factory versus the real, end use environment.

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Virtual TSA – Pro's/Con's?

Pro's

- Virtual TSA eliminates the need to probe non-failing DUTs… no addt'l loading.
- Quickly determines memory system margins & performance limitations.
- Provides information for easier debug if memory failures do exist.
- Cost and time to complete a memory system test is greatly reduced.
- Many DUTs can be run simultaneously - eliminates queue for test equipment.
- Provides comprehensive performance analysis of the complete memory system.
- Data logs provide pass/fail results, & the optimal settings for each parameter.

Con's

- Virtual TSA is a system level test that doesn't replace basic board level HW verification, like measuring voltage rails at the memory chip.

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What Makes Sense?

- Memory interfaces have two basic design guides:
  - Physical implementation on a printed circuit board: power supplies, reference layers, trace routing, component placement, etc…
  - Functional implementation of the software interaction to/from the processor: bus speeds, timing alignment, Vref settings, ODT settings, etc…
- If these design guides that Intel, AMD, Qualcomm, Micron, etc… provide for memory interface are understood and implemented properly, then it doesn't make sense to request a "Traditional TSA" for qualification purposes.
  - Does it provide comfort that the guide is correct? …or that the layout engineer got it right? …or is there a belief that if data from a single channel is good enough, then the whole system passes the qualification?
- What if the design guides aren't followed? …then it definitely doesn't make sense to request a "Traditional TSA" as we wouldn't know which is the worst case channel to probe.
- Both scenarios benefit the most by performing Virtual TSA… that makes sense.

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What Are The Industry Test Requirements?

- JEDEC – Some test equipment supplier's documents indicate there is a JEDEC standard, requiring verification measurements be made at the balls of the memory… which is quite frankly impossible, and they admit it too.
  - Blind and buried vias (HDI) don't allow probe access to the opposite side of memory chip… which even if it did have a though via, it isn't technically at the ball. In reality this would require access to the balls of the processor as well for certain measurements.
  - Sockets/risers used to elevate the interconnect to fit interposer boards, or test multiple chips also don't allow direct access to the balls of the BGA.
  - Interposers, whether for scope or logic analyzers add vias, additional trace lengths, and in some cases imbedded resistors for the probes not to cause additional loading to the net… in any case these probe locations are not technically at the ball of the BGA.
- We're under the opinion that the spec is defined at the package pins, and thus it assumed the measurements should be made as close as possible if connecting test equipment. There isn't a standard that negates virtual system testing.

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How Does the Industry Verify Memory Systems?

- Some companies design their systems with probe points at accessible through vias near the balls of the BGA for as close as possible test capability… then spend months probing each DQ, DQS, C/A, etc… on every memory device, to verify their interface has met the datasheet requirements… Then proceed to system tests, exercising the memory interface.
- Some companies without generous testing schedules, can't probe every net. They may or may not follow the design guides, may or may not simulate the layout… being hopeful that the hardware is ok & go directly into system testing, relying on one of many memory suppliers to function properly with their implementation.
- Some companies will require the memory suppliers to gain certification of functionality with their system from an outside test facility… relying on that certification as a full system level memory qualification without ever probing a single signal. (Those outside test facilities use SW like Intel's RMT)

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What's the Correct Method for Memory Qualification?

- We need to reiterate the difference between board level verification vs system level qualification.
  - Simulation tools like Hyperlynx can provide excellent data on board layout analysis, but you wouldn't count that as your HW verification… you need actual hardware to test. Similarly you wouldn't take a few measurements with a scope or logic analyzer and count that as your full system level qual. You would layout, simulate, build, perform basic board bring up verification, then proceed into system tests.
  - By performing the Traditional TSA, we're backing up from system level qual testing into a very complex hardware/board level verification state, which should really be reserved for debugging known failures.
- An automated system test can provide a greater level of confidence than probing every signal. Probing a few memory signals cannot guarantee a full system level qualification, nor can probing every signal.

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Future of Memory System Qualification?

- The future is already here in the test arena.
  - Proposed probing techniques using sockets and custom interposer boards on these high speed, low voltage memory interfaces (LPDDR4) is not only complicated, costly, time consuming, but can also cause loading affects that result in measurement errors and can even cause systems to not boot.
  - Probing a circuit may be necessary for debugging a failure with the memory interface, but we need to focus on system level qualification test methods that don't require making physical contact with the signal.
- Advanced memory controllers have the capability of making tuning adjustments during boot and performing parameter changes on the fly during normal operation. We need that same capability to run the "RMT" style test on every system… that essentially is a Virtual TSA.
- Customers already have and continue to use automated tools like "RMT", to evaluate memory performance from multiple suppliers in their systems.

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Micron Needs You to Help Us Help You

- You now know what is capable when we can tap into the processor's memory interface controls to make adjustments for testing, like they do for normal operation, and see the actual results of your system.
- Not all processor suppliers provide access to the memory interface controls for this type of testing. We need our customers to engage with their processor supplier of choice to gain access to these controls and provide us a serial UART port (or similar) from the controller to log tests & results.
- Being able to perform virtual tests on the full memory system allows us to provide our customers with the complete qualification data they need… and in an efficient manner resulting in faster turn-around times for the numerous requests we receive.

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Sample Memory Controls Needed for V-TSA

Parameters For LPDDR4
DRAM Vref_CA
DRAM Vref_DQ
DRAM DQ Voh
DRAM Drive Strength
DRAM CA ODT
DRAM DQ ODT
Controller CA Voh
Controller DQ Voh
Controller CA Drive Strength
Controller CK Drive Strength
Controller DQ Drive Strength
Controller DQS Drive Strength
Controller DQ ODT
Controller's trained value for the centered tDQS2DQ per byte lane for writes… along with the right & left boundaries.
Controller's trained value for the edge aligned tDQS2DQ per byte lane for reads… along with the right & left boundaries.

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Summary

- Connecting traditional test equipment to a memory interface should be to debug an issue, not qualify a part.
- Partial hardware design verification (Traditional TSA) is a costly and time consuming engineering task, and doesn't provide the system level performance/qualification results we and our customers are looking for.
- Virtual TSA utilizes the full memory interface of your system to measure its own margin.
  - Creates a more accurate measurement of your system's performance than what any externally attached test equipment could provide.
- Virtual TSA is an exciting, "non-contact" approach for system level memory quals.
- In certain cases, Virtual TSA can be performed in our customers' own labs, enabling a heightened sense of confidentiality and security for new products in development.

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