SYNOPSYS®

DesignWare Cores LPDDR5/4/4X PHY Interconnect Signal and Power Integrity Guidelines Application Note

DWC LPDDR5/4/4X PHY

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June 1, 2021

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Contents

Revision History

Doc. Revision	Date	Description

0.6	June 1, 2021	Updated:
		• Section 4.1.5 Package Considerations for LPDDR4/4X
		  ○ Removed outdated reference
		• 5 Power Integrity Analysis
		  ○ Removed outdated reference

0.5	August 20, 2020	Corrected: • Table 3-1, memory density for LPDDR5 • Table 3-1, CA bus rate for LPDDR5 changed to DDR. • Removed conflicting guidance from LP4/4X routing guidelines in section 4.1.4. • Removed reference to BP_ZN_SENSE from section 6.1.
0.3	April 17, 2020	Updated: • Removed 34& output impedance reference in table 3-1 • Clarified LPDDR4X logic levels in table 3-1. • Added note regarding controlling intra-pair skew of differential pairs. • Added note regarding availability of timing budget spreadsheets in section 7. • Minor editorial
0.2	November 26, 2019	Updated: • Table 4-1 "Summary of outing skew requirements for LPDDR4” - to align skew guidance with PUB documentation. • Table 4-2 "Summary of Outing Skew Requirements for LPDDR5” - to align skew guidance with PUB documentation. Minor Formatting Edits
0.1	March, 2019	Minor Formatting Edits
0.0	February, 2019	Initial Release

1 Introduction

This document provides general guidance for all the signaling protocols supported by the LPDDR5/4/4X PHY IP. This application note applies to all the process nodes for which the subject IP is available.

In this document the user will find:

- An outline of the signal and power integrity support Synopsys can provide for this IP.
- A discussion of the JEDEC protocols covered by this IP.
- Routing and implementation guidelines specific to the supported protocols.
- Example Timing budgets for all the protocols supported by this IP.
    - *These are example budgets for each protocol. The values in the budget are very close to what can be expected for any particular process node.*

2 Review Services and Signal Integrity Support

Synopsys encourages all our customers to take advantage of the visual review services we offer as part of any DDR PHY license. These services include, but are not limited to, the following:

- IO ring review
- Floorplan review
- SoC layout (GDSII) review
- Package design review
- PCB design review
- Signaling environment review
- Review of simulation results

These reviews, conducted early in the design process, are extremely effective in catching potential problems while they can be easily remedied. To begin any such review, please file a SolvNet case requesting the review or contact your Synopsys representative.

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3 Features and Benefits of Protocols Supported by the LPDDR5/4/4X PHY

This section will discuss the JEDEC protocols that are supported by the LPDDR5/4/4X PHY. A summary of supported protocols can be found in the table below. Additionally, more in depth discussion of the features that each protocol supports are found in subsequent sections.

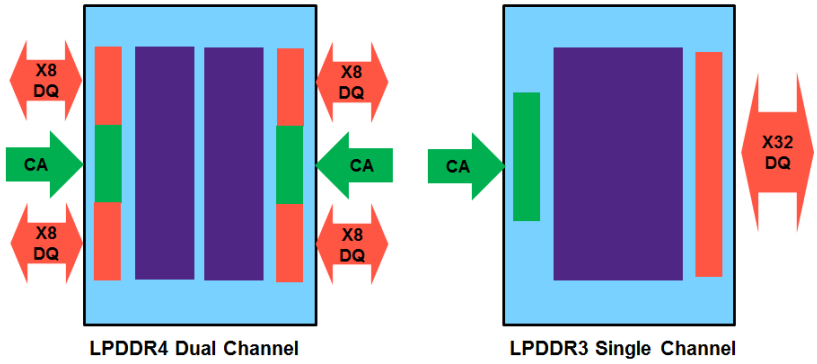
Table 3-1 Summary of supported protocols

Protocol	LPDDR4	LPDDR4X	LPDDR5
Applications	Mobile Electronics (PCB, PoP)	Mobile Electronics (PCB, PoP)	Mobile Electronics (PCB, PoP)
Maximum Data Rate [Mbps]	4266	4266	6400 (4X Mode)
Minimum Data Rate [Mbps]	533	533	533 (2X Mode)
Maximum Clock [MHz]	2133	2133	800
Minimum Clock [Mhz]	267	267	133
Memory Density/Size	4Gb - 32Gb	4Gb - 32Gb	8Gb - 64Gb
Prefetch	16N	16N	16N
Width Options	x16, x32	x16, x32	x16, x32
Logic Levels	1.1	0.6V, 1.1V-CKE/Reset	0.5V, Down to 0.3V with DVFSQ
IO Logic Type	Terminated LVSTL	Terminated LVSTL	Terminated LVSTL
Strobing	Differential Bidirectional	Differential Bidirectional	Differential - Separate WCK and RDQS
Delay Locked Loop in SDRAM	No	No	No
Clocking	Differential Clock	Differential Clock	Differential Clock
Drive Strength Options	PVT Compensated Output Driver	PVT Compensated Output Driver	PVT Compensated Output Driver
Termination Type/Options	PVT Compensated pull down termination on DQ/DQS/CA/CK	PVT Compensated pull down termination on DQ/DQS/CA/CK	PVT Compensated pull down termination on DQ/DQS/CA/CK
DQ Termination Voltage	VSS	VSS	VSS
CA Termination Voltage	VSS	VSS	VSS
Read/Write Data Leveling	yes	yes	yes
Data Bus Rate	DDR	DDR	DDR
CA Bus Rate	SDR	SDR	DDR
DQ VREF	Internally Generated	Internally Generated	Internally Generated
CA VREF	Internally Generated	Internally Generated	Internally Generated
Calibration Aids	MANY	MANY	MANY
OCD (Off-Chip Calibration) - ZQ	yes	yes	yes
ODT (On-Die Termination)	yes	yes	yes
DQ Data Bus Invertion?	yes	yes	yes
DQ CRC Check	no	no	no
CA Parity Check	no	no	yes
Boundary Scan	yes	yes	yes
Bank Groups	no	no	yes

3.1 LPDDR4/4X Features and Benefits

The most significant difference between LPDDR4 and LPDDR4X is the reduction of the data (DQ) IO voltage to 0.6 V for additional power savings. Beyond this, there is no difference. LPDDR4 is a mobile memory device specification governed by the JEDEC standard JESD-4, *"Low Power Double Data Rate 4 (LPDDR4)"*. The LPDDR4X interface is governed by this standard as well as *"Addendum No. 1 to JESD209-4 - Low Power Double Data Rate 4X (LPDDR4X)"*. These standards cover interfaces operating up to 4266 Mbps. These standards strive to reduce power and improve signal integrity by implementing a lower voltage IO power rail, employing ODT on the Command/Address bus and reducing the overall width of the Command/Address bus among other features. LPDDR4/4X has been organized into 2 channels compared to LPDDR3's single channel allowing for wide flexibility in interface configuration (Figure 1). What is presented here is an introduction to the major concepts that define LPDDR4/4X.

Figure 3-1 Dual Channel Organization



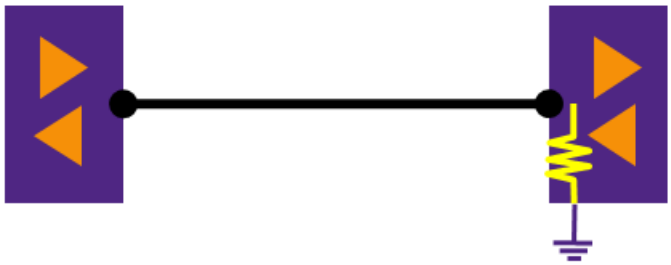
3.1.1 1.1 V LVSTL Signaling

The signaling level for LPDDR4 is 1.1 V -40 mV/+ 70 mV DC for the I/O voltage. Termination for the data lanes and the Command/Address lane is a pull-down resistor to VSS. Final swing of the received signal will be determined by the termination value at the target device and the pull-up termination value of the driver. The advantage of this is that only a "1" toggle will burn termination power, "0s" can be signaled without burning any termination power. A very low signal swing can be implemented to control simultaneous switching noise as well as reduce the amplitude of the crosstalk. VREF is determined through a training algorithm.

3.1.2 0.6 V Signaling for LPDDR4X

LPDDR4X uses a nominal voltage supply of 0.6 V with a tolerance of -30 mV and +50 mV DC. to power the data lanes during Write and Read operations. The CA bus continues to operate at 1.1 V for LPDDR4X.

Figure 3-2 Data lanes and Command/Address Signals Implement a Pull-down Termination to VSS



3.1.3 Command/Address Features

3.1.3.1 Narrow Bus

To reduce power, the width of the CA bus has been reduced to 6 bits. Though there are two of these 6 bit busses on the dual channel interface, many of the operational configurations only require a single set of CA signals to be driven from the SOC.

3.1.3.2 On Die Termination

LPDDR4 is the first JEDEC memory standard to offer ODT on the unidirectional CA bus. This will improve signal integrity and allow support for longer routed lengths such as would be encountered in side by side implementations. Since ODT for the CA is also to VSS, the VREF levels are nominally the same between the data lanes and the CA bus.

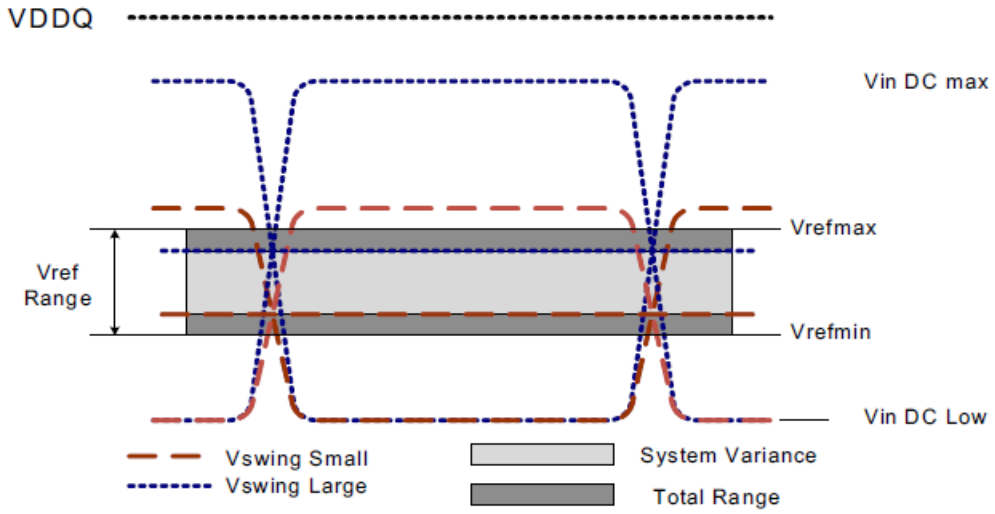
3.1.3.3 Single Data Rate Signaling

Unlike LPDDR3, LPDDR4 implements single data rate signaling for the Command/Address bus. This will allow for better signal integrity and/or heavier loading on the CA busses, depending on the configuration. To support this, LPDDR4 has implemented 4 phase addressing, with some commands taking 4 cycles to execute.

3.1.4 VREF Training for DQ and CA

Because the VREF level for DQ and CA can vary by ODT level as described in Figure 3, VREF must be able to be trained to the correct level. The LPDDR4 SDRAMs have internally generated VREF for both DQ and CA signals. Additionally, loading conditions will impact the available signal swing through inter-symbol interference effects. The VREF training algorithm will allow the placement to be done within 0.5% of VDDQ accuracy. Training will settle to the average calculated Vref level across the byte lane. Since signal channel configurations can vary from lane to lane, training for different VREF levels between byte lanes is supported (Figure 3).

Figure 3-3 Vref Training Optimizes the Centering of VREF in the Vertical Scale for Both DQ and DMI



3.1.5 DMI Pin – Data Mask/Data Bus Inversion

Data Bus Inversion allows the LPDDR4/4X data interface to conserve termination by inverting busses that signal a greater number of “1”s then “0”s. Since LPDDR4/4X is terminated to VSS, signaling a 0 draws no termination current, as opposed to signaling a 1. Data Bus Inversion will take an example pattern of 1011 0011 and invert this to a more power friendly 0100 1100 pattern. This has the added benefit of reducing simultaneous switching noise and, to a certain extent, crosstalk. While the DDR4 standard offered DBI, it was implemented in an either-or manner with the data mask command. The DMI solution allows both DBI and DM to be enabled simultaneously when the DMI pin is enabled in concert with the proper mode register commands.

3.1.6 Eye Characterization Techniques for LPDDR4/4X

As DDR bit rates have been increasing, the impact of random jitter has become a more significant component in timing closure. The LPDDR4/4X standard is written to accommodate Bit Error Rate techniques by defining the DQ receive parameters in terms of a data window instead of setting up and hold specifications. Figure 4 illustrates this new window. For DQ, the window, 0.25 UI in width and 120 mV in height for 4266 Mbps operation represents the needed window to support a BER of 1E-16. The CA timing also uses a rectangular window, but since this is single data rate, there is no provision for random jitter in the form of a target bit error rate. The assumption is that at the lower signaling rate, the BER contribution is small.

Figure 3-4 DQ and CA Receiver Data Input Valid Windows

DQ Mask

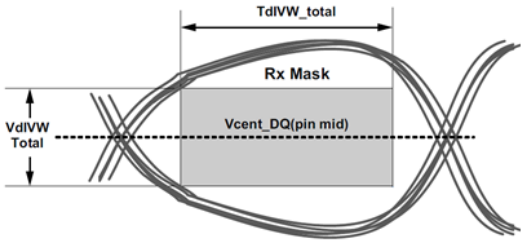


Figure 114 — DQ Receiver(Rx) mask

Table 94 — DRAM DQs In Receive Mode

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9
tDQSDQ	DQ to DQ offset	-	30	-	30	-	30	-	30	ps	10
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	-	0.6	ps/°C	11
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	-	33	ps/50mV	12
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	V/ns	13

* UI = tCK(avg)min/2

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TdIVW(ps) = 450ps at or below 1333 operating frequencies.

CA Mask

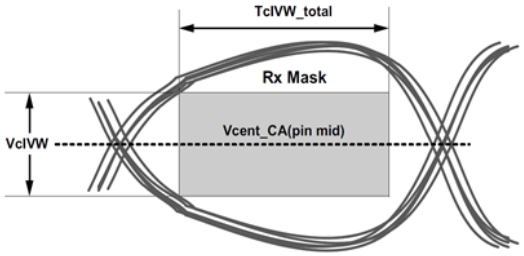


Figure 107 — CA Receiver(Rx) mask

Table 91 — DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	V/ns	7

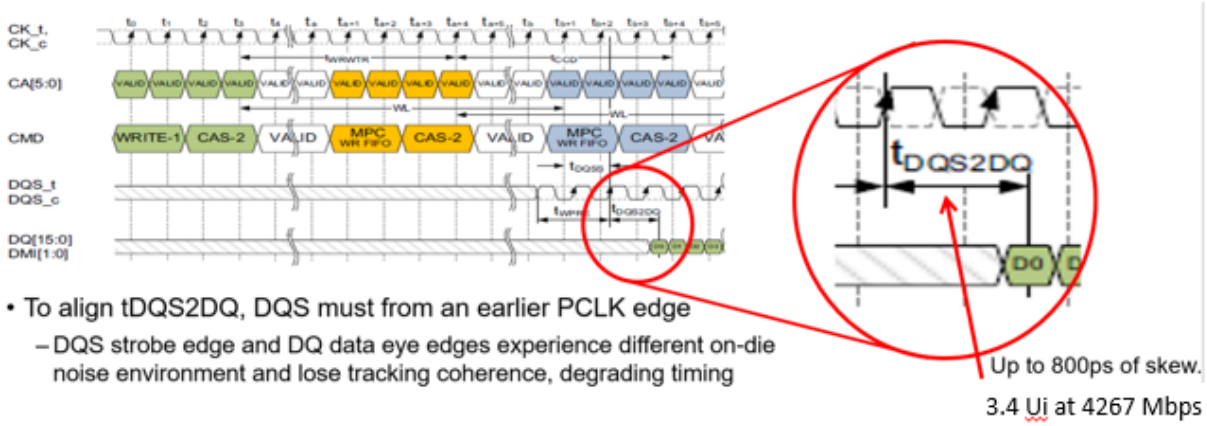
* UI = tck(avg)min

A The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

3.1.7 tDQS2DQ-Write

LPDDR4 implements an un-matched DQS to DQ path. This reduces the latching power consumed by the SDRAM. This introduces a skew between DQS and DQ of as much as 800 ps. 800 ps equates to ~3.4 UI at 4267 Mbps. To this amount of skew reduces the amount of beneficial jitter tracking between DQS and DQ. The impact of this is to increase the amount of relative jitter between DQS and DQ during Write operations. To close timing, the power rail noise specifications must be reduced for LPDDR4 to +/-2% on the VDD and +/-5% on the VDDQ and VDDQLP domains. Implementing data bus inversion will make these levels easier to achieve.

Figure 3-5 Illustration of tDQS2DQ Specification



3.1.7.1 DQS to DQ – Read

Similarly, the architecture of the LPDDR5/4/4X employs an unmatched DQS to DQ path to reduce the power and area of the IP.

3.1.8 Multichannel Architecture

Dual channels in the LPDDR4/4X device give the user many choices for connectivity compared to a single channel device. Each of these configurations have pros and cons in terms of pin usage, bandwidth and ease of implementation. Please refer to Figure 6 though Figure 8 below for connectivity options offered with a dual channel device.

Figure 3-6 Parallel Configuration

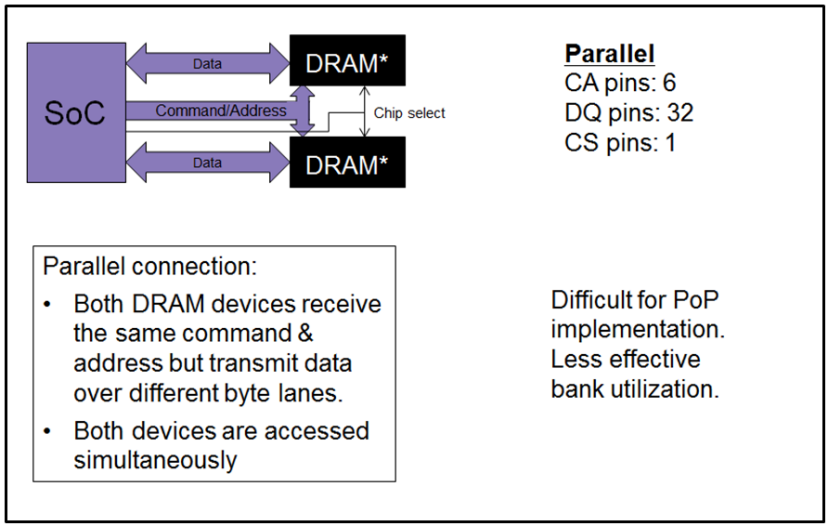


Figure 3-7 Series Configuration

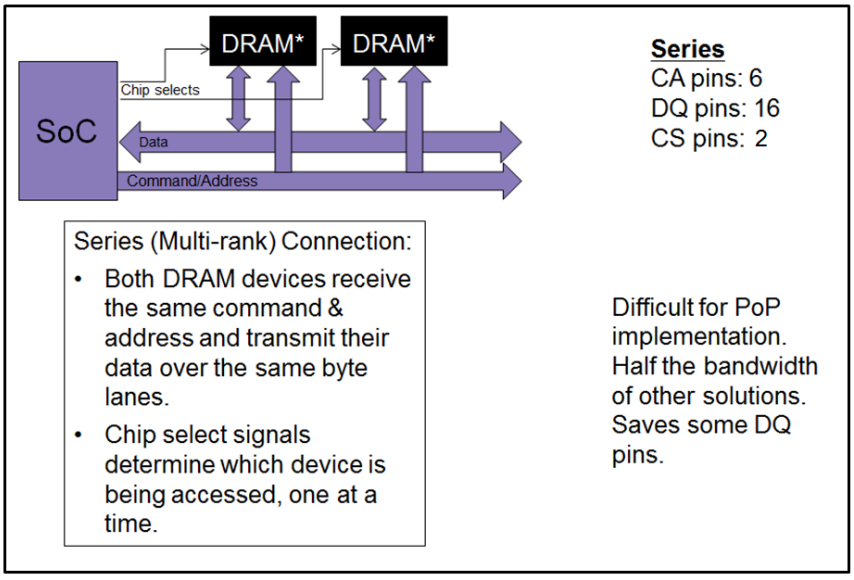
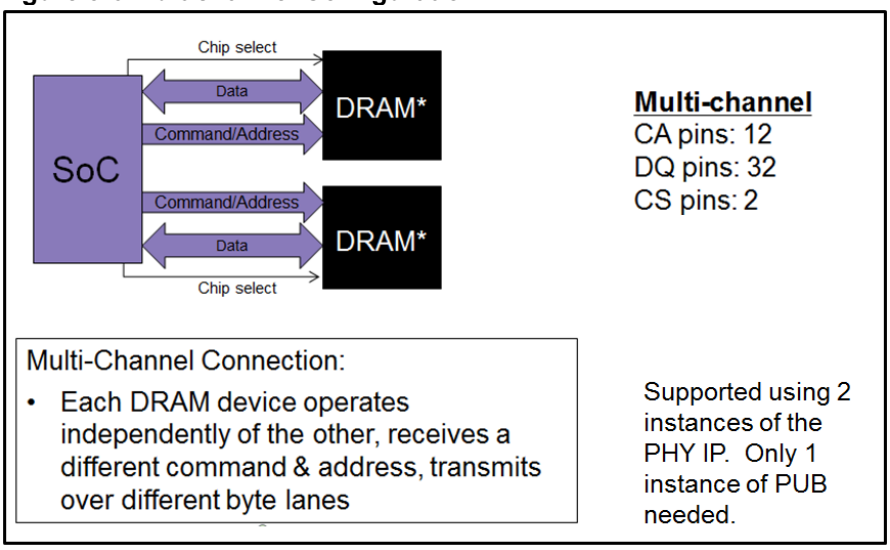


Figure 3-8 Multichannel Configuration



3.2 LPDDR5 Features and Benefits

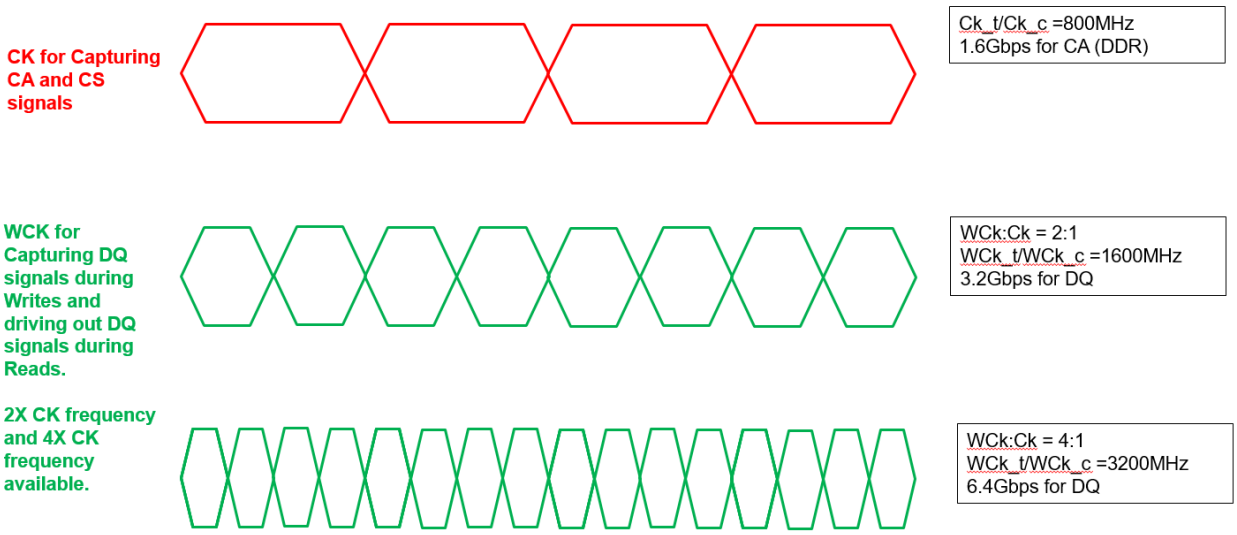
3.2.1 WCK and RDQS

The bidirectional DQS found in LPDDR4 has been replaced with the differential WCk_t/WCk_c for strobing Write data and the RDQS_t/RDQS_c for strobing in Read data. The Ck_t /CK_c pair captures the double data rate CA signals of rising and falling edges of the differential pair, and CS signals on the rising edge only.

The WCK pair operates at either twice the CK frequency or four times the CK frequency. The multiplier is set with a mode register command. A WCK:CK ratio of 4:1 allows an 800 MHz CK pair to generate a 3.2 GHz WCK pair resulting in a DDR bit rate of 6.4 Gbps (Figure 9). Note that the LPDDR5/4/4X IP only supports the 4:1 ratio at bit rates greater than 3.2 Gbps.

CA bus uses double data rate timing. Rising and Falling edges of the CK/CK# 800 MHz signal result in a CA bit rate of 1.6 Gbps.

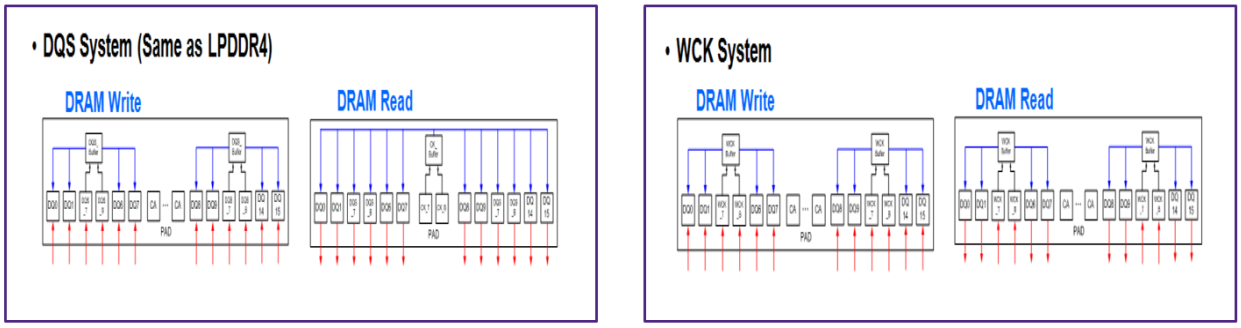
Figure 3-9 Relationship of CK to WCK



3.2.1.1 WCK Drives out DQ and RDQS

LPDDR4 uses the CK/CK# to drive out data during Reads. Aside from the limitations of the CK/CK#'s being ¼ of the frequency of the data for LPDDR5, this can introduce considerable jitter due to the long clock tree needed to distribute the signal to all byte. LPDDR5 uses the WCK pair to drive out the data in each byte. This reduces jitter with shorter distribution and saves power during the transaction.

Figure 3-10: WCK vs. CK for Driving Out Data



During Read operation, CK/CK# is received and then distributed via long clock tree to all bytes DQ/DQS buffers to drive out data.

During Read operation, WCK/WCK# is received and then distributed DQ/DQS buffers within a single byte to drive out data.

3.2.1.2 RDQS to DQ – Read

Similarly, the architecture of the LPDDR5/4/4X employs an unmatched RDQS to DQ path to reduce the power and area of the IP for LPDDR5 operation.

3.2.2 Single Ended Strobing

At lower bit rates, 1600 Mbps is anticipated to be the break point, single ended strobing for CK, WCK and RDQS are available. During this operation, the single-ended signal will be captured relative to the appropriate VREF level. This mode can be applied to CK, WCK, and RDQS independently. For certain low bit rates, strobeless Reads can be implemented for an additional power savings.

3.2.3 Lower Signaling Voltage Swing with DVFSQ

Dynamic Voltage and Frequency Scaling for VDDQ will lower the operating voltage on the IO domain from 0.5 V nominal to 0.3 V. To achieve this, signaling must be done without ODT implemented in order to achieve the necessary signal swing. Consequently, this implementation should be limited to lower frequencies and shorter lengths to minimize transmission line effects.

3.2.4 Link ECC

Both Read and Write have error correction available. It is anticipated that this feature will be used at bit rates approaching 6.0 Gbps and higher.

3.2.5 Signal Conditioning, DFE

In order to improve signal capture, a single tap of decision feedback equalization is available at both the DRAM and at the host IO.

4 Protocol Specific Implementation and Routing Guidelines

The following sections discuss routing and interconnect implementation recommendations and emphasize the parameters that are critical for the specific protocols.

4.1 LPDDR4/4X Specific Routing and Implementation Guidelines

4.1.1 Supply Noise Requirements.

To control power supply induced jitter effects, the power rail noise should adhere to the following conditions:

LPDDR4
VDD - +/-2.0% noise
VDDQ/VDD2: +/- 5% noise. (These are merged for LPDDR4 operation)
Package/Die LC resonant peak should be below 150 MHz

LPDDR4X
VDD - +/-2.0% noise
VDDQ (0.6V): +/- 5% noise.
VDD2 (1.1V): +/- 5% noise.
Package/Die LC resonant peak should be below 150 MHz

4.1.2 Crosstalk Control

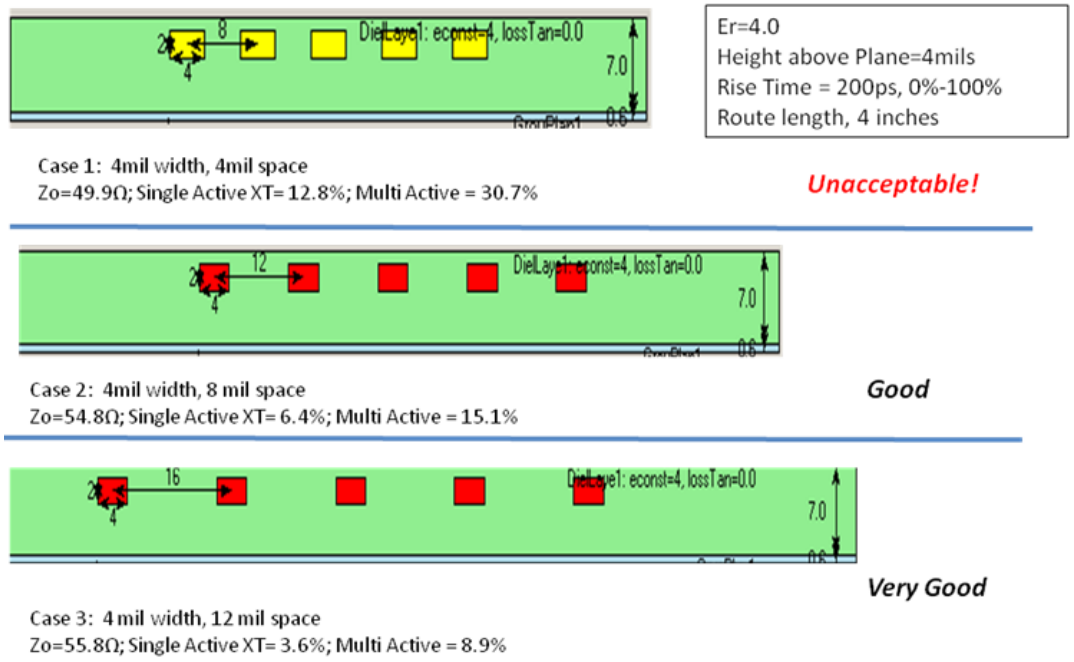
Crosstalk and characteristic impedance of an array of traces are interrelated. To minimize crosstalk, the characteristic impedance of a trace should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces. To achieve this, the space between traces should be 2X to 3X the height of the trace above the ground plane. Longer routed parallel lengths should have wider spacing.

Figure 11 shows three cases that depict this relationship. Case 1 depicts a typical routing scheme with equal lines and spaces. While the Zo of these lines looks good at 49.9 Ω, much of this impedance is determined by the proximity of the neighboring lines. Consequently, there is very high near end crosstalk from multiple aggressors of 30.8%. For a 1.8 V signal, this is 473 mV. For Case 2, where the space is doubled, the Zo rises to 54.8 Ω and the multi-active crosstalk is cut in half to 15.1%, a more manageable number. In this case, the Zo is determined more by the proximity of

the reference plane instead the neighboring traces. Further isolation, shown in Case 3, decreases crosstalk with only a 1 Ω increase in Zo. When increasing spacing has no effect on Zo, the traces are said to be isolated.

Note that stripline applications can tolerate narrower spacing within in signal groups. Because the fields from all signals are captured within the same dielectric constant substrate, there are no differences in the mode velocities from different switching patterns. If necessary, spacing can be cut to 1.5X to 2X the height to the nearest reference plane in stripline applications. While this tighter spacing can be used if necessary in stripline, wider spacing is always preferred.

Figure 4-1 Relationship between Characteristic Impedance and Crosstalk



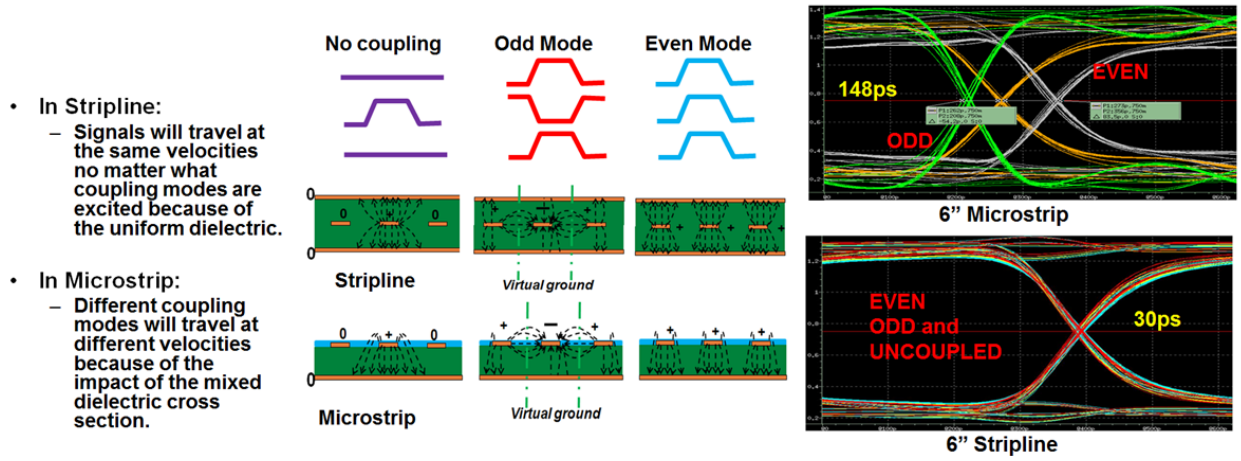
Crosstalk between dissimilar function groups can have unpredictable timing effects and should be avoided. It is recommended that the spacing between byte lanes and the spacing between the byte lanes and the CA region be a minimum of 3X the height above the reference plane. Also, spacing to strobes and clocks must also be increased to assure that crosstalk does not compromise the monotonicity of the system's strobes and clocks.

4.1.3 Stripline vs. Microstrip.

For LPDDR4/4X applications that exceed 2400 Mbps, it is highly recommended that microstrip configurations be avoided. Because of the mixed dielectric materials in a microstrip configuration, different coupled modes will travel at different velocities causing temporal dispersion at the target device. This increases with routed length. Since signals traveling in stripline see a uniform dielectric, the dispersion is greatly reduced. At high bit rates, timing budgets cannot tolerate the

margin loss to this modal dispersion. If Microstrip must be used, it should be confined to short lengths with spacing that is greater than 3X the height to the reference plane.

Figure 4-2 Signal Dispersion in Microstrip and Stripline.



4.1.4 Routing Skew for LPDDR4/4X – Summary and Discussion

There are many trainings available for the LPDDR4/4X interface that can remove skew. The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table 2 lists recommended skew targets for LPDDR4/4X. A further discussion of these is found below.

Note

Intra-pair skew between the true and complement legs of a differential pair should be kept below 3ps to preserve monotonicity of the DQS/DQS# or CK/CK# differential signals. Uncertainty at the zero crossing point can lead to timing budget erosion.

Table 4-1 Summary of outing skew requirements for LPDDR4

System Routing requirements for LPDDR4/4X 4267 operation			
Constraints	**Available Deskew Range***	**Recommended Routed Skew Limits (RDL, Package, and Board)**	**Notes**
DQ to DQS domain	DQS position +/-100 ps	DQS position +/-25 ps	It is highly recommended that flight times across the data lanes be tightly matched in order to preserve operating margin and reduce vertical eye collapse that can occur from crosstalk between unaligned DQ signals.

ODT, CKE, Cmd, Add to CK/CK#	CK position +/- 100 ps	CK position +/-50 ps	PHY supports per bit deskew of all CA bits other than CS.
CS	CK position +/- 100 ps	CK position +/-10 ps	Tight skew is required because deskew is not supported for CS. Also, there can be significant skew associated with DRAM implementation with multiple ranks.
DQS to CK domain	-0.5 to +4.47 Clock Cycles	CK edge position +/- 60 ps. (without Write Leveling)	Write Leveling training can compensate for delay differences that extend over multiple clock cycles.

*Available deskew range represents the total deskew capability of the IP. This value must will be consumed by DRAM skews, including skew impact of routing to different ranks, and interconnect skews from the PHY IO pad to the DRAM pin.

4.1.5 Package Considerations for LPDDR4/4X

- Wire bond packages are not recommended for LPDDR4/4X interfaces.
- An analysis of the supply impedance should be undertaken to make sure the targets listed previously are met. The implementer should simulate his particular interface with expected switching patterns to assure that the targets listed herein are appropriate to their application.
- To control crosstalk, the spacing between signals of the same group should be kept to a minimum of 2X the height to the nearest reference plane. Spacing of 3X should be maintained to all differential signals and between signal groups.
- To reduce power supply induced jitter, data bus inversion should be implemented. Because DQ and DQS intentionally, the interface is more susceptible to PSIJ. DBI can reduce the amount of supply noise and consequently the jitter produced.
- For operation above 2400 Mbps, microstrip routing should be avoided. Since the signals routed in microstrip are exposed to a mixed dielectric environment, crosstalk will create timing differences among the different coupling modes. This will result in far end crosstalk that will erode the timing margins.

4.2 LPDDR5 Specific Routing and Implementation Guidelines

All guidance for LPDDR4/4X applies to LPDDR5. Guidance specific to LPDDR5 is found below.

4.2.1 Via Impact

With planned bit rates of 6400 Mbps, the impact of via stubs may have an impact on eye quality, depending on the thickness of the substrate or board environment. The impact of stubs should be minimized through judicious routing layer selection as well as, potentially, the use of blind and

buried vias and back-drilling. Simulations should be performed to determine the eye quality and the impact of via stubs on the final result.

4.2.2 Supply Noise Requirements.

To control power supply induced jitter effects, the power rail noise should adhere to the following conditions:

LPDDR5
VDD - +/-2.0% noise
VDDQ (0.5V and 0.3V): +/- 5% noise.
VDD2 (1.05V): +/- 5% noise.
Package/Die LC resonant peak should be below 150 MHz

4.2.3 Routing Skew for LPDDR5 – Summary and Discussion

There are many trainings available for the LPDDR5 interface that can remove skew. The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table 2 lists recommended skew targets for LPDDR4/4X. A further discussion of these is found below.

Note

Intra-pair skew between the true and complement legs of a differential pair should be kept below 3ps to preserve monotonicity of the DQS/DQS# or CK/CK# differential signals. Uncertainty at the zero crossing point can lead to timing budget erosion.

Table 4-2 Summary of Outing Skew Requirements for LPDDR5

System Routing requirements for LPDDR5 Operation			
Constraints	**Available Deskew Range***	**Recommended Routed Skew Limits (RDL, Package, and Board)**	**Notes**
DQ to WCK (Write)	WCK position +/-75 ps	WCK position +/-25 ps	It is highly recommended that flight times across the data lanes be tightly matched in order to preserve operating margin and reduce vertical eye collapse that can occur from crosstalk between unaligned DQ signals.
DQ to RDQS (Read)	RDQS position +/-75 ps	RDQS position +/-25 ps	
CS and CA to CK/CK#	CK position +/-150 ps	CK position +/-50 ps	PHY supports per bit deskew of the CA and CS bits.
WCK to CK domain	-1.5 - 4.47 Clock Cycles	CK edge position +/-50 ps. (without Write Leveling)	Write Leveling training can compensate for delay differences that extend over multiple clock cycles.

*Available deskew range represents the total deskew capability of the IP. This value must will be consumed by DRAM skews, including skew impact of routing to different ranks, and interconnect skews from the PHY IO pad to the DRAM pin.

5 Power Integrity Analysis

Power Integrity (PI) analysis and design is key for the successful system integration, function and sign-off.

The goal of this section is to raise awareness to specific aspects relevant to Synopsys DDR PHY, namely matching the usage of PI deliverables provided by Synopsys to the analysis being targeted.

Synopsys IP support and standard delivery includes PI deliverable package containing:

- Supply current profile (icc(t) piecewise linear current vs time in a PWL file format), and
- On-die equivalent Cdie/Rdie report/information for the IP hard macros.

These are provided typically for the following Process-Voltage-Temperature (PVT) corners:

- TT process corner, nominal voltage, 25ºC
- FF process corner, high voltage, 125ºC
- SS process corner, low voltage, -40ºC. Note that PWL at SS/-40ºC is provided for limited PHY deliveries. In cases where PWL at SS/-40ºC is not provided, scaling TT/25ºC PWL by 90% is a very good approximation

In general, the SIPI wise sign-off a DDR IP integration in a SOC requires two type of power integrity analysis:

1. Reliability Analysis, which typically includes Electromigration (EM) and IR-drop analysis
    a. The goal is to ensure that on-die (and on-chip) supply power and ground mesh are robust, and hot spots are under control and do not cause any reliability issues.
    b. Worst case condition for EM/IR is usually FF process corner/high voltage/high temperature.
    c. Consequently, the use of the supply icc(t) PWL for this corner is recommended.

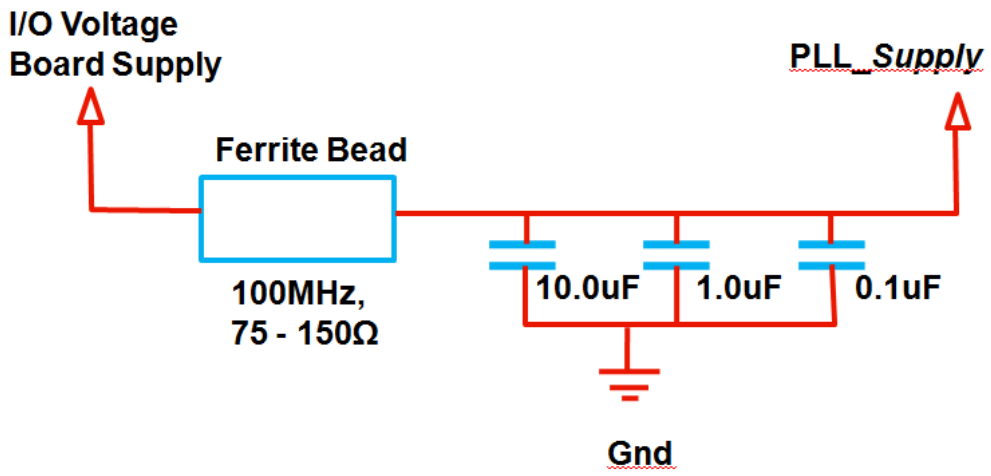
2. Supply AC ripple Analysis
    a. Both IO and core supply of IP hard macros present specific supply current transient signatures. When such current transient interacts with non-ideal power distribution network comprised of die, package and board, it results in voltage fluctuation observed across the chip power nodes. Consequently, power supply induced jitter (PSIJ) is generated both in IO and core domain, directly affecting the system timing and function.

b. Synopsys IP databook defines supply AC ripple spec both for IO and core voltage. Customer system design (on-die, package and board) should be such that the AC ripple specs are met. Otherwise, additional timing penalty due to higher voltage ripple must be considered.
c. PSIJ is usually worst at SS process corner, so supply icc(t) PWL and associated Cdie/Rdie at SS corner should be used to assess the supply AC ripple of the system as seen on-die at the IP pins.

5.1 PLL Supply (VAA_VDD2) Guidance

The supply impedance for the PLL should be designed to maintain ripple within a +/-1% envelope. One filter network on the board should be adequate to support the PLLs for up to 6 channels. An example filter network is shown below. A ferrite bead is included based on the assumption that the PLL supply is shared with VDD2 (1.1 or 1.05 V supply). If a dedicated supply for VAA_VDD is supplied, the ferrite bead shouldn't be necessary.

Figure 5-1 Example Filter Network for PLL Supply Impedance



6 Other Topics

6.1 BP_ZN Calibration Resistor Connection

The total capacitance on the net connecting from the BP_ZN bump to the external calibration resistor must be limited. The limit is set to allow signal level updates during calibration to settle within the required amount of time to generate a valid reading. Drive impedance changes on BP_ZN can be large, so excess capacitance will not allow the signal to settle to its final level.

The capacitance limit includes intrinsic wiring capacitance as well as explicitly placed capacitance.

Parameter	Minimum	Maximum
BP_ZN cap loading	0	100 pF

7 Timing Budgets for the LPDDR5/4/4X PHY

When implementing a DDR interface, the primary determinant of overall functionality is whether the timing budget closes at the target bit rate. There are three primary components to any timing budget:

1. SDRAM Contributions
2. PHY Contributions
3. Interconnect Contributions

Each of these contributors erodes the source synchronous timing of the SDRAM interface. SDRAM contributions should be obtained from the databook of the vendor of the SDRAM to be used. Values from JEDEC standards can also be used if they are available, though the vendor datasheets are always preferred.

Interconnect contributions are application specific and are the responsibility of the interface implementer. These contributions include crosstalk, skew, simultaneous switching noise, intersymbol interference, reflections, etc. These should be determined through measurement or simulation. Note that the maximum bit rates supported by JEDEC protocols typically represent point to point interconnect implementations. Interconnect environments other than point to point will result in a final supported bit rate lower than the maximum outlined in the JEDEC protocol.

PHY contributions include all those effects associated with the PLL, macro blocks and I/O during transmitting and receiver operations. These effects include skews, pulse width distortion, jitter effects and training errors. These effects are detailed within the timing budgets found in the foregoing sections. The budgets listed include all the PHY components for each operation as well as the SDRAM contributions. These elements will be summed. The margin that remains will apply to the interconnect contributions.

The timing budgets that are presented in this section are general example budgets for the LPDDR5/4/4X IP family.

They do not represent a specific IP silicon process implementation and are intended only as guidance in determining how much budget must be allocated for the host IP.

Budget spreadsheets for specific IP products, protocols and bit rates are available upon request.

7.1 LPDDR4/4X Protocol Timing Budgets-4267Mbps

7.1.1 Write Transaction Budget

The budget below applies to both LPDDR4 and LPDDR4X interfaces.

For the transmit timing budget, the PHY components contributing to the DQ to WCK timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM input mask requirements. Write budgets for LPDDR4 are shown below. Subtracting this total from the Unit Interval, 234.4 ps at 4267 Mbps, will yield the budget available for interconnect induced uncertainties. Summation of the components is done using two methods, an extremely conservative method that sums all components linearly, and a method that sums the variable elements in the budget using a root sum squares methodology to remove the extreme conservatism of the linear method. Synopsys recommends using the RSS method to qualify an interface. The components comprising the PHY contributions are:

- PLL jitter sources
- Power supply induced jitter assuming:
    - +/-2.0% noise with primary resonance below 150 MHz for VDD Supply,
    - +/-5.0% noise with primary resonance below 150 MHz for VDDQ Supply.
    - Note: tDQS2DQ specification will shift DQ relative to its strobing DQS by several unit intervals. Consequently, beneficial jitter tracking is reduced requiring a tighter noise specification during Write transmit operations.
- Strobe alignment errors including
    - Delay line step granularity
    - Integrated nonlinearity
    - Aging
- Delay mismatch between rising and falling edges
- SDRAM data input mask width requirements are defined by JEDEC Standard JESD209-4.

.

Table 7-1 Write Budget for LPDDR4/4X for 0.75 V Core Voltage

Transmit (Write) Budget Tables VDD=0.7125 V (0.75 V Nominal)			
Component	**Setup (ps)**	**Hold (ps)**	**Notes**
UI width at 4266.7 Mb/s	**117.2**	**117.2**	
Data Dependent Jitter			
Output Rise/Fall Mismatch	3.2	3.2	Delay differences between rising and falling edges after trainng.
VDD -PSIJ (+/-2% from HF noise)	18.0	18.0	Jitter induced by noise on the VDD Rail
VDDQ/LP -PSIJ (+/- 5% from HF noise)	1.0	1.0	Jitter induced by noise on the VDDQ Rail
Training Error			
Strobe Alignment Error	11.1	12.9	Alignment of Strobe in Data
Aging	2.0	2.0	Aging of Delay Lines
PLL Jitter (BER=1E-16)	1.1	1.1	RefClk feed-through, internal noise,supply modulation
Total TX Components	**36.4**	**38.2**	
Total TX Components (RSS)	**24.5**	**25.5**	
DRAM Receiver Mask	29.3	29.3	0.25UI Requirement
Oscillator Tracking Error	20.0	20.0	
Oscillator Granularity	2.0	2.0	
Total RX Components	**51.3**	**51.3**	
Total RX Components (RSS)	**35.5**	**35.5**	
Remaining System Margin after PHY and SDRAM	**29.5**	**27.7**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.
Remaining System Margin after PHY and SDRAM (RSS)	**57.2**	**56.2**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.

7.1.2 Read Transaction Budget

The budget below applies to both LPDDR4 and LPDDR4X interfaces.

For the receive timing budget, the PHY components contributing to the DQ to RDQS timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM output timing specifications. Subtracting this total from the Unit Interval, 234.4 ps at 4267 Mbps, will yield the budget available for interconnect induced uncertainties. Summation of the components is done using two methods, an extremely conservative method that sums all components linearly, and a method that sums the variable elements in the budget using a root sum squares methodology to remove the extreme conservatism of the linear method. Synopsys recommends using the RSS method to qualify an interface. The components comprising the PHY contributions are:

- Power supply induced jitter assuming:
  - +/-2.0% noise on the VDD Rail
  - Note: The VDDQ domain is not involved during the Read operation capturing
  - The PHY receiver path will shift DQS relative to DQ by several unit intervals. Consequently, beneficial jitter tracking is reduced requiring a tighter noise specification during Read operations.
- Strobe alignment errors including
  - Delay line step granularity
  - Integrated nonlinearity
  - aging
- Delay mismatch between rising and falling edges
- Receiver flop set up and hold
- Receiver VREF placement error
- SDRAM data output timings are defined by JEDEC Standard JESD209-4.

Table 7-2 Read Budget for LPDDR4/4X for 0.75 Core Voltage

Receive (Read) Budget Tables VDD=0.7125V (0.75V Nominal)- Linear and RSS Summation non-Boost			
Component	**Setup (ps)**	**Hold (ps)**	**Notes**
UI width at 4266.7Mb/s	**117.2**	**117.2**	
Power Supply Induce Jitter			
VDD(DQSIO) -PSIJ (+/- 2.0% from HF noise)	18.6	18.6	Data to Strobe Power supply induced jitter, assuming 2.5UI DQ/DQS separation
Training Error			
Strobe Alignment Error	9.4	11.4	Alignment of Strobe in Data
Replica to DQS tracking Error	3.5	3.5	RX replica tracking error
Aging	4.0	4.0	Aging of Delay Lines
Vref Error	1.2	1.2	Vref accuracy and Supply noise
Flop SU/Hd Requirements	8.0	8.0	
Total RX Components (Linear)	***44.7***	***46.7***	
Total RX Components (RSS)	**29.5**	**30.5**	
DRAM Transmitter Data Valid Window	35.2	35.2	Uncertainty based on (1-tQW_Total)*UI from JEDEC standard. 0.7@4267Mbps.
Total TX Components	**35.2**	**35.2**	
Remaining System Margin after PHY and SDRAM (Linear)	***37.3***	***35.3***	*Linear Summation of RX components.*
Remaining System Margin after PHY and SDRAM (RSS)	**52.5**	**51.5**	RSS Summation of RX components.

7.1.3 Command/Address /Control Transaction Budget

The budget below applies to both LPDDR4 and LPDDR4X interfaces.

For LPDDR4/4X at 6400 Mbps, the CA operates at 2133 Mbps, captured by a 2133 MHz SDR clock. For the Cmd/Add/Ctl transmit timing budget, the PHY components contributing to the CA to CK timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM input mask requirements. Subtracting this total from the Unit Interval, 468.8 ps at 2133 Mbps, will yield the budget available for interconnect induced uncertainties including skew. Only a linear summation budget is shown for the single data rate CA budget. RSS techniques may be applied if desired. The components comprising the PHY contributions are:

- PLL jitter sources
- Power supply induced jitter assuming:
  - +/-2.0% noise on the VDD Rail
  - +/-5% noise on the VDDQ rail
- On die delay mismatch.
- SDRAM CA input mask width requirements are defined by JEDEC Standard JESD209-4.

Table 7-3 Cmd/Add/Ctrl Budget for LPDDR4/4X for 0.75V Core Voltage

CA Transmit Budget Tables VDD=0.7125V (0.75V Nominal) - Linear Summation Component	Setup (ps)	Hold (ps)	Notes
CA UI width at 4266.7Mb/s - 1066.675Mbps	**234.4**	**234.4**	
Data Dependent Jitter			
Output Rise/Fall Mismatch	3.2	3.2	Delay differences between rising and falling edges. Includes lane to lane variation.
VDD -PSIJ (+/-2.0 from HF noise)	6.8	6.8	Jitter induced by noise on the VDD Rail
VDDQ/LP -PSIJ (+/-5% from HF noise)	1.0	1.0	Jitter induced by noise on the VDDQ Rail
On Die Mismatch	25.0	25.0	Process delay variations across CA bus.
PLL Jitter	1.4	1.4	RefClk feed-through, internal noise,supply modulation
Total TX Components	**37.4**	**37.4**	
DRAM Receiver Requirement	**70.3**	**70.3**	0.3UI Requirement (UI=tCK(avg))
CK to CA Routing Skew	**25.0**	**25.0**	Per Synopsys Guidelines
Remaining System Margin after PHY and SDRAM	**101.7**	**101.7**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.
Budget assumes all error terms correlated at worst case values, a highly pessimistic assumption. Silicon performance will be better than the numbers reflected here.			

7.2 LPDDR5 Protocol Timing Budgets-6400 Mbps

7.2.1 Write Transaction Budget

For the transmit timing budget, the PHY components contributing to the DQ to WCK timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM input mask requirements. Write budgets for LPDDR5 are shown below. Subtracting this total from the Unit Interval, 156.3 ps at 6400 Mbps, will yield the budget available for interconnect induced uncertainties. Summation of the components is done using two methods, an extremely conservative method that sums all components linearly, and a method that sums the variable elements in the budget using a root sum squares methodology to remove the extreme conservatism of the linear method. Synopsys recommends using the RSS method to qualify an interface. The components comprising the PHY contributions are:

- PLL jitter sources.
- Power supply induced jitter assuming:
    - +/-2.0% noise with primary resonance below 150 MHz for VDD Supply,
    - +/-5.0% noise with primary resonance below 150 MHz for VDDQ Supply.
    - Note: tWCK2DQi specification will shift DQ relative to its strobing WCK by several unit intervals. Consequently, beneficial jitter tracking is reduced requiring a tighter noise specification during Write transmit operations.
- Strobe alignment errors including
    - Delay line step granularity
    - Integrated nonlinearity
    - Aging
- Delay mismatch between rising and falling edges.
- SDRAM data input mask width requirements are defined by JEDEC Standard TBD.

Table 7-4 Write Budget for LPDDR5 for 0.75 V Core Voltage

Transmit (Write) Budget Tables VDD=0.7125V (0.75V Nominal) - Linear Summation			
Component	**Setup (ps)**	**Hold (ps)**	**Notes**
UI width at 6400Mb/s	**78.1**	**78.1**	
Data Dependent Jitter			
Output Rise/Fall Mismatch	3.2	3.2	Delay differences between rising and falling edges after trainng.
VDD -PSIJ (+/-2% from HF noise)	16.9	16.9	Jitter induced by noise on the VDD Rail
VDDQ -PSIJ (+/- 5% from HF noise)	1.0	1.0	Jitter induced by noise on the VDDQ Rail
Training Error			
Strobe Alignment Error	10.1	11.1	Alignment of Strobe in Data
Aging	2.0	2.0	Aging of Delay Lines
PLL Jitter (BER=1E-16)	0.7	0.7	RefClk feed-through, internal noise,supply modulation
Total TX Components	**33.9**	**34.9**	
Total TX Components (RSS)	**23.0**	**23.6**	
DRAM Receiver Mask	27.3	27.3	0.35UI Requirement (tDIVW1)
Oscillator Tracking Error	7.5	7.5	Voltage Matching Error.
Oscillator Granularity	2.0	2.0	
Total RX Components	**36.8**	**36.8**	
Total RX Components (RSS)	**28.4**	**28.4**	
Remaining System Margin after PHY and SDRAM	**7.4**	**6.4**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.
Remaining System Margin after PHY and SDRAM (RSS)	**26.7**	**26.1**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.

7.2.2 Read Transaction Budget

For the receive timing budget, the PHY components contributing to the DQ to RDQS timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM output timing specifications. Subtracting this total from the Unit Interval, 156.3 ps at 6400 Mbps, will yield the budget available for interconnect induced uncertainties. Summation of the components is done using two methods, an extremely conservative method that sums all components linearly, and a method that sums the variable elements in the budget using a root sum squares methodology to remove the extreme conservatism of the linear method. Synopsys recommends using the RSS method to qualify an interface. The components comprising the PHY contributions are:

- Power supply induced jitter assuming:
  - +/-2.0% noise on the VDD Rail
  - Note: The VDDQ domain is not involved during the Read operation capturing
  - The PHY receiver path will shift RDQS relative to DQ by several unit intervals. Consequently, beneficial jitter tracking is reduced requiring a tighter noise specification during Read operations.
- Strobe alignment errors including
  - Delay line step granularity
  - Integrated nonlinearity
  - aging
- Delay mismatch between rising and falling edges
- Receiver flop set up and hold
- Receiver VREF placement error
- SDRAM data output timings are defined by JEDEC Standard TBD.

Table 7-5 Read Budget for LPDDR5 for 0.75 Core Voltage

Receive (Read) Budget Tables VDD=0.7125V (0.75V Nominal)- Linear and RSS Summation non-Boost			
Component	**Setup (ps)**	**Hold (ps)**	**Notes**
UI width at 6400Mb/s	**78.1**	**78.1**	
Power Supply Induce Jitter			
VDD(DQSIO) -PSIJ (+/- 2.0% from HF noise)	12.4	12.4	Data to Strobe Power supply induced jitter, assuming 2.5UI DQ/DQS separation
Training Error			
Strobe Alignment Error	9.7	10.5	Alignment of Strobe in Data
Replica to DQS tracking Error	3.5	3.5	RX replica tracking error
Aging	4.0	4.0	Aging of Delay Lines
Vref Error	1.2	1.2	Vref accuracy and Supply noise
Flop SU/Hd Requirements	8.0	8.0	
Total RX Components (Linear)	***38.8***	***39.6***	
Total RX Components (RSS)	**24.7**	**25.1**	
DRAM Transmitter Data Valid Window	22.6	22.6	From latest Jedec "LPDDR5 DQ N-UI Tx Jitter Spec" Sept 27
Total TX Components	**22.6**	**22.6**	
Remaining System Margin after PHY and SDRAM (Linear)	***16.7***	***15.9***	*Linear Summation of RX components.*
Remaining System Margin after PHY and SDRAM (RSS)	**30.9**	**30.4**	RSS Summation of RX components.
Budget assumes all error terms correlated at worst case values, a highly pessimistic assumption. Silicon performance will be better than the numbers reflected here.			

7.2.3 Command/Address /Control Transaction Budget

For LPDDR5 at 6400 Mbps, the CA operates at 1600 Mbps, captured by an 800 MHz DDR clock. For the Cmd/Add/Ctl transmit timing budget, the PHY components contributing to the CA to CK timing error are summed at the output of the I/O portion of the PHY. These components are then summed with the SDRAM input mask requirements. Subtracting this total from the Unit Interval, 625 ps at 1600 Mbps, will yield the budget available for interconnect induced uncertainties including skew. Only the linear summation budget is shown below. RSS techniques may be applied if desired. The components comprising the PHY contributions are:

- PLL jitter sources
- Power supply induced jitter assuming:
  - +/-2.0% noise on the VDD Rail
  - +/-5% noise on the VDDQ rail
- On die delay mismatch.

SDRAM CA input mask width requirements are defined by JEDEC Standard TBD.

Table 7-6 Cmd/Add/Ctrl Budget for LPDDR5 for 0.75 V Core Voltage

CA Transmit Budget Tables VDD=0.7125V (0.75V Nominal) - Linear Summation Component	Setup (ps)	Hold (ps)	Notes
CA UI width at 6400Mb/s - 1600Mbps	**312.5**	**312.5**	
Data Dependent Jitter			
Output Rise/Fall Mismatch	3.2	3.2	Delay differences between rising and falling edges. Includes lane to lane variation.
VDD -PSIJ (+/-2.0 from HF noise)	9.2	9.2	Jitter induced by noise on the VDD Rail
VDDQ -PSIJ (+/-5% from HF noise)	1.0	1.0	Jitter induced by noise on the VDDQ Rail
On Die Mismatch	25.0	25.0	Process delay variations across CA bus.
PLL Jitter	1.4	1.4	RefClk feed-through, internal noise,supply modulation
Total TX Components	**39.8**	**39.8**	
DRAM Receiver Requirement	**93.8**	**93.8**	0.3UI Requirement (UI=tCK(avg)) At VREF Level
CA to CA offset in 2 Rank Implementation	**75.0**	**75.0**	
CK to CA Routing Skew	**25.0**	**25.0**	Per Synopsys Guidelines
Remaining System Margin after PHY and SDRAM	**79.0**	**79.0**	Interconnect uncertainty from simulation measured at DRAM receiver thresholds.
Budget assumes all error terms correlated at worst case values, a highly pessimistic assumption. Silicon performance will be better than the numbers reflected here.			