



# **DesignWare® Cores LPDDR5/4/4X PHY Initialization (PHYInit) Software Overview**

**Application Note**

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***DWC LPDDR5/4/4X PHY***

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# Revision History

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Links and references to section, table, figure, and page numbers in this table are only assured to be valid for the version in which the change is made.

This application note supports current and previous PHYInit version.

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Date	Document Version	Description
December 12, 2019	1.00	Generic Document Initial release



# 1

## Introduction

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### 1.1 What is PHYInit?

PhyInit is a program to generate txt files corresponding to sequence of registers writes/reads required to initialize the PHY for mission mode. The output txt file is generated based on user programming of PhyInit inputs.

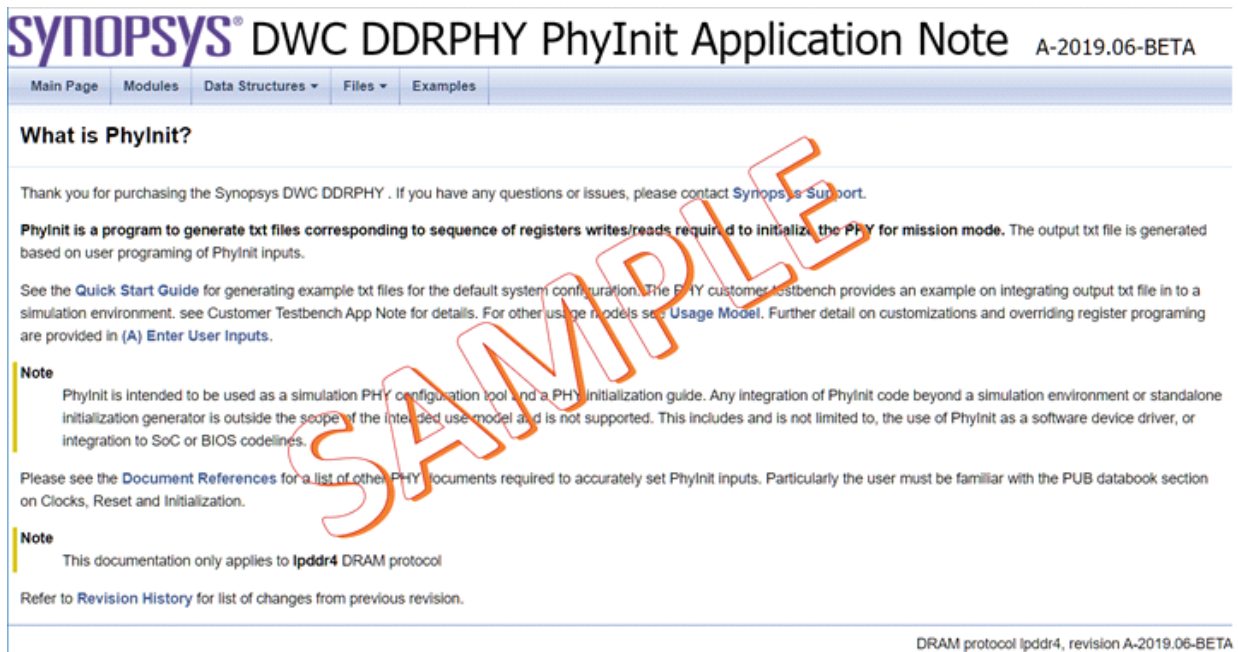
A quick start guide and a README is provided in PhyInit folder in order to speed up initial integration. Final sequence can be obtained only when all PhyInit configuration is fully considered. This document only covers a high level overview of the initialization process.

The PhyInit software and corresponding PhyInit Application Note (HTML version) are available in the following path in the deliverables directory:

```
<PHY Install  
Directory>/synopsys/<technology>_<process>/Latest/phyinit/Latest/software/<protocol>/doc/
```

For ease of use, a Microsoft Compiled HTML (.CHM) as well as HTML tar file of the documentation is provided. This document will provide an introductory overview of PhyInit with references to HTML documentation. [Figure 1-1](#) on page 8 shows the opening page of HTML documentation.

Figure 1-1 PhyInit HTML Documentation

**Note**

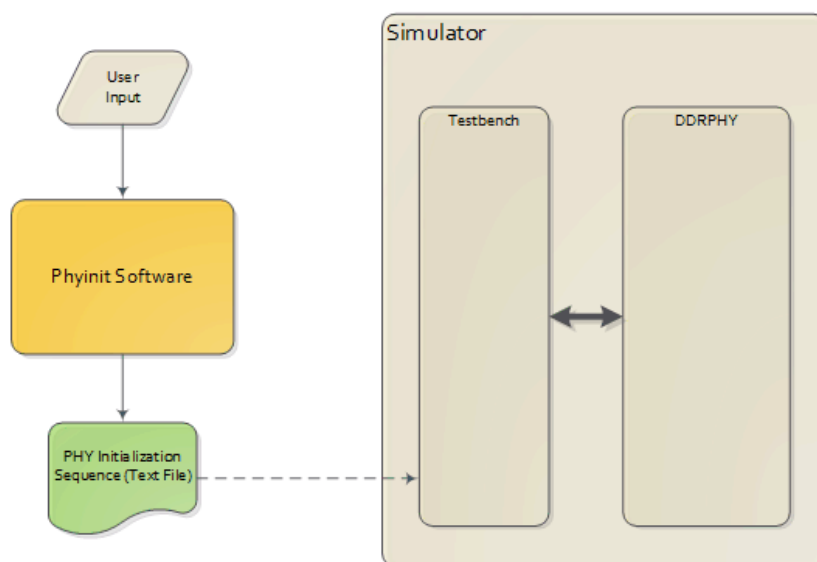
PhyInit is intended to be used as a simulation PHY configuration tool and a PHY initialization guide. Any integration of PhyInit code beyond a simulation environment or standalone initialization generator is outside the scope of the intended use model and is not supported. This includes and is not limited to, the use of PhyInit as a software device driver, or integration to SoC or BIOS codelines.

## 1.2 Purpose

The purpose of the PHY initialization software (PhyInit) is to allow the user to generate a customized PHY initialization sequence specific to the user's system configuration. The user will provide a set of configuration inputs to the program and it will output a PHY initialization sequence text file specific to the inputs provided. The user can choose to execute or skip the training firmware in the initialization sequence.

The PHYInit software is written in C and outputs a text file for each DRAM protocol specifying the exact registers that need to be set at each of the PHY initialization steps describes in the section “Phase Bits and Chip Selects” of the *PUB Databook*. [Figure 1-2](#) shows the role of PHYInit software in a simulation of the PHY.



**Figure 1-2 Overview**

The following sections of this document will describe organization and use of the PhyInit software.



## 2

## About This Document

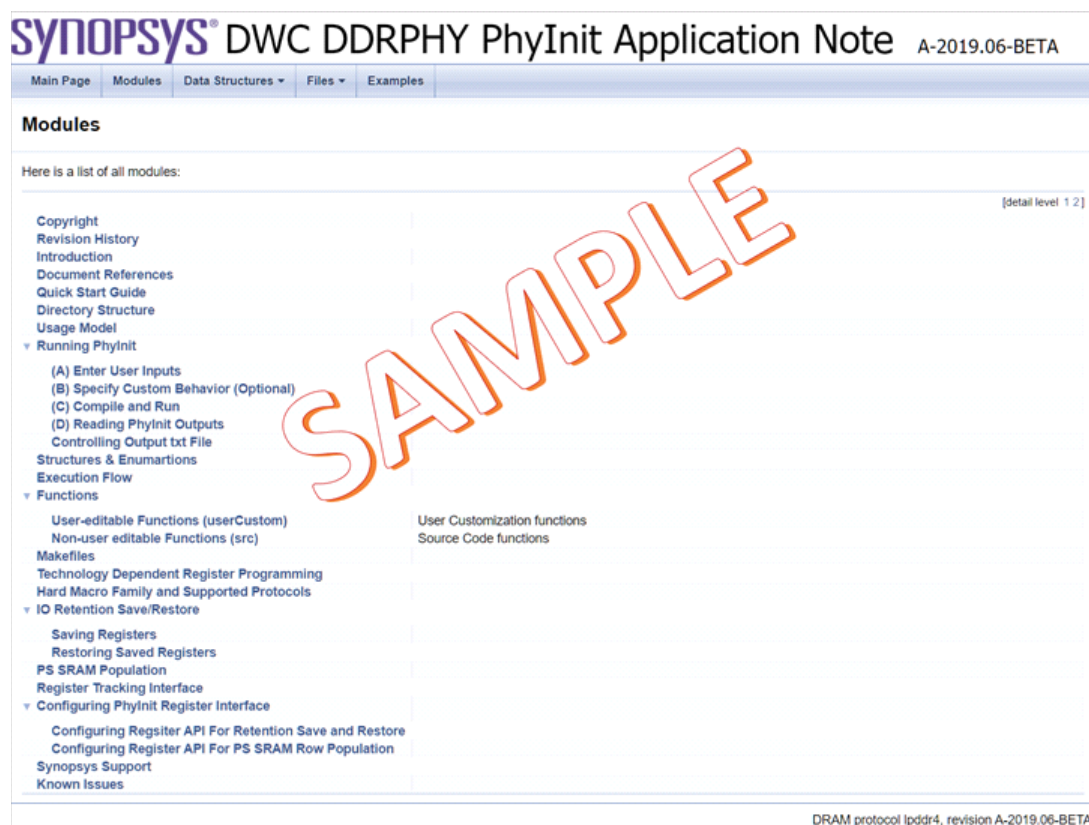
This document provides only an overview of topics on PhyInit. For detailed documentation, refer to the “Modules” page in the HTML document pictured below. Specific details for each DRAM protocol differ. A dedicated version of HTML documentation for each DRAM protocol is provided in the release package.



### Note

The image captures of the Phylnit HTML documentation in this document are provided for reference and can be out of date. Always refer the HTML documentation directly for accurate up-to-date documentation.

**Figure 2-1 Modules page in HTML Documentation**





## 3

## Document References

Following documents are referenced in the application note.

**Table 3-1** PHY Documents Required to Set PHYInit Inputs

Document Reference	Document Name
Training firmware Application Note	DesignWare® Cores Firmware Training Application Notes
PUB Databook	DesignWare® Cores PHY Utility Block (PUB) Databook
PHY Databook	DesignWare® Cores PHY Databook
DQ HSPICE Application Note	DesignWare® Cores TXRXDQ Slice HSPICE Driver and Receiver Model for your process technology
CA HSPICE Application Note	DesignWare® Cores TXRXCA Slice HSPICE Driver and Receiver Model for your process technology
Customer Testbench App Note	DesignWare® Cores DDRn PHY Customer Testbench Application Note



# 4

## Running PHYInit

The user shall follow the flow shown in [Figure 4-1](#) to prepare the input data and run PhyInit. Each step is described further in details in the HTML documentation under the section “Running PhyInit”. For details of each step from A through D refer to HTML documentation.

**Figure 4-1** Running PhyInit Page

**SYNOPSYS®** DWC DDRPHY PhyInit Application Note A-2019.06-BETA

Main Page Modules Data Structures Files Examples

### Running PhyInit

Modules

- (A) Enter User Inputs
- (B) Specify Custom Behavior (Optional)
- (C) Compile and Run
- (D) Reading PhyInit Outputs Controlling Output txt File

#### Detailed Description

##### Overview of steps

The user shall follow the flow shown in Figure 3 to prepare the input data and run PhyInit. Each step is described in subsequent sections.

```
graph TD; A["(A) Enter User Input"] --> B["(B) Specify Custom Behavior (Optional)"]; B --> C["(C) Compile and Run"]; C --> D["(D) Read Outputs"]; style A fill:#f0f0f0,stroke:#333,stroke-width:1px; style B fill:#f0f0f0,stroke:#333,stroke-width:1px; style C fill:#f0f0f0,stroke:#333,stroke-width:1px; style D fill:#f0f0f0,stroke:#333,stroke-width:1px;
```

PhyInit usage flow

DRAM protocol lpddr4, revision A-2019.06-BETA

## 4.1 (A) Enter User Inputs

There are 5 keys inputs that need to be specified:

1. `user_input_basic`
2. `user_input_advanced`
3. `user_input_sim` (simulation only)
4. Technology specific register programming
5. Firmware Message Block

These inputs are discussed in the details in various sections in the HTML documentation. The user must obtain the required data to program and configure them for their specific application. More detail guidance is provided in the HTML documentation. A capture of the specific page in HTML documentation is provided below for reference.

**Figure 4-2 Enter User Inputs Page**

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### (A) Enter User Inputs

Running PhyInit

The user must provide a set of configuration inputs to PhyInit to indicate physical PHY configuration, clock frequencies, DRAM-specific information and feature options.

In the simplest use case, the user must edit the file `userCustom/dwc_ddrphy_phyinit_setDefault.c`. The file is composed of user input fields and the associated values that the user shall provide. A detailed description of each user input field for the above structures can be found in documentation for `src/dwc_ddrphy_phyinit_struct.h`. Each protocol has a unique `dwc_ddrphy_phyinit_setDefault.c` file containing fields specific for the protocol. The user inputs are divided into 4 main categories:

1. **`user_input_basic`** - these are inputs that the user must enter information specific to their configuration. The user must replace the default values in the field with their specific settings.
2. **`user_input_advanced`** - these are optional inputs. The user can choose to enter new values or use the default values.
3. **`user_input_sim`** - these are inputs that the user shall enter if execution of training firmware skipped. If training firmware is executed, the user can leave these fields at their default value.
4. **Technology specific register programming** - These are register programming that is specific to a particular technology node or specific characteristics of an SoC. See PhyInit App Note for details.
5. **Firmware Message Block ( `mnPmuSramMsgBlock_lpddr4.h` `mnPmuSramMsgBlock_lpddr4_2d.h` )** these are inputs to the firmware message block required to execute the training firmware. PhyInit populates some of the message block variables based on `user_input_basic` and `user_input_advanced`. See `dwc_ddrphy_phyinit_calcMb()` source code for details. These settings can still be change inside `dwc_ddrphy_phyinit_setDefault()` if desired.
  - A detailed description of each field in the message block can be found in the `mnPmuSramMsgBlock_lpddr4.h` file in the firmware release folder. This file is included in the protocol folder of the firmware package.

In addition to editing `dwc_ddrphy_phyinit_setDefault()` file the user has the option to customize the function `dwc_ddrphy_phyinit_userCustom_overrideUserInput()` to dynamically override any value set in `dwc_ddrphy_phyinit_setDefault()`. Please see example `examples/simple/dwc_ddrphy_phyinit_userCustom_overrideUserInput.c` for implementation of this function.

DRAM protocol lpddr4, revision A-2019.06-BETA



## 4.2 (B) Specify Custom Behavior (Optional)

Behavior of PhyInit can be overridden using the userCustom() functions described in the documentation. These overrides can be either before or after training has been completed:

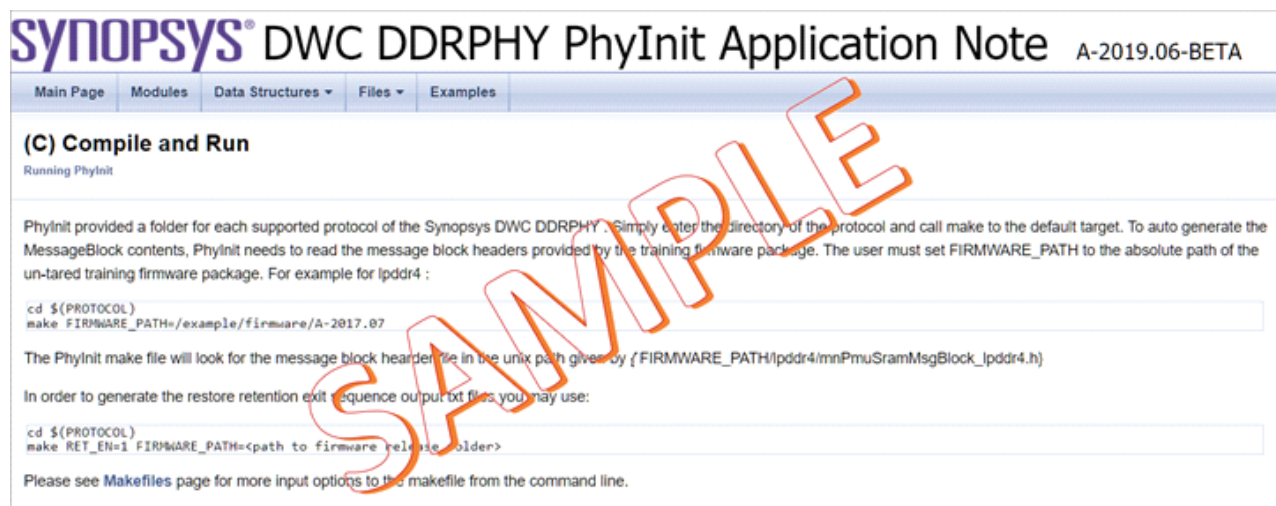
- **dwc\_ddrphy\_phyinit\_userCustom\_customPreTrain():** This function is called before training firmware is executed. Any register override in this function might affect the firmware training results. Technology specific register programming can be done here.
- **dwc\_ddrphy\_phyinit\_userCustom\_customPreTrainPsLoop():** This function is called for each PState, before training firmware is executed. Any per-PState register override in this function might affect the firmware training results.
- **dwc\_ddrphy\_phyinit\_userCustom\_customPostTrain():** This function is called after the execution of training firmware is complete. The user can use this function to override any CSR value programmed by PhyInit or training firmware. For further examples see related document section below.
- **dwc\_ddrphy\_phyinit\_userCustom\_customPreTrainPsLoop():** This function is called for each PState, after training firmware is executed. Any per-PState register override meant to change a CSR value programmed by PhyInit or training firmware can be done at this moment.

For details and examples see HTML documentation section.

## 4.3 (C) Compile and Run

A makefile is provided to compile PhyInit code and execute the object to generate the initialization sequence. Further instructions are provided in the pages referred in the HTML documentation in the release package.

Figure 4-3 Compile and Run Page



**Figure 4-4** PhyInit Makefile Documentation Page

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## Makefiles

### Overview

A Makefile is provided for each protocol in the corresponding folder. This file contains the recipes for compiling source code and executing the final binary to generate output text files. The table below lists all the optional variable and targets available in the Makefile.

Table 1 PhyInit Makefile Variables

Variable	Req/Opt	Description
FIRMWARE_PATH	Required	Set to absolute unix path to the extracted firmware release package
DEBUG	Optional	Print additional debug information in the output txt file 1:Enable, other values:Disable (default)
RET_EN	Optional	Creates the retention exit sequence output.txt file in addition to other output txt files. 1:Enable, other values:Disable(default)

**Note**  
For examples on makefile command lines see (C) Compile and Run

Table 2 PhyInit Makefile Targets

Target	Description
clean	Cleans all the built files
link	Checks FIRMWARE_PATH is set correctly or not
compile	Creates the PhyInit executable for a specified protocol.
run	Creates the all various txt files in the protocol output folder.
print_obj	Prints list of object files created for a specified protocol.
print_custobj	Prints list of object files created for customer-editable source code.
print_hdr	Prints list of header files used for a specified protocol.
print_func	Prints list of function files used for a specified protocol.
print_custfunc	Prints a list of customer editable functions for a specified protocol.

### PhyInit Executable

The PhyInit executable is created in the object folder for each protocol. The Makefile generates and uses this binary to create output texts files for each initialization sequence. For example and usage see documentation for `main()` function.

DRAM protocol lpddr4, revision A-2019.06-BETA

## 4.4 (D) Reading PhyInit Outputs

The output text files for each protocol are placed in an output folder. Depending on the Makefile parameters, a number of output sequences are generated. Details on the usage and intention is provided further in the HTML documentation as shown below.

Figure 4-5 Reading Outputs Page

**SYNOPSYS®**
**DWC DDRPHY PhyInit Application Note**
A-2019.06-BETA

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Examples

### (D) Reading Phynit Outputs

Running Phynit

The output text files for each protocol are placed in `lpddr4/output`. For each protocol, multiple text files are created:

1. `dwc_ddrphy_phyinit_out_lpddr4_skiptrain.txt`
  - this file contains the PHY initialization sequence for skipping training firmware. This is useful for shortening simulation time.
2. `dwc_ddrphy_phyinit_out_lpddr4_train1d.txt`
  - this file contains the PHY initialization sequence which runs 1D training firmware.
3. `dwc_ddrphy_phyinit_out_lpddr4_train1d2d.txt`
  - applicable only for ddr4, ddr4\_rdimm, ddr4\_lrdimm and lpddr4, this file contains the PHY initialization sequence which runs 1D and 2D training firmware.
4. `dwc_ddrphy_phyinit_out_lpddr4_devinit_skiptrain.txt`
  - this file contains the PHY initialization sequence for skipping training but executing the Training firmware for the purpose of initializing the DRAM device. This is useful for shortening simulation time.
5. `dwc_ddrphy_phyinit_out_lpddr4_*_retention_exit.txt`
  - if makefile parameter `RET_EN` is set, for each of the text files in 1-4 and additional file with `*_retention_exit` is created. This file contains the IO restore retention exit sequence. see [IO Retention Save/Restore](#) for more information.

Each text file contains all the APB write commands needed to initialize the PHY along with comment descriptions. The APB write commands are expressed as `dwc_ddrphy_apb_wr(address, data)` function calls.

For steps where actions other than APB writes are required, a function call with associated comments will be printed. For example, function call to `dwc_ddrphy_phyinit_userCustom_E_setDfciClk()` will be printed for Step E and can potentially be used as a trigger event in the user environment to change the DfciClk frequency for the specified PState.

The output text files are compatible with Verilog syntax. Users can include the text file in their testbench if they provide definition of these functions:

- `dwc_ddrphy_phyinit_userCustom_A_bringup?`
- `dwc_ddrphy_phyinit_userCustom_B_startClockResetPhy()`
- `dwc_ddrphy_phyinit_userCustom_customPreTrain()`
- `dwc_ddrphy_phyinit_userCustom_customPostTrain()`
- `dwc_ddrphy_phyinit_userCustom_E_setDfciClk()`
- `dwc_ddrphy_phyinit_userCustom_G_waitFwDone()`
- `dwc_ddrphy_phyinit_userCustom_H_readMsgBlock()`
- `dwc_ddrphy_phyinit_userCustom_io_write16()`
- `dwc_ddrphy_phyinit_userCustom_io_read16()`
- `dwc_ddrphy_phyinit_userCustom_J_enterMissionMode()`
- `dwc_ddrphy_phyinit_userCustom_overrideUserInput()`
- `dwc_ddrphy_phyinit_userCustom_saveRetRegs()`
- `dwc_ddrphy_phyinit_print()`
- `dwc_ddrphy_phyinit_cmnt()`
- `dwc_ddrphy_phyinit_assert()`

DRAM protocol lpddr4, revision A-2019.06-BETA



# 5

## Synopsys Support

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### 5.1 PhyInit Support and Debugging

A default configuration is provided to help run PHYInit for the first time and generate the desired txt file.

While PHYInit and the training firmware are tested in our environment, errors may occur due to unforeseen configurations and conditions. If you are experiencing issues, you may wish to contact Customer Support. The quickest and most efficient way is to open a SolvNet ticket, however, you may also email [support\\_center@synopsys.com](mailto:support_center@synopsys.com).

When requesting support, you will need to provide the following logs:

- PhyInit output.txt
- PhyInit release revision
- Training Firmware release revision
- Training Firmware log

