Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

OneNAND Flash
Palladium Memory Model
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

OneNAND Flash Palladium Memory Models

1. Introduction

The Cadence Palladium OneNAND Flash Models are based on data sheet specifications from Samsung.

The models are available in several configurations with model sizes to match real devices manufactured by both Samsung and Toshiba.

Currently only a few different sizes are available, please consult the memory model catalog for the latest complete list of available models.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

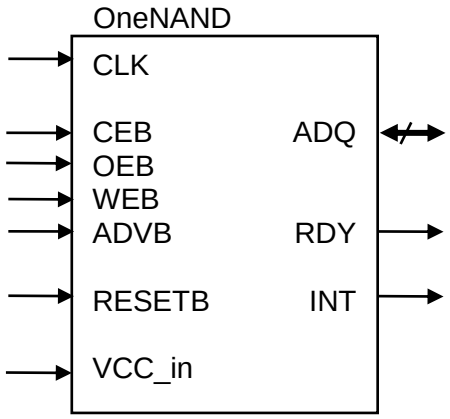
Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations

The following tables list the configurations specified in the four data sheets listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Model	Vendor	Density	Sector Size	Sectors per Page	Pages per Block	Blocks
KFM1216Q2M	**Samsung**	**512Mb**	**512B + 16B**	**4**	**64**	**512**
TC58RYM9S8E	**Toshiba**	**512Mb**	**512B + 16B**	**4**	**64**	**512**
KFM1G16Q2M	**Samsung**	**1Gb**	**512B + 16B**	**4**	**64**	**1024**
KFM2G16Q2M	**Samsung**	**2Gb**	**512B + 16B**	**4**	**64**	**2048**
KFM4G16Q4M	**Samsung**	**4Gb**	**512B + 16B**	**8**	**64**	**2048**
KFM8G16Q5M	**Samsung**	**8Gb**	**512B + 16B**	**8**	**64**	**4096**

4. Model Block Diagram



5. Command Support

The following table shows the commands that are supported in the OneNAND Flash Palladium model. The commands vary from part to part and not all commands are supported in each model.

OneNAND Commands

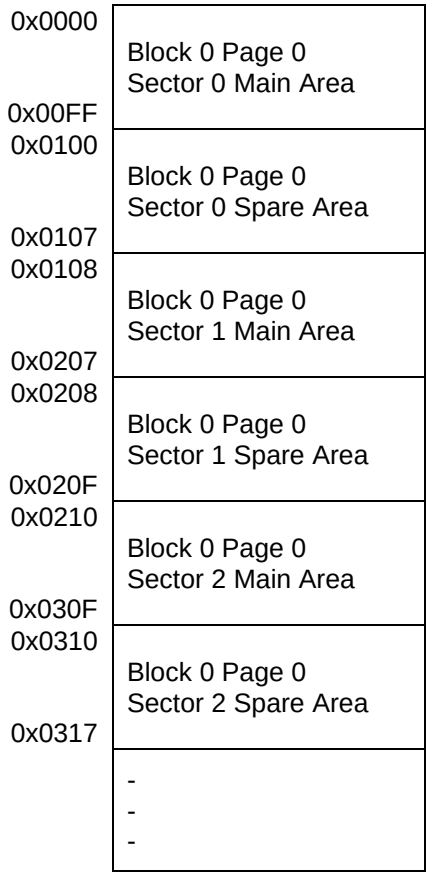
		Samsung					Toshiba
Part		KFM8G16Q5M	KFM4G16Q4M	KFM2G16Q2M	KFM1G16Q2M	KFM1216Q2M	TC58RYM9S8E
Code	Command						
0x00	Load Main						
0x13	Load Spare						
0x23	Unlock block						
0x2A	Lock block						
0x2C	Tight lock block						
0x27	All block Unlock						
0x80	Prog Main						
0x1A	Prog Spare						
0x94	Block Erase						
0x95	Multi Block Erase						
0xB0	Erase Suspend						
0x30	Erase Resume						
0x71	Erase Verify Read						
0x7D	2X Prog						
0x7E	2X Dump						
0x7F	Cache Prog						
0x03	Superload						
0x1B	Copyback						
0x0E	Cache Read						
0x0C	Cache Read Finish						
0x0A	Sync Burst Block Read						
0xF3	Reset						

Cmd Supported in Pd model
Cmd Not Supported in Pd model
Cmd not available for this part

6. Address mapping

The array of the OneNAND Flash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The main array in the OneNAND model is called int_mem_array. This is a 16bit data width array.

Addressing of the internal array is based on pages including spare area as shown below.



7. Boot Sequence

In order to model the Boot sequence correctly an additional pin is provided on the model, VCC_in. This pin is used to model the power up event. If the model sees a low to high transition on this pin it causes the BootRAM to be loaded with the contents of the First page of the first block of the array.

If the boot sequence does not need to be modeled in the Palladium environment then the VCC_in pin needs to be tied high.

The runtime sequence requires the user to preload the main array with the boot code in the first two sectors of the first page in the first block as per the Samsung specification.

8. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compilation. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64 +sv -ua +dut+<model_name>\
    ./<model_name>.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis:

```
1)
hdlInputFile <model_name>.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog <model_name>.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
<model_name>
……

2)
vavlog <model_name>.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog <model_name>.vg
<model_name>
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations which are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

9. Model Size

To reduce memory utilization the model only has 256 blocks but the actual device sizes vary from 512 to 4096 blocks. If a larger size is needed please contact Cadence Customer Support.

10. Limitations

1. OTP features and commands are not supported.
2. DQ6 Toggle functionality is not supported.
3. ECC operations and commands are not supported.
4. Status register F240 always returns a zero.
5. Model does not check illegal sequence of command cycles.
6. Model does not check for attempts to program a bit to 1, user should make sure the block is erased before program.

Revision History

The following table shows the revision history for this document

Date	Version	Revision
February 2011	1.0	Initial version
June 2011	1.1	Updated with “Related Documents” information
July 2014	1.3	Repaired doc title property. Added revision history. Updated legal.
September 2014	1.4	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.5	Remove emulation capacity info. Update related publications list.
July 2015	1.6	Update Cadence naming on front page
January	1.7	Update for Palladium-Z1 and VXE
July 2016	1.8	Remove hyphen in Palladium naming
January 2018	1.9	Modify header and footer
July 2018	2.0	Update for new utility library