Automotive LPDDR5 SDRAM

MT62F512M64D4, MT62F1G64D8

Features

- **Architecture**
  - 12.8 GB/s maximum bandwidth per channel
  - Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR
- **LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - 4KB page size with 8-bank (8B mode), 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Link protection (link ECC) support
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.8V NOM
  - V_{DD2H} = 1.01–1.12V; 1.05V NOM
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V NOM
  - V_{DDQ} = 0.5V NOM or 0.3V NOM (ODT off)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK, and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
• LPDDR5 V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}: 1.8V/1.05V/0.9V/0.5V	MT62F
• Array configuration	
– 512 Meg x 64 (4 channels x16 I/O)	512M64
– 1 Gig x 64 (4 channels x16 I/O)	1G64
• Device configuration	
– 4 die in package	D4[1]
– 8 die in package	D8
• FBGA "green" package	
– 441-ball TFBGA (14.0mm × 14.0mm, seated height: 1.1mm MAX, Ø0.42 SMD)	EK
• Speed grade, cycle time (^{t}WCK)	
– 6400 Mb/s	-031
• Functional Safety (FuSa)	F[2]
– Micron HW-Evaluated (ISO 26262-8:2018, cl. 13)	
– FMEDA (ISO 26262-5:2018, cl. 8, 9)	
– External assessment report	
– Suitable for systems up to ASIL D	
• Automotive grade	A
– AEC-Q100	
– PPAP	
• Operating temperature:	
– –40°C ≤ T_C ≤ +95°C	IT
– –40°C ≤ T_C ≤ +105°C	AT
– –40°C ≤ T_C ≤ +125°C	UT[3]
• Revision	:B

Notes:
1. Preliminary status: Products and specifications herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted to meet Micron's production data sheet specifications.
2. For functional safety documentation, contact Micron sales representative.
3. Based on automotive usage model. Contact Micron sales representative with questions.

Part Number Ordering Information

Figure 1: Part Number Chart

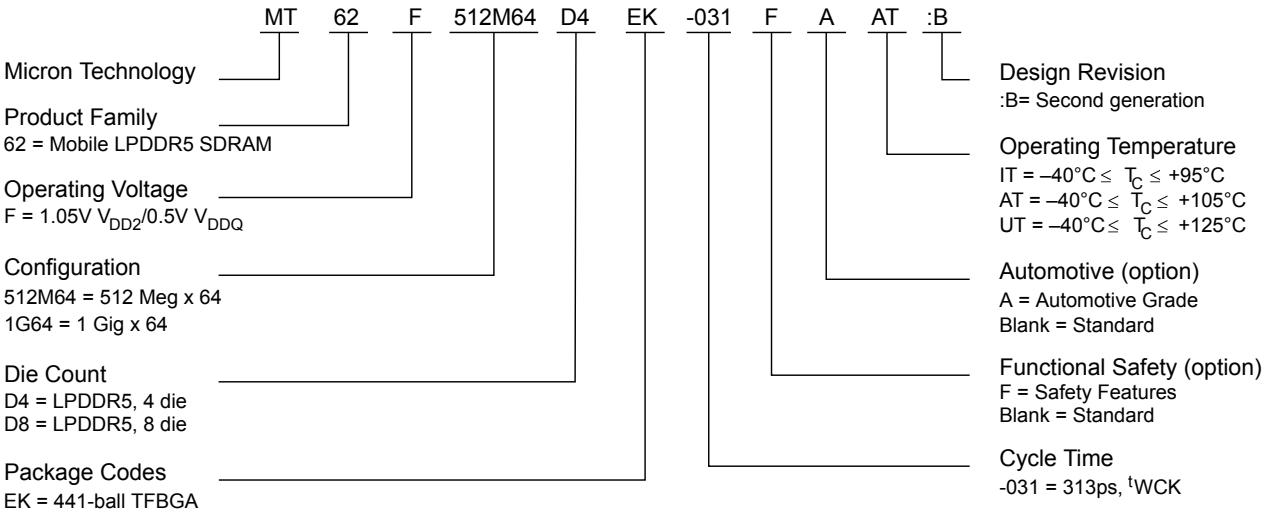

Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F512M64D4EK-031 AIT:B	4GB (32Gb)	6400 Mb/s
MT62F512M64D4EK-031 AAT:B	4GB (32Gb)	6400 Mb/s
MT62F512M64D4EK-031 AUT:B	4GB (32Gb)	6400 Mb/s
MT62F512M64D4EK-031 FAAT:B	4GB (32Gb)	6400 Mb/s
MT62F1G64D8EK-031 AIT:B	8GB (64Gb)	6400 Mb/s
MT62F1G64D8EK-031 AAT:B	8GB (64Gb)	6400 Mb/s
MT62F1G64D8EK-031 AUT:B	8GB (64Gb)	6400 Mb/s
MT62F1G64D8EK-031 FAAT:B	8GB (64Gb)	6400 Mb/s

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5 Data Sheet List

This data sheet only describes the product specifications that are unique to the Micron devices listed in Table 1.

For general LPDDR5 specifications, please refer to the data sheets below.

- General LPDDR5 Specifications 1: Mode Registers
- General LPDDR5 Specifications 2: AC/DC and Interface Specifications
- General LPDDR5 Specifications 3: Features and Functionalities

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Functional Safety Notes

This automotive LPDDR5 DRAM product family has been HW evaluated as outlined by ISO 26262-8:2018, clause 13. The HW evaluation was certified by an external assessor to provide a level of systematic fault coverage that allows its use in systems targeting up to ASIL D compliance.

This LPDDR5 DRAM contains several new functional safety (FuSa) features that operate within the JEDEC LPDDR5 protocols (commands, timings, and so forth). The specification addendum governing these FuSa features is available under NDA. This LPDDR5 DRAM may operate as a standard LPDDR5 DRAM only, or as a standard LPDDR5 DRAM with the additional functional safety features for substantially improved random hardware fault metrics. Contact a Micron sales representative to initiate the process required to obtain the specification addendum.

Device Configuration

Table 2: Die Organization in the Package

Die Organization	512M64 (32 Gb/package)	1G64 (64 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	512M64 (32 Gb/package)/1G64 (64 Gb/package)		
Density per die	8Gb		
Bits	8,589,934,592		
Bank mode	BG mode	16B mode	8B mode
Configuration	32Mb × 16 DQ × 4 banks × 4BG	32Mb × 16 DQ × 16 banks	64Mb × 16 DQ × 8 banks
Number of banks	4	16	8
Number of bank groups	4	1	1
Array prefetch bits	256	256	512
Rows per bank	32,768		
Columns	64		
Page size (bytes)	2048	2048	4096
Native burst length	16	16	32
Number of I/Os	16		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–
Row address	R[14:0]		
Column address	C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit		

Notes: 1. Refer to the SDRAM Addressing section in General LPDDR5 Specifications 3.
2. Refer to the Speed Grades and Effective Burst Length in General LPDDR5 Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

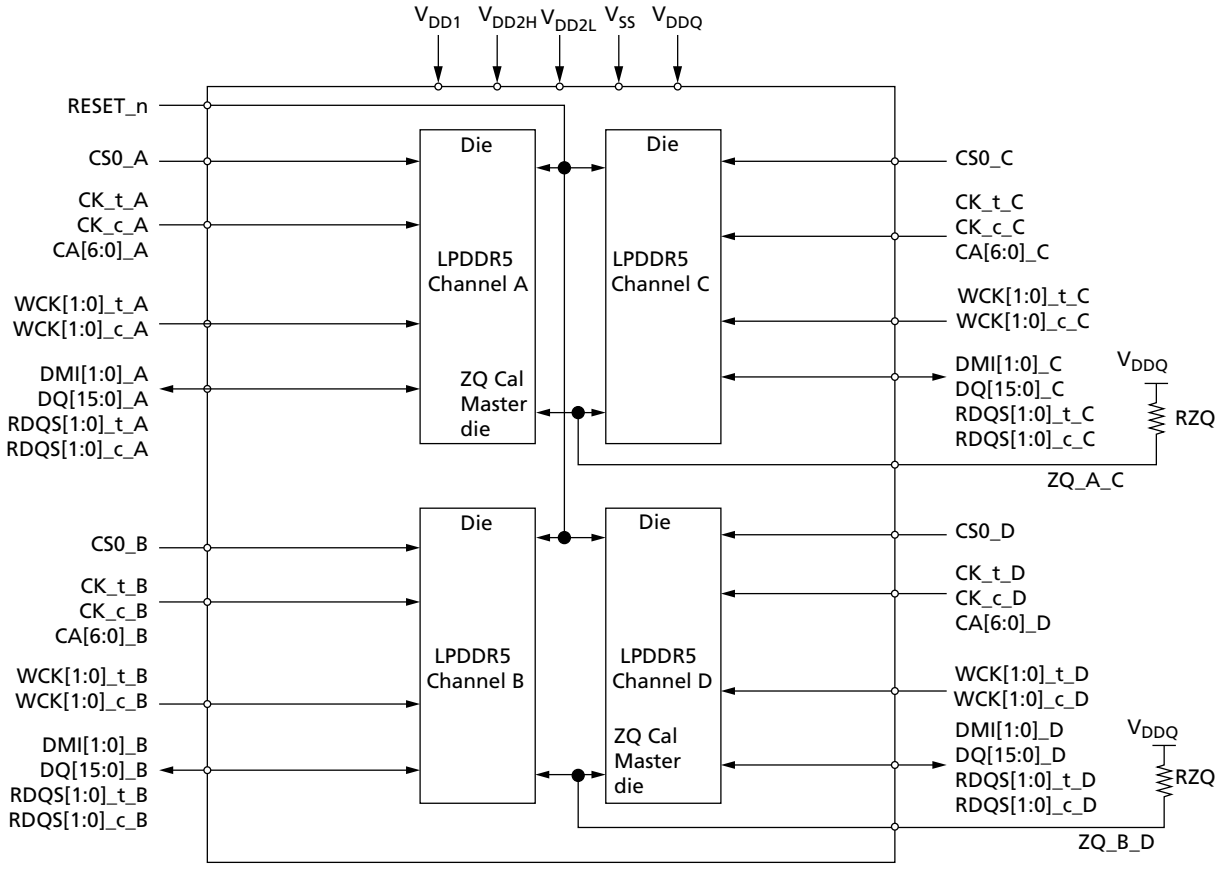
Parameter	Symbol	8Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	210	210	ns
REFRESH cycle time (per bank)	^{t}RFCpb	120	120	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5 Specifications 3 for all refresh parameters.

Package Block Diagrams

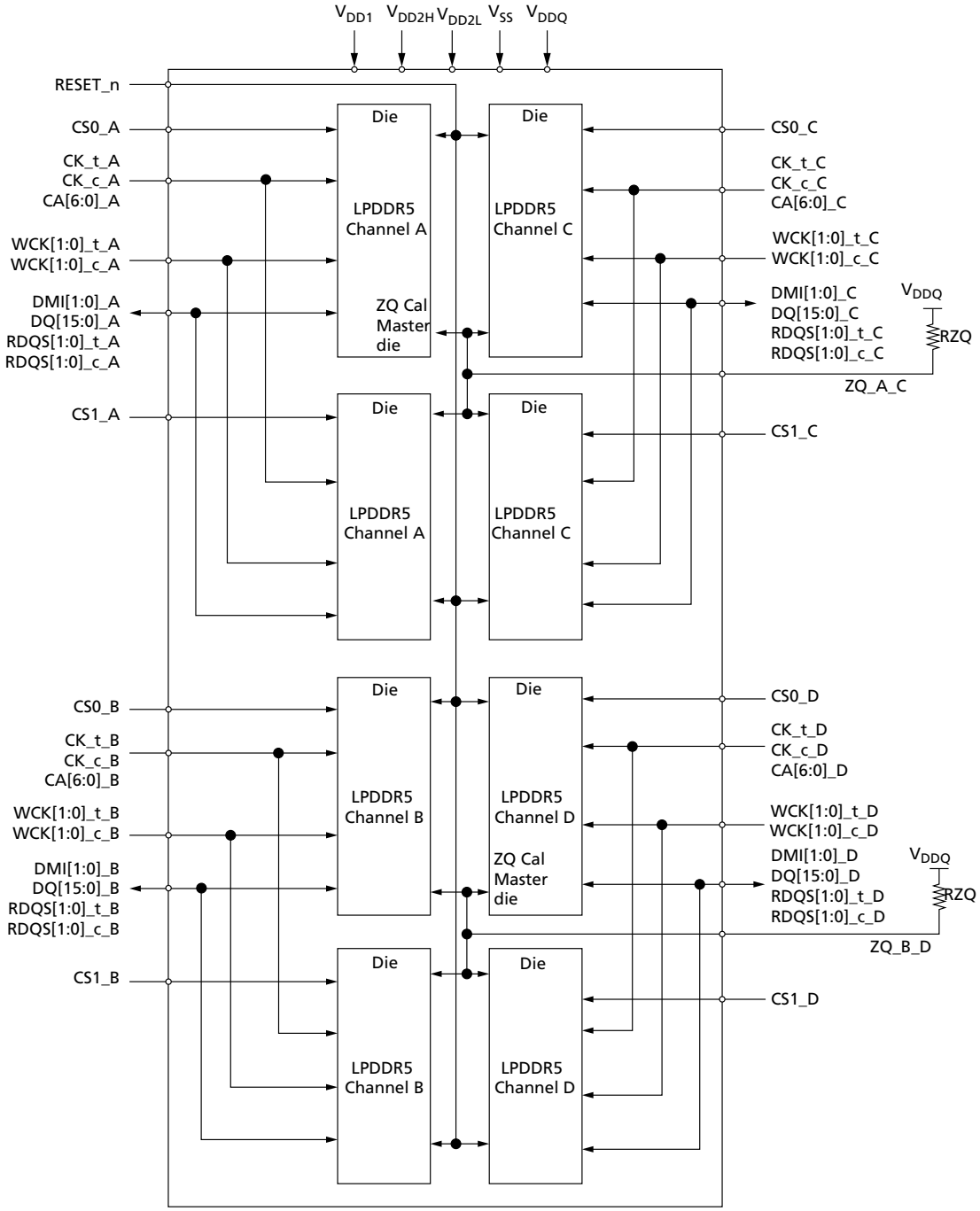
Quad Die, Quad Channel

Figure 2: Quad-Die, Quad-Channel Package Block Diagram



Eight Die, Quad Channel

Figure 3: Eight-Die, Quad-Channel Package Block Diagram



Ball Assignments and Descriptions

Figure 4: 441-Ball Quad-Channel FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	V_{SS}	V_{SS}	V_{DD1}	V_{DD2L}	V_{SS}	V_{DD2H}	V_{DD1}	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD1}	V_{DD2L}	V_{SS}	V_{DD2H}	V_{DD1}	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	A
B	V_{SS}	DQ0_A	V_{SS}	DQ3_A	V_{DD2H}	V_{SS}	DQ11_A	DQ9_A	DQ8_A	V_{SS}	V_{DD2H}	DQ0_C	V_{SS}	DQ3_C	V_{DD2H}	V_{SS}	DQ11_C	DQ9_C	DQ8_C	RFU	V_{SS}	B
C	V_{DD2H}	V_{SS}	DQ2_A	V_{DDQ}	CA0_A	V_{DD2H}	V_{SS}	DQ10_A	V_{DDQ}	V_{DD2H}	V_{SS}	V_{SS}	DQ2_C	V_{DDQ}	CA0_C	V_{DD2H}	V_{SS}	DQ10_C	V_{DDQ}	V_{DD2H}	V_{DD2H}	C
D	V_{SS}	DQ1_A	WCK0_c_A	V_{SS}	CA1_A	CS0_A	V_{DDQ}	V_{SS}	WCK1_t_A	V_{DD2H}	V_{DDQ}	DQ1_C	WCK0_c_C	V_{SS}	CA1_C	CS0_C	V_{DDQ}	V_{SS}	WCK1_t_C	V_{DDQ}	V_{SS}	D
E	V_{DDQ}	RDQS0_c_A	V_{SS}	WCK0_t_A	V_{SS}	CS1_A	V_{SS}	WCK1_c_A	DMI1_A	V_{SS}	V_{DDQ}	RDQS0_c_C	V_{SS}	WCK0_t_C	V_{SS}	CS1_C	V_{SS}	WCK1_c_C	DMI1_C	V_{SS}	V_{DD2H}	E
F	V_{DDQ}	RDQS0_t_A	V_{SS}	V_{DDQ}	V_{SS}	CA2_A	V_{SS}	RDQS1_t_A	V_{SS}	V_{DDQ}	V_{SS}	RDQS0_t_C	V_{SS}	V_{DDQ}	V_{SS}	CA2_C	V_{SS}	RDQS1_t_C	V_{SS}	V_{DDQ}	V_{DD2H}	F
G	V_{SS}	DQ4_A	V_{DDQ}	DMI0_A	RFU	RFU	CA6_A	V_{SS}	RDQS1_c_A	V_{SS}	V_{DDQ}	DMI0_C	V_{DDQ}	DQ4_C	RFU	RFU	CA6_C	V_{SS}	RDQS1_c_C	V_{SS}	V_{SS}	G
H	V_{DD2L}	V_{SS}	DQ5_A	V_{SS}	CK_t_A	V_{SS}	CA5_A	V_{DDQ}	V_{SS}	DQ12_A	V_{SS}	V_{SS}	DQ5_C	V_{SS}	CK_t_C	V_{SS}	CA5_C	V_{DDQ}	V_{SS}	DQ12_C	V_{DD2L}	H
J	V_{DD2H}	DQ6_A	DQ7_A	V_{DD2H}	V_{SS}	CK_c_A	V_{SS}	DQ14_A	DQ13_A	V_{SS}	V_{DD2L}	DQ6_C	DQ7_C	V_{DD2L}	ZQ_A_C	CK_c_C	V_{SS}	DQ14_C	DQ13_C	V_{SS}	V_{DD2H}	J
K	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	CA3_A	CA4_A	V_{DD2L}	V_{SS}	DQ15_A	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	CA3_C	CA4_C	V_{DD2H}	V_{SS}	DQ15_C	V_{SS}	K
L	V_{DD2H}	V_{DD2L}	V_{DD2L}	V_{DD2H}	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	V_{DD2H}	V_{DD2L}	V_{DD2L}	V_{DD2H}	L
M	V_{SS}	DQ15_B	V_{SS}	V_{DD2H}	CA4_B	CA3_B	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	DQ15_D	V_{SS}	V_{DD2L}	CA4_D	CA3_D	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	M
N	V_{DD2H}	V_{SS}	DQ13_B	DQ14_B	V_{SS}	CK_c_B	ZQ_B_D	V_{DD2L}	DQ7_B	DQ6_B	V_{DD2L}	V_{SS}	DQ13_D	DQ14_D	V_{SS}	CK_c_D	V_{SS}	V_{DD2H}	DQ7_D	DQ6_D	V_{DD2H}	N
P	V_{DD2L}	DQ12_B	V_{SS}	V_{DDQ}	CA5_B	V_{SS}	CK_t_B	V_{SS}	DQ5_B	V_{SS}	V_{SS}	DQ12_D	V_{SS}	V_{DDQ}	CA5_D	V_{SS}	CK_t_D	V_{SS}	DQ5_D	V_{SS}	V_{DD2L}	P
R	V_{SS}	V_{SS}	RDQS1_c_B	V_{SS}	CA6_B	RFU	RFU	DQ4_B	V_{DDQ}	DMI0_B	V_{DDQ}	V_{SS}	RDQS1_c_D	V_{SS}	CA6_D	RFU	RFU	DMI0_D	V_{DDQ}	DQ4_D	V_{SS}	R
T	V_{DD2H}	V_{DDQ}	V_{SS}	RDQS1_t_B	V_{SS}	CA2_B	V_{SS}	V_{DDQ}	V_{SS}	RDQS0_t_B	V_{SS}	V_{DDQ}	V_{SS}	RDQS1_t_D	V_{SS}	CA2_D	V_{SS}	V_{DDQ}	V_{SS}	RDQS0_t_D	V_{DDQ}	T
U	V_{DD2H}	V_{SS}	DMI1_B	WCK1_c_B	V_{SS}	CS1_B	V_{SS}	WCK0_t_B	V_{SS}	RDQS0_c_B	V_{DDQ}	V_{SS}	DMI1_D	WCK1_c_D	V_{SS}	CS1_D	V_{SS}	WCK0_t_D	V_{SS}	RDQS0_c_D	V_{DDQ}	U
V	V_{SS}	V_{DDQ}	WCK1_t_B	V_{SS}	V_{DDQ}	CS0_B	CA1_B	V_{SS}	WCK0_c_B	DQ1_B	V_{DDQ}	V_{DD2H}	WCK1_t_D	V_{SS}	V_{DDQ}	CS0_D	CA1_D	V_{SS}	WCK0_c_D	DQ1_D	V_{SS}	V
W	V_{DD2H}	V_{DD2H}	V_{DDQ}	DQ10_B	V_{SS}	V_{DD2H}	CA0_B	V_{DDQ}	DQ2_B	V_{SS}	V_{SS}	V_{DD2H}	V_{DDQ}	DQ10_D	V_{SS}	V_{DD2H}	CA0_D	V_{DDQ}	DQ2_D	V_{SS}	V_{DD2H}	W
Y	V_{SS}	RESET_N	DQ8_B	DQ9_B	DQ11_B	V_{SS}	V_{DD2H}	DQ3_B	V_{SS}	DQ0_B	V_{DD2H}	V_{SS}	DQ8_D	DQ9_D	DQ11_D	V_{SS}	V_{DD2H}	DQ3_D	V_{SS}	DQ0_D	V_{SS}	Y
AA	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	V_{DD1}	V_{DD2H}	V_{SS}	V_{DD2L}	V_{DD1}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	V_{DD1}	V_{DD2H}	V_{SS}	V_{DD2L}	V_{DD1}	V_{SS}	V_{SS}	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Top View (ball down)

V_{SS} V_{DD1} V_{DD2H} V_{DD2L} V_{DDQ} CK RDQS WCK DQ, DMI CA, CS, ZQ, RESET NC

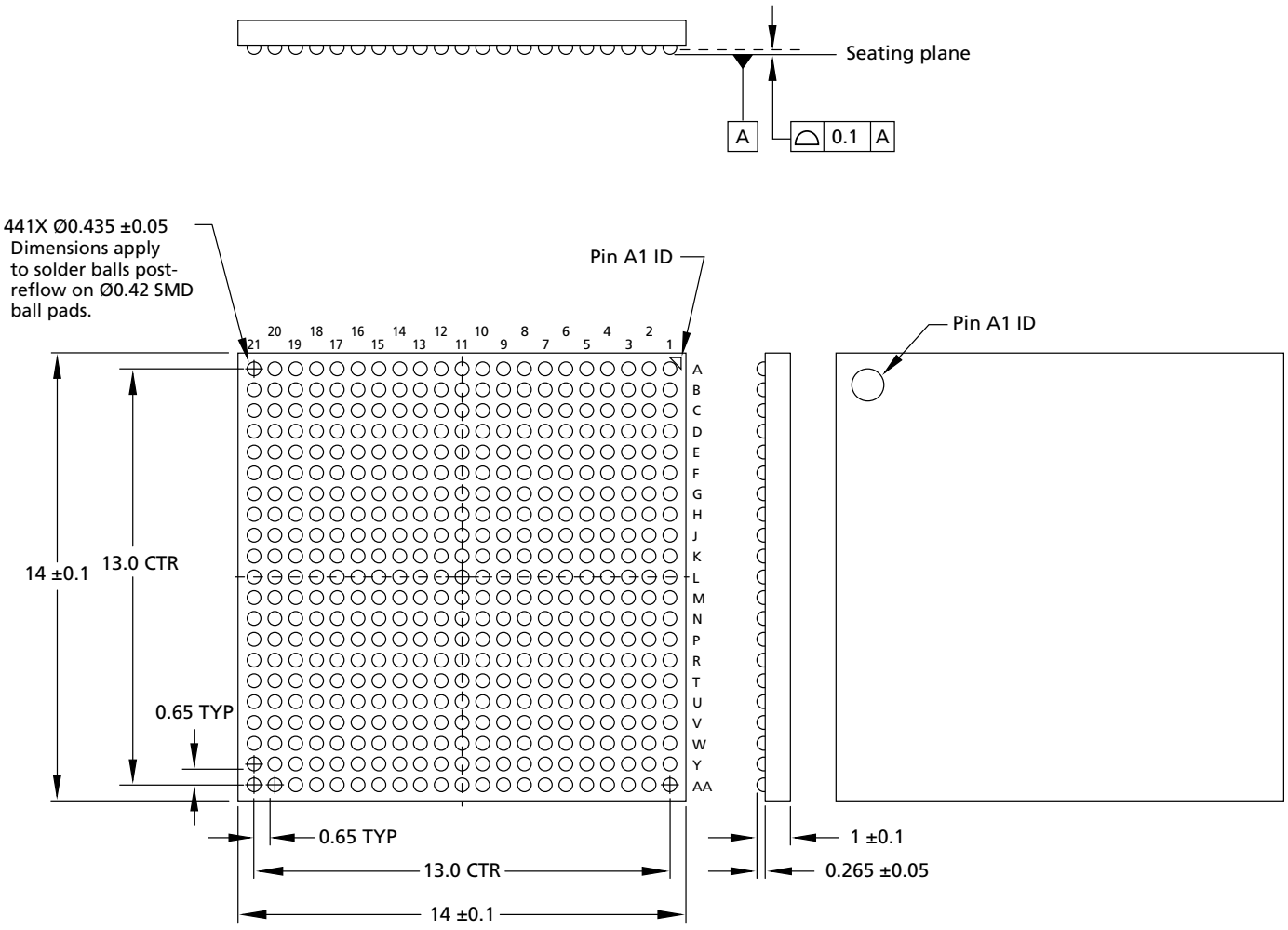
Table 5: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Package Dimensions

441-Ball Package (Package Code: EK)

Figure 5: 441-Ball TFBGA – 14.0mm x 14.0mm x 1.1mm (Package Code: EK)



Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni).

Product-Specific Mode Register Definition

Table 6: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
MR5	**Manufacturer ID**							
	1111 1111b : Micron							
MR6	**Revision ID1**							
	0000 0110b							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16		OP[5:2] = 0100b: 8Gb					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	**RECC**		**WECC**					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 3)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 3)							
MR24	**DFES**							
	OP[7] = 1b: DFE is supported							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							

Table 6: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27								**RFM**
	OP[0] = 0b: RFM not required							
MR43		**SBEC Rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							

Notes:
1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5 Specification 1 for mode registers not described here.
3. Write link ECC and read link ECC are supported.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5 Specifications 2 for detailed conditions.

Table 7: I_{DD} Parameters – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V;

Notes 1 and 2 apply to entire table.

Symbol	Supply	6400 Mb/s			Unit	Note
		AIT	AAT	AUT		
I_{DD01}	V_{DD1}	2.9	2.9	3.5	mA	
I_{DD02H}	V_{DD2H}	45.0	45.0	58.0		
I_{DD02L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD0Q}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2P1}	V_{DD1}	1.3	1.3	1.5	mA	
I_{DD2P2H}	V_{DD2H}	2.5	2.5	3.1		
I_{DD2P2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD2PQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2PS1}	V_{DD1}	1.3	1.3	1.5	mA	
$I_{DD2PS2H}$	V_{DD2H}	2.5	2.5	3.1		
$I_{DD2PS2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD2PSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2N1}	V_{DD1}	1.3	1.3	1.5	mA	
I_{DD2N2H}	V_{DD2H}	30.0	30.0	50.0		
I_{DD2N2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD2NQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2NS1}	V_{DD1}	1.3	1.3	1.5	mA	
$I_{DD2NS2H}$	V_{DD2H}	30.0	30.0	50.0		
$I_{DD2NS2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD2NSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3P1}	V_{DD1}	1.5	1.5	1.9	mA	
I_{DD3P2H}	V_{DD2H}	8.4	8.4	12.0		
I_{DD3P2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD3PQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3PS1}	V_{DD1}	1.5	1.5	1.9	mA	
$I_{DD3PS2H}$	V_{DD2H}	8.4	8.4	12.0		
$I_{DD3PS2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD3PSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3N1}	V_{DD1}	1.9	1.9	2.3	mA	
I_{DD3N2H}	V_{DD2H}	39.0	39.0	50.0		
I_{DD3N2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD3NQ}	V_{DDQ}	0.75	0.75	0.75		

Table 7: I_{DD} Parameters – Single Die (Continued)

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V;

Notes 1 and 2 apply to entire table.

Symbol	Supply	6400 Mb/s			Unit	Note
		AIT	AAT	AUT		
I_{DD3NS1}	V_{DD1}	1.9	1.9	2.3	mA	
$I_{DD3NS2H}$	V_{DD2H}	39.0	39.0	50.0		
$I_{DD3NS2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD3NSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD4R1}	V_{DD1}	7.2	7.2	7.7	mA	3, 4
I_{DD4R2H}	V_{DD2H}	372	372	384		
I_{DD4R2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD4RQ}	V_{DDQ}	106	106	106		
I_{DD4W1}	V_{DD1}	6.2	6.2	6.7	mA	3
I_{DD4W2H}	V_{DD2H}	310	310	340		
I_{DD4W2L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD4WQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD51}	V_{DD1}	23.0	23.0	23.0	mA	
I_{DD52H}	V_{DD2H}	170	170	170		
I_{DD52L}	V_{DD2L}	0.25	0.25	0.25		
I_{DD5Q}	V_{DDQ}	0.75	0.75	0.75		
I_{DD5AB1}	V_{DD1}	2.2	2.2	2.6	mA	
$I_{DD5AB2H}$	V_{DD2H}	35.0	35.0	50.0		
$I_{DD5AB2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD5ABQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD5PB1}	V_{DD1}	2.2	2.2	2.6	mA	
$I_{DD5PB2H}$	V_{DD2H}	35.0	35.0	50.0		
$I_{DD5PB2L}$	V_{DD2L}	0.25	0.25	0.25		
I_{DD5PBQ}	V_{DDQ}	0.75	0.75	0.75		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF, R_{ON} = 40 ohm, T_C = 25°C.

Table 8: Full-Array Power-Down Self Refresh Current/Deep-Sleep Mode Current – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V

Temperature	Symbol	Supply	Value	Unit
25°C	I_{DD61}	V_{DD1}	0.25	mA
	I_{DD62H}	V_{DD2H}	0.60	
	I_{DD62L}	V_{DD2L}	0.01	
	I_{DD6Q}	V_{DDQ}	0.01	
	I_{DD6DS1}	V_{DD1}	0.25	
	$I_{DD6DS2H}$	V_{DD2H}	0.60	
	$I_{DD6DS2L}$	V_{DD2L}	0.01	
	I_{DD6DSQ}	V_{DDQ}	0.01	
95°C	I_{DD61}	V_{DD1}	3.6	
	I_{DD62H}	V_{DD2H}	14.5	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	
	I_{DD6DS1}	V_{DD1}	3.6	
	$I_{DD6DS2H}$	V_{DD2H}	14.5	
	$I_{DD6DS2L}$	V_{DD2L}	0.25	
	I_{DD6DSQ}	V_{DDQ}	0.75	
105°C	I_{DD61}	V_{DD1}	3.6	
	I_{DD62H}	V_{DD2H}	14.5	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	
	I_{DD6DS1}	V_{DD1}	3.6	
	$I_{DD6DS2H}$	V_{DD2H}	14.5	
	$I_{DD6DS2L}$	V_{DD2L}	0.25	
	I_{DD6DSQ}	V_{DDQ}	0.75	
125°C	I_{DD61}	V_{DD1}	5.6	
	I_{DD62H}	V_{DD2H}	30.0	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	
	I_{DD6DS1}	V_{DD1}	5.6	
	$I_{DD6DS2H}$	V_{DD2H}	30.0	
	$I_{DD6DS2L}$	V_{DD2L}	0.25	
	I_{DD6DSQ}	V_{DDQ}	0.75	

Notes:
1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}95°C, I_{DD6}105°C and I_{DD6}125°C are the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.

Revision History

Rev. E – 2/2021

- Updated legal status to Production of 8DP package
- Updated IDD6(Power Down) specification and added IDD6DS(Deep Sleep) specification up to 125°C
- Updated FuSa features
- Updated Automotive grade features
- Added Functional Safety Notes section
- Added again FuSa MPNs(MT62F512M64D4EK-031 FAAT:B, MT62F1G64D8EK-031 FAAT:B) in the Part Number List table

Rev. D – 10/2020

- Updated Operating Temperature in Features
- Removed FuSa MPNs from Part Number List table
- Added FuSa introduction in General Notes
- Updated Package Dimensions (Package Code: EK): Updated coplanarity from 0.08mm to 0.1mm; Updated standoff (ball height) from 0.3 ±0.05mm to 0.265 ±0.05mm
- Updated $I_{DD3PS2H}$ of AUT part from 8.4mA to 12.0mA

Rev. C – 7/2020

- Updated legal status to Preliminary
- Added I_{DD} Parameters
- Updated Micron part number with functional safety enabled option

Rev. B – 5/2020

- Corrected lower operating temperature from –45°C to –40°C for AIT/AAT/AUT.

Rev. A – 4/2020

- Initial release

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