Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

ONFI 3.0 Flash
Palladium Memory Model
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

ONFI 3.0 Flash Palladium Memory Models

1. Introduction

The Cadence Palladium ONFI 3.x-compliant Flash Models are based on data sheet specifications of the following Micron devices:

MT29F Flash memory with MLC technology (128Gb per die, ONFI 3.0, L85A)
MT29F Flash memory with MLC+ technology (128Gb per die, ONFI 3.0, L85C+)
MT29F Flash memory with MLC+ technology (64Gb per die, ONFI 3.0, L84C+)
MT29F Flash memory with MLC technology (128Gb per die, ONFI 3.2, L95B)
MT29F Flash memory with MLC+ technology (128Gb per die, ONFI 3.2, L95B+)

These models support asynchronous, synchronous NV-DDR, and synchronous NV-DDR2 I/O interfaces.

The models are available in several configurations with model sizes to match real devices manufactured by the following vendor: Micron.

Currently only a few different sizes are available, please consult the memory model catalog for the current available list.

Please note that the information in this user guide applies to both ONFI 3.0-compliant and ONFI 3.2-compliant models unless otherwise specified.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations

The following tables list the configurations specified in the data sheets listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Model (ONFI 3.0)	Density	Level	# of Die	# of CE#	# of R/B#	I/O	Interface
MT29F128G08CBCAB	128Gb	MLC	1	1	1	Common	Sync/Async
MT29F256G08CECAB	256Gb	MLC	2	2	2	Separate	Sync/Async
MT29F512G08CKCAB	512Gb	MLC	4	2	2	Separate	Sync/Async
MT29F512G08CMCAB	512Gb	MLC	4	4	4	Separate	Sync/Async
MT29F1024G08CUCAB	1024Gb	MLC	8	4	4	Separate	Sync/Async
MT29F128G08CBCBB	128Gb	MLC+	1	1	1	Common	Sync/Async
MT29F256G08CECBB	256Gb	MLC+	2	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CKCBB	512Gb	MLC+	4	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CMCBB	512Gb	MLC+	4	4	4	Sep – 2 CH	Sync/Async
MT29F1T08CTCBB	1Tb	MLC+	8	4	4	Sep – 4 CH	Sync/Async
MT29F1T08CUCBB	1Tb	MLC+	8	4	4	Sep – 2 CH	Sync/Async
MT29F2T08CVCBB	2Tb	MLC+	16	8	4	Sep – 4 CH	Sync/Async
MT29F1T08CQCBB	1Tb	MLC+	8	4	4	Sep - 4 CH	Sync/Async
MT29F2T08CTCBB	2Tb	MLC+	16	8	4	Sep – 2CH	Sync/Async
MT29F64G08CBCDB	64Gb	MLC+	1	1	1	Common	Sync/Async
MT29F128G08CECDB	128Gb	MLC+	2	2	2	Sep – 2 CH	Sync/Async
MT29F192G08CGCDB	192Gb	MLC+	3	3	3	Sep – 3 CH	Sync/Async
MT29F256G08CKCDB	256Gb	MLC+	4	2	2	Sep – 2 CH	Sync/Async
MT29F256G08CMCDB	256Gb	MLC+	4	4	4	Sep – 2 CH	Sync/Async
MT29F512G08CUCDB	512Gb	MLC+	8	4	4	Sep – 2 CH	Sync/Async
MT29F1T08CVCDB	1Tb	MLC+	16	8	4	Sep – 4 CH	Sync/Async

Model (ONFI 3.2)	Density	Level	# of Die	# of CE#	# of R/B#	I/O	Interface
MT29F128G08CBECB	128Gb	MLC	1	1	1	Common	Sync/Async
MT29F256G08CEECB	256Gb	MLC	2	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CKECB	512Gb	MLC	4	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CMECB	512Gb	MLC	4	4	4	Sep – 2 CH	Sync/Async
MT29F1T08CUECB	1Tb	MLC	8	4	4	Sep – 2 CH	Sync/Async
MT29F2T08CTECB	2Tb	MLC	16	8	4	Sep – 2 CH	Sync/Async
MT29F128G08CBCCB	128Gb	MLC+	1	1	1	Common	Sync/Async
MT29F256G08CECCB	256Gb	MLC+	2	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CKCCB	512Gb	MLC+	4	2	2	Sep – 2 CH	Sync/Async
MT29F512G08CMCCB	512Gb	MLC+	4	4	4	Sep – 2 CH	Sync/Async
MT29F512G08CLCCB	512Gb	MLC+	4	4	4	Sep - 4 CH	Sync/Async
MT29F1T08CQCCB	1Tb	MLC+	8	4	4	Sep – 4 CH	Sync/Async
MT29F1T08CUCCB	1Tb	MLC+	8	4	4	Sep – 2 CH	Sync/Async
MT29F2T08CTCCB	2Tb	MLC+	16	8	4	Sep – 2 CH	Sync/Async
MT29F2T08CVCCB	2Tb	MLC+	16	8	4	Sep – 4 CH	Sync/Async

Notes: MLC = 2bits/cell, 512 pages per block, 2K blocks per die
Separate I/O = 2 sets of pins
Separate I/O 2 CH = 2 sets of pins
Separate I/O 4 CH = 4 sets of pins
Common I/O = 1 set of pins
(pin set: ALE,CLE,DQ,DQS,RE#,WE#,WP#)
Die and LUN are used interchangeably
Target and CE# are used interchangeably
ONFI 3.0 models have 16KB (16384+1216 bytes) per page
ONFI 3.2 models have 16KB (16384+1872 bytes) per page
MLC+ models support SLC mode via Set Feature address 91h

4. Model Parameter Descriptions

The following table provides details on the user adjustable parameters for the Palladium ONFI 3.x Memory Model. These parameters may be modified when instantiating the model.

User Adjustable Parameter	Default Value	Description
nb	32	Number of blocks per LUN

The value of parameter nb is passed into the LUN core module's BLK_IN_MEMORY parameter. It specifies the number of blocks per LUN. This parameter can be adjusted when the model is instantiated by assigning a value to the nb parameter. The maximum value should limit the total address bits to 30. Total address bits = column address bits + page address bits + block address bits, as described in the vendor data sheet. For example, 16K page size requires 15 bits, 512 pages per block adds 9 bits, leaving only 6 bits or 64 blocks.

The following table provides some information about exposed parameters that are NOT user adjustable. On rare occasion the user may find one of these parameters needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

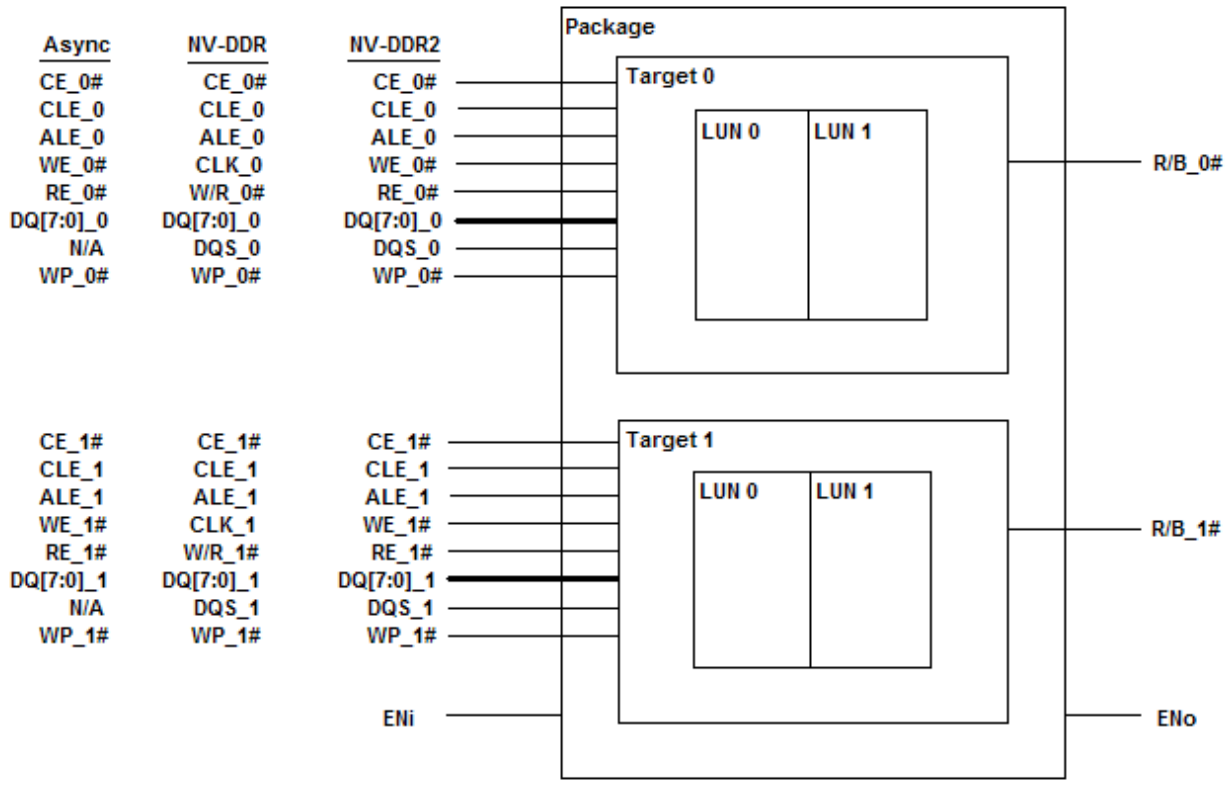
User Adjustable Parameter	Default Value	Description
data_bits	8	Width of DQ bus

The parameter data_bits should not be adjusted. It specifies the width for the DQ bus declaration.

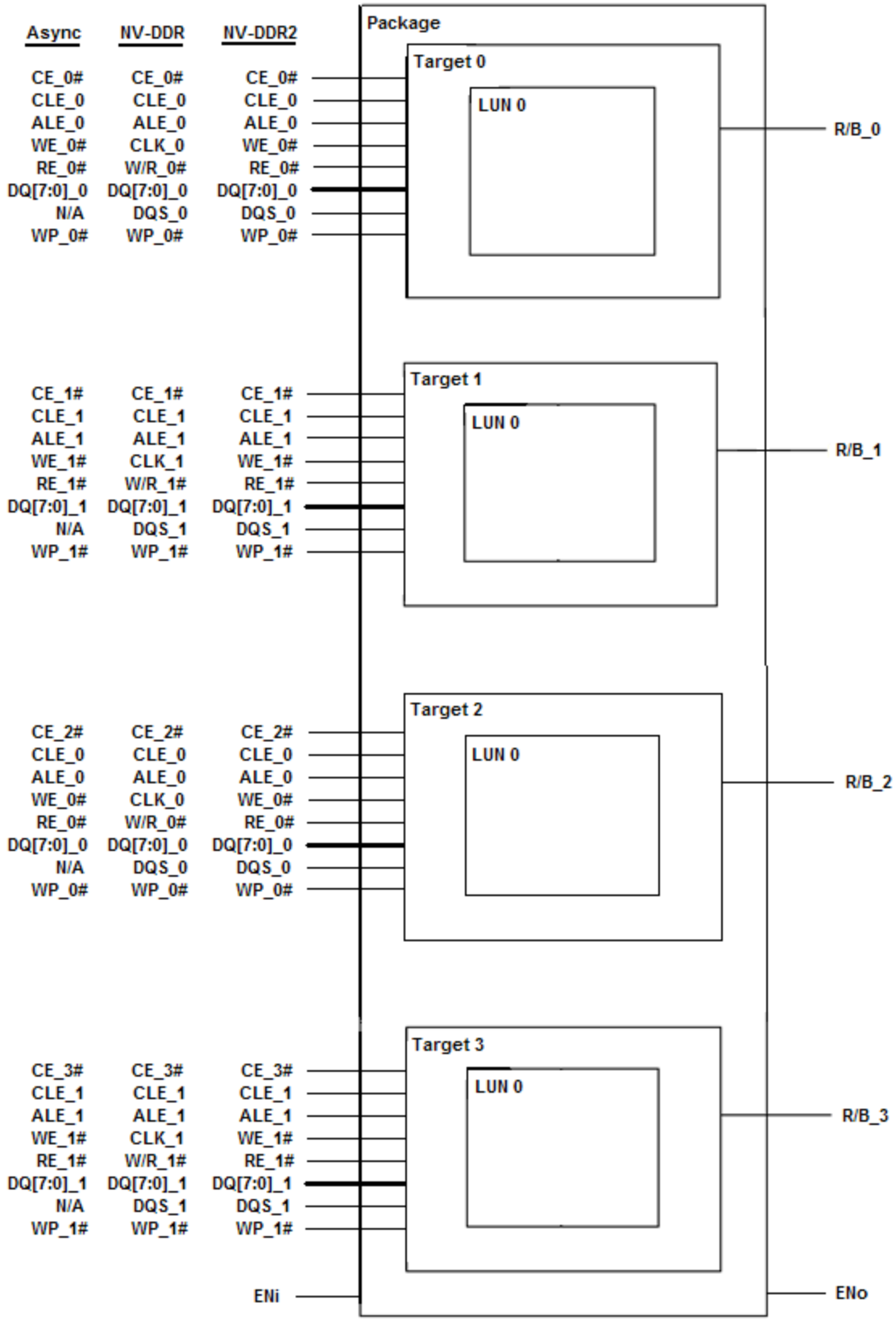
5. Model Block Diagram

These models are implemented modularly based on the LUN core, which is instantiated as many times as needed within each model. The user does not need to instantiate the core directly. The user instantiate the model based on the model's number of dies.

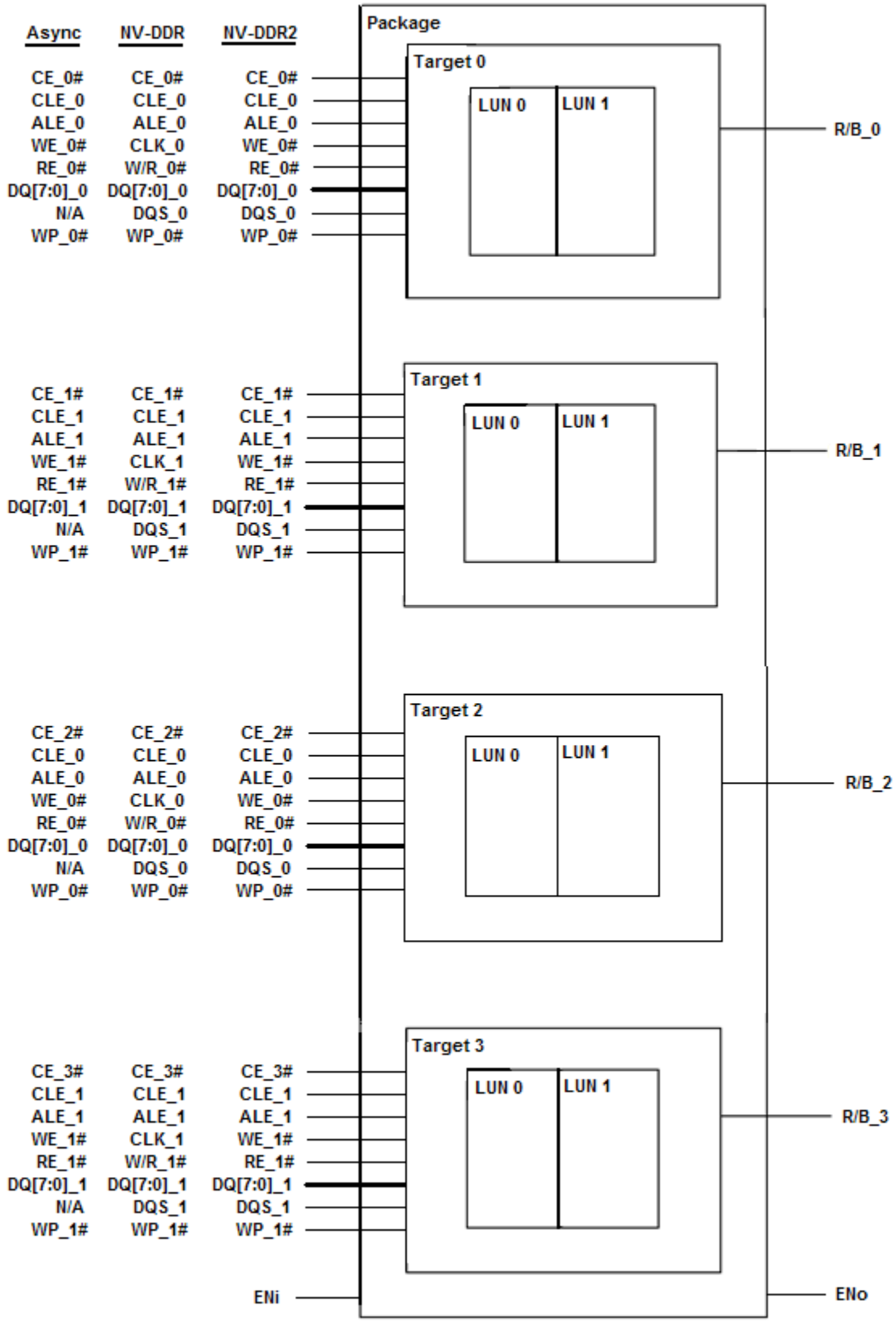
A block diagram of a model that has 4 dies or LUNs with 2 CE# is shown below.



The following block diagram shows a model that has 4 LUNs with 4 CE#.



The following block diagram shows a model that has 8 LUNs with 4 CE#.



Note that the optional pin/signal DQS_c is present but it is not required to be connected.

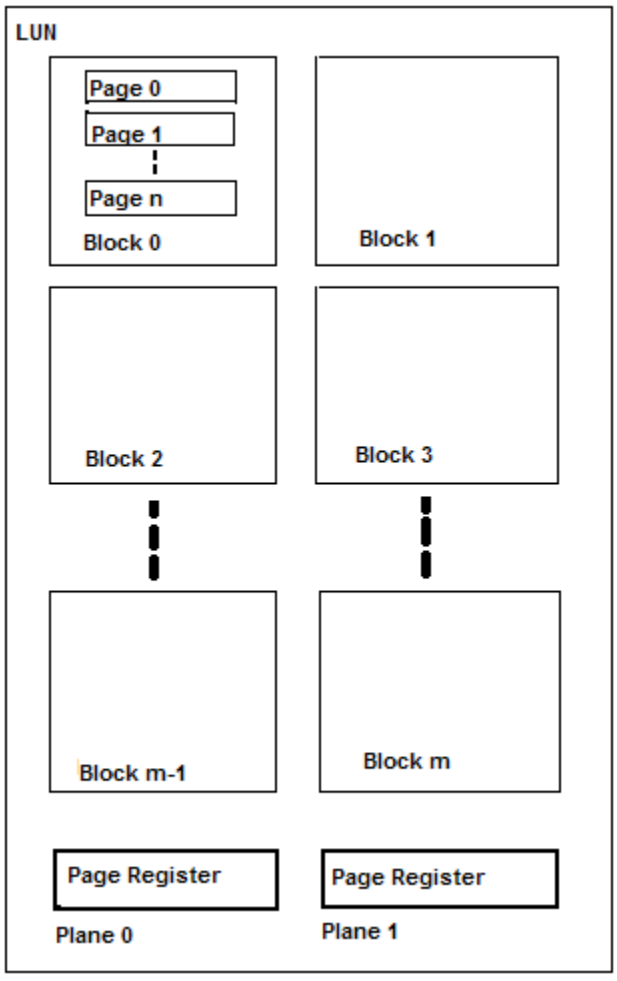
6. Address mapping

The array of the ONFI 3.x Flash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The mapping of lun, block, page and column addresses to the internal model array is as follows:

ARRAY_ADDR = { LA, BA, PA, CA}

This information is required if the memory needs to be preloaded with user data. Here are the array organization and addressing cycle table for MLC models.

Array Organization for MLC Array



1 page = (16K + 1216 bytes)

1 block = (16K + 1216) bytes x 512 pages
= (8192K + 608K) bytes

1 plane = (8192K + 608K) bytes x 1024 blocks
= 70,400Mb

1 LUN = 70,400Mb x 2 planes
= 140,800Mb

MLC Array Organization Per Logical Unit (LUN)

Address Cycle Table for MLC Array

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	CA14	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	PA8
Fifth	LOW	LOW	LOW	LA0	BA19	BA18	BA17	BA16

Notes from Micron data sheet:
CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

For ONFI 3.0 models column addresses 17,600 (44C0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

For ONFI 3.2 models column addresses 18,256 (4750h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

BA[9] is the plane-select bit:
Plane 0: BA[9] = 0
Plane 1: BA[9] = 1

LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.
LUN 0: LA0 = 0
LUN 1: LA0 = 1

MLC+ models have 48 extended blocks per LUN which requires one additional block address bit BA20, and shifts LA0 up one bit to DQ5 in the fifth address cycle.

7. Feature Address Definitions

In the data sheets there are up to 256 feature addresses defined – a 256 x 32 array. The Palladium models implement the entire array. However the only features that can be activated are the synchronous data interfaces and volume configuration. Other addresses can be written to and read back using the Set and Get Feature commands but the set features will not be active. For example timing mode change and OTP are not supported. The following table shows the feature address definitions as described in the Micron data sheet.

Feature Address	Definition
00h	Reserved
01h	Timing mode and Data interface
02h	NV-DDR2 configuration
03h-0Fh	Reserved
10h	Programmable output drive strength
11h-2Fh	Reserved
30h	Vpp
31h-57h	Reserved
58h	Volume configuration
59h-7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable R/B# pull-down strength
82h-88h	Reserved
89h	Read Retry
90h	Array Operation Mode
91h	SLC mode for MLC+ models
92h-FFh	Reserved

8. ID Operations

8.1. READ ID

The READ ID parameters for addresses 00h, 20h and 40h have been hardcoded into each model. Therefore user data file is not required.

8.2. READ PARAMETER PAGE

The data for the ONFI and JEDEC parameter pages are provided in the <model_name><package_code>_param.dat and <model_name><package_code>_jedec_param.dat files. The package_code is two characters. These data files should be preloaded into the model if the user wants to read ONFI and JEDEC information from the model. The LUN instance names are L<CE><LUN>. Using a model with 2 CEs and each CE has 2 LUNs as an example the paths to the parameter pages are as follows:

<path.to.model.inst>.L11.param_page
<path.to.model.inst>.L11.jedec_param_page
<path.to.model.inst>.L12.param_page
<path.to.model.inst>.L12.jedec_param_page
<path.to.model.inst>.L21.param_page
<path.to.model.inst>.L21.jedec_param_page
<path.to.model.inst>.L22.param_page
<path.to.model.inst>.L22.jedec_param_page

8.3. READ UNIQUE ID

The READ UNIQUE ID command is used to read a unique identifier programmed into the target. Preloading the uid_page is similar to preloading the param_page mentioned in the previous section. The path to each LUN's unique id page is as follows:

<path.to.model.inst>.L11.uid_page
<path.to.model.inst>.L12.uid_page
<path.to.model.inst>.L21.uid_page
<path.to.model.inst>.L22.uid_page

9. Features

The following table shows a list of features for the NAND flash model:

FEATURE	SUPPORT	NOTE
COMMANDS		
Reset	Yes	
Synchronous Reset	Yes	
Read ID	Yes	
Read Parameter Page (ONFI)	Yes	
Read Parameter Page (JEDEC)	Yes	
Read Unique ID	Yes	
Volume Select	Yes	
Get Features	Yes	
Set Features	Partial	Activate Synchronous Interface
Get Features by LUN	Yes	ONFI 3.2 models
Set Features by LUN	Partial	ONFI 3.2 models
Read Status	Yes	
Read Status Enhanced	Yes	
Change Read Column	Yes	
Change Read Column Enhanced (ONFI)	Yes	
Change Read Column Enhanced (JEDEC)	Yes	
Change Write Column	Yes	
Change Row Address	Yes	
Read Mode	Yes	
Read Page	Yes	
Read Page Multi-Plane	Yes	
Read Page Cache Sequential	Yes	
Read Page Cache Random	Yes	
Read Page Cache Last	Yes	
Program Page	Yes	
Program Page Multi-Plane	Yes	
Program Page Cache	Yes	
Erase Block	Yes	
Erase Block Multi-Plane (ONFI)	Yes	
Erase Block Multi-Plane (JEDEC)	Yes	
Copyback Read	Yes	
Copyback Program	Yes	
Copyback Program Multi-Plane	Yes	
Reset LUN	Yes	
SPECIAL OPERATIONS		
One-Time Programmable (OTP) Operations	No	
ODT Configure Operation	No	
Multi-Plane Operations	Yes	
Read Retry	No	
Interleaved Die (Multi-LUN) Operations	Yes	
Error Management	No	Spare area is available

The following table shows the command set as described in the Micron data sheet.

Command	Com-mand Cycle #1	# of Valid Address Cycles	Data Input Cycles	Com-mand Cycle #2	# of Valid Address Cycles #2	Com-mand Cycle #3	Valid while se-lected LUN is busy (1)	Valid while other LUNs are busy (2)	Notes
Reset Operations									
RESET	FFh	0	-	-	-	-	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	-	-	-	-	Yes	Yes	
RESET LUN	FAh	3	-	-	-	-	Yes	Yes	
Identification Operations									
READ ID	90h	1	-	-	-	-			3
READ PARAMETER PAGE	ECh	1	-	-	-	-			
READ UNIQUE ID	EDh	1	-	-	-	-			
Configuration Operations									
VOLUME SELECT	E1h	1	-	-	-	-			
GET FEATURES	EEh	1	-	-	-	-			3
SET FEATURES	EFh	1	4	-	-	-			4
GET FEATURES by LUN	D4h	2	-	-	-	-		Yes	3
SET FEATURES by LUN	D5h	2	4	-	-	-		Yes	4
Status Operations									
READ STATUS	70h	0	-	-	-	-	Yes		
READ STATUS ENHANCED	78h	3	-	-	-	-	Yes	Yes	
Column Address Operations									
CHANGE READ COLUMN	05h	2	-	E0h	-	-		Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	-	E0h	-	-		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5	-	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	opt	-	-	-		Yes	
CHANGE ROW ADDRESS	85h	5	opt	11h(opt)	-	-		Yes	5
Read Operations									
READ MODE	00h	0	-	-	-	-		Yes	
READ PAGE	00h	5	-	30h	-	-		Yes	6
READ PAGE MULTIPLANE	00h	5	-	32h	-	-		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	-	-	-	-		Yes	7
READ PAGE CACHE RANDOM	00h	5	-	31h	-	-		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	-	-	-	-		Yes	7
Program Operations									
PROGRAM PAGE	80h	5	Yes	10h				Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h				Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h				Yes	8
Erase Operations									
ERASE BLOCK	60h	3	-	D0h				Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3	-	D1h				Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3	-	60h	3	D0h		Yes	
Copyback Operations									
COPYBACK READ	00h	5	-	35h				Yes	6
COPYBACK PROGRAM	85h	5	opt	10h				Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	opt	11h				Yes	

Notes from Micron data sheet:

1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations.
3. The READ ID (90h), GET FEATURES (EEh), and GET FEATURES by LUN (D4h) output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands require data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.

5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 114 of data sheet) for more details.
6. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.

Set Feature Command for SLC mode:

Mode	FA	P1	P2	P3	P4
SLC	91h	00h	01h	00h	00h
MLC	91h	02h	01h	00h	00h

P2 = 01h means Non-squashed SLC address mode – address bits do not shift from MLC address (default).
P2 = 00h means Squashed address mode - address bits shift from MLC address.

10. MMP and ECC (Error Correcting Code)

MMP models do not support Error Correcting Code (ECC) functionality. ECC functions, if they are present in a memory device, are typically found in the NAND and DDRx families. The MMP product does not have any plans to provide such functions in the models. MMP models are provided as system level emulation models and not as verification IP. The below sections discuss work-arounds that enable the user to deal with some ECC scenarios. Note that ECC means different things to different device families.

10.1. NAND FLASH and ECC (Error Correcting Code)

MMP NAND models do not support Error Correcting Code (ECC) functionality. There will not be an ECC error in a Palladium MMP flash model; the data stored in a MMP model should not need to be corrected because the model does not degrade over time like the real device. The data returned is always correct. The paragraphs below provide details about host ECC in relation to MMP NAND Flash.

For NAND Flash devices, ECC means that the internal engine in the Flash device calculates the ECC when programming and writes the resulting value into the spare array. The low level details of this operation are in the device specification. The Flash then re-calculates the ECC on reads and compares with the value stored in the spare array. If non-equivalence is found, bit error is indicated, and the device corrects and/or flags an error. There are several cases:

- If the controller relies on ECC generation internal to the Flash device, then the model needs to do nothing. This has worked for all users so far.
    - To support this scenario, model parameters can be modified to indicate that ECC is enabled. The controller is then happy. NOTE: the model will NOT actually do the ECC calculation.

- If the controller uses its own ECC and manually writes to the spare array in the device, then again the MMP model does not need to do anything.
    - There is a spare area is implemented in the NAND model for the host to store ECCs. This spare area allows the host to do data correction.

- If the controller relies on ECC generation internal to the memory device AND the controller reads and examines the spare calculation itself, then the MMP model will not work.
    - There is no MMP plan to enhance NAND FLASH MMP models to support this case. It is a large effort.

Occasionally, an issue may be seen due to the parameter page setting for the available number of bits of ECC correction. According to the ONFI standard this setting is handled by byte 112 of the parameter page. See the figure below for an example entry from the standard. Problems may occur with some controllers when byte 112 of the parameter page is set to the value '0'. If the controller requires some positive value for the *Number of bits ECC correctability*, then the user may need to change the setting to a value of '1'.

Table 13: Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
112	Number of bits ECC correctability	–	0Ch
113	Number of interleaved address bits	–	01h

11. Initialization Sequence

The ONFI 3.x Flash model requires that the memory controller or host follows the initialization sequence as documented in the specification. The sequence basically entails the following steps.

For Single Volume (one package per CE# or host target):

1. The asynchronous interface is active by default for each target.
2. The RESET (FFh) command must be the first command issued to the target (CE#). The target will become busy. The RESET busy time can be monitored with the R/B# pin or checked by polling the status register with the 70h status command.
3. Read configuration data from the model using READ ID, READ PARAMETER PAGE, etc. (optional)
4. The model is now initialized and ready for normal operation.

For CE# Pin Reduction and Volume Addressing:

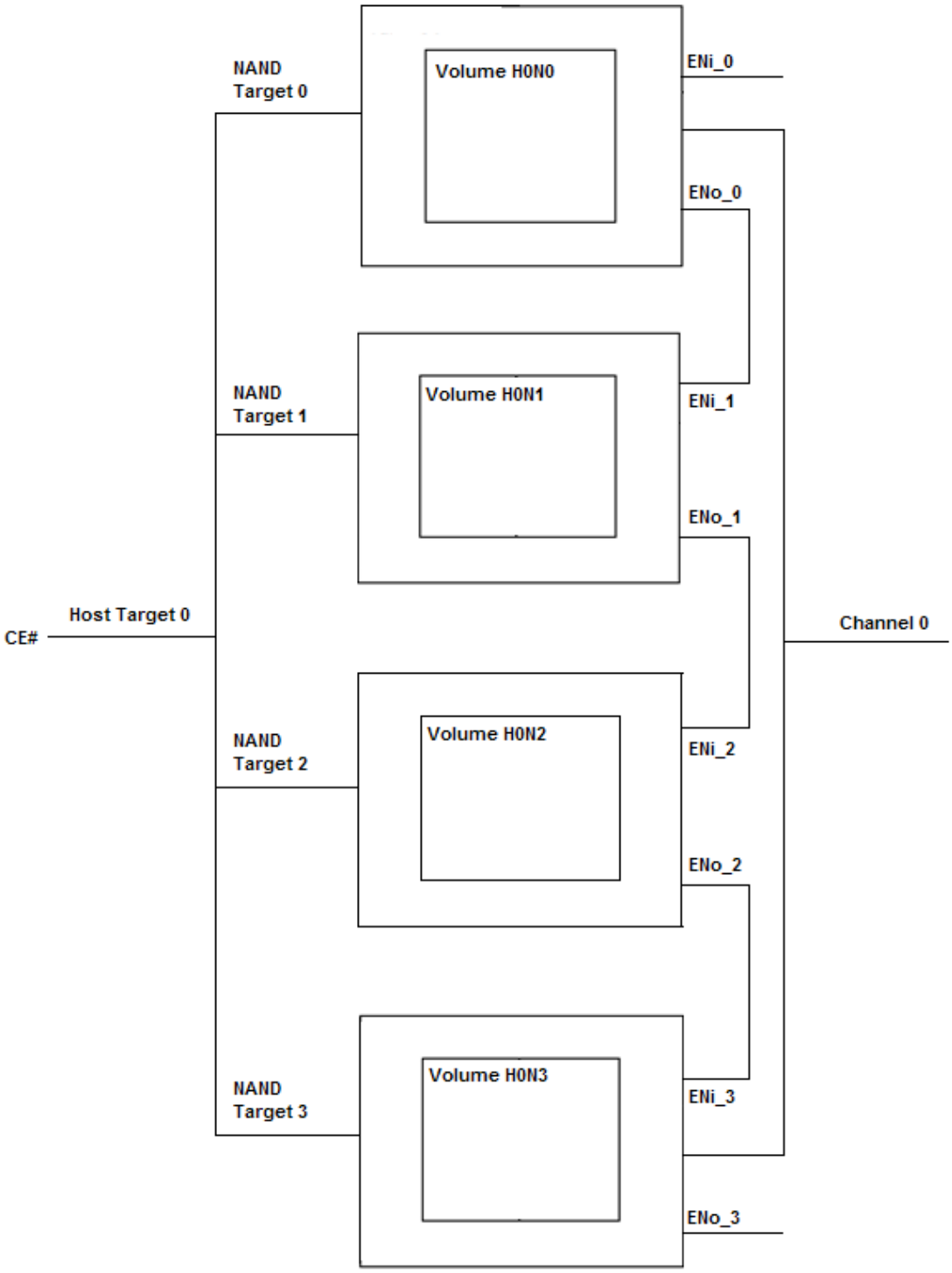
1. The asynchronous interface is active by default for each target.

2. Multiple Host Targets (CE#'s) can be active at the same time. See note below on how to properly issue multiple SET FEATURES (EFh) commands to appoint volume addresses.
3. The RESET (FFh) command must be the first command issued to the target (CE#) or targets. The target will become busy. The RESET busy time can be monitored with the R/B# pin or checked by polling the status register with the 70h status command.
4. R/B# goes LOW for tRST and can be monitored by the host by issuing READ STATUS (70h) commands and monitoring.
5. Read configuration data from the model using READ ID, READ PARAMETER PAGE, etc. (optional)
6. The host issues SET FEATURES (EFh) command to the Volume Configuration feature address to appoint the Volume address for the first NAND Target. The Volume Address specified shall be unique amongst all NAND Targets. After the SET FEATURE (EFh) command completes, ENo is set to one to enable the next volume in the chain to be appointed an address.
7. For each NAND Target connected to a CE# pin or Host Target, repeat step 6.
8. Repeat steps 3-7 for the next Host Target (CE# pin), if any.
9. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next Volume that is going to execute a command.

The model requires that these steps are performed in the correct sequence in order to complete initialization. The model will not respond to any others commands unless this sequence is completed.

Note: In cases where there are multiple NAND Targets within a package (i.e., multiple CE#'s), those NAND Targets share the same ENo signal, the host shall not stagger SET FEATURES (EFh) commands that appoint the Volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously then the host shall wait until Volume appointment for previous NAND Target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the Volume address for the next NAND Target that shares the ENo within a package.

A diagram of CE# Pin Reduction Topology with single channel is shown below:



12. Model Size

To reduce memory utilization each LUN has only 32 blocks (blocks 0 to 31) but the actual device has 2048 blocks. If larger size is needed please contact Customer Support.

13. Limitations

1. The Set Features command supports activating synchronous modes, SLC mode, and appointing volume address only.
2. Model does not check illegal sequence of command cycles.
3. Model does not support timing parameters, except tRHOH.
4. The time to program a page or erase a block is 1 fclk (fast clock) per address location.
5. Unsupported and partially supported features are listed in Features table.

14. Timing Parameter tRHOH

The model does not generally support timing parameters because it is cycle based. However tRHOH (an asynchronous mode parameter that controls RE# HIGH to output hold) is supported in number of fclks (fast clocks). The user may define a macro at compile time to hold the data by a number of fclks after RE# goes high. Use this macro only if data output is not already held long enough. The model holds the data valid for 2 fclks by default. The data can be held 3 additional fclks by using the following example command line option in ixcom flow:

```
vlan +define+tRHOH=3
```

15. Compile and Emulation

The memory models are currently provided in one format: an encrypted RTL file(s) (*.vp) that targets use in the IXCOM flows or in the ICE flow. The encrypted RTL (*.vp) file(s) must be synthesized along with other design code prior to acceleration / emulation.

An example of the command for compilation (including synthesis) of this model in IXCOM flow is shown below:

```
ixcom -64bit +sv -ua +dut+mt29f128g08cbcab \
../tb.v ../src/mt29f_128.vp \
../src/mt29f128g08cbcab.vp \
-incdir ../../../utils/cdn_mmp_utils/sv \
../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
……

xeDebug -64 --ncsim \
  -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
  -input auto_xedebug.tcl
```

Note that +sv switch is needed.

ICE flow synthesis commands:

```
vavlog ../src/mt29f_128.vp ../src/mt29f128g08cbcab.vp

vaelab –keepRtlSymbol –keepAllFlipFlop –outputVlog mt29f128g08cbcab.vgp
mt29f128g08cbcab
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can

remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

15.1. Model file list

mt29f_128.vp - LUN or die module that is instantiated by ONFI 3.0 and 3.2 models. It is located under flash/nand/onfi_3.0 within MMP release.
<model_name>.vp - model wrapper that instantiates one or more LUNs.

16. Sample Waveform

A waveform showing basic startup sequence - reset, read id, program page, read page, is available in the release under the onfi_3.0/micron/golden_waveform directory. It may be useful to have a look at this waveform when using the model for the first time. The waveform is also applicable to models in onfi_3.2/micron directory.

17. Debug Display

Debug messaging can be enabled with ONFI 3.x models. Please refer to the MMP_Debug_Display user guide under <release_dir>/docs directory for more details.

18. Revision History

The following table shows the revision history for this document

Date	Version	Revision
January 2013	1.0	Initial Release
February 2014	1.1	Added MLC+ models and SLC mode feature
July 2014	1.2	Repaired doc property title
September 2014	1.3	Remove version from UG file name. Update UXE / IXE documentation reference titles.
October 2014	1.4	Remove beta watermark. Add notation about optional signal DQS_c
November 2014	1.5	Remove emulation capacity info.
December 2014	1.6	Add emulation script info for IXCOM compile, including +sv switch. Update related publications list.
March 2015	1.7	Add timing parameter limitation and a section on tRHOH.
May 2015	1.8	Added some ONFI 3.0 and 3.2 models. Added Get/Set Features by LUN commands for ONFI 3.2 models. Replaced list of commands with features table. Added user adjustable parameter table. Added Sample Waveform and Debug Display sections.
July 2015	1.9	Update Cadence naming on front page
September 2015	2.0	Updated compile examples with .vp files. Removed references to <model_name>.vgp as an input file. Updated Limitations list. Updated initialization sequence with Read Configuration step as optional. Updated Set Features by LUN in Features table.
January 2016	2.1	Update for Palladium-Z1 and VXE
July 2016	2.2	Remove hyphen in Palladium naming
January 2018	2.3	Modify header and footer
February 2018	2.4	Ported ECC section from NAND UG to ONFI and TDDR UGs
July 2018	2.5	Update for new utility library