Technical Note

LPDDR5 Architecture

Introduction

This technical note describes the new features introduced in LPDDR5. LPDDR5 can operate at an I/O rate of 6400 Mb/s, which is 50% higher than the first version of LPDDR4. This higher operating rate significantly boosts memory speed and efficiency for a variety of applications including mobile computing devices such as smartphones, tablets, and ultrathin notebooks. In addition, LPDDR5 offers new features designed for mission-critical applications for segments such as automotive.

To achieve new levels of high-speed operation and lower power consumption than previous generations, the LPDDR5 architecture was designed using new techniques like bank groups and multi-clocking.

Key LPDDR5 specification updates include the following:

- To enable higher speeds:
  - I/O throughput up to 6400 Mb/s
  - Non-target on-die termination (NT ODT) for DQ added to support higher data rate in dual-rank configuration
  - Programmable multi-bank organization (4 banks/4-bank groups, 8 banks, and 16 banks)
  - Selectable background and command-based ZQ calibration
- To enable lower power consumption:
  - Multi-clocking architecture
  - Dynamic voltage and frequency scaling (DVFS) for core and I/O
  - Selectable differential and single-ended CK, WCK, and RDQS
  - Low-power READ/WRITE operation with DATA COPY and WRITE X functions

LPDDR5 Features

LPDDR5 offers new features designed for extremely high-speed operation and lower power consumption compared to LPDDR4 while maintaining some of the same key functions.

Table 1: LPDDR5 New Features

Feature	Description	Reference Document[1]
High data rate	Enables I/O throughput up to 6400 Mb/s	
Clocking architecture	Splits the clock into low-speed command/address (CA) clock (CK) up to 800 MHz and high-speed data clock (WCK) up to 3.2 GHz	TN-6204 LPDDR5 Clocking
Ultra-low-voltage core and I/O power supplies	Reduces supply voltage: V_{DD2} (1.05V/0.9V) and V_{DDQ} (0.5V termination/0.3V un-termination)	
Programmable bank organization	Supports 8 banks, 16 banks, and 4 banks with 4-bank groups to achieve higher data rates without increasing data granularity	TN-6201 LPDDR5 Bank Architecture
DVFS	Reduces both core power and I/O power at low frequencies	See Dynamic Voltage Frequency Scaling section of this technical note
Non-target DRAM ODT	Reduces reflection and improves signal integrity for DQ bus signals in dual-rank configuration	TN-6208 LPDDR5 Non-Target On-Die Termination
ZQ calibration	Supports two calibration modes selected by the system on a chip (SOC): background calibration and command-based calibration	TN-6207 LPDDR5 ZQ Calibration
Clock power reduction with single-ended mode	Supports single-ended mode with _t or _c selectable for CK, WCK, and RDQS	
Data copy	When the data transmitted on DQ0 through DQ7 or DQ8 through DQ15 is the same, only DQ0 or DQ8 is used for data transfer between LPDDR5 and controller	
Write X	Writes all 1s or all 0s to a specific address, eliminating the need to send data from the SOC	
Link ECC (optional)	Recovers data even when transmission errors are introduced, enabling high data reliability targeting automotive applications	

Note: 1. For more details, refer to these feature-specific Micron technical notes.

The features of LPDDR5 architecture differ significantly from the architectures of LPDDR4 technologies. The table below shows the key differences between LPDDR4/ LPDDR4X and LPDDR5.

Table 2: Key Feature Comparison: LPDDR4/LPDDR4X vs. LPDDR5

Feature	LPDDR4/LPDDR4X	LPDDR5	Notes for LPDDR5
Die density (MAX)	32Gb	32Gb	
Number of channel per die	1 or 2	1	Most DRAM vendor LPDDR4 die development is single-channel die for package design flexibility. Based on this trend, LPDDR5 only defines single-channel die.
Core voltage (V_{DD1})	1.8V	1.8V	
Core voltage (V_{DD2})	1.1V	V_{DD2H} = 1.05V V_{DD2L} = 1.05V or 0.9V (DVFSC mode for power reduction at low speed)	V_{DD2H} = V_{DD2L} = 1.05V is acceptable
I/O voltage (V_{DDQ})	1.1V/0.6V	0.5V termination or 0.3V un-termination (DVFSQ mode at low speed)	
Interface	LVSTL1.1/ LVSTL0.6	LVSTL0.5/0.3	Same concept as LPDDR4X but with lower interface voltage
MAX data rate (per pin)	4266 Mb/s	6400 Mb/s	
Burst length	16 or 32	16 or 32	Same prefetch size and same data granularity as LPDDR4/LPDDR4X
Bank organization	8 banks	4 banks/4-bank group mode, 8-bank mode, 16-bank mode	Bank group concept introduced in LPDDR5
Clock input	CK: 2133 MHz (MAX)	CK: 800 MHz (MAX) WCK: 3200 MHz (MAX)	In LPDDR4/LPDDR4X, CK is used as both CA clock and data clock In LPDDR5, CK is used as CA clock; WCK is used as data clock. WCK runs only when there is data traffic
WCK-to-CK ratio	N/A	2:1 or 4:1	2:1 ratio supported up to 3.2 Gb/s
Write strobe	DQS	WCK	
Read strobe	DQS	RDQS	
CA rate	SDR	DDR	
CA pin count	6 pins CA[5:0]	7 pins CA[6:0]	Removes CKE

Dynamic Voltage and Frequency Scaling

LPDDR5 uses dynamic voltage and frequency scaling (DVFS) to reduce energy consumption. DVFS is not available in LPDDR4/LPDDRX. DVFS has two modes, DVFS core (DVFSC) and DVFS V_{DDQ} (DVFSQ), shown in the table below.

Table 3: DVFSC and DVFSQ Modes Comparison

Mode	Frequency	Details	Note
DVFSC	High	V_{DD2H} = 1.05V rail only	For core power reduction
	Low	V_{DD2H} = 1.05V rail and V_{DD2L} = 0.9V rail	
DVFSQ	High	V_{DDQ} =0.5V with termination	For I/O power reduction
	Low	V_{DDQ} = 0.3V without termination	

DVFSC Mode

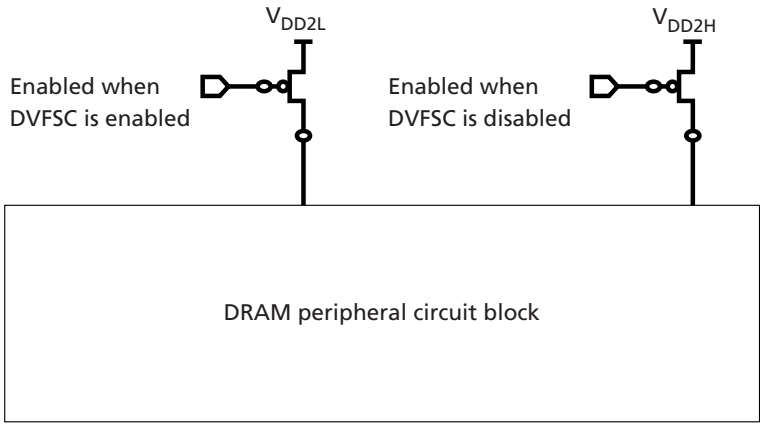
Memory circuits can be classified into two categories: stable voltage for memory cells and variable voltage for interface circuits and logic. DVFSC connects variable voltage circuits to low supply voltage to reduce power when operating at low data rates.

Using DVFSC mode is optional. Systems that do not implement DVFSC must supply the specified V_{DD2H} voltage level to both the V_{DD2H} and V_{DD2L} rails of the device and must set MR13 OP[7] = 1b and MR19 OP[1:0] = 00b at all times. Users unable to provide a 0.9V power rail can set V_{DD2L} = 1.05V. A single V_{DD2} rail (V_{DD2H} = V_{DD2L} = 1.05V) is acceptable but results in no power reduction.

DVFSC mode affects some AC parameters, such as ^{t}RC, ^{t}RCD, and ^{t}RP.

Refer to Micron's General LPDDR5 Specifications 3 for more information about DVFSC mode.

Figure 1: DVFSC Block Diagram



DVFSQ Mode

DVFSQ mode is used to reduce I/O power consumption at a data rate of 3200 Mb/s or lower. DVFSQ can only be used under un-terminated conditions.

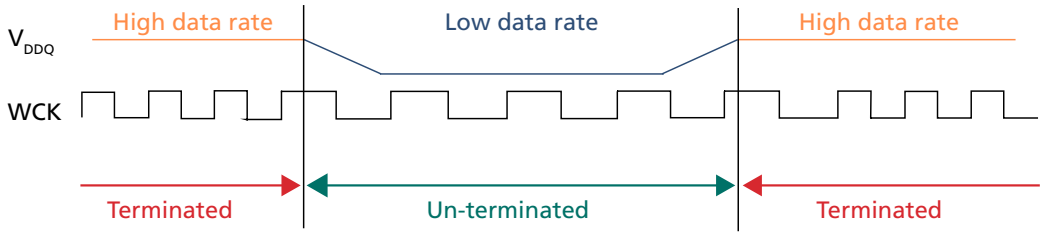
Table 4: DVFSQ Mode

DVFSQ	Frequency	V_{DDQ}	DQ ODT	DC Swing
Disabled	Greater than 3200 Mb/s	0.5V	Terminated	0.5 x V_{DDQ} = 250mV
Enabled	Less than or equal to 3200 Mb/s	0.3V	Un-terminated	V_{DDQ} = 300mV

Signal swing does not vary much whether DVFSQ is enabled or disabled; therefore, the same receiver specification is applied in both cases.

Refer to Micron's General LPDDR5 Specifications 3 for more information about DVFSQ mode.

Figure 2: V_{DDQ} Change When DVFSQ Is Enabled



Revision History

Rev. A – 07/19

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992