SYNOPSYS®
Silicon to Software™

LPDDR4x mulitPHY
Silicon Bring Up Script Review

LPDDR4 3200Mbps example

2020-03-26

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Summary

The PHY initialization script review Synopsys conducts is purely visual

– Customer need to validate the sequence through simulation
– Customer need to get the initial driver strength/ODT/Vref etc value from SIPI simulation result
– Customer need to check the register setting for lane connection with PCB design
– Customer need to follow the Streaming Messages in firmware APP note for training log decoder
– Customer need to check all published STAR in DWDL
  https://www.synopsys.com/dw/star.php?c=dwc_ap_lpddr4x_multiphy_tsmc16ffc18

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Ref Documents

- dwc_lpddr4x_multiphy_pub_databook.pdf
- dwc_ap_lpddr4x_multiphy_tsmc16ffc18_databook.pdf
- dwc_ddrn_phy_phyinit_application_note.pdf
- dwc_ddrn_phy_training_firmware_application_note.pdf
- HSPICE_model_app_note.pdf
- phyinit\<version>\software\lpddr4\src\dwc_ddrphy_phyinit_struct.h
- firmware\<version>\lpddr4\mnPmuSramMsgBlock_lpddr4.h
- firmware\<version>\lpddr4\lpddr4_pmu_train.strings
- JESD209-4B

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Technology Dependent Register Programming

dwc_ddrphy_phyinit_userCustom_customPreTrain()

- Please follow the section Technology Dependent Register Programming in training APP note

Some PHY register programming are technology dependent. This section documents the list of such registers and pointers to documents containing the technology specific values to program.

PhyInit will program these registers to a default value or leave them at default hardware reset state. It is highly recommended that users consult the documentation provided in the table below and program each registers with recommended values for the respective process technology in the dwc_ddrphy_phyinit_userCustom_customPreTrain() function.

Table 3 Technology Dependent Registers

Register Name	Bits	Sub-field name	PhyInit default	Technology specific documentation
ATxSlewRate	[3:0]	ATxPreP	0xf	CA HSPICE App Note – Calibration Codes DWC_TXRXCA/rise_index in table
ATxSlewRate	[7:4]	ATxPreN	0xf	CA HSPICE App Note – Calibration Codes DWC_TXRXCA/fall_index in table
TxSlewRate	[3:0]	TxPreP	0xf	DQ HSPICE App Note – Calibration Codes DWC_TXRXDQ/rise_index in table
TxSlewRate	[7:4]	TxPreN	0xf	DQ HSPICE App Note – Calibration Codes DWC_TXRXDQ/fall_index in table
PllCtrl1	[4:0]	PllCpIntCtrl	0x0	PHY Databook
PllCtrl1	[8:5]	PllCpPropCtrl	0x1	PHY Databook
PllTestMode	[15:0]		0x0124	PHY Databook

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HSPICE_model_app_note_lp4x.pdf

							DWC_TXRXDQ		DWC_TXRXCA	
Mode	VDDQ	Transistor	Resistor	Temperature	ncode	pcode	fall_index	rise_index	fall_index	rise_index
DDR4	1.14V	ss	s	125C	23	24	15	2	15	11
	1.14V	ss	s	-40C	19	16	15	2	15	11
	1.20V	tt	t	25C	14	13	15	2	15	11
	1.3V	ff	f	-40C	6	5	15	2	15	11
LPDDR4	1.06	ss	s	125C	25	26	8	15	5	15
	1.06	ss	s	-40C	20	18	8	15	5	15
	1.1	tt	t	25C	16	14	8	15	5	15
	1.17	ff	f	-40C	8	7	8	15	5	15
LPDDR4X	1.06 (VDDQLP=0.57)	ss	s	125C	23	11	4	15	5	15
	1.06 (VDDQLP=0.57)	ss	s	-40C	19	13	4	15	5	15
	1.1 (VDDQLP=0.6)	tt	t	25C	14	7	4	15	5	15
	1.17 (VDDQLP=0.65)	ff	f	-40C	6	3	4	15	5	15

```
ATxSlewRate:1ff
ATxImpedance:7f
TxSlewRate:1ff
TxOdtDrvStren:600
TxImpedanceCtrl1:e3f
CalDrvStr0:11
```


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Register Review

Table 11-114 Register Name: CalDrvStr0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	CalDrvStrPd50	5..15 - Reserved for future. 4 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ*35% 3 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ/2.5 2 - 40R pull-down and 40R PMOS pull-up 1 - 120R pull-down and 120R PMOS pull-up 0 - 120R pull-down and 120R NMOS pull-up (Default)	R/W	0x0
[7:4]	CalDrvStrPu50	5..15 - Reserved for future. 4 - Calibrates with 120-ohm external resistance at VOH= VOH=VDDQ*35% (for low-power LPDDR4) 3 - Calibrates with 120-ohm external resistance at VOH=VDDQ/2.5 (for low-power LPDDR4) 2 - Calibrates linear pull-up with 40-ohm external resistance at VOH=VDDQ/2 (for DDR4, LPDDR4) 1 - Calibrates linear pull-up with 120-ohm external resistance at VOH=VDDQ/2 (for DDR4, LPDDR4) 0 - Calibrates with 120-ohm external resistance at VOH=VDDQ/2 (for LPDDR4x) (Default)	R/W	0x0

```
ATxSlewRate:1ff
ATxImpedance:7f
TxSlewRate:1ff
TxOdtDrvStren:600
TxImpedanceCtrl1:e3f
CalDrvStr0:11
```


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Register Review

Table 11-11 Register Name: ATxImpedance Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[4:0]	ADrvStrenP	5 bit bus used to select the target pull up output impedance. Please Refer to Technology specific PHY DATABOOK for supported options Connects to the DrvStren pins of the driver. 110_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 120R DRAM termination LPDDR4 low-power drive into 240R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power drive into 120R DRAM termination at VOH=VDDQ*35% [1] 100_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 60R DRAM termination LPDDR4 low-power drive into 120R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power drive into 60R DRAM termination at VOH=VDDQ*35% [1] 000_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 40R DRAM termination LPDDR4 low-power into 80R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power into 40R DRAM termination at VOH=VDDQ*35% [1] 111_00 = 120R linear pull-up connected to VDDQ (DDR4, LPDDR4) 111_01 = 60R linear pull-up connected to VDDQ (DDR4, LPDDR4) 111_11 = 40R linear pull-up connected to VDDQ (DDR4, LPDDR4) NOTE [1]: see PHY data book for complete description of LPDDR4 VDDQLP pull-up mode NOTE [2]: if any pull-up connected to VDDQLP is enabled, all pull-ups connected to VDDQ will be disabled.	R/W	0x1f
[9:5]	ADrvStrenN	5 bit bus used to select the target pull down output impedance. Please Refer to Technology specific PHY DATABOOK for supported option Connects to the DrvStren pins of the driver. xxx_00 = 120R pull-down (DDR4, LPDDR4/LPDDR4x) xxx_01 = 60R pull-down (DDR4, LPDDR4/LPDDR4x) xxx_11 = 40R pull-down (DDR4, LPDDR4/LPDDR4x)	R/W	0x1f

```
ATxSlewRate:1ff
ATxImpedance:7f
TxSlewRate:1ff
TxOdtDrvStren:600
TxImpedanceCtrl1:e3f
CalDrvStr0:11
```


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Register Review

Table 11-55 Register Name: TxImpedanceCtrl1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	DrvStrenFSDqP	Please Refer to Technology specific PHY DATABOOK for supported options. 6 bit bus used to select the target pull up output impedance. Connects to the DrvStren pins of the driver. xxx_110 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 120R DRAM termination LPDDR4 low-power drive into 240R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power drive into 120R DRAM termination at VOH=VDDQ*35% [1] xxx_100 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 60R DRAM termination LPDDR4 low-power drive into 120R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power drive into 60R DRAM termination at VOH=VDDQ*35% [1] xxx_000 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 40R DRAM termination LPDDR4 low-power into 80R DRAM termination at VOH=VDDQ/2.5 [1] LPDDR4 low-power into 40R DRAM termination at VOH=VDDQ*35% [1] 000_111 = HiZ 001_111 = 120R linear pull-up connected to VDDQ (DDR4, LPDDR4) 011_111 = 60R linear pull-up connected to VDDQ (DDR4, LPDDR4) 111_111 = 40R linear pull-up connected to VDDQ (DDR4, LPDDR4) NOTE [1]: see PHY data book for complete description of LPDDR4 VDDQLP pull-up mode NOTE [2]: if any pull-up connected to VDDQLP is enabled, all pull-ups connected to VDDQ will be disabled.	R/W	0x3f

Bits	Name	Description	Access	Default
[11:6]	DrvStrenFSDqN	Please Refer to Technology specific PHY DATABOOK for supported options. 6 bit bus used to select the target pull down output impedance. Connects to the DrvStren pins of the driver. 000_xxx = HiZ 001_xxx = 120R pull-down (DDR4, LPDDR4/LPDDR4x) 011_xxx = 60R pull-down (DDR4, LPDDR4/LPDDR4x) 111_xxx = 40R pull-down (DDR4, LPDDR4/LPDDR4x)	R/W	0x3f
[15:12]	Unimplemented	Returns zero on reads	R	0x0

```
ATxSlewRate:1ff
ATxImpedance:7f
TxSlewRate:1ff
TxOdtDrvStren:600
TxImpedanceCtrl1:e3f
CalDrvStr0:11
```


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Lane connection

dwc_ddrphy_phyinit_userCustom_customPreTrain()

- DQ Lane Swapping limitation
  - Only DQ lanes may be swapped. DQS signals and DM signals may not be swapped
  - When operating with x16 devices, DQ lanes may only be swapped within a byte and cannot be swapped across bytes
- CA
  - See CSR register MapCAAntoDfi ..MapCABntoDfi (n=0..5)

Table 2-2 Swapped connection Dq*X*LnSel programming

DBYTE Register	SDRAM Bit	DBYTE Lane	Programming
Dq0LnSel	0 (DQ0)	1	0x1
Dq1LnSel	1 (DQ1)	0	0x0
Dq2LnSel	2 (DQ2)	3	0x3
Dq3LnSel	3 (DQ3)	2	0x2
Dq4LnSel	4 (DQ4)	5	0x5
Dq5LnSel	5 (DQ5)	4	0x4
Dq6LnSel	6 (DQ6)	7	0x7
Dq7LnSel	7 (DQ7)	6	0x6

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HdtCtrl=0x4 for training debug

Ref 11 Streaming Messages in training APP note

Pseudocode for polling and printing the full string value is given below:

```
//-------------------------------------------------------------------------
// Decode_Streaming_Message Pseudocode
//-------------------------------------------------------------------------
Function decode_streaming_message(){
        string_index = get_mail(32bit)
        debug_string = lookup_string_index(string_index)
        while (i <= (string_index & 0xffff)){
                args[i] = get_mail(32bit)
                i++
                }
        Printf(debug_string, arg[0], arg[1],  … , arg[i-1])
        }
```

Example log can be get through IP CTB env

runtc cfg=ac10d4ch2 tc=demo_basic dram=lpddr4 dimm=udimm skip_train=0 freq0=1600 freq_ratio0=1 rank=1 pstates=1 hard_macro=E hdtCtrl=4 hdtCtrl=131f

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Controller Sequence Check

DWC_ddr_umctl2 and Memory Initialization with LPDDR4X multiPHY

Table 6-9 DWC_ddr_umctl2 and Memory Initialization with LPDDR4X multiPHY

Step	Application	SVTB Task	Notes
1	Follow the PHYs power up procedure		See PUB databook for details
2	Program the DWC_ddr_umctl2 registers		Note 1
3	De-assert reset signal `core_ddrc_rstn`	`reset_dut`	
25	Wait for DWC_ddr_umctl2 to move to normal operating mode by monitoring `STAT.operating_mode` signal	`reset_dut`	
26	Set back registers in step 4 to the original values if desired		

Note 1: When running training with the PHY. The following controller registers must be programmed to these values at this stage: `INIT0.skip_dram_init`=2'b11 `PWRCTL.selfref_sw` = 1'b1 Programming them as follows is only allowed for simulation purposes when skipping training `INIT0.skip_dram_init`=0 (that is, SDRAM INIT through the controller) `PWRCTL.selfref_sw` = 0

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Training Log example

A snapshot need for further debug

```
PMU10: **** Start LPDDR4 Training. PMU Firmware Revision 0x1002 ****
PMU10: Setting boot clock divider to 32
PMU10: PHY TOTALS - NUM_DBYTES 4 NUM_NIBBLES 8 NUM_ANIBS 12
PMU10: CSA=0x01, CSB=0x01, TSTAGES=0x131F, HDTOUT=4, MMISC=1 DRAMFreq=3200MT DramType=LPDDR4
PMU10: Pstate0 MRS MR01_A0=0x14 MR02_A0=0x2D MR03_A0=0x29 MR11_A0=0x64
PMU10: Pstate0 MRS MR12_A0=0x4D MR13_A0=0x28 MR14_A0=0x42 MR22_A0=0x18
PMU10: Pstate0 MRS MR01_B0=0x14 MR02_B0=0x2D MR03_B0=0x29 MR11_B0=0x64
PMU10: Pstate0 MRS MR12_B0=0x4D MR13_B0=0x28 MR14_B0=0x42 MR22_B0=0x18
PMU5: CA bitmap dump for cs 0
PMU5: CAA0 ffffffff80000000000000003fffffffffffffffffffffff
PMU5: CAA1 ffffffffe00000000000000007fffffffffffffffffffffff
PMU5: CAA2 ffffffffe00000000000000007fffffffffffffffffffffff
PMU5: CAA3 ffffffffc00000000000000001fffffffffffffffffffffff
PMU5: CAA4 ffffffffc00000000000000003fffffffffffffffffffffff
PMU5: CAA5 ffffffffe00000000000000007fffffffffffffffffffffff
PMU5: CA bitmap dump for cs 0
PMU5: CAB0 ffffffffc00000000000000007fffffffffffffffffffffff
PMU5: CAB1 ffffffffe00000000000000003fffffffffffffffffffffff
PMU5: CAB2 ffffffff80000000000000003fffffffffffffffffffffff
PMU5: CAB3 ffffffffc00000000000000003fffffffffffffffffffffff
PMU5: CAB4 ffffffff80000000000000003fffffffffffffffffffffff
PMU5: CAB5 ffffffffc00000000000000003fffffffffffffffffffffff
End of initialization
PMU5: CS0 <<KEY>> 0 RxEnDly, 1 RxClkDly <<KEY>> coarse(10:6) fine(5:0)
PMU5: ID=0 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x  3cd  39b  399  3c9    0    0    0    0    0    0
PMU5: [1]:0x  3cd  39b  399  3c9    0    0    0    0    0    0
PMU5: ID=1 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [1]:0x   10   10   10   10    0    0    0    0    0    0
End of read enable training
PMU5: CS0 <<KEY>> 0 TxDqsDly, 1 TxDqDly <<KEY>> coarse(9:6) fine(5:0)
PMU5: ID=0 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   49   5b   57   47    0    0    0    0    0    0
PMU5: [1]:0x   49   5b   57   47    0    0    0    0    0    0
PMU5: ID=1 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [1]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [2]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [3]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [4]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [5]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [6]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [7]:0x   10   10   10   10    0    0    0    0    0    0
PMU5: [8]:0x   10   10   10   10    0    0    0    0    0    0
End of fine write leveling
```

```
PMU5: CS0 <<KEY>> 0 RxPBDly <<KEY>> 1 Delay Unit ~= 7ps
PMU5: ID=0 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x    5    3    2    3    0    0    0    0    0    0
PMU5: [1]:0x    a    3    6    2    0    0    0    0    0    0
PMU5: [2]:0x    3    7    7    b    0    0    0    0    0    0
PMU5: [3]:0x    7    3    b    7    0    0    0    0    0    0
PMU5: [4]:0x    2    1    2    8    0    0    0    0    0    0
PMU5: [5]:0x    7    4    5    2    0    0    0    0    0    0
PMU5: [6]:0x    9    4    5    4    0    0    0    0    0    0
PMU5: [7]:0x    c    5    c    e    0    0    0    0    0    0
PMU5: [8]:0x    0    0    0    0    0    0    0    0    0    0
End of read dq deskew training
PMU4: RxClkDly Passing Regions (EyeLeft EyeRight -> EyeCenter)
PMU4: DB 0 nibble 0:   8  30 ->  19
PMU4: DB 0 nibble 1:   3  25 ->  14
PMU4: DB 1 nibble 0:   6  27 ->  16
PMU4: DB 1 nibble 1:   2  24 ->  13
PMU4: RxClkDly Passing Regions (EyeLeft EyeRight -> EyeCenter)
PMU4: DB 2 nibble 0:   6  26 ->  16
PMU4: DB 2 nibble 1:   2  22 ->  12
PMU4: DB 3 nibble 0:   7  27 ->  17
PMU4: DB 3 nibble 1:   4  22 ->  13
PMU5: CS0 <<KEY>> 0 RxEnDly, 1 RxClkDly <<KEY>> coarse(10:6) fine(5:0)
PMU5: ID=0 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x  3cd  39b  399  3c9    0    0    0    0    0    0
PMU5: [1]:0x  3cd  39b  399  3c9    0    0    0    0    0    0
PMU5: ID=1 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   13   10   10   11    0    0    0    0    0    0
PMU5: [1]:0x    e    d    c    d    0    0    0    0    0    0
End of MPR read delay center optimization
PMU4: Dbyte 1 dqs2dq = 64/32 UI
PMU4: Dbyte 2 dqs2dq = 62/32 UI
PMU5: CS0 <<KEY>> 0 TxDqsDly, 1 TxDqDly <<KEY>> coarse(9:6) fine(5:0)
PMU5: ID=0 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   c9   db   d7   c7    0    0    0    0    0    0
PMU5: [1]:0x   c9   db   d7   c7    0    0    0    0    0    0
PMU5: ID=1 -- db0  db1  db2  db3  db4  db5  db6  db7  db8  db9 --
PMU5: [0]:0x   9a   cb   c7   98    0    0    0    0    0    0
PMU5: [1]:0x   9b   cb   c9   98    0    0    0    0    0    0
PMU5: [2]:0x   9c   cf   c9   9b    0    0    0    0    0    0
PMU5: [3]:0x   9d   cd   c9   9a    0    0    0    0    0    0
PMU5: [4]:0x   9b   cb   c7   99    0    0    0    0    0    0
PMU5: [5]:0x   9c   cc   c9   97    0    0    0    0    0    0
PMU5: [6]:0x   9d   cc   c9   99    0    0    0    0    0    0
PMU5: [7]:0x   9d   cb   cb   9b    0    0    0    0    0    0
PMU5: [8]:0x   9d   cb   cb   9b    0    0    0    0    0    0
End of Write leveling coarse delay
```


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CSR Dump Registers

Required when training failed or mission mode debug

- Register List
  - The register list description 11.2 Register Address Map in PUB databook
  - macro/Latest/ipxact/acx10_dat4.dwc_ddrphy_top.ipxact.xml
  - CTB reference files after runtc ctb/Latest/sim/csr_defines.sv

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Thank You