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LOW POWER DOUBLE DATA RATE 3 SDRAM (LPDDR3)

(From JEDEC Board ballot JCB-12-22, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memory.)

1 Scope

This document defines the LPDDR3 specification, including features, functionalities, ACand DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for JEDEC compliant 4 Gb through 32 Gb for x16 and x32 SDRAM devices. This specification was created using aspects of the following specifications: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR2 (JESD209-2). Each aspect of the specification was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR3 specification.

2 Package ballout & Pin Definition

2.1 POP FBGA Ball-outs

2.1.1 216-ball 12mm x 12mm 0.4mm Pitch Dual-Channel POP FBGA (top view) Using Variation VCCCDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSSa/b	VDD2_a/b	DQ30_a	DQ29_a	VSSQ_a	DQ26_a	DQ25_a	VSSQ_a	DQS3_c_a	VSSQ_a	DQ14_a	DQ13_a	VSS_a	VDD1_a	VDD2_a	DQ11_a	DQ10_a	DQ9_a	DQS1_t_a	DM_1_a	VDDQ_a	DQS0_t_a	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS_a/b	DNU
B	VSSQ_b/ VSS	NC	DQ31_a	VDDQ_a	DQ28_a	DQ27_a	VDDQ_a	DQ24_a	VDDQ_a	DQS3_t_a	DM3_a	DQ15_a	VDDQ_a	VSSQ_a	Vref(DQ)_a	VDD2_a	DQ12_a	VDDQ_a	DQ8_a	DQS1_c_a	VSSQ_a	DM_0_a	DQS0_c_a	VSSQ_a	VDDQ_a	DQ5_a	DQ2_a	NC	VSSQ_a
C	VDD1_a/b	DQ16_b																										VDD1_a	VDD2_a/b
D	DQ17_b	VDDQ_b																										DQ1_a	VDDQ_a
E	DQ18_b	DQ19_b																										VSSQ_a	DQ0_a
F	VSSQ_b	DQ20_b																										DM2_a	VDDQ_a
G	DQ21_b	VDDQ_b																										DQS2_t_a	DQS2_c_a
H	DQ22_b	DQ23_b																										VSSQ_a	DQ23_a
J	VSSQ_b	VDDQ_b																										VDDQ_a	DQ22_a
K	DQS2_c_b	DQS2_t_b																										DQ20_a	DQ21_a
L	DM2_b	DQ0_b																										DQ19_a	VSSQ_a
M	DQ1_b	VSSQ_b																										VDDQ_a	DQ18_a
N	DQ2_b	VDD1_b																										DQ16_a	DQ17_a
P	VSS_b	VSS_b																										VDD2_b	VDD1_b
R	VDD1_b	Vref(DQ)_b																										VSS_b	CA0_b
T	VDD2_b	VDD2_b																										VDDCA_b	CA1_b
U	VDDQ_b	DQ3_b																										Vref(CA)_b	CA2_b
V	DQ4_b	VSSQ_b																										VSSCA_b	CA3_b
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b
Y	VDDQ_b	DQ7_b																										CSB0_b	CKE1_b
AA	DQS0_t_b	DQS0_c_b																										VSSCA_b	CKE0_b
AB	DM0_b	VSSQ_b																										CK_t_b	CK_c_b
AC	VDDQ_b	DM1_b																										VDDCA_b	CA5_b
AD	DQS1_c_b	DQS1_t_b																										CA7_b	CA6_b
AE	DQ8_b	VSSQ_b																										CA8_b	VDDCA_b
AF	DQ9_b	VDDQ_b																										VSSCA_b	CA9_b
AG	DQ10_b	DQ11_b																										VDD2_a/b	ZQ_b
AH	VSSQ_b	VDD1_a/b	VDD2_a/b	DQ13_b	VSSQ_b	DQ15_b	DM3_b	DQS3_t_b	VDDQ_b	DQ26_b	DQ27_b	VDDQ_b	DQ30_b	VSSQ_b	VDD2_a	Vref(CA)_a	CA9_a	VSSCA_a	CA7_a	CA6_a	CK_c_a	VDDCA_a	CKE0_a	CSB0_a	CA3_a	CA2_a	CA1_a	VDD1_a/b	VSSCA_a
AJ	DNU	VSS_a/b	DQ12_b	VDDQ_b	DQ14_b	VDDQ_b	VSSQ_b	DQS3_c_b	DQ24_b	DQ25_b	VSSQ_b	DQ28_b	DQ29_b	DQ31_b	VDD1_a	VSS_a	ZQ_a	CA8_a	VDDCA_a	CA5_a	CK_t_a	VSSCA_a	CKE1_a	CSB1_a	CA4_a	VDDCA_a	CA0_a	VSS_a/b	DNU

Channel b
Channel a
Power
Ground
Do Not Use
ZQ
Clock
NC

Note 1: 12x12 mm, 0.4mm pitch, 29 rows

Note 2: 216 Ball Count

Note 3: Top View, A1 in Top Left Corner

Note 4: See JESD21-C, Section 3.12.2

Note 5: ODT pin is NOT supported. ODT die pads are connected to VSS inside the package.

Note 6: VSS_a, VSS_b, VSS_a/b, VSSQ_a, VSSQ_b, VSSQ_b/VSS, VSSCA_a, and VSSCA_b, may be connected to a common VSS inside the package, see manufacturer datasheet for actual connection. As such, all balls labeled VSSxyz are equivalent to the label "VSSxyz, VSS".

2.1.2 256-ball 14mm x 14mm 0.4mm Pitch Dual-Channel POP FBGA (top view) Using Variation VEECDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	DNU	DNU	VDD2	DQ30_a	DQ28_a	DQ27_a	VDDQ	DQ24_a	DQS3_t_a	VDDQ	VDD2	DQ15_a	VDDQ	DQ12_a	DQ11_a	VDDQ	DQ8_a	DQS1_t_a	VDDQ	VDD2	ODT_a	Vref(DQ)_a	VDDQ	DQS0_c_a	DQ7_a	VDDQ	DQ4_a	DQ3_a	VDDQ	DQ0_a	VDDQ	VDD2	DNU	DNU	A
B	DNU	VSS	VDD1	DQ31_a	DQ29_a	VSS	DQ26_a	DQ25_a	VSS	DQS3_c_a	DM3_a	VSS	DQ14_a	DQ13_a	VSS	DQ10_a	DQ9_a	VSS	DQS1_c_a	DM1_a	VSS	DM0_a	DQS0_t_a	VSS	DQ6_a	DQ5_a	VSS	DQ2_a	DQ1_a	VSS	DM2_a	VDD1	VSS	DNU	B
C	VDD2	VDD1																															DQS2_c_a	VDDQ	C
D	DQ17_b	DQ16_b																															VSS	DQS2_t_a	D
E	DQ19_b	DQ18_b																															DQ22_a	DQ23_a	E
F	DQ20_b	VSS																															DQ21_a	VDDQ	F
G	VDDQ	DQ21_b																															VSS	DQ20_a	G
H	DQ23_b	DQ22_b																															DQ18_a	DQ19_a	H
J	DQS2_t_b	VSS																															DQ16_a	DQ17_a	J
K	VDDQ	DQS2_c_b																															VSS	VDDQ	K
L	VDD2	DM2_b																															VDD1	VDD2	L
M	DQ0_b	VSS																															VSS	VSS	M
N	VDDQ	DQ1_b																															CA0_b	VDDCA	N
P	DQ3_b	DQ2_b																															CA2_b	CA1_b	P
R	DQ4_b	VSS																															VSS	VDD2	R
T	VDDQ	DQ5_b																															CA4_b	CA3_b	T
U	DQ7_b	DQ6_b																															CS1_n_b	CS0_n_b	U
V	DQS0_c_b	VSS																															CKE1_b	CKE0_b	V
W	VDDQ	DQS0_t_b																															VSS	VDDCA	W
Y	Vref(DQ)_b	DM0_b																															CK_c_b	CK_t_b	Y
AA	ODT_b	VSS																															Vref(CA)_b	VDD2	AA
AB	VDD2	DM1_b																															VSS	VDDCA	AB
AC	VDDQ	DQS1_c_b																															CA6_b	CA5_b	AC
AD	DQS1_t_b	VSS																															VSS	CA7_b	AD
AE	DQ8_b	DQ9_b																															CA8_b	VDDCA	AE
AE	VDDQ	DQ10_b																															ZQ0_b	CA9_b	AE
AG	DQ11_b	VSS																															RFU	ZQ1_b	AG
AH	DQ12_b	DQ13_b																															VDD1	VDD2	AH
AJ	VDDQ	DQ14_b																															VSS	VSS	AJ
AK	DQ15_b	VSS																															DNU	DNU	AK
AL	VDDQ	DM3_b																															DNU	DNU	AL
AM	VDD2	VDD1																															DNU	DNU	AM
AN	DNU	VSS	DQS3_c_b	VSS	DQ25_b	DQ26_b	VSS	DQ29_b	DQ31_b	VSS	VDD1	RFU	ZQ0_a	CA8_a	VSS	CA6_a	VSS	Vref(CA)_a	CK_c_a	VSS	CKE1_a	CS1_n_a	CA4_a	VSS	CA2_a	CA0_a	VSS	VDD1	VSS	DNU	DNU	DNU	DNU	DNU	AN
AP	DNU	DNU	VDDQ	DQS3_t_b	DQ24_b	VDDQ	DQ27_b	DQ28_b	DQ30_b	VDDQ	VDD2	ZQ1_a	CA9_a	VDDCA	CA7_a	CA5_a	VDDCA	VDD2	CK_t_a	VDDCA	CKE0_a	CS0_n_a	CA3_a	VDD2	CA1_a	VDDCA	VSS	VDD2	VSS	DNU	DNU	DNU	DNU	DNU	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

- VDD1
- VDD2
- VDDCA
- VDDQ
- VSS
- Vref(CA)_a, Vref(CA)_b, Vref(DQ)_a, Vref(DQ)_b
- Channel a, DQ,DQS_t,DQS_c,DM,CA,CS_n,CKE
- Channel b, DQ,DQS_t,DQS_c,DM,CA,CS_n,CKE
- CK_t,CK_c
- ZQ
- RFU

NOTE 1 14mm x 14mm, 0.4mm pitch, 34rows x 34 columns

NOTE 2 256 ball count

NOTE 3 Top View, A1 in Top Left Corner

NOTE 4 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to GND in the package.

NOTE 5 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
- ZQ1 is NC.

NOTE 6 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).

2.2 FBGA Package Ball-outs

2.2.1 253-Ball 0.5mm Pitch Discrete Dual-Channel FBGA (top view) MO TBD

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	NC	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VDDCA_a/b	VDD2_a/b	VSS_a/b	VDDCA_a/b	Vref(CA)_a	VDD2_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VDD1_a/b	VDD1_a/b	NC	A
B	VSS_a/b	VDD1_a/b	VSS_a/b	VSS_a/b	CA0_a	CA3_a	CSB1_a	CK_t_a	VDDCA_a/b	CA7_a	ZQ0_a	VDDQ_a/b	DQ28_b	DQ29_b	DQ30_b	DQ31_b	VDD2_a/b	B
C	VSS_a/b	VSS_a/b	VDD2_a/b	VSS_a/b	CA1_a	CA4_a	CKE0_a	CK_c_a	CA5_a	CA8_a	ZQ1_a	VDDQ_a/b	DQ24_b	DQ25_b	DQ26_b	DQ27_b	VDD2_a/b	C
D	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	CA2_a	CSB0_a	CKE1_a	RFU	CA6_a	CA9_a	RFU	VSS_a/b	DQ15_b	DM3_b	DQS3_c_b	DQS3_t_b	VSS_a/b	D
E	VDDCA_a/b	ZQ0_b	ZQ1_b	RFU	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	DQ11_b	DQ12_b	DQ13_b	DQ14_b	VDDQ_a/b	E
F	VSS_a/b	CA7_b	CA8_b	CA9_b	VSS_a/b							VSS_a/b	DM1_b	DQ8_b	DQ9_b	DQ10_b	VSS_a/b	F
G	VSS_a/b	VDDCA_a/b	CA5_b	CA6_b	VSS_a/b							VDDQ_a/b	DQS1_c_b	DQS1_t_b	VSS_a/b	VSS_a/b	VDDQ_a/b	G
H	VDD2_a/b	CK_c_b	CK_t_b	RFU	VSS_a/b							VSS_a/b	ODT_b	DM0_b	VSS_a/b	VDD2_a/b	Vref(DQ)_b	H
J	Vref(CA)_b	CSB1_b	CKE0_b	CKE1_b	VSS_a/b							RFU	DQS0_c_b	DQS0_t_b	DQ6_b	DQ7_b	VSS_a/b	J
K	VDDCA_a/b	CA3_b	CA4_b	CSB0_b	VSS_a/b							VDDQ_a/b	DQ2_b	DQ3_b	DQ4_b	DQ5_b	VDDQ_a/b	K
L	VDD2_a/b	CA0_b	CA1_b	CA2_b	VSS_a/b							VSS_a/b	DQ23_b	DM2_b	DQ0_b	DQ1_b	VDDQ_a/b	L
M	VSS_a/b	VDDQ_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	RFU	VDDQ_a/b	VSS_a/b	VDDQ_a/b	DQ21_b	DQ22_b	DQS2_c_b	DQS2_t_b	VSS_a/b	M
N	VDDQ_a/b	DQ19_a	DQ23_a	DQ0_a	DQ4_a	DM0_a	DQS0_c_a	ODT_a	DQS1_c_a	DQ13_a	DQ24_a	DQ25_a	VSS_a/b	DQ18_b	DQ19_b	DQ20_b	VSS_a/b	N
P	VSS_a/b	DQ18_a	DQ22_a	DM2_a	DQ3_a	DQ7_a	DQS0_t_a	DM1_a	DQS1_t_a	DQ12_a	DM3_a	DQ26_a	DQ29_a	VSS_a/b	DQ16_b	DQ17_b	VDDQ_a/b	P
R	VDD1_a/b	DQ17_a	DQ21_a	DQS2_c_a	DQ2_a	DQ6_a	VSS_a/b	VSS_a/b	DQ9_a	DQ11_a	DQ15_a	DQS3_c_a	DQ28_a	DQ31_a	VDD2_a/b	VSS_a/b	VSS_a/b	R
T	VDD1_a/b	DQ16_a	DQ20_a	DQS2_t_a	DQ1_a	DQ5_a	VSS_a/b	VDD2_a/b	DQ8_a	DQ10_a	DQ14_a	DQS3_t_a	DQ27_a	DQ30_a	VSS_a/b	VDD1_a/b	VSS_a/b	T
U	NC	VDD2_a/b	VDD2_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VDDQ_a/b	Vref(DQ)_a	VSS_a/b	VDDQ_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	NC	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

NOTE 1 Pins E4, H4, D8, M9, and J12 are reserved as "RFU"s.

NOTE 2 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to GND in the package.

NOTE 3 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
- ZQ1 is NC.

NOTE 4 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).

2.2.2 178-Ball Discrete Single-Channel FBGA (top view) MO TBD

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ0	ZQ1	VSS	VSSQ		DQ31 NC	DQ30 NC	DQ29 NC	DQ28 NC	VSSQ	DNU	B
C		CA9	VSSCA	NC	VSS	VSSQ		DQ27 NC	DQ26 NC	DQ25 NC	DQ24 NC	VDDQ		C
D		CA8	VSSCA	VDD2	VDD2	VDD2		DM3 NC	DQ15	DQS3_t NC	DQS3_c NC	VSSQ		D
E		CA7	CA6	VSS	VSS	VSSQ		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSSCA	VSS	VSSQ		DQ11	DQ10	DQ9	DQ8	VSSQ		F
G		VDDCA	VSSCA	VSSCA	VDD2	VSSQ		DM1	VSSQ	DQS1_t	DQS1_c	VDDQ		G
H		VSS	VDDCA	Vref(CA)	VDD2	VDD2		VDDQ	VDDQ	VSSQ	VDDQ	VDD2		H
J		CK_c	CK_t	VSSCA	VDD2	VDD2		ODT	VDDQ	VDDQ	Vref(DQ)	VSS		J
K		VSS	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	VSSQ	VDDQ	VDD2		K
L		VDDCA	CS0_n	CS1_n	VDD2	VSS		DM0	VSSQ	DQS0_t	DQS0_c	VDDQ		L
M		VDDCA	CA4	VSSCA	VSS	VSSQ		DQ4	DQ5	DQ6	DQ7	VSSQ		M
N		CA2	CA3	VSS	VSS	VSSQ		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSSCA	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t NC	DQS2_c NC	VSSQ		P
R		CA0	NC	VSS	VSS	VSSQ		DQ20 NC	DQ21 NC	DQ22 NC	DQ23 NC	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSSQ		DQ16 NC	DQ17 NC	DQ18 NC	DQ19 NC	VSSQ	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTE 1 When using the x16 configuration DQ16 through DQ31 become NC as indicated by the second row of signal names for those signals in the ball-out diagram.
NOTE 2 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), x16/x32, 17 rows
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 See JESD21-C, Section 3.12.1
NOTE 5 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to GND in the package.
NOTE 6 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC

NOTE 7 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).

2.2.3 346-ball 0.5mm Pitch Dual-Channel Multi-Chip Package (MCP) FBGA (top view) MO TBD

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A				NC			NC				NC				NC			NC			
B																					
C	NC		DNU	DNU	CLEn NCm	VCCn VCCQm	R/B0n DATA5m	VCCn VCCQm	R/B1n CLKm	VCCn VCCQm	CEB1n RSTm	VCCn VCCQm	CEB0n NCm	VCCn VCCQm	REBn VCCm	VCCn VCCm	VSSn VSSm	DNU	DNU		NC
D			DNU	NCn VCCQm	WEBn NCm	VSSn VSSQm	IO6n DAT1m	VSSn VSSQm	IO4n DAT2m	VSSn VSSQm	IO2n NCm	VSSn VSSQm	IO0n NCm	VSSn VSSQm	ALEn VCCm	VSSn VSSm	VSSn VSSm	NCn NCm	DNU		
E			VCCn VCCm	NCn VSSQm	VCCn VCCm	NCn VSSQm	IO14n DAT4m	NCn VSSQm	IO12n DAT6m	NCn VSSQm	IO10n NCm	NCn VSSQm	IO8n NCm	NCn VDDIm	WPBn VCCm	NCn NCm	NCn NCm	NCn NCm	NCn NCm		
F			VCCn VCCm	VSSn VSSm	VCCn VCCm	NCn VSSQm	IO7n DAT0m	NCn VSSQm	IO5n DAT3m	NCn VSSQm	IO3n NCm	NCn VSSQm	IO1n NCm	NCn NCm	NCn NCm	NCn NCm	NCn NCm	NCn NCm	NCn NCm		
G			VSSn VSSm	VSSn VSSm		NCn NCm	IO15n CMDm			IO13n DAT7m	IO11n NCm	IO9n NCm			NCn NCm	NCn NCm		NCn NCm	NCn NCm		
H																					
J																					
K																					
L			NC	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VDDCA_a/b	VDD2_a/b	VSS_a/b	VDDCA_a/b	Vref(CA)_a	VDD2_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VDD1_a/b	VDD1_a/b	NC		
M			VSS_a/b	VDD1_a/b	VSS_a/b	VSS_a/b	CA0_a	CA3_a	CSB1_a	CK_t_a	VDDCA_a/b	CA7_a	ZQ0_a	VDDQ_a/b	DQ28_b	DQ29_b	DQ30_b	DQ31_b	VDD2_a/b		
N			VSS_a/b	VSS_a/b	VDD2_a/b	VSS_a/b	CA1_a	CA4_a	CKE0_a	CK_c_a	CA5_a	CA8_a	ZQ1_a	VDDQ_a/b	DQ24_b	DQ25_b	DQ26_b	DQ27_b	VDD2_a/b		
P			VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	CA2_a	CSB0_a	CKE1_a	RFU	CA6_a	CA9_a	RFU	VSS_a/b	DQ15_b	DM3_b	DQS3_c_b	DQS3_t_b	VSS_a/b		
R			VDDCA_a/b	ZQ0_b	ZQ1_b	RFU	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VSS_a/b	DQ11_b	DQ12_b	DQ13_b	DQ14_b	VDDQ_a/b		
T			VSS_a/b	CA7_b	CA8_b	CA9_b	VSS_a/b							VSS_a/b	DM1_b	DQ8_b	DQ9_b	DQ10_b	VSS_a/b		
U			VSS_a/b	VDDCA_a/b	CA5_b	CA6_b	VSS_a/b							VDDQ_a/b	DQS1_c_b	DQS1_t_b	VSS_a/b	VSS_a/b	VDDQ_a/b		
V			VDD2_a/b	CK_c_b	CK_t_b	RFU	VSS_a/b							VSS_a/b	ODT_b	DM0_b	VSS_a/b	VDD2_a/b	Vref(DQ)_b		
W			Vref(CA)_b	CSB1_b	CKE0_b	CKE1_b	VSS_a/b							RFU	DQS0_c_b	DQS0_t_b	DQ6_b	DQ7_b	VSS_a/b		
Y			VDDCA_a/b	CA3_b	CA4_b	CSB0_b	VSS_a/b							VDDQ_a/b	DQ2_b	DQ3_b	DQ4_b	DQ5_b	VDDQ_a/b		
AA			VDD2_a/b	CA0_b	CA1_b	CA2_b	VSS_a/b							VSS_a/b	DQ23_b	DM2_b	DQ0_b	DQ1_b	VDDQ_a/b		
AB			VSS_a/b	VDDQ_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	RFU	VDDQ_a/b	VSS_a/b	VDDQ_a/b	DQ21_b	DQ22_b	DQS2_c_b	DQS2_t_b	VSS_a/b		
AC			VDDQ_a/b	DQ19_a	DQ23_a	DQ0_a	DQ4_a	DM0_a	DQS0_c_a	ODT_a	DQS1_c_a	DQ13_a	DQ24_a	DQ25_a	VSS_a/b	DQ18_b	DQ19_b	DQ20_b	VSS_a/b		
AD			VSS_a/b	DQ18_a	DQ22_a	DM2_a	DQ3_a	DQ7_a	DQS0_t_a	DM1_a	DQS1_t_a	DQ12_a	DM3_a	DQ26_a	DQ29_a	VSS_a/b	DQ16_b	DQ17_b	VDDQ_a/b		
AE			VDD1_a/b	DQ17_a	DQ21_a	DQS2_c_a	DQ2_a	DQ6_a	VSS_a/b	VSS_a/b	DQ9_a	DQ11_a	DQ15_a	DQS3_c_a	DQ28_a	DQ31_a	VDD2_a/b	VSS_a/b	VSS_a/b		
AF			VDD1_a/b	DQ16_a	DQ20_a	DQS2_t_a	DQ1_a	DQ5_a	VSS_a/b	VDD2_a/b	DQ8_a	DQ10_a	DQ14_a	DQS3_t_a	DQ27_a	DQ30_a	VSS_a/b	VDD1_a/b	VSS_a/b		
AG	NC		NC	VDD2_a/b	VDD2_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VDDQ_a/b	Vref(DQ)_a	VSS_a/b	VDDQ_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	VDDQ_a/b	VSS_a/b	VSS_a/b	NC		NC
AH																					
AJ				NC			NC				NC				NC			NC			

NOTE 1 0.5mm ball pitch, 346 ball count

NOTE 2 Target package sizes : 12mm x 16mm and 14mm x 18mm

NOTE 3 Target package, size depends on Flash density.

NOTE 4 Top view, A1 in top left corner

NOTE 5 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to GND in the package.

NOTE 6 For channel using x32 DRAM
- ZQ0 is connected to R0 DRAM and R1 DRAM (if present)
- ZQ1 is NC

NOTE 7 For channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of R0 DRAM and R1 DRAM (if present)
- ZQ1 is connected to Byte 2-3 of R0 DRAM and R1 DRAM (if present)

NOTE 8 For flash ball-out, “n” ball assignments are used for NAND flash, and “m” ball assignments for e-MMC.

2.3 LPDDR3 Pad Sequence

Table 1 — LPDDR3 Pad Sequence

CA Pad Seq	DQ Pad Sequence	
	x32	x16
VDD2	VDD2	VDD2
VSS	VSS	VSS
VSS	VSS *1	VSS *1
VDD1	VDD1	VDD1
VDD2	VDDQ	
VSS	VSSQ	
	DQ31	
	DQ30	
	VDDQ	
	DQ29	
	DQ28	
	VSSQ	
	DQ27	
	DQ26	
	VDDQ	
	DQ25	
	DQ24	
	VSSQ	
	DQS3_t	
	DQS3_c	
	VDDQ	
	DM3	
	VSSQ	VSSQ
	DQ15	DQ15
	DQ14	DQ14
	VDDQ	VDDQ
	DQ13	DQ13
	DQ12	DQ12
	VSSQ	VSSQ
	DQ11	DQ11
	DQ10	DQ10
	VDDQ	VDDQ
ZQ	DQ9	DQ9
CA9	DQ8	DQ8
CA8	VSSQ	VSSQ
VSSCA	DQS1_t	DQS1_t
VDDCA	DQS1_c	DQS1_c
CA7	VDDQ	VDDQ
CA6	DM1	DM1
CA5	VSSQ	VSSQ
	VDDQ	VDDQ
VDD2	VDD2	VDD2
Vref(CA)	ODT	ODT
VSS	VSS	VSS
VDDCA	Vref(DQ)	Vref(DQ)
CK_c		
CK_t		
VSSCA	VSS	VSS
CKE	VDD2	VDD2
CS_N		
CA4	VDDQ	VDDQ
CA3	VSSQ	VSSQ
CA2	DM0	DM0
VDDCA	VDDQ	VDDQ
VSSCA	DQS0_c	DQS0_c
CA1	DQS0_t	DQS0_t
CA0	VSSQ	VSSQ
	DQ7	DQ7
	DQ6	DQ6
	VDDQ	VDDQ
	DQ5	DQ5
	DQ4	DQ4
	VSSQ	VSSQ
	DQ3	DQ3
	DQ2	DQ2
	VDDQ	VDDQ
	DQ1	DQ1
	DQ0	DQ0
	VSSQ	VSSQ
	DM2	
	VDDQ	
	DQS2_c	
	DQS2_t	
	VSSQ	
	DQ23	
	DQ22	
	VDDQ	
	DQ21	
	DQ20	
	VSSQ	
	DQ19	
	DQ18	
	VDDQ	
	DQ17	
	DQ16	
	VSSQ	
VSS	VDDQ	
VDD2		
VDD1	VDD1	VDD1
VSS	VSS *1	VSS *1
VSS	VSS	VSS
VDD2	VDD2	VDD2

NOTE 1 Pads with (*1) are optional.

NOTE 2 Ordering of DQ bits shall be maintained in the system, including within the package and on the PCB. DQ byte swapping and DQ bit Swapping are not allowed in the system.

NOTE 3 CA pads and DQ pads shall be separated on opposite sides of die from top of silicon view.

2.4 LPDDDR3 Pad Definition and Description

Table 2 — Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	**On-Die Termination**: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{SSQ}	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE 1 Data includes DQ and DM.

3 LPDDR3 Functional Description

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:

4 Gb has 4,294,967,296 bits
8 Gb has 8,589,934,592 bits
16 Gb has 17,179,869,184 bits
32 Gb has 34,359,738,368 bits

LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an $8n$ prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single $8n$-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 LPDDR3 SDRAM Addressing

Table 3 — LPDDR3 SDRAM Addressing

Items		4Gb	8Gb	16Gb	32Gb
Number of Banks		8	8	8	TBD
Bank Addresses		BA0-BA2	BA0-BA2	BA0-BA2	TBD
t_{REFI}(us)[2]		3.9	3.9	3.9	TBD
x16	Row Addresses	R0-R13	R0-R14	R0-R14	TBD
	Column Addresses[1]	C0-C10	C0-C10	C0-C11	TBD
x32	Row Addresses	R0-R13	R0-R14	R0-R14	TBD
	Column Addresses[1]	C0-C9	C0-C9	C0-C10	TBD

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 2 t_{REFI} values for all bank refresh is Tc = -25~85 °C, Tc means Operating Case Temperature

NOTE 3 Row and Column Address values on the CA bus that are not used are “don’t care.”

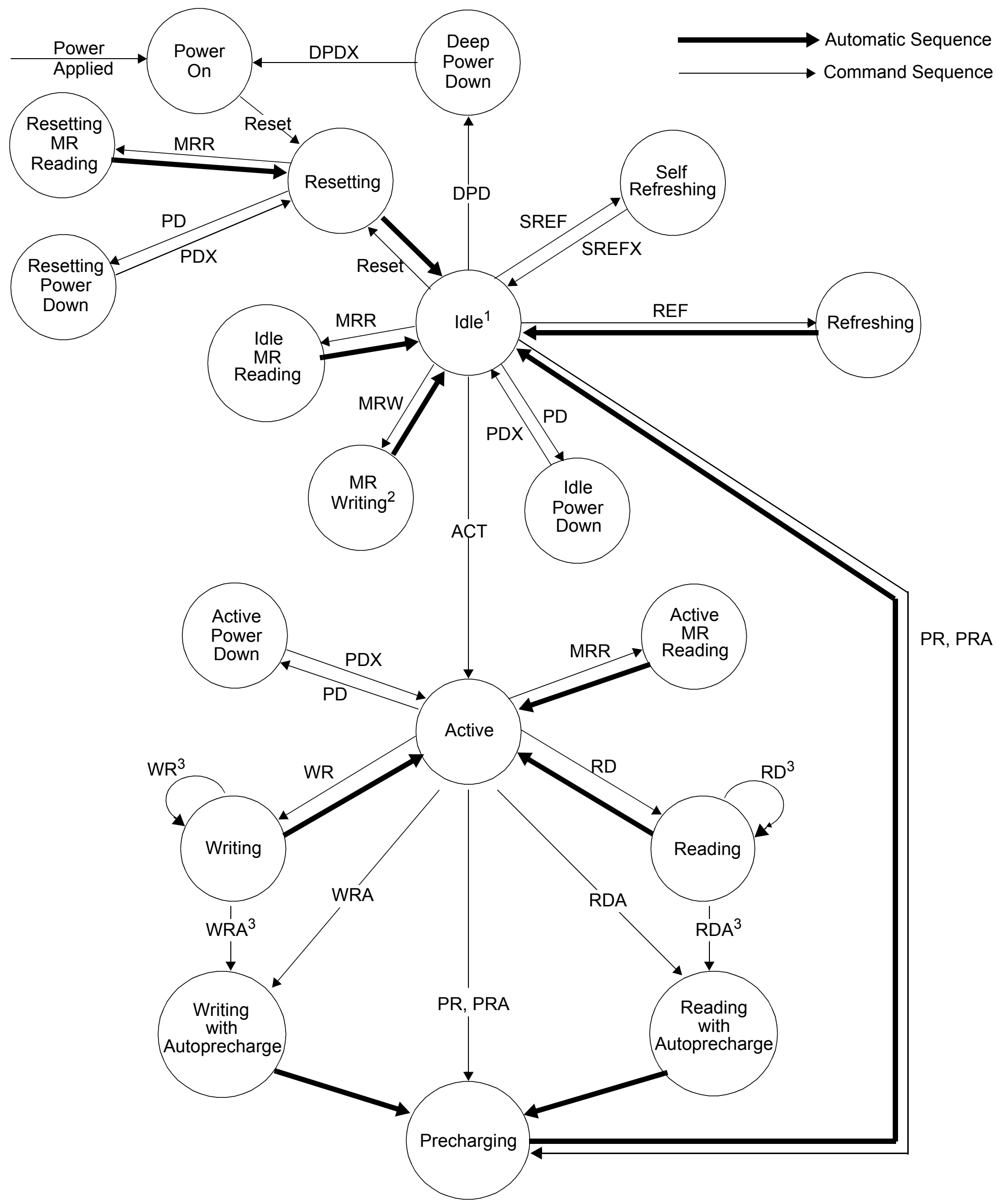
3.2 Simplified LPDDR3 State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see "LPDDR3 Command Definitions and Timing Diagrams" on page 25.

3.2 Simplified LPDDR3 State Diagram (cont'd)



ACT = Activate
PR(A) = Precharge (All)
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
MRW = Mode Register Write
MRR = Mode Register Read
Reset = Reset is achieved through MRW command

PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Figure 1 — LPDDR3: Simplified Bus Interface State Diagram

NOTE 1 In the Idle state, all banks are precharged.

NOTE 2 In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections "CA Training" or "Write Leveling".

NOTE 3 Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.

NOTE 4 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

3.3 Power-up, Initialization, and Power-off

3.3.1 Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp: While applying power (after Ta), CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table 4.

Table 4 — Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{Ref} must always be less than all other supply voltages

NOTE 1 Ta is the point when any power supply first reaches 300mV.
NOTE 2 Noted conditions apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined operating ranges.
NOTE 4 Power ramp duration t_{INIT0} (Tb - Ta) must not exceed 20ms.
NOTE 5 The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Beginning at Tb, CKE must remain LOW for at least t_{INIT1}, after which CKE can be asserted HIGH. The clock must be stable at least t_{INIT2} prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS_n, and CA inputs must observe setup and hold requirements (t_{IS}, t_{IH}) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for t_{CKb}. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least t_{INIT3} (Td). The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{ZQINIT}.

2. RESET Command: After t_{INIT3} is satisfied, the MRW RESET command must be issued (Td).

An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time t_{INIT4}.

3. MRRs and Device Auto Initialization (DAI) Polling: After t_{INIT4} is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of t_{INIT5}, or until the DAI bit is set before proceeding. As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than t_{INIT5} after the RESET command. The controller must wait at least t_{INIT5} or until the DAI bit is set before proceeding.

3.3 Power-up, Initialization, and Power-off (cont'd)

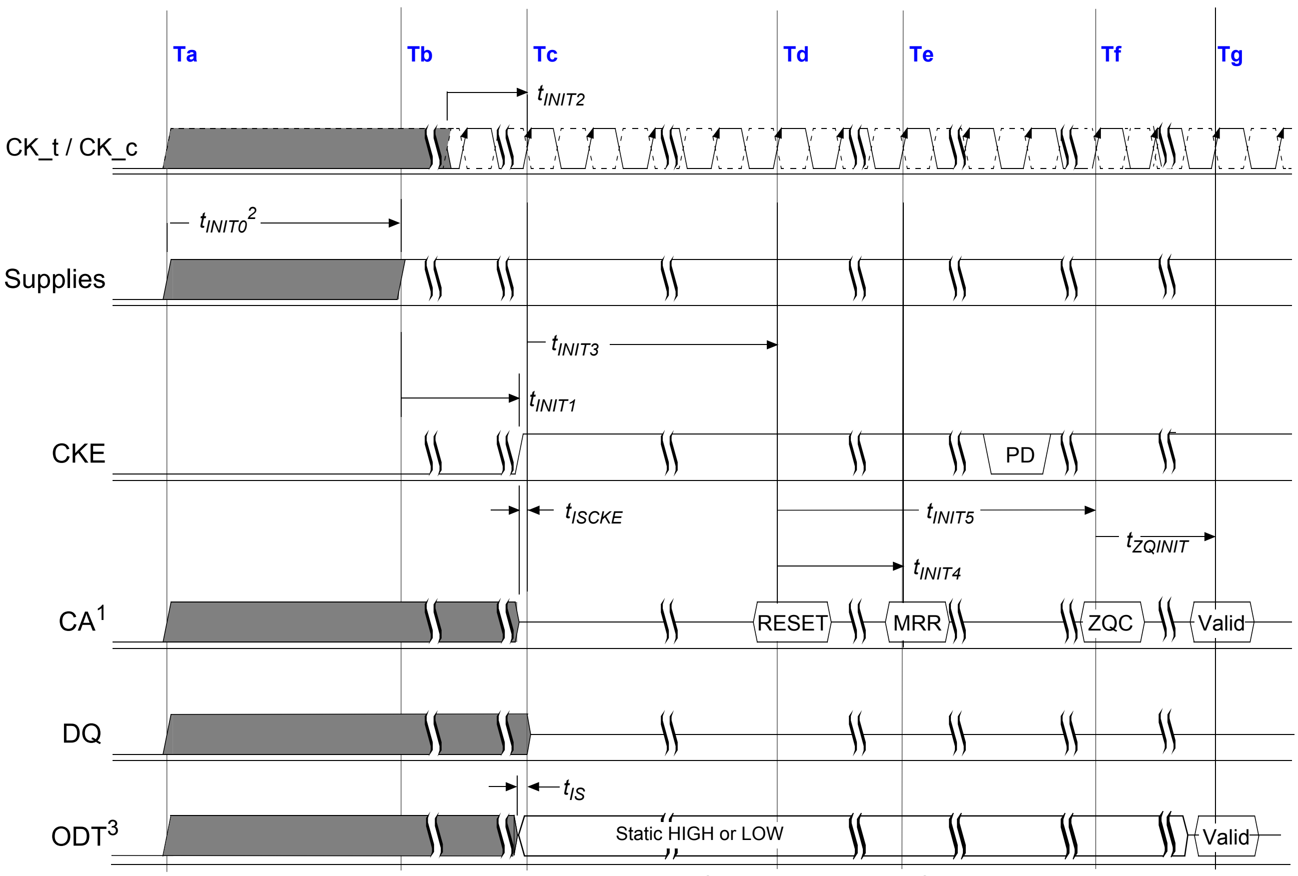
4. ZQ Calibration: After reaching Tf, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after t_{ZQINIT}.

5. Normal Operation: After t_{ZQINIT} (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification.

Figure 2 — Voltage Ramp and Initialization Sequence



* Midlevel on CA bus means: valid NOP

NOTE 1 High-Z on the CA bus indicates NOP.

NOTE 2 For t_{INIT} values, see Table 5.

NOTE 3 After RESET command (time Te), R_{TT} is disabled until ODT function is enabled by MRW to MR11 following Tg.

3.3 Power-up, Initialization, and Power-off (cont'd)

Table 5 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	–	20	ms	Maximum voltage-ramp time
t_{INIT1}	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
t_{INIT2}	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
t_{INIT3}	200	–	µs	Minimum idle time after first CKE assertion
t_{INIT4}	1	–	µs	Minimum idle time after RESET command
t_{INIT5}	–	10	µs	Maximum duration of device auto initialization
t_{ZQINIT}	1	–	µs	ZQ initial calibration
t_{CKb}	18	100	ns	Clock cycle time during boot

3.3.1.1 Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

3.3.2 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see Table 1).

Table 6 — Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDCA}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDQ}—200mV
Tx and Tz	V_{REF} must always be less than all other supply voltages

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

3.3.2.1 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

3.3 Power-up, Initialization, and Power-off (cont'd)

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 7 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

3.4 Mode Register Definition

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM

Table 8 shows the mode registers for LPDDR3 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 8 — Mode Register Assignment in LPDDR3 SDRAM

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	**00_H**	Device Info.	R	RL3	(RFU)		RZQI (optional)		(RFU)		DAI	**go to MR0**
1	**01_H**	Device Feature 1	W	*n*WR (for AP)			(RFU)		BL			**go to MR1**
2	**02_H**	Device Feature 2	W	WR Lev	(RFU)		*n*WRE	RL & WL				**go to MR2**
3	**03_H**	I/O Config-1	W	(RFU)				DS				**go to MR3**
4	**04_H**	Refresh Rate	R	TUF	(RFU)				Refresh Rate			**go to MR4**
5	**05_H**	Basic Config-1	R	LPDDR3 Manufacturer ID								**go to MR5**
6	**06_H**	Basic Config-2	R	Revision ID1								**go to MR6**
7	**07_H**	Basic Config-3	R	Revision ID2								**go to MR7**
8	**08_H**	Basic Config-4	R	I/O width		Density				Type		**go to MR8**
9	**09_H**	Test Mode	W	Vendor-Specific Test Mode								**go to MR9**
10	**$0A_H$**	IO Calibration	W	Calibration Code								**go to MR10**
11	**$0B_H$**	ODT Feature		(RFU)					PD CTL	DQ ODT		**go to MR11**
12:15	**$0C_H$~$0F_H$**	(reserved)		(RFU)								**go to MR12**
16	**10_H**	PASR_Bank	W	PASR Bank Mask								**go to MR16**
17	**11_H**	PASR_Seg	W	PASR Segment Mask								**go to MR17**
18-31	**12_H-$1F_H$**	(Reserved)		(RFU)								**go to MR18**
32	**20_H**	DQ Calibration Pattern A	R	See “DQ Calibration” on page 53								**go to MR32**
33:39	**21_H~27_H**	(Do Not Use)										**go to MR33**
40	**28_H**	DQ Calibration Pattern B	R	See “DQ Calibration” on page 53								**go to MR40**
41	**29_H**	CA Training 1	W	See “Mode Register Write - CA Training Mode” on page 57								**go to MR41**
42	**$2A_H$**	CA Training 2	W	See “Mode Register Write - CA Training Mode” on page 57								**go to MR42**
43:47	**$2B_H$~$2F_H$**	(Do Not Use)										**go to MR43**
48	**30_H**	CA Training 3	W	See “Mode Register Write - CA Training Mode” on page 57								**go to MR48**
49:62	**31_H~$3E_H$**	(Reserved)		(RFU)								**go to MR49**
63	**$3F_H$**	Reset	W	X								**go to MR63**
64:255	**40_H~FF_H**	(Reserved)		(RFU)								**go to MR64**

NOTE 1 RFU bits shall be set to ‘0’ during mode register writes.
NOTE 2 RFU bits shall be read as ‘0’ during mode register reads.
NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
NOTE 4 All mode registers that are specified as RFU shall not be written.
NOTE 5 See vendor device datasheets for details on vendor-specific mode registers.
NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont’d)

MR0_Device Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI (optional)		**(RFU)**		**DAI**

DAI (Device Auto-Initialization Status)	Read-only	OP<0>	**0_B:** DAI complete **1_B:** DAI still in progress	
RZQI (Built in Self Test for RZQ Information)	Read-only	OP<4:3>	**00_B:** RZQ self test not supported **01_B:** ZQ-pin may connect to V_{DDCA} or float **10_B:** ZQ-pin may short to GND **11_B:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DDCA} or float nor short to GND)	1-4
WL (Set B) Support	Read-only	OP<6>	**0_B**: DRAM does not support WL (Set B) **1_B**: DRAM supports WL (SetB)	WL (Set B) Option Support
RL3 Option Support	Read-only	OP<7>	**0_B**: DRAM does not support RL=3, nWR=3, WL=1 **1_B**: DRAM supports RL=3, nWR=3, WL=1 for frequencies ≤ 166	RL3 Option Support

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 2 If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for R_{ON}, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-Ω ±1%).

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR1_Device Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
*n*WR (for AP)			(RFU)		BL		

BL	**Write-only**	**OP<2:0>**	**011**$_B$**:** BL8 (default) All others: reserved	
***n*WR**	**Write-only**	**OP<7:5>**	If *n*WRE (MR2 OP<4>) = 0: **001**$_B$: *n*WR=3 (optional) **100**$_B$: *n*WR=6 **110**$_B$: *n*WR=8 **111**$_B$: *n*WR=9 If *n*WRE (MR2 OP<4> = 1: **000**$_B$: *n*WR=10 (default) **001**$_B$: *n*WR=11 **010**$_B$: *n*WR=12 All others: reserved	**1**

NOTE 1 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table 9 — Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0_B	0_B	0_B	8	0	1	2	3	4	5	6	7
0_B	1_B	0_B		2	3	4	5	6	7	0	1
1_B	0_B	0_B		4	5	6	7	0	1	2	3
1_B	1_B	0_B		6	7	0	1	2	3	4	5

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 - C0.

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR2_Device Feature 2 (MA<7:0> = 02$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	*n*WRE	RL & WL			

RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) **0001**$_B$: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) **0100**$_B$: RL = 6 / WL = 3 (≤ 400 MHz) **0110**$_B$: RL = 8 / WL = 4 (≤ 533 MHz) **0111**$_B$: RL = 9 / WL = 5 (≤ 600 MHz) **1000**$_B$: RL = 10 / WL = 6 (≤ 667 MHz, default) **1001**$_B$: RL = 11 / WL = 6 (≤ 733 MHz) **1010**$_B$: RL = 12 / WL = 6 (≤ 800 MHz) All others: reserved If OP<6> =1 (WL Set B, optional[2]) **0001**$_B$: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) **0100**$_B$: RL = 6 / WL = 3 (≤ 400 MHz) **0110**$_B$: RL = 8 / WL = 4 (≤ 533 MHz) **0111**$_B$: RL = 9 / WL = 5 (≤ 600 MHz) **1000**$_B$: RL = 10 / WL = 8 (≤ 667 MHz, default) **1001**$_B$: RL = 11 / WL = 9 (≤ 733 MHz) **1010**$_B$: RL = 12 / WL = 9 (≤ 800 MHz) All others: reserved	
*n*WRE	Write-only	OP<4>	**0**$_B$**:** enable *n*WR programming ≤ 9 **1**$_B$**:** enable *n*WR programming > 9 (default)	
WL Select	Write-only	OP<6>	**0**$_B$**:** Select WL Set A (default) **1**$_B$**:** Select WL Set B (optional[2])	
WR Leveling	Write-only	OP<7>	**0**$_B$**:** disabled (default) **1**$_B$**:** enabled	

NOTE 1 See MR0, OP<7>

NOTE 2 See MR0, OP<6>

MR3_I/O Configuration 1 (MA<7:0> = 03$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0001**$_B$**:** 34.3Ω typical pull-down/pull-up **0010**$_B$**:** 40Ω typical pull-down/pull-up (default) **0011**$_B$**:** 48Ω typical pull-down/pull-up **0100**$_B$**:** reserved for 60Ω typical pull-down/pull-up **0110**$_B$**:** reserved for 80Ω typical pull-down/pull-up **0001**$_B$**:** 34.3Ω typical pull-down, 40Ω typical pull-up **0010**$_B$**:** 40Ω typical pull-down, 48Ω typical pull-up **0011**$_B$**:** 34.3Ω typical pull-down, 48Ω typical pull-up **All others:** reserved	

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010_B:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011_B:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85°C) **100_B:** 0.5x t_{REFI}, 0.5x t_{REFIpb}, 0.5x t_{REFW}, do not de-rate SDRAM AC timing **101_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85°C.

NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

NOTE 5 SDRAM might not operate properly when OP[2:0] = 000_B or 111_B.

NOTE 6 For specified operating temperature range and maximum operating temperature refer to Table 31 on page 79.

NOTE 7 LPDDR3 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: t_{RCD}, t_{RC}, t_{RAS}, t_{RP}, and t_{RRD}. t_{DQSCK} shall be de-rated according to the t_{DQSCK} de-rating in Table 63 on page 112. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 8 See "Temperature Sensor" on page 51 for information on the recommended frequency of reading MR4.

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont’d)

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR3 Manufacturer ID							

LPDDR3 Manufacturer ID	Read-only	OP<7:0>	See JESD-TBD LPDDR3 Manufacturer ID encodings	

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR7 is vendor specific.

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR8_Basic Configuration 4 (MA<7:0> = 08B$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**11$_B$:** S8 SDRAM **all others:** Reserved	
Density	Read-only	OP<5:2>	**0110$_B$:** 4Gb **0111$_B$:** 8Gb **1000$_B$:** 16Gb **1001$_B$:** 32Gb **all others:** reserved	
I/O width	Read-only	OP<7:6>	**00$_B$:** x32 **01$_B$:** x16 **all others:** reserved	

MR9_Test Mode (MA<7:0> = 09$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
vendor-specific test mode							

MR10_Calibration (MA<7:0> = 0A$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values

NOTE 2 LPDDR3 devices shall ignore calibration command when a "Reserved" value is written into MR10.

NOTE 3 See AC timing table for the calibration latency.

NOTE 4 If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on page 55) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

NOTE 5 LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.

NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR11_ODT Control (MA<7:0> = $0B_H$:

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					PD CTL	DQ ODT	

DQ ODT	Write-only	OP<1:0>	**00_B:** Disable (Default) **01_B:** Reserved **10_B:** $R_{ZQ}/2$ **11_B:** $R_{ZQ}/1$	
PD Control	Write-only	OP<2>	**0_B:** ODT disabled by DRAM during power down (default) **1_B:** ODT enabled by DRAM during power down	

MR12:15_(Reserved) (MA<7:0> = $0C_H$-$0F_H$):

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the bank (= unmasked, default) **1_B:** refresh blocked (= masked)	1

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	**Bank 0**
1	XXXXXX1X	**Bank 1**
2	XXXXX1XX	**Bank 2**
3	XXXX1XXX	**Bank 3**
4	XXX1XXXX	**Bank 4**
5	XX1XXXXX	**Bank 5**
6	X1XXXXXX	**Bank 6**
7	1XXXXXXX	**Bank 7**

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)	

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

Segment	OP	Segment Mask	4Gb	8Gb	16Gb	32Gb
			R13:11	R14:12	R14:12	TBD
0	0	XXXXXXX1	**000_B**			
1	1	XXXXXX1X	**001_B**			
2	2	XXXXX1XX	**010_B**			
3	3	XXXX1XXX	**011_B**			
4	4	XXX1XXXX	**100_B**			
5	5	XX1XXXXX	**101_B**			
6	6	X1XXXXXX	**110_B**			
7	7	1XXXXXXX	**111_B**			

NOTE 1 This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18-31_Reserved (MA<7:0> = 012_H - $01F_H$):

MR32_DQ Calibration Pattern A (MA<7:0> = 20_H):

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on page 53.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0> = 28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on page 53.

MR41_CA Training_1 (MA<7:0> = 29_H):

Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode on page 57

MR42_CA Training_2 (MA<7:0> = $2A_H$):

Writes to MR42 exits CA Training. See Mode Register Write - CA Training Mode on page 57.

MR43:47_(Do Not Use) (MA<7:0> = $2B_H$-$2F_H$):

MR48_CA_Training_3 (MA<7:0> = 30_H):

Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode on page 57.

MR49:62_(Reserved) (MA<7:0>=31_H-$3E_H$:

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE 1 For additonal information on MRW RESET see "Mode Register Write" on page 54.

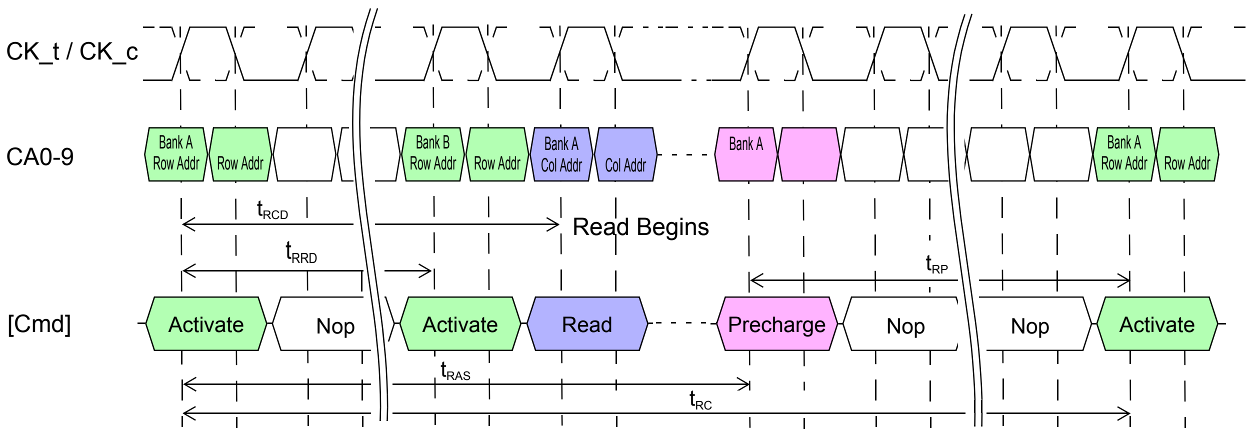
MR64:255_(Reserved) (MA<7:0> = 40_H-FF_H):

4 LPDDR3 Command Definitions and Timing Diagrams

4.1 Activate Command

The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at t_{RCD} after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between ACTIVATE commands to different banks is t_{RRD} (see Figure 1).

Figure 3 — ACTIVATE Command



2. A PRECHARGE-all command uses t_{RPab} timing, while a single-bank PRECHARGE command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

4.1.1 8-Bank Device Operation

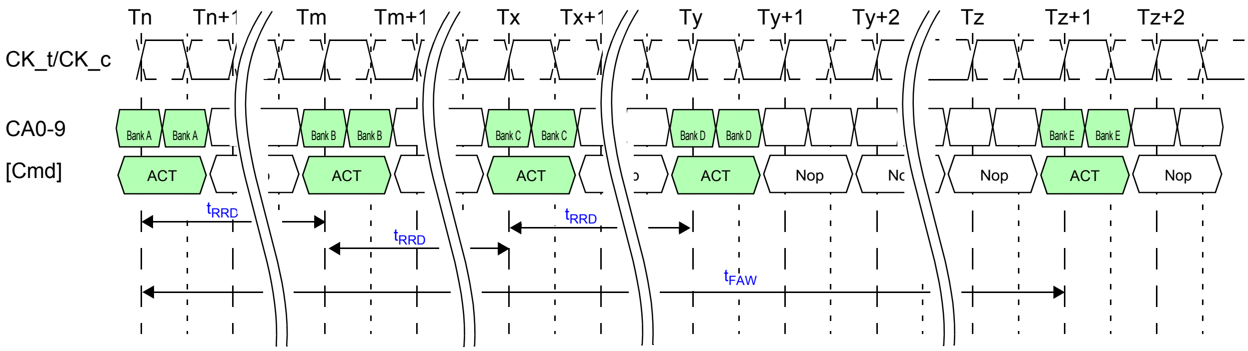
Certain restrictions on operation of the 8-bank LPDDR3 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

The 8-Bank Device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. The number of clocks in a t_{FAW} period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(t_{FAW}/t_{CK}) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock $n + 1$ and $n + 9$. REFpb also counts as bank activation for purposes of t_{FAW}. If the clock frequency is changed during the t_{FAW} period, the rolling t_{FAW} window may be calculated in clock cycles by adding up the time spent in each clock period. The t_{FAW} requirement is met when the previous n clock cycles exceeds the t_{FAW} time.

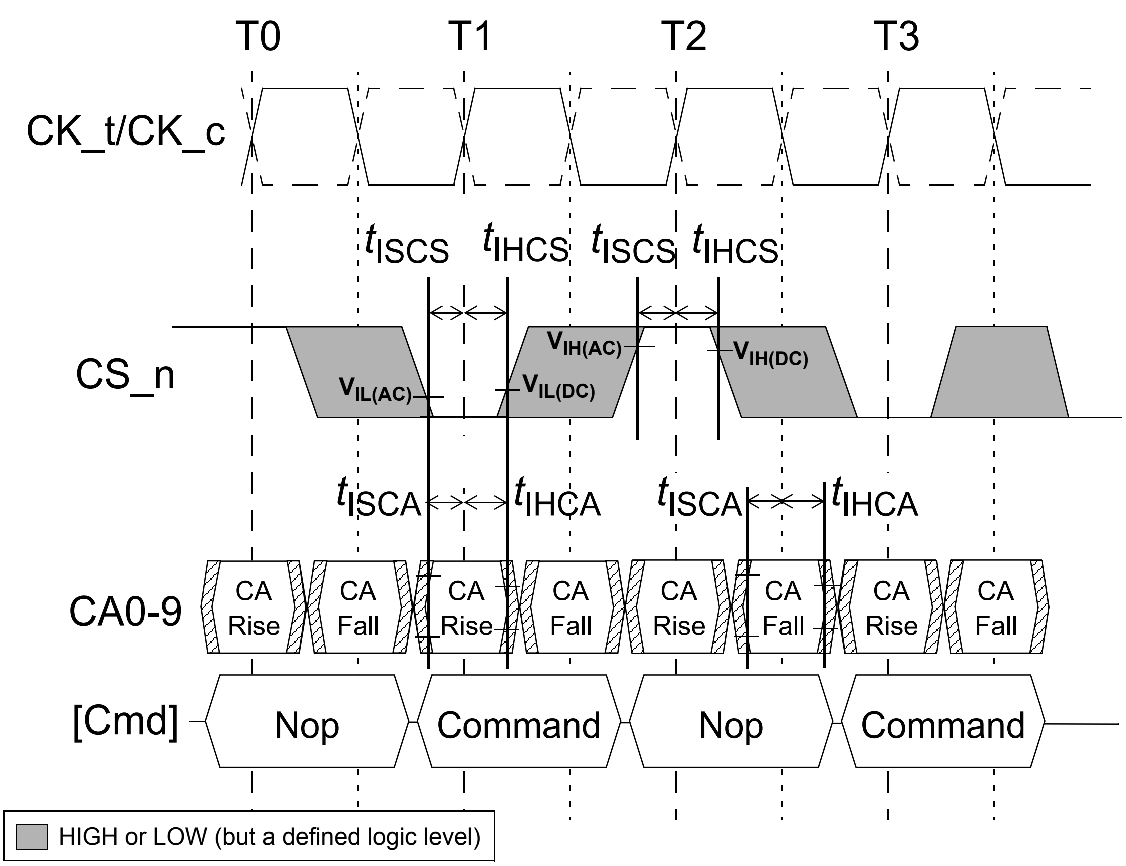
The 8-Bank Device Precharge-All Allowance: t_{RP} for a PRECHRGE ALL command must equal t_{RPab}, which is greater than t_{RPpb}.

4.1 Activate Command (cont'd)

Figure 4 — LPDDR3 t_{FAW} Timing



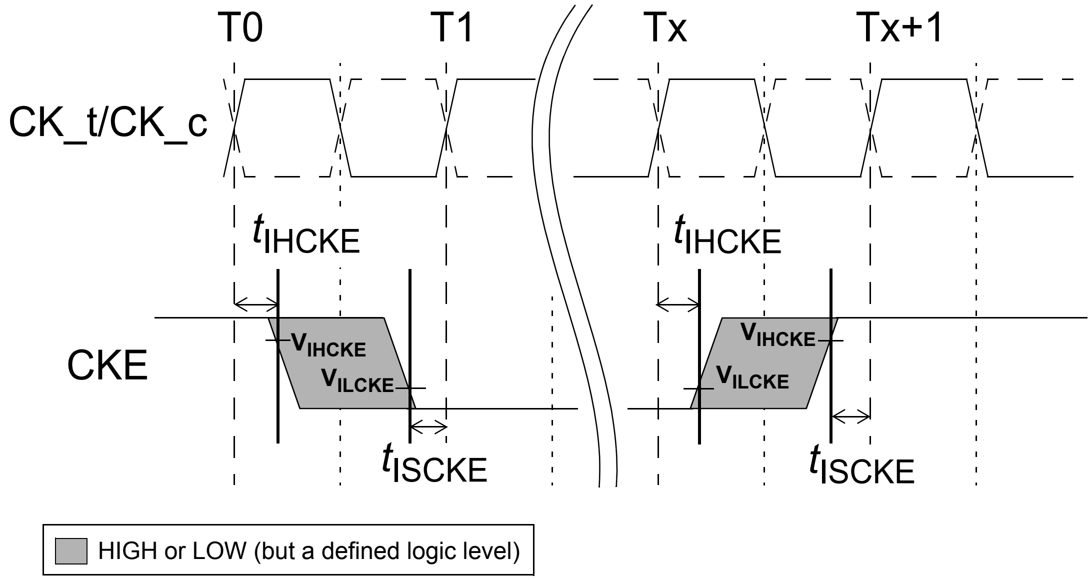
4.2 LPDDR3 Command Input Signal Timing Definition



NOTE Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 5 — LPDDR3: Command Input Setup and Hold Timing

4.2.1 LPDDR3 CKE Input Setup and Hold Timing



NOTE 1: After CKE is registered LOW, CKE signal level shall be maintained below V_{ILCKE} for t_{CKE} specification (LOW pulse width).

NOTE 2: After CKE is registered HIGH, CKE signal level shall be maintained above V_{IHCKE} for t_{CKE} specification (HIGH pulse width).

Figure 6 — LPDDR3: Command Input Setup and Hold Timing

4.3 Read and Write access modes

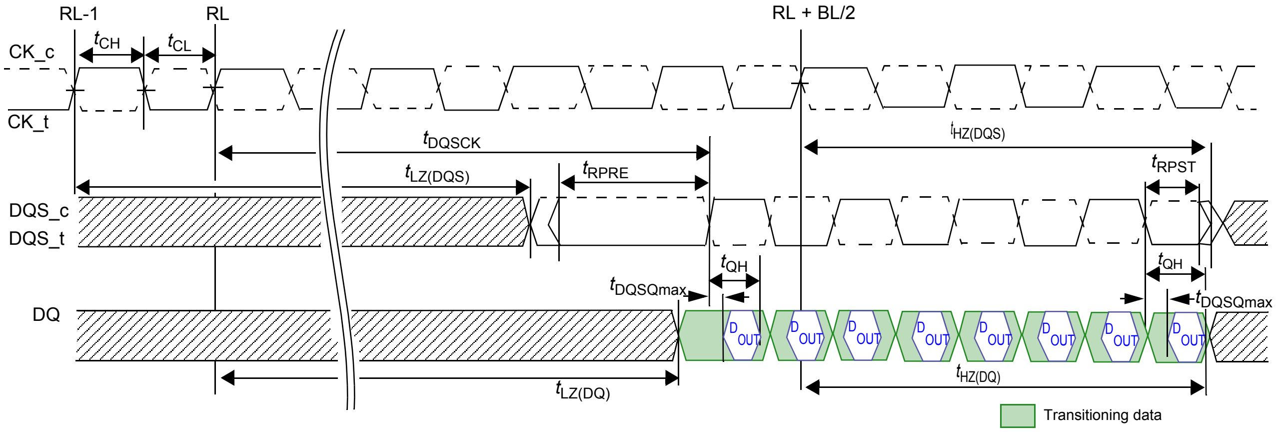
After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. Burst interrupts are not allowed.

4.4 Burst Read Operation

The burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r–CA6r and CA1f–CA9f determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid data is available RL × $t_{CK} + t_{DQSCK} + t_{DQSQ}$ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW ^{t}RPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure 7 — Read Output Timing



NOTE 1 t_{DQSCK} can span multiple clock periods.

NOTE 2 An effective burst length of 8 is shown.

4.4 Burst Read Operation (cont'd)

Figure 8 — Burst Read: RL = 12, BL = 8, t_{DQSCK} > t_{CK}

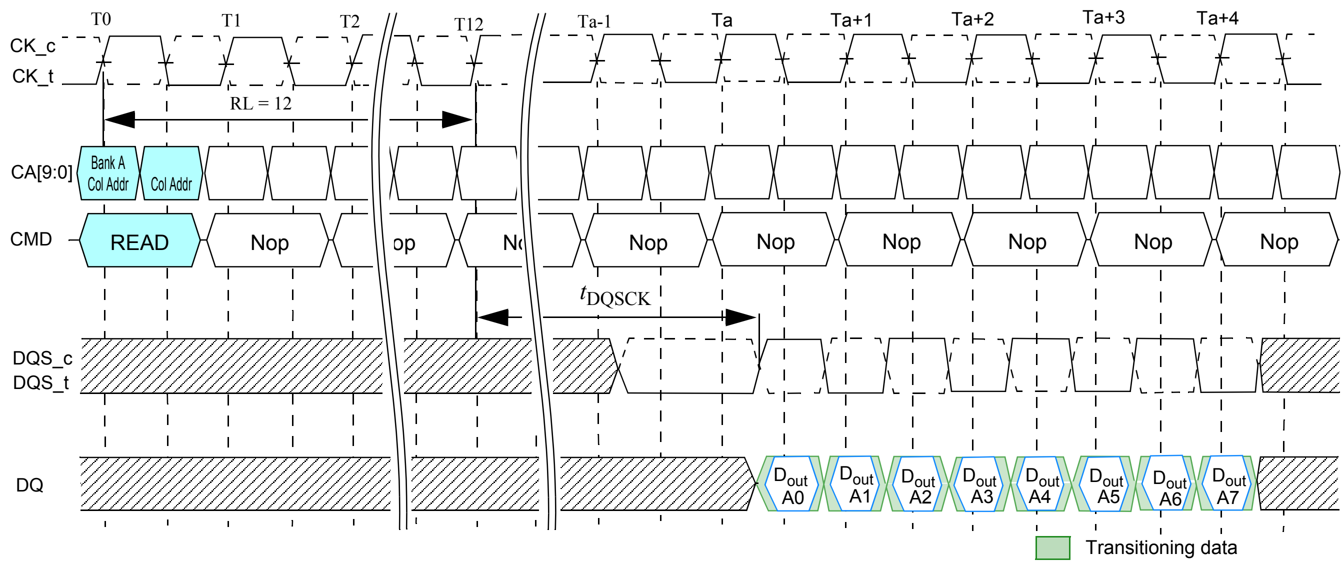
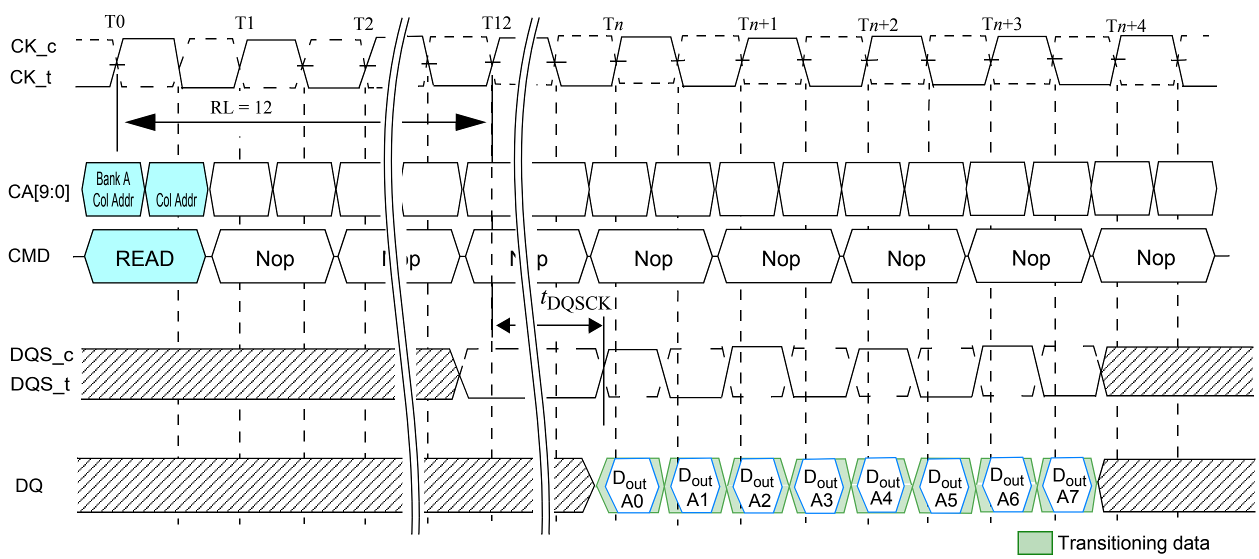


Figure 9 — Burst Read: RL = 12, BL = 8, t_{DQSCK} < t_{CK}



4.4 Burst Read Operation (cont'd)

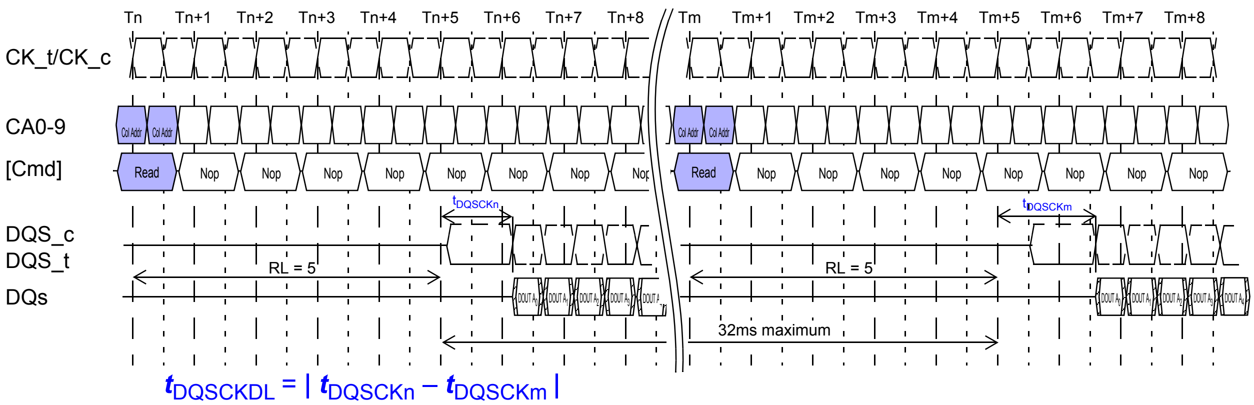


Figure 10 — LPDDR3: $t_{DQSCKDL}$ timing

NOTE 1 $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair within any 32ms rolling window.

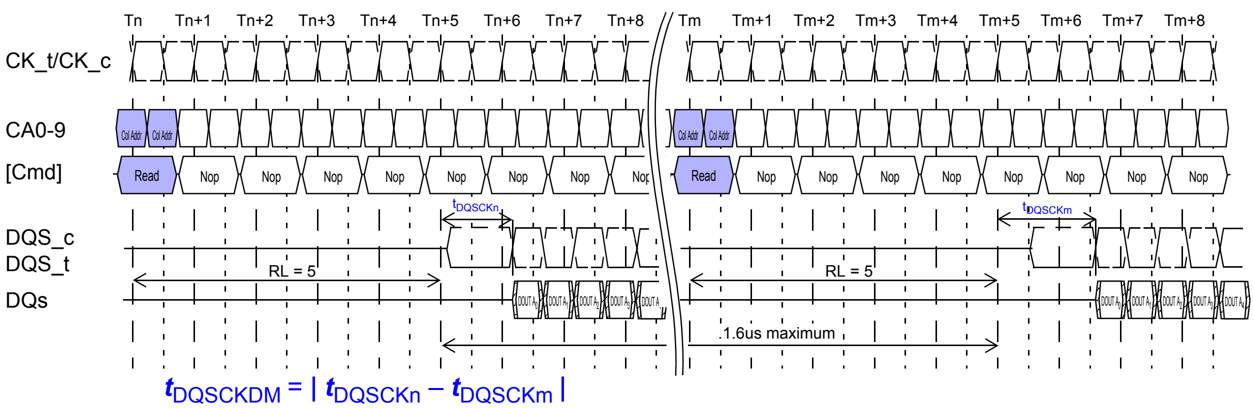


Figure 11 — LPDDR3: $t_{DQSCKDM}$ timing

NOTE 1 $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window.

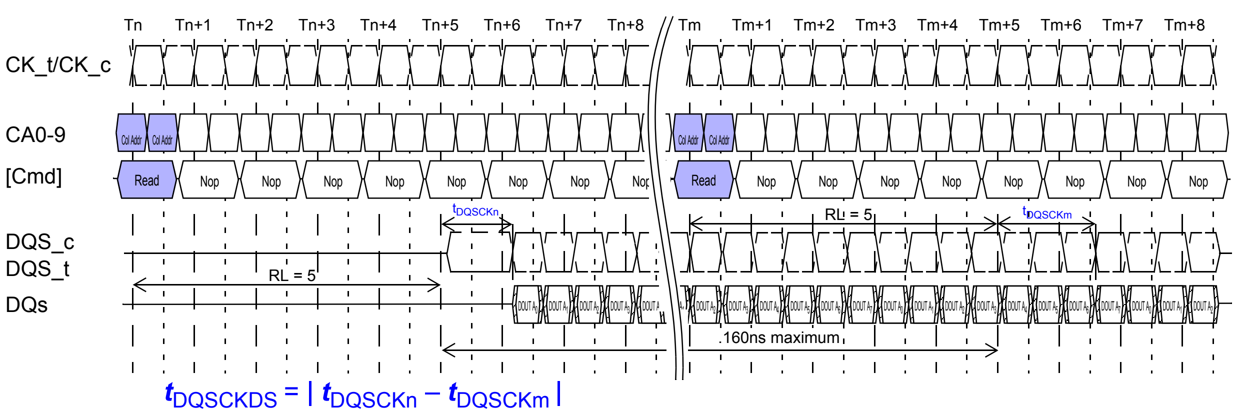
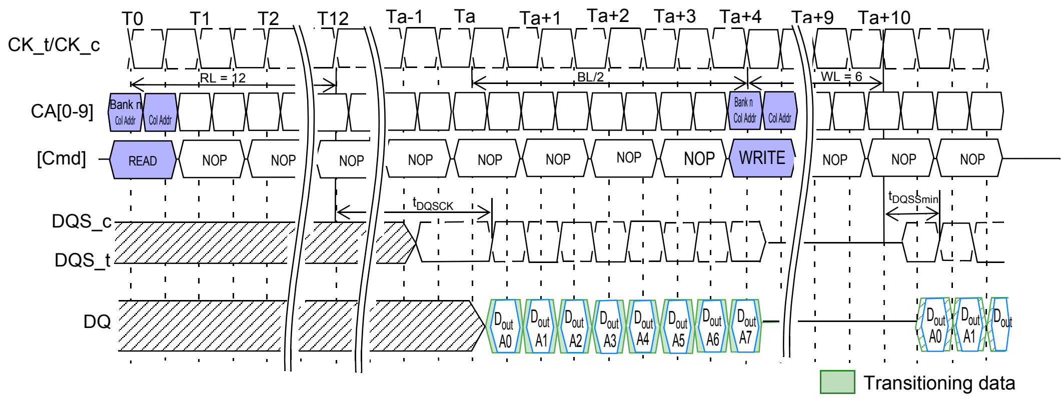


Figure 12 — LPDDR3: $t_{DQSCKDS}$ timing

NOTE 1 $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair for reads within a consecutive burst within any 160ns rolling window.

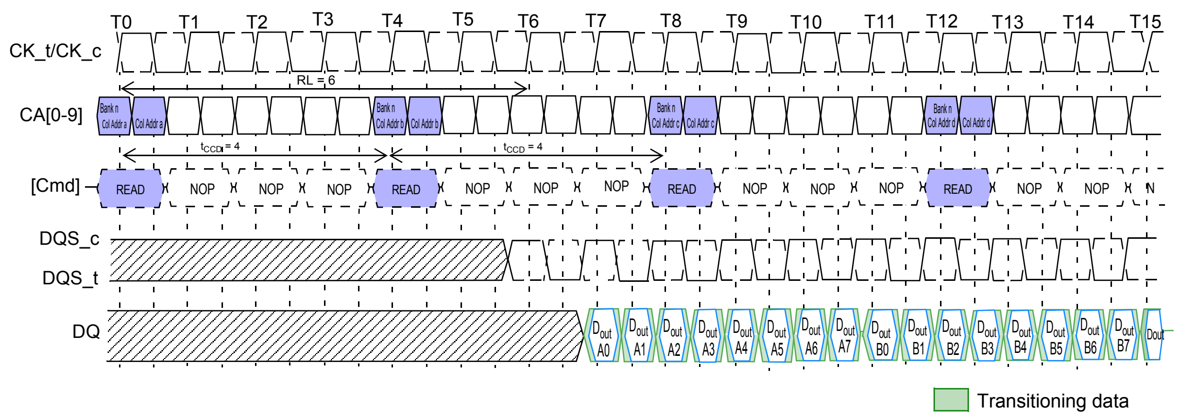
4.4 Burst Read Operation (cont'd)

Figure 13 — Burst Read Followed By Burst Write:



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 - WL clock cycles.

Figure 14 — Seamless Burst Read:



The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

4.5 Burst Write Operation

The burst WRITE command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid data must be driven WL × t_{CK} + t_{DQSS} from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW t_{WPRE} prior to data input. The burst cycle data bits must be applied to the DQ pins t_{DS} prior to the associated edge of the DQS and held valid until t_{DH} after that edge. Burst data is sampled on successive edges of the DQS until the 8-bit burst length is completed. After a burst WRITE operation, t_{WR} must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

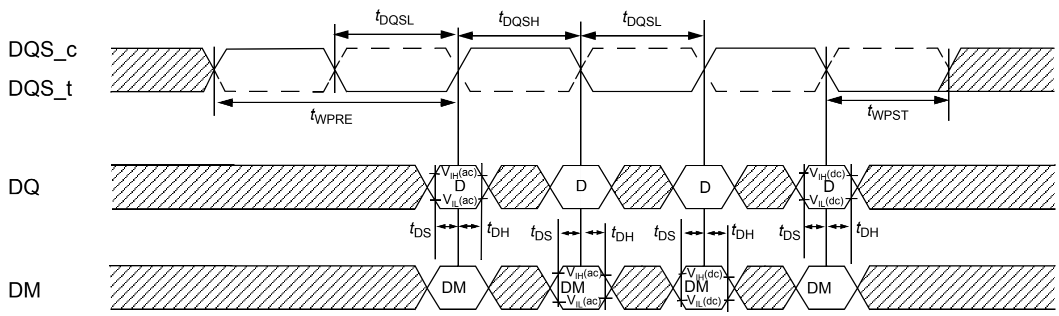


Figure 15 — Data input (write) timing

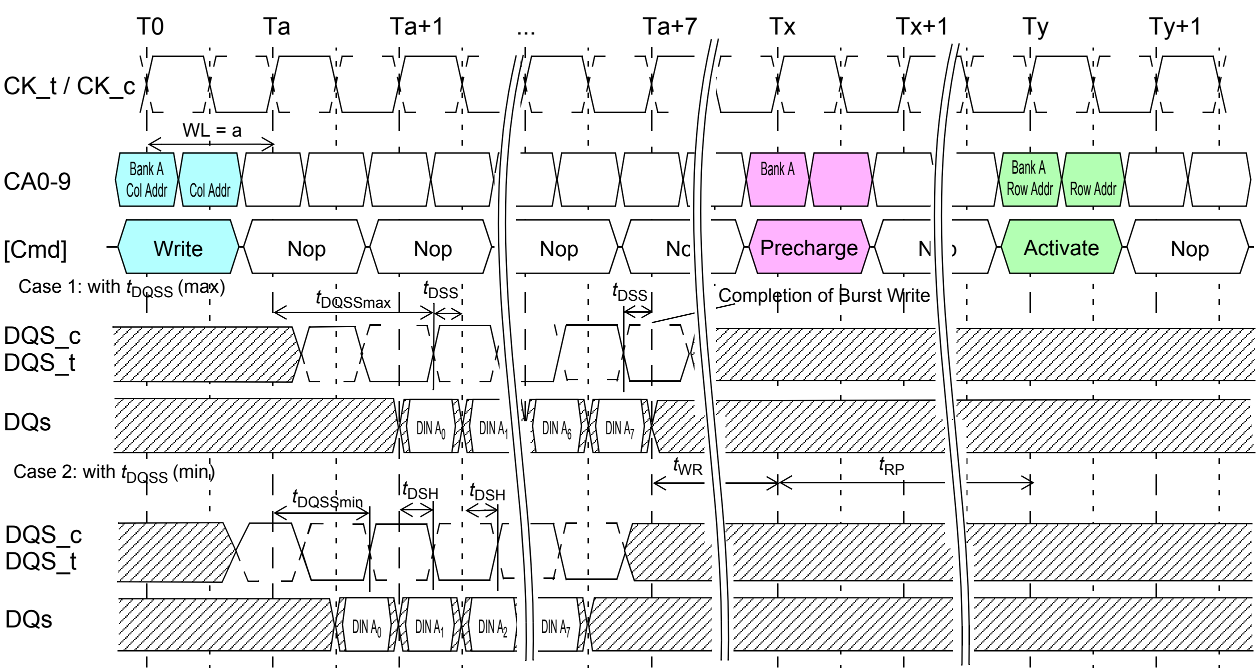
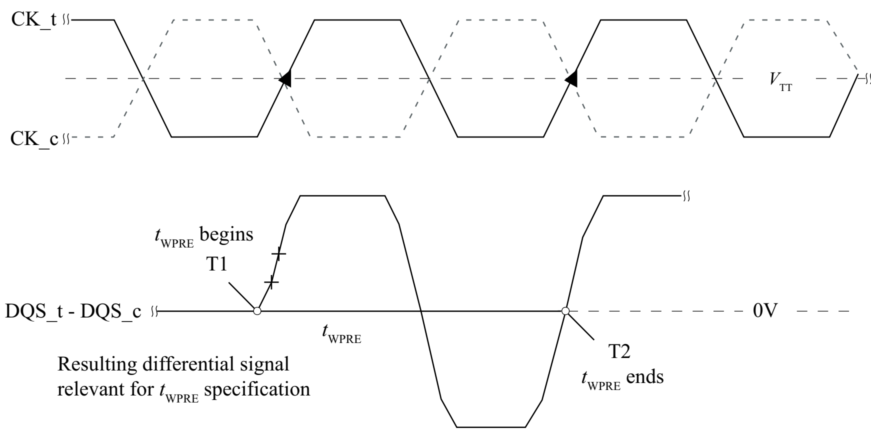


Figure 16 — LPDDR3: Burst Write

4.5.1 t_{WPRE} Calculation

The method for calculating t_{WPRE} is shown in the following figure:

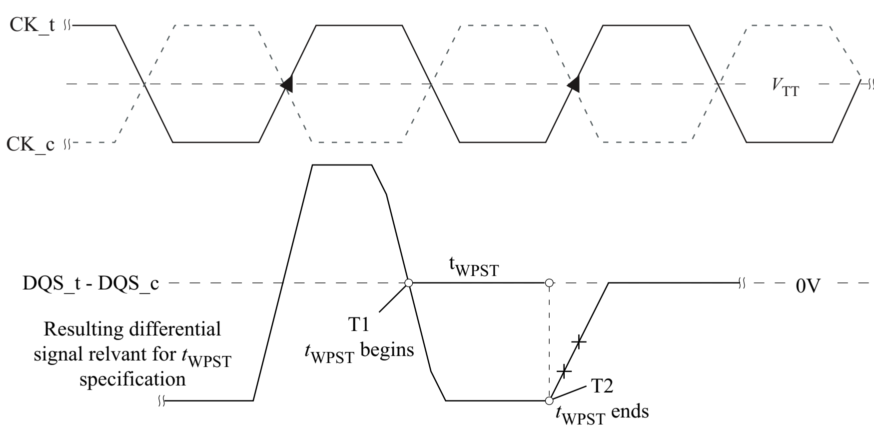
Figure 17 — Method for Calculating t_{WPRE} Transitions and Endpoints



4.5.2 t_{WPST} Calculation

The method for calculating t_{WPST} is shown in the follwing figure:

Figure 18 — Method for Calculating t_{WPST} Transitions and Endpoints



4.5 Burst Write Operation (cont'd)

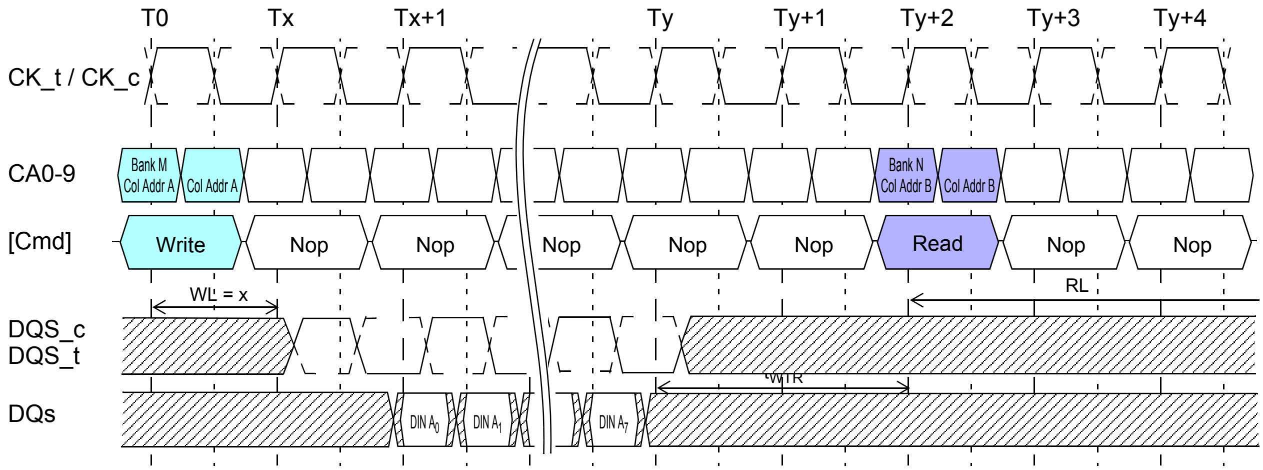


Figure 19 — LPDDR3: Burst Write Followed By Burst Read

NOTE 1 The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

NOTE 2 t_{WTR} starts at the rising edge of the clock after the last valid input datum.

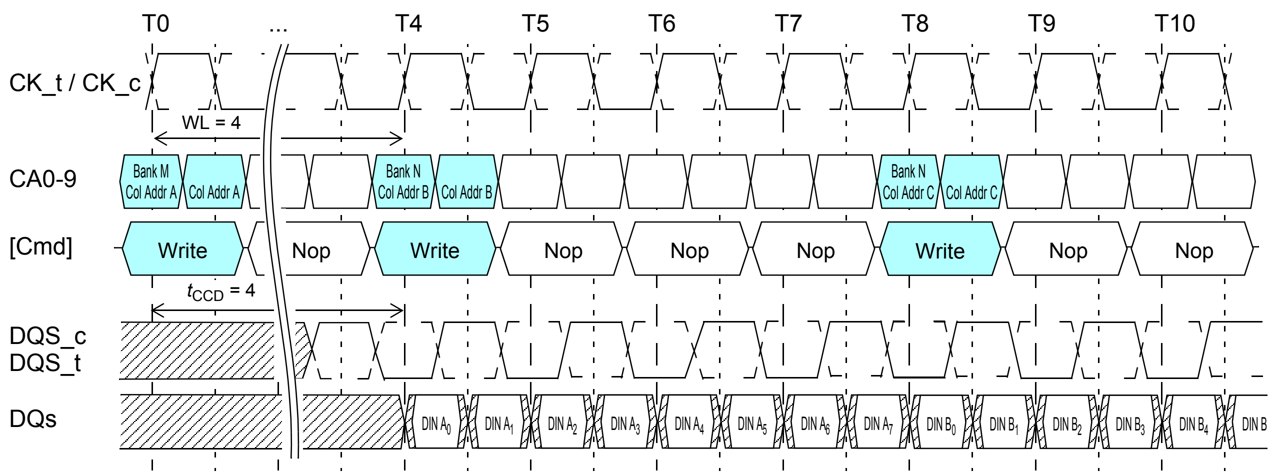


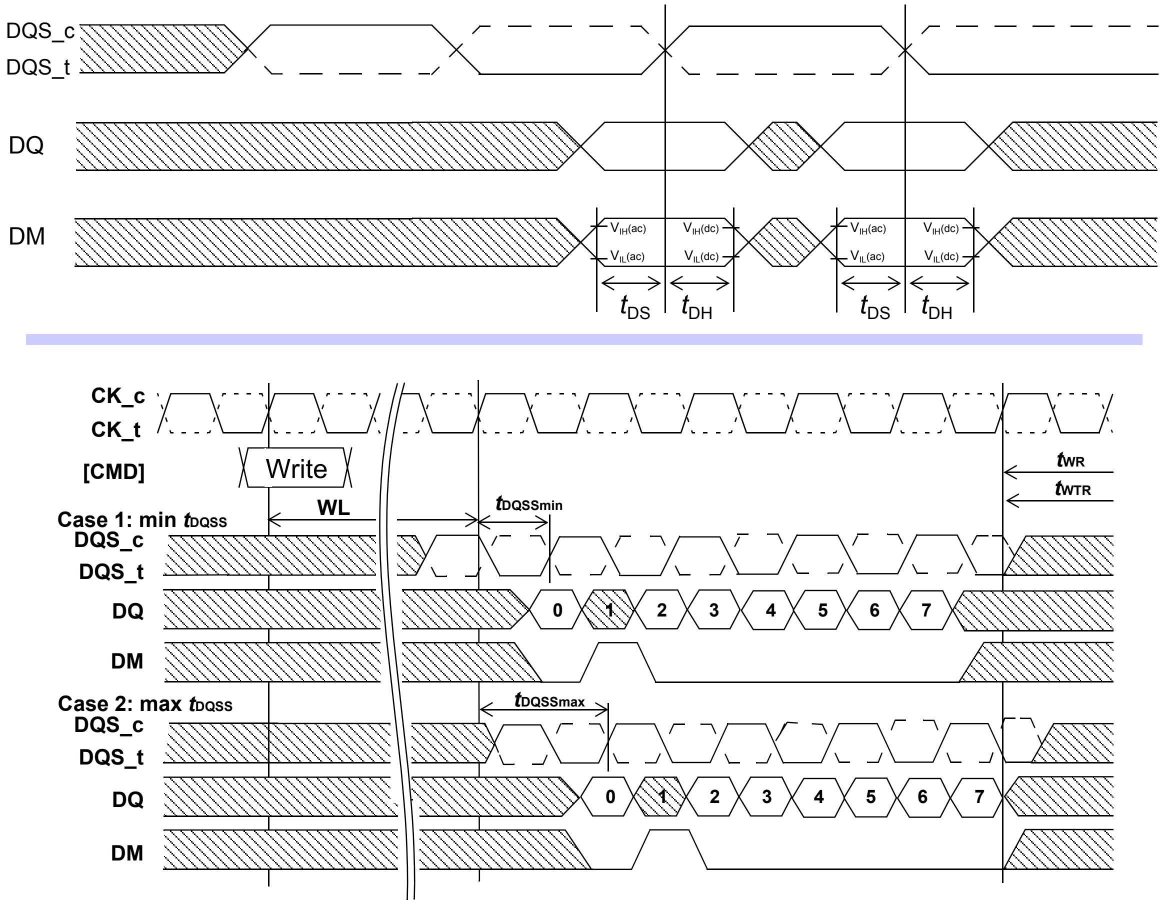
Figure 20 — LPDDR3: Seamless burst write: WL = 4, t_{CCD} = 4

NOTE 1: The seamless burst write operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is allowed for any activated bank.

4.6 Write Data Mask

On LPDDR3 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR2 SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loading is identical to data-bit loading to ensure matched system timing. For data mask timing, see Figure 1.

Figure 21 — Data Mask Timing



NOTE 1 For the data mask function, BL = 8 is shown; the second data bit is masked.

4.7 Precharge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access t_{RPab} after an all-bank PRECHARGE command is issued, or t_{RPpb} after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row-precharge time for an all-bank PRECHARGE (t_{RPab}) will be longer than the row PRECHARGE time for a single-bank PRECHARGE (t_{RPpb}). Activate to Precharge timing is shown in Figure 4.1 on page 25.

4.7 Precharge Operation (cont'd)

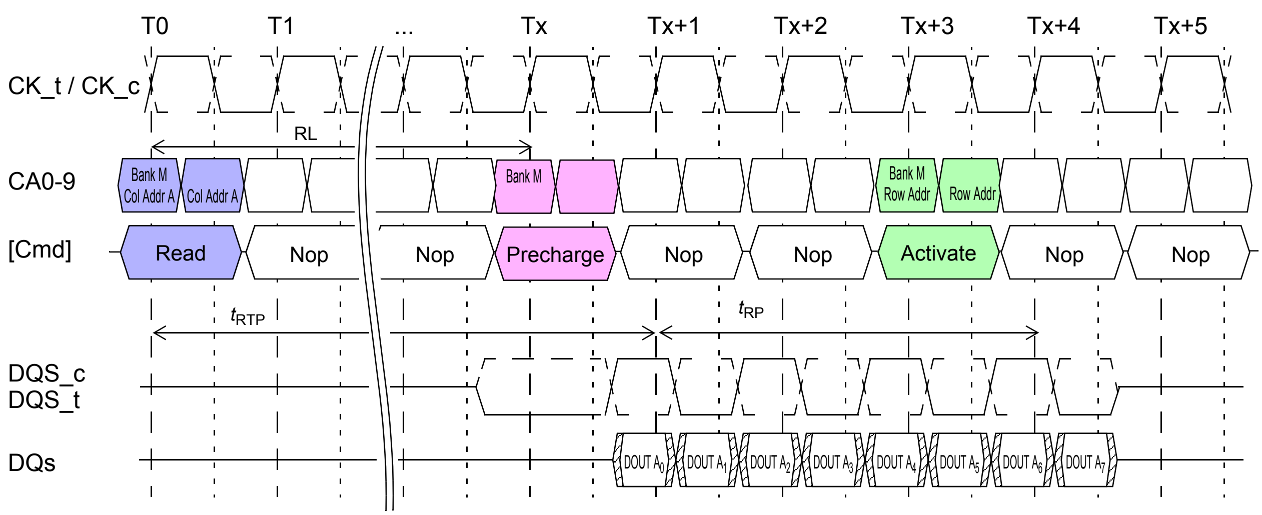
Table 10 — Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks

4.7.1 Burst Read operation followed by Precharge

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (t_{RP}) has elapsed. A PRECHARGE command cannot be issued until after t_{RAS} is satisfied. The minimum READ-to-PRECHARGE time (t_{RTP}) must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. t_{RTP} begins BL/2 - 2 clock cycles after the READ command. For LPDDR3 READ-to-PRECHARGE timings see Table 11 on page 39.

Figure 22 — LPDDR3: Burst Read Followed by Precharge

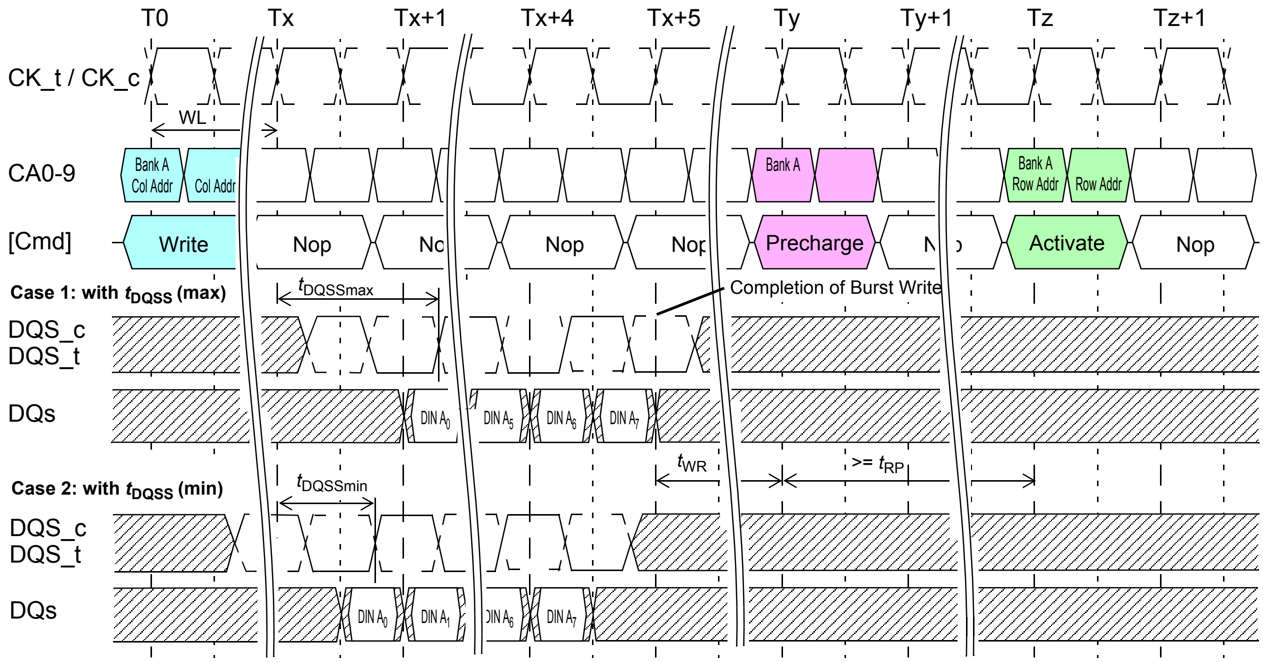


4.7.2 Burst Write followed by Precharge

For WRITE cycles, a WRITE recovery time (t_{WR}) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. A PRECHARGE command must not be issued prior to the t_{WR} delay. For LPDDR3 Write-to-Precharge timings see Table 11 on page 39.

LPDDR3 devices write data to the array in prefetch multiples(prefetch = 8). An internal WRITE operation can only begin after a prefetch group has been completely latched, so t_{WR} starts at prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(t_{WR}/t_{CK}) clock cycles.

Figure 23 — LPDDR3: Burst Write Followed by Precharge



4.7.3 Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or a WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency) thus improving system performance for random data access.

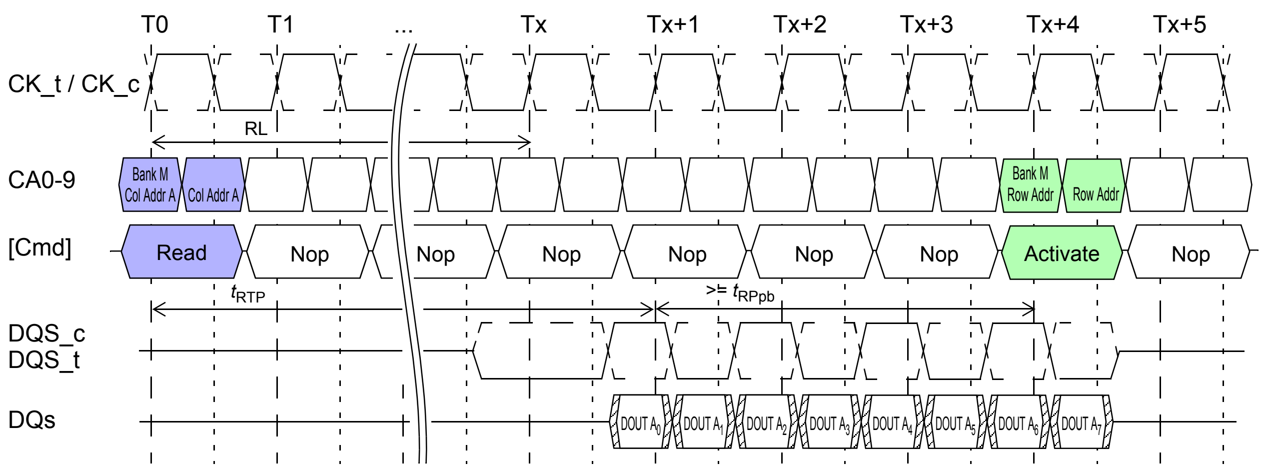
4.7.3.1 Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto-precharge function is engaged. LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(t_{RTP}/t_{CK}) clock cycles later than the READ with auto precharge command, whichever is greater. For LPDDR3 auto-precharge calculations see Table 2. Following an auto-precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

a) The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto- precharge begins.

b) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure 24 — Burst Read with Auto Precharge



4.7.3.2 Burst write with Auto-Precharge

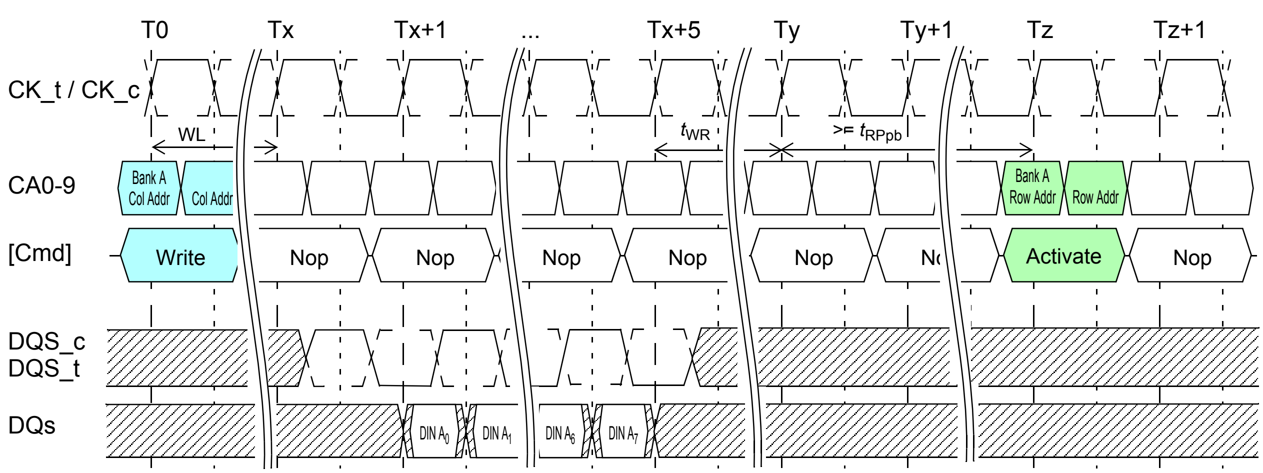
If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge t_{WR} cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto- precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure 25 — Burst Write with Auto Precharge



4.7.3 Auto-Precharge (cont'd)

Table 11 — Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
	Precharge All	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1,2
	Precharge All	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(4, RU(t_{RTP}/t_{CK})) - 4 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU($t_{DQSCKmax}$/t_{CK}) - WL + 1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE 1 For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after t_{RP} depending on the latest precharge command issued to that bank.

NOTE 2 Any command issued during the minimum delay time as specified in Table 11 is illegal.

NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

4.8 Refresh command

The REFRESH command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met (see Table 12 on page 41):

- t_{RFCab} has been satisfied after the prior REFab command
- t_{RFCpb} has been satisfied after the prior REFpb command
- t_{RP} has been satisfied after the prior PRECHARGE command to that bank
- t_{RRD} has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (t_{RFCpb}), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met (see Table 12 on page 41):

- t_{RFCpb} must be satisfied before issuing a REFab command
- t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank
- t_{RRD} must be satisfied before issuing an ACTIVATE command to a different bank
- t_{RFCpb} must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met (see Table 12 on page 41):

- t_{RFCab} has been satisfied following the prior REFab command
- t_{RFCpb} has been satisfied following the prior REFpb command
- t_{RP} has been satisfied following the prior PRECHARGE commands.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- t_{RFCab} latency must be satisfied before issuing an ACTIVATE command
- t_{RFCab} latency must be satisfied before issuing a REFab or REFpb command.

4.8 Refresh Command (cont'd)

Table 12 — REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From...	To...	Notes
t_{RFCab}	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
t_{RFCpb}	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
t_{RRD}	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

NOTE 1 A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

LPDDR3 devices provide significant flexibility in scheduling REFRESH commands as long as the boundary conditions shown in Figure 26 on page 42 are met. In the most straightforward implementations, a REFRESH command should be scheduled every t_{REFI}. In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for example, to enable a period where no refreshes are required. In the extreme (e.g., LPDDR3 4Gb), the user can choose to issue a refresh burst of 8192 REFRESH commands at the maximum supported rate (limited by t_{REFBW}), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: t_{REFW} - (R/8) × t_{REFBW} = t_{REFW} - R × 4 × t_{RFCab}. For example, a 4Gb LPDDR3 device at $T_C \leq 85°C$ can be operated without REFRESH commands up to 32ms - 8192 × 4 × 130ns ≈ 28 ms.

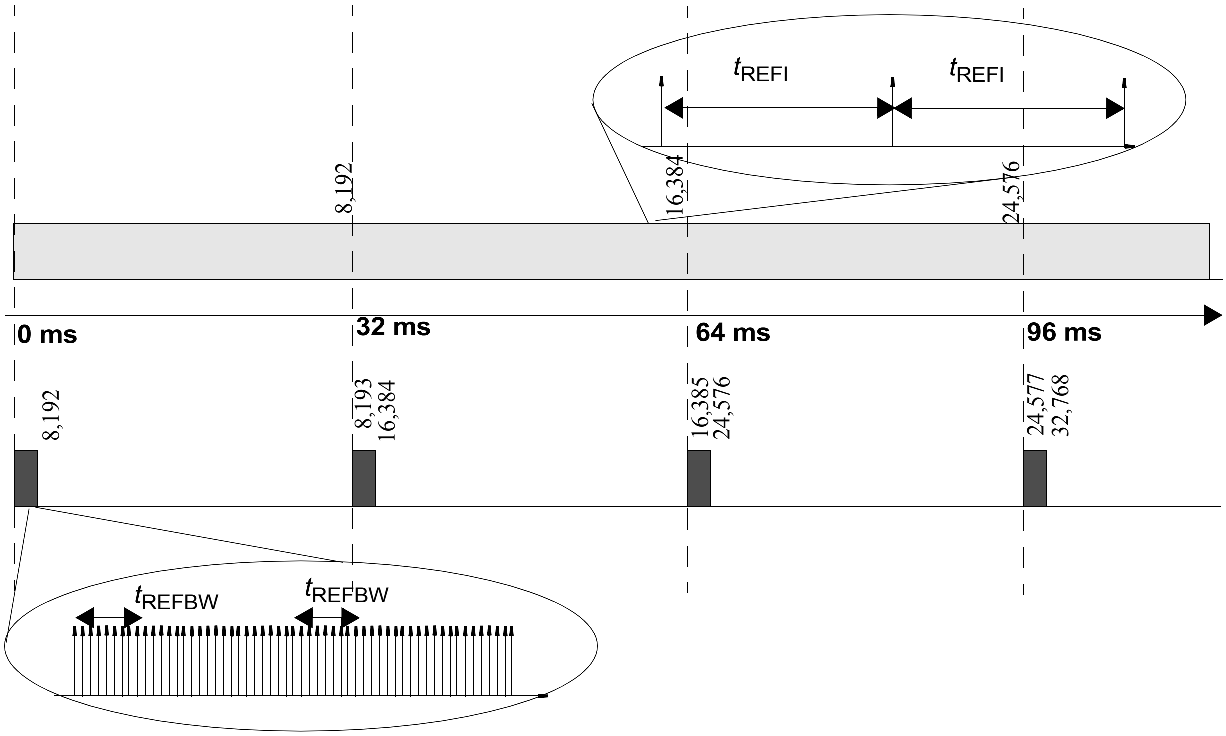
Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in *every* rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in Figure 27 on page 42. If this transition occurs immediately after the burst refresh phase, all rolling t_{REFW} intervals will meet the minimum required number of refreshes.

A non-supported transition is shown in Figure 28. In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling t_{REFW} intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed-refresh pattern must be assumed. It is recommend that self refresh mode is entered immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see Figure 29 on page 43).

4.8 Refresh Command (cont'd)

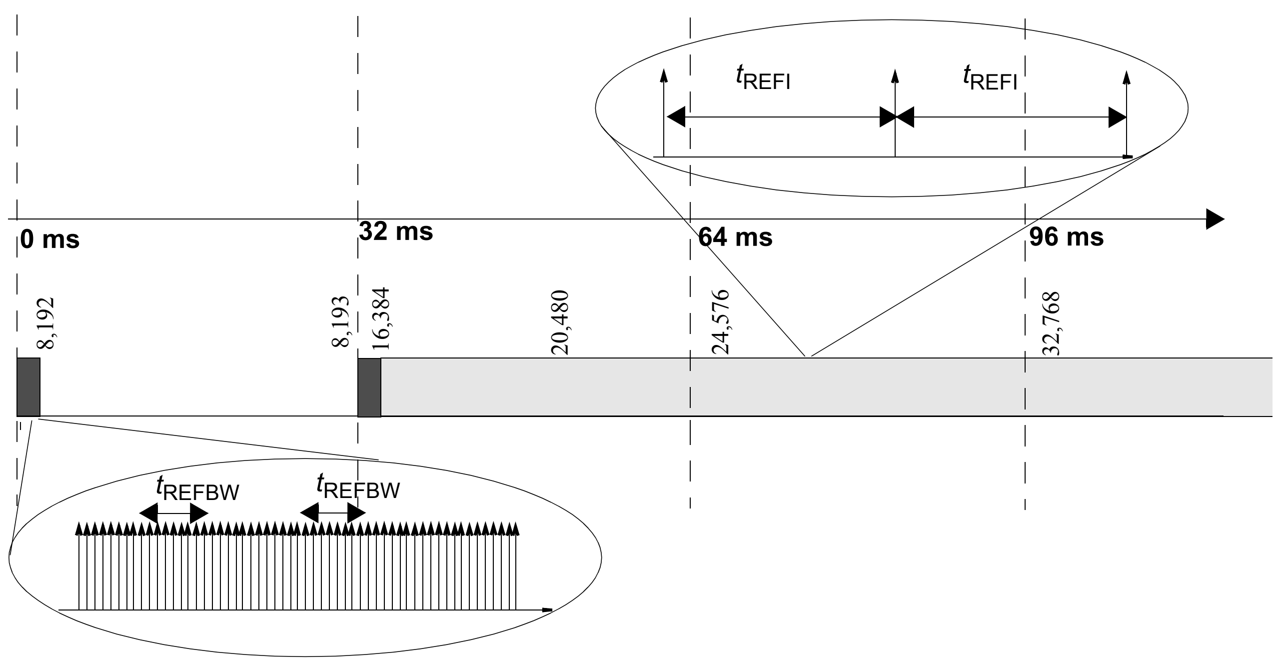
Figure 26 — Regular, Distributed REFRESH Pattern



NOTE 1 Compared to repetitive burst REFRESH with subsequent REFRESH pause.

NOTE 2 As an example, in a 4Gb LPDDR3 device at $T_C \leq 85°C$, the distributed refresh pattern has one REFRESH command per 3.9µs; the burst refresh pattern has one refresh command per 0.26µs, followed by ≈ 28ms without any REFRESH command.

Figure 27 — Supported Transition from Repetitive Burst REFRESH

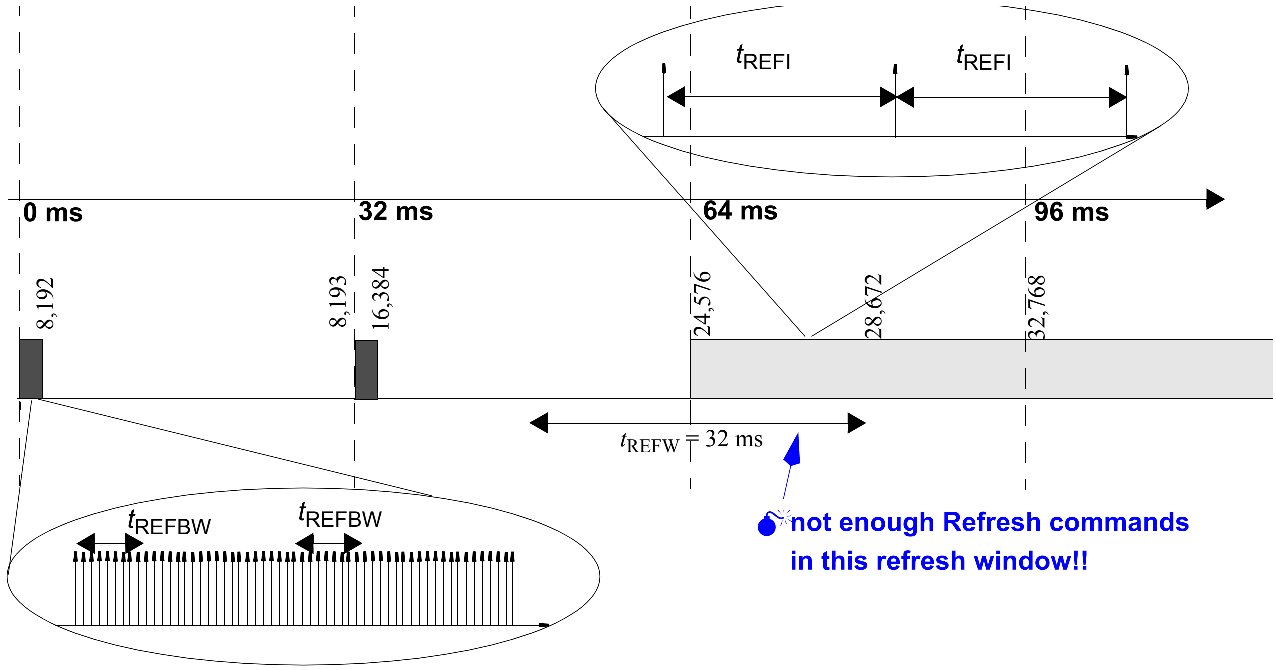


NOTE 1 Shown with subsequent REFRESH pause to regular, distributed-refresh pattern.

NOTE 2 As an example, in a 4Gb LPDDR3 device at $T_C \leq 85°C$, the distributed refresh pattern has one REFRESH command per 3.9µs; the burst refresh pattern has one refresh command per 0.52µs, followed by ≈ 28ms without any REFRESH command.

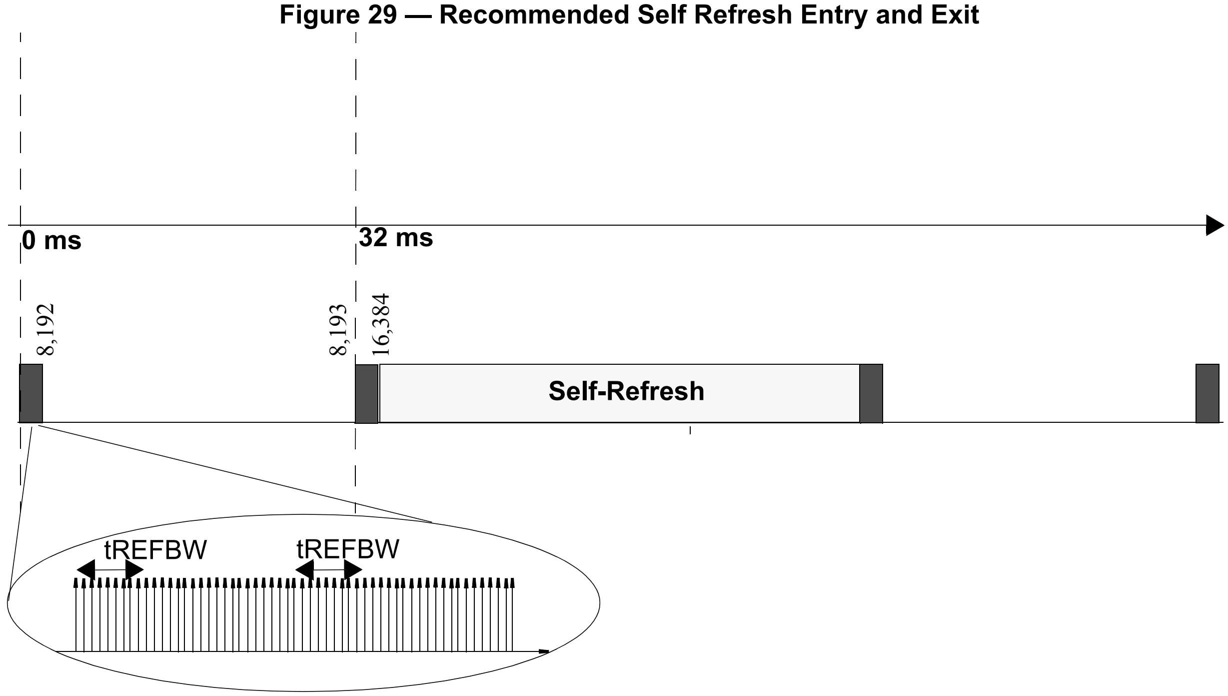
4.8 Refresh Command (cont'd)

Figure 28 — Nonsupported Transition from Repetitive Burst REFRESH



NOTE 1 Shown with subsequent REFRESH pause to regular, distributed-refresh pattern.
NOTE 2 There are only ≈ 4096 REFRESH commands in the indicated t_{REFW} window. This does not provide the minimum number of REFRESH commands (R).

Figure 29 — Recommended Self Refresh Entry and Exit



NOTE 1 In conjunction with a burst/pause refresh pattern.

4.8 Refresh Command (cont'd)

4.8.1 Refresh Requirements

a) Minimum number of REFRESH commands

LPDDR3 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (t_{REFW} = 32 ms @ MR4[2:0] = 011 or $T_C \leq 85°C$). For t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings, refer to the MR4 definition.

When using per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

b) Burst REFRESH limitation

To limit current consumption, a maximum of 8 REFab commands can be issued in any rolling t_{REFBW} ($t_{REFBW} = 4 \times 8 \times t_{RFCab}$). This condition does not apply if REFpb commands are used.

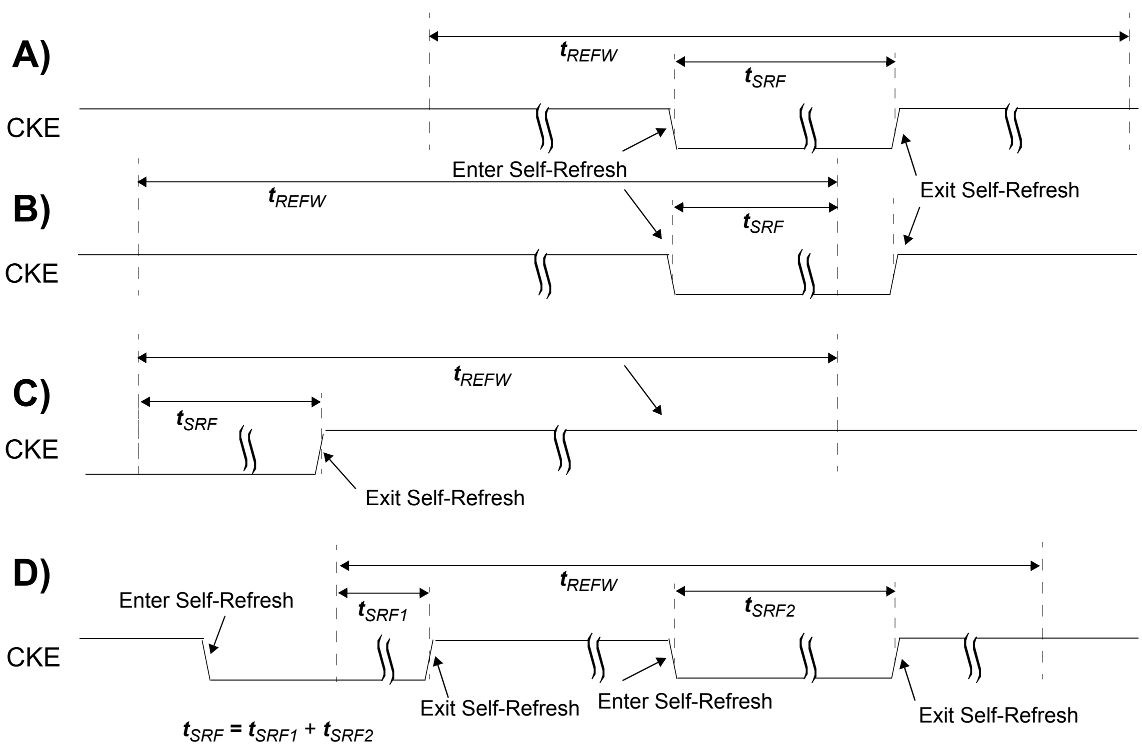
c) REFRESH Requirements and SELF REFRESH

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in this particular window is reduced to:

$$R' = R - RU\{(tSRF)/(tREFI)\} = R - RU\{R \times (tSRF)/(tREFW)\}$$

where RU stands for the round-up function.

Figure 30 — t_{SRF} Definition



NOTE 1 Time in self refresh mode is fully enclosed in the refresh window (t_{REFW}).

NOTE 2 At self refresh entry.

NOTE 3 At self refresh exit.

NOTE 4 Several intervals in self refresh during one t_{REFW} interval. In this example, $t_{SRF} = t_{SRF1} + t_{SRF2}$.

4.8 Refresh Command (cont'd)

Figure 31 — All-Bank REFRESH Operation

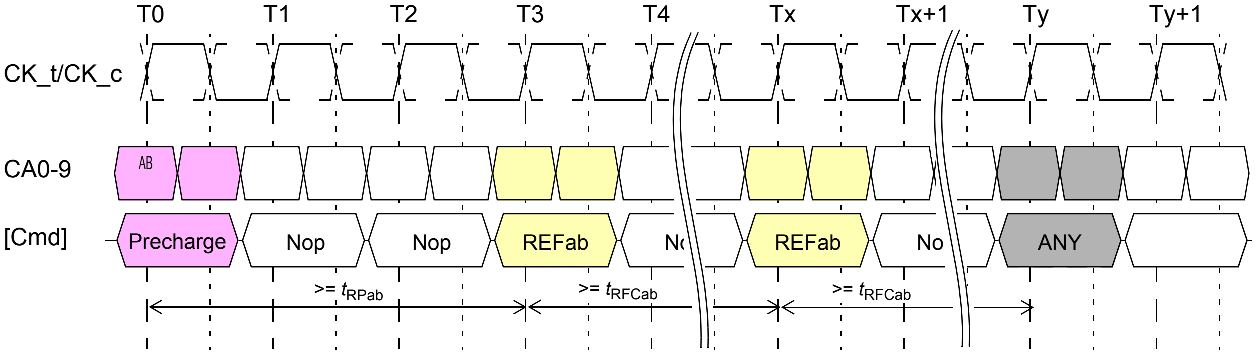
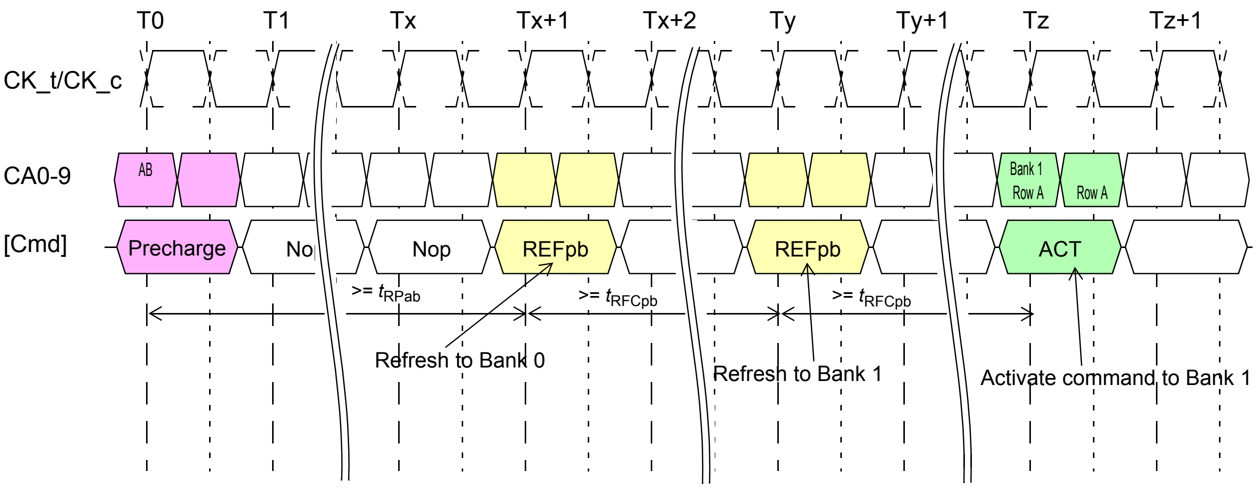


Figure 32 — Per-Bank REFRESH Operation



NOTE 1 In the beginning of this example, the REFpb bank is pointing to bank 0.

NOTE 2 Operations to banks other than the bank being refreshed are supported during the t_{RFCpb} period.

4.9 Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR3 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as t_{CPDED}. CKE LOW will result in deactivation of input receivers after t_{CPDED} has expired. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR3 SDRAM devices can operate in Self Refresh in both the standard or elevated temperature ranges. LPDDR3 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (V_{DD1}, V_{DD2}, and V_{DDCA}) must be at valid levels. V_{DDQ} may be turned off during Self-Refresh. Prior to exiting Self-Refresh, V_{DDQ} must be within specified limits. V_{refDQ} and V_{refCA} may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self-Refresh, V_{refDQ} and V_{refCA} must be within specified limits (see Recommended DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is $t_{CKESR,min}$. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 t_{CK} prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSR}. For the description of ODT operation and specifications during self-refresh entry and exit, see section On-Die Termination on page 60.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

4.9 Self Refresh operation (cont'd)

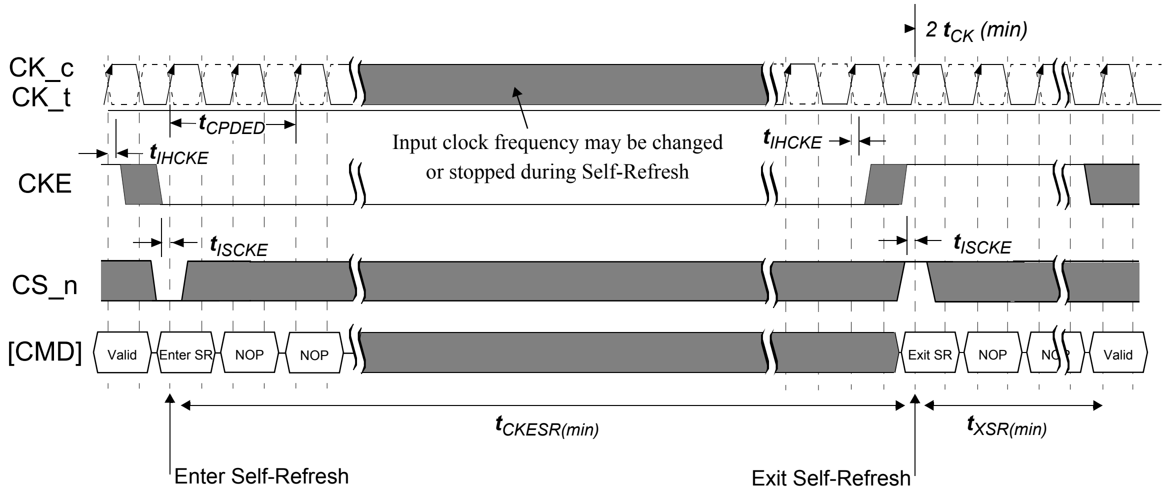


Figure 33 — LPDDR3: Self-Refresh Operation

NOTE 1 Input clock frequency may be changed or can be stopped or floated during self-refresh, provided that upon exiting self-refresh, the clock is stable and within specified limits for a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the speed grade in use.

NOTE 2 Device must be in the “All banks idle” state prior to entering Self Refresh mode.

NOTE 3 t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.

NOTE 4 A valid command may be issued only after t_{XSR} is satisfied. NOPs shall be issued during t_{XSR}.

4.9.1 Partial Array Self-Refresh (PASR)

4.9.1.1 PASR Bank Masking

The LPDDR3 SDRAM has eight banks (additional banks may be required for higher densities). Each bank of an LPDDR3 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16 as described on page 23.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

4.9.1.2 PASR Segment Masking

A segment masking scheme may be used in lieu of or in combination with the bank masking scheme in LPDDR3 SDRAM. LPDDR3 devices utilize eight segments per bank. For segment masking bit assignments, see Mode Register 17 as described on page 23.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. Eight segments are used as listed in Mode Register 17 as described on page 23. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

4.9 Self Refresh operation (cont'd)

Table 13 — Example of Bank and Segment Masking use in LPDDR3 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE 1 This table illustrates an example of an 8-bank LPDDR3 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

4.10 Mode Register Read (MRR) Command

The Mode Register Read (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × t_{CK} + t_{DQSCK} + t_{DQSQ} following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are toggled for the duration of the mode register read burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted.

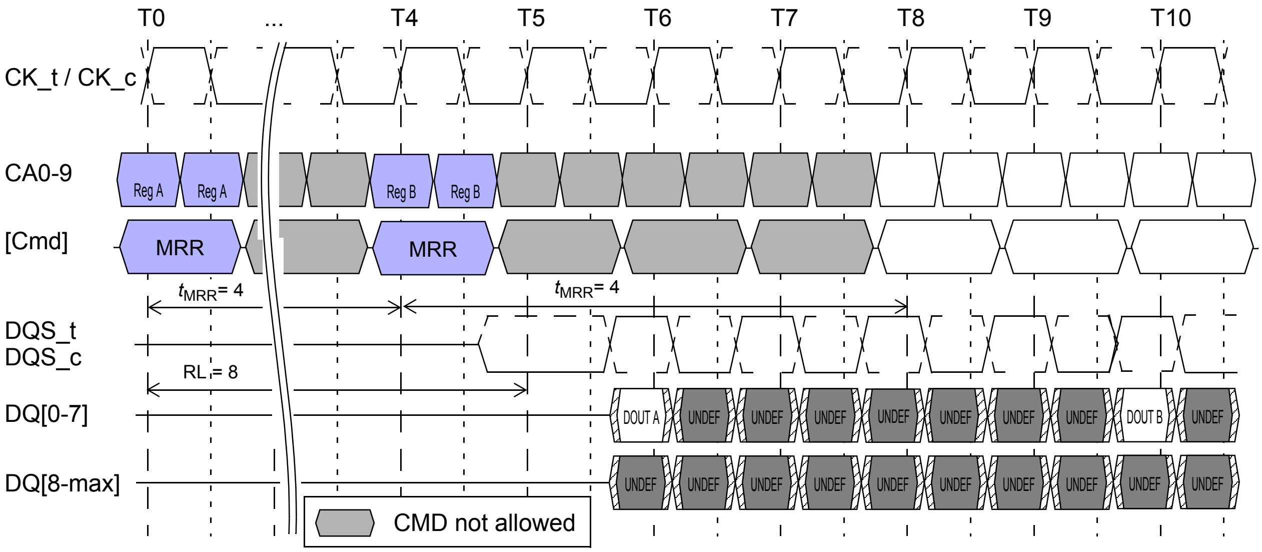


Figure 34 — Mode Register Read timing example: RL = 8

NOTE 1 MRRs to DQ calibration registers MR32 and MR40 are described in DQ calibration section.

NOTE 2 Only the NOP command is supported during t_{MRR}.

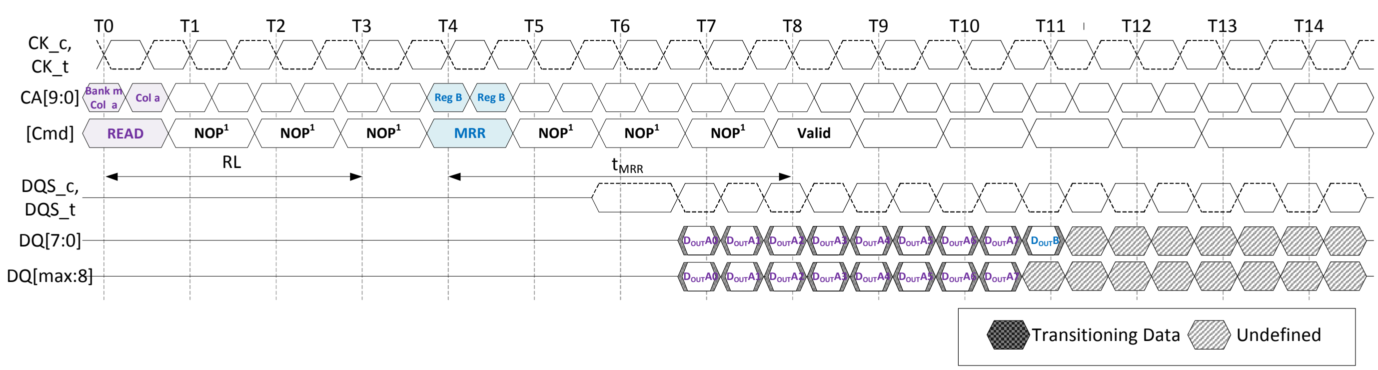
NOTE 3 Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.

NOTE 4 Minimum Mode Register Read to write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + 8/2 + 1 - WL clock cycles.

NOTE 5 Minimum Mode Register Read to Mode Register Write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + 8/2 + 1clock cycles.

NOTE 6 In this example, RL = 8 for illustration purposes only.

Figure 35 — READ to MRR Timing



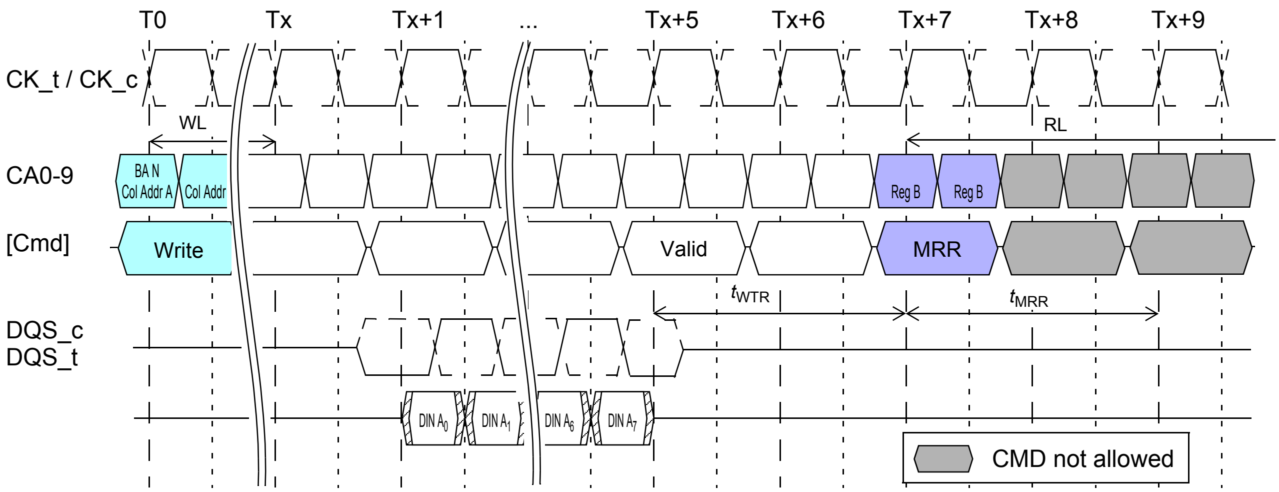
NOTE 1 Only the NOP command is supported during ^{t}MRR.

NOTE 2 The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.

4.10 Mode Register Read Command (cont'd)

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(t_{WTR}/t_{CK}) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.

Figure 36 — Burst Write Followed by MRR

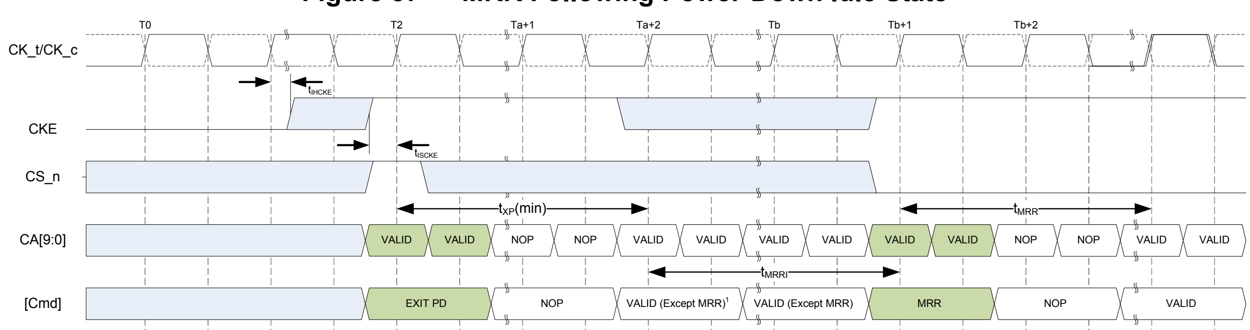


NOTE 1 The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
NOTE 2 Only the NOP command is supported during t_{MRR}.

4.10.0.1 MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, t_{MRRI}, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to t_{RCD}) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

Figure 37 — MRR Following Power-Down Idle State



Notes:
1. Any valid command from the idle state except MRR
2. $t_{MMRI} = t_{RCD}$

4.10.1 Temperature Sensor

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device T_{OPER} (Table 32 on page 79) may be used to determine whether operating temperature requirements are being met.

LPDDR3 devices shall monitor device temperature and update MR4 according to t_{TSI}. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than t_{TSI}.

When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} specification (Table 32 on page 79) that applies for the standard or elevated temperature ranges. For example, T_{CASE} may be above 85° C when MR4[2:0] equals 011B. LPDDR3 devices shall allow for 2° C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2° C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2C$$

Table 14 — Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	t_{TSI}	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 32ms + 1ms) \leq 2C$$

In this case, ReadInterval shall be no greater than 167 ms.

4.10.1 Temperature Sensor (cont'd)

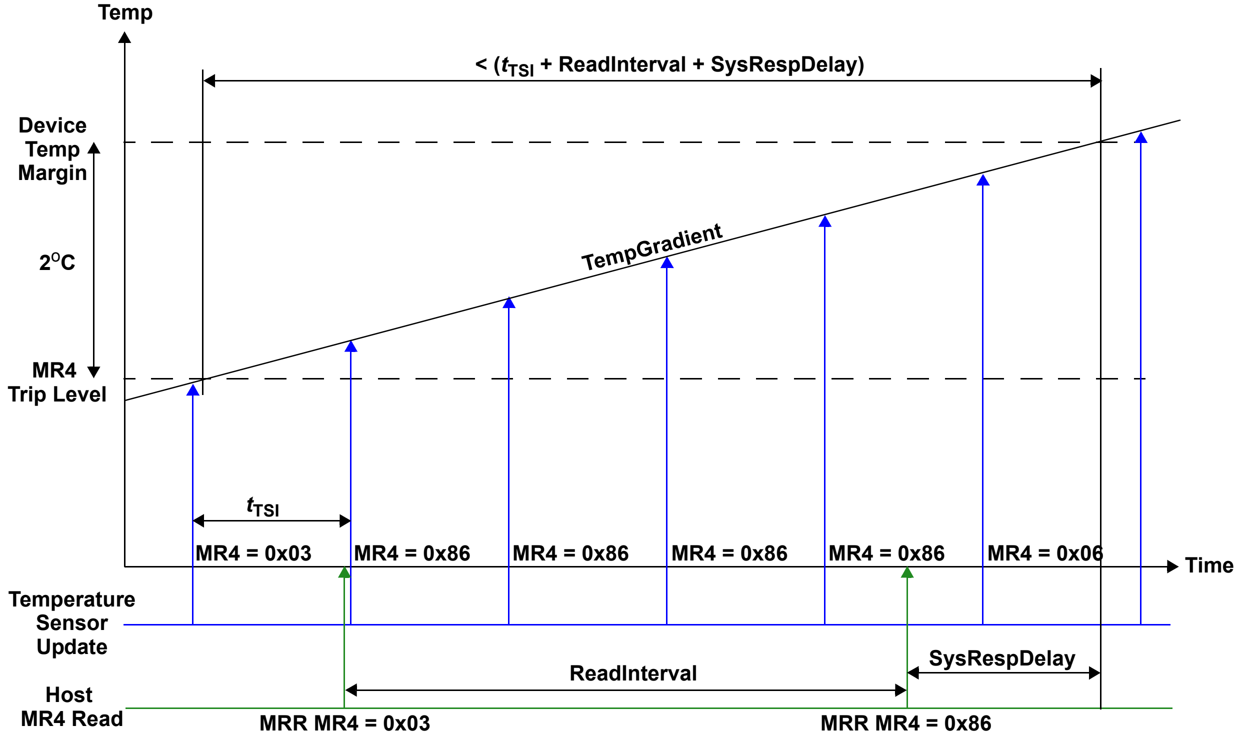


Figure 38 — Temp Sensor Timing

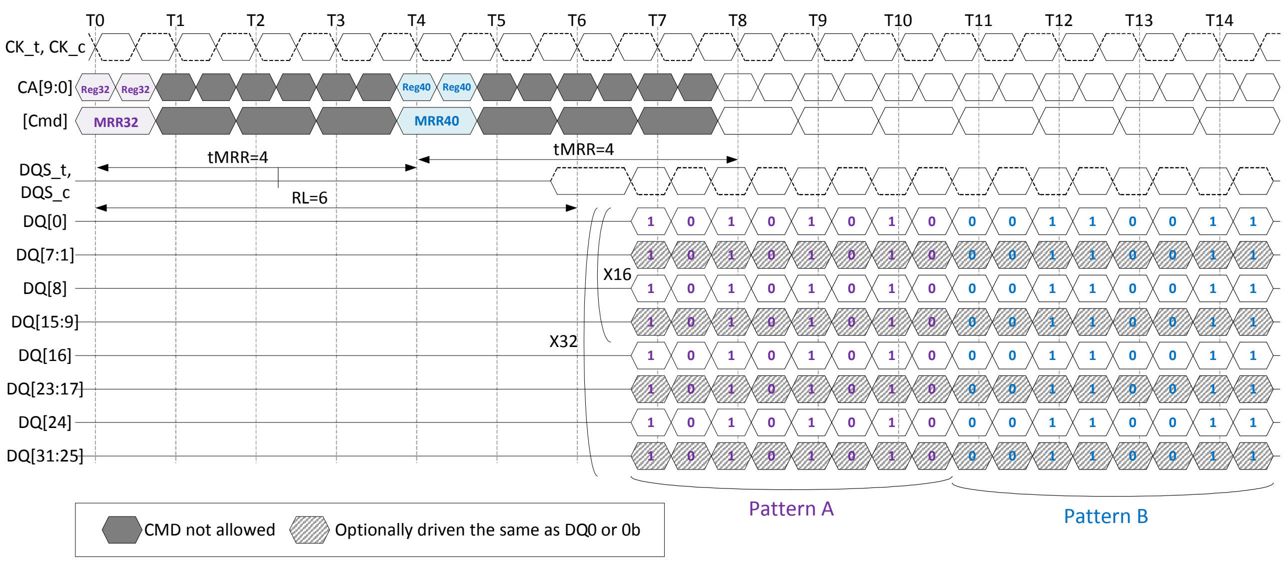
4.10.2 DQ Calibration

LPDDR3 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst..

Table 15 — Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7
Pattern “A” (MR32)	1	0	1	0	1	0	1	0
Pattern “B” (MR40)	0	0	1	1	0	0	1	1

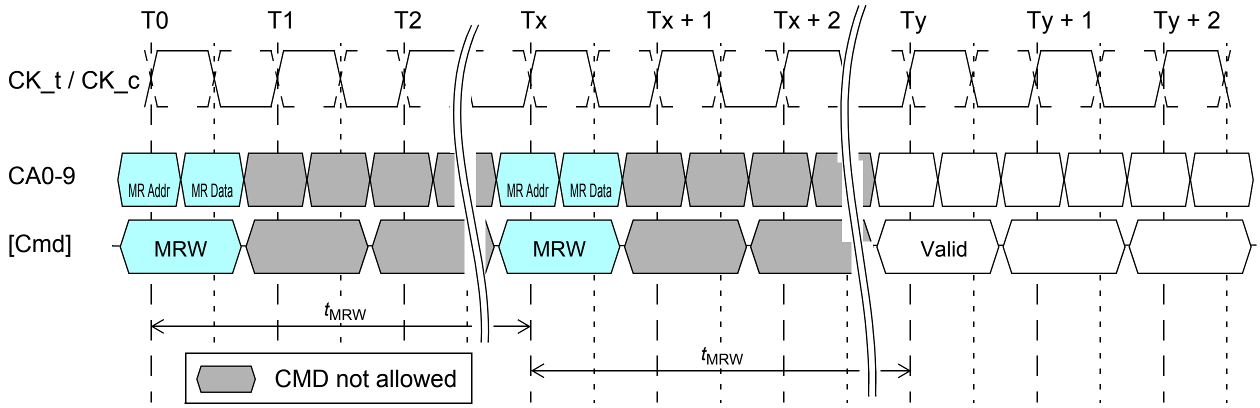
Figure 39 — DQ Calibration Timing



4.11 Mode Register Write (MRW) Command

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode register WRITEs to read-only registers have no impact on the functionality of the device.

Figure 40 — Mode Register Write Timing



NOTE 1 At time Ty, the device is in the idle state.

NOTE 2 Only the NOP command is supported during t_{MRW}.

4.11.1 Mode Register Write

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

4.11.1.1 MRW RESET

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

Table 16 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
SDRAM		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Init)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

4.11.2 Mode Register Write ZQ Calibration Command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance and on-die termination across process, temperature, and voltage. LPDDR3 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: t_{ZQINIT}, $t_{ZQRESET}$, t_{ZQCL}, and t_{ZQCS}. t_{ZQINIT} is for initialization calibration; $t_{ZQRESET}$ is for resetting ZQ to the default output impedance; t_{ZQCL} is for long calibration(s); and t_{ZQCS} is for short calibration(s).

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of ±15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system. The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQCorrection) of output impedance errors within t_{ZQCS} for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)} = CalibrationInterval$$

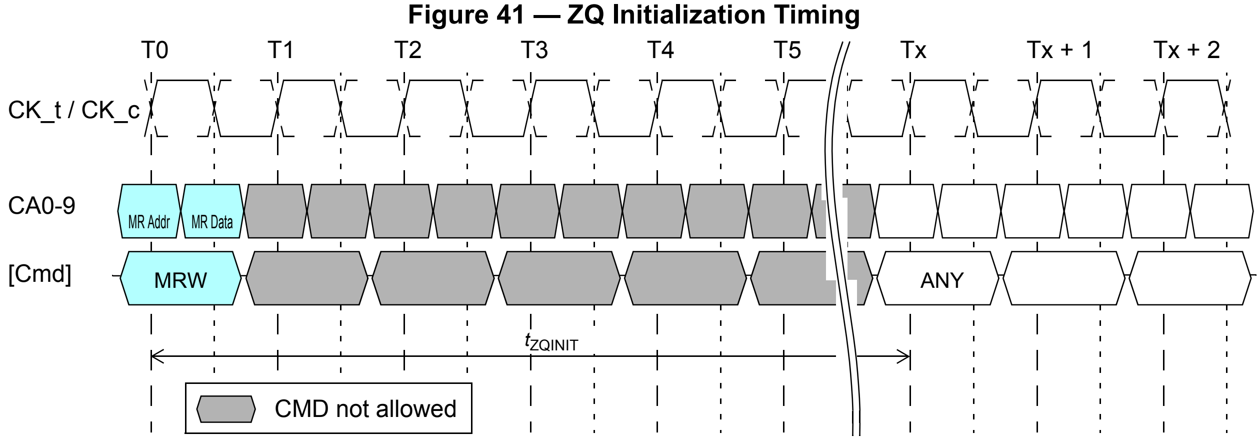
Where T_{sens} = MAX ($dR_{ON}dT$) and V_{sens} = MAX ($dR_{ON}dV$) define temperature and voltage sensitivities.

For example, if T_{sens} = 0.75%/°C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1°C/sec, and $V_{driftrate}$ = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged. ODT shall be disabled via the mode register or the ODT pin prior to issuing a ZQ calibration command. No other activities can be performed on the data bus and the data bus shall be un-terminated during calibration periods (t_{ZQINIT}, t_{ZQCL}, or t_{ZQCS}). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQ RESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption. In systems sharing a ZQ resistor between devices, the controller must prevent t_{ZQINIT}, t_{ZQCS}, and t_{ZQCL} overlap between the devices. ZQ RESET overlap is acceptable.

Figure 41 — ZQ Initialization Timing



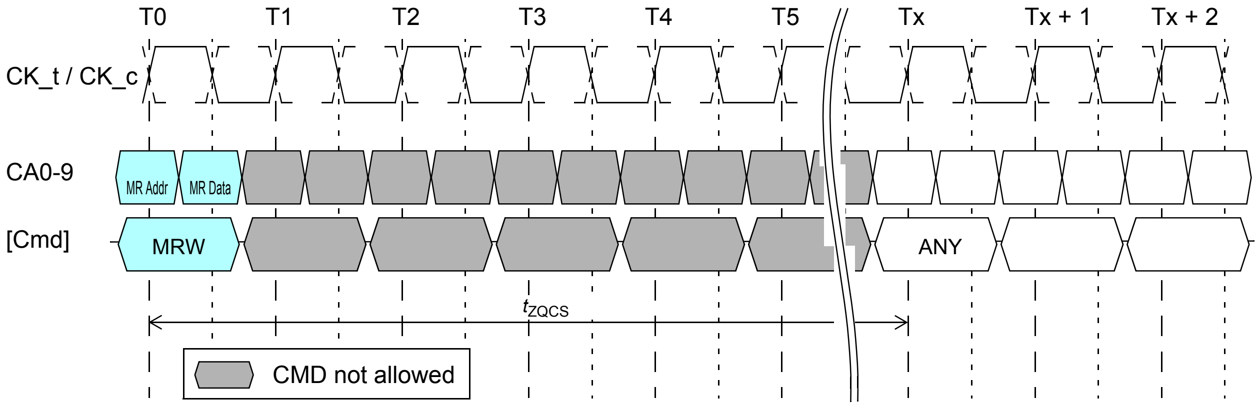
NOTE 1 Only the NOP command is supported during ZQ calibration.

NOTE 2 CKE must be registered HIGH continuously during the calibration period.

NOTE 3 All devices connected to the DQ bus should be High-Z during the calibration process.

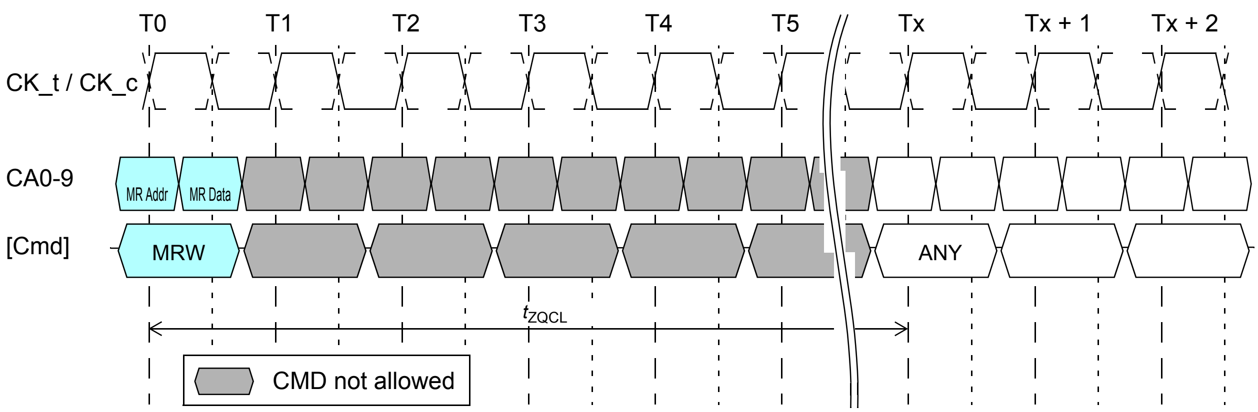
4.11.2 Mode Register Write ZQ Calibration Command (cont'd)

Figure 42 — ZQ Calibration Short Timing



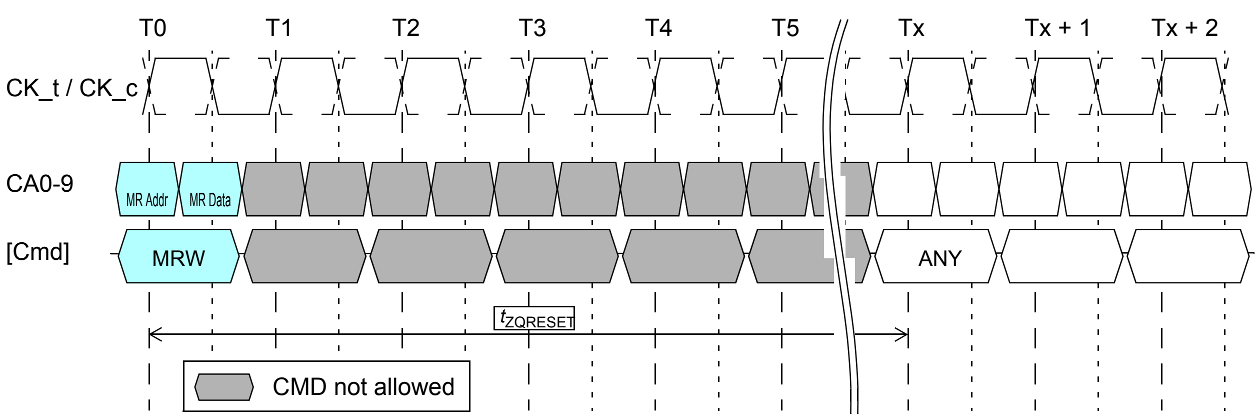
NOTE 1 Only the NOP command is supported during ZQ calibration.
NOTE 2 CKE must be registered HIGH continuously during the calibration period.
NOTE 3 All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 43 — ZQ Calibration Long Timing



NOTE 1 Only the NOP command is supported during ZQ calibration.
NOTE 2 CKE must be registered HIGH continuously during the calibration period.
NOTE 3 All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 44 — ZQ Calibration Reset Timing



NOTE 1 Only the NOP command is supported during ZQ calibration.
NOTE 2 CKE must be registered HIGH continuously during the calibration period.
NOTE 3 All devices connected to the DQ bus should be High-Z during the calibration process.

4.11.2 Mode Register Write ZQ Calibration Command (cont'd)

4.11.2.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, an R_{ZQ} ±1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see Pin Capacitance table, Table 55 on page 99).

4.11.3 Mode Register Write - CA Training Mode

Because CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. A CA Training mechanism is provided.

4.11.3.1 CA Training Sequence

a) CA Training mode entry: Mode Register Write to MR41

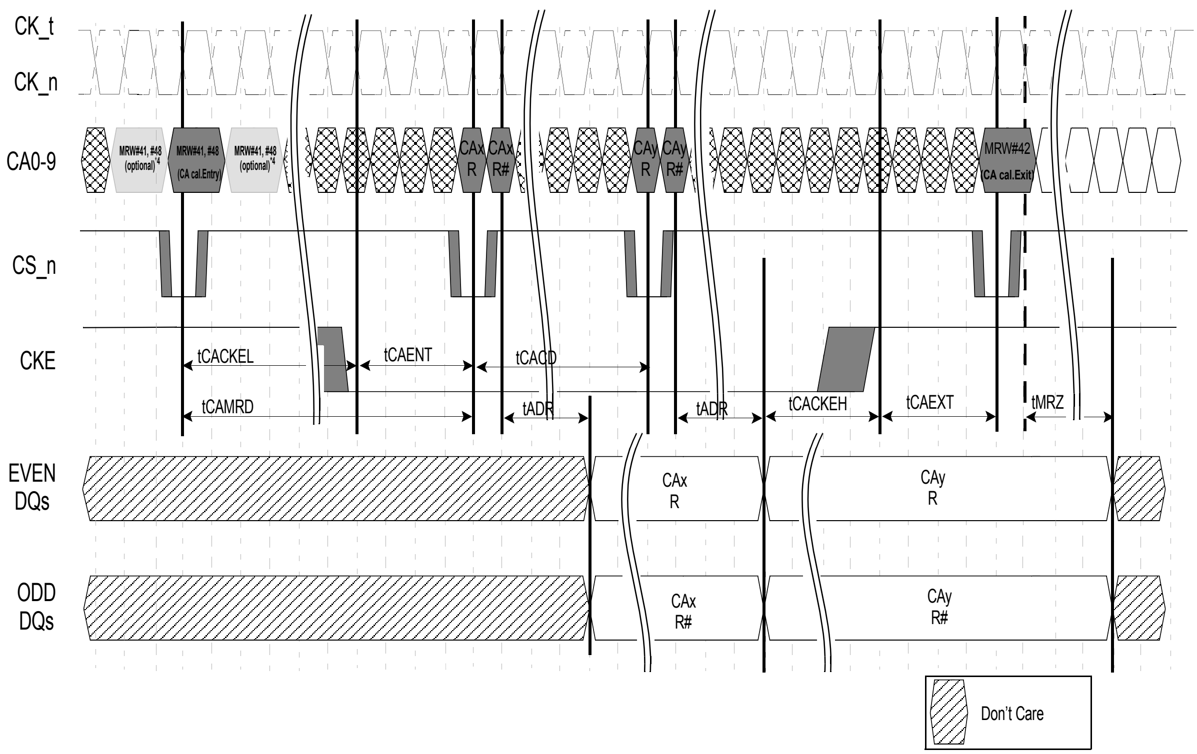
b) CA Training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see Table 17 on page 58)

c) CA to DQ mapping change: Mode Register Write to MR48

d) Additional CA Training session: Calibrate remaining CA pins (CA4 and CA9) (see Table 19 on page 58)

e) CA Training mode exit: Mode Register Write to MR42

Figure 45 — CA Training Timing chart



NOTE 1 Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.

NOTE 2 CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Both MR41 and MR48 training sequences must be completed before exiting the training mode (MR42). To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command.

NOTE 3 Because data out control is asynchronous and will be an analog delay from when all the CA data is available, t_{ADR} and t_{MRZ} are defined from CK_t falling edge.

NOTE 4 It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA training entry command to ensure setup and hold timings on the CA bus.

4.11.3 Mode Register Write -- CA Training Mode (cont'd)

The LPDDR3 SDRAM may not properly recognize a Mode Register Write command at normal operation frequency before CA Training is finished. Special encodings are provided for CA Training mode enable/disable. MR41 and MR42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR41 and MR42 at normal operation frequency even before CA timing adjustment is finished.

Calibration data will be output through DQ pins. CA to DQ mapping is described in Table 19.

After timing calibration with MR41 is finished, users will issue MRW to MR48 and calibrate remaining CA pins (CA4 and CA9) using (DQ0/DQ1and DQ8/DQ9) as calibration data output pins (see Table 21).

CA Training timing values are specified in the AC Timing Table on page 112.

Table 17 — CA Training mode enable (MR41(29H, 0010 1001B), OP=A4H(1010 0100B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	H	L	L	H	L	H
Falling Edge	L	L	L	L	H	L	L	H	L	H

Table 18 — CA Training mode disable (MR42(2AH,0010 1010B),OP=A8H(1010 1000B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	H	L	H	L	H
Falling Edge	L	L	L	L	L	H	L	H	L	H

Table 19 — CA to DQ mapping (CA Training mode enabled with MR41)

CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8	Clock edge
DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14	CK_t rising edge
DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15	CK_t falling edge

Table 20 — CA Training mode enable (MR48(30H, 0011 0000B), OP=C0H(1100 0000B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	L	L	L	H	H
Falling Edge	L	L	L	L	L	L	L	L	H	H

Table 21 — CA to DQ mapping (CA Training mode is enabled with MR48)

CA4	CA9	Clock edge
DQ0	DQ8	CK_t rising edge
DQ1	DQ9	CK_t falling edge

NOTE 1 Other DQs must have valid output (either HIGH or LOW)

4.11.4 Mode Register Write - WR Leveling Mode

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as t_{DQSS}, t_{DSS}, and t_{DSH}.

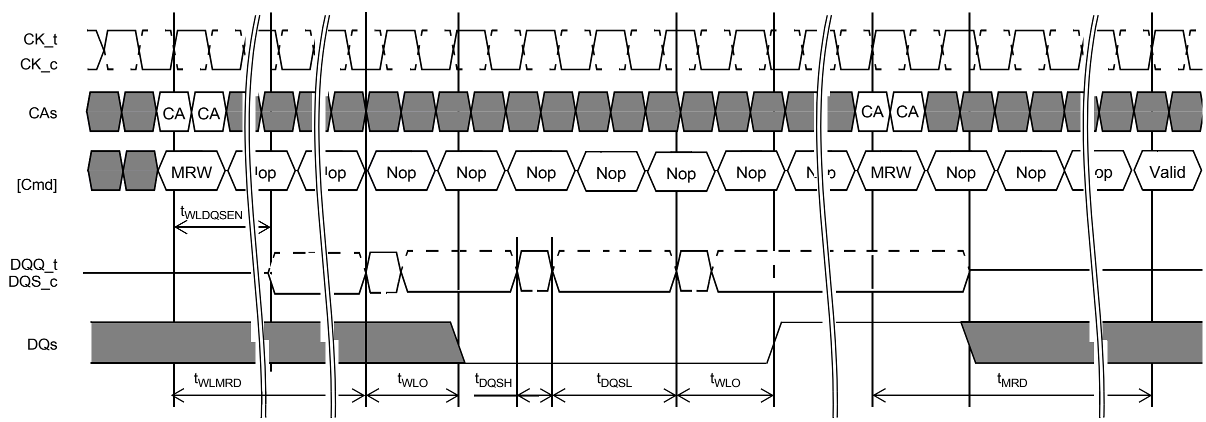
The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS_t/DQS_c signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS_t/DQS_c signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals delay established through this exercise ensures the t_{DQSS} specification can be met.

All data bits carry the leveling feedback to the controller (DQ[15:0] for x16 configuration, DQ[31:0] for x32 configuration). All DQS signals must be leveled independently.

The LPDDR3 SDRAM enters into write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS_t LOW and DQS_c HIGH after a delay of $t_{WLDQSEN}$. After time t_{WLMRD}, the controller provides DQS signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time $t_{WLMRD(max)}$ is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time t_{WLO}. The controller samples this information and either increment or decrement the DQS_t and/or DQS_c delay settings and launches the next DQS/DQS# pulse. The sample time and trigger time is controller dependent. Once the following DQS_t/DQS_c transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. Figure 46 describes the timing for the write leveling operation.

Figure 46 — Write Leveling Timing



4.12 On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DM via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. Unlike other command inputs, the ODT pin directly controls ODT operation and is not sampled by the clock.

The ODT feature is turned off and not supported in Self-Refresh and Deep Power Down modes. ODT operation can optionally be enabled during CKE Power Down via a mode register. Note that if ODT is enabled during Power Down mode VDDQ may not be turned off during Power Down. The DRAM will also disable termination during read operations.

A simple functional representation of the DRAM ODT feature is shown in Figure 47.

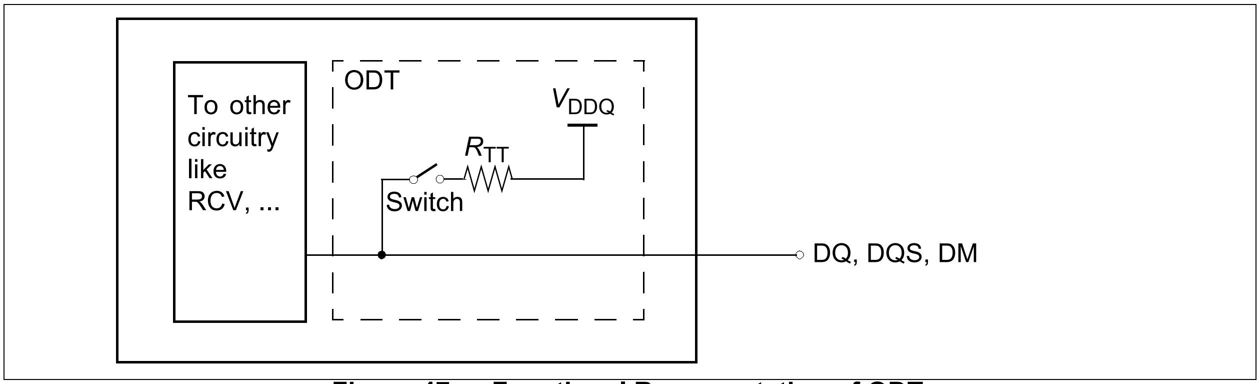


Figure 47 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of R_{TT} is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR11 is programmed to disable ODT, in self-refresh, in deep power down, in CKE power down (mode register option) and during read operations.

4.12.1 ODT Mode Register

The ODT Mode is enabled if MR11 OP<1:0> are non zero. In this case, the value of R_{TT} is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP<1:0> are zero.

MR11 OP<2> determines whether ODT, if enabled through MR11 OP<1:0>, will operate during CKE power down.

4.12.2 Asynchronous ODT

The ODT feature is controlled asynchronously based on the status of the ODT pin, except ODT is off when:.

- ODT is disabled through MR11 OP<1:0>
- DRAM is performing a read operation (RD or MRR)
- DRAM is in CKE Power Down and MR11 OP<2> is zero
- DRAM is in Self-Refresh or Deep Power Down modes.
- DRAM is in CA Training Mode.

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin: $t_{ODTon,min,max}$, $t_{ODToff,min,max}$.

Minimum R_{TT} turn-on time ($t_{ODTon,min}$) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum R_{TT} turn on time ($t_{ODTon,max}$) is the point in time when the ODT resistance is fully on. $t_{ODTon,min}$ and $t_{ODTon,max}$ are measured from ODT pin high.

Minimum R_{TT} turn-off time ($t_{ODToff,min}$) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time ($t_{ODToff,max}$) is the point in time when the on-die termination has reached high impedance. $t_{ODToff,min}$ and $t_{ODToff,max}$ are measured from ODT pin low.

4.12.3 ODT During Read Operations (RD or MRR)

During read operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT Mode is enabled).

4.12 On-Die Termination (cont'd)

4.12.4 ODT During Power Down

When MR11 OP<2> is zero, termination control through the ODT pin will be disabled when the DRAM enters CKE power down. After a power down command is registered, termination will be disabled within a time window specified by $t_{ODTd,min,max}$. ODT pin control is resumed when power down is exited (if ODT Mode is enabled). Between the power down exit command and until t_{XP} is satisfied, termination will transition from disabled to control by the ODT pin. When t_{XP} is satisfied, the ODT pin is used to control termination.

Minimum R_{TT} disable time ($t_{ODTd,min}$) is the point in time when the device termination circuit is no longer be controlled by the ODT pin. Maximum ODT disable time ($t_{ODTd,max}$) is the point in time when the on-die termination will be in high impedance.

When MR11 OP<2> is enabled and MR11 OP<1:0> are non zero, ODT operation is supported during CKE power down with ODT control through the ODT pin.

4.12.5 ODT During Self Refresh

LPDDR3 SDRAM disables the ODT function during self refresh. After a self refresh command is registered, termination will be disabled within a time window specified by $t_{ODTd,min,max}$. During self refresh exit, ODT control through the ODT pin is resumed (if ODT Mode is enabled). Between the self refresh exit command and until t_{XSR} is satisfied, termination will transition from disabled to control by the ODT pin. When t_{XSR} is satisfied, the ODT pin is used to control termination.

4.12.6 ODT During Deep Power Down

LPDDR3 SDRAM disables the ODT function during deep power down. After a deep power down command is registered, termination will be disabled within a time window specified by $t_{ODTd,min,max}$.

4.12.7 ODT During CA Training and Write Leveling

During CA Training Mode, LPDDR3 SDRAM will disable on-die termination and ignore the state of the ODT control pin. For ODT operation during Write Leveling mode, refer to the DRAM Termination Function In Write Leveling Mode Table on page 61 for termination activation and deactivation for DQ and DQS_t/DQS_c.

Table 22 — DRAM Termination Function In Write Leveling Mode

ODT pin	DQS_t/DQS_c termination	DQ termination
de-asserted	OFF	OFF
asserted	ON	OFF

If ODT is enabled, the ODT pin must be high, in Write Leveling mode.

Table 23 — ODT States Truth Table

	Write	Read/ DQ Cal	ZQ Cal	CA Training	Write Level
DQ Termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS Termination	Enabled	Disabled	Disabled	Disabled	Enabled

NOTE 1 ODT is enabled with MR11[1:0]=01b, 10b, or 11b and ODT pin HIGH. ODT is disabled with MR11[1:0]=00b or ODT pin LOW.

4.12 On-Die Termination (cont'd)

Figure 48 — Asynchronous ODT Timing Example for RL = 12

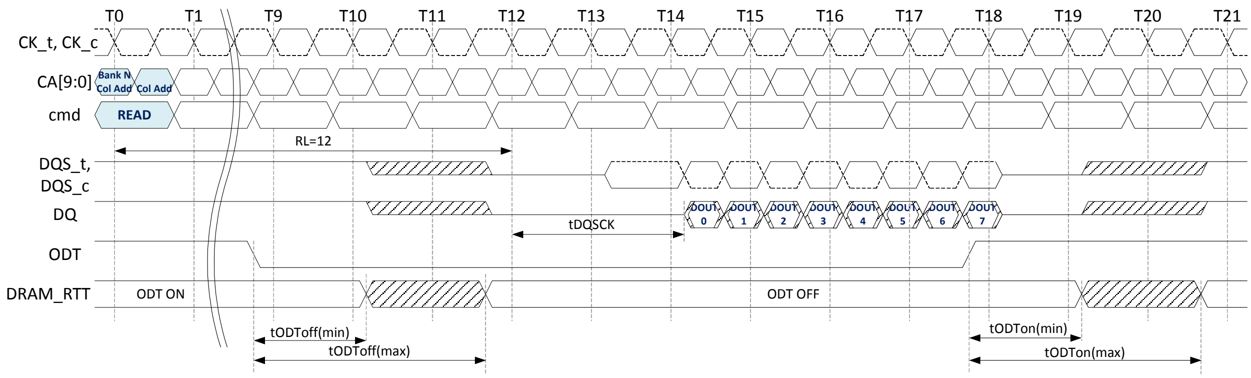
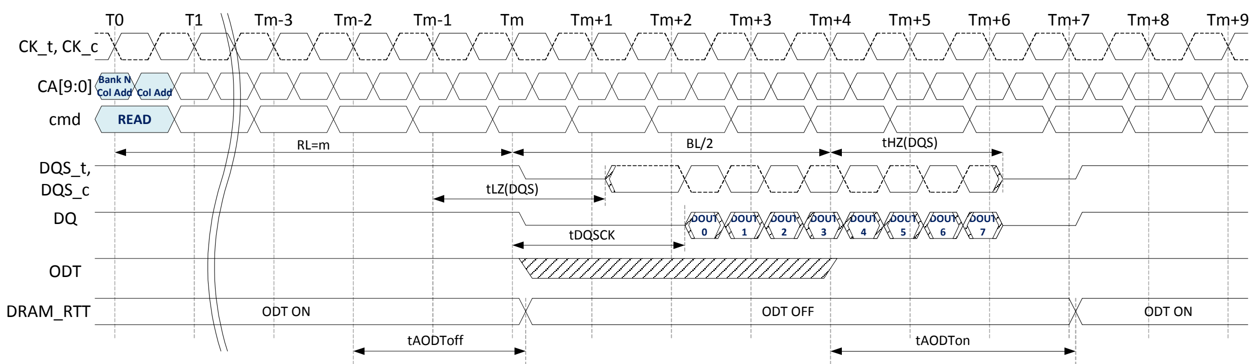


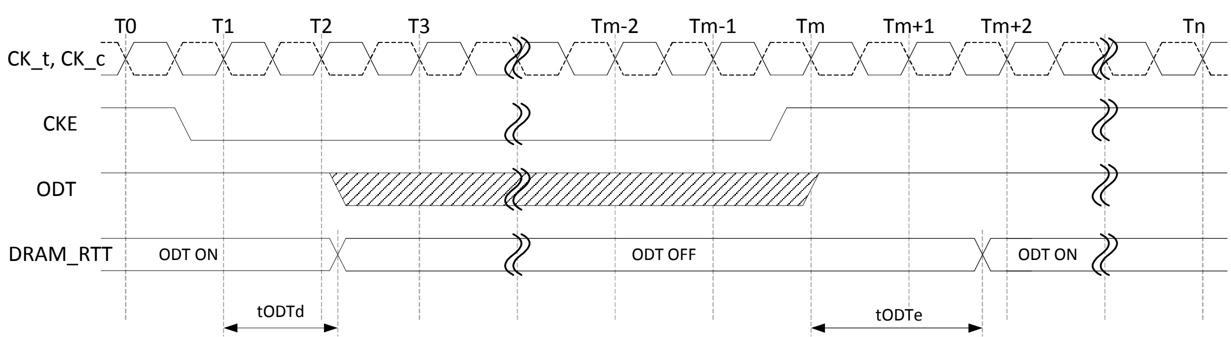
Figure 49 — Automatic ODT Timing During READ Operation Eaxample for RL = *m*



NOTE 1 The automatic R_{TT} turn-off delay, $t_{AODToff}$, is referenced from the rising edge of "RL-2" clock at T_{m-2}.

NOTE 2 The automatic R_{TT} turn-on delay, t_{AODTon}, is referenced from the rising edge of "RL+ BL/2" clock at T_{m+4}.

Figure 50 — ODT Timing During Power Down, Self Refresh, Deep Power Down Entry/Exit Example



NOTE 1 Upon exit of Deep Power Down mode, a complete power-up initialization sequence is required.

4.13 Power-down

Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down I_{DD} specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 51 on page 63 through Figure 62 on page 67.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as t_{CPDED}. CKE LOW will result in deactivation of input receivers after t_{CPDED} has expired. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until $t_{CKE,min}$ is satisfied. V_{REFCA} must be maintained at a valid level during power-down.

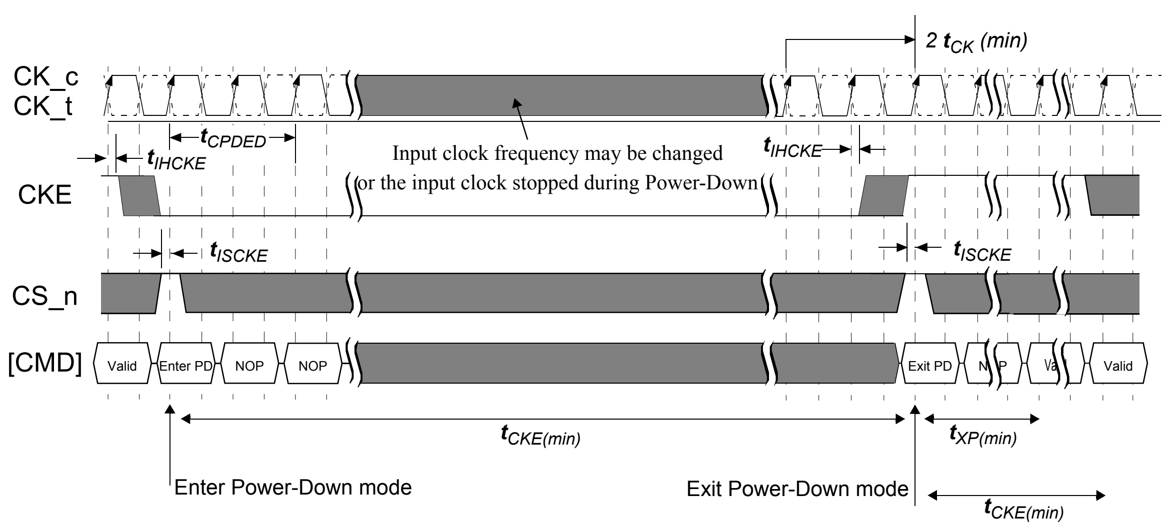
V_{DDQ} can be turned off during power-down. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting power-down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until $t_{CKE,min}$ is satisfied. A valid, executable command can be applied with power-down exit latency t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see section On-Die Termination on page 60.

Figure 51 — Basic Power-Down Entry and Exit Timing



NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

4.13 Power-down (cont'd)

Figure 52 — CKE-Intensive Environment

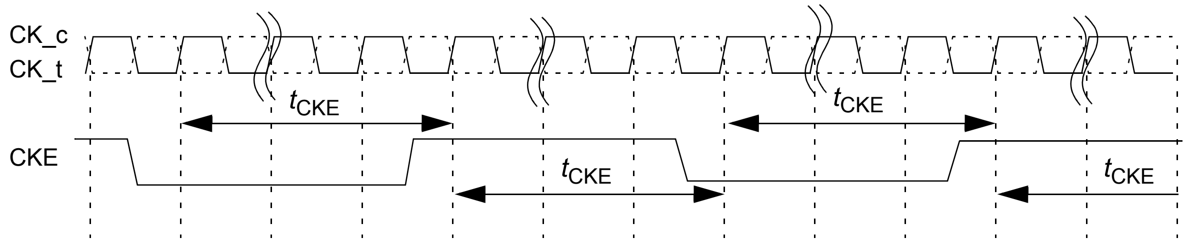
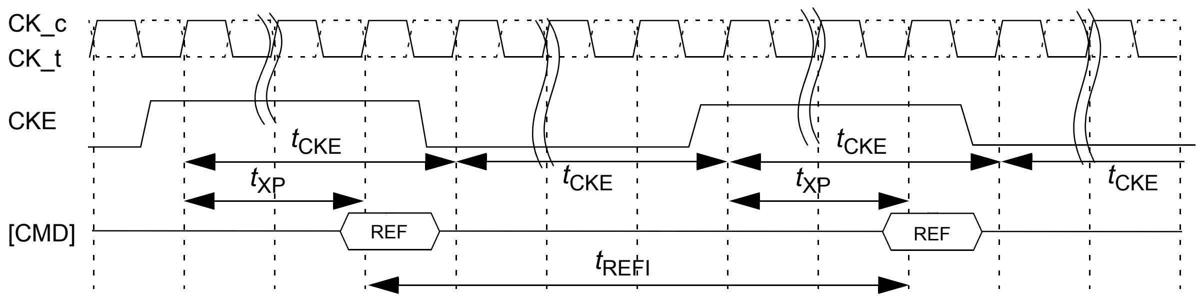
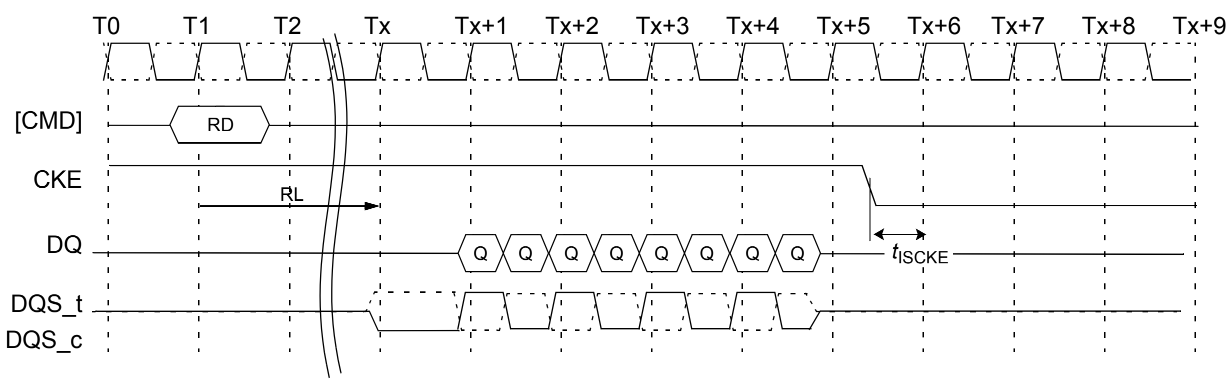


Figure 53 — REFRESH-to-REFRESH Timing in CKE-Intensive Environments



NOTE 1 The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure 54 — READ to Power-Down Entry

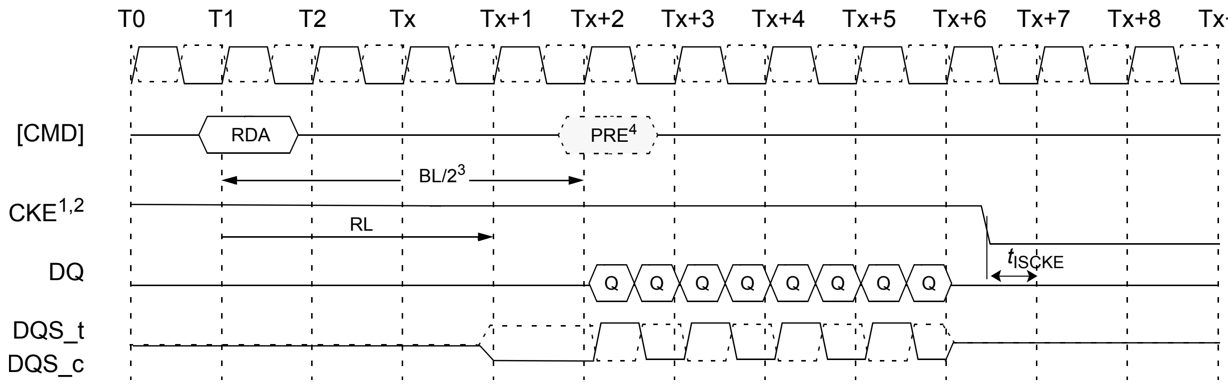


NOTE 1 CKE must be held HIGH until the end of the burst operation.

NOTE 2 CKE can be registered LOW at RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 clock cycles after the clock on which the READ command is registered.

4.13 Power-down (cont'd)

Figure 55 — READ with Auto Precharge to Power-Down Entry



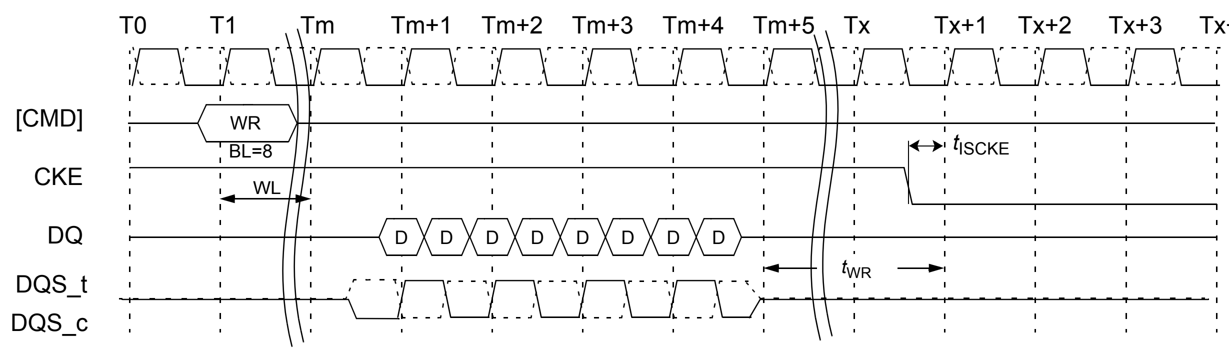
NOTE 1 CKE must be held HIGH until the end of the burst operation.

NOTE 2 CKE can be registered LOW at RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.

NOTE 3 BL/2 with t_{RTP} = 7.5ns and $t_{RAS(MIN)}$ is satisfied.

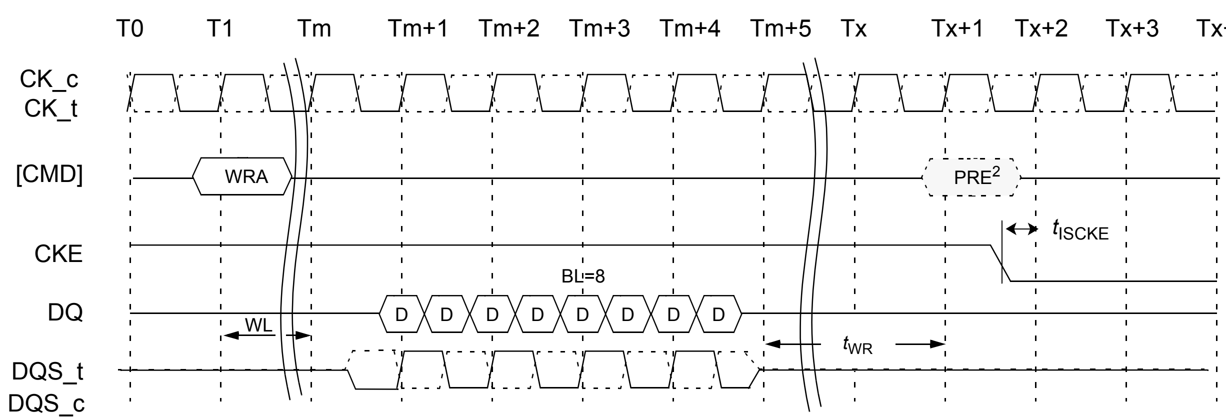
NOTE 4 Start internal PRECHARGE.

Figure 56 — WRITE to Power-Down Entry



NOTE 1 CKE can be registered LOW at WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) clock cycles after the clock on which the WRITE command is registered.

Figure 57 — WRITE with Auto Precharge to Power-Down Entry

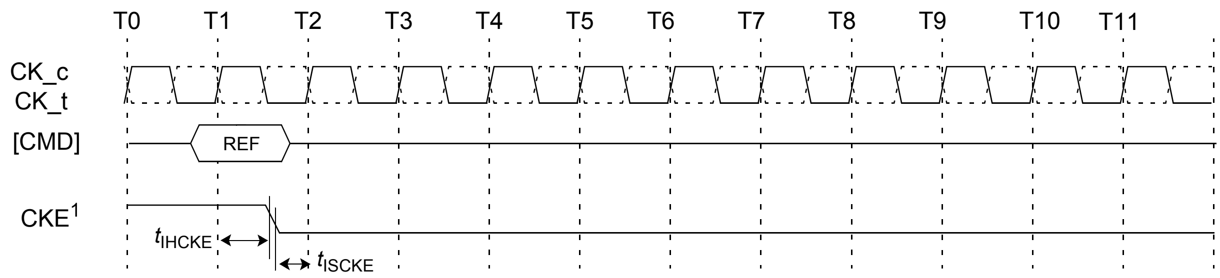


NOTE 1 CKE can be registered LOW at WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1 clock cycles after the WRITE command is registered.

NOTE 2 Start internal PRECHARGE.

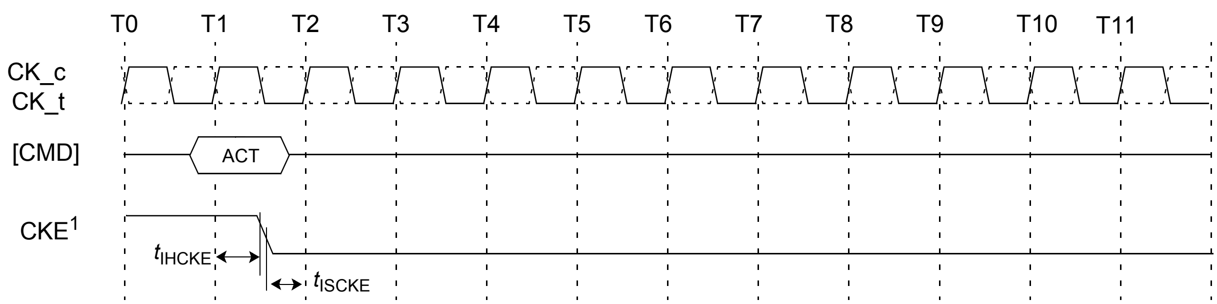
4.13 Power-down (cont'd)

Figure 58 — REFRESH Command to Power-Down Entry



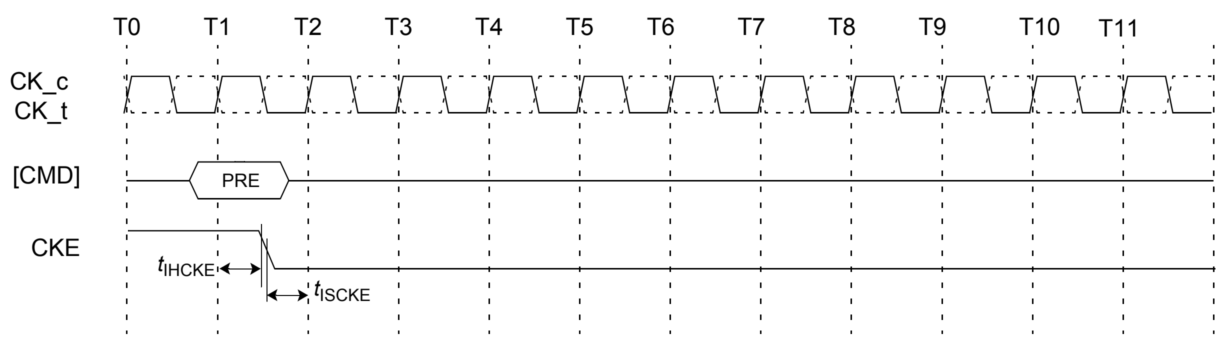
NOTE 1 CKE can go LOW tIHCKE after the clock on which the REFRESH command is registered.

Figure 59 — ACTIVATE Command to Power-Down Entry



NOTE 1 CKE can go LOW at t_{IHCKE} after the clock on which the ACTIVATE command is registered.

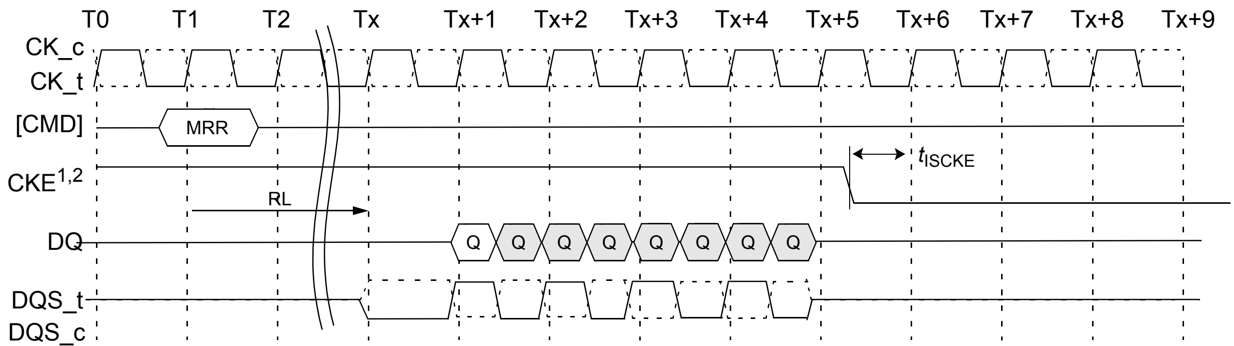
Figure 60 — PRECHARGE Command to Power-Down Entry



NOTE 1 CKE can go LOW t_{IHCKE} after the clock on which the PRECHARGE command is registered.

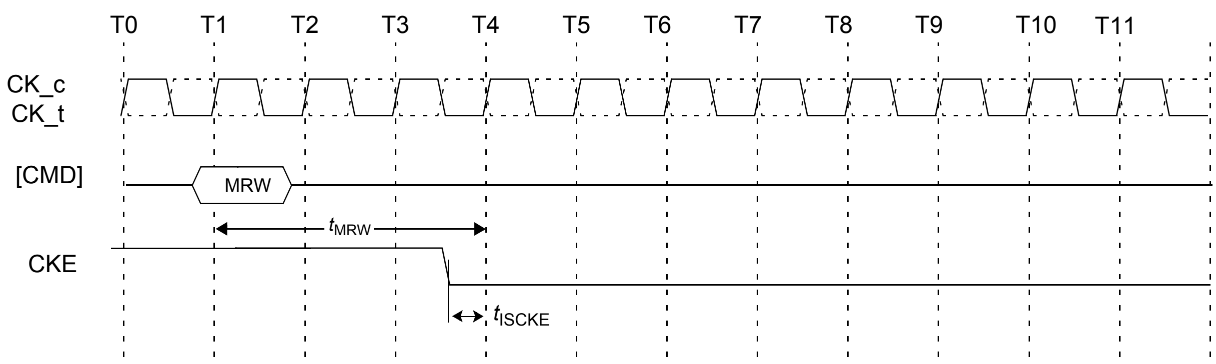
4.13 Power-down (cont'd)

Figure 61 — MRR to Power-Down Entry



NOTE 1 CKE can be registered LOW RL + RU(t_{DQSCK}/t_{CK})+ BL/2 + 1 clock cycles after the clock on which the MRR command is registered.
NOTE 2 CKE should be held high until the end of the burst operation.

Figure 62 — MRW to Power-Down Entry



NOTE 1 CKE can be registered LOW t_{MRW} after the clock on which the MRW command is registered.

4.14 Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW. The contents of the SDRAM will be lost upon entry into Deep Power-Down mode.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as t_{CPDED}. CKE LOW will result in deactivation of command and address receivers after t_{CPDED} has expired. All power supplies must be within specified limits prior to exiting Deep Power-Down. V_{refDQ} and V_{refCA} may be at any level within minimum and maximum levels (see Abolute Maximum Ratings). However prior to exiting Deep Power-Down, V_{ref} must be within specified limits (See Recommended DC Operating Conditions).

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting t_{ISCKE} with a stable clock input. The SDRAM must be fully re-initialized as described in the power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence is completed. For the description of ODT operation and specifications during DPD entry and exit, see section On-Die Termination on page 60.

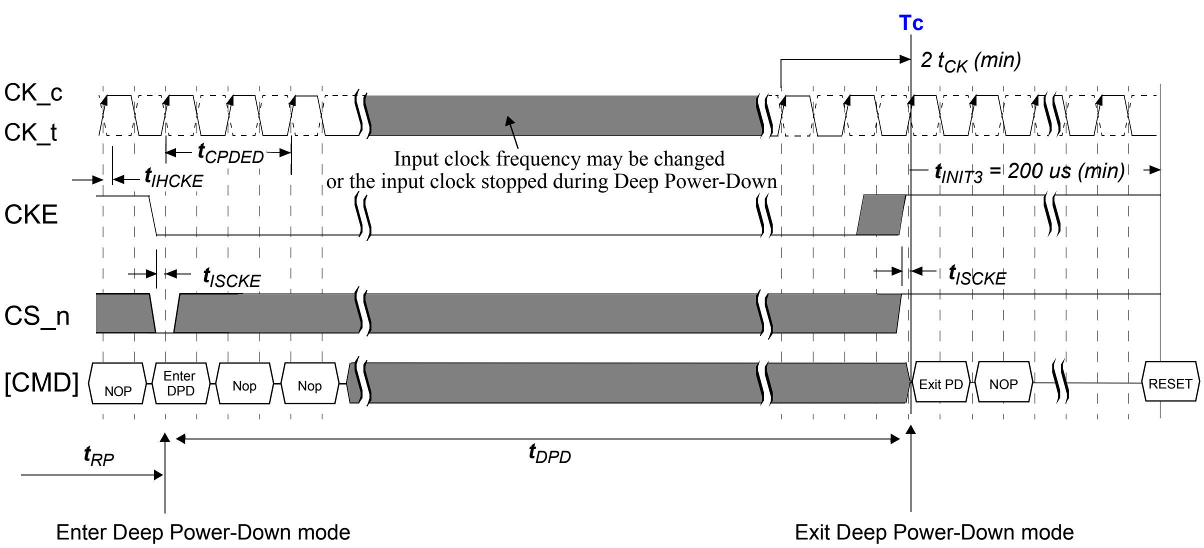


Figure 63 — LPDDR3: Deep power down entry and exit timing diagram

NOTE 1 Initialization sequence may start at any time after Tc.

NOTE 2 t_{INIT3}, and Tc refer to timings in the LPDDR3 initialization sequence. For more detail, see Power-Up and Initialization.

NOTE 3 Input clock frequency may be changed or the input clock can be stopped or floated during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

4.15 Input clock stop and frequency change

LPDDR3 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR3 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR3 SDRAM is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2*t_{CK} + t_{XP}$.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR3 SDRAM is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2*t_{CK} + t_{XP}$.

4.16 No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR3 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

4.17 Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

4.17.1 Command Truth Table

Table 24 — Command Truth Table

	SDR Command Pins			DDR CA pins (10)										
SDRAM Command	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK_t EDGE
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	X								
Refresh (per bank)[11]	H	H	L	L	L	H	L	X						
			X	X										
Refresh (all bank)	H	H	L	L	L	H	H	X						
			X	X										
Enter Self Refresh	H	L	L	L	L	H	X							
	X		X	X										
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Precharge (pre bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
			X	X	X	X	X	X	X	X	X	X	X	
Enter Deep Power Down	H	L	L	H	H	L	X							
	X		X	X										
NOP	H	H	L	H	H	H	X							
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							
			X	X										
NOP	H	H	H	X										
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	H	X										
			X	X										
Enter Power Down	H	L	H	X										
	X		X	X										
Exit PD, SREF, DPD	L	H	H	X										
	X		X	X										

4.17.1 Command Truth Table (cont'd)

Notes to Table 24

NOTE 1 All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.

NOTE 3 AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

NOTE 4 "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case CS_n, CK_t/CK_c, and CA can be floated.

NOTE 5 Self refresh exit and Deep Power Down exit are asynchronous.

NOTE 6 V_{REF} must be between 0 and V_{DDQ} during Self Refresh and Deep Power Down operation.

NOTE 7 CAxr refers to command/address bit "x" on the rising edge of clock.

NOTE 8 CAxf refers to command/address bit "x" on the falling edge of clock.

NOTE 9 CS_n and CKE are sampled at the rising edge of clock.

NOTE 10 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 11 AB "high"during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

4.17.2 CKE Truth Table

Table 25 — LPDDR3: CKE Table[1,2]

Device Current State*3	CKE$_{n-1}$*4	CKE$_{n}$*4	CS_n*5	Command n*6	Operation n*6	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	7
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	7
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	7, 10
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	11
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Enter Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE 1 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 2 'X' means 'Don't care'.

NOTE 3 "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.

NOTE 4 "CKE$_{n}$" is the logic state of CKE at clock rising edge n; "CKE$_{n-1}$" was the state of CKE at the previous clock edge.

NOTE 5 "CS_n" is the logic state of CS_n at the clock rising edge n;

NOTE 6 "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".

NOTE 7 Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XP} period.

NOTE 8 Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XSR} time.

NOTE 9 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.

NOTE 10 Upon exiting Resetting Power Down, the device will return to the Idle state if t_{INIT5} has expired.

NOTE 11 In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

4.17.3 State Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

Table 26 — Current State Bank *n* - Command to Bank *n*

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	8
	Precharge	Deactivate row in bank or banks	Precharging	9, 14
Row Active	Read	Select column, and start read burst	Reading	11
	Write	Select column, and start write burst	Writing	11
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 13
Power On	Reset	Begin Device Auto-Initialization	Resetting	8
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: The bank or banks have been precharged, and t_{RP} has been met.

Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accessesare in progress.

Reading: A Read burst has been initiated, with Auto Precharge disabled.

Writing: A Write burst has been initiated, with Auto Precharge disabled.

NOTE 4 The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 2, and according to Table 3.

Precharging: starts with the registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'Active' state.

Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.

Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

4.17.3 State Truth Tables (cont'd)

Table 26, Notes (cont'd)

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when t_{RFCpb} is met. Once t_{RFCpb} is met, the bank will be in an 'idle' state.

Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when t_{RFCab} is met. Once t_{RFCab} is met, the device will be in an 'all banks idle' state.

Idle MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.

MR Writing: starts with the registration of an MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.

Precharging All: starts with the registration of a Precharge-All command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

NOTE 6 Bank-specific; requires that the bank is idle and no bursts are in progress.

NOTE 7 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 8 Not bank-specific reset command is achieved through Mode Register Write command.

NOTE 9 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 10 A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

NOTE 11 The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

NOTE 12 A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.

NOTE 13 A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

NOTE 14 If a Precharge command is issued to a bank in the Idle state, t_{RP} shall still apply.

4.17.3 State Truth Tables (cont'd)

Table 27 — Current State Bank *n* - Command to Bank *m*

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank *m*	
Idle	Any	Any command allowed to Bank *m*	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank *m*	Active	6
	Read	Select column, and start read burst from Bank *m*	Reading	7
	Write	Select column, and start write burst to Bank *m*	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9, 10, 12
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank *m*	Reading	7
	Write	Select column, and start write burst to Bank *m*	Writing	7, 13
	Activate	Select and activate row in Bank *m*	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank *m*	Reading	7, 15
	Write	Select column, and start write burst to Bank *m*	Writing	7
	Activate	Select and activate row in Bank *m*	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank *m*	Reading	7, 14
	Write	Select column, and start write burst to Bank *m*	Writing	7, 13, 14
	Activate	Select and activate row in Bank *m*	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Autoprecharge	Read	Select column, and start read burst from Bank *m*	Reading	7, 14, 15
	Write	Select column, and start write burst to Bank *m*	Writing	7, 14
	Activate	Select and activate row in Bank *m*	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-Initialization	Resetting	11, 16
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: the bank has been precharged, and t_{RP} has been met.

Active: a row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Reading: a Read burst has been initiated, with Auto Precharge disabled.

Writing: a Write burst has been initiated, with Auto Precharge disabled.

NOTE 4 Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.

4.17.3 State Truth Tables (cont'd)

Table 27, Notes (cont'd)

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

Idle MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.

MR Writing: starts with the registration of an MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.

NOTE 6 t_{RRD} must be met between Activate command to Bank *n* and a subsequent Activate command to Bank *m*. Additionally, in the case of multiple banks activated, t_{FAW} must be satisfied.

NOTE 7 Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

NOTE 8 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 9 MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)

NOTE 10 MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.

NOTE 11 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 12 The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when an MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.

NOTE 13 A Write command may be applied after the completion of the Read burst, burst terminates are not permitted..

NOTE 14 Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the precharge and auto-precharge clarification table are followed.

NOTE 15 A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

NOTE 16 Reset command is achieved through Mode Register Write command.

4.17.3.1 Data Mask Truth Table

Table 28 provides the data mask truth table.

Table 28 — DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data.

5 Absolute Maximum Ratings

5.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 29 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.6	V	1
V_{DDCA} supply voltage relative to V_{SSCA}	V_{DDCA}	-0.4	1.6	V	1,2
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.6	V	1,3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	4

NOTE 1 See “Power-Ramp” section in “Power-up, Initialization, and Power-off” on page 12 for relationships between power supplies.

NOTE 2 $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$ provided that $V_{REFCA} \leq 300mV$.

NOTE 3 $V_{REFDQ} \leq 0.6 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.

NOTE 4 Storage Temperature is the case surface temperature on the center/top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

6 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

6.1 Recommended DC Operating Conditions

Table 30 — Recommended DC Operating Conditions

Symbol	Voltage			DRAM	Unit
	Min	Typ	Max		
V_{DD1}	1.70	1.80	1.95	Core Power1	V
V_{DD2}	1.14	1.20	1.30	Core Power2	V
V_{DDCA}	1.14	1.20	1.30	Input Buffer Power	V
V_{DDQ}	1.14	1.20	1.30	I/O Buffer Power	V

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

6.2 Input Leakage Current

Table 31 — Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-2	2	uA	1, 2
V_{REF} supply leakage current	I_{VREF}	-1	1	uA	3, 4

NOTE 1 For CA, CKE, CS_n, CK_t, CK_c. Any input 0V ≤ V_{IN} ≤ V_{DDCA} (All other pins not under test = 0V)

NOTE 2 Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

NOTE 3 Minimum limit requirement is for testing purposes. Leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

NOTE 4 $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$. (All other pins not under test = 0V)

6.3 Operating Temperature Range

Table 32 — Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	^oC
Elevated		85	105	^oC

NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 2 Some applications require operation of LPDDR3 in the maximum temperature conditions in the Elevated Temperature Range between 85 ^oC and 105 ^oC case temperature. For LPDDR3 devices, derating may be neccessary to operate in this range. See MR4 on page 22.

NOTE 3 Either the device case temperature rating or the temperature sensor (See “Temperature Sensor” on page 51) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85 ^oC when the temperature sensor indicates a temperature of less than 85 ^oC.

7 AC and DC Input Measurement Levels

7.1 AC and DC Logic Input Levels for Single-Ended Signals

7.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

Table 33 — Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCA}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	V	1, 2
V_{IHCA}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDCA}	V	1
V_{ILCA}(DC)	DC input logic low	V_{SSCA}	V_{Ref} - 0.100	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS_n inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3, 4

NOTE 1 For CA and CS_n input only pins. $V_{Ref} = V_{RefCA(DC)}$.

NOTE 2 See “Overshoot and Undershoot Specifications” on page 92

NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than +/-1% V_{DDCA} (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. V_{DDCA}/2 +/- 12 mV.

7.1.2 AC and DC Input Levels for CKE

Table 34 — Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.65 * V_{DDCA}	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.35 * V_{DDCA}	V	1

Note 1 See “Overshoot and Undershoot Specifications” on page 92

7.1.3 AC and DC Input Levels for Single-Ended Data Signals

Table 35 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHDQ}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDQ}	V	1
V_{ILDQ}(DC)	DC input logic low	V_{SSQ}	V_{Ref}- 0.100	V	1
$V_{RefDQ(DC)}$ (DQ ODT disabled)	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3, 4
$V_{RefDQ(DC)}$ (DQ ODT enabled)	Reference Voltage for DQ, DM inputs	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V	3, 5, 6

NOTE 1 For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

NOTE 2 See “Overshoot and Undershoot Specifications” on page 92

NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% V_{DDQ} (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. V_{DDQ}/2 +/- 12 mV.

NOTE 5 For reference: approx. V_{ODTR}/2 +/- 12 mV.

NOTE 6 R_{ON} and R_{ODT} nominal mode register programmed values are used for the calculation of V_{ODTR}.

.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

7.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 64. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). V_{DD} stands for V_{DDCA} for V_{RefCA} and V_{DDQ} for V_{RefDQ}. $V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA} also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 33. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than +/- 1% V_{DD}. $V_{Ref}(t)$ cannot track noise on V_{DDQ} or V_{DDCA} if this would send V_{Ref} outside these specifications.

:

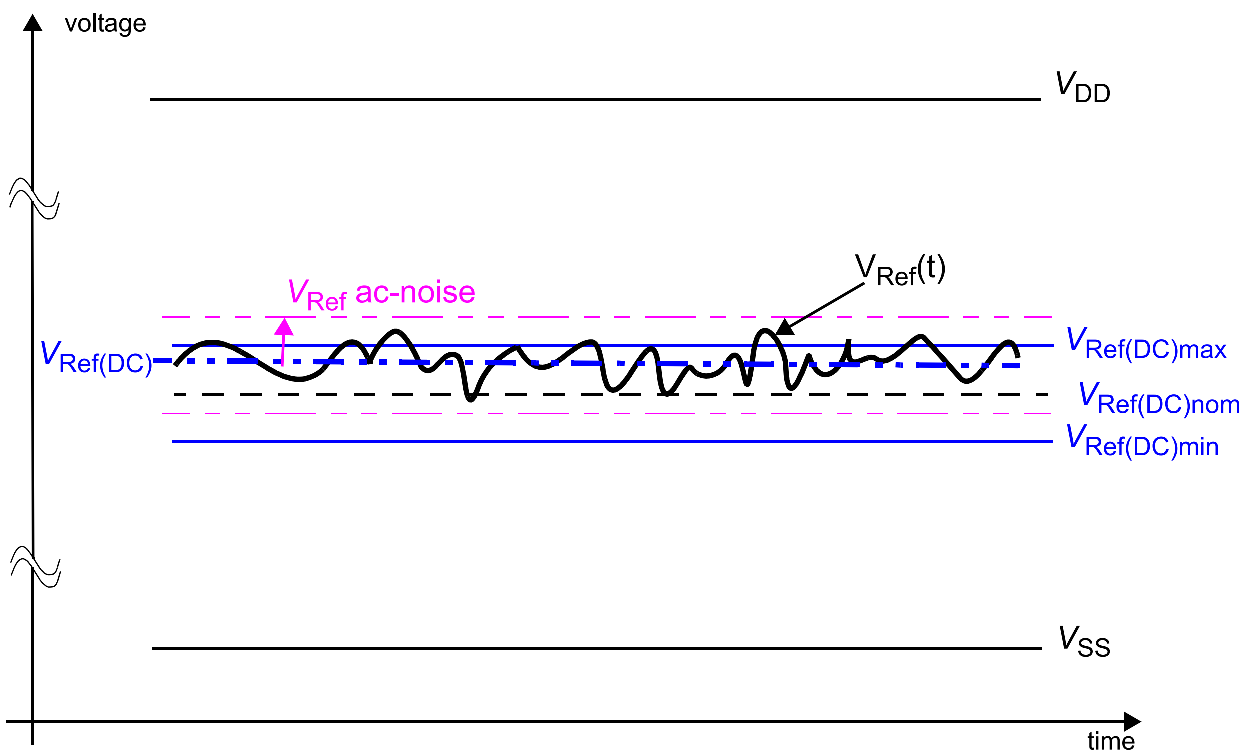


Figure 64 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}. "V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in Figure 64.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of V_{DD}) are included in LPDDR3 timings and their associated deratings.

7.3 Input Signal

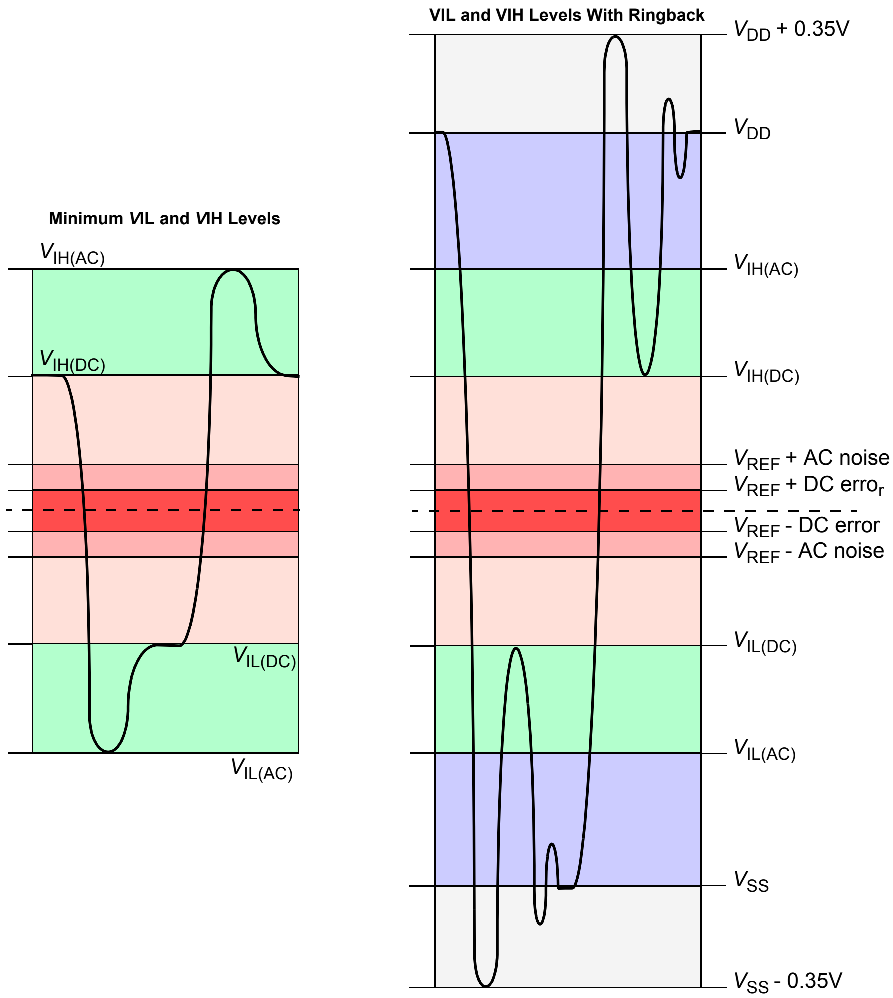


Figure 65 — LPDDR3 Input Signal

NOTE 1 Numbers reflect nominal values.

NOTE 2 For CA0-9, CK_t, CK_c,and CS_n, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ}.

NOTE 3 For CA0-9, CK_t, CK_c, and CS_n, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS_t, and DQS_c, V_{SS} stand for V_{SSQ}.

7.4 AC and DC Logic Input Levels for Differential Signals

7.4.1 Differential signal definition

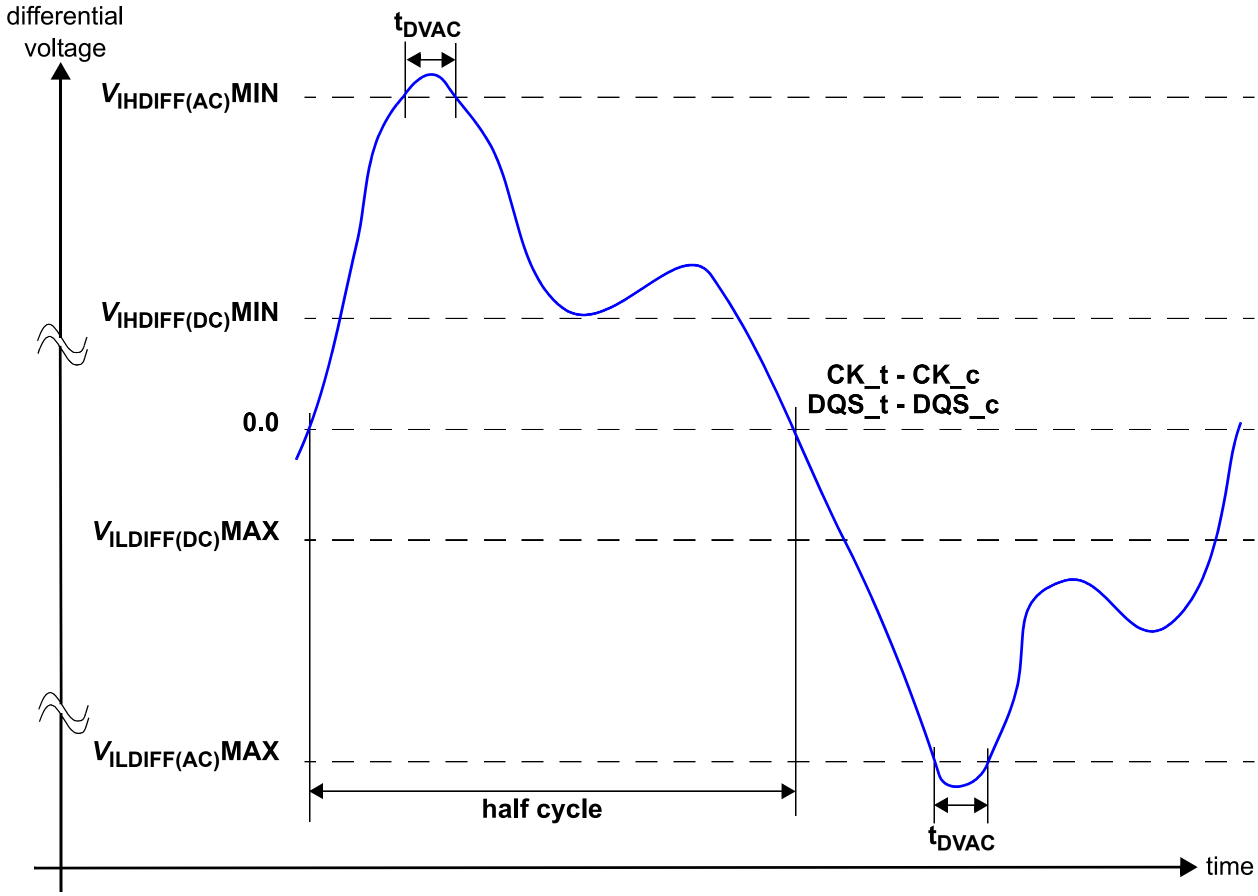


Figure 66 — Definition of differential ac-swing and “time above ac-level” t_{DVAC}

7.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

Table 36 — Differential AC and DC Input Levels

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{IHdiff(dc)}$	Differential input high	2 x (V_{IH}(dc) - V_{Ref})	note 3	V	1
$V_{ILdiff(dc)}$	Differential input low	Note 3	2 x (V_{IL}(dc) - V_{Ref})	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (V_{IH}(ac) - V_{Ref})	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (V_{IL}(ac) - V_{Ref})	V	2

NOTE 1 Used to define a differential signal slew-rate. For CK_t - CK_c use $V_{IH}/V_{IL(dc)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(dc)}$ of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

NOTE 2 For CK_t - CK_c use $V_{IH}/V_{IL(ac)}$ of CA and V_{REFCA}; for DQS_t - DQS_c, use $V_{IH}/V_{IL(ac)}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3 These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits ($V_{IH(dc)}$ max, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 92.

NOTE 4 For CK_t and CK_c, $V_{Ref} = V_{RefCA(DC)}$. For DQS_t and DQS_c, $V_{Ref} = V_{RefDQ(DC)}$.

7.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c) (cont'd)

Table 37 — Allowed time before ringback t_{DVAC} for DQS_t/DQS_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1333Mbps		t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1600Mbps	
	min	max	min	max
> 8.0	58	-	48	-
8.0	58	-	48	-
7.0	56	-	46	-
6.0	53	-	43	-
5.0	50	-	40	-
4.0	45	-	35	-
3.0	37	-	27	-
< 3.0	37	-	27	-

Table 38 — Allowed time before ringback t_{DVAC} for CK_t/CK_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1333Mbps		t_{DVAC} [ps] @ $\lvert V_{IH/Ldiff(ac)}\rvert$ = 300mV 1600Mbps	
	min	max	min	max
> 8.0	58	-	48	-
8.0	58	-	48	-
7.0	56	-	46	-
6.0	53	-	43	-
5.0	50	-	40	-
4.0	45	-	35	-
3.0	37	-	27	-
< 3.0	37	-	27	-

7.4.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle.

DQS_t, DQS_c shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

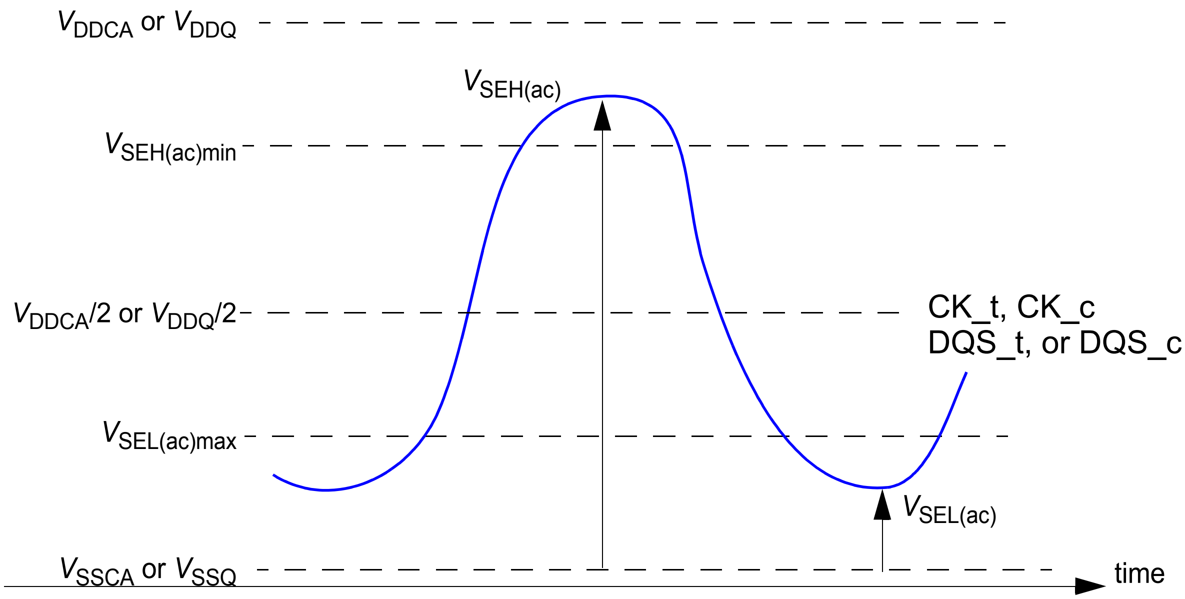


Figure 67 — Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS_t, DQS_c and $V_{DDCA}/2$ for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(ac)max}$, $V_{SEH(ac)min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK_t, CK_c, DQS_t, and DQS_c are found in tables 33 and 35, respectively.

Table 39 — Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{SEH(AC)}$	Single-ended high-level for strobes	$(V_{DDQ} / 2) + 0.150$	note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	$(V_{DDCA} / 2) + 0.150$	note 3	V	1, 2
$V_{SEL(AC)}$	Single-ended low-level for strobes	note 3	$(V_{DDQ} / 2) - 0.150$	V	1, 2
	Single-ended low-level for CK_t, CK_c	note 3	$(V_{DDCA} / 2) - 0.150$	V	1, 2

NOTE 1 For CK_t, CK_c use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

NOTE 2 $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, ho\wever the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)\ max}$, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 92

7.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 39. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

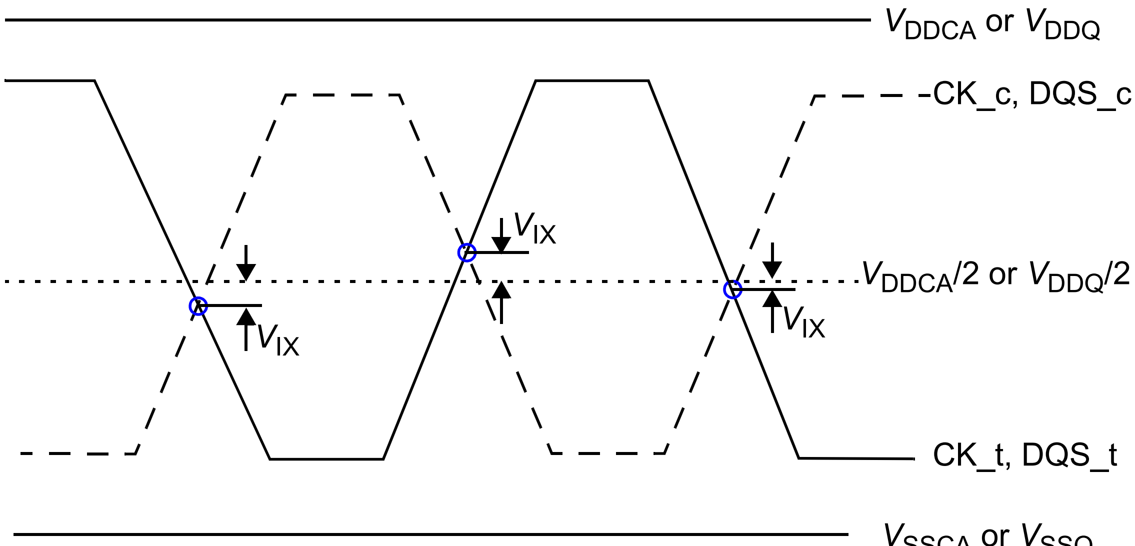


Figure 68 — V_{IX} Definition

Table 40 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK_t, CK_c	- 120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c	- 120	120	mV	1,2

NOTE 1 The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

NOTE 2 For CK_t and CK_c, $V_{Ref} = V_{RefCA(DC)}$. For DQS_t and DQS_c, $V_{Ref} = V_{RefDQ(DC)}$.

7.6 Slew Rate Definitions for Single-Ended Input Signals

See "CA and CS_n Setup, Hold and Derating" on page 119 for single-ended slew rate definitions for address and command signals.

See "Data Setup, Hold and Slew Rate Derating" on page 125 for single-ended slew rate definitions for data signals.

7.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 41 and Figure 69.

Table 41 — Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff
NOTE 1 The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.			

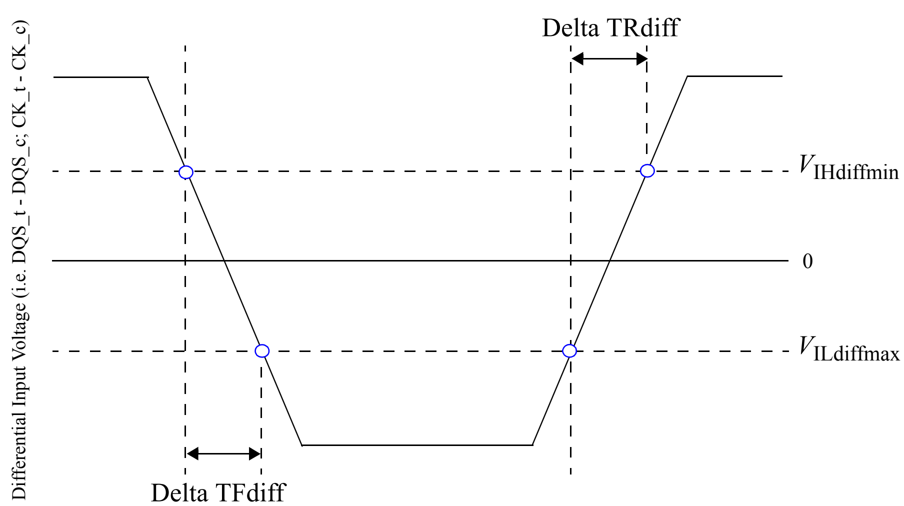


Figure 69 — Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

8 AC and DC Output Measurement Levels

8.1 Single Ended AC and DC Output Levels

Table 42 shows the output levels used for measurements of single ended signals.

Table 42 — Single-ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$ ODT disabled	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OL(DC)}$ ODT enabled	DC output low measurement level (for IV curve linearity)		V_{DDQ} x [0.1 + 0.9 x (R_{ON} / (R_{TT} + R_{ON}))]	V	3
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; 0V $\le$ V_{OUT} $\le$ V_{DDQ}	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta R_{ON} between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE 1 I_{OH} = -0.1mA.

NOTE 2 I_{OL} = 0.1mA.

NOTE 3 The min value is derived when using $R_{TT,\ min}$ and $R_{ON,max}$ (+/- 30% uncalibrated, +/-15% calibrated).

8.2 Differential AC and DC Output Levels

Table 43 shows the output levels used for measurements of differential signals (DQS_t, DQS_c).

Table 43 — Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	2

NOTE 1 I_{OH} = -0.1mA.

NOTE 2 I_{OL} = 0.1mA

8.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 44 and Figure 70.

Table 44 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

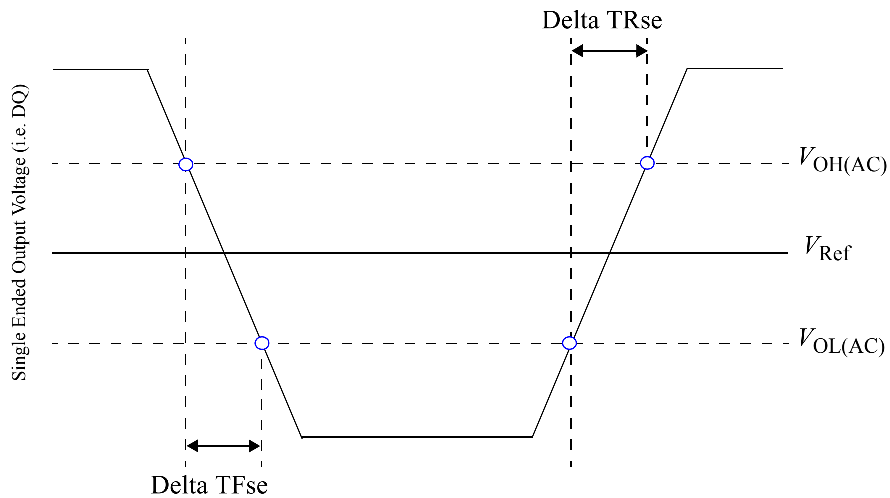


Figure 70 — Single Ended Output Slew Rate Definition

Table 45 — Output Slew Rate (single-ended)

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (RON = 40W +/- 30%)	SRQse	1.5	4.0	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
NOTE 1 Measured with output reference load.
NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
NOTE 3 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 46 and Figure 71.

Table 46 — Differential Output Slew Rate Definition

Description	Measured from	Measured to	Defined by
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

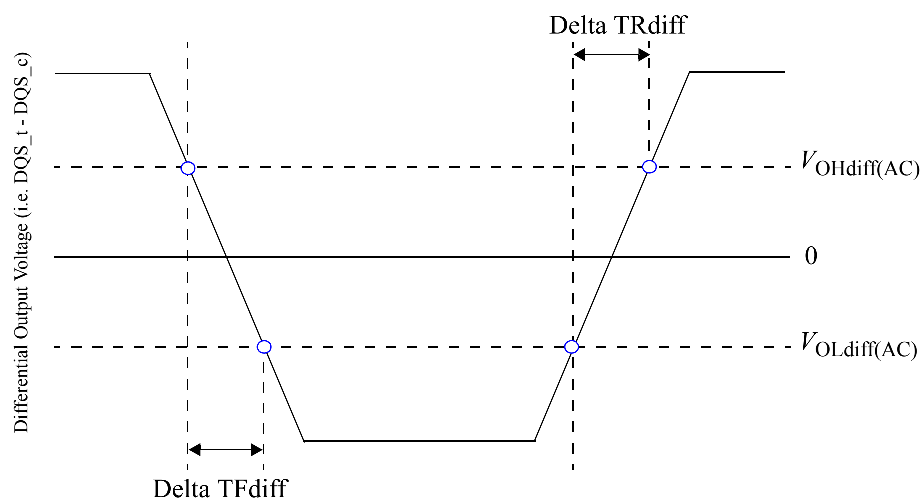


Figure 71 — Differential Output Slew Rate Definition

Table 47 — Differential Output Slew Rate

Parameter	Symbol	Value Min	Value Max	Units
Differential Output Slew Rate (R_{ON} = 40W +/- 30%)	SRQdiff	3.0	8.0	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.5 Overshoot and Undershoot Specifications

Table 48 — AC Overshoot/Undershoot Specification

Parameter		1333	1600	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 72)	Max	0.35		V
Maximum peak amplitude allowed for undershoot area. (See Figure 72)	Max	0.35		V
Maximum area above VDD. (See Figure 72)	Max	0.12	0.10	V-ns
Maximum area below VSS. (See Figure 72)	Max	0.12	0.10	V-ns

NOTE 1 V_{DD} stands for V_{DDCA} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, ODT, DQS_t, and DQS_c.
NOTE 1 V_{SS} stands for V_{SSCA} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, ODT, DQS_t, and DQS_c.

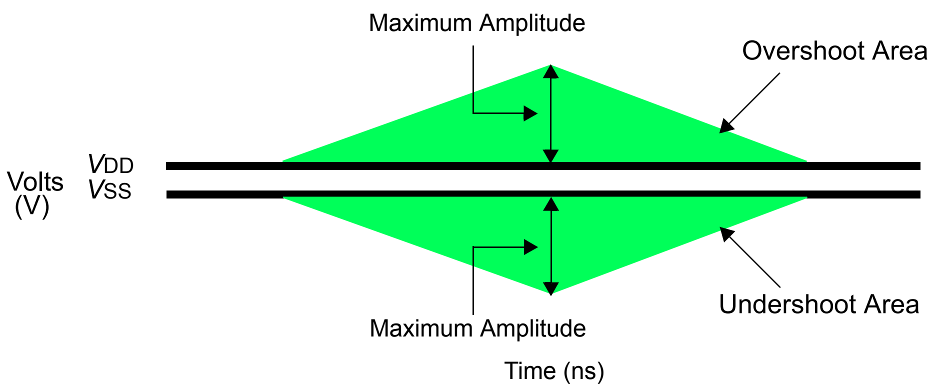


Figure 72 — Overshoot and Undershoot Definition

NOTE 1 V_{DD} stands for V_{DDCA} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, ODT, DQS_t, and DQS_c.
NOTE 2 V_{SS} stands for V_{SSCA} for CA[9:0], CK_t, CK_c, CS_n, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, ODT, DQS_t, and DQS_c.
NOTE 3 Absolute maximum requirements apply.

8.6 Output buffer characteristics

8.6.1 HSUL_12 Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

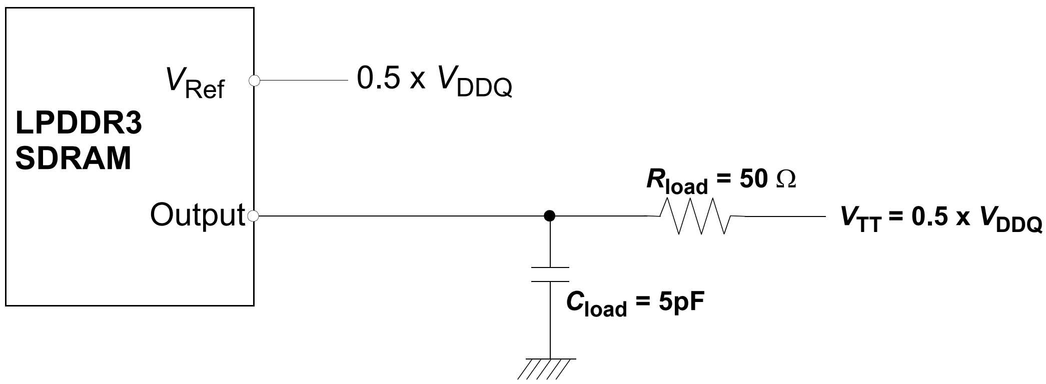


Figure 73 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE 1: All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

8.7 R_{ONPU} and R_{ONPD} Resistor Definition

$$R_{ONPU} = \frac{(V_{DDQ} - V_{out})}{ABS(I_{out})}$$

NOTE 1: This is under the condition that R_{ONPD} is turned off

$$R_{ONPD} = \frac{V_{out}}{ABS(I_{out})}$$

NOTE 1: This is under the condition that R_{ONPU} is turned off

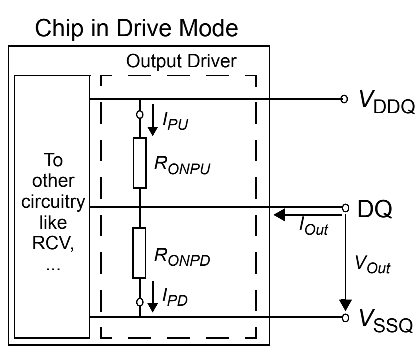


Figure 74 — Output Driver: Definition of Voltages and Currents

8.7.1 R_{ONPU} and R_{ONPD} Characteristics with ZQ Calibration

Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ}. Nominal R_{ZQ} is 240Ω.

Table 49 — Output Driver DC Electrical Characteristics with ZQ Calibration

$R_{ON,NOM}$	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3W	R_{ON34PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/7$	1,2,3,4
	R_{ON34PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/7$	1,2,3,4
40.0W	R_{ON40PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/6$	1,2,3,4
	R_{ON40PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/6$	1,2,3,4
48.0W	R_{ON48PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/5$	1,2,3,4
	R_{ON48PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/5$	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2 R_{ZQ} = 240Ω.

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}.

NOTE 5 Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure R_{ONPU} and R_{ONPD}, both at 0.5 x V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

For example, with $MM_{PUPD(max)}$ = 15% and R_{ONPD} = 0.85, R_{ONPU} must be less than 1.0.

NOTE 6 Output driver strength measured without ODT.

8.7.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 50 — Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
R_{ONPD} / R_{ONPU}	0.5 x V_{DDQ}	$85 - (dRONdT \times \lvert\Delta T\rvert) - (dRONdV \times \lvert\Delta V\rvert)$	$115 + (dRONdT \times \lvert\Delta T\rvert) + (dRONdV \times \lvert\Delta V\rvert)$	%	1,2
R_{TT}	0.5 x V_{DDQ}	$85 - (dRTTdT \times \lvert\Delta T\rvert) - (dRTTdV \times \lvert\Delta V\rvert)$	$115 + (dRTTdT \times \lvert\Delta T\rvert) + (dRTTdV \times \lvert\Delta V\rvert)$	%	1,2

NOTE 1 $\Delta T = T - T$(@ calibration), $\Delta V = V - V$(@ calibration)

NOTE 2 $dR_{ON}dT$, $dR_{ON}dV$, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.

4.17.3 Output Driver Temperature and Voltage Sensitivity (cont'd)

Table 51 — Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	% / C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	% / mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	% / C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.20	% / mV

8.7.3 R_{ONPU} and R_{ONPD} Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by design and characterization as default setting.

Table 52 — Output Driver DC Electrical Characteristics without ZQ Calibration

$R_{ON,NOM}$	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3W	R_{ON34PD}	0.5 x V_{DDQ}	24	34.3	44.6	W	1
	R_{ON34PU}	0.5 x V_{DDQ}	24	34.3	44.6	W	1
40.0W	R_{ON40PD}	0.5 x V_{DDQ}	28	40	52	W	1
	R_{ON40PU}	0.5 x V_{DDQ}	28	40	52	W	1
48.0W	R_{ON48PD}	0.5 x V_{DDQ}	33.6	48	62.4	W	1
	R_{ON48PU}	0.5 x V_{DDQ}	33.6	48	62.4	W	1
60.0W (optional)	R_{ON60PD}	0.5 x V_{DDQ}	42	60	78	W	1
	R_{ON60PU}	0.5 x V_{DDQ}	42	60	78	W	1
80.0W (optional)	R_{ON80PD}	0.5 x V_{DDQ}	56	80	104	W	1
	R_{ON80PU}	0.5 x V_{DDQ}	56	80	104	W	1

NOTE 1 Across entire operating temperature range, without calibration.

8.7.4 R_{ZQ} I-V Curve

Table 53 — R_{ZQ} I-V Curve

Voltage[V]	R_{ON} = 240W (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current [mA] / R_{ON} [Ohms]				Current [mA] / R_{ON} [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

8.7.4 R_{ZQ} I-V Curve (cont'd)

Figure 75 — I-V Curve After ZQ Reset

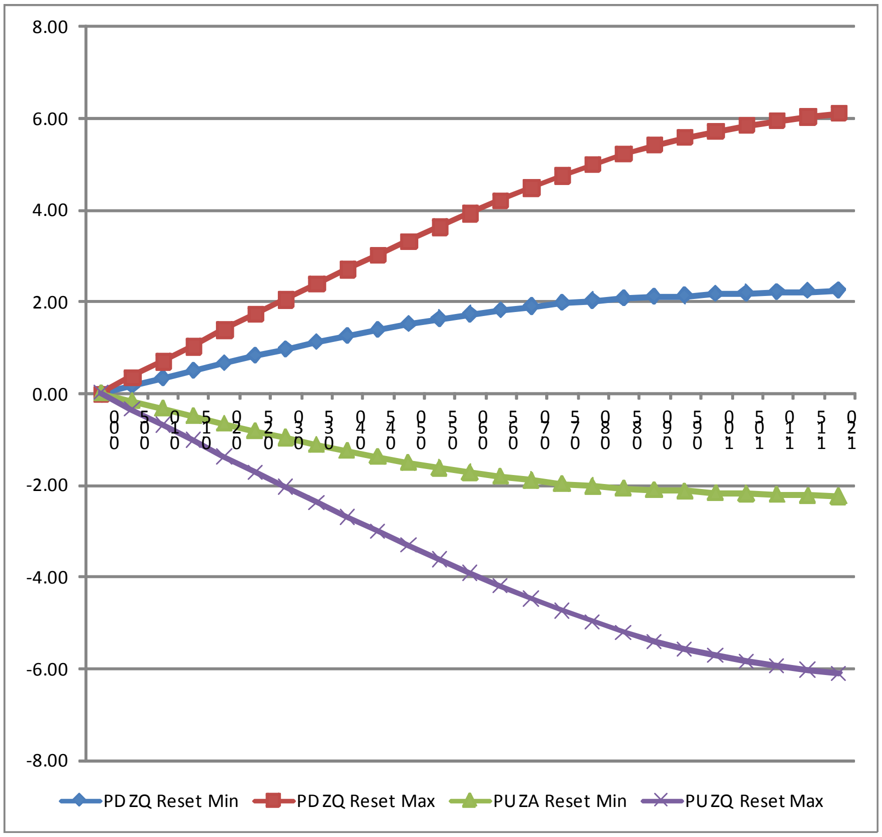
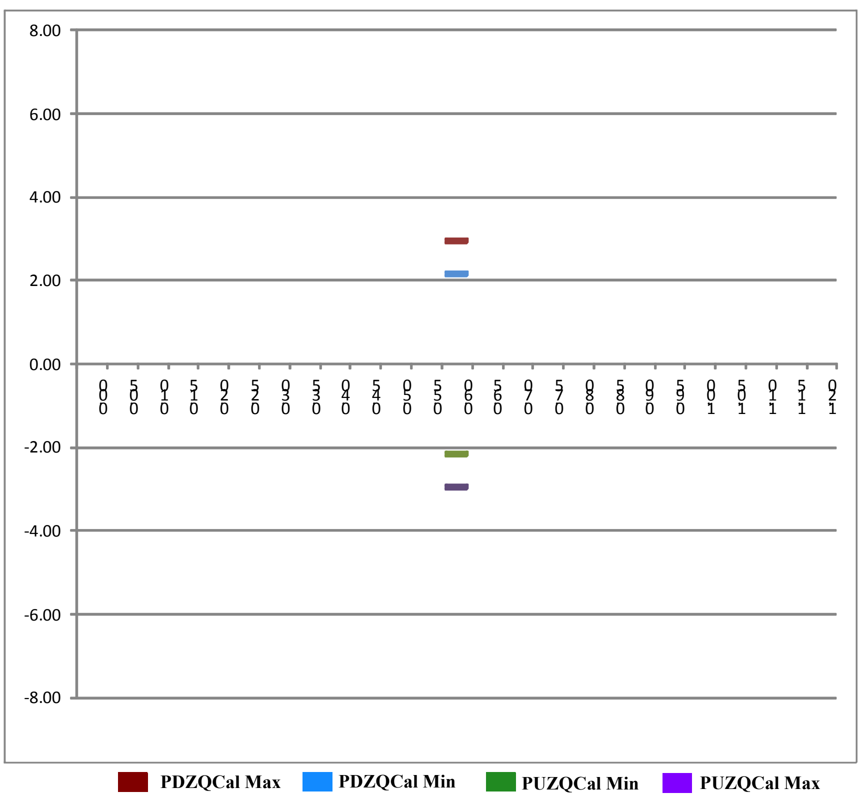


Figure 76 — I-V Curve After Calibration



8.7.5 ODT Levels and I-V Characteristics

On-Die Termination effective resistance, R_{TT}, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown in the figure below. R_{TT} is defined by the following formula:

$R_{TTPU} = (V_{DDQ} - V_{Out}) / | I_{Out} |$

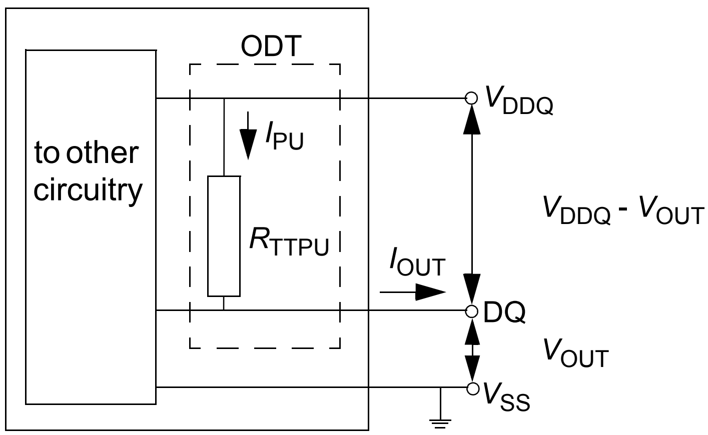


Table 54 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 ohm after proper ZQ calibration

R_{TT} (ohm)	V_{OUT} (V)	I_{OUT}	
		Min (mA)	Max (ma)
$R_{ZQ}/1$	0.6	-2.17	-2.94
$R_{ZQ}/2$	0.6	-4.34	-5.88

9 Input/Output Capacitance

9.1 Input/Output Capacitance

Table 55 — Input/output capacitance

Parameter	Symbol	Min/ Max	Value	Units	Notes
Input capacitance, CK_t and CK_c	C_{CK}	Min	0.7	pF	1,2
		Max	1.4	pF	1,2
Input capacitance delta, CK_t and CK_c	C_{DCK}	Min	0	pF	1,2,3
		Max	015	pF	1,2,3
Input capacitance, all other input-only pins	C_I	Min	0.7	pF	1,2,4
		Max	1.3	pF	1,2,4
Input capacitance delta, all other input-only pins	C_{DI}	Min	-0.20	pF	1,2,5
		Max	0.20	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	C_{IO}	Min	1.0	pF	1,2,6,7
		Max	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	Min	0	pF	1,2,7,8
		Max	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	C_{DIO}	Min	-0.25	pF	1,2,7,9
		Max	0.25	pF	1,2,7,9
Input/output capacitance ZQ Pin	C_{ZQ}	Min	0	pF	1,2
		Max	2.0	pF	1,2

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

NOTE 1 This parameter applies to die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, V_{SSQ} applied and all other pins floating.

NOTE 3 Absolute value of C_{CK_t} - C_{CK_c}.

NOTE 4 C_I applies to CS_n, CKE, CA0-CA9, ODT.

NOTE 5 $C_{DI} = C_I - 0.5 * (C_{CK\_t} + C_{CK\_c})$

NOTE 6 DM loading matches DQ and DQS.

NOTE 7 MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)

NOTE 8 Absolute value of C_{DQS_t} and C_{DQS_c}.

NOTE 9 $C_{DIO} = C_{IO} - 0.5 * (C_{DQS\_t} + C_{DQS\_c})$ in byte-lane.

10 I_{DD} Specification Parameters and Test Conditions

10.1 I_{DD} Measurement Conditions

The following definitions are used within the I_{DD} measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL(DC)}$ MAX

HIGH: $V_{IN} \geq V_{IH(DC)}$ MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See tables 56 and 57.

Table 56 — Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 CS_n must always be driven HIGH.

NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

NOTE 3 The above pattern (N, N+1, N+2, N+3...) is used continuously during I_{DD} measurement for I_{DD} values that require SWITCHING on the CA bus.

Table 57 — Definition of Switching for I_{DD4R}

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLH	HLHLLHL	L
Rising	H	L	N + 4	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N + 4	Read_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLH	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2 The above pattern (N, N+1...) is used continuously during I_{DD} measurement for I_{DD4R}.

Table 58 — Definition of Switching for I_{DD4W}

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLL	HLHLLHL	L
Rising	H	L	N + 4	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N + 4	Write_Falling	LHH	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLL	LHLHLHL	L

NOTE 1 Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
NOTE 2 Data masking (DM) must always be driven LOW.
NOTE 3 The above pattern (N, N+1...) is used continuously during I_{DD} measurement for I_{DD4W}.

10.2 I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of I_{DD6ET} which is for the entire extended temperature range.

Table 59 — I_{DD} Specification Parameters and Operating Conditions

Notes 1, 2, 3 apply for all values.

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	I_{DD0in}	V_{DDCA}, V_{DDQ}	3
Idle power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	3
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	3
Idle non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	3
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	3
Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	3

Table 59 — I_{DD} Specification Parameters and Operating Conditions (cont'd)

Notes 1, 2, 3 apply for all values.

Parameter/Condition	Symbol	Power Supply	Notes
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3PS1}	V_{DD1}	
	$I_{DD3PS}S_2$	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	4
Operating burst READ current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	4
All-bank REFRESH burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	4

Table 59 — I_{DD} Specification Parameters and Operating Conditions (cont'd)

Notes 1, 2, 3 apply for all values.

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	4
Per-bank REFRESH average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	4
Self refresh current (–25°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate ODT disabled	I_{DD61}	V_{DD1}	6, 7, 9
	I_{DD62}	V_{DD2}	6, 7, 9
	I_{DD6IN}	V_{DDCA}, V_{DDQ}	4, 6, 7, 9
Self refresh current (+85°C to +105°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD6ET1}	V_{DD1}	7, 8, 9
	I_{DD6ET2}	V_{DD2}	7, 8, 9
	$I_{DD6ET,in}$	V_{DDCA}, V_{DDQ}	4, 7, 8, 9
Deep power-down current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD81}	V_{DD1}	
	I_{DD82}	V_{DD2}	
	I_{DD8IN}	V_{DDCA}, V_{DDQ}	4

NOTE 1 Published I_{DD} values are the maximum of the distribution of the arithmetic mean.

NOTE 2 ODT disabled: MR11[2:0] = 000B.

NOTE 3 I_{DD} current specifications are tested after the device is properly initialized.

NOTE 4 Measured currents are the summation of V_{DDQ} and V_{DDCA}.

NOTE 5 Guaranteed by design with output load = 5 pF and R_{ON} = 40 ohm.

NOTE 6 The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.

NOTE 7 This is the general definition that applies to full-array SELF REFRESH.

NOTE 8 I_{DD6ET} is a typical value, is sampled only, and is not tested.

NOTE 9 Supplier datasheets may contain additional Self-Refresh I_{DD} values for temperature subranges within the standard or elevated temperature ranges.

NOTE 10 For all I_{DD} measurements, $V_{IHCKE} = 0.8 \times V_{DDCA}$, $V_{ILCKE} = 0.2 \times V_{DDCA}$.

Table 60 — I_{DD6} Partial Array Self-Refresh Current

Parameter		Value	Unit
I_{DD6} Partial Array Self-Refresh Current	Full Array	-	μA
	1/2 Array	-	μA
	1/4 Array	-	μA
	1/8 Array	-	μA

NOTE 1 I_{DD6} currents are measured using bank-masking only.

NOTE 2 I_{DD} values published are the maximum of the distribution of the arithmetic mean.

11 Electrical Characteristics and AC Timing

11.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

11.1.1 Definition for $t_{CK(avg)}$ and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$
$$where \qquad N = 200$$

Unit '$t_{CK(avg)}$' represents the actual clock average $t_{CK(avg)}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
$t_{CK(avg)}$ may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

11.1.2 Definition for $t_{CK(abs)}$

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
$t_{CK(abs)}$ is not subject to production test.

11.1.3 Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

11.1.4 Definition for t_{JIT}(per)

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.

$t_{JIT(per)}$ = Min/max of $\{t_{CKi} - t_{CK}(avg)$ where $i = 1$ to $200\}$.
$t_{JIT(per),act}$ is the actual clock jitter for a given system.
$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

11.1.5 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT(cc)}$ = Max of $|\{t_{CKi+1} - t_{CKi}\}|$.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

11.1.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.

$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.
$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.
$t_{ERR(nper)}$ is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$t_{ERR(nper),min}$ can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$t_{ERR(nper),max}$ can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

11.1.7 Definition for duty cycle jitter $t_{JIT(duty)}$

$t_{JIT(duty)}$ is defined with absolute and average specification of t_{CH} / t_{CL}.

$$y), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK$$

$$), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tC$$

11.1.8 Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 61 — Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg),min} + t_{JIT(per),min}$	ps
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	$t_{CH(avg),min} + t_{JIT(duty),min} / t_{CK(avg)min}$	$t_{CK(avg)}$
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	$t_{CL(avg),min} + t_{JIT(duty),min} / t_{CK(avg)min}$	$t_{CK(avg)}$

NOTE 1 $t_{CK(avg),min}$ is expressed is ps for this table.

NOTE 2 $t_{JIT(duty),min}$ is a negative value.

11.2 Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter ($t_{JIT(per)}$) in excess of the values found in Table 63 on page 112 and how to determine cycle time de-rating and clock cycle de-rating.

11.2.1 Clock period jitter effects on core timing parameters (t_{RCD}, t_{RP}, t_{RTP}, t_{WR}, t_{WRA}, t_{WTR}, t_{RC}, t_{RAS}, t_{RRD}, t_{FAW})

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support $t_{nPARAM} = RU\{t_{PARAM} / t_{CK}(avg)\}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or t_{CK}(avg) may need to be increased based on the values for each core timing parameter.

11.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (t_{nPARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR}(t_{nPARAM})$,act) in excess of the allowed cumulative period error ($t_{ERR}(t_{nPARAM})$,allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

11.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (t_{nPARAM}) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter ($t_{JIT(per)}$).

For a given number of clocks (t_{nPARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR}(t_{nPARAM),act}$) in excess of the allowed cumulative period error ($t_{ERR}(t_{nPARAM),allowed}$), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

11.2.2 Clock jitter effects on Command/Address timing parameters (t_{ISCA}, t_{IHCA}, t_{ISCS}, t_{IHCS},t_{ISCKE}, t_{IHCKE}, t_{ISb}, t_{IHb}, t_{ISCKEb}, t_{IHCKEb})

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.3 Clock jitter effects on Read timing parameters

11.2.3.1 t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} needs to be de-rated by the actual period jitter ($t_{JIT(per),act,max}$) of the input clock in excess of the allowed period jitter ($t_{JIT(per),allowed,max}$). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR3-1600 device has $t_{CK(avg)}$ = 1250 ps, $t_{JIT(per),act,min}$ = -92 ps and $t_{JIT(per),act,max}$ = + 134 ps, then

$t_{RPRE,min,derated} = 0.9 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max})/t_{CK(avg)} = 0.9 - (134 - 100)/1250 = .8728\ t_{CK(avg)}$

11.2.3.2 $t_{LZ(DQ)}$, $t_{HZ(DQ)}$, t_{DQSCK}, $t_{LZ(DQS)}$, $t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$.

11.2.3.3 t_{QSH}, t_{QSL}

These parameters are affected by duty cycle jitter which is represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$. These parameters determine absolute Data-Valid Window (DVW) at the LPDDR3 device pin.

Absolute min DVW @ LPDDR3 device pin =

$\min\{ (t_{QH(abs)min} - t_{DQSQmax}) , (t_{QSL(abs)min} - t_{DQSQmax}) \}$

This minimum DVW shall be met at the target frequency regardless of clock jitter.

11.2.3.4 t_{RPST}

t_{RPST} is affected by duty cycle jitter which is represented by $t_{CL(abs)}$. Therefore $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$.

$t_{RPST(abs)min} = t_{CL(abs)min} - 0.05 = t_{QSL(abs)min}$

11.2.4 Clock jitter effects on Write timing parameters

11.2.4.1 t_{DS}, t_{DH}

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.2 t_{DSS}, t_{DSH}

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.3 t_{DQSS}

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter $t_{JIT(per),act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per),allowed}$.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR3-1600 device has $t_{CK(avg)}$= 1250 ps, $t_{JIT(per),act,min}$= -93 ps and $t_{JIT(per),act,max}$= + 134 ps, then

$t_{DQSS,(min,derated)} = 0.75 - (t_{JIT(per),act,min} - t_{JIT(per),allowed,min})/t_{CK(avg)} = 0.75 - (-93 + 100)/1250 = 0.7444\ t_{CK(avg)}$

and

$t_{DQSS,(max,derated)} = 1.25 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max})/t_{CK(avg)} = 1.25 - (134 - 100)/1250 = 1.2228\ t_{CK(avg)}$

11.3 LPDDR3 Refresh Requirements by Device Density

Table 62 — LPDDR3 Refresh Requirement Parameters (per density)

Parameter		Symbol	4 Gb	8 Gb	16 Gb	32 Gb	Unit
Number of Banks			8			TBD	-
Refresh Window Tcase ≤ 85°C		t_{REFW}	32			TBD	ms
Refresh Window 1/2-Rate Refresh		t_{REFW}	16			TBD	ms
Refresh Window 1/4-Rate Refresh		t_{REFW}	8			TBD	ms
Required number of REFRESH commands (min)		R	8,192			TBD	-
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	3.9			TBD	us
	REFpb	t_{REFIpb}	0.4875	0.4875	0.4875	TBD	us
Refresh Cycle time		t_{RFCab}	130	210	TBD	TBD	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	90	TBD	TBD	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	6.72	TBD	TBD	us

11.4 LPDDR3 Read and Write Latencies

Parameter	Value							Unit
Max. Clock Frequency	166	400	533	600	667	733	800	MHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	MT/s
Average Clock Period	6	2.5	1.875	1.67	1.5	1.36	1.25	ns
Read Latency	3[1]	6	8	9	10	11	12	t_{CK}(avg)
Write Latency (Set A)	1[1]	3	4	5	6	6	6	t_{CK}(avg)
Write Latency (Set B)[2]	1[1]	3	4	5	8	9	9	t_{CK}(avg)

NOTE 1 RL=3/WL=1setting is an optional feature. Refer to MR0 OP<7>.

NOTE 2 Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>.

11.5 AC Timing

Table 63 — AC Timing

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/ Max	Data Rate 1333	Data Rate 1600	Unit
Maximum clock frequency		–	667	800	MHz
Clock Timing					
Average clock period	$t_{CK(avg)}$	MIN	1.5	1.25	ns
		MAX	100		
Average HIGH pulse width	$t_{CH(avg)}$	MIN	0.45		$t_{CK(avg)}$
		MAX	0.55		
Average LOW pulse width	$t_{CL(avg)}$	MIN	0.45		$t_{CK(avg)}$
		MAX	0.55		
Absolute clock period	$t_{CK(abs)}$	MIN	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN		ns
Absolute clock HIGH pulse width	$t_{CH(abs)}$	MIN	0.43		$t_{CK(avg)}$
		MAX	0.57		
Absolute clock LOW pulse width	$t_{CL(abs)}$	MIN	0.43		$t_{CK(avg)}$
		MAX	0.57		
Clock period jitter (with supported jitter)	$t_{JIT(per)}$, allowed	MIN	-80	-70	ps
		MAX	80	70	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT(cc)}$, allowed	MAX	160	140	ps
Duty cycle jitter (with supported jitter)	$t_{JIT(duty)}$, allowed	MIN	$min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$		ps
		MAX	$max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$		
Cumulative errors across 2 cycles	$t_{ERR(2per)}$, allowed	MIN	-118	-103	ps
		MAX	118	103	
Cumulative errors across 3 cycles	$t_{ERR(3per)}$, allowed	MIN	-140	-122	ps
		MAX	140	122	
Cumulative errors across 4 cycles	$t_{ERR(4per)}$, allowed	MIN	-155	-136	ps
		MAX	155	136	
Cumulative errors across 5 cycles	$t_{ERR(5per)}$, allowed	MIN	-168	-147	ps
		MAX	168	147	
Cumulative errors across 6 cycles	$t_{ERR(6per)}$, allowed	MIN	-177	-155	ps
		MAX	177	155	
Cumulative errors across 7 cycles	$t_{ERR(7per)}$, allowed	MIN	-186	-163	ps
		MAX	186	163	

Table 63 — AC Timing (cont'd)

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/Max	Data Rate 1333	Data Rate 1600	Unit
Cumulative errors across 8 cycles	$t_{ERR(8per), allowed}$	MIN	-193	-169	ps
		MAX	193	169	
Cumulative errors across 9 cycles	$t_{ERR(9per), allowed}$	MIN	-200	-175	ps
		MAX	200	175	
Cumulative errors across 10 cycles	$t_{ERR(10per), allowed}$	MIN	-205	-180	ps
		MAX	205	180	
Cumulative errors across 11 cycles	$t_{ERR(11per), allowed}$	MIN	-210	-184	ps
		MAX	210	184	
Cumulative errors across 12 cycles	$t_{ERR(12per), allowed}$	MIN	-215	-188	ps
		MAX	215	188	
Cumulative errors across *n* = 13, 14, 15…, 19, 20 cycles	$t_{ERR(nper), allowed}$	MIN	$t_{ERR(nper),allowed}$ MIN = (1 + 0.68ln(n)) × $t_{JIT(per), allowed}$ MIN		ps
		MAX	$t_{ERR (nper), allowed}$ MAX = (1 + 0.68ln(n)) × $tJ_{IT(per), allowed}$ MAX		
ZQ Calibration Parameters					
Initialization calibration time	t_{ZQINIT}	MIN	1		µs
Long calibration time	t_{ZQCL}	MIN	360		ns
Short calibration time	t_{ZQCS}	MIN	90		ns
Calibration RESET time	$t_{ZQRESET}$	MIN	max(50ns,3*n*CK)		ns
READ Parameters[4]					
DQS output access time from CK_t/CK_c	t_{DQSCK}	MIN	2500		ps
		MAX	5500		
DQSCK delta short[5]	$t_{DQSCKDS}$	MAX	265	220	ps
DQSCK delta medium[6]	$t_{DQSCKDM}$	MAX	593	511	ps
DQSCK delta long[7]	$t_{DQSCKDL}$	MAX	733	614	ps
DQS-DQ skew	t_{DQSQ}	MAX	165	135	ps
DQS output HIGH pulse width	t_{QSH}	MIN	$t_{CH(abs)}$ - 0.05		$t_{CK(avg)}$
DQS output HIGH pulse width	t_{QSL}	MIN	$t_{CL(abs)}$ - 0.05		$t_{CK(avg)}$
DQ/DQS output hold time from DQS	t_{QH}	MIN	min(t_{QSH}, t_{QSL})		ps
READ preamble[8, 11]	t_{RPRE}	MIN	0.9		$t_{CK(avg)}$
READ postamble[8, 12]	t_{RPST}	MIN	0.3		$t_{CK(avg)}$
DQS Low-Z from clock[8]	$t_{LZ(DQS)}$	MIN	$t_{DQSCK (MIN)}$ - 300		ps
DQ Low-Z from clock[8]	$t_{LZ(DQ)}$	MIN	$t_{DQSCK,(MIN)}$ - 300		ps
DQS High-Z from clock[8]	$t_{HZ(DQS)}$	MAX	$t_{DQSCK,(MAX)}$ - 100		ps

Table 63 — AC Timing (cont'd)

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1333	1600	
DQ High-Z from clock[8]	$t_{HZ(DQ)}$	MAX	$t_{DQSCK,(MAX)} + (1.4 \times t_{DQSQ,(MAX)})$		ps
WRITE Parameters[4]					
DQ and DM input hold time (V_{REF} based)	t_{DH}	MIN	175	150	ps
DQ and DM input setup time (V_{REF} based)	t_{DS}	MIN	175	150	ps
DQ and DM input pulse width	t_{DIPW}	MIN	0.35		$t_{CK(avg)}$
Write command to 1st DQS latching transition	t_{DQSS}	MIN	0.75		$t_{CK(avg)}$
		MAX	1.25		
DQS input high-level width	t_{DQSH}	MIN	0.4		$t_{CK(avg)}$
DQS input low-level width	t_{DQSL}	MIN	0.4		$t_{CK(avg)}$
DQS falling edge to CK setup time	t_{DSS}	MIN	0.2		$t_{CK(avg)}$
DQS falling edge hold time from CK	t_{DSH}	MIN	0.2		$t_{CK(avg)}$
Write postamble	t_{WPST}	MIN	0.4		$t_{CK(avg)}$
Write preamble	t_{WPRE}	MIN	0.8		$t_{CK(avg)}$
CKE Input Parameters					
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	MIN	max(7.5ns,3*n*CK)		ns
CKE input setup time	t_{ISCKE}[13]	MIN	0.25		$t_{CK(avg)}$
CKE input hold time	t_{IHCKE}[14]	MIN	0.25		$t_{CK(avg)}$
Command path disable delay	t_{CPDED}	MIN	2		$t_{CK(avg)}$
Command Address Input Parameters[4]					
Address and control input setup time	t_{ISCA}[15]	MIN	175	150	ps
Address and control input hold time	t_{IHCA}[15]	MIN	175	150	ps
CS_n input setup time	t_{ISCS}[15]	MIN	290	270	ps
CS_n input hold time	t_{IHCS}[15]	MIN	290	270	ps
Address and control input pulse width	t_{IPWCA}	MIN	0.35		$t_{CK(avg)}$
CS_n input pulse width	t_{IPWCS}	MIN	0.7		$t_{CK(avg)}$
Boot Parameters (10 MHz–55 MHz)[16, 17, 18]					
Clock cycle time	t_{CKb}	MAX	100		ns
		MIN	18		
CKE input setup time	t_{ISCKEb}	MIN	2.5		ns
CKE input hold time	t_{IHCKEb}	MIN	2.5		ns
Address and control input setup time	t_{ISb}	MIN	1150		ps

Table 63 — AC Timing (cont'd)

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/ Max	Data Rate 1333	Data Rate 1600	Unit
Address and control input hold time	t_{IHb}	MIN	1150		ps
DQS output data access time from CK_t/CK_c	t_{DQSCKb}	MIN	2.0		ns
		MAX	10.0		
Data strobe edge to output data edge	t_{DQSQb}	MAX	1.2		ns
Mode Register Parameters					
MODE REGISTER WRITE command period	t_{MRW}	MIN	10		$t_{CK(avg)}$
MODE REGISTER READ command period	t_{MRR}	MIN	4		$t_{CK(avg)}$
Core Parameters[19]					
READ latency	RL	MIN	10	12	$t_{CK(avg)}$
WRITE latency	WL	MIN	6	6	$t_{CK(avg)}$
ACTIVATE-to- ACTIVATE command period	t_{RC}	MIN	$t_{RAS} + t_{RPab}$ (with all-bank precharge) $t_{RAS} + t_{RPpb}$ (with per-bank precharge)		ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	t_{CKESR}	MIN	max(15ns,3*n*CK)		ns
SELF REFRESH exit to next valid command delay	t_{XSR}	MIN	max(t_{RFCab} + 10ns,2*n*CK)		ns
Exit power- down to next valid command delay	t_{XP}	MIN	max(7.5ns,3*n*CK)		ns
CAS-to-CAS delay	t_{CCD}	MIN	4		$t_{CK(avg)}$
Internal READ to PRECHARGE command delay	t_{RTP}	MIN	max(7.5ns,4*n*CK)		ns
RAS-to-CAS delay	t_{RCD} (fast)	MIN	max(15ns,3*n*CK)		ns
	t_{RCD} (typ)		max(18ns,3*n*CK)		
	t_{RCD} (slow)		max(24ns,3*n*CK)		
Row precharge time (single bank)	t_{RPpb} (fast)	MIN	max(15ns,3*n*CK)		ns
	t_{RPpb} (typ)		max(18ns,3*n*CK)		
	t_{RPpb} (slow)		max(24ns,3*n*CK)		
Row precharge time (all banks)	t_{RPpab} (fast)	MIN	max(18ns,3*n*CK)		ns
	t_{RPpab} (typ)		max(21ns,3*n*CK)		
	t_{RPpab} (slow)		max(27ns,3*n*CK)		
Row active time	t_{RAS}	MIN	max(42ns,3*n*CK)		ns
		MAX	70		µs
WRITE recovery time	t_{WR}	MIN	max(15ns,4*n*CK)		ns
Internal WRITE-to- READ command delay	t_{WTR}	MIN	max(7.5ns,4*n*CK)		ns

Table 63 — AC Timing (cont'd)

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/ Max	Data Rate 1333	Data Rate 1600	Unit
Active bank A to active bank B	t_{RRD}	MIN	max(10ns,2nCK)		ns
Four-bank ACTIVATE window	t_{FAW}	MIN	max(50ns,8nCK)		ns
Minimum deep power- down time	t_{DPD}	MIN	500		µs
ODT Parameters					
Asynchronous R_{TT} turn-on dely from ODT input	t_{ODTon}	MIN	1.75		ns
		MAX	3.5		
Asynchronous R_{TT} turn-off delay from ODT input	t_{ODToff}	MIN	1.75		ns
		MAX	3.5		
Automatic R_{TT} turn-on delay after READ data	t_{AODTon}	MAX	$t_{DQSCK} + 1.4 \times t_{DQSQ,max} + t_{CK(avg,min)}$		ps
Automatic R_{TT} turn-off delay after READ data	$t_{AODToff}$	MIN	$t_{DQSCK,min}$ - 300		ps
R_{TT} disable delay from power down, self-refresh, and deep power down entry	t_{ODTd}	MIN	12		ns
R_{TT} enable delay from power down and self refresh exit	t_{ODTe}	MAX	12		ns
CA Training Parameters					
First CA calibration command after CA calibration mode is programmed	t_{CAMRD}	MIN	20		$t_{CK(avg)}$
First CA calibration command after CKE is LOW	t_{CAENT}	MIN	10		$t_{CK(avg)}$
CA caibration exit command after CKE is HIGH	t_{CAEXT}	MIN	10		$t_{CK(avg)}$
CKE LOW after CA calibration mode is programmed	t_{CACKEL}	MIN	10		$t_{CK(avg)}$
CKE HIGH after the last CA calibration results are driven.	t_{CACKEH}	MIN	10		$t_{CK(avg)}$
Data out delay after CA training calibration command is programmed	t_{ADR}	MAX	20		ns
MRW CA exit command to DQ tri-state	t_{MRZ}	MIN	3		ns
CA calibration command to CA calibration command delay	t_{CACD}	MIN	RU(t_{ADR}+2 × t_{CK})		$t_{CK(avg)}$
Write Leveling Parameters					
DQS_t/DQS_c delay after write leveling mode is programmed	$t_{WLDQSEN}$	MIN	25		ns
		MAX	--		
First DQS_t/DQS_c edge after write leveling mode is programmed	t_{WLMRD}	MIN	40		ns
		MAX	--		

Table 63 — AC Timing (cont'd)

Notes 1–3 apply to all parameters. Notes begin below table on page 117.

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1333	1600	
Write leveling output delay	t_{WLO}	MIN	0		ns
		MAX	20		
Mode register set command delay	t_{MRD}	MIN	max(t_{MRW}, 15ns)		ns
		MAX	--		
Temperature Derating[18]					
DQS output access time from CK_t/CK_c (derated)	t_{DQSCK}	MAX	5620		ps
RAS-to-CAS delay (derated)	t_{RCD}	MIN	t_{RCD} + 1.875		ns
ACTIVATE-to- ACTIVATE command period (derated)	t_{RC}	MIN	t_{RC} + 1.875		ns
Row active time (derated)	t_{RAS}	MIN	t_{RAS} + 1.875		ns
Row precharge time (derated)	t_{RP}	MIN	t_{RP} + 1.875		ns
Active bank A to active bank B (derated)	t_{RRD}	MIN	t_{RRD} + 1.875		ns

NOTE 1 Frequency values are for reference only. Clock cycle time (t_{CK}) is used to determine device capabilities.

NOTE 2 All AC timings assume an input slew rate of 1 V/ns.

NOTE 3 Measured with 4 V/ns differential CK_t/CK_c slew rate and nominbal V_{IX}.

NOTE 4 READ, WRITE, and input setup and hold values are referenced to V_{REF}.

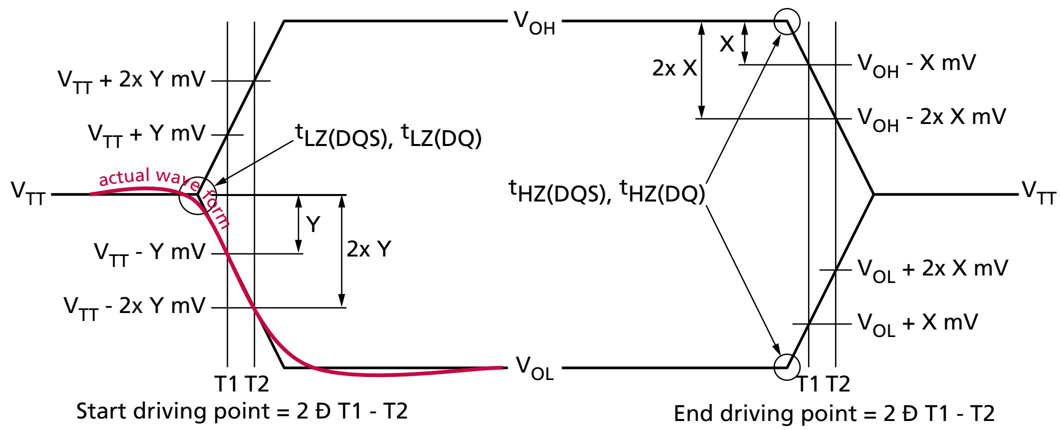
NOTE 5 $t_{DQSCKDS}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. $t_{DQSCKDS}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.

NOTE 6 $t_{DQSCKDM}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 1.6µs rolling window. $t_{DQSCKDM}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.

NOTE 7 $t_{DQSCKDL}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 32ms rolling window. $t_{DQSCKDL}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.

NOTE 8 For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). t_{HZ} and t_{LZ} transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for t_{RPST}, $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$), or begins driving (for t_{RPRE}, $t_{LZ(DQS)}$, $t_{LZ(DQ)}$). Figure 9 shows a method to calculate the point when device is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$ by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 9 Output Transition Timing



NOTE 10 The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as single-ended. The timing parameters t_{RPRE} and t_{RPST} are determined from the differential signal DQS/DQS#.
NOTE 11 Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
NOTE 12 Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
NOTE 13 CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
NOTE 14 CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
NOTE 15 Input set-up/hold time for signal (CA[9:0], CS_n).
NOTE 16 To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, t_{CK} during boot is t_{CKb}).
NOTE 17 The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
NOTE 18 The output skew parameters are measured with default output impedance settings using the reference load.
NOTE 19 The minimum t_{CK} column applies only when t_{CK} is greater than 6ns.

11.6 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet t_{IS}(base) and t_{IH}(base) value (see Table 64) to the Δt_{IS} and Δt_{IH} derating value (see Table 66) respectively. Example: t_{IS} (total setup time) = t_{IS}(base) + Δt_{IS}.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure Figure 77). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 79).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 78). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 80).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 67).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 66, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 64 — CA Setup and Hold Base-Values

unit [ps]	Data Rate		reference
	1333	1600	
$t_{ISCA(base)}$	100	75	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
$t_{IHCA(base)}$	125	100	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 ac/dc referenced for 2V/ns CA slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table 65 — CS_n Setup and Hold Base-Values

unit [ps]	Data Rate		reference
	1333	1600	
$t_{ISCS(base)}$	215	195	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
$t_{IHCS(base)}$	240	220	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 AC/DC referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t/CK_c slew rate.

11.6 CA and CS_n Setup, Hold and Derating (cont'd)

Table 66 — Derating values tIS/tIH - ac/dc based AC150

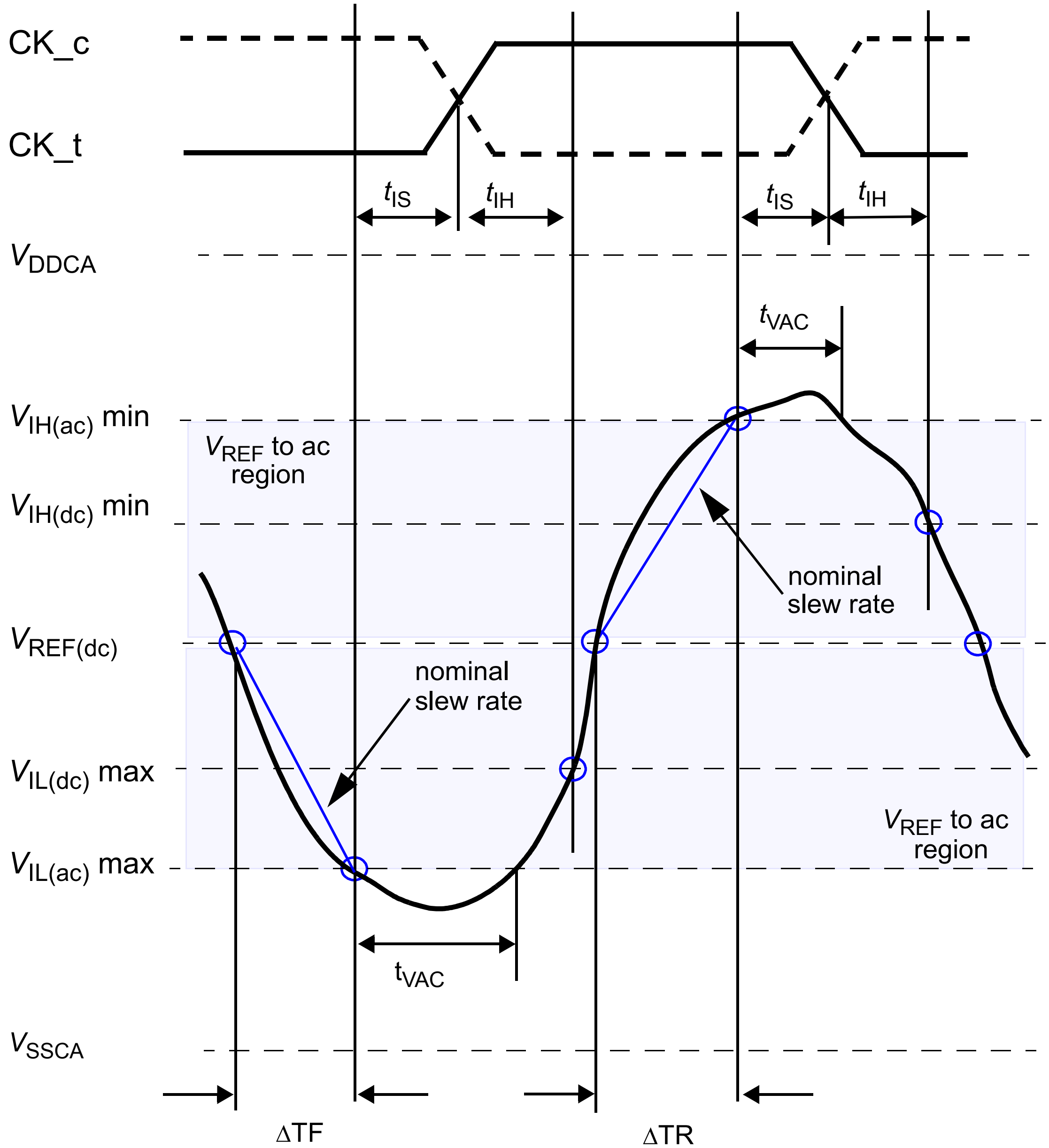
Δt_{ISCA}, Δt_{IHCA}, Δt_{ISCS}, Δt_{IHCS} derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+150mV$, $V_{IL(ac)}=V_{REF(dc)}-150mV$ DC100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+100mV$, $V_{IL(dc)}=V_{REF(dc)}-100mV$													
		CK_t, CK_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	30	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	1.5	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 67 — Required time t_{VAC} above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for CA

Slew Rate [V/ns]	t_{VAC} [ps] @ 150mV 1333Mbps		t_{VAC} [ps] @ 150mV 1600Mbps	
	min	max	min	max
> 4.0	58	-	48	-
4.0	58	-	48	-
3.5	56	-	46	-
3.0	53	-	43	-
2.5	50	-	40	-
2.0	45	-	35	-
1.5	37	-	27	-
< 1.5	37	-	27	-

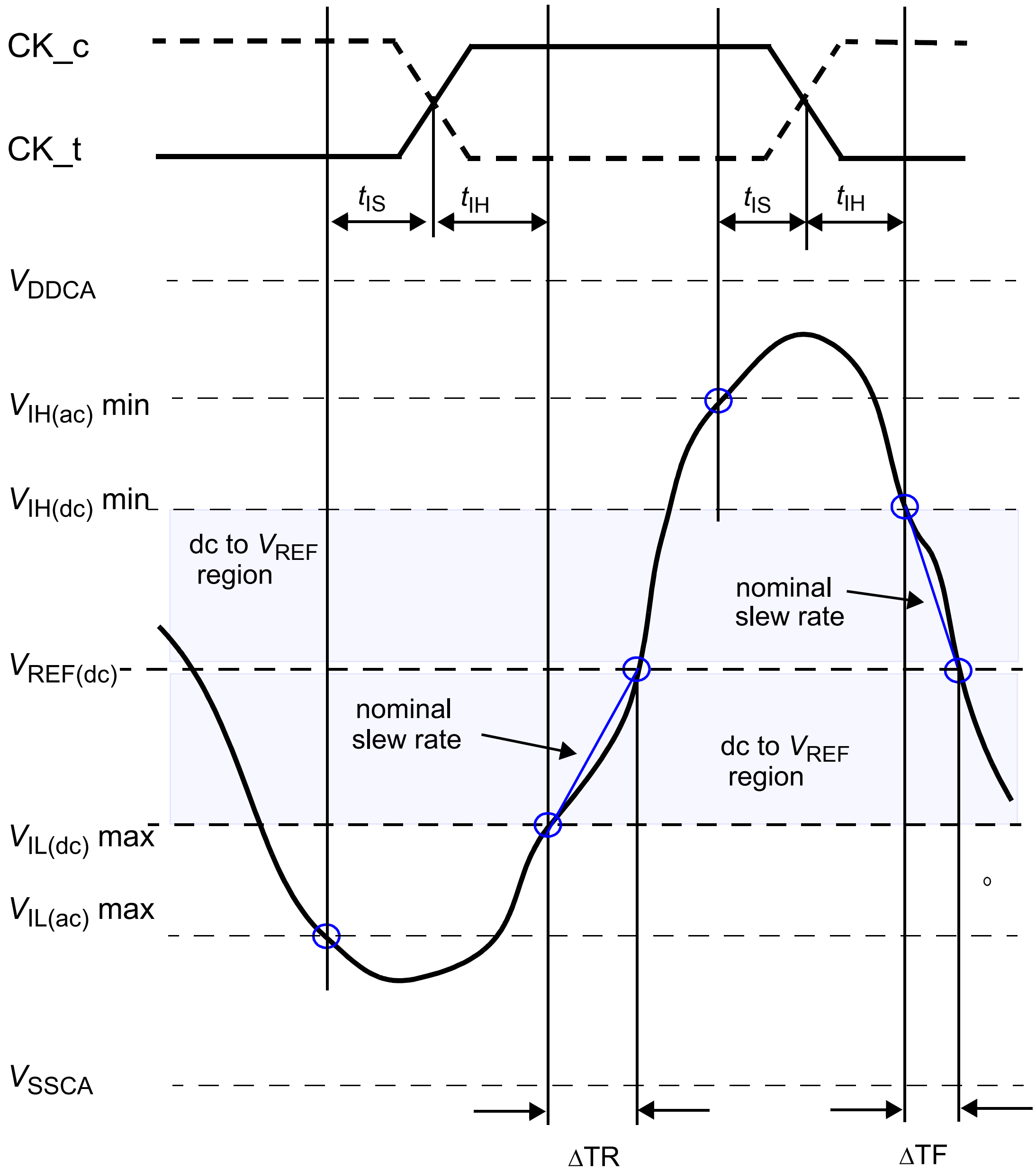
11.6CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 77 — Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock.

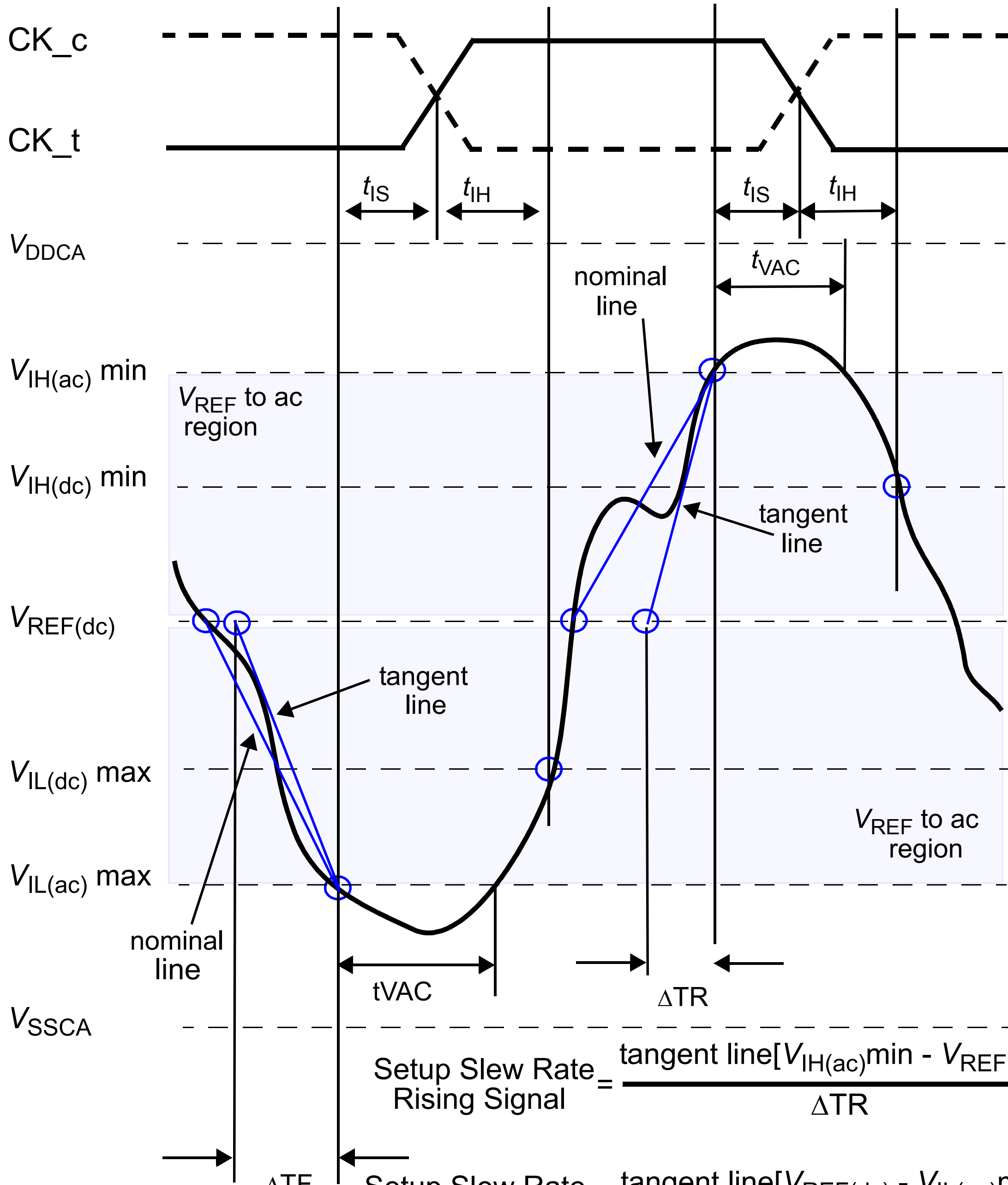
11.6 CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}\text{max}}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}\text{min} - V_{REF(dc)}}{\Delta TF}$$

Figure 78 — Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock

11.6 CA and CS_n Setup, Hold and Derating (cont'd)

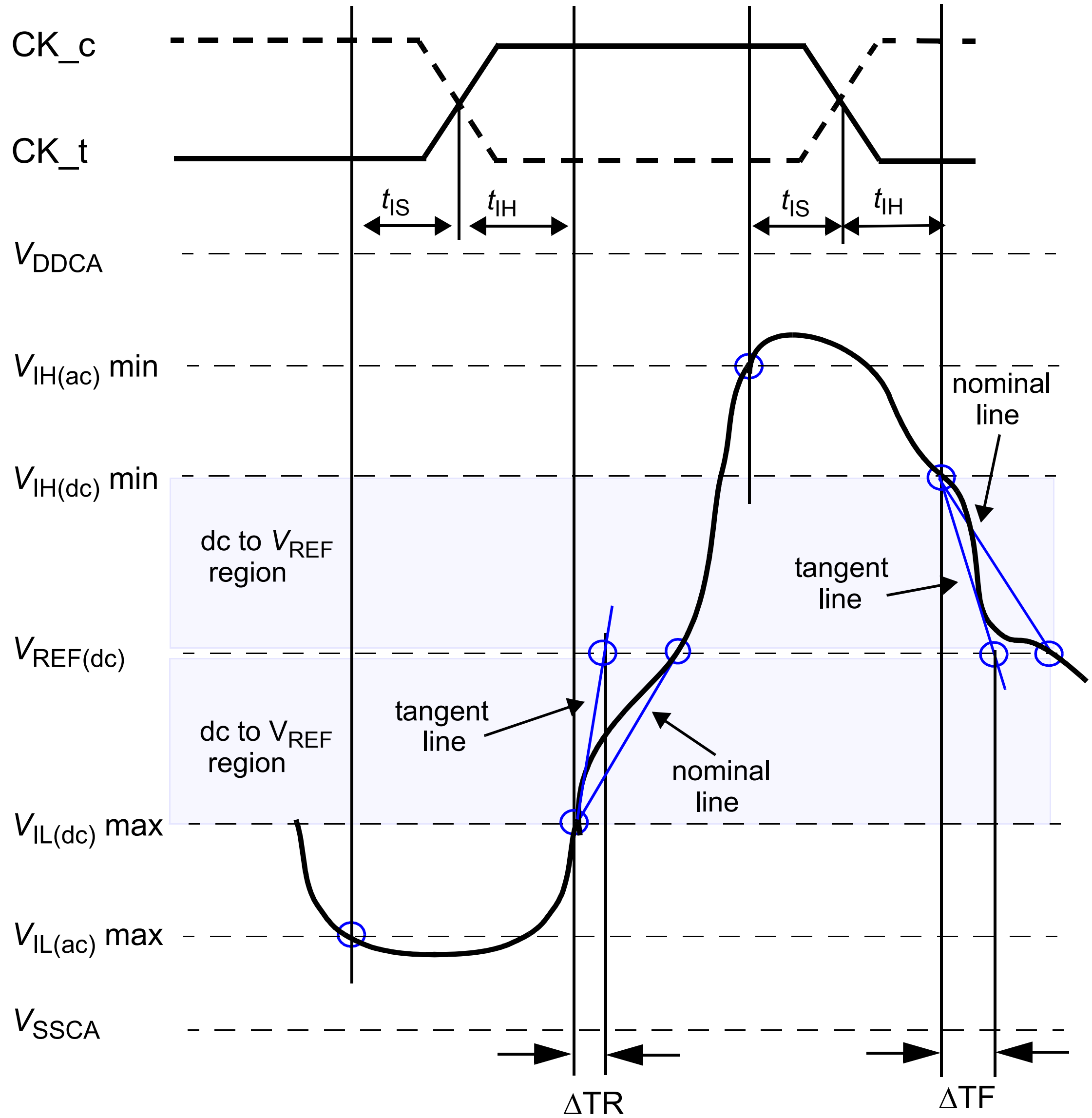


$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH(ac)}\text{min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(dc)} - V_{IL(ac)}\text{max}]}{\Delta TF}$$

Figure 79 — Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock

11.6 CA and CS_n Setup, Hold and Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(dc)} - V_{IL(dc)}\text{max} \,]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\, V_{IH(dc)}\text{min} - V_{REF(dc)} \,]}{\Delta TF}$$

Figure 80 — Illustration of tangent line for for hold time t_{IH} for CA and CS_n with respect to clock

11.7 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet t_{DS}(base) and t_{DH}(base) value (see Table 68) to the Δt_{DS} and Δt_{DH} (see Table 66) derating value respectively. Example: t_{DS} (total setup time) = t_{DS}(base) + Δt_{DS}.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 81). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 83).

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 82). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 84).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 37).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 68 — Data Setup and Hold Base-Values

[ps]	Data Rate		reference
	1333	1600	
$t_{DS(base)}$	100	75	$V_{IH/L(ac)} = V_{REF(dc)}$ +/- 150mV
$t_{DH(base)}$	125	100	$V_{IH/L(dc)} = V_{REF(dc)}$ +/- 100mV

NOTE 1 AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t/DQS_c slew rate and nominal V_{IX}.

11.7 Data Setup, Hold and Slew Rate Derating (cont'd)

Table 69 — Derating values LPDDR3 tDS/tDH - ac/dc based AC150

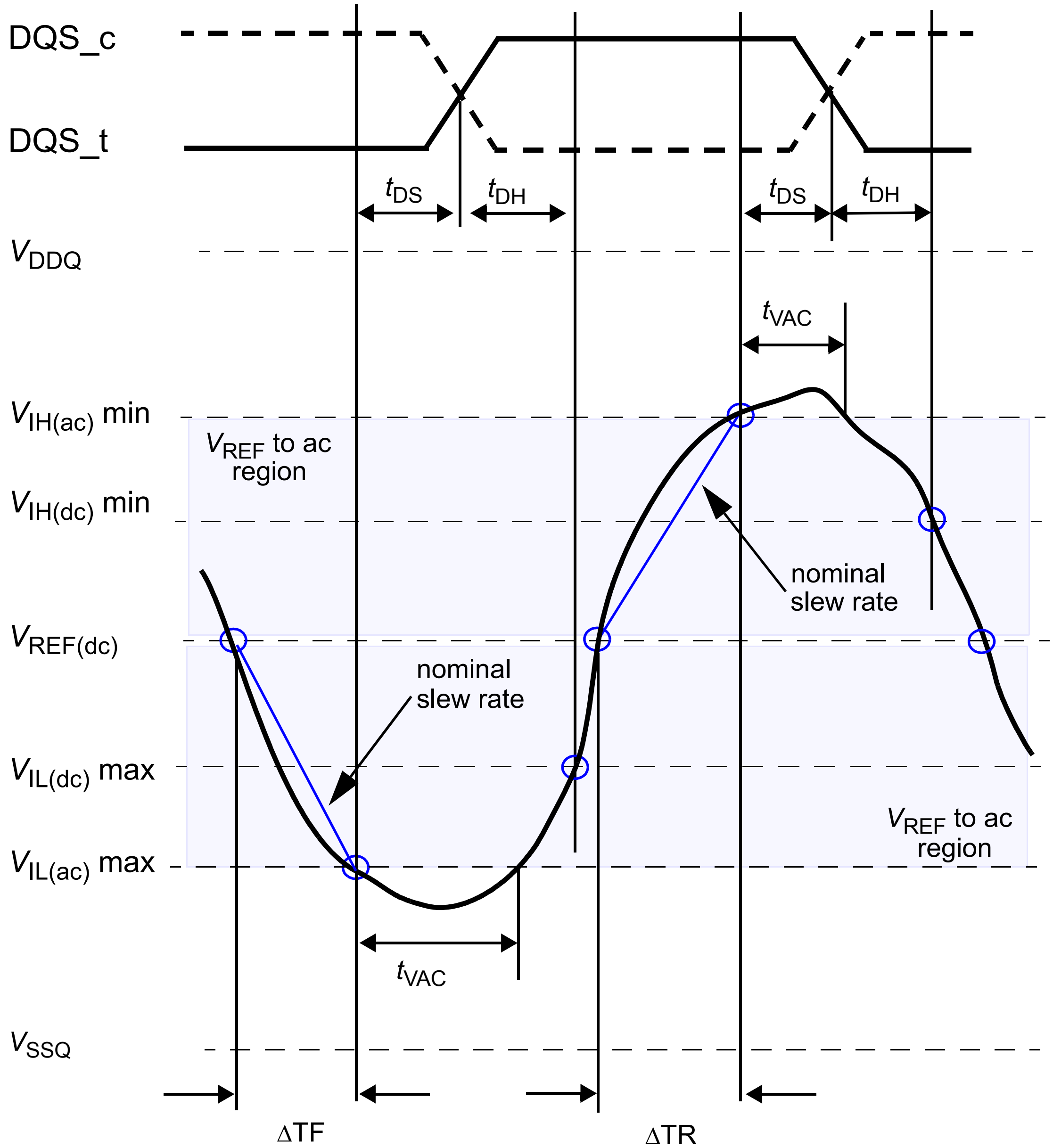
Δt_{DS}, Δt_{DH} derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+150mV$, $V_{IL(ac)}=V_{REF(dc)}-150mV$ DC100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+100mV$, $V_{IL(dc)}=V_{REF(dc)}-100mV$													
		DQS_t, DQS_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
DQ, DM Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25	-	-
	3.0	-	-	25	17	25	17	25	17	25	17	38	29
	2.0	-	-	-	-	0	0	0	0	0	0	13	13
	15	-	-	-	-	-	-	-25	-17	-25	-17	-12	-4

NOTE 1 Cell contents shaded in red are defined as 'not supported'.

Table 70 — Required time t_{VAC} above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for DQ, DM

Slew Rate [V/ns]	t_{VAC} [ps] @ 150mV 1333Mbps		t_{VAC} [ps] @ 150mV 1600Mbps	
	min	max	min	max
> 4.0	58	-	48	-
4.0	58	-	48	-
3.5	56	-	46	-
3.0	53	-	43	-
2.5	50	-	40	-
2.0	45	-	35	-
1.5	37	-	27	-
< 1.5	37	-	27	-

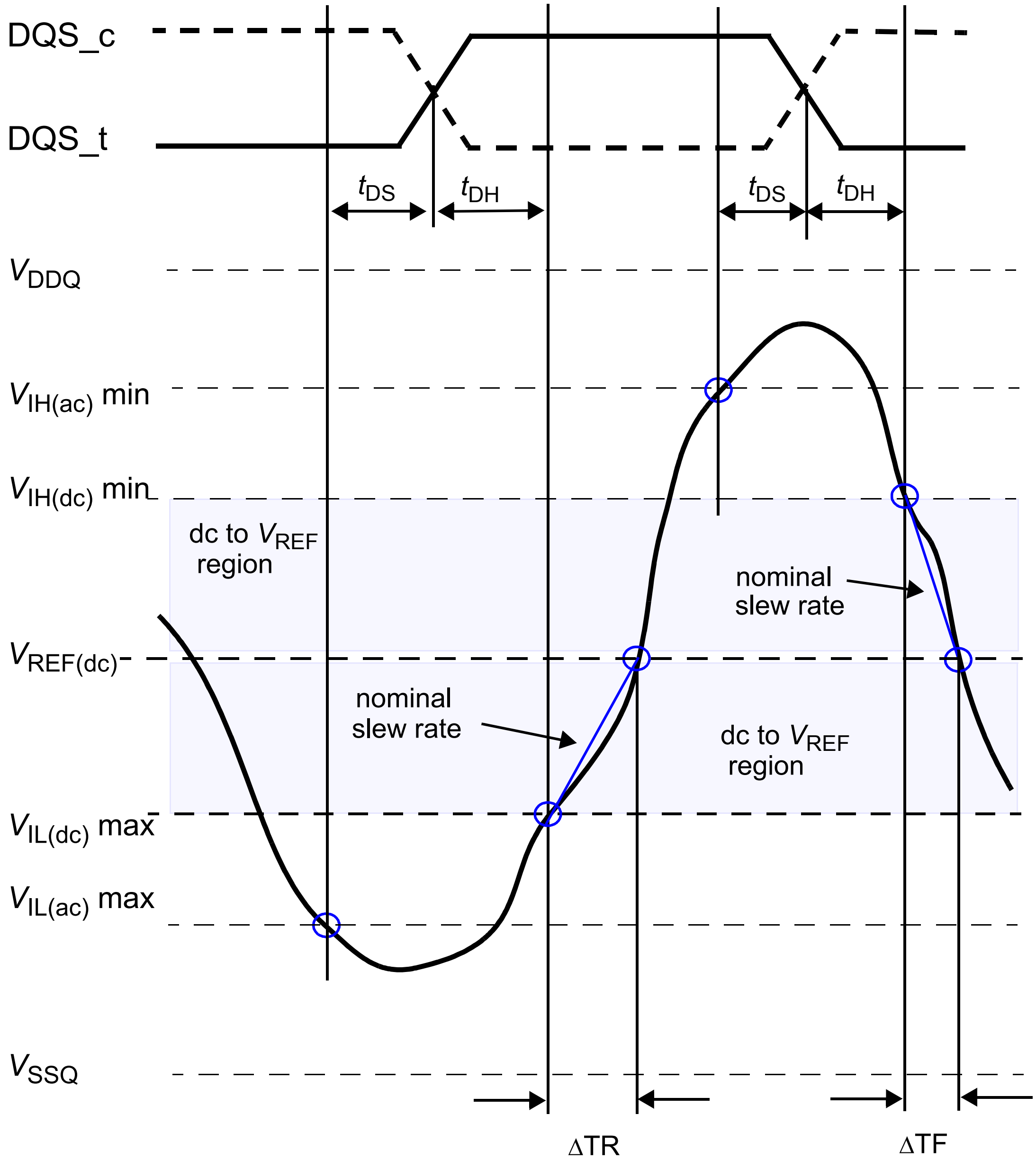
11.7 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 81 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe

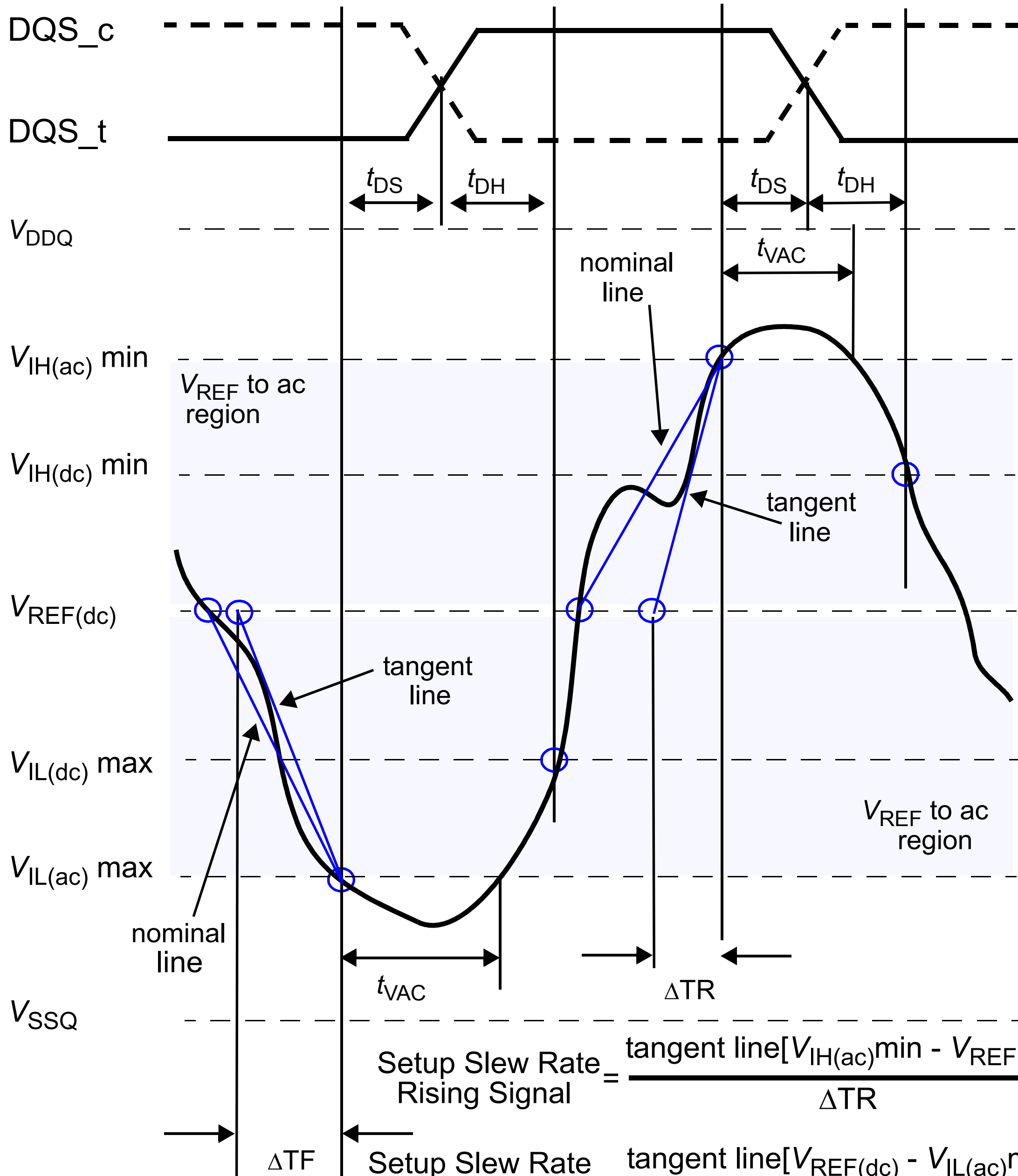
11.7 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 82 — Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

11.7 Data Setup, Hold and Slew Rate Derating (cont'd)

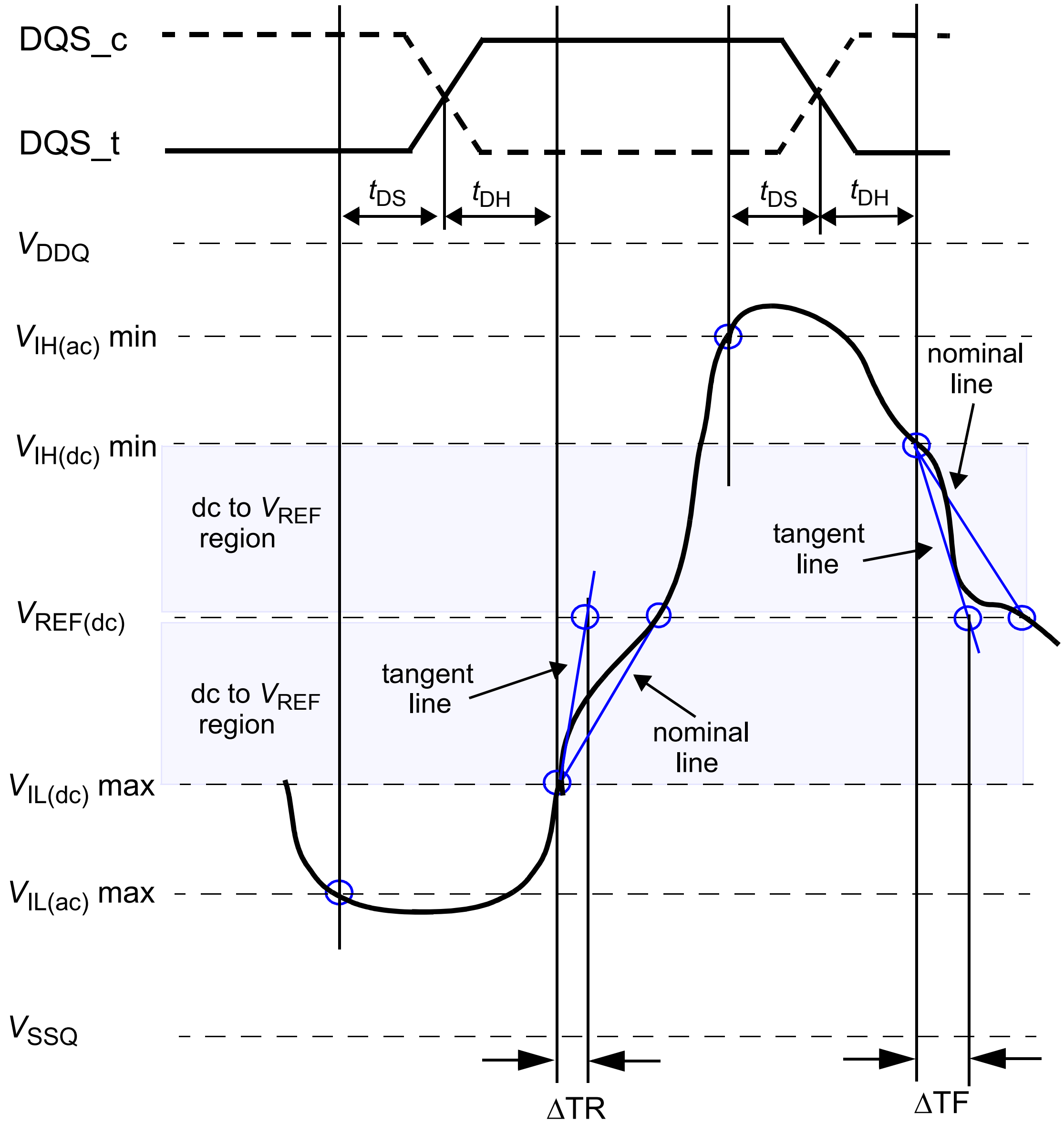


$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH(ac)}\text{min} - V_{REF(dc)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(dc)} - V_{IL(ac)}\text{max}]}{\Delta TF}$$

Figure 83 — Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

11.7 Data Setup, Hold and Slew Rate Derating (cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\,V_{REF(dc)} - V_{IL(dc)}\text{max}\,]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\,V_{IH(dc)}\text{min} - V_{REF(dc)}\,]}{\Delta TF}$$

Figure 84 — Illustration of tangent line for for hold time t_{DH} for DQ with respect to strobe

Annex A

Annex B (informative) Differences between Document Revisions

B.1 Initial Release JESD209-3

LPDDR3 Specification Released as JESD209-3.

B.2 Updated Specification to JESD209-3A

LPDDR3 Specification Updated as JESD209-3A.

Table 71 — Changes from JESD209-3 to JESD209-3A

Changes	Sections Effected	Description of Changes

3 UPDATE NOTES:

Update 3/12/12:

NOTE 1 Updated spec and ballot list with latest ballot pass/hold material Table 1 on page 6 and throughout document (see ballot table for links to updated material).
NOTE 2 VDDQ off during power-down -- ODT input buffer tied to VDDQ, if ODT is needed during power-down, per MR setting, then VDDQ off during PD cannot be allowed. Added clarification. "On-Die Termination" on page 60.
NOTE 3 Added 216-ball 12POP ball-out "216-ball 12mm x 12mm 0.4mm Pitch Dual-Channel POP FBGA (top view) Using Variation VCCCDB for MO-273" on page 2
NOTE 4 Added 256-ball 14POP ball-out "256-ball 14mm x 14mm 0.4mm Pitch Dual-Channel POP FBGA (top view) Using Variation VEECDB for MO-273" on page 3
NOTE 5 Added 346-ball MCP ball-out "346-ball 0.5mm Pitch Dual-Channel Multi-Chip Package (MCP) FBGA (top view) MO TBD" on page 6
NOTE 6 Added note to 178-ball discrete package ball-out "178-Ball Discrete Single-Channel FBGA (top view) MO TBD" on page 5
NOTE 7 Updated initialization section to include instance of CA Training occuring at time Tf "Voltage Ramp and Device Initialization" on page 12
NOTE 8 Corrected figure 9 per ballot comments Figure 9 on page 29
NOTE 9 Added MR255 RESET command ":255_(Reserved) (MA<7:0> = 40H-FFH):" on page 24 and "MRW RESET" on page 54
NOTE 10 Updated figures to remove red text per ballot comments: Figure 37 on page 50 and Figure 39 on page 53.
NOTE 11 tQHSb is no longer valid and should be removed from AC Timing table, Table 63 on page 112
NOTE 12 Need to fix figure color keys, Figure 76 on page 97
NOTE 13 Corrected segment mask row address encodings per ballot comments, "_PASR_Segment Mask (MA<7:0> = 011H):" on page 23.
NOTE 14 Added default condition to MR11 OP<2>=0 per ballot comments, "_ODT Control (MA<7:0> = 0BH:" on page 23
NOTE 15 Updated notes for single-ended and differential output slew rates per editorial comments and committee discussion "Single Ended Output Slew Rate" on page 90 and "Differential Output Slew Rate" on page 91.
NOTE 16 MR1 default value set to nWR=8 per ballot comments and committee discussion, "_Device Feature 1 (MA<7:0> = 01H):" on page 18.
NOTE 17 MR2 default value set to RL=10/WL=x per ballot comments committee discusion, "_Device Feature 2 (MA<7:0> = 02H):" on page 19.
NOTE 18 Note #10 added to IDD parameters table to define state of CKE levels during IDD measurements per ballot comments, "IDD Specifications" on page 102.
NOTE 19 tMRD specification value changed to max(tMRW, 15ns) per ballot comments Table 63 on page 112.
NOTE 20 Added cross-reference to figure 28 (nonsupported transition) in Refresh section per ballot comments.
NOTE 21 Added language to tFAW section to describe tFAW calculation during clock frequency change, "8-Bank Device Operation" on page 25.

Update 3/16/12

NOTE 1 moved t_{DVAC} tables from setup/hold de-rating section "CA and CS_n Setup, Hold and Derating" on page 119 and "Data Setup, Hold and Slew Rate Derating" on page 125 to differential input characteristics section "Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)" on page 84.
NOTE 2 Removed references to "preactive" command from clock stop and frequency change section, "Input clock stop and frequency change" on page 69.
NOTE 3 Changed MR1 nWR=3 to "optional" to align to MR0 RL3 option support. Changed MR1 default to nWR=10 to align to 1333MHz speed grade per committee decision on default settings. Also changed MR2 OP<4>=1 to default to match the nWR setting, "_Device Feature 1 (MA<7:0> = 01H):" on page 18 and "_Device Feature 2 (MA<7:0> = 02H):" on page 19.
NOTE 4 Changed tODTd and tODTe to 12ns to align with final pass/hold ballot as agreed by committe during San Diego, December 2011 committee meetings.
NOTE 5 Updated MRW RESET alternate encodings, "_Reset (MA<7:0> = 3FH): MRW only" on page 24 and "MRW RESET" on page 54.

Update 3/22/12

NOTE 1 Added tCPDED to AC Timings table.
NOTE 2 Updated POP MO definitions with MO variation designation.
NOTE 3 Updated ODT pin names in 253-ball package to match p/h ballot material. Added notes approved in committee and editorial to align to other package ball-outs in document.
NOTE 4 Added notes per ballot material to 178-ball package ball-out
NOTE 5 Updated ODT pin names in 346-ball package to match p/h ballot material. Added note as editorial to clarify NAND vs. e-MMC ball-out designations.

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1. I recommend changes to the following:
   - ☐ Requirement, clause number ________
   - ☐ Test method number ________ Clause number ________

   The referenced clause number has proven to be:
   - ☐ Unclear ☐ Too Rigid ☐ In Error
   - ☐ Other ____________________

2. Recommendations for correction:

   ____

   ____

   ____

   ____

3. Other suggestions for document improvement:

   ____

   ____

   ____

   ____

Submitted by

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