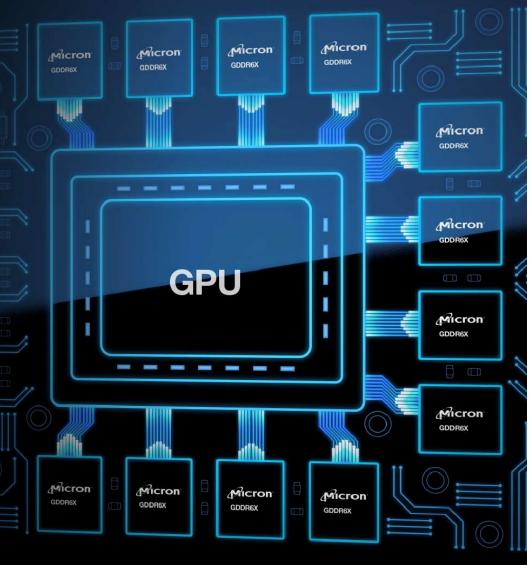
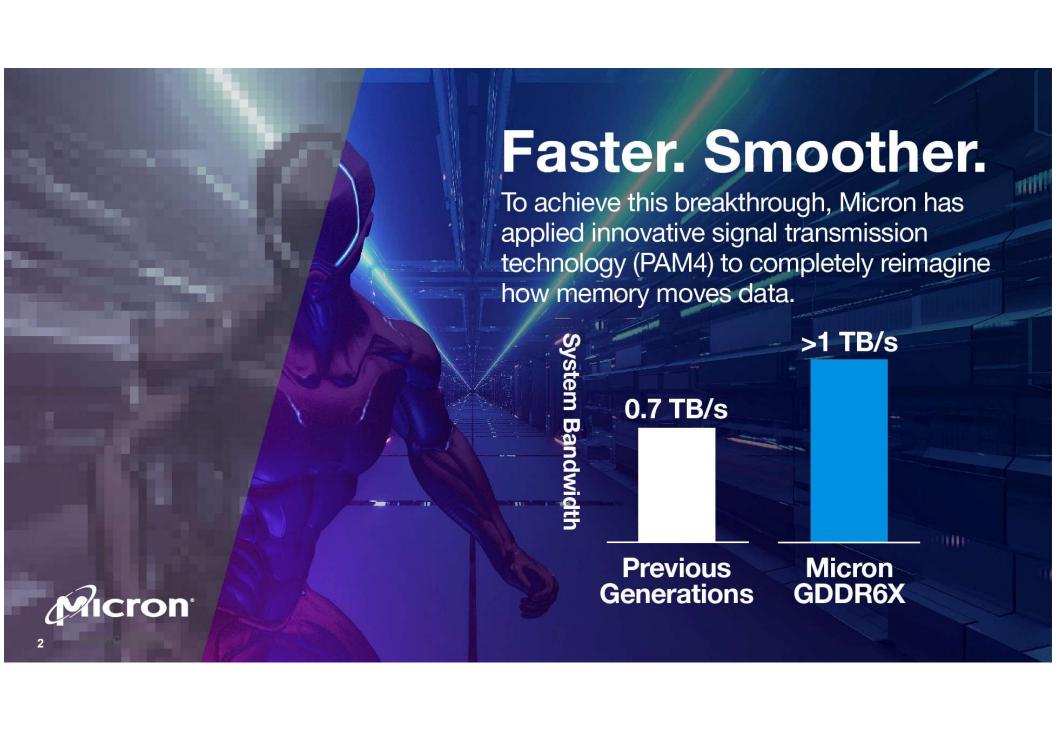


GDDR6X Memory Reimagined

Micron's GDDR6X memory uses innovative signaling technology to double the data rate, delivering unprecedented graphics memory performance to feed the most data-hungry workloads.

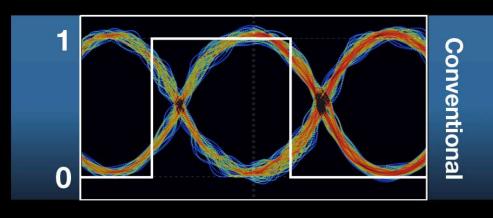


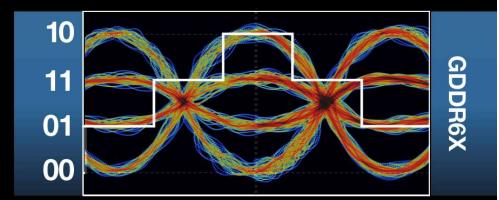




Doubling Data Down Every Wire

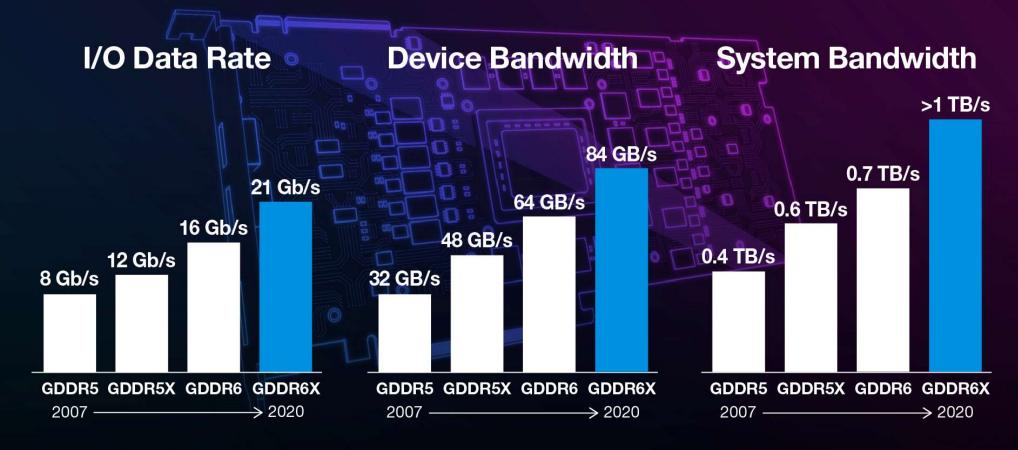
By using PAM4 multilevel signaling, Micron GDDR6X transfers more data and at a much faster rate, moving two bits of information at a time to double the I/O data rate.





Delivering Ultra-Bandwidth





High Performance DRAM Comparison

		O. J. IRDAN				- 111/ B 1 1 11/ 0 1 //			
	Standard DRAM				Ultra-Bandwidth Solutions				
Туре	DDR4	DDR5*	LPDDR4/X	LPDDR5*	GDDR5	GDDR6	GDDR6X	HBM2E	
Die Density	Up to 16Gb	Up to 64Gb	Up to 32Gb	Up to 32Gb	Up to 8Gb	Up to 32Gb	Up to 16Gb	16 Gb 4-H and 8-H	
Prefetch Size	8n	16n	16n	16n/32n	8n	16n	16n	4n	
Voltage (Vdd)	1.2V	1.1V	1.1V	1.05V	1.5V and 1.35V	1.35V and 1.25V	1.35V and 1.25V	1.2V	
I/O Voltage (Vddq)	Same as VDD	Same as VDD	1.1/0.6V	0.5V	Same as VDD	Same as VDD	Same as VDD	Same as VDD	
Max Data Rate	Up to 3.2Gbps	Up to 6.4Gbps	Up to 4.26Gbps	Up to 6.4Gbps (investigating > 6.4Gbs)	Up to 8.0 Gbps	Up to 16.0 Gbps (>16Gbps in planning)	21 Gbps (>21 Gbps in planning)	Up to 3.2Gbps	
Burst Length	BC4, 8	BC8,16	16, 32	16,32	8	16	8 in PAM4 mode 16 in RDQS mode	4	
Device Width (I/O)	x4, x8, x16	X4/x8/x16	2Ch x16	x8/x16	x32/x16	2ch x16/x8	2ch x16/x8	x1024	
Internal Banks	16 (x4/x8) 8 (x16)	32(x4/x8) 16(x16)	8/Ch	16	16	16	16	16 (4-H), 32 (8-H)	
Bank Groups	4 (x4/x8) 2 (x16)	8(x4/x8) 4(x16)	N/A	4	N/A	4	4	4 or 8	
Key Timing Parameters									
Data Rate	3.2Gbps	4.8Gbps	4.26Gbps	6.4Gbps	8.0Gbps	16.0Gbps	19 Gbps, 21 Gbps	3.2Gbps	
Read Latency (tAA)	~12.5 – 15ns	~15 – 18.33ns	~17	~22ns	~15 ns	~15 ns	~15ns	~25 ns	
Row Cycle Time (tRC)	45 - 47ns	47-50.3	60 - 63ns	60 to 63ns	40- 45ns	40- 45 ns	40-45ns	45ns	
Bank Address Delays (tRRD/tFAW)	2.5–6.4ns/ 10-30ns	1.67-5ns/ 13.3-16.7ns	10ns/ 40ns	5ns/ 20ns	4ns/ 16ns	2.5ns/ 10ns	2ns/ 8ns	2.5ns/ 10ns	
Bus Turn Delay (tWTR)	2.5 – 7.5ns	2.5 - 10ns	10ns	12ns	5ns	5ns	5ns	5.4ns	
Energy per bit (est.)	10pJ/bit	6pJ/bit	5pJ/bit	4pJ/bit	9pJ/bit	8.5pJ/bit	7.25pJ/bit	6pJ/bit	
Self refresh power (IDD6R)	24mW	TBD	< 1mW	< 1mW	20mW	40mW	NA	TBD	

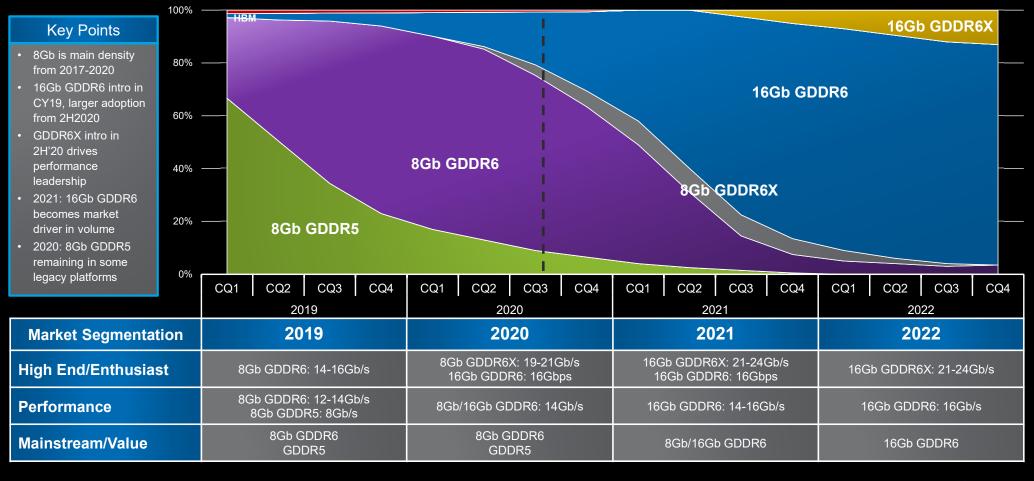
Micron Confidential

*DDR5 and LPDDR5 still in JEDEC definition. Subject to change

Minimum associated clock cycles may also appl

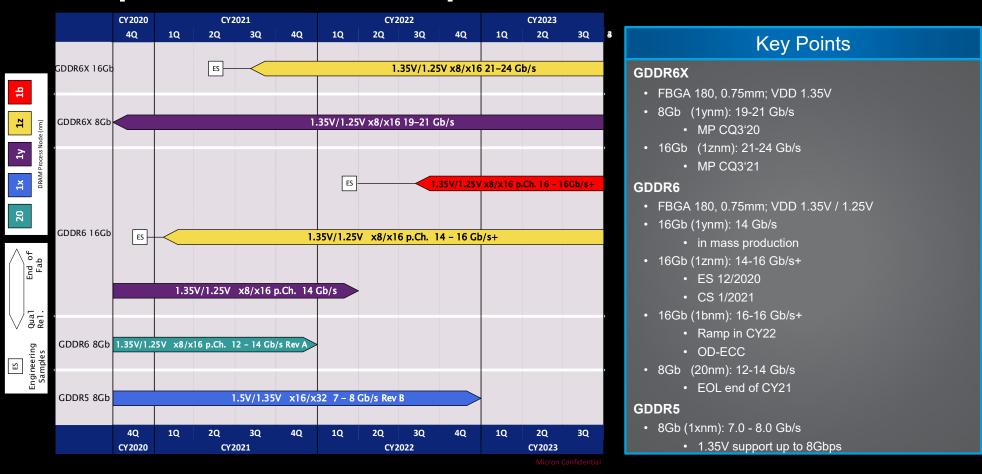


Graphic Card Market Transition (Volume 1Gb equivs)





Graphics DRAM Roadmap – Nov'20





Top Performance by a Memory Technology

