Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

SPI EEPROM
Palladium Memory Model
User Guide

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

SPI EEPROM Memory Model

1. Introduction

The Cadence Palladium SPI EEPROM Memory models are available with model sizes matching real SPI EEPROM devices manufactured by STMicroelectronics and Microchip. Different sizes are available; please consult the memory model catalog for the current available list.

Available SPI EEPROM memory models are listed in the table below.

Table 1: SPI EEPROM Memory Model List

Model Source File	Description
STMicroelectronics M95XXX Series	
st_eeprom_m95080.vhdp	ST M95160 / M95160-W / M95160-R / M95160-F SPI EEPROM Model
st_eeprom_m95160.vhdp	ST M95160 / M95160-W / M95160-R / M95160-F SPI EEPROM Model
st_eeprom_m95320.vhdp	ST M95320-W / M95320-R SPI EEPROM Model
st_eeprom_m95640.vhdp	ST M95640-W / M95640-R SPI EEPROM Model
st_eeprom_m95128.vhdp	ST M95128-W / M95128-R SPI EEPROM Model
st_eeprom_m95256.vhdp	ST M95256-W / M95256-R SPI EEPROM Model
st_eeprom_m95512.vhdp	ST M95512-W / M95512-R SPI EEPROM Model
st_eeprom_m95m01.vhdp	ST M95M01-R SPI EEPROM Model
STMicroelectronics M95XXX-D Series	
st_eeprom_m95320d.vhdp	ST M95320-DF SPI EEPROM Model
st_eeprom_m95640d.vhdp	ST M95640-DF SPI EEPROM Model
st_eeprom_m95128d.vhdp	ST M95128-DF SPI EEPROM Model
st_eeprom_m95256d.vhdp	ST M95256-DR / M95256-DF SPI EEPROM Model
st_eeprom_m95512d.vhdp	ST M95512-DR / M95512-DF SPI EEPROM Model
st_eeprom_m95m01d.vhdp	ST M95M01-DF SPI EEPROM Model
st_eeprom_m95m02d.vhdp	ST M95M02-DR SPI EEPROM Model
STMicroelectronics M95XXX-A Series	
st_eeprom_m95320a.vhdp	ST M95320-A125 / M95320-A145 SPI EEPROM Model
st_eeprom_m95640a.vhdp	ST M95640-A125 / M95640-A145 SPI EEPROM Model
st_eeprom_m95128a.vhdp	ST M95128-A125 / M95128-A145 SPI EEPROM Model
st_eeprom_m95256a.vhdp	ST M95256-A125 / M95256-A145 SPI EEPROM Model
st_eeprom_m95512a.vhdp	ST M95512-A125 / M95512-A145 SPI EEPROM Model
st_eeprom_m95m01a.vhdp	ST M95M01-A125 / M95M01-A145 SPI EEPROM Model
Microchip 25LCXXX Series	
mc_eeprom_25lc080c.vhdp	Microchip 25LC080C SPI EEPROM Model
mc_eeprom_25lc080d.vhdp	Microchip 25LC080D SPI EEPROM Model
mc_eeprom_25lc160c.vhdp	Microchip 25LC160C SPI EEPROM Model
mc_eeprom_25lc160d.vhdp	Microchip 25LC160D SPI EEPROM Model
mc_eeprom_25lc320a.vhdp	Microchip 25LC320A SPI EEPROM Model

mc_eeprom_25lc640a.vhdp	Microchip 25LC640A SPI EEPROM Model
mc_eeprom_25lc128.vhdp	Microchip 25LC128 SPI EEPROM Model
mc_eeprom_25lc256.vhdp	Microchip 25LC256 SPI EEPROM Model

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release as shown in the table below.

Table 2: Model Release Levels

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completely Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Features

The feature of STMicroelectronics and Microchip SPI EEPROM models is listed in the table below.

Table 3: STMicroelectronics and Microchip SPI EEPROM Model Feature List

Feature	Support	Note
Write Enable	Yes	
Write Disable	Yes	
Write Status Register	Yes	
Read Status Register	Yes	
Write Memory Array	Yes	
Read Memory Array	Yes	
Write Identification Page	Yes	1
Read Identification Page	Yes	1
Read ID Page Lock Status	Yes	1
Lock ID Page in Read Only Mode	Yes	1
Memory Block Write Protection	Yes	
Status Register Write Protection	Yes	

1. This feature is only supported in STMicroelectronics SPI EEPROM models with “-D” series.

4. Configurations

The SPI EEPROM models are compliance with the data sheet of the corresponding SPI parts. Table 4 and Table 5 list some configurations for the models. Only a few features are listed. For more details, please check SPI EEPROM data sheet from vendor.

Table 4: STMicroelectronics SPI EEPROM Model List

Model Number	Density (bits)	Organization	Page Size (Bytes)	Identification Page
st_eeprom_m95080	8k	1k x 8	32	N.A.
st_eeprom_m95160	16k	2k x 8	32	N.A.
st_eeprom_m95320	32k	4k x 8	32	N.A.
st_eeprom_m95320d	32k	4k x 8	32	Support
st_eeprom_m95320a	32k	4k x 8	32	Support
st_eeprom_m95640	64k	8k x 8	32	N.A.
st_eeprom_m95640d	64k	8k x 8	32	Support
st_eeprom_m95640a	64k	8k x 8	32	Support
st_eeprom_m95128	128k	16k x 8	64	N.A.
st_eeprom_m95128d	128k	16k x 8	64	Support
st_eeprom_m95128a	128k	16k x 8	64	Support
st_eeprom_m95256	256k	32k x 8	64	N.A.
st_eeprom_m95256d	256k	32k x 8	64	Support
st_eeprom_m95256a	256k	32k x 8	64	Support
st_eeprom_m95512	512k	64k x 8	128	N.A.
st_eeprom_m95512d	512k	64k x 8	128	Support
st_eeprom_m95512a	512k	64k x 8	128	Support
st_eeprom_m95m01	1024k	128k x 8	256	N.A.
st_eeprom_m95m01d	1024k	128k x 8	256	Support
st_eeprom_m95m01a	1024k	128k x 8	256	Support
st_eeprom_m95m02d	2048k	256k x 8	256	Support

Table 5: Microchip SPI EEPROM Model List

Model Number	Density (bits)	Organization	Page Size (Bytes)	Identification Page
mc_eeprom_25lc080c	8k	1k x 8	16	N.A.
mc_eeprom_25lc080d	8k	1k x 8	32	N.A.
mc_eeprom_25lc160c	16k	2k x 8	16	N.A.
mc_eeprom_25lc160d	16k	2k x 8	32	N.A.
mc_eeprom_25lc320a	32k	4k x 8	32	N.A.
mc_eeprom_25lc640a	64k	8k x 8	32	N.A.
mc_eeprom_25lc128	128k	16k x 8	64	N.A.
mc_eeprom_25lc256	256k	32k x 8	64	N.A.

5. Model Block Diagram

5.1 Interface Diagram

The interface of STMicroelectronics and Microchip SPI EEPROM Models are depicted in Figure 1 and **Figure** 2 respectively. Signal description of the interface is listed in Table 6. For the use of these pins, please refer to related SPI EEPROM data sheet.

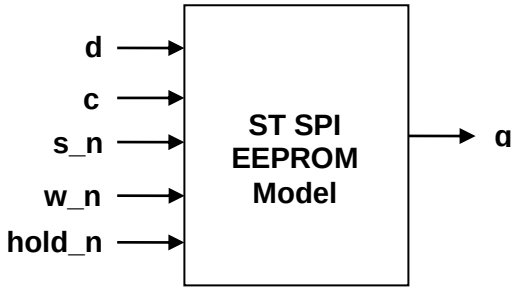

Figure 1: STMicroelectronics SPI EEPROM Model Interface Diagram

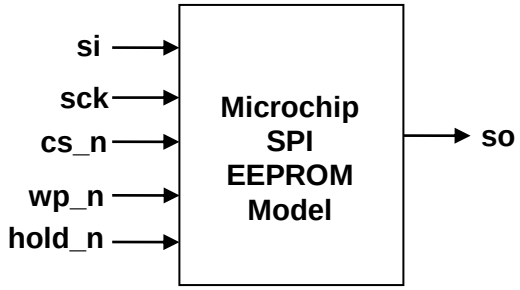

Figure 2: Microchip SPI EEPROM Model Interface Diagram

Table 6: Signal List of SPI EEPROM Model

Signal	Description	I/O
c / sck	Serial clock	Input
d / si	Serial data input	Input
q / so	Serial data output	Output
s_n / cs_n	Chip select	Input
w_n / wp_n	Write protect	Input
hold_n	Hold	Input

5.2 Connection Diagram

The connections between the SPI master controller and the SPI EEPROM model are drawn in the figure below.

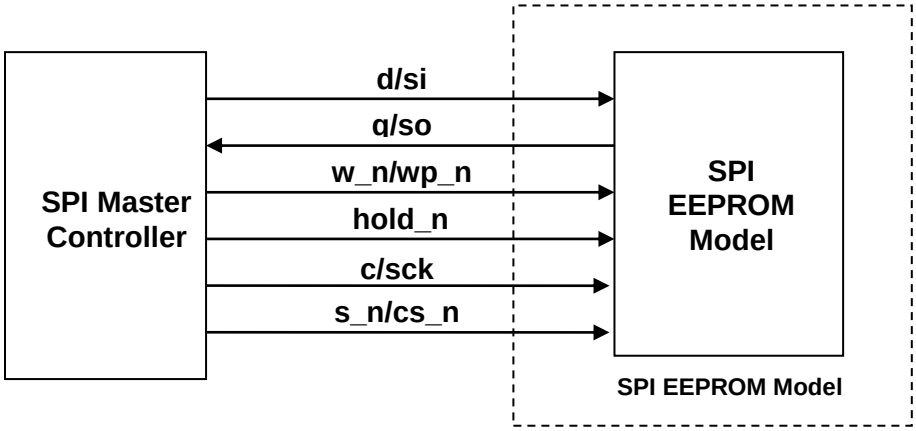

Figure 3: Connection Diagram

6. Limitations

There are some limitations for this version of the models, which are listed below:

- In SPI EEPROM model, the internal write cycle consumes shorter time than silicon's.
- The ECC function, supported in STMicroelectronics SPI EEPROMs, is not implemented in SPI EEPROM memory model. The ECC feature is transparent for SPI communications and the user controller never sees the ECC codes. It just repairs the error automatically and improves read reliability in silicon.
- The Standby Power Mode and the Active Power Mode does not imply that the memory model works under a different power supply current as described in EEPROM silicon's datasheet; in the model these modes just match the conditions and functions of these two power modes.

7. Model Emulation

7.1 Emulation Notes

There are several considerations when running emulation with the SPI EEPROM model in Palladium.

- The SPI EEPROM models are delivered as protected VHDL source code with specific EERPOM configuration unprotected.

- The top-level module name of the SPI EEPROM model is listed in the “Model Number” column of **Table 4** and **Table 5**. To use the model in your design, just instantiate the top level eeprom module and map the ports to your actual wires. For more details of the top-level declaration, please open the protected VHDL source with a text viewer and search the relevant top-level module name. For instance, if you use st_eeprom_m95128d memory model, yon can search “entity st_eeprom_m95128d” for the details of top-level declaration.

7.2 IXCOM Notes

For the IXCOM the SPI EEPROM model requires an internal clock generator called mmp_spi_clk_gen. This clock generator file, called mmp_spi_clk_gen.v, is located in the MMP top level common directory. Note that the clock generator module uses an IXCOM clock generator which is System Verilog based. As part of the IXCOM compile flow you must include the IXCclkgen.sv file from the UXE installation.

Below is an example of st_eeprom_m95128d model usage:

```
vlan mmp_spi_clk_gen.v

vhan -93 \
     st_eeprom_m95128d.vhdp

Other design files…

ixcom -ua \
      -top eeprom_tb \
      +dut+st_eeprom_m95128d
```

8. Revision History

The following table shows the revision history for this document.

Date	Version	Revision
September 2013	1.0	Initial release
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name. Update UXE / IXE documentation reference titles. Update related publications list.
June 2015	1.3	Add the “Features” chapter. Update model names and IXCOM compile section.
July 2015	1.4	Update Cadence naming on front page
September 2015	1.5	VHDL flow enhancements now a release old so removed compile related enhancement notes.
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Add the common mmp_spi_clk_gen description in IXCOM notes.
April 2017	1.8	Modify the common mmp_spi_clk_gen description in IXCOM notes, the mmp_spi_clk_gen link file is removed now.
January 2018	1.9	Modify header and footer