SYNOPSYS®

# DesignWare® Cores AP LPDDR5/4/4X PHY

## Reliability Report for Automotive Grade 2 (AP) TSMC7FFC18

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Synopsys, Inc.
690 E. Middlefield Road
Mountain View, CA 94043
www.synopsys.com

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# Revision History

| Date | Revision | Description |
|---|---|---|
| July 10, 2020 | 1.0 | Initial Release |
| | | |
| | | |
| | | |

# 1 Executive Summary

This report shows the results of the reliability tests Synopsys conducted to evaluate how DesignWare® Cores LPDDR5/4/4X PHY for TSMC 7FFC18 would qualify if submitted to the stress tests defined by the AEC-Q100 standards.

No problems were found during testing.

# 2
# Test Results

## 2.1 Qualification Test Plan

**Automotive Grade Level = 2 (-40 to +105C)**

| | |
|---|---|
| **Supplier Name:** | Synopsys |
| **Device Description:** | LPDDR5/4/4X PHY, part d859/879 |
| **General Specification:** | AEC-Q100 Rev. H |

| Test | Reference Standards | Test Conditions | Lots | S.S. | Total | Results Lot/Pass/Fail | Comments: (N/A =Not Applicable) |
|---|---|---|---|---|---|---|---|
| HTOL | JESD22 A108 | High Temp Operating Life:<br>Stress: $T_A$=105°C for 1000h<br>Pre/Post ATE test:<br>$T_A$ =room/cold/hot | 1 | 30 | 30 | 30 of 30 | |
| ELFR | AEC-Q100-008 | Early Life Failure Rate:<br>Stress: $T_A$ =105°C for 48h<br>Pre/Post ATE test:<br>$T_A$ =room/hot | 1 | 30 | 30 | 30 of 30 | |
| HBM | AEC-Q100-002<br>JS-001 | Electrostatic Discharge<br>Human Body Model:<br>Stress: 500V, 1KV, 2KV<br>HBM / Class 2<br>Pre/Post ATE test: $T_A$ =room/hot | 1 | 3 | 3 | 3 of 3<br>ESD Level = 2 | |
| CDM | AEC-Q100-011 | Electrostatic Discharge<br>Charged Device Model:<br>Stress: 500V / Class C2<br>Pre/Post ATE test: $T_A$ =room/hot | 1 | 3 | 3 | 3 of 3<br>ESD Level = C2 | Note 1 |
| LU | AEC-Q100-004<br>JESD78 | Latch-Up:<br>Stress: +/- 200mA<br>Pre/Post ATE test: $T_A$ =room/hot | 1 | 6 | 6 | 6 of 6 | |

Note 1) This IP supports CDM Class C2 and supports an SoC being tested to CDM Class C2A assuming the signals of this IP are not assigned to corner pins(/balls) of the package. The AEC-Q100 rating of CDM Class C2A is applicable to the SoC and is related specifically to 750V support at the corner pins(/balls). This IP is not intended to support 750V CDM and the customer of this IP should not assign signals of this IP to corner pins(/balls) of the SoC package. The customer of this IP may choose to leave the corner pins(/balls) of the SoC package unconnected, unpopulated, or assign to another function of the SoC or supply of the SoC such as a ground plane.

## 2.2 Summary of results

| Stress | Condition | Device IDs | ATE Test | Comments |
|---|---|---|---|---|
| HTOL | 105ºC / 1000h | 30 units | PASS | |
| ELFR | 105ºC / 48h | 30 units | PASS | |
| HBM | 500V, 1000V, 2000V | 1006, 1007, 1008 | PASS | |
| CDM | 500V | 1021, 1022, 1024 | PASS | |
| LU | 125ºC@200mA | 1013, 1014, 1015, 1016, 1017, 1019 | PASS | |

# 3
# Test Details

## 3.1 Package configuration

| | |
|---|---|
| **Type** | BGA |
| **Number of pins** | 400 |
| **Pin pitch** | 1 mm |
| **Body size** | 21 x 21 mm |

## 3.2 HTOL

| | |
|---|---|
| **Stress temperature** | +105 ºC |
| **Stress duration** | 1000h |
| **Operating mode during stress** | Test Burn In mode |
| **Sample size** | 30 |
| **Power Supply #1 – VDD** | 0.825V |
| **Power Supply #2 – VDDQ/VDDQLP** | 0.825V |
| **Power Supply #3 – CLK/JTAG/VDDQ1** | 3.3V / 1.2V / 1.2V |
| **Power Supply #4 – VAA** | 1.98V |

## 3.3 ELFR

| | |
|---|---|
| **Stress temperature** | +105 ºC |
| **Stress duration** | 60h |
| **Operating mode during stress** | Test Burn In mode |
| **Sample size** | 30 |
| **Power Supply #1 – VDD** | 0.825V |
| **Power Supply #2 – VDDQ/VDDQLP** | 0.825V |
| **Power Supply #3 – CLK/JTAG/VDDQ1** | 3.3V / 1.2V / 1.2V |
| **Power Supply #4 – VAA** | 1.98V |

## 3.4 HBM

***Tester details:***

Equipment ID: Thermo Mk.2-6

***Pins groupings:***

**Device Pin List and Test Groups**

| | | |
|---|---|---|
| IO | i/o | A2, B1, B20, B3, C2, D1, D18, D20, F1, F20, H1, H20, J19, J2, K1, K20, L19, M2, M20, N1, P2, R1, R11, R13, R16, R20, R3, R9, T10, T12, T14, T17, T19, T4, T6, T8, U13, U15, U16, U20, U5, U7, U9, V10, V12, V14, V17, V4, V6, V8, W1, W11, W13, W15, W18, W20, W3, W5, W7, W9, Y17, Y19, Y2, Y4, Y6 |
| IO2 | i/o | U18, V19 |
| IO3 | i/o | P19, R18 |
| IO4 | i/o | E19, F18 |
| IO5 | i/o | G19, H18 |
| IO6 | i/o | U1, V2 |
| IO7 | i/o | T2, U3 |
| IO8 | i/o | D3, E2 |
| IO9 | i/o | F3, G2 |
| VAA_VDD2 | power | R7 |
| VDD_CORE | power | G12, G13, G8, G9, H10, H11, H14, H15, H6, H7, J12, J13, J8, J9, K10, K11, K14, K15, L12, L13, L8, L9, M10, M11, M14, M15 |
| VDD_HM1 | power | F14- F16 |
| VDD_HM3 | power | F6, F7, F9, N12, N13, N16, N8, N9, P10, P14, P15, P17, P6, P7, R5 |
| VDD2_HM3 | power | P11 |
| VDD2GPIO | power | A10, A12, A14, A16, A18, A5, A8 |
| VDDQ_HM1 | power | C20, G17, G20, H16 |
| VDDQ_HM3 | power | A3, C1, G1, G5, J5, L5, M17, N5, P1, P20, T11, T15, T7, V1, V20, Y14, Y16, Y18, Y3, Y7, Y9 |
| VSS | ground | A1, A11, A13, A20, A7, A9, B10, B12, B14, B15, B17, B19, B2, B4, B6, B8, C11, C13, C15, C16, C18, C3, C5, C7, C9, D10, D12, D15, D17, D19, D2, D4, D6, D8, E1, E10, E11, E13- E16, E18, E20, E3, E5, E7, E8, F10, F12, F13, F17, F19, F2, F4, F8, G10, G14- G16, G18, G3, G6, G7, H12, H13, H17, H19, H2, H5, H8, H9, J1, J10, J11, J14- J18, J20, J3, J4, J6, J7, K12, K13, K19, K2, K4, K5, K8, K9, L1, L10, L11, L14, L15, L18, L2, L20, L3, M1, M12, M13, M16, M18, M19, M3, M5, M8, M9, N10, N11, N14, N15, N17, N19, N2, N20, N4, N6, N7, P12, P13, P16, P18, P3, P5, P8, P9, R10, R12, R14, R15, R17, R19, R2, R4, R6, R8, T1, T13, T16, T18, T20, T3, T5, T9, U10, U12, U14, U17, U2, U4, U6, U8, V11, V13, V15, V16, V18, V3, V5, V7, V9, W10, W12, W14, W16, W17, W19, W2, W4, W6, W8, Y1, Y11, Y13, Y15, Y20, Y5, Y8, U19 |
| NC | n/c | A15, A17, A19, A4, A6, B11, B13, B16, B18, B5, B7, B9, C10, C12, C14, C17, C19, C4, C6, C8, D11, D13, D14, D16, D5, D7, D9, E12, E17, E4, E6, E9, F11, F5, G11, G4, H3, H4, K16- K18, K3, K6, K7, L16, L17, L4, L6, L7, M4, M6, M7, N18, N3, P4, U11, Y10, Y12 |

***Stress pin combinations:***

| Pin Combination Set Number | Pin(s) Connected to Terminal B | Pin Connected to Terminal A (Single Pins, tested one at a time) |
|---|---|---|
| 1 | VSS | Every Supply Pin except pins of Supply Pin Group 1, Every Non-supply Pin |
| 2 | VAA_VDD2 | Every Supply Pin except pins of Supply Pin Group 2, Every Non-supply Pin |
| 3 | VDD_CORE | Every Supply Pin except pins of Supply Pin Group 3, Every Non-supply Pin |
| 4 | VDD_HM1 | Every Supply Pin except pins of Supply Pin Group 4, Every Non-supply Pin |
| 5 | VDD_HM3 | Every Supply Pin except pins of Supply Pin Group 5, Every Non-supply Pin |
| 6 | VDD2_HM3 | Every Supply Pin except pins of Supply Pin Group 6, Every Non-supply Pin |
| 7 | VDD2GPIO | Every Supply Pin except pins of Supply Pin Group 6, Every Non-supply Pin |
| 8 | VDDQ_HM1 | Every Supply Pin except pins of Supply Pin Group 6, Every Non-supply Pin |
| 9 | VDDQ_HM3 | Every Supply Pin except pins of Supply Pin Group 6, Every Non-supply Pin |
| 10 | All Non-supply Pins, except PUT | All Non-supply Pins, except PUT |
| 11 | One Pin of Each Coupled Non-Supply Pin Pair, one pair at a time | One Pin of Each Coupled Non-Supply Pin Pair, one pair at a time |

## 3.5 CDM

***Tester details:***

Equipment ID: Thermo Orion3

***Charging/Discharging method:***

Field-induced charging / Contact discharging.

## 3.6 Latch-Up

***Tester details:***

Equipment ID: Thermo Mk.4