DesignWare® Cores LPDDR5/4/4X Memory Controller

Installation Guide

DWC LPDDR5/4/4X Controller – Product Code: E092-0
DWC LPDDR5/4/4X Controller AFP – Product Code: E093-0
DWC AP LPDDR5/4/4X Controller – Product Code: E094-0

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Contents

Revision History

The following table provides a summary of changes made to this Installation Guide.

Version	Date	Description
1.10a-lca00	September 2021	**Added:** ■ "STAR on the Web (SotW)" on page 24 ■ "Synopsys Statement on Inclusivity and Diversity" on page 26 **Updated:** ■ Table 1-4 on page 15
1.01a-lca01	January 2021	**Updated:** ■ Table 1-2 "Licenses Required" ■ Table 1-4 "Supported Tool Versions" ■ Table 1-5 "Environment Variables for the DDR Controller" ■ "Tools"
1.00a-lca01	June 2020	Initial release

Note In some instances, documentation-only updates occur. The DesignWare IP product https://www.synopsys.com/designware-ip.html has the latest information.

1

Installing the DDR Controller

This guide provides information on how to install and set up the DesignWare® Cores DDR5/4 Memory Controller (referred to as DWC_lpddr54_controller). After you complete the installation procedure, you work primarily with the Synopsys coreConsultant tool to configure and synthesize the controller, and simulate it in the provided verification environment — a UVM-based Packaged Verification Environment (PVE). The PVE provides a starting point for understanding how to use DesignWare Verification IP (VIP) and the configured DDR controller together in your verification environment.

Attention	If the DDR controller is already installed and you are performing only the set-up procedures, check the component summary pages to confirm that you have the latest version. https://www.synopsys.com/dw/ipdir.php?c=dwc_lpddr54_controller

1.1 Accessing Product Documentation

Before you install the controller, you can download the full document set, including this document, the databook, user guide, and release notes, at the following link for DWC_lpddr54_controller:

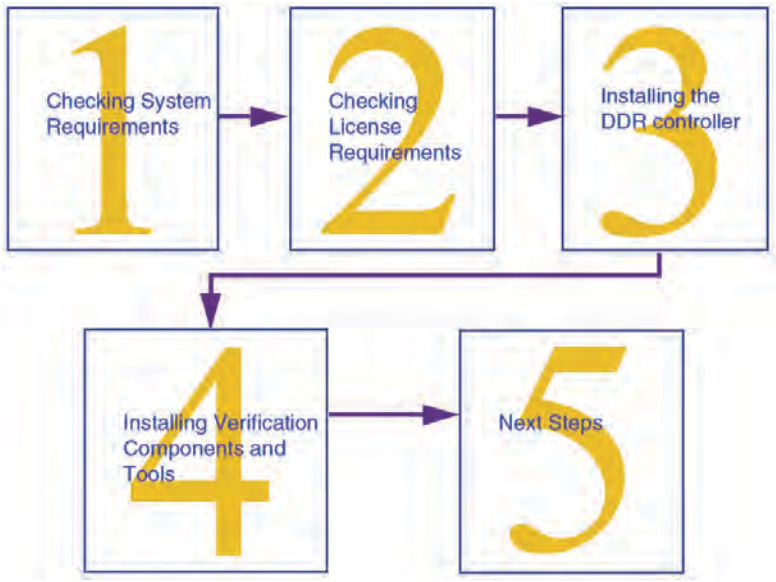
https://www.synopsys.com/dw/ipdir.php?c=dwc_lpddr54_controller

(A SolvNet ID and a valid product license is required.)

To access product documentation that resides in your installation directory, first create a workspace using coreConsultant. Instructions for creating a workspace are provided later in "Next Steps" on page 18.

1.2 Process Overview

To use the DDR controller, follow the steps in this installation guide.



- "Checking System Requirements" on page 10
- "Checking License Requirements" on page 11
- "Installing the DDR Controller" on page 7
- "Installing Verification Components and Tools" on page 15
- "Next Steps" on page 18

1.3 Checking System Requirements

Table 1-1 describes the system requirements for the DDR controller.

Table 1-1 System Requirements

Element	Requirement
Operating System	Current information about supported operating system configurations and required patches is at the “Release Specific Support” page at: https://www.synopsys.com/support/licensing-installation-computeplatforms/compute-platforms/compute-platforms-roadmap.html Select the entry that corresponds to the prefix letter for the first entry in the “Design Compiler (DC)” column of Table 1-4 on page 15. For example, “J”.
Disk Space	■ 150 MB available hard disk space for coreConsultant installation ■ 400 MB available hard disk space for the DDR controller
Memory	■ 1,024 MB available swap space ■ 1,024 MB RAM

Note You must have access towww.mydesignware.com to download the release image. You can sign up to receive updates for any DesignWare component through this web site.

1.4 Checking License Requirements

This section provides the required license information needed to use the DDR controller.

DesignWare IP uses the Synopsys Common Licensing (SCL) software to control its usage. You can find general SCL information at:

https://www.synopsys.com/support/licensing-installation-computeplatforms/licensing/scl-supported-os.html

1.4.1 Controller Licenses

Table 1-2 lists the licenses needed for the DDR controller.

Table 1-2 Licenses Required

Product Configuration	License Required
All; required to install the .run file	DWC-DDRCTL
DWC_lpddr54_controller	DWC-LPDDR54-CONTROLLER
Configurations with any of the following features: ■ UMCTL2_OCPAR_EN==1 ■ MEMC_INLINE_ECC = 1 ■ MEMC_ECCAP = 1 ■ UMCTL2_OCECC_EN = 1 ■ UMCTL2_REGPAR_EN = 1 ■ UMCTL2_OCCAP_EN==1 ■ MEMC_ECC_SUPPORT==1 ■ MEMC_LINK_ECC==1 (AFP or AP) ■ UMCTL2_HWFFC_EN==1 (AFP)	DWC-LPDDR54-CONTROLLER-AFP or DWC-AP-LPDDR54-CONTROLLER

The DDR controller is shipped with the licenses shown in Table 1-3.

To make full use of the DesignWare synthesizable components, you need additional licenses for the Synopsys and third-party tools for synthesis, TetraMax, Formality, PrimeTime, and HDL simulation. A Vera license is not required to run the verification environment supplied with the component.

Table 1-3 License Features Supplied with the DDR Controller

Function	License Feature (and Quantity)
RTL generation	DWC-LPDDR54-CONTROLLER (1) DWC-LPDDR54-CONTROLLER-AFP (1) DWC-AP-LPDDR54-CONTROLLER (1)
VC VIP Library (Some of these VIP licenses are only supplied in conjunction with specific DDR controller add-on licenses – see Table 1-2 on page 11)	VIP-LPDDR5-IIPACK

1.4.2 Setting License File Environment Variable

Make sure that your product's license keys are installed on your license server. For more information about installing license keys, refer to the following site:

http://www.synopsys.com/Support/LI/Licensing/Pages/default.aspx/

A SolvNet ID may be required to access this page.

You must set the SNPSLMD_LICENSE_FILE or LM_LICENSE_FILE environment variable to include a pointer to a license server that contains your license key for the DDR controller.

Note You must set this environment variable before you install the .run file; otherwise, only encrypted source files are installed and you receive errors if you try to configure the DDR controller using coreConsultant.

To set the license file environment variable:

1. Set the license variable to include your license file or point to your license server:

```
% setenv SNPSLMD_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}:<my_license_-
file|port@host>
```

or

```
% setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file|port@host>
```

Attention If you use both LM_LICENSE_FILE and SNPSLMD_LICENSE_FILE in your environment, ensure they are set to exactly the same string. For example:

```
% setenv SNPSLMD_LICENSE_FILE
${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
% setenv LM_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}
```

2. Verify the license setup:

```
% echo $LM_LICENSE_FILE
% lmstat -a -c $LM_LICENSE_FILE -f <LICENSE_NAME>
```

or

```
% echo $SNPSLMD_LICENSE_FILE
% lmstat -a -c $SNPSLMD_LICENSE_FILE -f <LICENSE_NAME>
```

Note

1. Use these commands to check the license setup for all of your component's required licenses.
2. For valid LICENSE_NAME strings, see Table 1-2 on page 11.

If you encounter any problems setting the license file environment variable, for more information, see "Licensing" on page 20.

1.5 Installing the DDR Controller

This section provides required steps and information to download and install the DDR controller image.

1.5.1 Downloading the DDR Controller

The latest version of the DDR controller is available through the DesignWare Download Web site.

1. Go to www.mydesignware.com (a SolvNet ID is required).
2. Expand DesignWare Cores and click the DWC_lpddr54 product for which you have a license. The product page of the component is displayed.
3. Click the link in the Download field.
4. Click dw_iip_DWC_ddrctl_lpddr54_1.10a-lca00.run to download the file to a Unix file server.
5. Make sure to save the .run file to a directory outside of any existing DESIGNWARE_HOME tree (any previously installed Synopsys IP tree).

1.5.2 Setting Up Your Environment

Before you install the DDR controller, you must set the following environment variables:

1. Set the DESIGNWARE_HOME environment variable to your installation directory:

   ```
   % setenv DESIGNWARE_HOME <path to c_ddrctl/DWC_ddrctl_Installation_Base_Directory>
   ```

2. Set either the SNPSLMD_LICENSE_FILE or the LM_LICENSE_FILE variable, if you have not already done so.

   ```
   % setenv SNPSLMD_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
   ```

   or

   ```
   % setenv LM_LICENSE_FILE ${LM_LICENSE_FILE}:<my_license_file|port@host>
   ```

3. Include the following in your PATH environment variable:

   ```
   $DESIGNWARE_HOME/bin
   ```

   $DESIGNWARE_HOME/bin is required in your PATH environment variable as it contains scripts that are necessary when using your DWC components. For more information about these scripts, see to Table A-1 on page 21.

Table 1-5 on page 16 summarizes the environment variables you may need to set when using the DDR controller. The “Example Setup File” on page 27 shows how to configure commonly used environment variables.

1.5.3 Installing the DDR Controller

The downloaded .run file is a self-extracting image that installs the IP product and performs some set-up operations. For more information about command options, enter:

```
% ./dw_iip_DWC_ddrctl_lpddr54_1.10a-lca00.run --help
```

For a list of the .run file command options, see “Options for .run Files” on page 29.

1. Change the permissions on the downloaded .run file:

   ```
   % chmod u+x dw_iip_DWC_ddrctl_lpddr54_1.10a-lca00.run
   ```

   If you want to view the README information before performing the installation:

```
% dw_iip_DWC_ddrctl_lpddr54_1.10a-lca00.run --readme
```

2. Execute the .run file:

```
% dw_iip_DWC_ddrctl_lpddr54_1.10a-lca00.run
```

3. When prompted, enter the Project ID that you specified at the time of purchase. Without a project ID, encrypted files are installed.
4. Important: Carefully review the installation transcript to make sure source RTL is installed. If you have entered the project ID incorrectly, the transcript indicates that encrypted RTL is installed.

For tips on debugging problems with installation, see "Troubleshooting and Support" on page 19.

1.5.4 DDR Controller Deliverables

The DDR controller is shipped with the following deliverables:

- Custom-configured Verilog RTL source code (using coreConsultant or coreAssembler)
- Synthesis, design-for-test, and power reduction scripts
- Verilog and SystemVerilog, UVM test environment
- DesignWare Cores LPDDR5/4/4X Databook (PDF)
- DesignWare Cores LPDDR5/4/4X User Guide (PDF)
- DesignWare Cores LPDDR5/4/4X Programming Guide (PDF)
- DesignWare Cores LPDDR5/4/4X Installation Guide (PDF)
- DesignWare Cores LPDDR5/4/4X Release Notes (PDF)

1.6 Installing Verification Components and Tools

This section includes information for the supported tools that allow you to configure, synthesize, and verify the DDR controller. Instructions for installing only coreConsultant are also provided in this section. If you need to install a synthesis or simulation tool, refer to the product documentation for that specific product.

1.6.1 Verifying Verification IP Components and Tool Versions

The tools listed in Table 1-4 have been tested for use with the DDR Controller. The list of qualified tools is complete at the time of this release. Releases subsequent to this one may also be qualified.

Table 1-4 Supported Tool Versions

Tool	Supported Versions	Purpose
coreConsultant	R-2020.12-SP3-1	Used for configuring the controller and running simulation and synthesis tools
Simulation tools[a]	Q-2020.03-SP2	Simulates the controller using the verification environment
Verdi	Q-2020.03-SP2-1	A waveform viewer to open FSDB databases
Design Compiler (DC) (optional)	R-2020.09-SP4	Synthesis (contains DFT Compiler)
Fusion Compiler (FC) (optional)	R-2020.09-SP4	Synthesis
Formality (optional)	R-2020.09-SP4	Formal verification
PrimeTime (optional)	R-2020.09-SP4	Timing and signal integrity
Spyglass (optional)	R-2020.12-SP1	Spyglass lint and CDC checking (only GuideWare, Version 2020.12 is supported)
VC SpyGlass (optional)	R-2020.12-SP1	VC SpyGlass Lint, CDC and RDC verification.
VC VIP Library ■ SVT[b] ■ AMBA SVT (APB, AXI, CHI) ■ DDR SVT ■ LPDDR SVT ■ DFI SVT[c]	■ S-2021.06 ■ S-2021.06 ■ S-2021.06 ■ S-2021.06 ■ S-2021.06	Used when simulating the DDR controller verification environment. Licenses of Synopsys Verification IP used in the testbench are included with the controller. You only have to download the AMBA VIP and amba svt .run files Download information is in “Downloading and Installing Synopsys Verification IP” on page 17. If the supported versions are not available on Solvnet, please contact Synopsys VIP support.

a. To run 64-bit simulations, make sure you select the 64-bit option in coreConsultant (Edit > Tool Installation Roots dialog), which sets environment variables to point to the 64-bit version of the simulator.
b. SVT is the base library of other VIP. It is installed together with other VIPs
c. Although, installing DDR installs the DFI SVT, the DFI SVT version listed in the table must be explicitly downloaded and installed for this release.

Note While no VHDL simulators are supported, you can generate a VHDL GTECH netlist of the design for use in your own environment.

1.6.2 Setting Environment Variables for Tools

Table 1-5 describes the environment variables required for the supported synthesis and simulation tools.

Table 1-5 Environment Variables for the DDR Controller

Tool	Environment Variable	Description
Synthesis Tools		
Design Compiler, Fusion Compiler, Formality, PrimeTime, Synplicity, Other third-party tools	SYNOPSYS	Path to Synopsys tools tree (Design Compiler and others)
	PATH	$SYNOPSYS/bin Path to <tool> bin directory, if used
	DESIGNWARE_HOME	Path to the DDR controller installation base directory
	SNPSLMD_LICENSE_FILE or LM_LICENSE_FILE	Path to license file for Synopsys tools such as Design Compiler, VCS, SpyGlass, any third-party tool)
Simulation Tools		
LD_LIBRARY_PATH		Path to OS and tool libraries
VCS	VCS_HOME	Path to VCS installation directory. For more information, see the VCS documentation
	VCS_CC	Path to SunPro C or gcc compiler
	VCS_BITMODE	Specifies 32- or 64-bit operation for VCS simulator
	PATH	Include the absolute path to $VCS_HOME/bin
VERDI	VERDI_HOME	Path to VERDI installation directory
	VERDI_LIB	$VERDI_HOME/share/PLI/VCS/LINUX64
	PATH	Include the absolute path to $VERDI_HOME/bin
	VERDI_BITMODE	Specify 32 or 64-bit install for Verdi

1.6.3 Downloading and Installing coreConsultant

The Synopsys coreConsultant is a tool that is used to configure, verify, and synthesize the DDR controller. Supported versions of coreConsultant are listed in Table 1-4 on page 15. If you do not have a supported version of coreConsultant installed on your system or network, you must download and install it. If a supported version of coreConsultant is already installed, skip to "Setting Environment Variables for Tools" on page 16.

1. Go to the SolvNet Download Center, at:
   https://solvnet.synopsys.com/DownloadCenter/dc/product.jsp
2. Click "coreConsultant (coreTools)" in the "My Product Releases" list.
3. Select the required version of the coreConsultant from the versions list.

4. Download the coreConsultant either by clicking the Download Here button or the “Download via FTP” link. For the instructions to download the coreConsultant, click “FTP Download Instructions.”
5. The coretools_INSTALL_README.txt file is available for download from the download center when you click the Download Here button or from the FTP site. This file provides the instructions necessary to install coreConsultant. Follow the instructions in the README file to install coreConsultant.

1.6.4 Downloading and Installing Synopsys Verification IP

The testbenches provided with the DDR controller use Synopsys Verification IP. If you do not have supported versions of Synopsys Verification IP installed (specified as “VC VIP Library” in Table 1-4 on page 15), you must install them by performing the following steps:

To install Synopsys VC VIP Library IP:

1. Select “VC VIP Library” from the SolvNet Download Center, at:

   https://solvnet.synopsys.com/DownloadCenter/dc/product.jsp
2. Select “VC VIP Library” version specified in Table 1-4 on page 15 and download the .run files.
3. Install the Synopsys AMBA, DDR, and LPDDR Verification IP following the instructions in VC_VIP_Library_README.txt.

1.7 Next Steps

After installing the DDR controller and setting up your environment, the next steps are to configure, synthesize, simulate, and export the controller into your design. For information about configuring, synthesizing, verifying, and integrating the DDR controller, see the DesignWare Cores LPDDR5/4/4X Controller User Guide. For architectural, functional, and configuration parameter descriptions, see the DesignWare Cores LPDDR5/4/4X Controller Databook. For programming sequences and register descriptions, see the DesignWare Cores LPDDR5/4/4X Controller Programming Guide. After you create a workspace, all documents are available in the doc directory of your workspace and in the coreConsultant Help menu.

A

Troubleshooting and Support

This appendix provides troubleshooting information and details on how to contact customer support should you need further assistance during installation and set up.

A.1 Troubleshooting

This section provides troubleshooting tips if you encounter problems with licensing, installation, setting up your environment, and supported tools. If your troubleshooting uncovers a problem that you cannot solve, open a Customer Support case as described in section "Customer Support" on page 26.

A.1.1 Licensing

Question:

I did a source installation, but when I invoked coreConsultant to configure the controller, I got encrypted RTL. Why?

Answer:

You receive this error when your source installation is not done properly. Either the Project ID (PID) is not entered correctly or not entered at all, or the SNPSLMD_LICENSE_FILE (or LM_LICENSE_FILE) is not set properly – that is, not pointing to the server that has a source license.

You must set either the LM_LICENSE_FILE or SNPSLMD_LICENSE_FILE environment variable BEFORE you install the dw_iip_DWC_ddrctl_1.10a-lca00.run file. For more information about setting this environment variable, see "Setting License File Environment Variable" on page 12.

A.1.2 Installation

Question:

How can I make sure that the source installation was done properly?

Answer:

You can make sure that the source installation is done properly in one of three ways:

- Go to the $DESIGNWARE_HOME/iip/DWC_ddrctl/latest/auxiliary directory and check to see that the .DWC_lpddr54 file is present in this directory.
- Configure the IP in coreConsultant and check the <workspace>/src directory for source RTL.
- The .run installer script writes out a log file that you can use to debug any issues with installation. The log file is located in the installation directory and is named as follows:

  `<image>_<yyyymmdd>_<hhmmss>_<processid>.log`

  By default, this log file is retained only if errors occur; it is removed if installation completes successfully. To retain the log file irrespective of the installation status, you can use the `--keep-log` switch with the .run installer script:

  ./<product_name>_<version>.run --keep-log

A source license gives you access to all of the files when you configure your controller. If you do not have a source license, you can only access a limited number of files (such as the top-level <core_name>.v and the <controller_name>_cc_constants.v files). Other files are encrypted.

Question:

How do I verify that I installed the DDR controller correctly?

Answer:

Once you have correctly downloaded and installed the controller, the product deliverables are unpacked into the $DESIGNWARE_HOME directory (environment variable you set that points to the installation root directory).

To view the contents of the directory in the $DESIGNWARE_HOME path, enter the following command at a Unix prompt:

```
% ls -l $DESIGNWARE_HOME/iip/DWC_ddrctl_<controller>/latest
```

Note The latest directory is a symbolic link to the DWC_ddrctl_<controller>/<current_version> directory.

Figure Figure D-2 on page 31 illustrates the directory structure after you have installed the product in the $DESIGNWARE_HOME directory.

Question:

How can I verify the version of my installed DesignWare Cores product to make sure I have the latest version?

Answer:

To verify whether your DesignWare Cores products are current, use one of the following methods:

- Subscribe to MyDesignware notifications on a component basis, where you receive an email when a component updates or has new/updated STAR information.
- Enable automatic update checking in coreConsultant to check the components in your design against both your DesignWare Cores and the currently supported Synopsys components.

  Table A-1 on page 21 provides more information about these features.

Table A-1 DesignWare Component Update Features

DesignWare Update Feature	Description
MyDesignWare Notifications	Enables you to receive product updates, technical articles, in-depth application notes and more for products of interest to you. You can add or remove selected subscriptions at any time. Sign-up through your SolvNet user account at: https://www.synopsys.com/dw/mydesignware.php myDesignWare subscriptions include: ■ DesignWare Technical Bulletin ■ DesignWare Component Notifications
coreTools Update Checking	When you complete the Specify Configuration activity in coreConsultant, it checks your component versions against the most recent versions available both for download from Synopsys, and in your local $DESIGNWARE_HOME library. A report gives you newer version information, if available, and lists STARs created/fixed for the components you are using. You can manually check at any time using Help > Check for IP Updates. For more information about Automatic/Manual IP update checks in coreConsultant, see “Component Update Checking” in the coreConsultant User Guide. **NOTE:** Components are not automatically updated; this operation only generates a report. You must make these component updates manually.

A.1.3 Tools

Question:

I have a DesignWare license and installed the image properly. When I invoke coreConsultant, I get the following message. Why?

```
Command not found
```

Answer:

You get this message because coreConsultant is not installed or the $PATH is not updated with the path to the coreConsultant tool installation directory. It is not a part of an image and has to be installed separately. For more information about installing coreConsultant, see "Downloading and Installing coreConsultant" on page 16*. The other possibility is not having DESIGNWARE_HOME/bin in the PATH.*

Question:

How can I tell if coreConsultant is installed?

Answer:

Issue the following command, which should return the path to your coreConsultant installation directory. If not, complete the steps in "Downloading and Installing coreConsultant" on page 16.

```
% which coreConsultant
```

Question:

How can I verify if my tools are correctly set up to work with coreConsultant?

Answer:

After completing the controller installation and setting the required environment variables, confirm system and coreConsultant access to the tools:

1. Check that you have access to the supported tools specified in Table 1-4 on page 12, as follows:

   ```
   % echo $SYNOPSYS
   % which coreConsultant
   % which vcs
   ```

2. Set DESIGNWARE_HOME to the controller installation base directory where you installed the DWC_ddrctl_lpddr54 files, then invoke coreConsultant:

   ```
   % setenv DESIGNWARE_HOME <Installation_Base_Directory>
   % coreConsultant &
   ```

3. Click the DWC_ddrctl_lpddr54 link to create a new configuration.
4. In the coreConsultant menu bar, select Edit > Tool Installation Roots to verify valid versions of all tools needed. These may include:
   - Design Compiler (dc_shell)
   - Fusion Compiler (fc_shell)
   - PrimeTime (pt_shell)
   - Formality (fm_shell)
   - TetraMax (tmax)
   - Synplify FPGA (synplify)
5. Exit coreConsultant by selecting File > Exit from the menu bar.

Note	If you want to use the 64-bit execution, make sure to select the 64-bit option in **Edit > Tool Installation Roots**

A.2 STAR on the Web (SotW)

You must review all STARs on the Web (SotWs) associated with your product. SotWs are considered a part of the Synopsys documentation suite, and show critical information related to your product. To review product SotWs, refer to the DesignWare IP product information:

https://www.synopsys.com/designware-ip.html

A.3 Synopsys Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

A.4 Customer Support

To obtain support for your product, choose one of the following:

1. Prepare the following debug information, if applicable:
   - For environment setup problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, use the following menu entry:

     `File > Build Debug Tar-file`

     Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file <core tool startup directory>/debug.tar.gz.
   - For simulation issues outside of coreConsultant or coreAssembler:
     - Create a waveforms file (such as VPD or FSDB)
     - Identify the hierarchy path to the DesignWare instance
     - Identify the timestamp of any signals or locations in the waveforms that are not understood
2. Contact the Support Center with a description of your question and supply the previously mentioned information, using one of the following methods:
   - For fastest response, use the SolvNet website. If you fill in your information as explained here, your issue is automatically routed to a support engineer who is experienced with your product. The Sub Product entry is critical for correct routing.

     Go to http://solvnet.synopsys.com/support/open_case.action. Provide the requested information, including:
     - Product: DesignWare Cores
     - Sub Product: Memory - Controller
     - Version: 1.10a-lca00
     - Problem Type:
     - Priority:
     - Title: <insert the appropriate controller name>
     - Description: For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

     After creating the case, attach any debug files you created in the previous step.
   - Or, send an e-mail to support_center@synopsys.com (your e-mail is queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
     - Include the Product name, Sub Product name, process, Product version, and Tool Version number in your e-mail (as identified previously) so it can be routed correctly.
     - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.
     - Attach any debug files you created in the previous step.
   - Or, telephone your local support center:
     - North America: call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
     - All other countries: http://www.synopsys.com/Support/GlobalSupportCenters

B

Example Setup File

The following example setup file demonstrates how to configure the required environment. The example shows both supported simulation tools, choose the commands for the tool you are using and replace the example directory paths and placeholders (in <...>) with the correct paths for your tool installations.

Note When you create your setup file, name it as .setup and then place it in the root of your DDR controller installation directory.

Example of Setup File

```
# Synopsys Setup
setenv SYNOPSYS <synopsys_install_dir>
set path = ($path $SYNOPSYS/bin)
set path = ($path $SYNOPSYS/<platform>/syn/bin)


# DESIGNWARE_HOME
setenv DESIGNWARE_HOME <DDR Controller_Installation_Base_Directory>


# coreConsultant Setup
set path = ($path <cC_install_dir>/bin)


# VCS Setup
setenv VCS_HOME <vcs_install_dir>
setenv VCS_CC /opt/SUNWspro/bin/cc
set path = ($path ${VCS_HOME}/bin)


# Formality Setup
set path = ($path <fm_install_dir>/bin)


# License Setup
setenv SNPSLMD_LICENSE_FILE ${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
```

C

Options for .run Files

The dw_iip_DWC_ddrctl_1.10a-lca00.run file is a self-extracting image that contains the DDR controller. Executing the dw_iip_DWC_ddrctl_1.10a-lca00.run file without optional switches extracts (installs) the image to a $DESIGNWARE_HOME, if available, or to a specified directory.

You can choose only one of the following optional switches:

--help	Displays this message and exits.
--readme	Displays additional installation information, if available and exits.
--check	Checks image integrity and exits.
--dir <path>	Installs product into <path> instead of $DESIGNWARE_HOME

If you are doing an installation, you can use either of the following options:

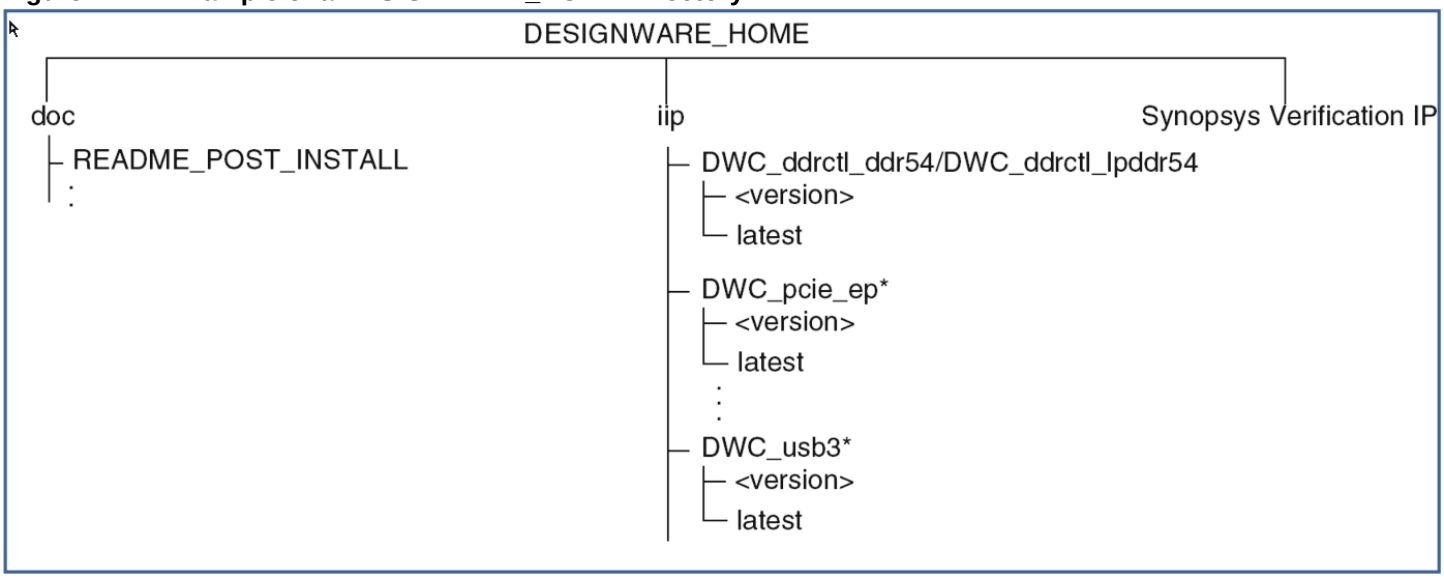
--keep-log	Keeps the installer log file regardless of the error count. By default, the log is deleted when there are no errors.
--quiet	Eliminates confirmation prompts.

D

DESIGNWARE_HOME Directory Structure

This appendix provides two examples of a DESIGNWARE_HOME directory—a top-level view (Figure D-1) and the directory structure after you have installed the DDR controller into the DESIGNWARE_HOME directory (Figure D-2) and the VIP libraries (Table 1-4 on page 15). Directory name "Synopsys Verification IP" is arbitrary (you choose it during IP installation). It also describes the directory structure of the DDR controller (Table D-1).

Figure D-1 Example of a DESIGNWARE_HOME Directory



*Multiple DesignWare Cores, Synopsys Verification IP, and DesignWare Library Synthesizable IP can reside in DESIGNWARE_HOME.

Figure D-2 Directory Structure of $DESIGNWARE_HOME/iip/DWC_ddrctl_lpddr54/latest

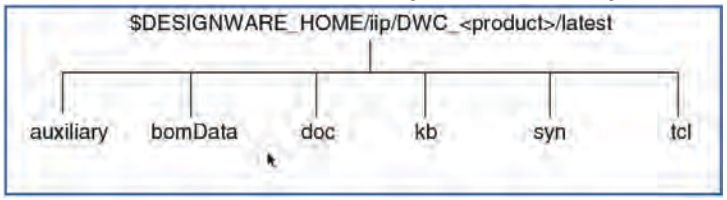


Table D-1 provides a description of the directories in the $DESIGNWARE_HOME/iip/DWC_ddrctl_lpddr54/latest directory.

Table D-1 $DESIGNWARE_HOME/iip/DWC_ddr_lpddr54/latest

Directory	Description
auxiliary	Scripts and text files used by coreConsultant.
bomData	Build Of Material data used by coreConsultant to create the RTL based on the configuration selected.
doc	Contains the DDR controller product documentation, such as the databook, user guide, installation guide, and release notes (pdf files).
kb	Contains knowledge base information used by coreConsultant. These are binary files containing information regarding the state of the design.
syn	Contains synthesis files for the DDR controller.
tcl	Contains synthesis intent scripts.