Technical Note

LPDDR5 Non-Target On-Die Termination

Introduction

DRAM non-target on-die termination (NT ODT) is a new feature introduced LPDDR5. The purpose of NT ODT is to improve signal integrity for DQ bus signals (DQ, DMI, RDQS) in a dual-rank configuration. In this configuration, DQ/DMI/DQS signals from controller to LPDDR5 are point-to-2-point connections. During READ or WRITE operation, reflection from a non-target DRAM device causes some noise and deteriorates signal waveforms at the receiver. Enabling termination on non-target DRAM devices reduces reflection and improves signal waveforms at the receiver.

NT ODT Overview

The DRAM NT ODT function is enabled by MR11 OP[3] = 1b, and its ODT value is set by MR41 OP[7:5]. The NT ODT is activated at all states. A simple DRAM ODT configuration at read and write is shown in the figure below. NT ODT enabling pins should be driven LOW in standby mode to avoid current leakage. A loopback test function for debugging and testing between the device and system on a chip (SOC) is supported by enabling the MR41 OP[7:5] NT ODT setting.

Figure 1: DRAM ODT Configuration of NT ODT Mode

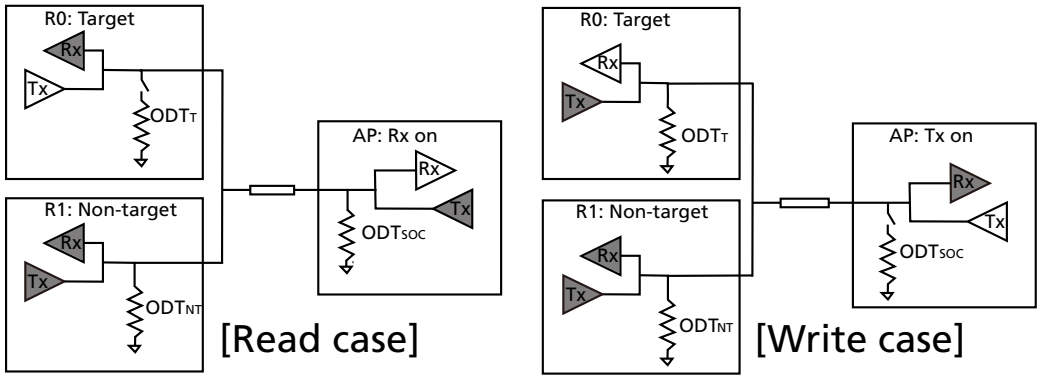

Table 1: ODT Status

Current DRAM State	Non-Target DRAM State	Target DRAM State
Power-down	NT ODT value (MR41 OP[7:5])	NT ODT value (MR41 OP[7:5])
Self refresh power-down		
Deep-sleep mode		
Precharge/active standby		
Write/masked write/write-FIFO		Target DRAM ODT value (MR11 OP[2:0])
Read/read-FIFO/read DQ calibration/MRR		PDDS/PUDS

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Table 2: MR11 Op Code Bit Definitions

Feature	Type	OP	Definition
DQ ODT (DQ bus receiver on-die termination)	R/W	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU
NT ODT EN (non-target on-die termination enabled)		OP[3]	0b: Target ODT mode (default) 1b: Non-target ODT mode

Table 3: MR41 Op Code Bit Definition

Feature	Type	OP	Data
NT DQ ODT (non-target DQ bus receiver on-die termination)	W	OP[7:5]	000b: Disable
			001b: RZQ/1
			010b RZQ/2
			011b: RZQ/3 (default)
			100b: RZQ/4
			101b: RZQ/5
			110b: RZQ/6
			111b: RFU

Because NT ODT must be used with target ODT, the mode register (MR) combination that disables DQ ODT and enables NT ODT is inhibited (MR11 OP[2:0] = 000B, MR11 OP[3] = 1b).

The table below shows all combinations where equivalent ODT is RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.

Table 4: Combination of Target ODT, NT ODT, and SOC ODT

ODT_{NT}	ODT_T	ODT_{SOC}	Write (ODTeq = ODT_{NT}‖ODT_T)	Read (SOC ODT MR17 OP[2:0])
RZQ/1	RZQ/1	RZQ/0 (disabled)	RZQ/2	RZQ/1
	RZQ/2	RZQ/1	RZQ/3	RZQ/2
	RZQ/3	RZQ/2	RZQ/4	RZQ/3
	RZQ/4	RZQ/3	RZQ/5	RZQ/4
	RZQ/5	RZQ/4	RZQ/6	RZQ/5
	–	RZQ/5	–	RZQ/6

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Table 4: Combination of Target ODT, NT ODT, and SOC ODT (Continued)

ODT_{NT}	ODT_T	ODT_{SOC}	Write ($ODTeq = ODT_{NT} \| ODT_T$)	Read (SOC ODT MR17 OP[2:0])
RZQ/2	RZQ/1	RZQ/0 (disabled)	RZQ/3	RZQ/2
	RZQ/2	RZQ/1	RZQ/4	RZQ/3
	RZQ/3	RZQ/2	RZQ/5	RZQ/4
	RZQ/4	RZQ/3	RZQ/6	RZQ/5
	–	RZQ/4	–	RZQ/6
RZQ/3	RZQ/1	RZQ/0 (disabled)	RZQ/4	RZQ/3
	RZQ/2	RZQ/1	RZQ/5	RZQ/4
	RZQ/3	RZQ/2	RZQ/6	RZQ/5
	–	RZQ/3	–	RZQ/6
RZQ/4	RZQ/1	RZQ/0 (disabled)	RZQ/5	RZQ/4
	RZQ/2	RZQ/1	RZQ/6	RZQ/5
	–	RZQ/2	–	RZQ/6
RZQ/5	RZQ/1	RZQ/0 (disabled)	RZQ/6	RZQ/5
	–	RZQ/1	–	RZQ/6
RZQ/6	RZQ/0 (disabled)	RZQ/0 (disabled)	RZQ/6	RZQ/6

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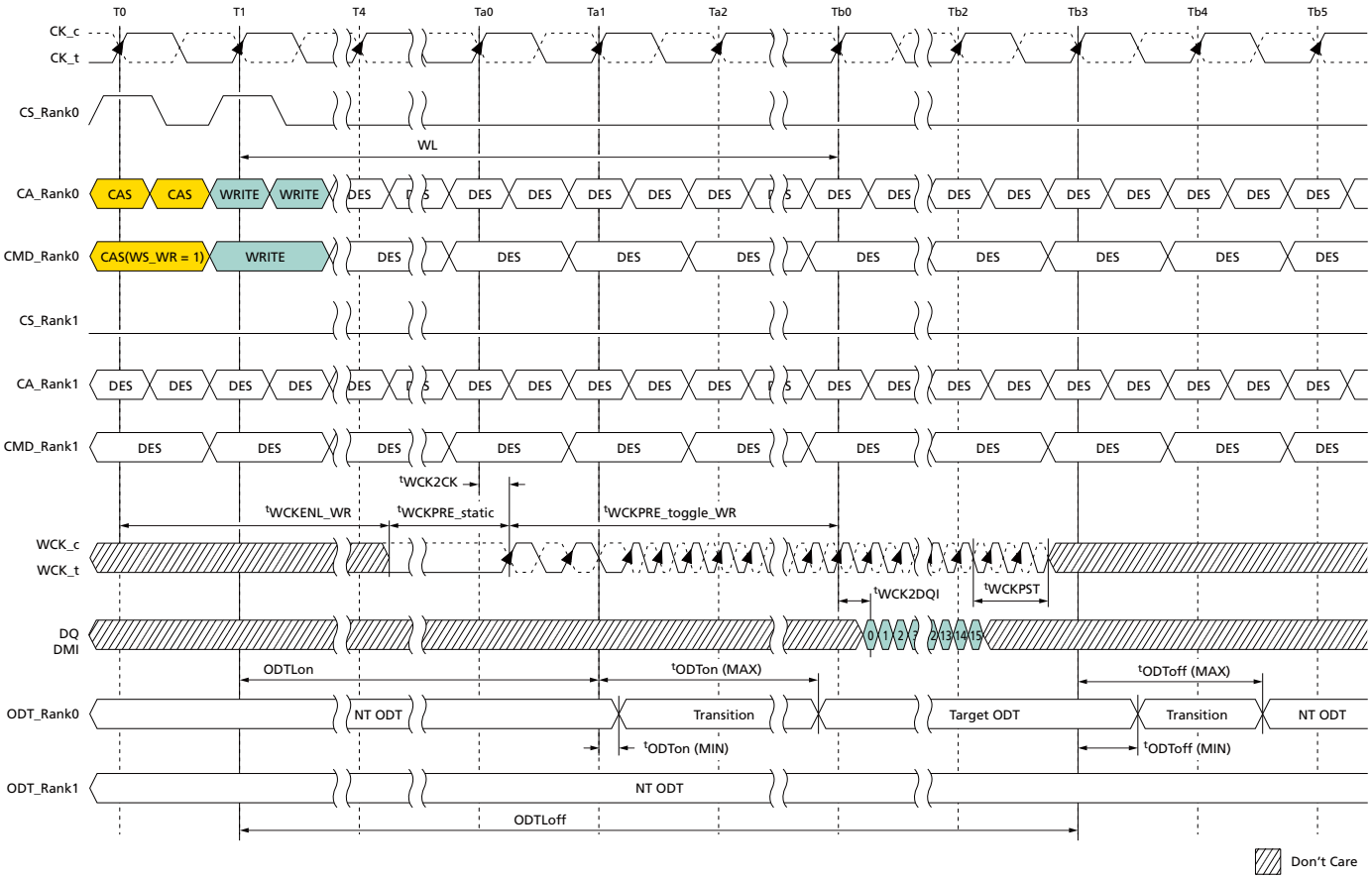
NT ODT Timing

Timing During Write

When NT ODT mode is enabled, ODT timings (ODTLon, ODTLoff) are referenced to the WRITE command, and the ODT value in the target rank can be updated within ^{t}ODTon,max, as shown in the figure below. After a WRITE operation, the target ODT value should be recovered to a predefined non-target DRAM ODT value within ^{t}ODToff,max.

Figure 2: ODT Control on a Non-Target DRAM for Write (MR0 OP[0] = 0b)



Timing During Read

When NT DRAM ODT mode is enabled, ODT timings (ODTLoff_RD, ODTLon_RD) are referenced to the READ command, and the ODT value in the target rank is disabled within ^{t}ODT_RDoff,max, as shown in the figure below. After a READ operation, disabled ODT should be recovered to a predefined non-target DRAM ODT value within ^{t}ODT_RDon,max.

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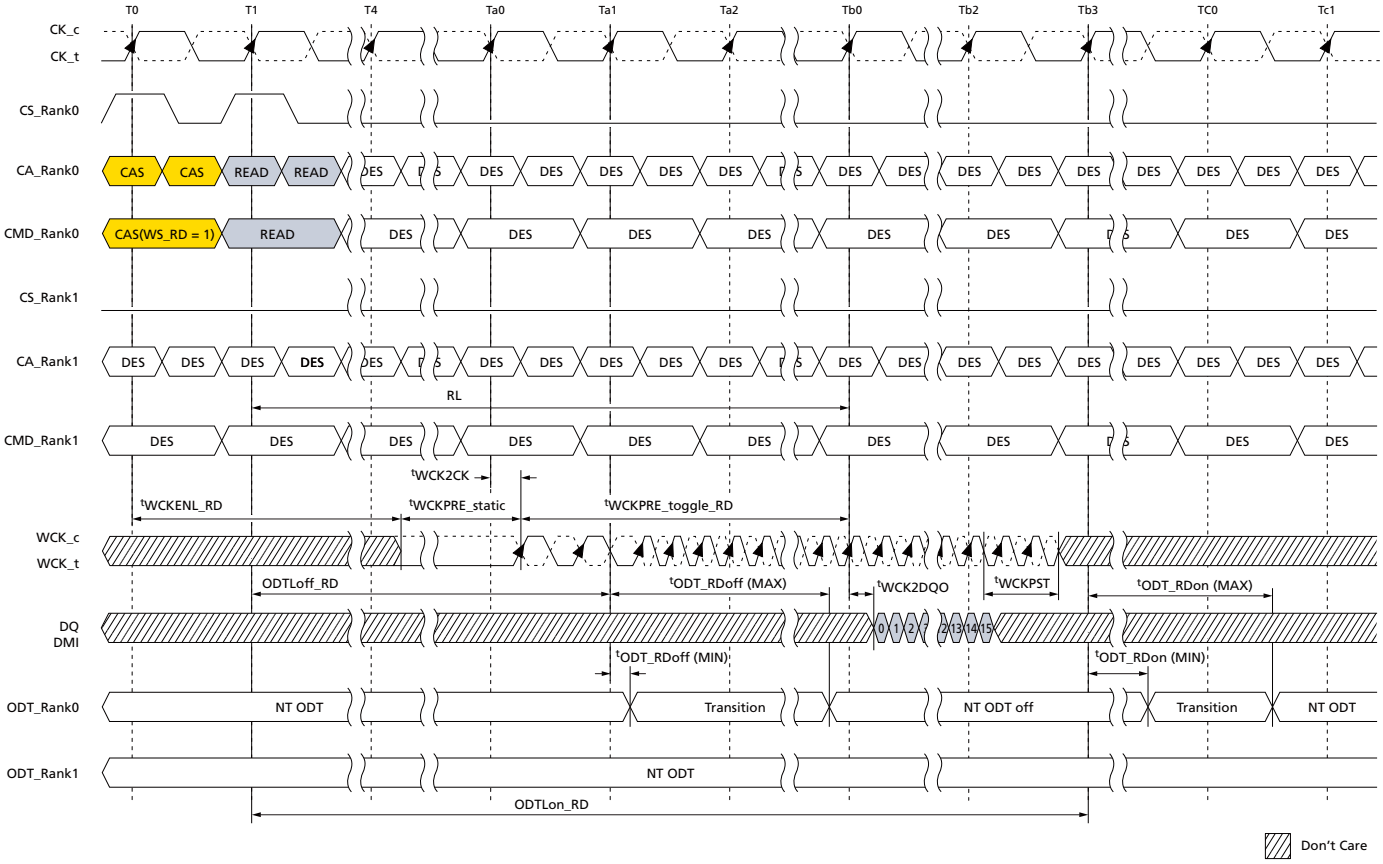
Figure 3: ODT Control on a Non-Target DRAM for Read



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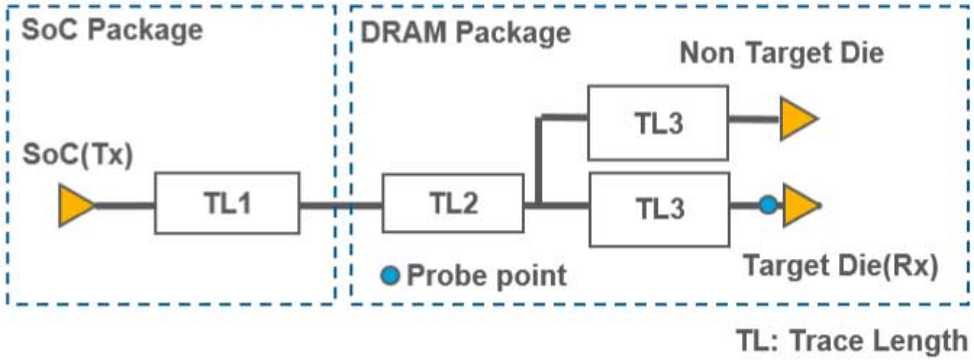
NT ODT Simulation

WRITE Operation Signal Integrity Improvement

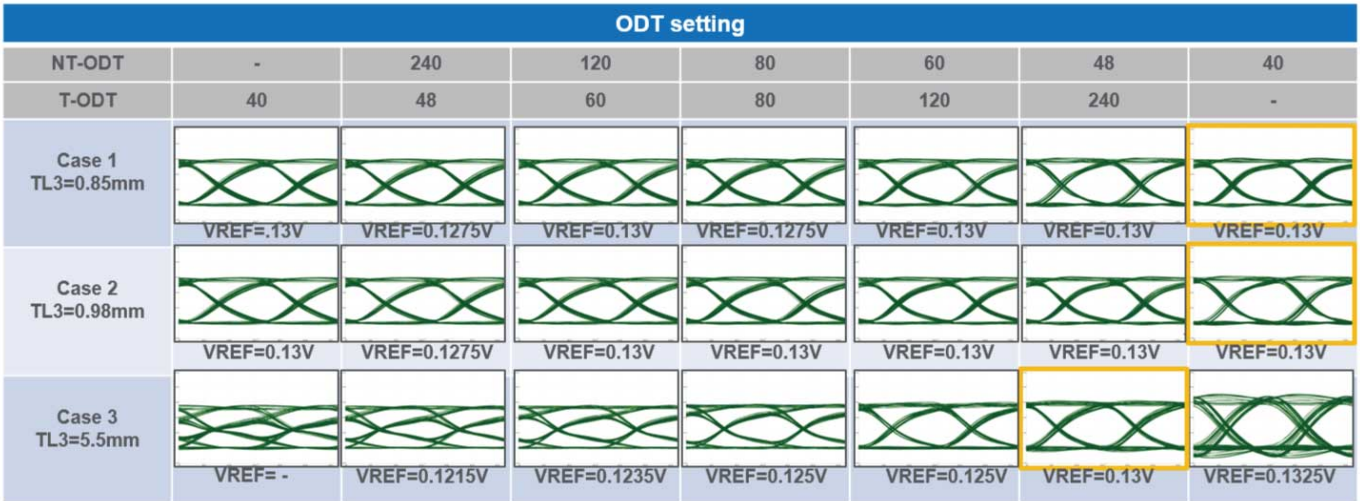
The figure below shows the LPDDR5 package stacked on a SOC package in a package-on-package (POP) configuration. TL3 is the stub length and simulation is done for three TL3 values: 0.85mm, 0.98mm, and 5.5mm.

Figure 4: WRITE Operation Topology



As shown in the figure below, if the stub length is short (TL3 = 0.85mm or 0.98mm), the signal waveform is clean even without NT ODT. However, when the stub length is very long (TL3 = 5.5mm), the signal waveform degrades and the data eye is significantly reduced without NT ODT. As the NT ODT value is reduced (stronger ODT), the data eye becomes larger. (The largest eye opening with NT ODT = 48 ohm and target ODT = 240 ohm for Case 3.)

Figure 5: WRITE Operation Simulation Waveform



The figure below shows the data eye value derived from the WRITE operation simulation waveform shown above.

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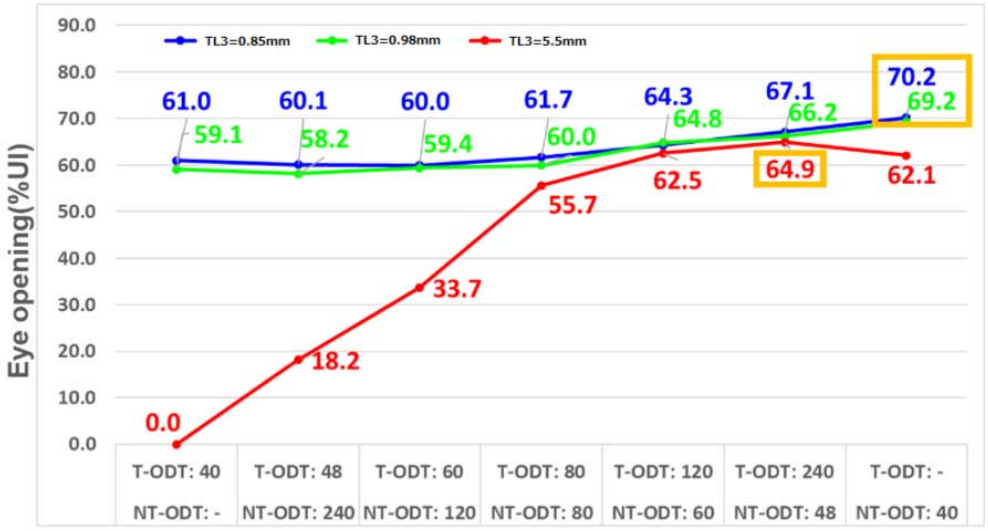
Figure 6: WRITE Operation Data Eye Result



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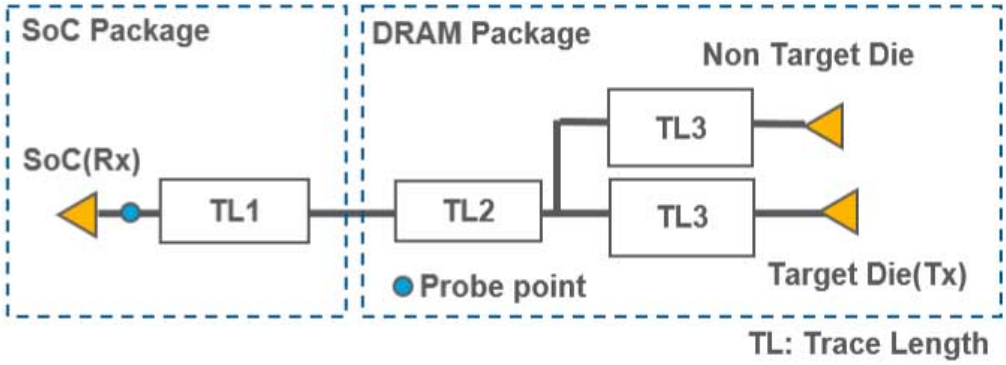
READ Operation Signal Integrity Improvement

READ operation topology is the same as WRITE operation topology, but the opposite data direction.

Figure 7: READ Operation Topology



As shown in the figure below, if the stub length is short (TL3 = 0.85mm or 0.98mm), the signal waveform is clean even without NT ODT. However, when the stub length is very long (TL3 = 5.5mm), the signal waveform degrades and the data eye is significantly reduced without NT ODT. As the NT ODT value is reduced (stronger ODT), the data eye becomes larger. (The largest eye opening with NT ODT = 120 ohm and target SOC ODT = 60 ohm for Case 3.)

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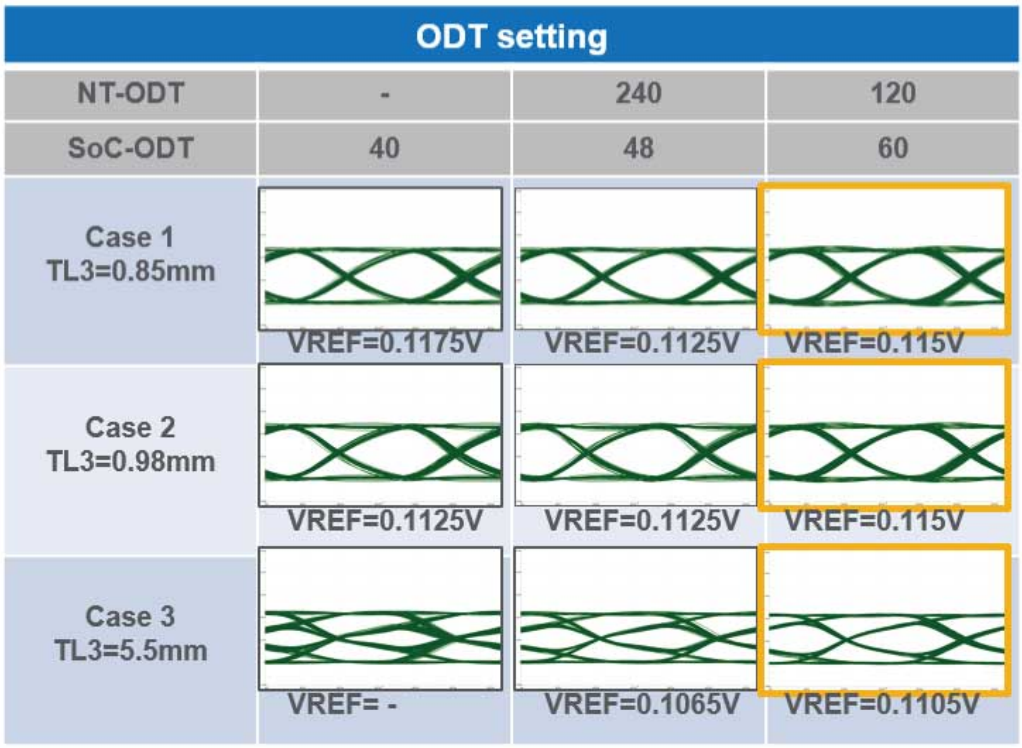
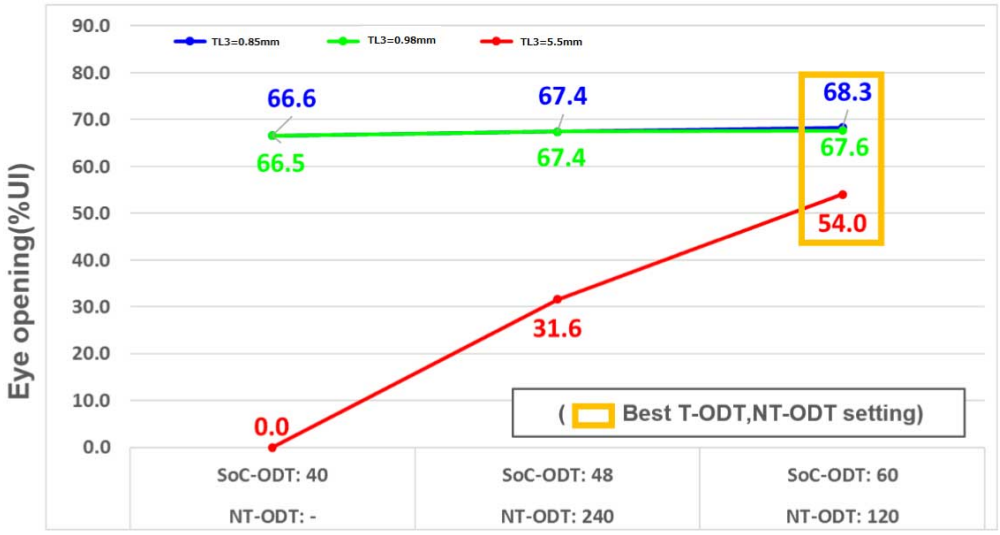
Figure 8: READ Operation Simulation Waveform



The figure below shows the data eye value derived from the READ operation simulation waveform shown above.

Figure 9: READ Operation Data Eye Result



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NT ODT value selection

Important Note

NT ODT value is common for Read and Write operation, programmed with MR41 OP[7:5]. NT ODT value cannot be changed in Read to Write or Write to Read with minimum command interval. NT ODT value must be carefully selected considering the same value is used for both Read and Write operation.

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Revision History

Rev. B– 04/2020

- Adding Important note to NT ODT simulation

Rev. A – 07/2019

- Initial release

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