Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

BETA

CompactFlash
Palladium Memory Model
User Guide

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1. General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

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2. CompactFlash Memory Model

1. Introduction

The Cadence Palladium CompactFlash Model is based on the CF+ and CompactFlash Specification Revision 6.0.

The model supports all the three basic mode functions: PC Card ATA using I/O Mode, PC Card ATA using Memory Mode and True IDE Mode.

The model is initially only available in one configuration 1024MB. Future versions will be based on the JEDEC specification once release and will cover different configurations.

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2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

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3. Features

- Support PC Card Memory interface Mode
- Support PC Card I/O interface Mode, including Primary IO Mode, Secondary IO Mode and Contiguous IO Mode
- Support True IDE interface Mode
- Support Attribute Memory Configuration Registers
- Support Ultra DMA mode in all the three interface modes
- Support Multiword DMA mode in True IDE interface mode
- Support sector buffer size setting in Ultra DMA mode
- Support three kinds of Addressing Mode, including CHS mode, LBA-28bit mode and LBA-48bit mode
- Support two kinds of Data Access Mode, including Word mode and Byte mode
- Support commands including 48-bit Address feature set commands, CFA feature set commands, Core feature set commands, Core Legacy feature set Commands, and Power management feature set commands.

The following features are NOT supported in the Palladium CompactFlash model.

- CF+ Card function is not supported
- General Purpose Log (GPL) feature set commands, Key Management feature set commands, Streaming Performance Control feature sets commands, Global Performance Control feature set commands and Security feature set commands are not supported
- Cache is not supported

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4. Configurations

The following table lists the possible configurations. Not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Capacity	No. of Cylinders	No. of Heads	No. of Sectors	Bytes of one Sector
128MB	980	8	32	512
256MB	980	16	32	512
512MB	993	16	63	512
1024MB	1986	16	63	512

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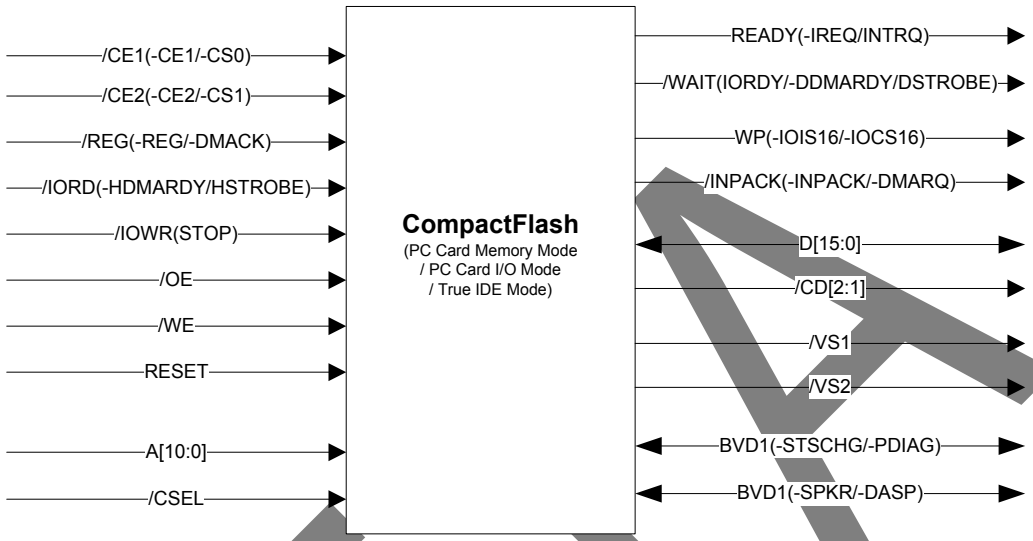
5. Model Block Diagram

There are three basic modes: PC Card ATA using I/O Mode, PC Card ATA using Memory Mode and True IDE Mode. The interface signals in the 3 modes are identical but some signal lines have different meanings in each mode.



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6. I/O Signals Description

Signal Name in Compact Flash Spec	Signal Name in Model	I/O	DESCRIPTION
A10 – A00 (PC Card Memory Mode) A10 – A00 (PC Card I/O Mode) A02 – A00 (True IDE Mode)	A10 – A00	I	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	BVD1	I/O	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol. It is not supported in this model.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	BVD2	I/O	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. This model does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present sign al in the Master/Slave handshake protocol. It is not supported in this model.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)	CD1_N CD2_N	O	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine the CompactFlash Storage Card or CF+ Card is fully inserted into its socket. Connect these pins low in this model. This signal is the same for all modes. This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	CE1_N CE2_N	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. While (-)DMACK is asserted, -CE1 and –CE2 shall be held negated and the width of the transfers shall be 16bits. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the address range select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	CSEL_N	I	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When this pin is open, this device is configured as a Slave.

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Signal Name in Compact Flash Spec	Signal Name in Model	I/O	DESCRIPTION
D15 – D00 (PC Card Memory Mode) D15 – D00 (PC Card I/O Mode) D15 – D00 (True IDE Mode)	D15 – D00	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active) -INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge -DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)	INPACK_N	O	This signal is not used in this mode. The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals. This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with (-)DMACK, i.e.,the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA IO Mode, the –DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while –DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0(-CE1) and –CS1(-CE2) shall be held negated and the width of the transfers shall be 16bits.
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active) -IORD (PC Card I/O Mode except Ultra DMA Protocol Active) -IORD (True IDE Mode - except Ultra DMA Protocol Active) -HDMARDY (All Modes – Ultra DMA Protocol DMA Read) HSTROBE (All Modes – Ultra DMA Protocol DMA Write)	IORD_N	I	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the ComapctFlash Storage Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negated –HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode except Ultra DMA Protocol Active) -IOWR (PC Card I/O Mode except Ultra DMA	IOWR_N	I	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is

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Signal Name in Compact Flash Spec	Signal Name in Model	I/O	DESCRIPTION
Protocol Active) -IOWR (True IDE Mode - except Ultra DMA Protocol Active) STOP (All Modes – Ultra DMA Protocol Active)			configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	OE_N	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	READY	O	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)	REG_N	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card, the host shall keep the –REG signal negated during the execution of any DMA Command by the device. The signal shall also be active (low) during I/O cycles when the I/O address is on the bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card, the host shall keep the –REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMACK signal, including a floating condition.
RESET (PC Card Memory Mode)	RESET	I	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the

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Signal Name in Compact Flash Spec	Signal Name in Model	I/O	DESCRIPTION
RESET (PC Card I/O Mode) -RESET (True IDE Mode)			application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the soft reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	VS1_N VS2_N	O	Voltage Sense Signals. It is not used in this model. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode except Ultra DMA Protocol Active) IORDY (True IDE Mode - except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	WAIT_N	O	The –WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	WE_N	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOCS16 (True IDE Mode)	WP	O	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O operation - When the CompactFlash Storage Card or CF+ Card is configured for I/O operation Pin 24 is used for the –I/O selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

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7. Address mapping

The array of the CompactFlash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The mapping to the internal model array in three addressing modes is as follows:

1) For CHS addressing mode:
   ARRAY_ADDR = ((C * HPC) + H) * SPT + S – 1;
   (C, H and S are the currently command operation cylinder, header and sector; the HPC is the number of headers per cylinder, and the SPT is the number of sectors per header.)

2) For LBA-28bit addressing mode:
   ARRAY_ADDR = {Device [3:0], LBA_High, LBA_Mid, LBA_Low};

3) For LBA-48bit addressing mode:
   ARRAY_ADDR = {LBA_High_pre, LBA_Mid_pre, LBA_Low_pre, LBA_High, LBA_Mid, LBA_Low};

Note: The first sector in CHS mode calls sector #1, but in LBA mode calls LBA#0.

The array name in the model hierarchy is: memcore

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8. Attribute Memory

Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The base address of the card configuration registers is 200h. The attribute memory can only be accessed in PC Card Memory mode and I/O mode, and can't be accessed in True IDE mode.

1) Configuration Option Register(Base + 00h)

Field	Type	Description
D7	RW	SRESET Soft Reset, active high
D6		LevelREQ 1: Level Mode Interrupt is selected 0: Pulse Mode is selected (default)
D5-D0		Conf5-Conf0 5'b00000: Memory Mode (default) 5'b00001: Contiguous IO Mode 5'b00010: Primary IO Mode 5'b00011: Secondary IO Mode Others: Reserved

2) Card Configuration and Status Register (Base + 02h)

Field	Type	Description
D7	R	Changed Indicates that one or both of the Pin Replacement register CReady, or CWProt bits are set to one.
D6	RW	SigChg This bit is set and reset by the host to enable and disable a state change "signal" from the Status Register
D5	RW	IOis8 The host sets this bit to a one if the CompactFlash Storage Card is to be configured in an 8 bit I/O Mode. The CompactFlash Storage Card is always configured for both 8 and 16 bit I/O, so this bit is ignored.
D4	RW	-XE This bit is set and reset by the host to disable and enable Power Level 1 commands in CF+ cards. This bit does not affect model function.
D3	RW	Audio This bit is set and reset by the host to enable and disable audio information on –SPKR when CF+ card is configured. This bit does not affect model function.
D2	RW	PwrDwn This bit indicates whether the host requests the CompactFlash Storage Card to be in the power saving or active mode. This bit does not affect model function.
D1	R	Int This bit represents the internal state of the interrupt request.
D0		Always 0

3) Pin Replacement Register (Base + 04h)

Field	Type	Description
D7-D6		Always 2'b00
D5	RW	CReady This bit is set to one when the bit RReady changes state. This bit can

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		also be written by the host.
D4	RW	CWProt This bit is set to one when the RWprot changes state. This bit may also be written by the host.
D3-D2	R	Always 2'b11
D1	RW	RReady (R) MReady (W) RReady is used to determine the internal state of the READY signal. MReady acts as a mask for writing the corresponding bit CReady
D0	RW	WProt (R) MWProt (W) WProt is always zero since the CompactFlash Storage Card does not have a Write Protect switch. MWProt acts as a mask for writing the corresponding bit CWProt.

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9. Commands Description

9.1. Task File Registers

1) Data Register (Address – 1F0h[170h]; Offset 0,8,9)
The Data Register is a 16 bit register and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. Data Register access as following:

Data Register Memory and I/O Modes	**-CE2**	**-CE1**	**A0**	**-REG**	**Offset**	**Data Bus**
Word Data Register	0	0	X	-	0,8,9	D15-D0
Even Data Register	1	0	0	-	0,8	D7-D0
Odd Data Register	1	0	1	-	9	D7-D0
Odd Data Register	0	1	X	-	8,9	D15-D8
Error/Feature Register	1	0	1	-	1,Dh	D7-D0
Error/Feature Register	0	1	X	-	1	D15-D8
Error/Feature Register	0	0	X	-	Dh	D15-D8
Data Register Ture IDE Mode	**-CS1**	**-CS0**	**A0**	**-DMACK**	**Offset**	**Data Bus**
PIO Word Data Register	1	0	0	1	0	D15-D0
DMA Word Data Register	1	1	X	0	X	D15-D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0	D7-D0

Notes: -REG signal is mode dependent. Signal shall be 0 for I/O mode and 1 for Memory Mode.

2) Error Register (Address – 1F1h[171h]; Offset 1, 0Dh Read Only)
This register contains additional information about the source of an error when an error is indicated in bit 0 of the status register.

D7	D6	D5	D4	D3	D2	D1	D0
BBK/ICRC	UNC	0	INDF	0	ABRT	0	AMNF

Notes: ICRC for UDMA CRC error will be reported; INDF for READ/WRITE address out of boundary will be reported; ABRT for Not Ready and invalid command will be reported. Other errors are not reported.

3) Feature Register (Address – 1F1[171h]; Offset 1, 0Dh Write Only)
This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. The register contains two bytes when using LBA-48bit address mode.

4) Sector Count Register (Address – 1F2h[172h]; Offset 2)
This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. The register contains two bytes when using LBA-48bit address mode.

5) LBA Low (LBA7-0) (Sector Number) Register (Address – 1F3h[173h]; Offset 3)
This register contains the starting sector number or bits7-0 of the LBA for any CompactFlash Storage Card data access for the subsequent command. When using LBA-48bit mode, the register has to be written twice to load the command's complete LBA. The current byte contains bits7-0, and the previous byte contains bits31-24 of LBA.

6) LBA Mid (LBA15-8) (Cylinder Low) Register (Address – 1F4h[174h]; Offset 4)
This register contains the low order 8bits of the starting cylinder address or bits15-8 of the LBA. When using LBA-48bit mode, the register has to be written twice to load the

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command's complete LBA. The current byte contains bits15-8, and the previous byte contains bits39-32 of LBA.

7) LBA High (LBA23-16) (Cylinder High) Register (Address – 1F5h[175h]; Offset 5)
This register contains the high order 8bits of the starting cylinder address or bits23-16 of the LBA. When using LBA-48bit mode, the register has to be written twice to load the command's complete LBA. The current byte contains bits23-16, and the previous byte contains bits47-40 of LBA.

8) Device (LBA27-24) Register (Address 1F6h[176h]; Offset 6)
The Device Register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Notes: DRV is the drive number. DRV should set to 0. Setting DRV bit to 1 is obsolete and is not supported in CompactFlash Model.

9) Status & Alternate Status Registers (Address 1F7h[177h]&3F6h[376h]; Offsets 7&Eh)
These registers return the CompactFlash Storage Card status when read by the host.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Notes: 1) RDY bit will be set to 1 when reset finished and ready to accept a command;
2) DWF bit is not supported and always return 0; DSC bit always returns 1; CORR bit always returns 0;
3) DRQ bit will be cleared by reading status register but not clear by reading alternate status register.

10) Device Control Register (Address – 3F6h[376h]; Offset Eh)
This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card.

D7	D6	D5	D4	D3	D2	D1	D0
HOB	0	0	0	0	SW Rst	-IEn	0

11) Card (Drive) Address Register (Address 3F7h[377h]; Offset Fh)
This register is provided for compatibility with the AT disk drive interface.

D7	D6	D5	D4	D3	D2	D1	D0
0	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

9.2. Task File registers address mapping

1) I/O Primary and Secondary Addressing

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data
0	1F(17)h	0	0	0	1	Error Register	Feature
0	1F(17)h	0	0	1	0	Sector Count	Sector Count
0	1F(17)h	0	0	1	1	Sector No.	Sector No.
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head
0	1F(17)h	0	1	1	1	Status	Command
0	3F(37)h	0	1	1	0	Alter Status	Device Control
0	3F(37)h	0	1	1	1	Drive Address	Reserved

2) Contiguous I/O Mapped Addressing

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-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0
0	0	0	0	0	0	Even RD Data	Even WR Data
0	0	0	0	1	1	Error Register	Feature
0	0	0	1	0	2	Sector Count	Sector Count
0	0	0	1	1	3	Sector No.	Sector No.
0	0	1	0	0	4	Cylinder Low	Cylinder Low
0	0	1	0	1	5	Cylinder High	Cylinder High
0	0	1	1	0	6	Select Card/Head	Select Card/Head
0	0	1	1	1	7	Status	Command
0	1	0	0	0	8	Dup Even RD Data	Dup Even WR Data
0	1	0	0	1	9	Dup Odd RD Data	Dup Odd WR Data
0	1	1	0	1	D	Dup Error	Dup Feature
0	1	1	1	0	E	Alt Status	Device Control
0	1	1	1	1	F	Drive Address	Reserved

3) Memory Mapped Addressing

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0
1	0	x	0	0	0	0	0	Even RD Data	Even WR Data
1	0	x	0	0	0	1	1	Error Register	Feature
1	0	x	0	0	1	0	2	Sector Count	Sector Count
1	0	x	0	0	1	1	3	Sector No.	Sector No.
1	0	x	0	1	0	0	4	Cylinder Low	Cylinder Low
1	0	x	0	1	0	1	5	Cylinder High	Cylinder High
1	0	x	0	1	1	0	6	Select Card/Head	Select Card/Head
1	0	x	0	1	1	1	7	Status	Command
1	0	x	1	0	0	0	8	Dup Even RD Data	Dup Even WR Data
1	0	x	1	0	0	1	9	Dup Odd RD Data	Dup Odd WR Data
1	0	x	1	1	0	1	D	Dup Error	Dup Feature
1	0	x	1	1	1	0	E	Alt Status	Device Control
1	0	x	1	1	1	1	F	Drive Address	Reserved
1	1	x	x	x	x	0	8	Even RD Data	Even WR Data[1]
1	1	x	x	x	x	1	9	Odd RD Data	Odd WR Data[1]

Note: Memory to Memory block move function is not supported in the CompactFlash model.

4) True IDE Mode Addressing

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit
1	1	x	x	x	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Feature	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
1	1	1	1	0	1	Alt Status	Device Control	8 bit

9.3. CF-ATA Commands

The following table lists all the commands for CompactFlash Model.

Class	COMMAND	Code	FR	LOW	MID	HIGH	D	LBA	Support
1	CFA Extended Identify Device Ext	B7h Feature0001h	Y	-	-	-	D	-	Y
1	Check Power Mode	E5h (or 98h)[1]	-	-	-	-	D	-	Y
2	Data Set Management	06h	Y	-	-	-	D	Y	N
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-	N
1	Erase Sectors	C0h	-	Y	Y	Y	Y	Y	Y
1	Flush Cache	E7h	-	-	-	-	D	-	Y
1	Flush Cache Ext	EAh	-	-	-	-	D	-	Y
2	Format Track	50h	-	Y	-	Y	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-	Y
1	Idle	E3h (or 97h)[1]	-	Y	-	-	D	-	Y

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1	Idle Immediate	E1h (or 95h)[1]	-	-	-	-	D	-	Y
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-	N
1	Key Management Structure Read	B9h Feature0-127	C	C	C	C	D C	-	N
1	Key Management Read Keying Material	B9 Feature 80	C	C	C	C	D C	-	N
2	Key Management Change Key Management Value	B9 Feature 81	C	C	C	C	D C	-	N
1	NOP	00h	-	-	-	-	D	-	Y
1	Read Buffer	E3h	-	-	-	-	D	-	Y
1	Read DMA	C8h	-	Y	Y	Y	Y	Y	Y
1	Read DMA Ext	25h	-	Y	Y	Y	D	Y	Y
1	Read Log Ext	2Fh	-	Y	Y	-	D	Y	N
1	Read Log DMA Ext	47h	-	Y	Y	-	D	Y	N
1	Read Long Sector	22h (or 23h)[1]	-	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y	Y
1	Read Multiple Ext	29h	-	Y	Y	Y	D	Y	Y
1	Read Sectors	20h (or 21h)[1]	-	Y	Y	Y	Y	Y	Y
1	Read Sectors Ext	24h	-	Y	Y	Y	D	Y	Y
1	Read Verify Sectors	40h (or 41h)[1]	-	Y	Y	Y	Y	Y	Y
1	Read Verify Sectors Ext	42h	-	Y	Y	Y	D	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-	N
1	Request Sense	03h	-	-	-	-	D	-	Y
1	Sanitize Status Ext	B4h Feature 00h	Y	-	-	-	D	-	N
1	Sanitize Crypto Scramble Ext	B4h Feature 11h	Y	Y	Y	Y	D	Y	N
1	Sanitize Block Erase Ext	B4h Feature 12h	Y	Y	Y	Y	D	Y	N
1	Sanitize Overwrite Ext	B4h Feature 14h	Y	Y	Y	Y	D	Y	N
1	Sanitize Freeze Lock Ext	B4h Feature 20h	Y	Y	Y	Y	D	Y	N
1	Security Disable Password	F6h	-	-	-	-	D	-	N
1	Security Erase Prepare	F3h	-	-	-	-	D	-	N
1	Security Erase Unit	F4h	-	-	-	-	D	-	N
1	Security Freeze Lock	F5h	-	-	-	-	D	-	N
1	Security Set Password	F1h	-	-	-	-	D	-	N
1	Security Unlock	F2h	-	-	-	-	D	-	N
1	Seek	7Xh	-	-	Y	Y	Y	Y	N
1	Set Features	EFh	Y	-	-	-	D	-	Y
1	Set Multiple Mode	C6h	-	Y	-	-	D	-	Y
1	Set Sleep Mode	E6h (or 99h)[1]	-	-	-	-	D	-	Y
1	Standby	E2h (or 96h)[1]	-	-	-	-	D	-	Y
1	Standby Immediate	E0h (or 94h)[1]	-	-	-	-	D	-	Y
1	Streaming Performance Assign	BBh Feature2h,3h	Y	Y	Y	Y	D	-	N
2	Streaming Performance Management	BBh Feauture 4h	Y	-	-	-	D	-	N
1	Streaming Performance Release	BBh Feature 8h	Y	Y	Y	Y	D	Y	N
1	Translate Sector	87h	-	Y	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-	N
2	Write Buffer	E8h	-	-	-	-	D	-	Y
2	Write DMA	CAh	-	Y	Y	Y	Y	Y	Y
2	Write DMA Ext	35h	-	Y	Y	Y	D	Y	Y
2	Write DMA FUA Ext	3Dh	-	Y	Y	Y	D	Y	Y
2	Write Log Ext	3Fh	-	Y	Y	-	D	Y	N
2	Write Log DMA Ext	57h	-	Y	Y	-	D	Y	N
2	Write Long Sector	32h (or 33h)[1]	-	-	Y	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y	Y
3	Write Multiple Ext	39h	-	Y	Y	Y	D	Y	Y
3	Write Multiple FUA Ext	CEh	-	Y	Y	Y	D	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y	Y
2	Write Sectors	30h (or 32h)[1]	-	-	Y	Y	Y	Y	Y
2	Write Sectors Ext	34h	-	Y	Y	Y	D	Y	Y
2	Write Sectors w/o Erase	38h	-	Y	Y	Y	Y	Y	Y

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3	Write Verify	3Ch	-	Y	Y	Y	Y	Y	Y

[1]The second command code in '( )' is a core legacy command.

	NOT supported in the CompactFlash Model
	Supported in the CompactFlash Model

Definitions:

- FR = Feature Register
- LOW = Sector Count Register
- MID = Sector Number Register
- HIGH = Cylinder Registers
- D = Device Register
- LBA = Logical Block Address Mode Supported
- Y – The register contains a valid parameter for this command. For Device Register Y means both the CompactFlash Storage Card and head Parameters are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data.

9.4. Commands Description

1) CFA Extended Identify Device Ext command
The content of CFA Extends Identify Device Information is not defined; and always returns 512 bytes of '0'.

2) Flush Cache and Flush Cache Ext command
The Model does not support cache and return status with RDY = 1 and DSC = 1 after issuing Flush Cache and Flush Cache Ext command and no other affections.

3) Format Track command
This command writes the desired head and cylinder of the selected drive with vendor unique data pattern. In this CompactFlash Model the data pattern is FFh.

4) Identify Device
The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration – signature for the CompactFlash Storage Card
1	07C2h	2	Default number of cylinders
2	0000h	2	Reserved
3	0010h	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	003Fh	2	Default number of sectors per track
7-8	001Eh 8BE0h	4	Number of sectors per card (Word7 = MSW, Word8 = LSW)
9	0000h	2	Obsolete
10-19	AAAA	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	AAAA	8	Firmware revision in ASCII, Big Endian Byte Order in Word
27-46	AAAA	40	Model number in ASCII (Left Justified). Big Endian Byte Order in Word
47	00FFh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0300h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field Validity

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54	07C2h	2	Current numbers of cylinders
55	0010h	2	Current numbers of heads
56	003Fh	2	Current sectors per track
57-58	8BE0h 001Eh	4	Current capacity in sectors(LBAs)(Word57 = LSW, Word58 = MSW)
59	0100h	2	Multiple sector setting
60-61	8BE0h 001Eh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Reserved
63	0104h	2	Multiword DMA transfer. In PC Card modes this value should be 0h
64	0000h	2	Advanced PIO modes supported
65	0000h	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h
66	0000h	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	0000h	2	Minimum PIO transfer cycle time without flow control
68	0000h	2	Minimum PIO transfer cycle time with IORDY flow control
69	0000h	2	Additional Supported
70-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	0000h	6	Features/command sets supported
85-87	0000h	6	Features/command sets enabled
88	0080h	2	Ultra DMA Mode Supported and Selected
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	0000h	2	Master Password revision code
93-99	0000h	14	Reserved
100-103	8BE0h 001Eh 0000h 0000h	8	Maximum user LBA for the 48-bit Address feature set
104	0000h	2	Reserved
105	0000h	2	Maximum number of 512 byte blocks of LBA range entries per the Data Set Management command
106-118	0000h	26	Reserved
119	0000h	2	Features/command sets supported
120	0000h	2	Features/command sets supported or enabled
121-127	0000h	14	Reserved
128	0000h	2	Security status
129-159	0000h	62	Vendor specific bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	CF Advanced PC Card I/O and Memory Timing Mode Capability
165	0000h	2	CF card operating temperature range
166	0000h	2	Reserved for assignment by the CFA
167	6002h	2	CFA Revision and Enhanced Features Supported
168	0000h	2	Reserved
169	0000h	2	Data Set Management support
170-254	0000h	170	Reserved
255	0000h	2	Reserved

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5) Read DMA and Write DMA command
   Before issuing DMA commands, the CompactFlash should be in DMA mode first using set feature 03h, otherwise the DMA commands are invalid.

6) Read Long Sector and Write Long Sector command

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These two commands implement same as Read one sector and Write one sector command and no 4 extra bytes defined.

7) Request Sense command
The CompactFlash Model supports the following extended error code.

Extended Error Code	Description
00h	No Error Detected
2Fh	Address Overflow
11h	Uncorrectable ECC Error
1Fh	Data Transfer Error / Aborted Command

8) Set Feature command
This command is used by the host to establish or select certain features. The CompactFlash Model supports the following feature set.

Feature	Operation
01h	Enable 8 bit data transfers
02h	Enable Write Cache. The CompactFlash Model accepts this feature value but no affection to memory.
03h	Set transfer mode based on value in Sector Count Register
81h	Disable 8 bit data transfer
82h	Disable Write Cache. The CompactFlash Model accepts this feature value but no affection to memory.

9) Translate Sector command
This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The Hot Count is not supported and always returns a value of 0.

10) Write DMA FUA Ext command
This command implements same as Write DMA Ext command.

11) Write Multiple FUA Ext command
This command implements same as Write Multiple Ext command.

12) Write Multiple without Erase command
This command implements same as Write Multiple command.

13) Write Sectors without Erase command
This command implements same as Write Sectors command.

14) Write Verify command
This command implements same as Write Sectors command.

15) Other commands
Other supported commands implement exactly same as specification.

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10. Compile and Emulation

The model is provided as protected RTL files (*.vp). The files need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64bit +sv -ua +dut+compactflash_1024MB \
    ./compactflash_1024MB.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile compactflash_1024MB.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog compactflash_1024MB.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
compactflash_1024MB
……

2)
vavlog compactflash_1024MB.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog
compactflash_1024MB.vg compactflash_1024MB
……
```

NOTE: It is common for UXE flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for UXE flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

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3. Revision History

The following table shows the revision history for this document

Date	Version	Revision
August 2013	1.0	Initial release
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name.
November 2014	1.3	Remove emulation capacity info. Update related publications list.
July 2015	1.4	Update Cadence naming on front page
September 2015	1.5	Adding Compile and Emulation section
January 2016	1.6	Update user guide for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming
January 2018	1.8	Modify header and footer
July 2018	1.9	Update for new utility library

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