Technical Note

LPDDR5 Interface

Introduction

This technical note is a general overview of LPDDR5 Interface and how it differs from LPDD4X. It provides detailed comparisons of pin types and descriptions, interface types, power mode state transitions, and DQ Rx masks.

Pin Comparison: LPDDR4X vs. LPDDR5

Table 1: Pin Comparison: LPDDR4X vs. LPDDR5

Item		LPDDR4X	LPDDR5
CKE		Supported	Not supported to reduce pin count; CS is used to exit from power-down mode or deep-sleep mode
CS		LVSTL	Dual-mode, high-speed input interface Class I synchronous mode used during normal operation Class II asynchronous mode used during power-down mode or deep-sleep mode
Control clock	CA circuit	CK_t/CK_c (2133 MHz MAX)	CK_t/CK_c (low-frequency signal, 800 MHz MAX)
	Data circuit	CK_t/CK_c (2133 MHz MAX)	WCK_t/WCK_c (high-frequency signal, 3200 MHz MAX) WCK:CK ratio is 2:1 or 4:1
CA		LVSTL	LVSTL
Data strobe	Write	Bidirectional DQS (DQS_t, DQS_c)	WCK (WCK_t, WCK_c)
	Read		RDQS (RDQS_t, RDQS_c)
DQ,DMI		LVSTL_0.6	LVSTL _0.5
Reset_n		LVCMOS	LVCMOS

LPDDR5 Pin Descriptions

The device contains one channel per die. A channel is defined as clocking, command, and address with associated data lanes.

Table 2: LPDDR5 Pin Descriptions

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All DDR command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and the second crossing point is the falling (rising) edge of CK_t (CK_c). For SDR inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS	Input	**Chip select:** CS is part of the command code and is sampled on the rising (falling) edge of CK_t (CK_c), unless the device is in power-down or deep-sleep mode and becomes an asynchronous signal.
CA[6:0]	Input	**Command/address inputs:** CA signals provide the command and address input according to the Command Truth Table.
WCK[1:0]_t, WCK[1:0]_c	Input	**Data clocks:** WCK_t and WCK_c are differential clocks used for write data capture and read data output.
RESET_n	Input	**RESET:** When asserted LOW, RESET_n resets the die. Reset is an asynchronous signal.
DQ[15:0]	I/O	**Data input/output:** Bidirectional data bus.
DMI[1:0]	I/O	**Data mask inversion:** Data mask inversion (DMI) serves multiple functions, such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
RDQS[1:0]_t, RDQS[1:0]_c	RDQS[1:0]_t:I/O RDQS[1:0]_c: Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled.
ZQ	Reference	**ZQ:** ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. ZQ is connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}	Supply	**Power supplies:** V_{DD1}: 1.8V; V_{DD2H}: 1.05V; V_{DD2L}: 0.9V; V_{DDQ}: 0.5V or 0.3V. V_{DD2L} (0.9V) and V_{DDQ} (0.3V) are used during DVFS mode enabled.
V_{SS}	GND	**Ground reference:** Power supply ground reference.

Interface Types

Table 3: Interface Description

Symbol	Interface Type	ODT Support[1]	V_{REF}	UI	Description
CK_t, CK_c	LVSTL	Available (RZQ/1 - RZQ/6) MR11OP[6:4]	V_{REFCA} Used as VIX_ck reference point during differential mode and as timing reference point during single-ended mode	N/A	Rx spec similar to LPDDR4X but with slower clock frequency (800 MHz MAX)
CS	Dual-mode interface	Available during synchronous mode (RZQ/3 only) MR17OP[4]	V_{DD2H}/3 (fixed V_{REF})	1UI = 1.0 x^{t}CK(AVG)	Synchronous mode for command input during normal operation; asynchronous mode during power-down mode or deep-sleep mode **CS synchronous mode spec:** Similar to LPDDR4X but with hexagonal Rx mask **CS asynchronous mode spec:** V_{IH} = 550 mV/V_{IL} = 130mV To exit power-down mode or deep-sleep mode, CS pulse must be applied; see power mode state transition section
CA	LVSTL	Available (RZQ/1 - RZQ/6) MR11OP[6:4]	V_{REFCA}	1UI = 0.5 x ^{t}CK(AVG)	LVSTL input. Rx spec similar to LPDDR4X but with a hexagonal Rx mask
DQ,DMI	LVSTL	Available (RZQ/1 - RZQ/6) MR11OP[2:0]	V_{REFDQ}	1UI = 0.5 x ^{t}WCK(AVG)	LVSTL I/O. Interface spec similar to LPDDR4X but with a hexagonal Rx mask
WCK_t, WCK_c	LVSTL	Available (RZQ/1 - RZQ/6) MR18OP[2:0]	V_{REFDQ} Used as VIX_wck reference point during differential mode and as timing reference point during single-ended mode	N/A	LVSTL. Rx spec similar to LPDDR4X DQS during writes
RDQS_t, RDQS_c	LVSTL	Available for RDQS_t parity mode (RZQ/1 - RZQ/6) MR11OP[2:0]	V_{REFDQ}	1UI = 0.5 x ^{t}WCK(AVG)	LVSTL I/O. Interface spec similar to LPDDR4X but with a hexagonal Rx mask
RESET_n	LVCMOS	No	N/A	N/A	

Note: 1. V_{REFCA} is commonly used between CK_t/CK_c and CA. Ensure the ODT setting achieves similar signal swing for CK_t/CK_c and CA; otherwise, a VIX_CK violation may occur.

Power Mode State Transitions with CS Pin

LPDDR5 does not have a CKE signal. To enter power-saving mode (power-down or deep-sleep) use the command code below with the PD or the DSM option asserted.

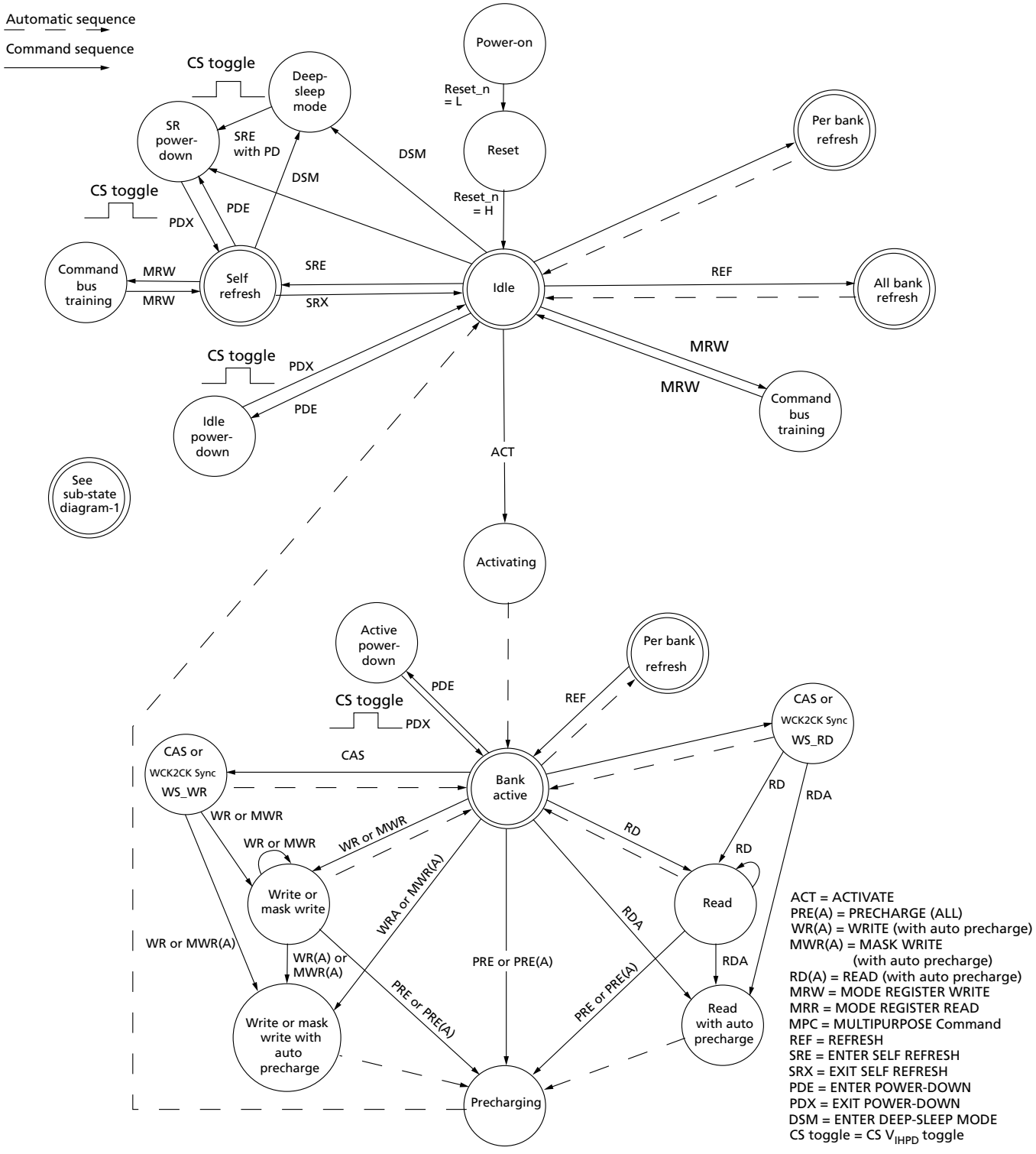
If neither the PD nor the DSM option is asserted, the interface is not disabled, and the SRX command code is used to exit self refresh.

Table 4: Command Truth Table for Power-Saving Mode

Command	SDR CMD Pin CS	DDR COMMAND PINS							CK Edge
		CA0	CA1	CA2	CA3	CA4	CA5	CA6	
POWER-DOWN ENTRY (PDE)	H	L	L	L	L	L	L	H	R1
	L	X	X	X	X	X	X	X	R2
SELF REFRESH ENTRY (SRE)	H	L	L	L	H	L	H	H	R1
	X	V	V	V	V	V	DSM	PD	F1
SELF REFRESH EXIT (SRX)	H	L	L	L	H	L	H	L	R1
	X	V	V	V	V	V	V	V	F1

When the device is in power-down mode or deep-sleep mode, the CS interface is switched from synchronous mode to asynchronous mode. The CS toggle is used to exit from power-down mode or deep-sleep mode. Note the CS toggle pulse in the Simplified State Diagram below.

Figure 1: Simplified State Diagram



LPDDR4 Rx Masks vs. LPDDR5 Rx Masks

This section uses a DQ receiver (Rx) example to illustrate the difference between the LPDDR4 and LPDDR5 Rx specification. The CA Rx/CS Rx concept is similar.

LPDDR4 DQ Rx Mask and Single Pulse Definition

The LPDDR4 DQ Rx mask is defined as the rectangular mask shown below. The mask (vDIVW, TdIVW_total) defines the area that must not be encroached on by the input signal in order for the DQ input receiver to successfully capture an input signal.

Figure 2: LPDDR4 DQ Rectangular Rx Mask

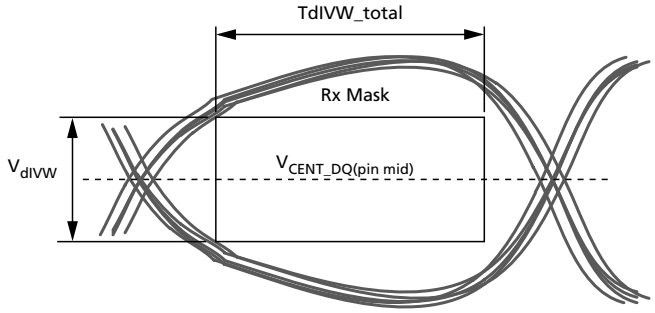
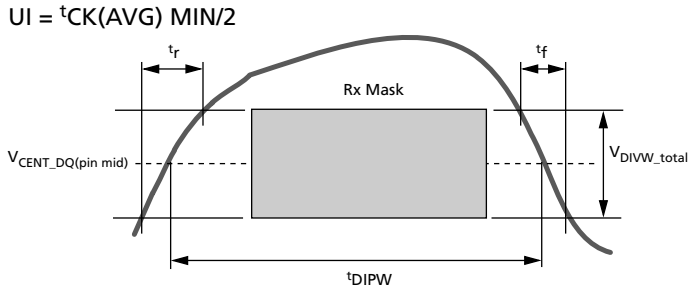
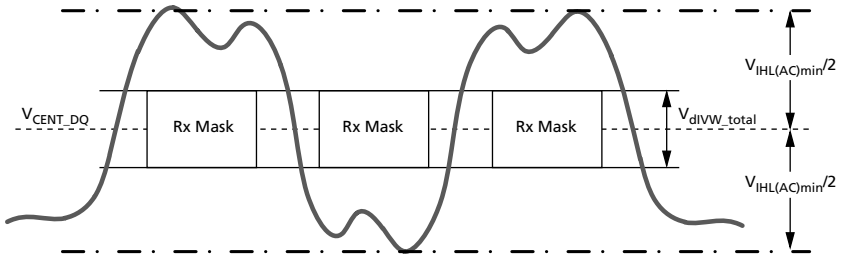


Figure 3: LPDDR4 DQ Rx Single Pulse Definition (^{t}DIPW and SRIN_dIVW)



Note: 1. SRIN_dIVW = V_{dIVW_total}/(^{t}r or ^{t}f) signal must be monotonic within ^{t}r and ^{t}f range.

Figure 4: LPDDR4 DQ Rx Single Pulse Definition ($V_{IHL(AC)}$)



LPDDR5 DQ Rx Mask and Single Pulse Definition

The LPDDR5 DQ Rx mask is defined as the hexagonal mask shown below. The mask (vDIVW, ^{t}DIVW1, ^{t}DIVW2) defines the area that the must not be encroached on by the input signal in order for the DQ input receiver to successfully capture an input signal.

Figure 5: LPDDR5 DQ Hexagonal Rx Mask

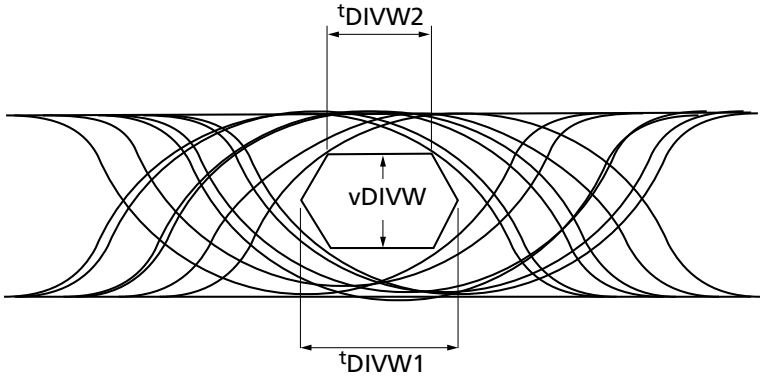
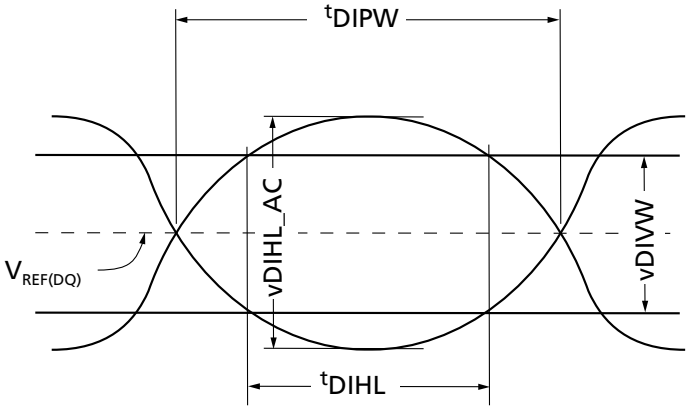


Figure 6: DQ Rx Single Pulse Definition



Notes:
1. Single pulse includes any cycle of pulse.
2. $V_{REF(DQ)}$ is a calculated value based on V_{DDQ} and MR14/MR15.

Revision History

Rev. A – 04/19

- Initial release

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