地 平 线
Horizon Robotics

Journey 2
LPDDR4 Design Check List

Rev. 1.0

January 19 2021

Important Notice and Disclaimer

Information in this document is provided solely to enable system and software implementers to use Horizon products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

All statements, information and recommendations in this document are provided "AS IS". Horizon makes no warranty, representation or guarantee of any kind, express or implied, regarding the merchantability, fitness or suitability of its products for any particular purpose, and non-infringement of any third party intellectual property rights, nor does Horizon assume any liability arising out of the application or use of any product, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

"Typical" parameters that may be provided in Horizon datasheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Buyers and others who are developing systems that incorporate Horizon products (collectively, "Users") understand and agree that Users shall remain responsible for using independent analysis, evaluation and judgment in designing their applications and that Users have full and exclusive responsibility to assure the safety of Users' applications and compliance of their applications (and of all Horizon products used in or for Users' applications) with all applicable regulations, laws and other applicable requirements.

User agrees to fully indemnify Horizon and its representatives against any claims, damages, costs, losses and/or liabilities arising out of User's unauthorized application of Horizon products and non-compliance with any terms of this notice.

Horizon Robotics, Inc.

https://www.horizon.ai

Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
1.0	2021/01/19	Initial release

Contents

1 Scope

The document is intended to provide necessary points which needs to be checked during the Journey2 LPDDR4 schematic design, PCB layout design and PCB manufacturing.

Any compromise should be carefully evaluated, otherwise the customer design may have high risk to degrade the LPDDR4 data rate.

2 Schematic Checklist

Item	Description	Y/N
1	Current output capability of power supply to J2 VDDQ and LPDDR4 VDDQ&VDD2 should be > 2.5A	
2	BP_ZN of J2 should be pulled down to VSS with a 240Ω ± 1% resistor	
3	The value of De-coupling capacitors for J2 VDDQ should follow reference design, and the capacitors should be placed as close as possible to the J2 VDDQ pins. Place on the back side of the J2 is highly preferred for smaller value capacitors.	
4	The value of De-coupling capacitors for J2 VDD_DDR should follow reference design, and the capacitors should be placed as close as possible to the J2 VDD_DDR pins. Place on the back side of the J2 is highly preferred for smaller value capacitors.	

3 PCB Layout Checklist

Item	Description	Y/N
1	The PCB stack up should follow reference design, 6-layers, 8-layers, 10-layers PCB stack up are recommended.	
2	The LPPDR4 signal trace length should be controlled to meet the requirements mentioned in J2 HW Design Guide V1.2 section 1.1.3.1.	
3	The PCB trace impedance should be strictly controlled. Refer to the J2 HW Design Guide V1.2 section 1.1.3.1.	
4	The decoupling capacitors of J2 VDDQ should be placed on the back side of J2.	
5	The decoupling capacitors of J2 VDD_DDR should be placed on the back side of J2.	

4 Manufacturing Checklist

Any Impedance deviation caused by the manufacturing process should be carefully reviewed.

Item	Description	Y/N
1	Requirements on Impedance of DQ, DM and DQS should meet target	
2	Requirements on Impedance of CA should meet target	
3	Requirements on Impedance of CA should meet target	
4	Requirements on Impedance of CLK_T/C should meet target	
Note: Refer to HW Design Guide V1.2 Section 1.1.3.1 for the trace impedance requirements		