Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

PSRAM and UtRAM
Palladium Memory Models
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

PSRAM and UtRAM Palladium Memory Models

1. Introduction

The Cadence Palladium PSRAM and UtRAM Models are based on data sheet specifications of the following devices:

- Numonyx StrataFlash Cellular Memory with Synchronous PSRAM
- Samsung UtRAM2
- Samsung UtRAM
- AP Memory Advanced PSRAM
- AP Memory OPIDDR PSRAM
- AP Memory DDR Octal SPI PSRAM

The table below indicates available part numbers and their respective revision levels and datasheets.

Please note that the PSRAM (Pseudo SRAM) is part of the multi-die Cellular Memory device. Since the PSRAM is not a standalone device the model numbers listed below are based on Cellular Memory part numbers. The PSRAM and UtRAM2 are based on the CellularRAM specification, UtRAM is based on Samsung's Uni-Transistor RAM specification.

The models are available in several configurations with model sizes to match real devices manufactured by the following vendor: Numonyx, Samsung, and AP Memory.

Currently only a few different sizes are available, please consult the memory model catalog for the current available list.

Table 1: Datasheet and Revision Level References

Part Number	Rev.	Datasheet Date	Reference Datasheet
Numonyx			
pf38f3040m0y3de	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f3040m0y0qe	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f3050m0y3de	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f4050m0y3ce	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f5060m0y3de	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f5060m0y3ce	034	Mar 2009	M18-x16C-SyncPS_DS.pdf

Part Number	Rev.	Datasheet Date	Reference Datasheet
pf38f5070m0y3de	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
pf38f6070m0y1ce	034	Mar 2009	M18-x16C-SyncPS_DS.pdf
Samsung			
k1c3216bkf	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c3216bff	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c6416bkf	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c6416bff	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c2816bkc	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c2816bfc	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1c5616bkb	1.0	Apr 2010	516977ds_k1c5616bkb_rev10.pdf
k1b1616b2b	0.1	Jan 2007	k1b1616b2b_rev01.pdf
k1b3216bdd	1.0	Apr 2005	k1b3216bdd_rev10.pdf
k1b6416b6c	1.0	Jan 2005	k1b6416b6c_rev10.pdf
k1b2816b2a	1.0	Mar 2007	k1b2816b2a10.pdf
k1b5616b2m	1.0	May 2006	K1B5616B2M.pdf
AP Memory			
aps3216h	10	2015-12-21	10-C6-0001-10 AP Memory AP-ADMUX Advanced PSRAM.pdf
aps6416f	10	2015-12-21	10-C6-0001-10 AP Memory AP-ADMUX Advanced PSRAM.pdf
aps12816g	10	2015-12-21	10-C6-0001-10 AP Memory AP-ADMUX Advanced PSRAM.pdf
aps25616g	10	2015-12-21	10-C6-0001-10 AP Memory AP-ADMUX Advanced PSRAM.pdf
aps1608k	1.5	2016-06-24	APM_APS3208K-OKUx_OPIDDR_PSRAM_Datasheet_v1.5.pdf
aps3208k	1.5	2016-06-24	APM_APS3208K-OKUx_OPIDDR_PSRAM_Datasheet_v1.5.pdf
aps6408k	1.5	2016-06-24	APM_APS3208K-OKUx_OPIDDR_PSRAM_Datasheet_v1.5.pdf
aps12808k	1.5	2016-06-24	APM_APS3208K-OKUx_OPIDDR_PSRAM_Datasheet_v1.5.pdf

Part Number	Rev.	Datasheet Date	Reference Datasheet
aps1608l	2.6	2018-04-26	APM-APS6408L-OBx_Octal-SPI_PSRAM Datasheet_v2.6.pdf
aps3208l	2.6	2018-04-26	APM-APS6408L-OBx_Octal-SPI_PSRAM Datasheet_v2.6.pdf
aps6408l	2.6	2018-04-26	APM-APS6408L-OBx_Octal-SPI_PSRAM Datasheet_v2.6.pdf
aps12808l	2.6	2018-04-26	APM-APS6408L-OBx_Octal-SPI_PSRAM Datasheet_v2.6.pdf
aps25608l	2.6	2018-04-26	APM-APS6408L-OBx_Octal-SPI_PSRAM Datasheet_v2.6.pdf

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations

The following table lists the configurations specified in the data sheets listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Model number	Density	I/O interface	I/O width	Type	Vendor
pf38f3040m0y3de	32Mb	AD-Mux	x16	PSRAM	Numonyx
pf38f3040m0y0qe	32Mb	Non-Mux	x16	PSRAM	Numonyx
pf38f3050m0y3de	64Mb	AD-Mux	x16	PSRAM	Numonyx
pf38f4050m0y3ce	64Mb	Non-Mux	x16	PSRAM	Numonyx
pf38f5060m0y3de	128Mb	AD-Mux	x16	PSRAM	Numonyx
pf38f5060m0y3ce	128Mb	Non-Mux	x16	PSRAM	Numonyx
pf38f5070m0y3de	256Mb	AD-Mux	x16	PSRAM	Numonyx
pf38f6070m0y1ce	256Mb	Non-Mux	x16	PSRAM	Numonyx
k1c3216bkf	32Mb	AD-Mux	x16	UtRAM2	Samsung
k1c3216bff	32Mb	Non-Mux	x16	UtRAM2	Samsung
k1c6416bkf	64Mb	AD-Mux	x16	UtRAM2	Samsung
k1c6416bff	64Mb	Non-Mux	x16	UtRAM2	Samsung
k1c2816bkc	128Mb	AD-Mux	x16	UtRAM2	Samsung
k1c2816bfc	128Mb	Non-Mux	x16	UtRAM2	Samsung
k1c5616bkb	256Mb	AD-Mux	x16	UtRAM2	Samsung
k1b1616b2b	16Mb	Non-Mux	x16	UtRAM	Samsung
k1b3216bdd	32Mb	Non-Mux	x16	UtRAM	Samsung
k1b6416b6c	64Mb	Non-Mux	x16	UtRAM	Samsung
k1b2816b2a	128Mb	Non-Mux	x16	UtRAM	Samsung
k1b5616b2m	256Mb	Non-Mux	x16	UtRAM	Samsung
aps3216h	32Mb	AD-Mux	x16	Advanced PSRAM	AP Memory

aps6416f	64Mb	AD-Mux	x16	Advanced PSRAM	AP Memory
aps12816g	128Mb	AD-Mux	x16	Advanced PSRAM	AP Memory
aps25616g	256Mb	AD-Mux	x16	Advanced PSRAM	AP Memory
aps1608k *	16Mb	AD-Mux	x8	OPIDDR PSRAM	AP Memory
aps3208k *	32Mb	AD-Mux	x8	OPIDDR PSRAM	AP Memory
aps6408k *	64Mb	AD-Mux	x8	OPIDDR PSRAM	AP Memory
aps12808k *	128Mb	AD-Mux	x8	OPIDDR PSRAM	AP Memory
aps1608l * ^	16Mb	AD-Mux	x8	DDR Octal SPI PSRAM	AP Memory
aps3208l * ^	32Mb	AD-Mux	x8	DDR Octal SPI PSRAM	AP Memory
aps6408l * ^	64Mb	AD-Mux	x8	DDR Octal SPI PSRAM	AP Memory
aps12808l * ^	128Mb	AD-Mux	x8	DDR Octal SPI PSRAM	AP Memory
aps25608l * ^	256Mb	AD-Mux	x8	DDR Octal SPI PSRAM	AP Memory

* Please contact Cadence emulation support team or MMP product team to arrange for use of these models. These models are not in the MMP release as they require additional permission.

^ BETA model: This model is only available at the IR (BETA) level. This model is not in the MMP release as it requires a BETA arrangement.

4. Parameters

The following table provides details on the user adjustable parameters for the Palladium Advanced PSRAM Memory Model. These parameters may be modified when instantiating the model.

User Adjustable Parameter	Default Value	Description
addr_bits	21 to 24	Width of address bus
data_bits	16	Width of data bus
didv	Model specific	DIDR value

The following table provides details on the user adjustable parameters for the Palladium OPIDDR PSRAM Memory Model. These parameters may be modified when instantiating the model.

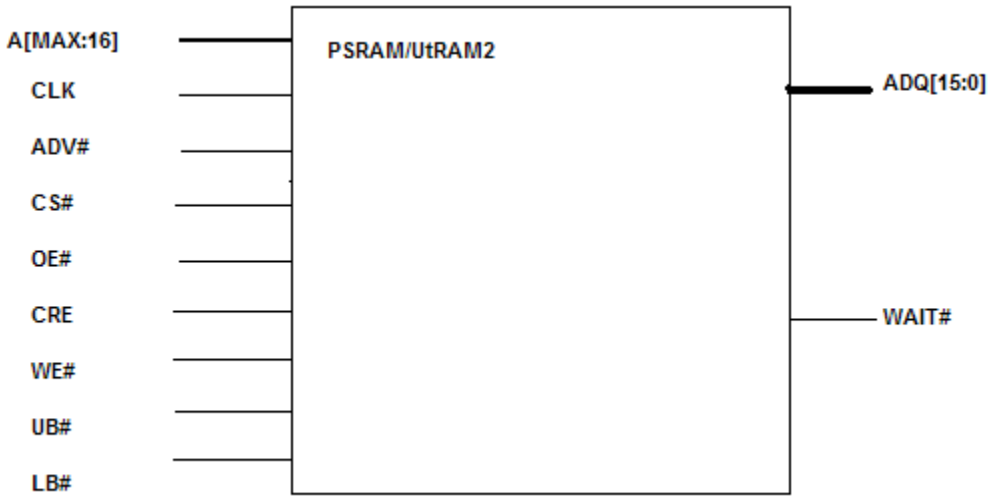
User Adjustable Parameter	Default Value	Description

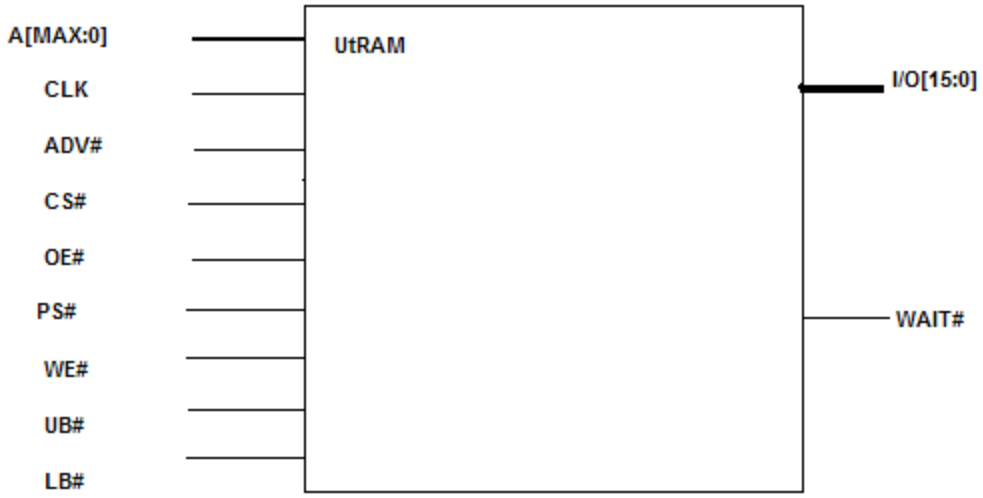
addr_bits	21 to 24	Width of address bus
data_bits	8	Width of data bus
mode_reg0	8'h13	Mode Register 0
mode_reg1	8'h0d or 8'h2d	Mode Register 1
mode_reg2	8'hc9	Mode Register 2
mode_reg4	8'h00	Mode Register 4

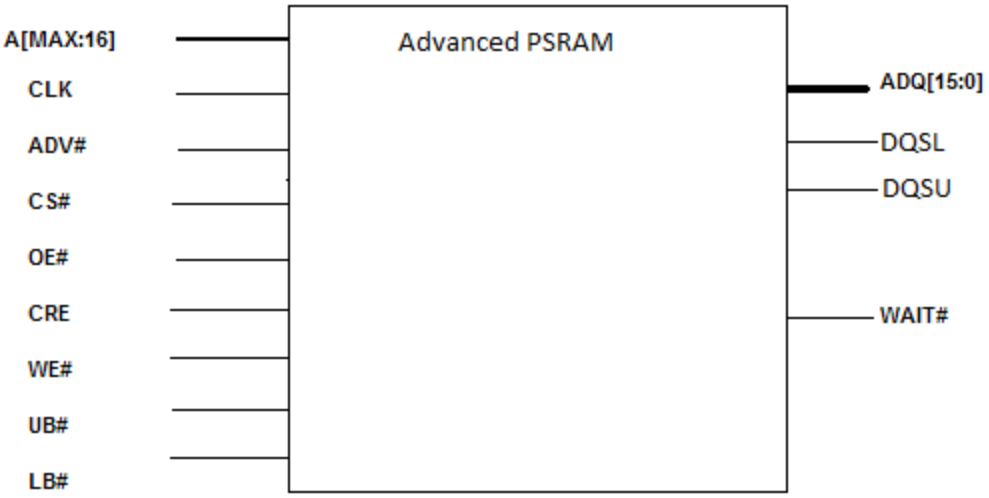
The following table provides details on the user adjustable parameters for the Palladium DDR Octal SPI PSRAM Memory Model. These parameters may be modified when instantiating the model.

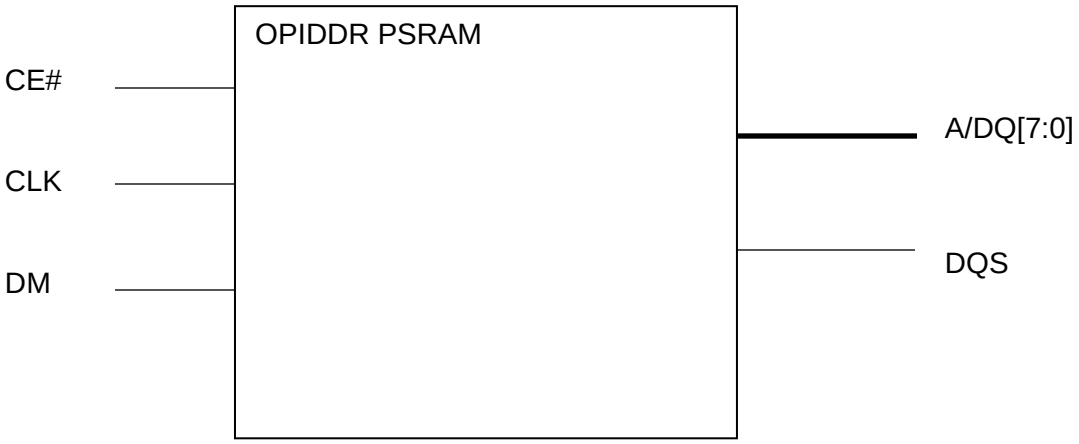
User Adjustable Parameter	Default Value	Description
addr_bits	21 to 25	Width of address bus
data_bits	8	Width of data bus
mode_reg0	8'h09	Mode Register 0
mode_reg1	8'h8d	Mode Register 1
mode_reg2	8'h91 (32Mb density)	Mode Register 2
mode_reg3	8'h00	Mode Register 3
mode_reg4	8'h40	Mode Register 4
mode_reg6	8'h00	Mode Register 6
mode_reg8	8'h05	Mode Register 8

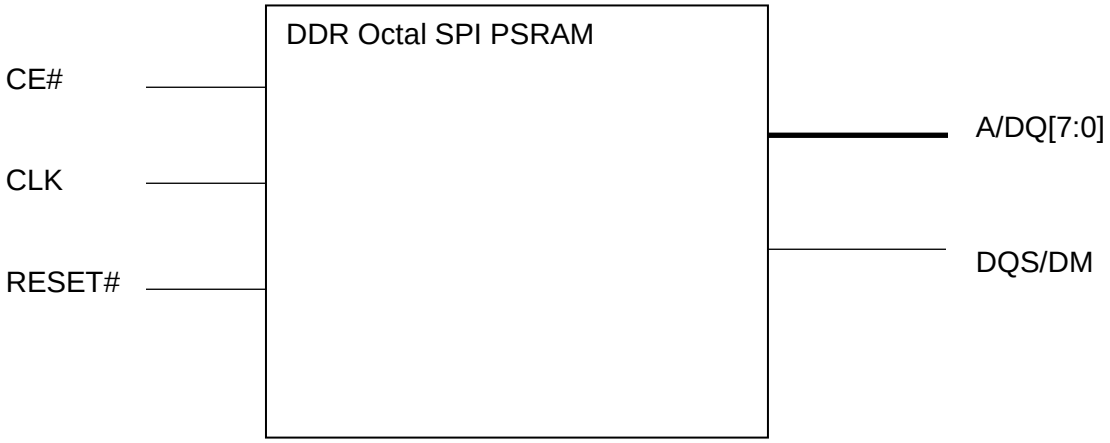
5. Model Logic Diagram











6. Model Pin Description

Pin name	Direction	Description
A/DQ[15:0]	Inout	Address/DQ bus [15:0]
A[max:16]	Input	Address [max:16]
LB#	Input	Lower byte select, active low.
UB#	Input	Upper byte select, active low.
CE#	Input	Chip select, active low.
WE#	Input	Write enable, active low.
ADV#	Input	Address-Data-Valid, active low.
CLK	Input	Clock.
DQSL	Inout	DQ sample for lower byte.
DQSU	Inout	DQ sample for upper byte.
WAIT	Output	Wait signal indicating the cycle's data is valid.
CRE	Input	Control register select.
OPIDDR PSRAM		
A/DQ[7:0]	Inout	Address/DQ bus [7:0]
DM	Input	Data mask, active high. DM=1 means "do not write".
CE#	Input	Chip select, active low.
CLK	Input	Clock.
DQS	Inout	DQ strobe.
DDR Octal SPI PSRAM		
A/DQ[7:0]	inout	Address/DQ bus [7:0]
DQS/DM	Inout	DQ strobe during read, Data mask during write. DM=1 means "do not write".
CE#	Input	Chip select, active low.
CLK	Input	Clock.
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.

7. Instantiation examples

```
aps3216h u1 (
        .Dq(DQ),
        .Waitpin(waitpin),
        .Clk(clk),
        .Uaddr(addr[addr_bits-1:data_bits]),
        .Ce_n(ce_n),
        .We_n(we_n),
        .Adv_n(adv_n),
        .Oe_n(oe_n),
        .Cre(cre),
        .Dqsl(Dqsl),
        .Dqsu(Dqsu),
        .Lb_n(lb_n),
        .Ub_n(ub_n));
```

```
aps3208k u1 (
        .Adq(dq),
        .Clk(clk),
        .Dm(dm),
        .Ce_n(ce_n),
        .Dqs(dqs));


aps3208l u1 (
        .Adq(dq),
        .Clk(clk),
        .Dqsdm(dqsdm),
        .Ce_n(ce_n),
        .Reset_n(rst_n));
```

8. Address Mapping

The array of the PSRAM and UtRAM models is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The direct mapping of address bus to the internal model array for AD-Mux models is as follows:

ARRAY_ADDR = {A[Max:16],ADQ[15:0]}

For Non-Mux models:

ARRAY_ADDR = {A}

For OPIDDR models:

ARRAY_ADDR = {A2,A1,A0} where A2, A1, A0 are ADQ inputs during address cycles.

For DDR Octal SPI models:

ARRAY_ADDR = {A3,A2,A1,A0} where A3, A2, A1, A0 are ADQ inputs during address cycles.

9. UtRAM and UtRAM2 Differences

While PSRAM and UtRAM2 are similar there are many differences between UtRAM and UtRAM2 devices. For example device operation is controlled by a Mode register in UtRAM but UtRAM2 has a Bus Configuration register instead. Setting the Mode register in UtRAM can be done using the active low PS# pin. Setting the Bus Configuration register in UtRAM2 can be

done using the active high CRE pin. While these registers can also be accessed by software using a unique sequence of read and write commands the sequences are different between UtRAM and UtRAM2. Also there are three modes of sync/async read/write operations in UtRAM but only two in UtRAM2. Here are the bit definitions of the Mode Register in the UtRAM:

A18	A17~A16	A15~A14	A13	A12	A11~A9	A8	A7~A5	A4	A3	A2	A1~A0
IL	DS	MS	WP	Wrap	Latency	WC	BL	DPD	PAR	PARA	PARS

Here are the bit definitions of the Bus Configuration Register in the UtRAM2 and PSRAM:

A19~A8	ADQ15	ADQ14	ADQ13~ADQ11	ADQ10	ADQ8	ADQ5~ADQ4	ADQ3	ADQ2~ADQ0
RS	OM	IL	LC	WP	WC	DS	BW	BL

The UtRAM2 and PSRAM have a separate Refresh Configuration Register for Partial Array Refresh (PAR) settings. The above tables are only used to illustrate the difference in bit definitions of the registers. Please see data sheets for more details on the functions defined by the bits.

10. ID Operations

10.1. PSRAM and UtRAM

PSRAM and UtRAM do not support ID operations

10.2. UtRAM2 and Advanced PSRAM DIDR

The Device Identification Register is a read-only register and can be read using CRE pin or software access.

11. Features

The following table shows a list of features for PSRAM, Advanced PSRAM, OPIDDR, PSRAM, and DDR Octal SPI PSRAM.

FEATURE	SUPPORT			
COMMANDS	**PSRAM/UtRAM**	**Advanced PSRAM**	**OPIDDR PSRAM**	**DDR Octal SPI PSRAM**
Asynchronous Mode				
Read	Yes	Yes	No	No
Write	Yes	Yes	No	No
Configuration Register Read	Yes	Yes	No	No
Configuration Register Write	Yes	Yes	No	No
Register Software Access	Yes	Yes	No	No
Device ID Register Read	Yes	Yes	No	No
Page Mode Read	Yes (supported by Non-ADMUX models)	No (Advanced PSRAM models are ADMUX)	No	No
Burst Mode (SDR)				
Async Read	Yes	Yes	No	No
Async Write	Yes	Yes	No	No
Burst Read	Yes	Yes	No	No
Burst Write	Yes	Yes	No	No
Burst continue	Yes	Yes	No	No
Burst suspend	Yes	Yes	No	No
Configuration Register Read	Yes	Yes	No	No
Configuration Register Write	Yes	Yes	No	No
Synchronous Mode (DDR)				
Read	No	Yes	Yes	Yes
Write	No	Yes	Yes	Yes
Row Boundary Crossing Latency	No	Yes	No	No
Mode Register Read	No	No	Yes	Yes
Mode Register Write	No	No	Yes	Yes
16 Byte Wrap	No	No	No	Yes
32 Byte Wrap	No	No	No	Yes
64 Byte Wrap	No	No	No	Yes
1K Byte Wrap	No	No	Yes	Yes
16 Byte Hybrid Wrap	No	No	No	Yes
32 Byte Hybrid Wrap	No	No	No	Yes
64 Byte Hybrid Wrap	No	No	No	Yes
Linear Burst Command	No	No	No	Yes
Half Sleep	No	No	No	Yes
Deep Power Down	No	No	No	Yes
Global Reset Command	No	No	No	Yes

12. Initialization Sequence

The PSRAM and UtRAM model requires that the memory controller follows the initialization sequence as documented in the specification. The sequence basically entails the following steps:

1. For UtRAM drive CS# and PS# high. For UtRAM2 and PSRAM drive CS# high and CRE low.
2. Drive CS# low.
3. The model is now initialized in Asynchronous mode and ready for normal operation.

The OPIDDR PSRAM requires the following initialization sequence:

1. Drive CE# high and CLK low.
2. Write at least 4 bytes to array.
3. Issue at least 4 NOPs (CE# high and CLK toggling).
4. Write at least 4 bytes to array.
5. Issue at least 4 NOPs.
6. Write to Mode Register 0.
7. Issue at least 4 NOPs.
8. Model ready for normal operation.

The DDR Octal SPI PSRAM requires the following initialization sequence:

1. Drive CE# high and CLK low.
2. Drive RESET# low then high, or issue Global Reset command.
3. Model ready for normal operation.

The model requires that these steps are performed in the correct sequence in order to complete initialization. The model may not respond correctly to any others commands unless this sequence is completed.

13. Model Size

Since the PSRAM and UtRAM devices listed in this user guide are in the Mbits range in size the models implement the full memory size without any size reduction at this time.

14. Limitations

1. Refresh and Strength related commands are not supported.
2. Page mode is not supported in AD-Mux I/O interface.
3. Model does not check illegal sequence of command cycles.

15. Known Problems

1. Model may fail in simulation mode when using IES13.2 or later.

16. Compilation and Synthesis examples

Shown below are some simple commands for compiling the standard Advanced PSRAM models in IXCOM flow and ICE flow.

```
ixcom -64bit +sv -ua +dut+aps3216h \
      ../tb/tb.v \
      ../src/aps3216h.vp \
      -incdir ../../../utils/cdn_mmp_utils/sv \
      ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
      ……

xeDebug -64 --ncsim \
   -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
     -input auto_xedebug.tcl
```

ICE flow synthesis commands:

```
vavlog ../src/aps3216h.vp

vaelab –keepRtlSymbol –keepAllFlipFlop –outputVlog aps3216h.vgp aps3216h
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

17. Preloading Memory Array

The path to memory array can be found in dbFiles/*mpart file after compilation. Shown below is an xeDebug preload example:

```
memory -load %readmemh tb_top.u1.mem -file mem.dat
```

18. Reference Waveform

A waveform showing various operations is available in the release under the golden_waveform directory. It may be useful to have a look at this waveform when using the model for the first time.

19. Debugging

- For issues that may not be PSRAM specific please review the *Memory Model Portfolio FAQ for All Models User Guide.*

- **Debug Display:** Debug messaging can be enabled with Advanced PSRAM model. Please refer to the *MMP_Debug_Display User Guide* under <release_dir>/docs directory for more details.

- **Manual Configuring of OPIDDR and DDR Octal SPI Model Families**

  These MMP models support manual configuration by accompanying the model mode register or configuration register declarations with synthesis directives, such as keep_net directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing. For a general description of this support please see the user guide in the MMP release with path and filename *docs/MMP_FAQ_for_All_Models.pdf*.

  While MMP strongly recommends following protocol based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments.

  The following table lists the internal register path and naming along with the specification or datasheet naming for model mode registers or configuration registers that are accompanied by keep_net synthesis directives in support of such manual configuration. ONLY writeable configuration registers or fields are supported thusly. Please read the relevant datasheet for details about individual register behavior and mapping to fields.

Table: Writeable Mode Register / Configuration Register Info

Hierarchical RTL Naming for Writeable Configuration Related Registers & Signals	Specification or Vendor Datasheet Naming for Configuration Related Registers	Access
OPIDDR PSRAM		
<model_name>.MR0	MR0	RW
<model_name>.MR1	MR1	R
<model_name>.MR2	MR2	R
<model_name>.MR4	MR4	RW
DDR Octal SPI PSRAM		
<model_name>.MR0	MR0	RW

<model_name>.MR1	MR1	R
<model_name>.MR2	MR2	R
<model_name>.MR3	MR3	R
<model_name>.MR4	MR4	RW
<model_name>.MR6	MR6	W
<model_name>.MR8	MR8	RW

Note: These models do not have init_done signal for runtime forcing.

Revision History

The following table shows the revision history for this document

Date	Version	Revision
May 2011	1.0	Initial version
June 2011	1.1	Updated with “Related Documents” information
July 2014	1.2	Repaired doc title property. Added revision history. Updated legal.
September 2014	1.3	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.4	Remove emulation capacity info.
March 2015	1.5	Update related publications list.
July 2015	1.6	Update Cadence naming on front page
September 2015	1.7	Added known problems section.
January 2016	1.8	Update for Palladium-Z1 and VXE
May 2016	1.9	Added Advanced PSRAM.
July 2016	2.0	Added RBX and Software Access support for Advanced PSRAM.
September 2016	2.1	Added OPIDDR PSRAM.
November 2016	2.2	Removed BETA notations for ADMUX PSRAM
May 2017	2.3	Removed Beta notations for OPIDDR PSRAM
January 2018	2.4	Modify header and footer
June 2018	2.5	Add Manual Configuring description in Debugging section
July 2018	2.6	Add DDR Octal DDR PSRAM models.
July 2018	2.7	Update for new utility library