Technical Note

LPDDR5 Training

Introduction

This technical note provides a general overview of LPDDR5 SDRAM training, which is used to help achieve reliable I/O operation.

LPDDR5 Training Features

During the power-up and initialization sequences of LPDDR5 devices, CA bus and DQ bus I/O operation can be adjusted (or trained) for the many available frequencies using the features described in the following table.

Table 1: LPDDR5 Training Features

Item to Be Adjusted		Training Feature	Notes
CA bus	R_{TT} for CK, CS, CA	ZQ calibration	Command-based ZQ calibration or background ZQ calibration
	V_{REF} for CK, CA	Command bus training	Similar function as LPDDR4
	CK-to-CS timing		
	CK-to-CA timing		
DQ bus	R_{TT} for DQ, WCK	ZQ calibration	Command-based ZQ calibration or background ZQ calibration
	R_{ON} for DQ, DMI,RDQS		
	CK-to-WCK timing adjustment	WCK2CK leveling	Similar function as LPDDR4 write leveling
	SOC V_{REFDQ} and read capture timing adjustment	Option 1: Read DQ calibration (MR33/34) (target frequency)	Similar function as LPDDR4 read DQ calibration
		Option 2: WRITE-FIFO (low frequency) + READ-FIFO (target frequency)	Similar function as LPDDR4 WRITE-FIFO/READ-FIFO
	LPDDR5 V_{REFDQ}	Write training: WRITE-FIFO + READ-FIFO	Similar training feature as LPDDR4
	^{t}WCK2DQI	Write training: WRITE-FIFO + READ-FIFO	Similar training feature as LPDDR4
		^{t}WCK2DQI OSC	Used to check ^{t}WCK2DQI shift periodically
Other functions	LPDDR5 WCK internal duty cycle improvement	Duty cycle monitor (DCM), duty cycle adjustment (DCA)	New feature in LPDDR5
	LPDDR5 DQ Rx margin improvement	Decision feedback equalization (DFE)	Effective V_{REF} adjustment; new feature in LPDDR5
	RDQS parity mode Rx adjustment (^{t}WCK2DQI for RDQS)	Read/write-based RDQS training	RDQS Rx adjustment if link ECC is used

Training Guidelines

General guidelines for LPDDR5 training are as follows:

- LPDDR5 must be trained for target frequency at a particular voltage/temperature.
- Users may choose to skip some training items if adequate interface margin for the appropriate frequency is accounted for.
- If the previous training result for a particular frequency/voltage/temperature is stored in the system, that result can be used. Because LPDDR5 supports three frequency set point (FSP) sets, this method can be useful when more than three operating frequencies exist.
- Periodic training may be needed for some interface characteristics, as explained in the Periodic Training section below.
- WCK2DQI/WCK2DQO oscillators can be used to check the timing shift for a parameter. For output driver and termination resistance shifts, background ZQ calibration is recommended.

Periodic Training

Periodic training may be needed for some interface characteristics. As a guideline for periodic training, temperature variation and voltage variation are defined for some parameters. If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown in this section.

Table 2: ^{t}WCK2DQ AC Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
DQ to WCK Rx offset temperature variation (write)	^{t}WCK2DQI_temp_HF	Max	0.6	ps/°C
	^{t}WCK2DQI_temp_LF	Max	0.7	
DQ to WCK Rx offset voltage variation (write)	^{t}WCK2DQI_volt_HF	Max	25	ps/50mV
	^{t}WCK2DQI_volt _LF	Max	50	
WCK to DQ offset temperature variation (read)	^{t}WCK2DQO_temp_HF	Max	1.5	ps/°C
	^{t}WCK2DQO_temp_LF	Max	1.8	
WCK to DQ offset voltage variation (read)	^{t}WCK2DQO_volt_HF	Max	3.0	ps/mV
	^{t}WCK2DQO_volt_LF	Max	5.0	

Notes:
1. _HF means high frequency and _LF means low frequency.
2. _HF is used for more than 1600 Mb/s and _LF is used for 1600 Mb/s or less.
3. WCK2DQ AC parameters (HF/LF) can be selected using MR18 OP[3]. Refer to MR18.

Table 3: Worst-Case Output Driver and Termination Resistance

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.5 × V_{DDQ}	R_{ONPD} (NOM) × (0.90 - ($dR_{ON}dT$ (MAX) × |ΔT|) - (dR_{ON} (MAX)dV2 × |ΔV2|) - (dR_{ON} (MAX)dVQ × |ΔVQ|))	R_{ONPD} (NOM) × (1.10 + ($dR_{ON}dT$ (MAX) × |ΔT|) + (dR_{ON} (MAX) dV2 × |ΔV2|) + (dR_{ON} (MAX) dVQ × |ΔVQ|))	ohm	1, 2, 3

Table 3: Worst-Case Output Driver and Termination Resistance (Continued)

Resistor	Definition Point	Min	Max	Unit	Notes
R_{TT}	0.5 × V_{DDQ}	R_{TT} (NOM) × (0.90 - ($dR_{ON}dT$ (MAX) × |ΔT|) - (dR_{ON} (MAX)dV2 × |ΔV2|) - (dR_{ON} (MAX) dVQ × |ΔVQ|))	R_{TT} (NOM) × (1.10 + ($dR_{ON}dT$ (MAX) × |ΔT|) + (dR_{ON} (MAX) dV2 × |ΔV2|) + (dR_{ON} (MAX) dVQ × |ΔVQ|))	ohm	1, 2, 3
R_{ONUNPU}	0.5 × V_{DDQ}	R_{ONUNPU} (NOM) × (0.70 - (dR_{ON}UNdT (MAX) × |ΔT|) - (dR_{ON} (MAX) UNdV2 × |ΔV2|) - (dR_{ON} (MAX) UNdVQ × |ΔVQ|))	R_{ONUNPU} (NOM) × (1.30 + (dR_{ON} (MAX) UNdT × |ΔT|) + (dR_{ON} (MAX) UNdV2 × |ΔV2|) + (dR_{ON} (MAX) UNdVQ × |ΔVQ|))	ohm	2, 3
R_{TTCS}	0.5 × V_{DDQ}	R_{TTCS} (NOM) × (0.90 - (dR_{ON} (MAX) × |ΔV2|) - (dR_{ON} (MAX) dV2 × |ΔV2|) - (dR_{ON} (MAX) dVQ × |ΔV2|))	R_{TTCS} (NOM) × (1.10 + (dR_{ON} (MAX) dT × |ΔT|) + (dR_{ON} (MAX) dV2 × |ΔV2|) + (dR_{ON} (MAX) dVQ × |ΔV2|))	ohm	1, 2, 3

Notes:
1. ΔT = T - T(@ calibration), ΔV2 = V_{DD2H} - V_{DD2H} (@ calibration), ΔVQ = V_{DDQ} - V_{DDQ} (@calibration)
2. $dR_{ON}dT$, $dR_{ON}dV2$, $dR_{ON}dVQ$, $dR_{TT}dV2$, $dR_{TT}dVQ$, $dR_{TT}dT$, dR_{ON}UNdT, dR_{ON}UNdV2, and dR_{ON}UNdVQ are not subject to production test but are verified by design and characterization.
3. V_{DD1}, V_{DD2H}, and V_{DDQ} must be nominal during measurement.

Table 4: Worst-Case Output High Voltage

Voltage	Min	Max	Unit	Notes
V_{OHPU}	V_{OHPU} (NOM) × (0.90 - (dVOH (MAX) dT × |ΔT|) - (dVOH (MAX) dV2 × |ΔV2|) - (dVOH (MAX) dVQ × |ΔVQ|))	V_{OHPD}PU (NOM) × (1.10 + (dV_{OH} (MAX) dT × |ΔT|) + (dV_{OH} (MAX) dV2 × |ΔV2|) + (dVOH (MAX) dVQ × |ΔVQ|))	V	1, 2, 3, 4

Notes:
1. ΔT = T - T (@ calibration), ΔV2 = V_{DD2H} - V_{DD2H} (@ calibration), ΔVQ = V_{DDQ} - V_{DDQ} (@ calibration)
2. dVOHdT and dV_{OH}dV2, and dVOHdVQ are not subject to production test but are verified by design and characterization.
3. Refer to the Pull-Up/Pull-Down Output Driver Characteristics and Calibration section of the data sheet for V_{OHPU}.
4. V_{DD1}, V_{DD2H}, and V_{DDQ} must be nominal during measurement.

Table 5: Output Driver and Termination Resistance Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} temperature sensitivity	0.00	0.75	%/°C
$dR_{ON}dV2$	R_{ON} V_{DD2H} voltage sensitivity	0.00	0.50	%/mV
$dR_{ON}dVQ$	R_{ON} V_{DDQ} voltage sensitivity	0.00	0.20	%/mV
dVOHdT	V_{OH} temperature sensitivity	0.00	0.75	%/°C
dVOHdV2	V_{OH} V_{DD2H} voltage sensitivity	0.00	0.35	%/mV

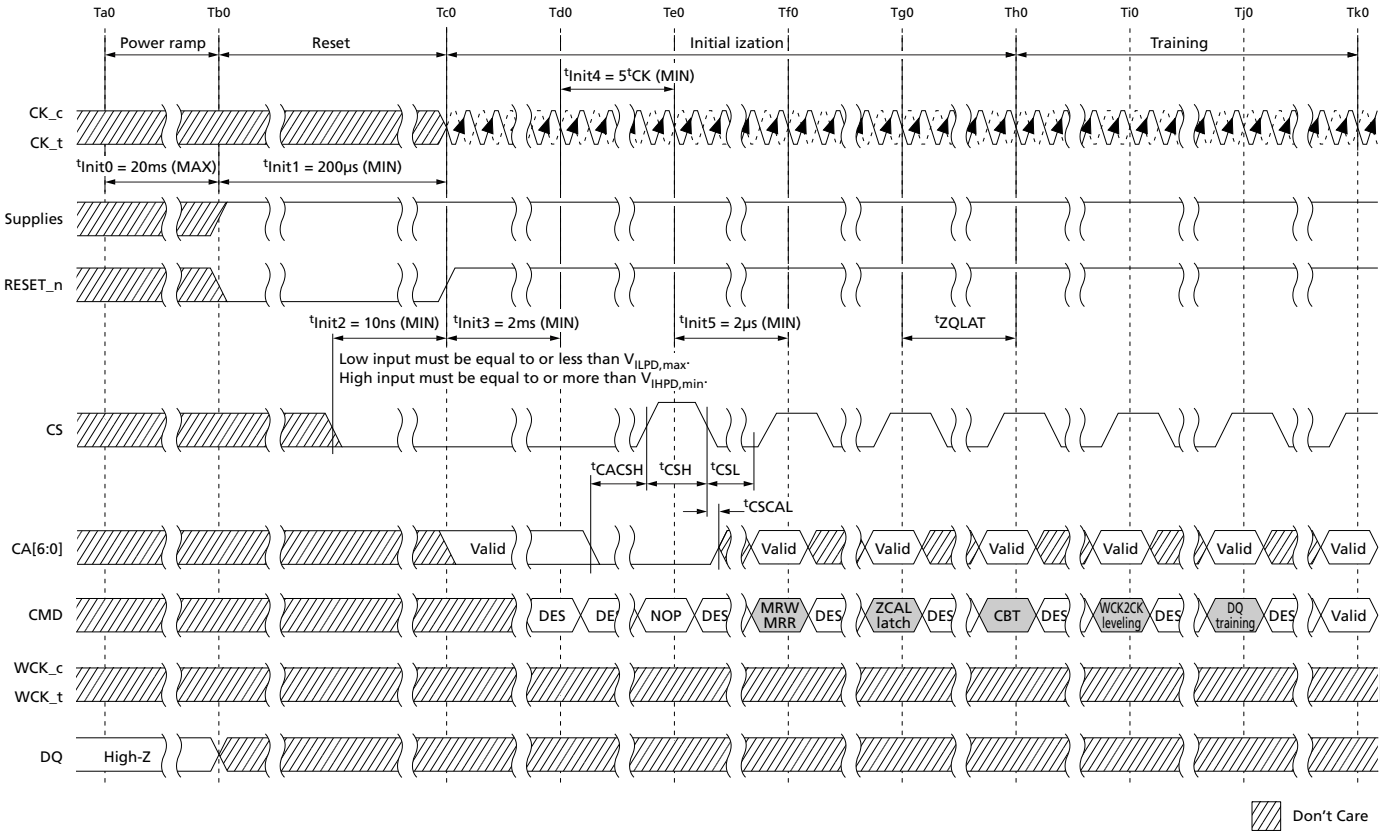
Table 5: Output Driver and Termination Resistance Temperature and Voltage Sensitivity (Continued)

Symbol	Parameter	Min	Max	Unit
dVOHdVQ	V_{OH} V_{DDQ} voltage sensitivity	0.00	0.35	%/mV
$dR_{TT}dT$	R_{TT} temperature sensitivity	0.00	0.75	%/°C
$dR_{TT}dV2$	R_{TT} V_{DD2H} voltage sensitivity	0.00	0.50	%/mV
$dR_{TT}dVQ$	R_{TT} V_{DDQ} voltage sensitivity	0.00	0.20	%/mV
dR_{ONUN} dT	Unterminated R_{ON} temperature sensitivity	0.00	0.75	%/°C
$dR_{ONUN}dV2$	Unterminated R_{ON} V_{DD2H} voltage sensitivity	0.00	0.75	%/mV
$dR_{ONUN}dVQ$	Unterminated R_{ON} V_{DDQ} voltage sensitivity	0.00	0.75	%/mV

Training Sequence Overview

This section provides a general overview of the LPDDR5 training sequence during power-up and initialization; however, it does not describe the sequence in detail. Refer to the General LPDDR5 Specifications 3 data sheet for detailed training sequence instructions.

Figure 1: Power Ramp and Initialization Sequence



Notes:
1. Training is optional and may be done at the system architect's direction. The training sequence after ZQ_CAL latch in this figure (Th) shows a simplified recommendation; the actual training sequence may vary depending on the system.
2. Initial ZQ calibration is started automatically by the device when RESET_n goes HIGH after ^{t}INIT1 and is completed before Td.
3. For the single V_{DD2} rail system, it is recommended to set MR13 OP[7] 1b to switch V_{DD2} mode right after the time any MRW/MRR can be asserted (Tf) prior to CBT.

Step 1: Perform a Power Ramp

Follow the voltage ramp conditions shown in the data sheet.

Step 2: Initiate a Reset Period

Drive Reset_n LOW for at least 200us.

Step 3: De-Assert Reset

Drive Reset_n = H. CK_t and CK_c need to either toggle or be at valid complementary levels near when RESET_n is de-asserted.

Step 4: Start the Clock

CK_t and CK_c are required to be toggling (Td) and stabilized for ^{t}INIT4 before CS receives one toggling (Te).

Step 5: Perform a Mode Register Read/Write (Optional)

Perform a mode register read (MRR) to check device information, and perform a mode register write (MRW) to change device parameters.

Step 6: Issue ZQ Latch

Since the initial ZQ calibration is performed automatically after the device ramps up, the ZQ LATCH command should be issued.

Steps 7 through 10 assume current FSP-OP is FSP-OP[x] (low frequency) and training is for FSP-OP[y] (target high frequency).

Step 7: Perform Command Bus Training (CBT Mode 2 Example)

Refer to the data sheet for detailed command bus training sequence instructions.

1. Set MR16 OP[1:0] to enable writing to FSP "Y" (FSP-WR[y]).
2. Write to FSP-WR[y] registers to set up high-frequency operating parameters.
3. Set MR13 OP[6] = 1B for command bus training mode 2, and set MR13 OP[7] = 0B to train the CA timing latched by CK rising edge.
4. Issue MRW-1 and MRW-2 commands to MR16 with OP[5:4] code for FSP-OP[y].
5. Drive DQ[7] HIGH, and then change CK frequency to the high-frequency operating point.
6. Perform CBT training (adjusting V_{REFCA},CLK-to-CS timing, and CLK-to-CA timing).
7. Change CK frequency to the low-frequency operating point, and then drive DQ[7] LOW.
   Note: When DQ[7] is driven LOW and the LPDDR5 device samples the LOW level of DQ[7] by WCK, the device automatically switches back to the FSP-OP registers that were used prior to training (that is, trained values are not retained by the device).
8. Issue MRW-1 and MRW-2 commands to MR16 to exit command bus training mode.
9. Repeat steps 3 through 8 to train the CA timing latched by the CK falling edge with MR13 OP[7] = 1B.
10. Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the device and setting all applicable mode register parameters.
11. Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination and change CK frequency to the high-frequency operation point. The command bus is now trained, and other training or normal operation can be executed.

Step 8: Perform WCK2CK Leveling

After performing command bus training, the DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR18-OP[6] is HIGH (Ti). Refer to the WCK2CK Leveling section of the data sheet for a detailed description of the WCK2CK leveling entry and exit sequence. After finishing WCK2CK leveling, ^{t}WCK2CK (WCK-to-CK relationship) is determined and WCK2CK SYNC operation is performed with the optimized margin.

1. Set MR16 OP[1:0] to enable writing to FSP "Y" (FSP-WR[y]).
2. Write FSP-WR[y] registers to set up high-frequency operating parameters (ODT_CK, ODT_WCK). This step can be skipped if FSP-WR[y] registers have already been programmed in a previous training sequence (Step 7: Perform Command Bus Training).
3. Perform WCK2CK leveling to adjust WCK-to-CK timing.

Step 9: Perform DQ Bus Training 1 (Read Training: SOC V_{REFDQ} and Read Capture Timing Adjustment)

1. Set MR16 OP[1:0] to enable writing to FSP "Y" (FSP-WR[y]).
2. Write FSP-WR[y] registers to set up high-frequency operating parameters. This step can be skipped if FSP-WR[y] registers have already been programmed in a previous training sequence.
3. Perform a read DQ calibration to adjust SOC DQV_{REF} and read capture timing.

Read training can be performed by other methods, such as a low-frequency FIFO write followed by target high-frequency FIFO read. A reliable, predefined data pattern is necessary for read training.

Step 10: Perform DQ Bus Training 2 (Write Training: LPDDR5 V_{REFDQ} and Write Timing Adjustment)

1. Issue a MRW command to MR16 to set VRCG to high-current mode.
2. Issue a MRW command to MR14/MR15 to set V_{REFDQ}.
3. Adjust WCK-to-DQ phase at SOC.
4. Issue a WRITE-FIFO command.
5. Issue a READ-FIFO command.
6. Perform a pass/fail judgement.
7. Repeat 2 thru 6 to find optimum V_{REFDQ} and WCK2DQI timing.
8. Issue a MRW command to MR16 to disable VRCG high-current mode.
9. Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the device and setting all applicable mode register parameters.

Step 11: Normal Operation

At Tkn, the device is ready for normal operation and can accept any valid command. Any mode registers that have not been previously set up for normal operation should be written at this time.

Revision History

Rev. A – 5/19

- Initial release

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