JEDEC STANDARD

Addendum No. 1 to JESD209-4 - Low Power Double Data Rate 4X (LPDDR4X)

JESD209-4-1

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Addendum No. 1 to JESD209-4 - LOW POWER DOUBLE DATA RATE 4X (LPDDR4X)

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(From JEDEC Board Ballot JCB-16-49, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit per channel SDRAM device with either one or two channels. LPDDR4 dual channel device density ranges from 4 Gb through 32 Gb and single channel density ranges from 2 Gb through 16 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR4 standard.

This addendum defines LPDDR4X specifications that supersede the LPDDR4 Standard (JESD209-4) to enable low V_{DDQ} operation of LPDDR4X devices to reduce power consumption.

2 Package Ballout and Pin Definition

2.1 Pad Order

Ch. A Top		Ch. A Bottom		Ch. B Top		Ch. B Bottom	
1	VDD2	41	VDD2	101	VDD2	141	VDD2
2	VSS	42	CKE_A	102	VSS	142	CKE_B
3	VDD1	43	CS_A	103	VDD1	143	CS_B
4	VDD2	44	VSS	104	VDD2	144	VSS
5	VSS	45	CA1_A	105	VSS	145	CA1_B
6	VSSQ	46	CA0_A	106	VSSQ	146	CA0_B
7	DQ8_A	47	VDD2	107	DQ8_B	147	VDD2
8	VDDQ	48	ODT(ca)_A	108	VDDQ	148	ODT(ca)_B
9	DQ9_A	49	VSS	109	DQ9_B	149	VSS
10	VSSQ	50	VDD1	110	VSSQ	150	VDD1
11	DQ10_A	51	VSSQ	111	DQ10_B	151	VSSQ
12	VDDQ	52	DQ7_A	112	VDDQ	152	DQ7_B
13	DQ11_A	53	VDDQ	113	DQ11_B	153	VDDQ
14	VSSQ	54	DQ6_A	114	VSSQ	154	DQ6_B
15	DQS1_t_A	55	VSSQ	115	DQS1_t_B	155	VSSQ
16	DQS1_c_A	56	DQ5_A	116	DQS1_c_B	156	DQ5_B
17	VDDQ	57	VDDQ	117	VDDQ	153	VDDQ
18	DMI1_A	58	DQ4_A	118	DMI1_B	158	DQ4_B
19	VSSQ	59	VSSQ	119	VSSQ	159	VSSQ
20	DQ12_A	60	DMI0_A	120	DQ12_B	160	DMI0_B
21	VDDQ	61	VDDQ	121	VDDQ	161	VDDQ
22	DQ13_A	62	DQS0_c_A	122	DQ13_B	162	DQS0_c_B
23	VSSQ	63	DQS0_t_A	123	VSSQ	163	DQS0_t_B
24	DQ14_A	64	VSSQ	124	DQ14_B	164	VSSQ
25	VDDQ	65	DQ3_A	125	VDDQ	165	DQ3_B
26	DQ15_A	66	VDDQ	126	DQ15_B	166	VDDQ
27	VSSQ	67	DQ2_A	127	VSSQ	167	DQ2_B
28	ZQ	68	VSSQ	128	RESET_n	168	VSSQ
29	VDDQ	69	DQ1_A	129	VDDQ	169	DQ1_B
30	VDD2	70	VDDQ	130	VDD2	170	VDDQ
31	VDD1	71	DQ0_A	131	VDD1	171	DQ0_B
32	VSS	72	VSSQ	132	VSS	172	VSSQ
33	CA5_A	73	VSS	133	CA5_B	173	VSS
34	CA4_A	74	VDD2	134	CA4_B	174	VDD2
35	VDD2	75	VDD1	135	VDD2	175	VDD1
36	CA3_A	76	VSS	136	CA3_B	176	VSS
37	CA2_A	77	VDD2	137	CA2_B	177	VDD2
38	VSS			138	VSS		
39	CK_c_A			139	CK_c_B		
40	CK_t_A			140	CK_t_B		
Ch. A Top				Ch. B Top			

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads ((#12,#21,#57,#66,#112,#121,#157 and #166) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

2.2 Single Channel Pad Order

Top	
1	VDD2
2	VSS
3	VDD1
4	VDD2
5	VSS
6	VSSQ
7	DQ8
8	VDDQ
9	DQ9
10	VSSQ
11	DQ10
12	VDDQ
13	DQ11
14	VSSQ
15	DQS1_t
16	DQS1_c
17	VDDQ
18	DMI1
19	VSSQ
20	DQ12
21	VDDQ
22	DQ13
23	VSSQ
24	DQ14
25	VDDQ
26	DQ15
27	VSSQ
28	ZQ
29	VDDQ
30	VDD2
31	RESET_n
32	VDD1
33	VSS
34	CA5
35	CA4
36	VDD2
37	CA3
38	CA2
39	VSS

40	CK_c
41	CK_t
42	VDD2
43	CKE
44	CS
45	VSS
46	CA1
47	CA0
48	VDD2
49	ODT(ca)
50	VSS
51	VDD1
52	VSSQ
53	DQ7
54	VDDQ
55	DQ6
56	VSSQ
57	DQ5
58	VDDQ
59	DQ4
60	VSSQ
61	DMI0
62	VDDQ
63	DQS0_c
64	DQS0_t
65	VSSQ
66	DQ3
67	VDDQ
68	DQ2
69	VSSQ
70	DQ1
71	VDDQ
72	DQ0
73	VSSQ
74	VSS
75	VDD2
76	VDD1
77	VSS
78	VDD2
Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads (#12, #21, #57 and #66) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

NOTE 4 A RESET_n pad is added. The RESET_n pad location is vendor specific. See vendor device datasheets for details about RESET_n pad location.

2.3 LPDDR4X packages

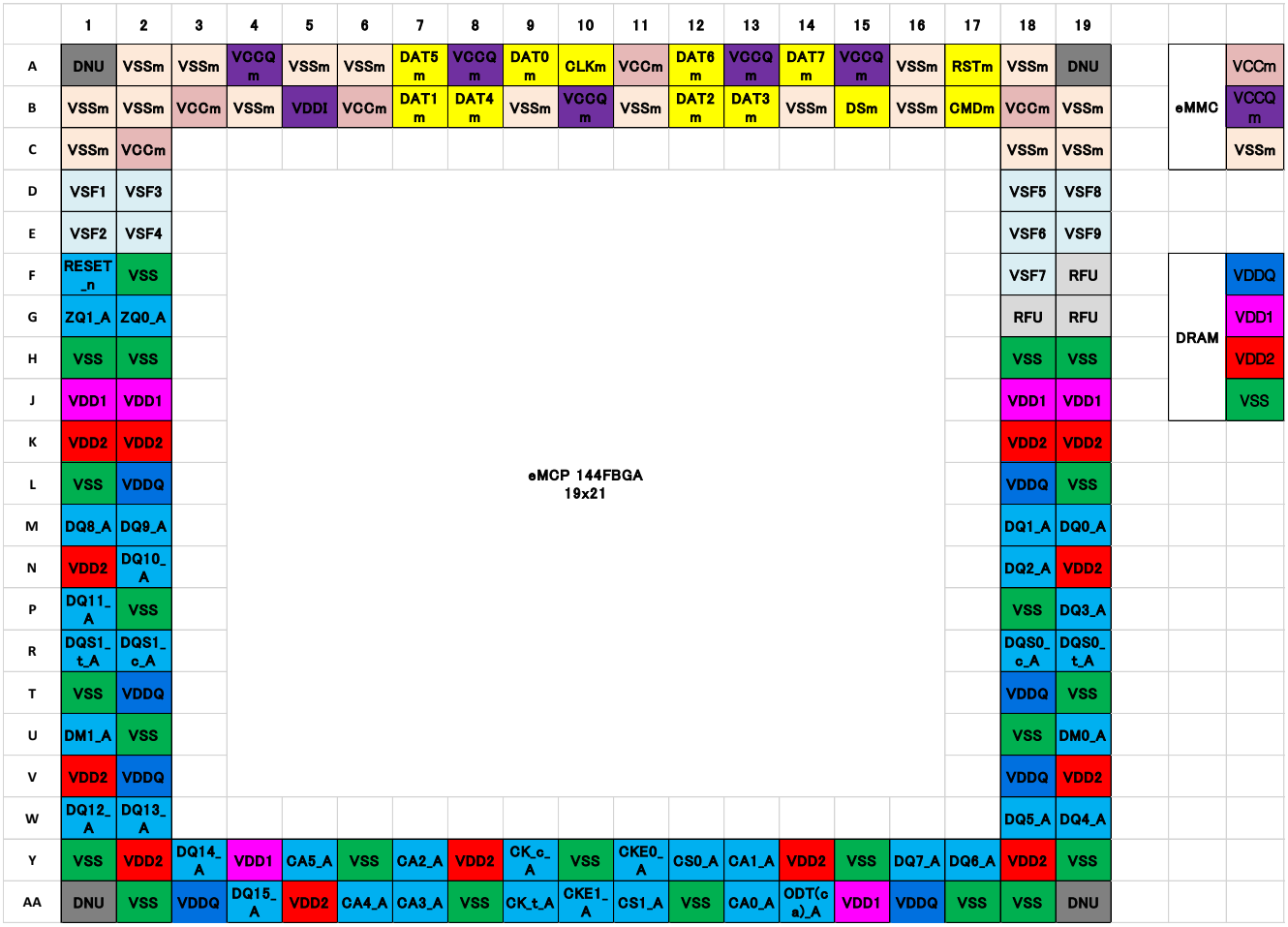
2.3.1 LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch) – Using MO-317A

LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	NC	VDD2	DQ3_A	VSS	DQ5_A	ODT(ca)_A	CA0_A	CS1_A	CKE1_A	CA2_A	VSS	VSS	DQ13_A	VDD2	VDD1	DQ10_A	ZQ1_A	ZQ1_D	DQ10_C	VDD1	VDD2	DQ13_C	VSS	VSS	CA2_C	CKE1_C	CS1_C	CA0_C	ODT(ca)_C	DQ5_C	VSS	DQ3_C	VDD2	NC	A
B	VSS	DQ2_A	VDDQ	DMI0_A	VDDQ	DQ7_A	VDD2	CS0_A	CKE0_A	VDD2	CA4_A	DQ15_A	VDDQ	DMI1_A	DQ11_A	VSS	ZQ0_A	ZQ0_D	VSS	DQ11_C	DMI1_C	VDDQ	DQ15_C	CA4_C	VDD2	CKE0_C	CS0_C	VDD2	DQ7_C	VDDQ	DMI0_C	VDDQ	DQ2_C	VSS	B
C	DQ0_A	VDDQ	VSS	VSS	DQ4_A	VDDQ	CA1_A	VDD2	VSS	CA3_A	VSS	VDDQ	DQ12_A	VSS	VDDQ	DQ9_A	RESET_n	RFU	DQ9_C	VDDQ	VSS	DQ12_C	VDDQ	VSS	CA3_C	VSS	VDD2	CA1_C	VDDQ	DQ4_C	VSS	VSS	VDDQ	DQ0_C	C
D	VDD1	DQ1_A	DQS0_t_A	DQS0_c_A	VSS	DQ6_A	VSS	CK_t_A	CK_c_A	VSS	CA5_A	DQ14_A	VSS	DQS1_c_A	DQS1_t_A	VDDQ	DQ8_A	DQ8_C	VDDQ	DQS1_t_C	DQS1_c_C	VSS	DQ14_C	CA5_C	VSS	CK_c_C	CK_t_C	VSS	DQ6_C	VSS	DQS0_c_C	DQS0_t_C	DQ1_C	VDD1	D
E	VDD2	VSS																															VSS	VDD2	E
F	VDD2	VDD2																															VDD2	VDD2	F
G	VSS	VSS																															VSS	VSS	G
H	RFU	RFU																															RFU	RFU	H
J	RFU	RFU																															RFU	RFU	J
K	RFU	RFU																															RFU	RFU	K
L	RFU	RFU																															RFU	RFU	L
M	RFU	RFU																															RFU	RFU	M
N	RFU	RFU																															RFU	RFU	N
P	RFU	RFU																															RFU	RFU	P
R	RFU	RFU																															RFU	RFU	R
T	RFU	RFU																															RFU	RFU	T
U	RFU	RFU																															RFU	RFU	U
V	RFU	RFU																															RFU	RFU	V
W	RFU	RFU																															RFU	RFU	W
Y	RFU	RFU																															RFU	RFU	Y
AA	RFU	RFU																															RFU	RFU	AA
AB	RFU	RFU																															RFU	RFU	AB
AC	RFU	RFU																															RFU	RFU	AC
AD	RFU	RFU																															RFU	RFU	AD
AE	RFU	RFU																															RFU	RFU	AE
AF	RFU	RFU																															RFU	RFU	AF
AG	RFU	RFU																															RFU	RFU	AG
AH	VSS	VSS																															VSS	VSS	AH
AJ	VDD2	VDD2																															VDD2	VDD2	AJ
AK	VDD2	VSS																															VSS	VDD2	AK
AL	VDD1	DQ1_B	DQS0_t_B	DQS0_c_B	VSS	DQ6_B	VSS	CK_t_B	CK_c_B	VSS	CA5_B	DQ14_B	VSS	DQS1_c_B	DQS1_t_B	VDDQ	DQ8_B	DQ8_D	VDDQ	DQS1_t_D	DQS1_c_D	VSS	DQ14_D	CA5_D	VSS	CK_c_D	CK_t_D	VSS	DQ6_D	VSS	DQS0_c_D	DQS0_t_D	DQ1_D	VDD1	AL
AM	DQ0_B	VDDQ	VSS	VSS	DQ4_B	VDDQ	CA1_B	VDD2	VSS	CA3_B	VSS	VDDQ	DQ12_B	VSS	VDDQ	DQ9_B	VDD2	VDD2	DQ9_D	VDDQ	VSS	DQ12_D	VDDQ	VSS	CA3_D	VSS	VDD2	CA1_D	VDDQ	DQ4_D	VSS	VSS	VDDQ	DQ0_D	AM
AN	VSS	DQ2_B	VDDQ	DMI0_B	VDDQ	DQ7_B	VDD2	CS0_B	CKE0_B	VDD2	CA4_B	DQ15_B	VDDQ	DMI1_B	DQ11_B	VSS	RFU	RFU	VSS	DQ11_D	DMI1_D	VDDQ	DQ15_D	CA4_D	VDD2	CKE0_D	CS0_D	VDD2	DQ7_D	VDDQ	DMI0_D	VDDQ	DQ2_D	VSS	AN
AP	NC	VDD2	DQ3_B	VSS	DQ5_B	ODT(ca)_B	CA0_B	CS1_B	CKE1_B	CA2_B	VSS	VSS	DQ13_B	VDD2	VDD1	DQ10_B	RFU	RFU	DQ10_D	VDD1	VDD2	DQ13_D	VSS	VSS	CA2_D	CKE1_D	CS1_D	CA0_D	ODT(ca)_D	DQ5_D	VSS	DQ3_D	VDD2	NC	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

NOTE 1 14 mm x 14 mm, 0.4 mm pitch.
NOTE 2 376 ball count, 34 rows.
NOTE 3 Top View, A1 in top left corner.
NOTE 4 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
NOTE 5 Package Channel a and Channel d shall be assigned to die Channel A of different LPDDR4 die.
NOTE 6 DRAM die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.2 144 ball ePoP MCP One-Channel FBGA (top view) using MO-323A



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	DNU	VSSm	VSSm	VCCQm	VSSm	VSSm	DAT5m	VCCQm	DAT0m	CLKm	VCCm	DAT6m	VCCQm	DAT7m	VCCQm	VSSm	RSTm	VSSm	DNU
B	VSSm	VSSm	VCCm	VSSm	VDDI	VCCm	DAT1m	DAT4m	VSSm	VCCQm	VSSm	DAT2m	DAT3m	VSSm	DSm	VSSm	CMDm	VCCm	VSSm
C	VSSm	VCCm																VSSm	VSSm
D	VSF1	VSF3																VSF5	VSF8
E	VSF2	VSF4																VSF6	VSF9
F	RESET_n	VSS																VSF7	RFU
G	ZQ1_A	ZQ0_A																RFU	RFU
H	VSS	VSS																VSS	VSS
J	VDD1	VDD1																VDD1	VDD1
K	VDD2	VDD2																VDD2	VDD2
L	VSS	VDDQ																VDDQ	VSS
M	DQ8_A	DQ9_A																DQ1_A	DQ0_A
N	VDD2	DQ10_A																DQ2_A	VDD2
P	DQ11_A	VSS																VSS	DQ3_A
R	DQS1_t_A	DQS1_c_A																DQS0_c_A	DQS0_t_A
T	VSS	VDDQ																VDDQ	VSS
U	DM1_A	VSS																VSS	DM0_A
V	VDD2	VDDQ																VDDQ	VDD2
W	DQ12_A	DQ13_A																DQ5_A	DQ4_A
Y	VSS	VDD2	DQ14_A	VDD1	CA5_A	VSS	CA2_A	VDD2	CK_c_A	VSS	CKE0_A	CS0_A	CA1_A	VDD2	VSS	DQ7_A	DQ6_A	VDD2	VSS
AA	DNU	VSS	VDDQ	DQ15_A	VDD2	CA4_A	CA3_A	VSS	CK_t_A	CKE1_A	CS1_A	VSS	CA0_A	ODT(ca)_A	VDD1	VDDQ	VSS	VSS	DNU

eMMC	
	VCCm
	VCCQm
	VSSm

DRAM	
	VDDQ
	VDD1
	VDD2
	VSS

NOTE 1 0.4 mm pitch, 2 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 Body size: 8 mm x 9.5 mm

NOTE 4 ODT(ca)_A balls are wired to ODT(ca)_A pads of Rank 0 DRAM die. ODT(ca) pads for other ranks (if present) are disabled in the package.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to V_{SS} package balls.

NOTE 6 The flash ball-out supports *e*•MMC 5.x

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.3 200-ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODTa	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

0.65mm Pitch

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.4 432-ball x64 HDI Discrete Package, 0.50 mm x 0.50 mm (MO-313)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	A
B	VDDQ	VDD1	DQ0_A	VSS	CA0_A	VDD2		VDD2	CA4_A	VSS	DQ8_A	VDD1	VDDQ		VDDQ	VDD1	DQ0_C	VSS	CA0_C	VDD2		VDD2	CA4_C	VSS	DQ8_C	VDD1	VDDQ	B
C	VDDQ	DQ1_A	VSS	DQ5_A	VSS	CA2_A		CA3_A	VSS	DQ13_A	VSS	DQ9_A	VDDQ		VDDQ	DQ1_C	VSS	DQ5_C	VSS	CA2_C		CA3_C	VSS	DQ13_C	VSS	DQ9_C	VDDQ	C
D	VDDQ	VSS	DQ4_A	VSS	CA1_A	VDD2		VDD2	CA5_A	VSS	DQ12_A	VSS	VDDQ		VDDQ	VSS	DQ4_C	VSS	CA1_C	VDD2		VDD2	CA5_C	VSS	DQ12_C	VSS	VDDQ	D
E	VDDQ	DQ2_A	VSS	DQ6_A	VSS	CLK_t_A		CLK_c_A	VSS	DQ14_A	VSS	DQ10_A	VDDQ		VDDQ	DQ2_C	VSS	DQ6_C	VSS	CLK_t_C		CLK_c_C	VSS	DQ14_C	VSS	DQ10_C	VDDQ	E
F	VDDQ	VSS	DQS0_t_A	VSS	CS1_A	VDD2		VDD2	CKE0_A	VSS	DQS1_t_A	VSS	VDDQ		VDDQ	VSS	DQS0_t_C	VSS	CS1_C	VDD2		VDD2	CKE0_C	VSS	DQS1_t_C	VSS	VDDQ	F
G	VDDQ	DQ3_A	VSS	DQS0_c_A	VSS	CS0_A		CKE1_A	VSS	DQS1_c_A	VSS	DQ11_A	VDDQ		VDDQ	DQ3_C	VSS	DQS0_c_C	VSS	CS0_C		CKE1_C	VSS	DQS1_c_C	VSS	DQ11_C	VDDQ	G
H	VDDQ	VSS	DMI0_A	VSS	DQ7_A	VDD2		VDD2	DQ15_A	VSS	DMI1_A	VSS	VDDQ		VDDQ	VSS	DMI0_C	VSS	DQ7_C	VDD2		VDD2	DQ15_C	VSS	DMI1_C	VSS	VDDQ	H
J	VDDQ	ZQ3_A	ZQ2_A	ODT ca_A	CS3_A	CS2_A		CKE3_A	CKE2_A	ZQ0_A	VSS	ZQ1_A	VDDQ		VDDQ	ZQ3_C	ZQ2_C	ODT ca_C	CS3_C	CS2_C		CKE3_C	CKE2_C	ZQ0_C	VSS	ZQ1_C	VDDQ	J
K																												K
L																												L
M																												M
N																												N
P																												P
R																												R
T																												T
V	VDDQ	VSS	VSS	ODT ca_B	CS3_B	CS2_B		CKE3_B	CKE2_B	VSS	VSS	RESET_n	VDDQ		VDDQ	VSS	VSS	ODT ca_D	CS3_D	CS2_D		CKE3_D	CKE2_D	VSS	VSS	NC	VDDQ	V
W	VDDQ	VSS	DMI0_B	VSS	DQ7_B	VDD2		VDD2	DQ15_B	VSS	DMI1_B	VSS	VDDQ		VDDQ	VSS	DMI0_D	VSS	DQ7_D	VDD2		VDD2	DQ15_D	VSS	DMI1_D	VSS	VDDQ	W
Y	VDDQ	DQ3_B	VSS	DQS0_c_B	VSS	CS0_B		CKE1_B	VSS	DQS1_c_B	VSS	DQ11_B	VDDQ		VDDQ	DQ3_D	VSS	DQS0_c_D	VSS	CS0_D		CKE1_D	VSS	DQS1_c_D	VSS	DQ11_D	VDDQ	Y
AA	VDDQ	VSS	DQS0_t_B	VSS	CS1_B	VDD2		VDD2	CKE0_B	VSS	DQS1_t_B	VSS	VDDQ		VDDQ	VSS	DQS0_t_D	VSS	CS1_D	VDD2		VDD2	CKE0_D	VSS	DQS1_t_D	VSS	VDDQ	AA
AB	VDDQ	DQ2_B	VSS	DQ6_B	VSS	CLK_t_B		CLK_c_B	VSS	DQ14_B	VSS	DQ10_B	VDDQ		VDDQ	DQ2_D	VSS	DQ6_D	VSS	CLK_t_D		CLK_c_D	VSS	DQ14_D	VSS	DQ10_D	VDDQ	AB
AC	VDDQ	VSS	DQ4_B	VSS	CA1_B	VDD2		VDD2	CA5_B	VSS	DQ12_B	VSS	VDDQ		VDDQ	VSS	DQ4_D	VSS	CA1_D	VDD2		VDD2	CA5_D	VSS	DQ12_D	VSS	VDDQ	AC
AD	VDDQ	DQ1_B	VSS	DQ5_B	VSS	CA2_B		CA3_B	VSS	DQ13_B	VSS	DQ9_B	VDDQ		VDDQ	DQ1_D	VSS	DQ5_D	VSS	CA2_D		CA3_D	VSS	DQ13_D	VSS	DQ9_D	VDDQ	AD
AE	VDDQ	VDD1	DQ0_B	VSS	CA0_B	VDD2		VDD2	CA4_B	VSS	DQ8_B	VDD1	VDDQ		VDDQ	VDD1	DQ0_D	VSS	CA0_D	VDD2		VDD2	CA4_D	VSS	DQ8_D	VDD1	VDDQ	AE
AF	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Notes:
1) 0.5mm ball pitch
2) 432 ball count
3) Top view, A1 in top left corner
4) ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package
5) Package Channel A and Channel C shall be assigned to die Channel A of different DRAM die
6) ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. ZQ3, CKE3_A, CKE3_B, CS3_A, and CS3_B balls are reserved for 4-rank package. For 1-rank and 2-rank package those balls are NC
7) Die pad VSS and VSSQ signals are combined to VSS package balls
8) Package requires dual channel die or functional equivalent of single channel die-stack

2.3.5 254 ball *e*•MMC MCP Two-Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0_A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VDDQ	VSS	DQ4_A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0t A				CA2_A	VSS	CA5_A	ZQ1			C
D			DQ3_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0c A				CA3_A	VSS	VSS	ZQ2			D
E													CA4_A	VSS	CS0_A	CKE0_A			E
F													CA1_A	VSS	CS1_A	CKE1_A			F
G			DQ13A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_A	VSS	CLK_cA			G
H			DMI1_A	VSS	VDDQ	DQ14A	VSS	DQ15A	VDDQ				VSS	CS2_A	VSS	CLK_tA			H
J			DQ11A	VDDQ	VDDQ	VSS	DQ12A	VDDQ	DQS1cA				ODT_A	CKE2_A	VCCQ	VCCQ	VCCQ		J
K		VDD2	DQ10A	VSS	DQ8_A	DQ9_A	VSS	VSS	DQS1tA				VSSm	VSSm	VCCQ	VSSm	NC		K
L							VDD2	VDD2	VDD2			VSSm	DAT7	DAT6	VSSm	VSSm	VDDI		L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			DS	VSSm	VSSm	DAT1	DAT4	VCC		M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			VSSm	DAT2	DAT5	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			CLK	VSSm	VSSm	DAT3	DAT0	VCC		P
R		VDD2	DQ10B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1tB				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11B	VDDQ	VDDQ	VSS	DQ12B	VDDQ	DQS1cB				ODT_B	CKE2_B	VCCQ	VCCQ	NC		T
U			DMI1_B	VSS	VDDQ	DQ14B	VSS	DQ15B	VDDQ				VSS	CS2_B	VSS	CLK_tB			U
V			DQ13B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_cB			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0cB				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0tB				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_CA_[x] balls are wired to ODT_CA)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

NOTE 8 The flash ball-out supports *e*•MMC 5.x.

2.3.6 254 ball UFS MCP Two-Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0_A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VDDQ	VSS	DQ4_A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0t A				CA2_A	VSS	CA5_A	ZQ1			C
D			DQ3_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0c A				CA3_A	VSS	VSS	ZQ2			D
E													CA4_A	VSS	CS0_A	CKE0_A			E
F													CA1_A	VSS	CS1_A	CKE1_A			F
G			DQ13A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_A	VSS	CLK_cA			G
H			DMI1_A	VSS	VDDQ	DQ14A	VSS	DQ15A	VDDQ				VSS	CS2_A	VSS	CLK_tA			H
J			DQ11A	VDDQ	VDDQ	VSS	DQ12A	VDDQ	DQS1cA				ODT_A	CKE2_A	VCCQ2	VCCQ2	VCCQ2		J
K		VDD2	DQ10A	VSS	DQ8_A	DQ9_A	VSS	VSS	DQS1tA				VSSm	VSSm	VCCQ2	VSSm	VDDIQ2		K
L							VDD2	VDD2	VDD2			VSSm	DIN1_c	DIN1_t	VSSm	VSSm	VDDI		L
M			NC	VSF1	VSF3	VSF5	RFU	VSSm	RFU			RST_n	VSSm	VSSm	DIN0_c	DIN0_t	VCC		M
N			NC	VSF2	VSF4	VSF6	RFU	VSSm	RFU			VSSm	DOUT1c	DOUT1t	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			REF_CLK	VSSm	VSSm	DOUT0c	DOUT0t	VCC		P
R		VDD2	DQ10B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1tB				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11B	VDDQ	VDDQ	VSS	DQ12B	VDDQ	DQS1cB				ODT_B	CKE2_B	VCCQ	VCCQ	VDDIQ		T
U			DMI1_B	VSS	VDDQ	DQ14B	VSS	DQ15B	VDDQ				VSS	CS2_B	VSS	CLK_tB			U
V			DQ13B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_cB			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0cB				CA3_B	VSS	VSS	RESET n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0tB				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_CA_[x] balls are wired to ODT_CA)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.7 254 ball *e*•MMC MCP One Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC	DNU	DNU	A
B	DNU		NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ0		DNU	B
C			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ1			C
D			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ2			D
E													NC	NC	NC	NC			E
F													NC	NC	NC	NC			F
G			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			G
H			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			H
J			NC	NC	NC	NC	NC	NC	NC				NC	NC	VCCQ	VCCQ	VCCQ		J
K		NC	NC	NC	NC	NC	NC	NC	NC				VSSm	VSSm	VCCQ	VSSm	NC		K
L							NC	NC	NC			VSSm	DAT7	DAT6	VSSm	VSSm	VDDI		L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			DS	VSSm	VSSm	DAT1	DAT4	VCC		M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			VSSm	DAT2	DAT5	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			CLK	VSSm	VSSm	DAT3	DAT0	VCC		P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(ca)_B	CKE2_B	VCCQ	VCCQ	NC		T
U			DMI1_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CLK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_(ca)_B ball is wired to ODT_(ca)_B pad of Rank 0 DRAM die. ODT_(ca) pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_B, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 6 Vender specific function (VSF) – this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vender specific operations.

NOTE 7 The flash ball-out supports *e*•MMC 5.x.

2.4 Pad Definition and Description

LPDDR4X pad definitions are the same as LPDDR4, except as described in Table 1.

Table 1 — Pad Definition and Description

Symbol	Type	Description
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either V_{DD2} or V_{SS}.

2.5 Mode Register Definition

Table 2 — Mode Register Assignment in LPDDR4 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	Reserved	RFU	RFU	RZQI		RFU	RFU	Refresh mode
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	LPDDR4 Manufacturer ID							
6	Revision ID-1							
7	Revision ID-2							
8	IO Width		Density				Type	
9	Vendor Specific Test Register							
10	RFU							ZQ-Reset
11	RFU	CA ODT			RFU	DQ ODT		
12	CBT Mode	VR-CA	V_{REF}(CA)					
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(dq)	V_{REF}(DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count - LSB							
19	DQS Oscillator Count - MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	ODT for x8_2ch(Byte) mode	ODTD-CA	ODTE-CS	ODTE-CK	CODT			
23	DQS interval timer run time setting							
24	TRR Mode	TRR Mode BAn			Unlimited MAC	MAC Value		
25	PPR Resource							
26	RFU							
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing - SDRAM will ignore							
31	RFU							
32	DQ Calibration Pattern “A” (default = 5AH)							
33	RFU							
34	RFU							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							

2.5.1 MR0 Register Information (MA [7:0] = 00H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved	RFU	RFU	RZQI		RFU	Latency Mode	Refresh mode

Function	Register Type	Operand	Data	Notes
Refresh mode	Read-only	OP[0]	0_B : Both legacy and modified refresh mode supported 1_B : Only modified refresh mode supported	
Latency mode		OP[1]	0_B : Device supports normal latency 1_B : Device supports byte mode latency	5,6
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00_B: RZQ Self-Test Not Supported 01_B: ZQ pin may connect to V_{SSQ} or float 10_B: ZQ-pin may short to V_{DDQ} 11_B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3, 4

NOTE 1 RZQI MR value, if supported, will be valid after the following sequence:
a. Completion of MPC ZQCAL Start command to either channel.
b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.
RZQI value will be lost after Reset.

NOTE 2 If the ZQ-pin is connected to V_{SSQ} to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.

NOTE 4 If ZQ Self-Test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ω ± 1%).

NOTE 5 See byte mode addendum spec for byte mode latency details.

NOTE 6 Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

2.5.2 MR3 Register Information (MA[7:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	0_B: V_{DDQ}*0.6 1_B: V_{DDQ}*0.5 (default)	1,4
WR PST(WR Post-Amble Length)		OP[1]	0_B: WR Post-amble = 0.5*tCK (default) 1_B: WR Post-amble = 1.5*tCK(Vendor specific function)	2,3,5
Post Package Repair Protection		OP[2]	0_B: PPR protection disabled (default) 1_B: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000_B: RFU 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 (default) 111_B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0_B: Disabled (default) 1_B: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0_B: Disabled (default) 1_B: Enabled	2,3

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.

NOTE 5 Refer to the supplier data sheet for vender specific function. 1.5*tCK apply > 1.6GHz clock.

NOTE 6 If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

2.5.3 MR12 Register Information (MA[7:0] = $0C_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CBT Mode	VR-CA	V_{REF}(CA)					

Function	Register Type	Operand	Data	Notes
V_{REF}(CA) (V_{REF}(CA) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See table below All Others: Reserved	1,2,3, 5,6
VR-CA (V_{REF}(CA) Range)		OP[6]	0_B: V_{REF}(CA) Range[0] enabled 1_B: V_{REF}(CA) Range[1] enabled (default)	1,2,4, 5,6
CBT Mode	Write	OP[7]	0_B: Mode1 (Default) 1_B: Mode2	7

NOTE 1 This register controls the V_{REF}(CA) levels. Refer to Table 3 for actual voltage of V_{REF}(CA).

NOTE 2 A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.

NOTE 3 A write to OP[5:0] sets the internal V_{REF}(CA) level for FSP[0] when MR13 OP[6] = 0_B, or sets FSP[1] when MR13 OP[6] = 1_B. The time required for V_{REF}(CA) to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF}(CA) training for more information.

NOTE 4 A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 7 This field can be activated in only Byte Mode: x8. Device.

2.5.3 MR12 Register Information (MA[7:0] = $0C_H$) (cont'd)

Table 3 — V_{REF} Settings for Range[0] and Range[1]

Step: 0.6% (1/167)

Function	Operand	Range[0] Values (% of V_{DDQ})				Range[1] Values (% of V_{DDQ})				Notes
V_{REF} Settings for MR12	OP [5:0]	000000_B:	15.0%	011010_B:	30.5%	000000_B:	32.9%	011010_B:	48.5%	1,2,3
		000001_B:	15.6%	011011_B:	31.1%	000001_B:	33.5%	011011_B:	49.1%	
		000010_B:	16.2%	011100_B:	31.7%	000010_B:	34.1%	011100_B:	49.7%	
		000011_B:	16.8%	011101_B:	32.3%	000011_B:	34.7%	011101_B: default	50.3%	
		000100_B:	17.4%	011110_B:	32.9%	000100_B:	35.3%	011110_B:	50.9%	
		000101_B:	18.0%	011111_B:	33.5%	000101_B:	35.9%	011111_B:	51.5%	
		000110_B:	18.6%	100000_B:	34.1%	000110_B:	36.5%	100000_B:	52.1%	
		000111_B:	19.2%	100001_B:	34.7%	000111_B:	37.1%	100001_B:	52.7%	
		001000_B:	19.8%	100010_B:	35.3%	001000_B:	37.7%	100010_B:	53.3%	
		001001_B:	20.4%	100011_B:	35.9%	001001_B:	38.3%	100011_B:	53.9%	
		001010_B:	21.0%	100100_B:	36.5%	001010_B:	38.9%	100100_B:	54.5%	
		001011_B:	21.6%	100101_B:	37.1%	001011_B:	39.5%	100101_B:	55.1%	
		001100_B:	22.2%	100110_B:	37.7%	001100_B:	40.1%	100110_B:	55.7%	
		001101_B:	22.8%	100111_B:	38.3%	001101_B:	40.7%	100111_B:	56.3%	
		001110_B:	23.4%	101000_B:	38.9%	001110_B:	41.3%	101000_B:	56.9%	
		001111_B:	24.0%	101001_B:	39.5%	001111_B:	41.9%	101001_B:	57.5%	
		010000_B:	24.6%	101010_B:	40.1%	010000_B:	42.5%	101010_B:	58.1%	
		010001_B:	25.1%	101011_B:	40.7%	010001_B:	43.1%	101011_B:	58.7%	
		010010_B:	25.7%	101100_B:	41.3%	010010_B:	43.7%	101100_B:	59.3%	
		010011_B:	26.3%	101101_B:	41.9%	010011_B:	44.3%	101101_B:	59.9%	
		010100_B:	26.9%	101110_B:	42.5%	010100_B:	44.9%	101110_B:	60.5%	
		010101_B:	27.5%	101111_B:	43.1%	010101_B:	45.5%	101111_B:	61.1%	
		010110_B:	28.1%	110000_B:	43.7%	010110_B:	46.1%	110000_B:	61.7%	
		010111_B:	28.7%	110001_B:	44.3%	010111_B:	46.7%	110001_B:	62.3%	
		011000_B:	29.3%	110010_B:	44.9%	011000_B:	47.3%	110010_B:	62.9%	
		011001_B:	29.9%	All Others: Reserved		011001_B:	47.9%	All Others: Reserved		

NOTE 1 These values may be used for MR12 OP[5:0] to set the V_{REF}(CA) levels in the LPDDR4-SDRAM.

NOTE 2 The range may be selected in the MR12 register by setting OP[6] appropriately.

NOTE 3 The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

2.5.4 MR14 Register Information (MA[7:0] = $0E_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(DQ)	V_{REF}(DQ)					

Function	Register Type	Operand	Data	Notes
V_{REF}(DQ) (V_{REF}(DQ) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See Table 4 All Others: Reserved	1,2,3, 5,6
VR(dq) (V_{REF}(DQ) Range)		OP[6]	0_B: V_{REF}(DQ) Range[0] enabled 1_B: V_{REF}(DQ) Range[1] enabled (default)	1,2,4, 5,6

NOTE 1 This register controls the V_{REF}(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.

NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See the section on MRR Operation.

NOTE 3 A write to OP[5:0] sets the internal V_{REF}(DQ) level for FSP[0] when MR13 OP[6] = 0_B, or sets FSP[1] when MR13 OP[6] = 1_B. The time required for V_{REF}(DQ) to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF}(DQ) training for more information.

NOTE 4 A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

2.5.4 MR14 Register Information (MA[7:0] = $0E_H$) (cont'd)

Table 4 — V_{REF} Settings for Range[0] and Range[1]

Step: 0.6% (1/167)

Function	Operand	Range[0] Values (% of V_{DDQ})				Range[1] Values (% of V_{DDQ})				Notes
V_{REF} Settings for MR14	OP [5:0]	000000_B:	15.0%	011010_B:	30.5%	000000_B:	32.9%	011010_B:	48.5%	1,2,3
		000001_B:	15.6%	011011_B:	31.1%	000001_B:	33.5%	011011_B:	49.1%	
		000010_B:	16.2%	011100_B:	31.7%	000010_B:	34.1%	011100_B:	49.7%	
		000011_B:	16.8%	011101_B:	32.3%	000011_B:	34.7%	011101_B default:	50.3%	
		000100_B:	17.4%	011110_B:	32.9%	000100_B:	35.3%	011110_B:	50.9%	
		000101_B:	18.0%	011111_B:	33.5%	000101_B:	35.9%	011111_B:	51.5%	
		000110_B:	18.6%	100000_B:	34.1%	000110_B:	36.5%	100000_B:	52.1%	
		000111_B:	19.2%	100001_B:	34.7%	000111_B:	37.1%	100001_B:	52.7%	
		001000_B:	19.8%	100010_B:	35.3%	001000_B:	37.7%	100010_B:	53.3%	
		001001_B:	20.4%	100011_B:	35.9%	001001_B:	38.3%	100011_B:	53.9%	
		001010_B:	21.0%	100100_B:	36.5%	001010_B:	38.9%	100100_B:	54.5%	
		001011_B:	21.6%	100101_B:	37.1%	001011_B:	39.5%	100101_B:	55.1%	
		001100_B:	22.2%	100110_B:	37.7%	001100_B:	40.1%	100110_B:	55.7%	
		001101_B:	22.8%	100111_B:	38.3%	001101_B:	40.7%	100111_B:	56.3%	
		001110_B:	23.4%	101000_B:	38.9%	001110_B:	41.3%	101000_B:	56.9%	
		001111_B:	24.0%	101001_B:	39.5%	001111_B:	41.9%	101001_B:	57.5%	
		010000_B:	24.6%	101010_B:	40.1%	010000_B:	42.5%	101010_B:	58.1%	
		010001_B:	25.1%	101011_B:	40.7%	010001_B:	43.1%	101011_B:	58.7%	
		010010_B:	25.7%	101100_B:	41.3%	010010_B:	43.7%	101100_B:	59.3%	
		010011_B:	26.3%	101101_B:	41.9%	010011_B:	44.3%	101101_B:	59.9%	
		010100_B:	26.9%	101110_B:	42.5%	010100_B:	44.9%	101110_B:	60.5%	
		010101_B:	27.5%	101111_B:	43.1%	010101_B:	45.5%	101111_B:	61.1%	
		010110_B:	28.1%	110000_B:	43.7%	010110_B:	46.1%	110000_B:	61.7%	
		010111_B:	28.7%	110001_B:	44.3%	010111_B:	46.7%	110001_B:	62.3%	
		011000_B:	29.3%	110010_B:	44.9%	011000_B:	47.3%	110010_B:	62.9%	
		011001_B:	29.9%	All Others: Reserved		011001_B:	47.9%	All Others: Reserved		

NOTE 1 These values may be used for MR14 OP[5:0] to set the V_{REF}(DQ) levels in the LPDDR4-SDRAM.

NOTE 2 The range may be selected in the MR14 register by setting OP[7,6] appropriately.

NOTE 3 The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

2.5.5 MR22 Register Information (MA[7:0] = 16_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ODTD for x8_2ch(Byte) mode		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 (illegal if MR3 OP[0] = 0_B) 010_B: RZQ/2 011_B: RZQ/3 (illegal if MR3 OP[0] = 0_B) 100_B: RZQ/4 101_B: RZQ/5 (illegal if MR3 OP[0] = 0_B) 110_B: RZQ/6 (illegal if MR3 OP[0] = 0_B) 111_B: RFU	1,2,3
ODTE-CK (CK ODT enabled for nonterminating rank)		OP[3]	ODT bond PAD is ignored 0_B: ODT-CK Enable (Default) 1_B: ODT-CK Disable	2,3,4,
ODTE-CS (CS ODT enable for nonterminating rank)		OP[4]	ODT bond PAD is ignored 0B: ODT-CS Enable (Default) 1_B: ODT-CS Disable	2,3,4
ODTD-CA (CA ODT termination disable)		OP[5]	ODT bond PAD is ignored 0_B: ODT-CA Enable (default) 1_B: ODT-CA Disable	2,3,4
X8ODTD[7:0] (CA/CLK ODT termination disable, [7:0] Byte select		OP[6]	Byte mode device x8 2ch only, lower [7:0] Byte selected Device 0_B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1_B: ODT-CS/CA/CLK Disabled	4
X8ODTD[15:8] (CA/CLK ODT termination disable, [15:8] Byte select		OP[7]	Byte mode device x8 2ch only, upper [15:8] Byte selected Device 0_B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1_B: ODT-CS/CA/CLK Disabled	4

NOTE 1 All values are “typical".

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 The ODT_CA pin is ignored by LPDDR4X devices. The ODT_CA pin shall be connected to either V_{DD2} or V_{SS}. CA/ CS/ CK ODT is fully controlled through MR11 and MR22. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed.

2.5.5 MR22 Register Information (MA[7:0] = 16_H) (cont'd)

Table 5 — LPDDR4X Byte Mode Device (MR11 OP[6:4] ≠ 000B Case)

MR22	ODTD Byte mode		ODT CA	ODT CS	ODT CK	ODT PAD Ignore					
						CA		CS		CK	
	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	Lower Byte	Upper Byte	Lower Byte	Upper Byte	Lower Byte	Upper Byte
LP4X	0	0	0	0	0	T	T	T	T	T	T
	0	0	0	0	1	T	T	T	T		
	0	0	0	1	0	T	T			T	T
	0	0	0	1	1	T	T				
	0	0	1	0	0			T	T	T	T
	0	0	1	0	1			T	T		
	0	0	1	1	0					T	T
	0	0	1	1	1						
	0	1	0	0	0		T		T		T
	0	1	0	0	1		T		T		
	0	1	0	1	0		T				T
	0	1	0	1	1		T				
	0	1	1	0	0				T		T
	0	1	1	0	1				T		
	0	1	1	1	0						T
	0	1	1	1	1						
	1	0	0	0	0	T		T		T	
	1	0	0	0	1	T		T			
	1	0	0	1	0	T				T	
	1	0	0	1	1	T					
	1	0	1	0	0			T		T	
	1	0	1	0	1			T			
	1	0	1	1	0					T	
	1	0	1	1	1						

NOTE T means "terminated" condition. Blank is "unterminated"

3 Command Definitions and Timing Diagrams

3.1 Pull Up/Pull Down Driver Characteristics and Calibration

Table 6 — Pull-down Driver Characteristics, with ZQ Calibration

R_{ONPD},nom	Resistor	Min	Nom	Max	Unit
40 Ω	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 Ω	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 Ω	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 Ω	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 Ω	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ω	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

NOTE All value are after ZQ Calibration. Without ZQ Calibration R_{ONPD} values are ± 30%.

Table 7 — Terminated Pull-Up Characteristics, with ZQ Calibration

VOH_{PU},nom	VOH,nom(mV)	Min	Nom	Max	Unit
V_{DDQ}*0.5	300	0.9	1	1.1	VOH,nom
V_{DDQ}*0.6	360	0.9	1	1.1	VOH,nom

NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%.

NOTE 2 VOH,nom (mV) values are based on a nominal V_{DDQ} = 0.6 V.

Table 8 — Terminated Valid Calibration Points

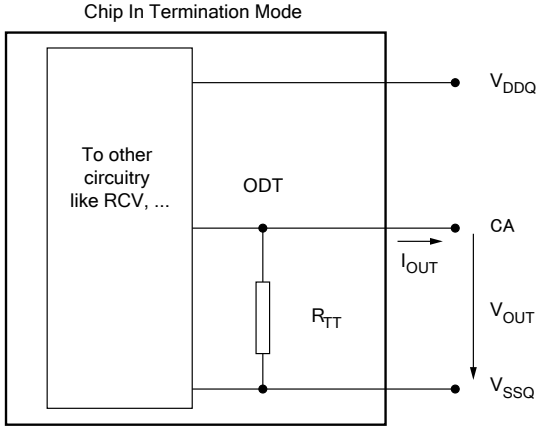
VOH_{PU},nom	SOC ODT Value					
	240	120	80	60	48	40
V_{DDQ}*0.5	VALID	VALID	VALID	VALID	VALID	VALID
V_{DDQ}*0.6	DNU	VALID	DNU	VALID	DNU	DNU

NOTE 1 Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.

NOTE 2 If the VOH(nom) calibration point is changed, then re-calibration is required.

NOTE 3 DNU = Do Not Use.

3.2 ODT Mode Register and ODT Characteristics



$$R_{TT} = \frac{Vout}{|Iout|}$$

Figure 1 — On Die Termination for CA

3.2 ODT Mode Register and ODT Characteristics (cont'd)

Table 9 — ODT DC Electrical Characteristics

(assuming RZQ = 240 Ω +/-1% over the entire operating temperature range after a proper ZQ calibration)

MR11 OP[6:4]	R_{TT}	Vout	Min	Nom	Max	Unit	Notes
001	240 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ	1,2
010	120 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/2	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/2	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/2	1,2
011	80 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/3	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/3	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/3	1,2
100	60 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/4	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/4	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/4	1,2
101	48 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/5	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/5	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/5	1,2
110	40 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/6	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/6	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/6	1,2
Mismatch CA-CA within clk group		0.50*V_{DDQ}	-		2	%	1,2,3

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 3.4 on voltage and temperature sensitivity.

NOTE 2 Pull-dn ODT resistors are recommended to be calibrated at 0.50*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75*V_{DDQ} and 0.2*V_{DDQ}.

NOTE 3 CA to CA mismatch within clock group (CA,CS) variation for a given component including CK_t and CK_c (characterized).

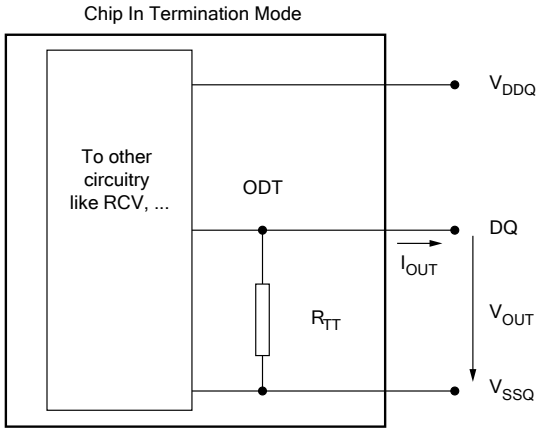
$$\mathrm{CA-CA_{Mismatch}} = \frac{\mathrm{RODT(max) - RODT(min)}}{\mathrm{RODT|T(avg)}}$$

3.3 On Die Termination for DQ, DQS and DMI

On-Die Termination effective resistance R_{TT} is defined by MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS_t and DQS_c pins.

A functional representation of the on-die termination is shown Figure 2.



$$R_{TT} = \frac{Vout}{|Iout|}$$

Figure 2 — On Die Termination

3.3 On Die Termination for DQ, DQS and DMI (cont'd)

Table 10 — ODT DC Electrical Characteristics

(assuming RZQ = 240 Ω +/-1% over the entire operating temperature range after a proper ZQ calibration)

MR11 OP[2:0]	R_{TT}	Vout	Min	Nom	Max	Unit	Notes
001	240 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ	1,2
010	120 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/2	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/2	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/2	1,2
011	80 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/3	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/3	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/3	1,2
100	60 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/4	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/4	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/4	1,2
101	48 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/5	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/5	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/5	1,2
110	40 Ω	VOLdc = 0.20*V_{DDQ}	0.8	1	1.1	RZQ/6	1,2
		VOMdc = 0.50*V_{DDQ}	0.9	1	1.1	RZQ/6	1,2
		VOHdc = 0.75*V_{DDQ}	0.9	1	1.3	RZQ/6	1,2
Mismatch DQ-DQ within byte		0.50*V_{DDQ}	-		2	%	1,2,3

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 3.4 on voltage and temperature sensitivity.

NOTE 2 Pull-dn ODT resistors are recommended to be calibrated at 0.75*V_{DDQ} and 0.2*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75*V_{DDQ} and 0.1*V_{DDQ}.

NOTE 3 DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).

$$\mathrm{DQ} - \mathrm{DQ}_{\mathrm{Mismatch}} = \frac{\mathrm{RODT(max)} - \mathrm{RODT(min)}}{\mathrm{RODT|T(avg)}}$$

3.4 Output Driver and Termination Register Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 11 and Table 12.

Table 11 — Output Driver and Termination Register Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.50 x V_{DDQ}	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2
VOH_{PU}	0.50 x V_{DDQ}	90-(dVOHdT x |ΔT|)-(dVOHdV x |ΔV|)	110+(dVOHdT x |ΔT|)+(dVOHdV x |ΔV|)	%	1,2,5
$R_{TT(I/O)}$	0.50 x V_{DDQ}	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2,3
$R_{TT(In)}$	0.50 x V_{DDQ}	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2,4

NOTE 1 ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)

NOTE 2 $dR_{ON}dT$, $dR_{ON}dV$, dVOHdT, dVOHdV, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.

NOTE 3 This parameter applies to Input/Output pin such as DQS, DQ and DMI and the input pins such as CK, CA, and CS.

NOTE 4 Refer to 4.36, Pull Up/Pull Down Driver Characteristics for VOH_{PU}.

Table 12 — Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	%/°C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	%/mV
dVOHdT	VOH Temperature Sensitivity	0.00	0.75	%/°C
dVOHdV	VOH Voltage Sensitivity	0.00	0.35	%/mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	%/°C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.20	%/mV

4 AC and DC Operating Conditions

4.1 Recommended DC Operating Conditions for low voltage

Table 13 — Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power	V_{DD1}	1.70	1.80	1.95	V	1,2
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	V_{DDQ}	0.57	0.6	0.65	V	2,3,4,5

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

NOTE 3 The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.

NOTE 4 V_{DDQ}(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.

NOTE 5 Pull up, pull down and ZQ calibration tolerance spec is valid only in normal V_{DDQ} tolerance range (0.57 V - 0.65 V).

4.2 Single Ended Output Slew Rate

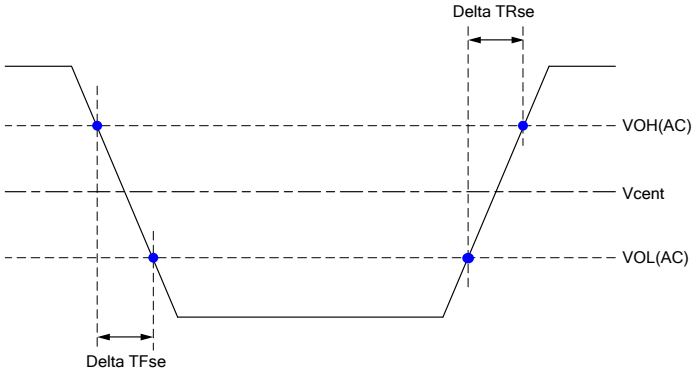


Figure 3 — Single Ended Output Slew Rate Definition

Table 14 — Output Slew Rate (single-ended) for 0.6 V V_{DDQ}

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (VOH = V_{DDQ}*0.5)	SRQse†	3.0	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-
† SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals				

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2*VOH(DC) and VOH(AC) = 0.8*VOH(DC).

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

4.3 Differential Output Slew Rate

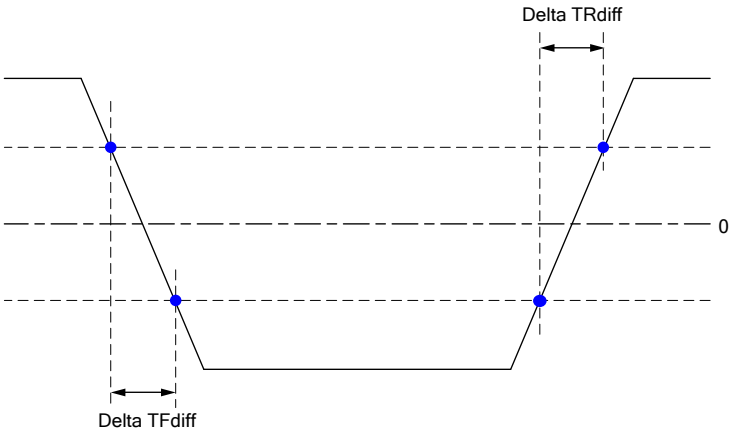


Figure 4 — Differential Output Slew Rate Definition

Table 15 — Differential Output Slew Rate for 0.6 V V_{DDQ}

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (VOH = V_{DDQ}*0.5)	SRQdiff†	6	18	V/ns
† SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals				

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC) = -0.8*VOH(DC) and VOH(AC) = 0.8*VOH(DC).

NOTE 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

5 V_{REF} Specifications

5.1 CA Internal V_{REF} Specifications

Table 16 — CA Internal V_{REF} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
V_{REF} Max operating point Range0	V_{REF}_max_R0	-	-	44.9%	V_{DDQ}	1,11
V_{REF} Min operating point Range0	V_{REF}_min_R0	15%	-	-	V_{DDQ}	1,11
V_{REF} Max operating point Range1	V_{REF}_max_R1	-	-	62.9%	V_{DDQ}	1,11
V_{REF}Min operating point Range1	V_{REF}_min_R1	32.9%	-	-	V_{DDQ}	1,11
V_{REF} Stepsize	V_{REF}_step	0.50%	0.60%	0.70%	V_{DDQ}	2
V_{REF}Set Tolerance	V_{REF}_set_tol	-11	0	11	mV	3,4,6
		-1.1	0	1.1	mV	3,5,7
V_{REF} Step Time	V_{REF}_time_Short	-	-	100	ns	8
	V_{REF}_time_Middle	-	-	200	ns	12
	V_{REF}_time_Long	-	-	250	ns	9
	V_{REF}_time_weak	-	-	1	ms	13,14
V_{REF} Valid tolerance	V_{REF}_val_tol	-0.10%	0.00%	0.10%	V_{DDQ}	10

NOTE 1 V_{REF} DC voltage referenced to V_{DD2}_DC.

NOTE 2 V_{REF} stepsize increment/decrement range. V_{REF} at DC level.

NOTE 3 V_{REF}_new = V_{REF}_old + n*V_{REF}_step; n= number of steps; if increment use "+"; if decrement use "-".

NOTE 4 The minimum value of V_{REF} setting tolerance = V_{REF}_new – 11 mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 11 mV. For n>4.

NOTE 5 The minimum value of V_{REF} setting tolerance = V_{REF}_new -1.1 mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 1.1 mV. For n≤ 4.

NOTE 6 Measured by recording the min and max values of the V_{REF} output over the range, drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 7 Measured by recording the min and max values of the V_{REF} output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for V_{REF}.

NOTE 9 Time from MRS command to increment or decrement V_{REF}min to V_{REF}max or V_{REF}max to V_{REF}min change across the V_{REF}CA Range in V_{REF} voltage.

NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.

NOTE 11 DRAM range 0 or 1 set by MR12 OP[6].

NOTE 12 Time from MRS command to increment or decrement more than one step size up to a full range of V_{REF} voltage withiin the same V_{REF}CA range.

NOTE 13 Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.

NOTE 14 V_{REF}_time_weak covers all V_{REF}(CA) Range and Value change conditions are applied to V_{REF}_time_Short/Middle/Long.

5.2 DQ Internal V_{REF} Specifications

Table 17 — DQ Internal V_{REF} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
V_{REF} Max operating point Range0	V_{REF}_max_R0	-	-	44.9%	V_{DDQ}	1,11
V_{REF} Min operating point Range0	V_{REF}_min_R0	15%	-	-	V_{DDQ}	1,11
V_{REF} Max operating point Range1	V_{REF}_max_R1	-	-	62.9%	V_{DDQ}	1,11
V_{REF} Min operating point Range1	V_{REF}_min_R1	32.9%	-	-	V_{DDQ}	1,11
V_{REF} Stepsize	V_{REF}_step	0.50%	0.60%	0.70%	V_{DDQ}	2
V_{REF} Set Tolerance	V_{REF}_set_tol	-11	0	11	mV	3,4,6
		-1.1	0	1.1	mV	3,5,7
V_{REF} Step Time	V_{REF}_time_Short	-	-	100	ns	8
	V_{REF}_time_Middle	-	-	200	ns	12
	V_{REF}_time_Long	-	-	250	ns	9
	V_{REF}_time_weak	-	-	1	ms	13,14
V_{REF} Valid tolerance	V_{REF}_val_tol	-0.10%	0.00%	0.10%	V_{DDQ}	10

NOTE 1 V_{REF} DC voltage referenced to V_{DDQ}_DC.

NOTE 2 V_{REF} stepsize increment/decrement range. V_{REF} at DC level.

NOTE 3 V_{REF}_new = V_{REF}_old + n*V_{REF}_step; n= number of steps; if increment use "+"; If decrement use "-".

NOTE 4 The minimum value of V_{REF} setting tolerance = V_{REF}_new – 11 mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 11 mV. For n>4.

NOTE 5 The minimum value of V_{REF} setting tolerance = V_{REF}_new – 1.1 mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 1.1 mV. For n≤ 4.

NOTE 6 Measured by recording the min and max values of the V_{REF} output over the range, drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 7 Measured by recording the min and max values of the V_{REF} output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for V_{REF}.

NOTE 9 Time from MRS command to increment or decrement V_{REF}min to V_{REF}max or V_{REF}fmax to V_{REF}min change across the V_{REF}DQ Range in V_{REF} voltage.

NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.

NOTE 11 DRAM range 0 or 1 set by MR14 OP[6].

NOTE 12 Time from MRS command to increment or decrement more than one step size up to a full range of V_{REF} voltage withiin the same V_{REF}DQ range.

NOTE 13 Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.

NOTE 14 V_{REF}_time_weak covers all V_{REF}(DQ) Range and Value change conditions are applied to V_{REF}_time_Short/Middle/Long.

6 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 18.

Table 18 — MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write and Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
V_{REF}(CA) Setting	MR12 OP[6]	1_B	V_{REF}(CA) Range[1] enabled
V_{REF}(CA) Value	MR12 OP[5:0]	011101_B	Range1: 50.3% of V_{DDQ}
V_{REF}(DQ) Setting	MR14 OP[6]	1_B	V_{REF}(DQ) Range[1] enabled
V_{REF}(DQ) Value	MR14 OP[5:0]	011101_B	Range1: 50.3% of V_{DDQ}

7 ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_C, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS and CA[5:0] signals. Generally, only one termination load will be present even if multiple devices are sharing the command signals. In contrast to LPDDR4 where the ODT_CA input is used in combination with mode registers, LPDDR4X uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In a multi rank system, the terminating rank should be trained first, followed by the nonterminating rank(s).

Table 19 — Command Bus ODT State

ODTE-CA MR11[6:4]	ODTD-CA MR22[5]	ODTF-CK MR22[3]	ODTF-CS MR22[4]	ODT State for CA	ODT State for CK_t/CK_c	ODT State for CS
Disabled[1]	Valid[2]	Valid[2]	Valid[2]	Off	Off	Off
Valid[2]	0	0	0	On	On	On
Valid[2]	0	0	1	On	On	Off
Valid[2]	0	1	0	On	Off	On
Valid[2]	0	1	1	On	Off	Off
Valid[2]	1	0	0	Off	On	On
Valid[2]	1	0	1	Off	On	Off
Valid[2]	1	1	0	Off	Off	On
Valid[2]	1	1	1	Off	Off	Off

NOTE 1 Default Value.

NOTE2 Valid" means "0 or 1".

8 Core Timing

Table 20 — Core Timing

Parameter	Symbol	Min/ Max	Data Rate							Unit
Core Parameters			**533**	**1066**	**1600**	**2133**	**2667**	**3200**	**3733**	**4266**	
Active bank-A to active bank-B[1]	tRRD	Min	Max(10ns, 4nCK)							Max (7.5ns, 4nCK)[2]	ns
Four bank ACT window	tFAW	Min	40							30[2]	ns

NOTE 1 Precharge to precharge timing restriction does not apply to Auto-Precharge commands.

NOTE 2 Devices supporting 4266 Mbps specification shall support these timings at lower data rates.

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