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Horizon Robotics

X3J3 DDR Tuning Guide

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1 Version

Version Number	Change List	Author	Date
0.1	Draft Version	Jeff.Chu	2020/12/27
0.2	Add trouble shooting and debug flow	Jeff.Chu	2020/12/28
0.3	Refine architecture of document Add Introduction of this document and the registers	Jeff.Chu	2021/1/7
0.4	Add CH2, 3, 4, and introduction of CH6	Jeff.Chu	2021/1/11
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0.8	1. remove PDN report 2. Add suggestion of PDN simulation	Jeff.Chu	2021/1/21
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2 Introduction

2.1 Objective

This DDR tuning guide provides the tuning guidelines and detailed definitions of DDR impedance registers. Following steps describe the DDR tuning guidelines:

A. Customers are encouraged to follow the PCB board level check list (described in Chapter 3) to avoid the discrepancies in the PCB design.
B. Customers are encouraged to use the memory components in the short list of recommended LPDDR/DDR chips (described in Chapter 4).
C. If both conditions could be met, the customers would have their PCB board up and running quickly by using the default DDR Register Settings provided by Horizon Robotics.
D. If customers want to fine tune DDR setting further, they could change DDR impedance register setting based on the following descriptions in this document.

2.2 Suggestion for Readers

If the user is familiar with DDR design, the user could try to change DDR impedance registers by themselves based on the default settings released by Horizon Robotics

2.3 Terms and Abbreviation

Abbreviation	Description
DDR	Double Data Rate SDRAM
LPDDR	Low Power Double Data Rate SDRAM
PHY	Physical (Port Physical Layer)
MR	Mode Register
ODT	On-Die-Termination

2.4 Relevant Manuals

1. AN-EN-2521-10-A-X3J3 Introduction to DDR partition and customized modification.docx

3 PCB Board Level Check List

Below is the PCB board level check list which provides the guidelines to customer's PCB design. The customers are encouraged to follow the PCB board level check list as these guidelines are verified by Horizon Robotics engineering team. The discrepancies of the PCB board level check list would increase the risk of DDR malfunctions. Under such circumstances, further customer support might be needed per the request. The customer's PCB board check list needs to be provided to Horizon Robotics prior to the call for customer support.

The SIPI simulation is essential to DDR4/LPDDR4 high speed design, the customers are encouraged to run the corresponding simulations prior to the PCB fabrication.

X3/J3 SOM	J3_02A	X3_01C	Customer Board
Board ID	2A-DV-SM-02A	2A-DV-SM-01C	
Base Material – part number	TU862	IT-180	
Base Material – DK value	3.71	4.3	
Base Material - DF value (1GHz)	0.013	0.0142	
Base Material - DF value (5GHz)	0.014	0.0154	
Base Material - DF value (10GHz)	0.015	0.0163	
DDR Line impedance	50ohm	50ohm	
DDR Line impedance tolerance	+/-10%	+/-10%	
PCB Layers	8	8	
PCB Vendor	兴森 / 牧泰莱 (MULTILAYER)	万龙精益 (WANLONGJINGYI)	
PCB DQ layout	0x2,0x1,0x7,0x0,0x5,0x3,0x4,0x6, 0x3,0x6,0x7,0x5,0x0,0x4,0x1,0x2, 0x4,0x0,0x1,0x2,0x7,0x3,0x6,0x5, 0x3,0x7,0x2,0x6,0x0,0x4,0x5,0x1,	0x2,0x1,0x7,0x0,0x5,0x3,0x4,0x6, 0x3,0x6,0x7,0x5,0x0,0x4,0x1,0x2, 0x4,0x0,0x1,0x2,0x7,0x3,0x6,0x5, 0x3,0x7,0x2,0x6,0x0,0x4,0x5,0x1,	
VAA power-up ramp rate (mV/us)	18.91mV/us	25.91mV/us	
VAA Power Management IC (for reference)	SPF5024AMMAMES	AXP15060 CLDO01	
VDDQ Resistor value	120	120	

VDDQ power-up ramp rate (mV/us)	14.81mV/us	1.39mV/us	
VDDQ Power Management IC (for reference)	MPQ2166GD-AEC1-Z	AXP15060 DCDC05	
VDDQ/VDDQLP Merge	No Power Merge	Power Merge	
Power Adapter	12V, 3A	12V, 3A	

4 Short list of recommended LPDDR/DDR chips

Below is the short list of recommended LPDDR/DDR chips which have been verified by Horizon Robotics engineering team. The customers are encouraged to use the memory components in the short list as well as to follow the PCB board level check list. If both conditions could be met, the customers would have their PCB board up and running quickly by using the default DDR Register Settings provided by Horizon Robotics.

LPDDR4:

Index	Vendor	Part Number	Data Rate	Operating Temperature	PCB Board
1	Micron	MT53D1024M32D4DT-046AAT	2666	-40 ~ 105℃	(2A-CV-BB-01)
2	Micron	MT53E1G32D2FW-046AUT:A	3200	-40 ~ 125℃	(2A-CV-BB-01)
4	Hynix	H9HCNNNBKUMLHR-NEO (H54G46BYYQX053)	2666 3200	-40 ~ 105℃	(2A-DV-SM-02A)
5	Hynix	H9HCNNN4KUMLHR-NMI	2666	-40 ~ 95℃	(2A-DV-SM-01A)
6	Samsung	K4F8E304HB-MGCJ	3200 3600	-25 ~ 85℃	(2A-DV-SM-01A)
7	Samsung	K4F6E3S4HM-MGCJ	3600	-25 ~ 85℃	(2A-DV-SM-01A)

DDR:

Index	Vendor	Part Number	Data Rate	Operating Temperautre	PCB Board
1	Micron	MT40A256M16LY-062E AIT	3200	-40 ~ 95℃	(X3-DV-SM-V02)
2	Samsung	K4A8G165WC-BCTD	2666	0 ~ 95℃	(X3-DV-SM-V02)
3	Samsung	K4A4G165WF	2666	-10 ~ 70℃	(X3-DV-SM-V02)

5 Introduction of impedance registers

The DDR PHY has registers that are used to configure, control or provide status of certain features of the PHY. The user accesses these registers using the configuration port write and read commands.
The following sections describe PHY impedance registers.

5.1 DDR PHY

Item	Register name	Description
1	ATxSlewRate	Set slew rates of address/command/memclk drivers
2	ATxImpedance	Set Tx impedance of Address driver cells
3	TxSlewRate	Set slew rates of the DQ/DQS drivers per nibble
4	TxOdtDrvStren	Set impedance value for Host ODT
5	TxOdtDrvStren	Set Tx impedance of DQ driver cells

5.2 DDR training firmware DMEM settings

Item	DDR type	Register name	Description
1	DDR4	MR1	The major impedance related bits of this register are bit 0, means DLL enable bit, bit 1, 2, meam Output driver impedance (ODI), and bit 8, 9, 10, mean Nominal ODT($R_{TT(NOM)}$).
2		MR2	The major impedance related bits of this register are bit 3, 4, 5, mean CWL(CAS Write Latency), and bit 9, 10, 11, mean Dynamic ODT($R_{TT(WR)}$).
3		MR5	The major impedance related bits of this register are bit 6, 7, 8, mean Parked ODT value ($R_{TT(Park)}$).
4	LPDDR4	MR3	The major impedance related bits of this register are bit 0, means PU-CAL (Pull-up calibration point), and bit 3, 4, 5, mean PDDS (Pull-down drive strength).
5		MR11	The major impedance related bits of this register are bit 0, 1, 2, mean DQ ODT, and bit 4, 5, 6, mean CA ODT.
6		MR22	The major impedance related bits of this register are bit 0, 1, 2, mean SOC ODT (controller ODT value for VOH calibration), and bit 4, ODTE-CS (CS ODT enabled for non-terminating rank).

6 Definition of impedance registers

6.1 DDR PHY registers

DDR PHY (Major IO) register has only 16 bits

6.1.1 ATxSlewRate

Bits	Name	Description	Access	Default
[3:0]	ATxPreP	4 bit binary trim for the driver pull up slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[7:4]	ATxPreN	4 bit binary trim for the driver pull down slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[10:8]	ATxPreDrvMode	Controls predrivers to adjust timing of turn-on and turn-off of pull-up and pull-down segments. - Recommended settings if the ANIB drives CK pins: -- DDR4 = 3'b000 -- LPDDR4 = 3'b001 - Recommended settings if the ANIB does not drive CK pins: -- DDR4 = 3'b011 -- LPDDR4 = 3'b001	R/W	0x7
[15:11]	Unimplemented	Returns zero on reads	R	0x0

6.1.2 AtxImpedance

Bits	Name	Description	Access	Default
[4:0]	ADrvStrenP	5 bit bus used to select the target pull up output impedance. Refer to Technology specific PHY Databook for supported options Connects to the DrvStren pins of the driver. 110_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 120R DRAM termination. LPDDR4 low- power drive into 240R DRAM termination at VOH=VDDQ/2.5 [1]. LPDDR4 low- power drive into 120R DRAM termination at VOH=VDDQ*35% [1] 100_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 60R DRAM termination. LPDDR4 low- power drive into 120R DRAM termination at VOH=VDDQ/2.5 [1]. LPDDR4 low- power drive into 60R DRAM termination at VOH=VDDQ*35% [1] 000_xx = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 40R DRAM termination. LPDDR4 low-power into 80R DRAM termination at VOH=VDDQ/2.5 [LPDDR4 low- power into 40R DRAM termination at VOH=VDDQ*35% [1] - 111_00 = 120R linear pull-up connected to VDDQ (DDR4, LPDDR4)	R/W	0x1f
[9:5]	ADrvStrenN	This 5- bit bus is used to select the target pull down output impedance. Refer to chnology specific PHY Databook for supported options. Connects to the DrvStren pins of the driver. xxx_00 = 120R pull-down (DDR4, LPDDR4/LPDDR4x)	R/W	0x1f
[15:10]	Unimplemented	Returns zero on reads	R	0x0

6.1.3 TxSlewRate

Bits	Name	Description	Access	Default
[3:0]	TxPreP	4 bit binary trim for the driver pull up slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[7:4]	TxPreN	4 bit binary trim for the driver pull down slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[10:8]	TxPreDrvMode	Controls predrivers to adjust timing of turn-on and turn-off of pull-up and pull-down segments. Recommended settings: - DDR4 = 3'b010. - LPDDR4 = 3'b001. - LPDDR4X = 3'b101.	R/W	0x7
[15:11]	Unimplemented	Returns zero on reads	R	0x0

6.1.4 TxOdtDrvStren

Bits	Name	Description	Access	Default
[5:0]	ODTStrenP	Selects the ODT pull-up impedance. Refer to Technology specific PHY Databook for supported options - 000_000 = HiZ - 001_000 = 120R pull-up connected to VDDQ (DDR4) - 011_000 = 60R pull-up connected to VDDQ (DDR4) - 111_000 = 40R pull-up connected to VDDQ (DDR4) Note: if any pull- up connected to VDDQLP is enabled, ODTStrenP value is ignored and a	R/W	0x00
[11:6]	ODTStrenN	Selects the ODT pull-down impedance. Refer to Technology specific PHY Databook for supported options - 000_000 = HiZ - 001_000 = 120R pull-down (LPDDR4/LPDDR4x) - 011_000 = 60R pull-down (LPDDR4/LPDDR4x) - 111_000 = 40R pull-down (LPDDR4/LPDDR4x)	R/W	0x00
[15:12]	Unimplemented	Returns zero on reads	R	0x0

6.1.5 TxImpedanceCtrl1

Bits	Name	Description	Access	Default
[5:0]	DrvStrenFSDqP	Refer to Technology specific PHY Databook for supported options. 6 bit bus used to select the target pull up output impedance. Connects to the DrvStren pins of the driver. xxx_110 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 120R DRAM termination. LPDDR4 low power drive into 240R DRAM termination at VOH=VDDQ/2.5 [1]. LPDDR4 low power drive into 120R DRAM termination at VOH=VDDQ*35% [1] xxx_100 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 60R DRAM termination. LPDDR4 low- power drive into 120R DRAM termination at VOH=VDDQ/2.5 [1]. LPDDR4 low- power drive into 60R DRAM termination at VOH=VDDQ*35% [1] xxx_000 = Non-linear pull-up to VDDQLP for the following modes: LPDDR4x into 40R DRAM termination. LPDDR4 low- power into 80R DRAM termination at VOH=VDDQ/2.5 [1]. LPDDR4 low- power into 40R DRAM termination at VOH=VDDQ*35% [1] 000_111 = HiZ - 001_111 = 120R linear pull-up connected to VDDQ (DDR4, LPDDR	R/W	0x3f
[11:6]	DrvStrenFSDqN	Refer to Technology specific PHY Databook for supported options. This 6-bit bus is used to select the target pull down output impedance. Connects to the DrvStren pins of the driver. 000_xxx = HiZ 001_xxx = 120R pull-down (DDR4, LPDDR4/LPDDR4x) 011_xxx = 60R pull-down (DDR4, LPDDR4/LPDDR4x) 111_xxx = 40R pull-down (DDR4, LPDDR4/LPDDR4x)	R/W	0x3f
[15:12]	Unimplemented	Returns zero on reads	R	0x0

6.2 DDR training firmware DMEM settings

DDR chips: Mode Register.

1 Mode Register 1 (MR1)

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 **001 = MR1** 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) 1 = Disabled (both ODI and RTT)
11	**Termination data strobe (TDQS) – Additional termination pins (x8 configuration only)** 0 = TDQS disabled 1 = TDQS enabled
10, 9, 8	**Nominal ODT (RTT(NOM) – Data bus termination setting** 000 = RTT(NOM) disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
7	**Write leveling (WL) – Write leveling mode** 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)

13, 6, 5	**Rx CTLE Control** 000 = Vendor Default 001 = Vendor Defined 010 = Vendor Defined 011 = Vendor Defined 100 = Vendor Defined 101 = Vendor Defined 110 = Vendor Defined 111 = Vendor Defined
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 1 [1] 10 = CL - 2 11 = Reserved
2, 1	**Output driver impedance (ODI) – Output driver impedance setting** 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

2 Mode Register 2 (MR2)

Mode Register	Description
11:9	**Dynamic ODT ($R_{TT(WR)}$) – Data bus termination setting during WRITEs** 000 = $R_{TT(WR)}$ disabled (WRITE does not affect R_{TT} value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (T_C: –40°C–85°C) 01 = Manual mode - Reduced operating temperature range (T_C: –40°C–45°C) 10 = Manual mode - Extended operating temperature range (T_C: –40°C–125°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1^tCK WRITE preamble** 000 = 9 (DDR4-1600) [1] 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600) [1] 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2^tCK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	**RFU** 0 = Must be programmed to 0 1 = Reserved
1:0	**RFU**

	0 = Must be programmed to 0 1 = Reserved

3 Mode Register 5 (MR5)

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 **101 = MR5** 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled 1 = Enabled
10	**Data mask (DM)** 0 = Disabled 1 = Enabled
9	**CA parity persistent error mode** 0 = Disabled 1 = Enabled
8:6	**Parked ODT value ($R_{TT(Park)}$)** 000 = $R_{TT(Park)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)

5	**ODT input buffer for power-down** 0 = Buffer enabled 1 = Buffer disabled
4	**CA parity error status** 0 = Clear 1 = Error
3	**CRC error status** 0 = Clear 1 = Error
2:0	**CA parity latency mode** 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400/2666) 011 = 6 clocks (DDR4-2933/3200) 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

4 Mode Register 3 (MR3)

Feature	OP	Definition
PU-CAL (Pull-up calibration point)	OP[0]	0b: V_{DDQ} × 0.6 1b: V_{DDQ} × 0.5 (default)
WR-PST(WR postamble length)	OP[1]	0b: WR postamble = 0.5 × ^{t}CK (default) 1b: WR postamble = 1.5 × ^{t}CK
PPRP (Post-package repair protection)	OP[2]	0b: PPR protection disabled (default) 1b: PPR protection enabled
PDDS (Pull-down drive strength)	OP[5:3]	000b: RFU 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 (default) 111b: Reserved
DBI-RD (DBI-read enable)	OP[6]	0b: Disabled (default) 1b: Enabled
DBI-WR(DBI-write enable)	OP[7]	0b: Disabled (default) 1b: Enabled

5 Mode Register 11 (MR11)

Feature	OP	Definition
DQ ODT DQ bus receiver on-die termination	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU
CA ODT CA bus receiver on-die termination	OP[6:4]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU

6 Mode Register 22 (MR22)

Function	OP	Data
SOC ODT (controller ODT value for V_{OH} calibration)	OP[2:0]	000b: Disable (default) 001b: R_{ZQ}/1 (Illegal if MR3 OP[0] = 0b) 010b: R_{ZQ}/2 011b: R_{ZQ}/3 (Illegal if MR3 OP[0] = 0b) 100b: R_{ZQ}/4 101b: R_{ZQ}/5 (Illegal if MR3 OP[0] = 0b) 110b: R_{ZQ}/6 (Illegal if MR3 OP[0] = 0b) 111b: RFU
ODTE-CK (CK ODT enabled for non-terminating rank)	OP[3]	ODT bond PAD is ignored 0b: ODT-CK enable (default) 1b: ODT-CK disable
ODTE-CS (CS ODT enabled for non-terminating rank)	OP[4]	ODT bond PAD is ignored 0b: ODT-CS enable (default) 1b: ODT-CS disable
ODTD-CA (CA ODT termination disable)	OP[5]	ODT bond PAD is ignored 0b: CA ODT enable (default) 1b: CA ODT disable
ODTD for x8_2ch (Byte) mode	OP[7:6]	See Byte Mode section

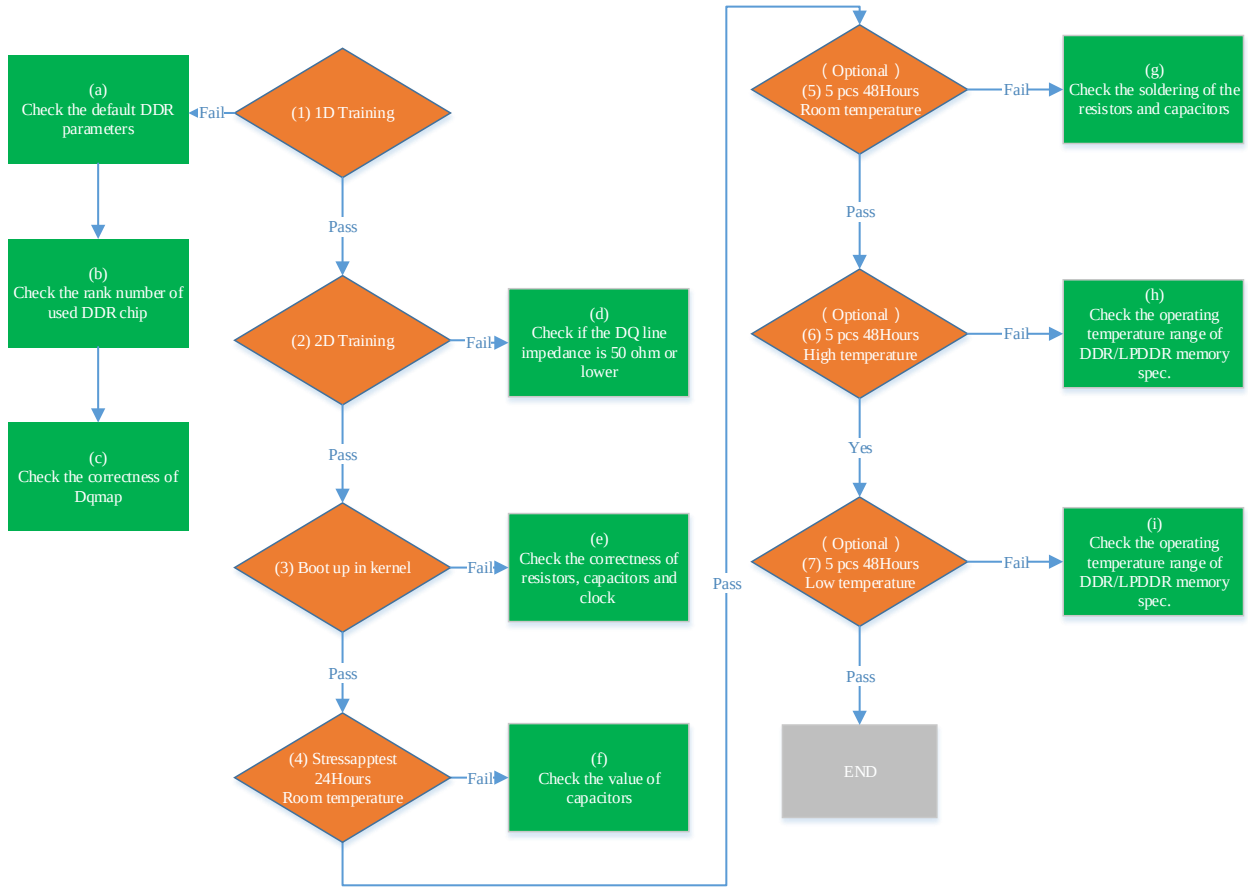
7 Trouble shooting of bringing up a new board

7.1 Introduction of DDR 1D/2D training

One dimensional training, or 1D training, is a group of training stages that optimize a system's delays at a set of user-provided reference voltages.
Two-dimensional training, or 2D training, is a group of training stages that can be run after 1D training to further refine the system's pstate 0 delay and voltage settings.

7.2 Debug flow chart

When bring up a board, you can check the correctness in following green rectangle based on the phenomenon (orange diamond) you encountered.



7.3 Detailed Debug steps description

The following table lists a detailed description of what to check.

Failed Step	Failed Phenomenon	Items to be check	Detail Descriptions
1	1D training fail	(a) Check the default DDR parameters	Check if use correct default DDR parameters from Horizon Robots' suggestion
		(b) Check the rank number of used DDR chip	Rank number=1, CsPresentChA & CsPresentChB of dmem setting is 0x1. Rank number=2, CsPresentChA & CsPresentChB of dmem setting is 0x3.
		(c) Check the correctness of Dqmap	Check the correctness of Dqmap connection in the schematic
2	2D training fail	(d) Check if the DQ line impedance is 50 ohm or lower	If the DQ line impedance is not 50 ohm, pls. refer to the DDR tuning guide to fine tune the registers corresponding to the changed impedance on the PCB
3	unable to boot up in kernel	(e) check the correctness of resistors, capacitors and clock	check the value and polarity of the resistors, capacitors and clock on the PCB board (LPDDR component area)
4	stressapptest room temperature 24 Hours fail	(f) check the value of capacitors	the value of the capacitors should follow the PDN simulation result if the suggested PCB schematic design is changed
5	stressapptest 5 pcs room temperature 48 Hour fail	(g) check the soldering of the resistors and capacitors	check if the resistors or capacitors on the PCB have solder empty, solder short or cold soldering. Also make sure there is no component shifted or missed.
6	stressapptest 5 pcs high temperature 48 Hour fail	(h) check the operating temperature range of DDR/LPDDR memory spec.	when the testing temperature is out of the DDR/LPDDR memory specification, the test will fail
7	stressapptest 5 pcs low temperature 48 Hour fail	(I) check the operating temperature range of DDR/LPDDR memory spec.	when the testing temperature is out of the DDR/LPDDR memory specification, the test will fail