JEDEC STANDARD

0.6 V Low Voltage Swing Terminated Logic (LVSTL06)

JESD8-29

DECEMBER 2016

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2016
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

0.6 V LOW VOLTAGE SWING TERMINATED LOGIC (LVSTL06)

(From JEDEC Board Ballot JCB-16-37, formulated under the cognizance of the JC-16 Committee on Interface Technology.

1 Scope

This standard defines power supply voltage range, dc interface, switching parameter and overshoot/undershoot for high speed low voltage swing terminated NMOS driver family digital circuits with 0.6V supply. The specifications in this standard represent a minimum set of interface specifications for low voltage terminated circuits.

The purpose of this standard is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. Class 1 describes low VOH (Nominal VOH = VDDQ*0.5) level terminated electrical characteristics. Class 2 describes high VOH (Nominal VOH = VDDQ*0.6) level terminated electrical characteristics.

2 LVSTL system definition

LVSTL (Low Voltage Swing Terminated Logic) Driver and ODT System LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in **Figure** 1.

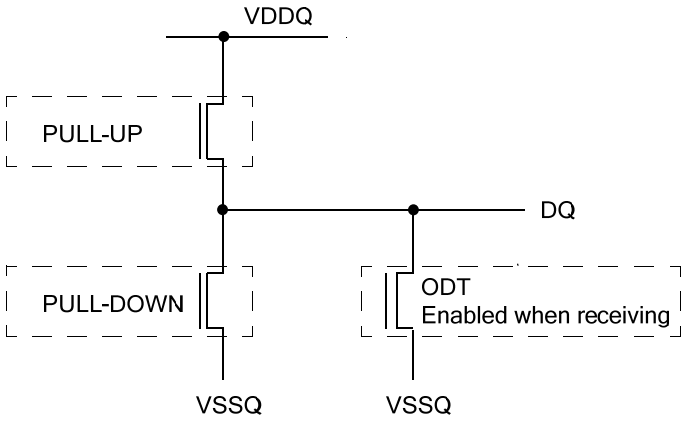


Figure 1 — LVSTL I/O Cell

2.1 Standard specifications

All voltages are referenced to ground except where noted.

2.2 Recommended DC Operating conditions

Table 1 — Recommended DC operating conditions

	Min	Nom	Max	Unit	
VDDQ	0.57	0.6	0.65	V	I/O Buffer Power

2.3 Pull Up Driver Characteristics for class 1 and class 2

Table 2 — Pull-Up Characteristics

VOH_{PU},nom	VOH(mV)			VOH_{PU}			Unit
	Min	Nom	Max	Min	Nom	Max	
Class 1 VDDQ*0.5	270	300	330	0.9	1	1.1	VOH, nom
Class 2 VDDQ*0.6	325	360	395	0.9	1	1.1	VOH, nom

2.4 Data Input Characteristics for class 1 and class 2

Input levels are same for both class 1 and class 2

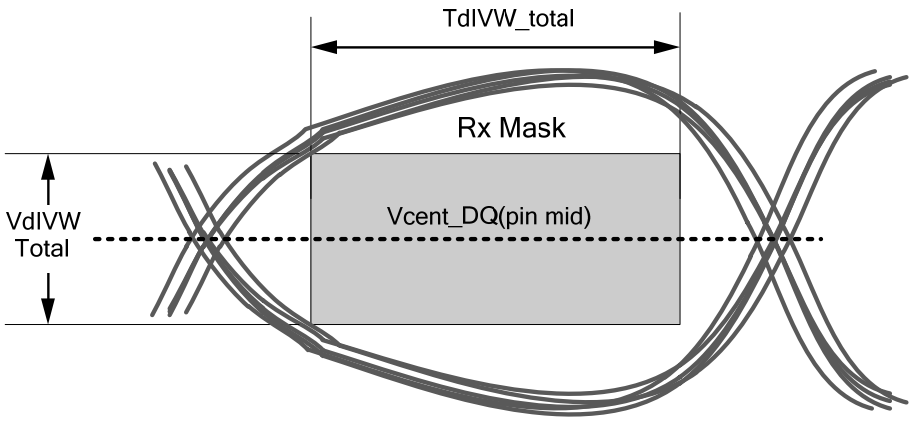
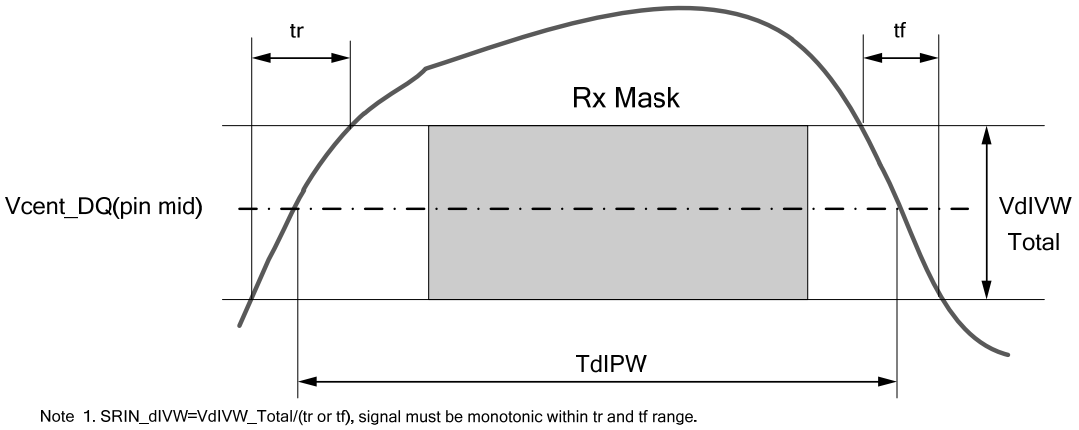


Figure 2 — DQ Receiver (Rx) mask

2.4 Data Input Characteristics for class 1 and class 2 (cont'd)



Note 1. SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 3 — DQ TdIPW definition (for each input pulse)

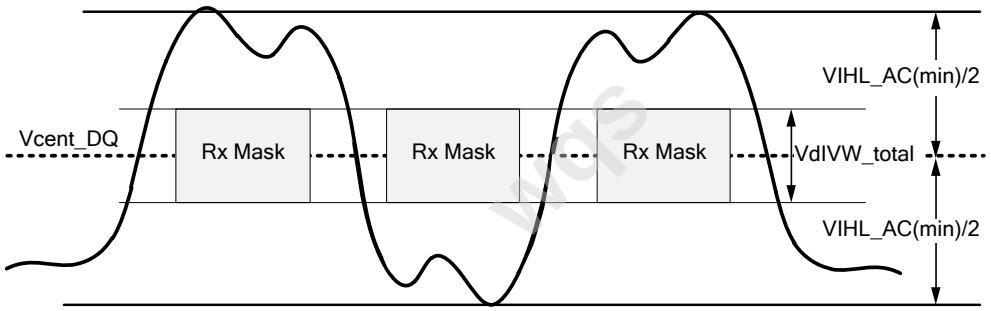


Figure 4 — DQ VIHL_AC definition (for each input pulse)

Table 3 — DQ Input Voltage

Symbol	Parameter	Range 1		Range 2		Unit
		Min	max	Min	max	
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	120	mV
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	170	-	mV
NOTE Each device specification defines Range 1 and Range 2 adaptation. Please refer to the device specification.						

2.5 CA Input Characteristics for class 1 and class 2

Input levels are same for both class 1 and class 2.

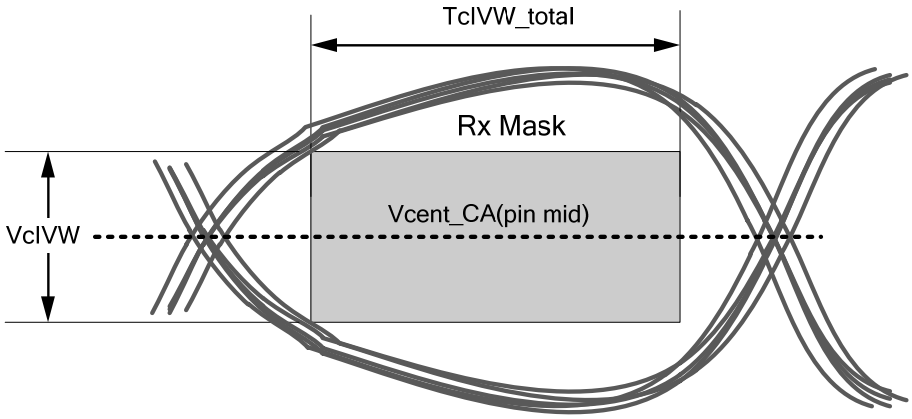
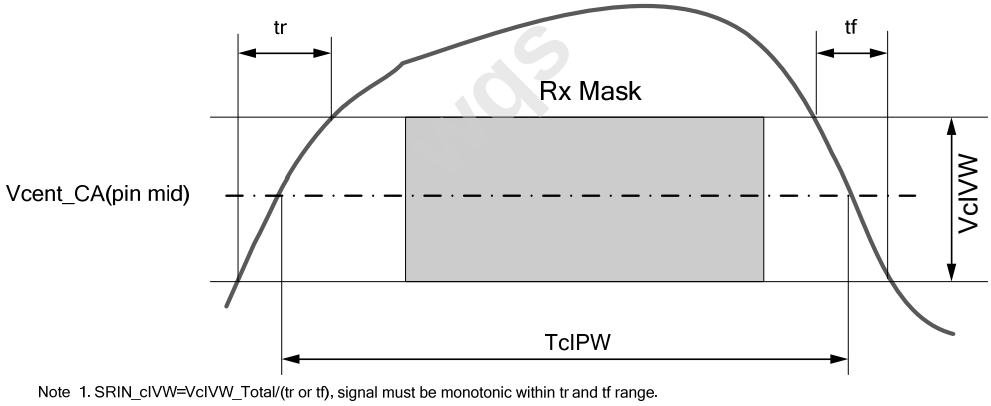


Figure 5 — CA Receiver(Rx) mask



Note 1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 6 — CA TcIPW definition (for each input pulse)

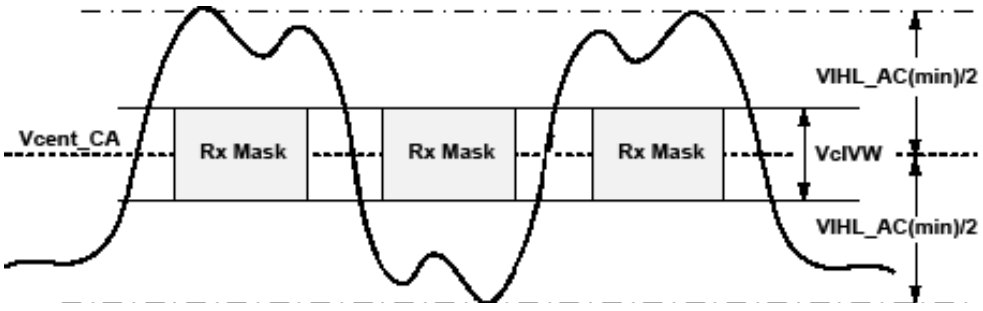


Figure 7 — CA VIHL_AC definition (for each input pulse)

2.5 CA Input Characteristics for class 1 and class 2 (cont'd)

Table 4 — CMD/ADR, CS voltage definitions

Symbol	Parameter	Range 1		Range 2		Range 3		Unit
		min	max	min	max	min	max	
VcIVW	Rx Mask voltage - p-p	-	175	-	155	-	145	mV
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	190	-	180	-	mV

NOTE Each device specification defines Range 1, Range 2, and Range 3 adaptations. Please refer to the device specification.

2.6 DQS Differential Input Cross Point Voltage

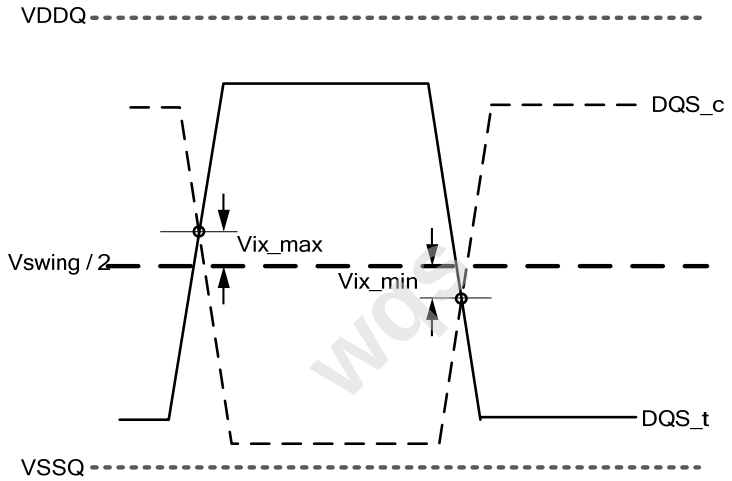


Figure 8 — DQS input Crosspoint voltage (Vix)

Table 5 — DQS input voltage crosspoint(Vix) ratio

Parameter	Symbol	Min	Max	Units	Notes
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	20	%	1,2

NOTE 1 The Vix voltage is referenced to Vswing/2(avg) = 0.5(VDQS_t + VDQS_c) where the average is over **TBD**[1] UI.

NOTE 2 The ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (Vix_DQS/Vdiff DQS pkpk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|

[1] At time of publication the formulating committee has not defined the value.

2.7 Clock Differential Input Cross Point Voltage

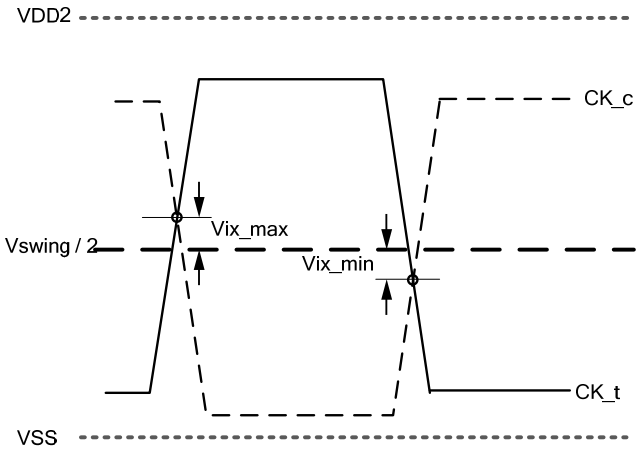


Figure 9 — CK input Crosspoint voltage (Vix)

Table 6 — CK input voltage crosspoint (Vix) ratio

Parameter	Symbol	Min	Max	Units	Notes
Clock Differential input crosspoint voltage ratio	Vix_CK_ratio	-	25	%	1,2
NOTE 1 The Vix voltage is referenced to Vswing/2(avg)= 0.5(VCK_t + VCK_c) where the average is over **TBD**[2] UI. NOTE 2 The ratio of the Vix pk voltage divided by Vdiff_CK : Vix_CK_Ratio = 100* (Vix_CK/Vdiff CK pk-pk) where VdiffCK pk-pk = 2*|VCK_t - VCK_c|					

2.8 Internal Reference Voltage Ranges

LVSTL interface use internal generated Reference Voltage (Vref) for single ended signals. Vref Range should be min 15% of VDDQ to 62.9% of VDDQ. Internal Vref should be adjusted to suitable value.

At time of publication the formulating committee has not defined the value.

[2] At time of publication the formulating committee has not defined the value.

2.9 Overshoot and Undershoot

Table 7 — AC Overshoot/Undershoot Specification

Parameter			Units
Maximum peak amplitude allowed for overshoot area. (See Figure 10)	Max	0.3	V
Maximum peak amplitude allowed for undershoot area. (See Figure 10)	Max	0.3	V
Maximum area above VDD. (See Figure 10)	Max	0.1	V-ns
Maximum area below VSS. (See Figure 10)	Max	0.1	V-ns
NOTE 1 VDD2 stands for VDD for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c. NOTE 2 VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c. NOTE 3 Maximum peak amplitude values are referenced from actual VDD and VSS values. NOTE 4 Maximum area values are referenced from maximum operating VDD and VSS values.			

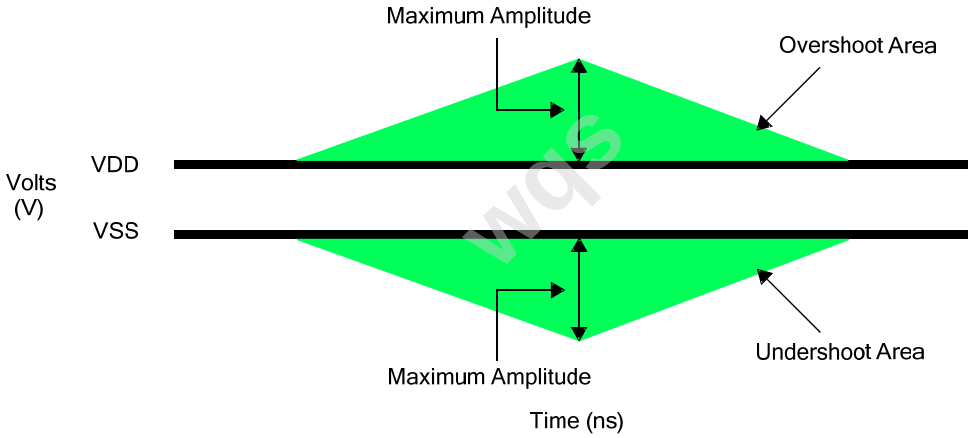


Figure 10 — Overshoot and Undershoot Definition

Standard Improvement Form JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____

Rev. 8/13