Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

DFI PHY Timing Monitor
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

DFI PHY Timing Monitor

1. Introduction

The Verilog based DFI PHY timing monitor is designed to work in Cadence DFI PHY IP simulation environment as well as other DFI PHY simulation environments. The monitor is intended to help users measure during simulation the timing parameters which are to be used in the Cadence Palladium DFI PHY emulation model (MMP DFI PHY model).

The I/O interface of the timing monitor is designed and named according to the DFI PHY 4.0 standard specification.

This timing monitor is configurable; it can be configured to meet a range of customer design requirements. Please follow the configuration instructions in the following sections of this user guide.

Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

2. Support List

The following table provides all the supported/unsupported features in the monitor.

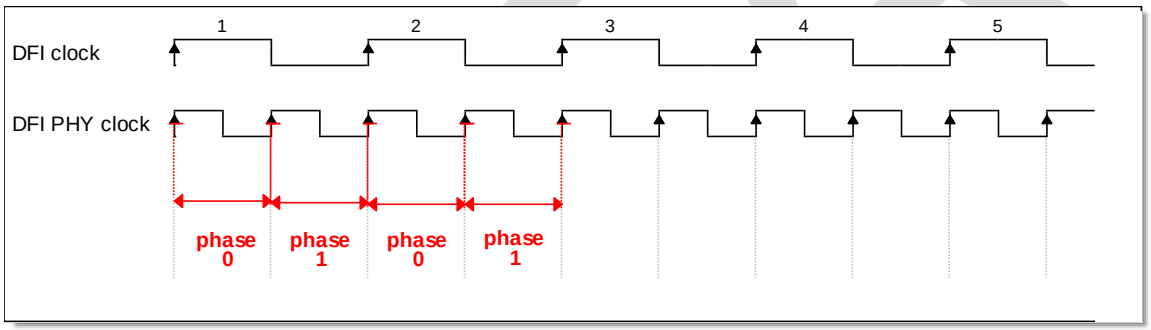
Table 1: Supported Configurations and Memory Types

Configurations	Support
Memory Types	
DDR3	Yes
DDR4	Yes
LPDDR3	Yes
LPDDR4	No
Configurations	
Frequency ratio 1:1 system	Yes
Frequency ratio 1:2 system	Yes
Frequency ratio 1:4 system	No
Cadence DFI controller	Yes
Other DFI controllers	Yes

3. Limitations and Assumptions

Several assumptions about the scenario and simulation conditions are made in order to constrain the monitor calculations practically.

- This monitor can **ONLY** be used in simulation. The monitor may be yield invalid results when used in emulation.
- Most users work with a 1:2 frequency ratio system. 1:2 frequency ratio system users **MUST** connect two **phase aligned** clocks in a 1:2 frequency ratio to the ports DFI_CLK and PHY_CLK of monitor. The clock relationship is shown below.



- Only 1:1 and 1:2 DFI PHY frequency ratio systems are supported by this monitor.
- In 1:2 frequency ratio systems, users need to send commands, data, and enable signals on both phases
- For DDR3 and DDR4 measurements, users need to **NOT** use the configuration for burst length called “BC on the fly”
- Users need to send multiple read and write commands to make sure monitor can acquire the timing parameters successfully. Cadence strongly recommends users to send at least tens of read or write commands in one test.
- If the user is **NOT** using a Cadence DFI controller, the parameter *CDNS_CONTROLLER_EN* should be SET to “0”. The default value of *CDNS_CONTROLLER_EN* in this monitor is “1”
- During write operations, the user must **NOT** send all “0”s or all “1”s or any other like-valued data in one burst write on the bus *dfi_wrdata_px*
- If there are only few changes of the enable signals during the period of the test, the monitor may **NOT** be able to successfully calculate the correct timing parameters. For example, if the signals *dfi_rddata_en_px* and/or *dfi_wrdata_en_px* remain HIGH for a long time, the monitor may not be able to calculate the correct parameter values. Such conditions can

typically occur during continuous and gapless reads or writes. It is recommended that the user structure the test for this monitor to include adequate enable signal value changes. **NOTE: We strongly recommend users make the controller send individual write bursts and read commands.**

- This monitor does **NOT** support t_ctrl_delay = ‘0’. If “t_ctrl_delay” equals a value of “0” in a simulation test, this monitor may NOT get the correct value --- “0”. This condition is deemed unlikely since such a scenario has not been observed to date.

4. Monitor Configuration

All parameters and configurations of the DFI PHY Timing Monitor are controlled in the model using Verilog parameters or defines. The following sections provide an overview of the user adjustable parameters, the exposed localparams, and the Verilog defines and then treat each adjustable parameter and define in more detail

4.1. Overview of User Adjustable Parameters and Non adjustable Localparam

The following tables provide details on the **user adjustable** parameters for the DFI PHY timing monitor. These parameters may be modified when instantiating the monitor.

Table 2: Description of User Adjustable Parameters

User Adjustable Parameter	Default Value	Description
CDNS_CONTROLLER_EN	1	This parameter setting indicates if the user is using a Cadence controller or not. If the user is using another company's controller, set the value to "0"
MEM_TYPE	0	This parameter MUST be set to a valid value when instantiating the monitor. 1: DDR 2: DDR2 3: DDR3 4: DDR4 11: LPDDR (mobile DDR) 12: LPDDR2; 13: LPDDR3; 14: LPDDR4 Other values: Not supported.
MONITOR_DISPLAY_PERIOD	10000	The period to print timing parameters, measured by PHY_CLK
mem_data_bits	32	This parameter is used to define the width of the memory interface data bus.
dfi_addr_bits	20	This parameter is used to define the width of the DFI PHY interface address bus. If LPDDR2/3 is being used then this should be set to 20bits wide as the CA bus is DDR (double data rate) of 10bits. LPDDR4 uses a 6-bit SDR (single data rate) CA bus and consequently there is a direct mapping from CA[5:0] to dfi_address[5:0]
dfi_bank_addr_width	3	This parameter is used to define the width of the DFI PHY interface bank bus and is only required for the DDRx models.

dfi_bg_addr_width	2	This parameter is used to define the width of the DFI PHY interface bank group bus. It is only required for model DDR4.
dfi_cs_width	4	This parameter is used to define the width of the DFI PHY chip select bus.
mem_ca_bits	10	This parameter is used to define the width of the memory interface bus for LPDDR2/3/4 implementations. It is not used for DDRx models. This parameter should be set to 10bits for LPDDR2/3 and be set to 6bits for LPDDR4.
t_DQSCK_in_LPDDRx	1	This parameter is used only with LPDDR2 / LPDDR3 / LPDDR4. The value MUST be the same as the value that the user sets in the MMP memory models. The default value is “1” in MMP models and users rarely change the value.

The following table provides some information about exposed localparams that are NOT user adjustable. On rare occasion the user may find one of these localparam needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

Table 3: Description of Visible Localparams

Localparam	Default Value	Description
mem_data_byte_width	8	Data byte width
mem_num_bytes	4	(mem_data_bits + (mem_data_byte_width - 1)) / mem_data_byte_width
dfi_data_bits	64	mem_data_bits * 2
dfi_num_bytes	8	mem_num_bytes * 2
ok_threshold	3	The number of times which monitor gets the same value of parameter CONTINUOUSLY. When the threshold is reached, OK flags will be pulled up.
abnormal_threshold	3	The times of abnormal values which monitor gets. When the threshold is reached, OK flags will be pulled down
wrdata_shift_depth	10	The maximum value of t_wrdata_en the monitor supports
DQ_wrdata_shift_depth	8	The maximum value of burst length the monitor supports. Maximum BL is (DQ_wrdata_shift_depth * 2)

5. I/O Ports and Connection of Monitor

Connection:

The buses connecting between the controller and PHY as well as the buses connecting between the PHY and memory are all input ports in the timing monitor.

The measured timing parameters and the corresponding OK flags are output ports of the monitor.

On the controller-PHY side, the connectivity is identical to the expected connectivity between the controller and the Palladium MMP DFI PHY model. Detailed information about this connectivity is covered in the Palladium DFI PHY model user guide--- *DFI_PHY_4.0_Model.pdf.*

On PHY-memory side, the connectivity is identical to the expected connectivity between the Palladium MMP DFI PHY model and the Palladium MMP DDR/LPDDR memory model. Detailed information about this connectivity is covered in the Palladium DFI PHY model user guide--- *DFI_PHY_4.0_Model.pdf.*

The names of the monitor ports are the same as on the ports of the Palladium MMP DFI PHY model. Some ports of the Palladium MMP DFI PHY model are not useful for the timing monitor and these ports are not included in the monitor interface.

The description for each of the I/O ports for the timing monitor is shown in the table below.

Table 4: Description of I/O Port

Port Name	Direction	Description
Interfaces between Controller and PHY		
DFI_CLK	Input	DFI clock, which is also the main clock of controller
PHY_CLK	Input	DFI PHY clock. In 1:2 and 1:4 frequency ratio systems, the frequency of this PHY_CLK clock is a multiple of the DFI_CLK frequency
RST_N	Input	Asynchronous reset of PHY model and monitor
dfi_cs_pN	Input	DFI chip select buses. They will be transformed into CS buses to memory.
dfi_address_pN	Input	DFI address buses. In DDR models they will be transformed into address buses to the memory. In LPDDR models they will be transformed into CA buses.
dfi_ras_n_pN	Input	DFI command control buses. Only valid with DDR models. Not used with LPDDR models.
dfi_cas_n_pN	Input	DFI command control buses. Only valid with DDR models. Not used with LPDDR models.

Port Name	Direction	Description
dfi_we_n_pN	Input	DFI command control buses. Only valid with DDR models. Not used with LPDDR models.
dfi_cke_pN	Input	DFI clock enable buses.
dfi_act_n_pN	Input	DFI command control buses. Only valid with DDR4 model.
dfi_bg_pN	Input	DFI bank group buses. Only valid with DDR4 model.
dfi_wrdata_pN	Input	DFI write data. Users are constrained to NOT to send all “0”s or all “1”s or other like-valued data in one burst write. See section of this user guide on Limitations and Assumptions.
dfi_wrdata_en_pN	Input	Enable signals for write data.
dfi_rddata_en_pN	Input	Enable signals for read data.
dfi_rddata_wN	Input	Read out data which is goes from the memory model then through the PHY model and finally is sent to controller.
dfi_rddata_valid_wN	Input	Signals which indicate the valid read out data.
dfi_freq_ratio	Input	Indicates the frequency ratio of current system. 2’b00 stands for 1:1 2’b01 stands for 1:2 2’b10 stands for 1:4
dfi_init_complete	Input	Indicates that the initialization is completed in PHY model. Also an indication that the monitor is going to work.
Interfaces between PHY and Memory		
MEM_DQ	Input	DQ buses sent from DFI model to memory side
MEM_DQS	Input	DQS buses sent from DFI model to memory side
MEM_CK	Input	Clock sent from DFI model to memory side
MEM_CKE	Input	Clock enable buses sent from DFI model to memory side
MEM_CS	Input	Chip select buses sent from DFI model to memory side
MEM_RESET_N	Input	Reset signal sent from DFI model to memory side. Only valid in DDR4 memory
MEM_RAS_N	Input	Command control buses sent from DFI model to memory side. Only valid with DDR models.
MEM_CAS_N	Input	Command control buses sent from DFI model to memory side. Only valid with DDR models.
MEM_WE_N	Input	Command control buses sent from DFI model to memory side. Only valid with DDR models.
MEM_BA	Input	Bank bus sent from DFI model to memory side. Only valid with DDR models.
MEM_ADDR	Input	Address bus sent from DFI model to memory side. Only valid with DDR models.
MEM_CA	Input	CA bus sent from DFI model to memory side. Only valid with LPDDR models.
MEM_BG	Input	Bank group bus sent from DFI model to memory side. Only valid with DDR4.
MEM_ACT_N	Input	Command control bus sent from DFI model to memory side. Only valid with DDR4.
Measured Timing Parameters		

Port Name	Direction	Description
t_ctrl_delay_ok	Output	Indicates that measuring of the corresponding timing parameter is complete.
t_ctrl_delay	Output	Delay from DFI interface control to memory interface control. Measured in DFI clock cycles
t_phy_wrdata_ok	Output	Indicates that measuring of the corresponding timing parameter is complete.
t_phy_wrdata	Output	Delay from wrdata_en assert until first wrdata value. Measured in PHY clock cycles
t_wrlat_adj_ok	Output	Indicates that measuring of the corresponding timing parameter is complete.
t_wrlat_adj	Output	Adjustment between PD model and DUT PHY write latency, measured in PHY clock cycles
t_rddata_en_adj_ok	Output	Indicates that measuring of the corresponding timing parameter is complete.
t_rddata_en_adj	Output	Adjustment between PD model and DUT PHY read latency, measured in PHY clock cycles
t_shift_p1_adjust_delay_ok	Output	Indicates that measuring of the corresponding timing parameter is complete. **This signal is not used when users are using a Cadence controller.**
t_shift_p1_adjust_delay	Output	Adjustment for P0/P1 timing mismatch. **This parameter is not used when users are using a Cadence controller.**
t_shift_p1_adjust_delay_wr_ok	Output	Indicates that measuring of the corresponding timing parameter is complete. **This signal is not used when users are using a Cadence controller.**
t_shift_p1_adjust_delay_wr	Output	Adjustment for P0/P1 timing mismatch**. This parameter is useless when users are using Cadence controller.**
t_phy_wrlat_ok	Output	Indicates that measuring of the corresponding timing parameter is complete. This port is used for debugging.
t_rddata_en_ok	Output	Indicates that measuring of the corresponding timing parameter is complete. This port is used for debugging.

Users can read the MMP DFI PHY model user guide to learn more details about the various timing parameters.

6. Procedure

The following steps are needed to obtain DFI PHY parameters for use in emulation with the MMP DFI PHY model.

- Connect the DFI PHY timing monitor module to the PHY Controller and PHY IP as described in sections above. For example, in the simulation environment with Cadence controller and PHY IP, all the “dfi_xxx” ports on monitor are connected to the similar “dfi_xxx” ports on controller. All the “MEM_xxx” ports on monitor are connected to “pad_mem_xxx” ports on PHY IP.

- Add the protected *.vp file called *mmp_dfi_timing_monitor.vp* to the simulation build and run.

- Run the targeted simulation test that meets the constraints listed in the “Limitations and Assumptions” section of this user guide. Be sure to dump a waveform database that includes timing monitor signals.

- Examine relevant signals in the waveform. The parameter is not valid unless the corresponding *_ok signal is asserted high by test completion. Some parameters can be measured independently of other parameters. For example, users can get t_rddata_en_adj parameter after sending read commands only, independently of and without need for write commands. For users of the Cadence DFI Controller these signals include:

    - t_ctrl_delay_ok
    - t_phy_wrdata_ok
    - t_wrlat_adj_ok
    - t_rddata_en_adj_ok
    - t_phy_wrlat_ok (only for debugging)
    - t_rddata_en_ok (only for debugging)

- For users of other DFI Controllers, these signals include:
    - t_ctrl_delay_ok
    - t_phy_wrdata_ok
    - t_wrlat_adj_ok
    - t_rddata_en_adj_ok
    - t_phy_wrlat_ok (only for debugging)
    - t_rddata_en_ok (only for debugging)
    - t_shift_p1_adjust_delay_ok
    - t_shift_p1_adjust_delay_wr_ok

- The parameter value for each parameter corresponding to its *_ok signal may be considered valid after the corresponding *_ok signal is asserted. Please see the I/O Port table above for a complete list of measured timing parameter ports/signals.

- t_phy_wrdata is a special parameter. In complicated corner cases, this monitor MAY calculate an incorrect value even if the corresponding *_ok flag is asserted HIGH. For Cadence IP users, please double check this parameter in configuration file, usually the parameter is called “TDFI_PHY_WRDATA” in the file “regconfig.h.sim_CTL”. For users of other DFI controllers, please double check the value in an equivalent configuration files.

- Read the parameter values and use them when instantiating the appropriate DFI PHY wrapper and model in emulation that include the DFI PHY and DDR / LPDDR.

- This timing monitor is in BETA phase. Please maintain a record of the simulation test and a dumped waveform database with all signals internal to the timing monitor included in the database. If issues arise please be prepared to share the waveform database with Cadence.

7. Timing Parameter Debug Display

Users have the option to make the monitor print out captured timing parameters by adding "+MMP_DEBUG_DISPLAY" in runtime commands.

As an example usage in a Cadence Denali simulation environment users need to add "+MMP_DEBUG_DISPLAY" in runtime commands as shown below:

ncverilog +access+rw **+MMP_DEBUG_DISPLAY** +nctimescale+10ps/1ns –l run.log

Typically in this environment the file to be modified is named "pattern.v" for each test case. For example --- /sim/axi_dac_wr/pattern.v

The displayed messages are shown as:

```
**********************************************

MMP DFI TIMING MONITOR PARAMETERS REPORT

TIME: 17640.00 ns; MMP DFI TIMING MONITOR: t_ctrl_delay is captured! t_ctrl_delay = 1

TIME: 17640.00 ns; MMP DFI TIMING MONITOR: t_phy_wrdata is captured! t_phy_wrdata = 2

TIME: 17640.00 ns; MMP DFI TIMING MONITOR: t_wrlat_adj is captured! t_wrlat_adj = 1

TIME: 17640.00 ns; MMP DFI TIMING MONITOR: t_rddata_en_adj is captured!
t_rddata_en_adj = 3

**********************************************
```

This set of messages will be printed periodically, controlled by the parameter "MONITOR_DISPLAY_PERIOD".

8. Revision History

The following table shows the revision history for this document.

Date	Version	Revision
June 2015	1.0	Initial release. support DDR3/DDR4/LPDDR3 support Cadence controllers and other controllers support 1:1 and 1:2 system
January 2016	1.1	Update for Palladium-Z1 and VXE
March 2016	1.2	Add more information about monitor test scenario constraints and recommendations
May 2016	1.3	Add information about debug display for timing parameters
July 2016	1.4	Remove hyphen in Palladium naming
January 2018	1.5	Modify header and footer