Technical Note

LPDDR5 Clocking

Background

The LPDDR5 clocking scheme differs from LPDDR4 in how they control command/address (CA) and data ciruits: LPDDR4 uses CK_t/CK_c signals to control both CA and data circuits, but LPDDR5 uses CK_t/CK_c signals for the CA circuit and WCK_t/WCK_c signals for the data circuit.

LPDDR5 CK speed is slow (800 MHz MAX) and WCK speed is fast (3200 MHz MAX). 800 MHz is enough for CK to support the required CA command band width, but WCK must be faster to support 6400 Mb/s MAX for DDR data input/output.

The WCK to CK ratio is 4:1 for high data rate operation; WCK to CK is 2:1 for low data rate operation. By using WCK:CK = 2:1, enough command band width can be achieved for low data rate operation.

The primary purpose of splitting the CA and data clocks in LPDDR5 is to reduce power consumption. High-speed WCK runs only during read/write traffic, but low-speed CK runs continuously except during power-down mode or deep-sleep mode. Reducing the frequency for a clock that is always running and using a high-speed clock only during read/write traffic can reduce clock circuit power consumption.

Table 1: LPDDR4/LPDDR5 Clocking Comparison

	LPDDR4/LPDDR4X	LPDDR5
CA circuit clock	CK_t/CK_c (2133 MHz MAX)	CK_t/CK_c (800 MHz MAX)
CA	CA[5:0] (SDR input)	CA[6:0] (DDR inpuit)
Data circuit clock	CK_t/CK_c (2133 MHz MAX)	WCK_t/WCK_c (3200 MHz MAX)
DQ, DMI	DDR I/O (4266 Mb/s MAX)	DDR I/O/(6400 Mb/s MAX)

Figure 1: Example of Block Diagram System

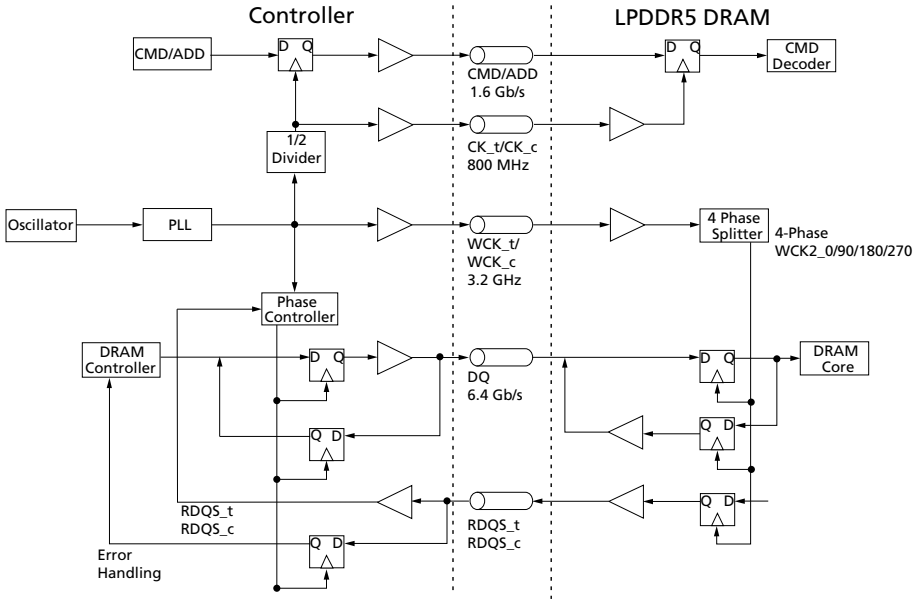


Table 2: Example of LPDDR5 Clock and Interface Signal Frequency Relationship (WCK:CK = 4:1)

Pin	Speed	Unit
CK_t, CK-c	0.8	GHz
Command/Address	1.6	Gb/s per pin
WCK_t, WCK_c	3.2	GHz
DQ, DMI	6.4	Gb/s per pin
RDQS_t, RDQS_c	3.2	GHz

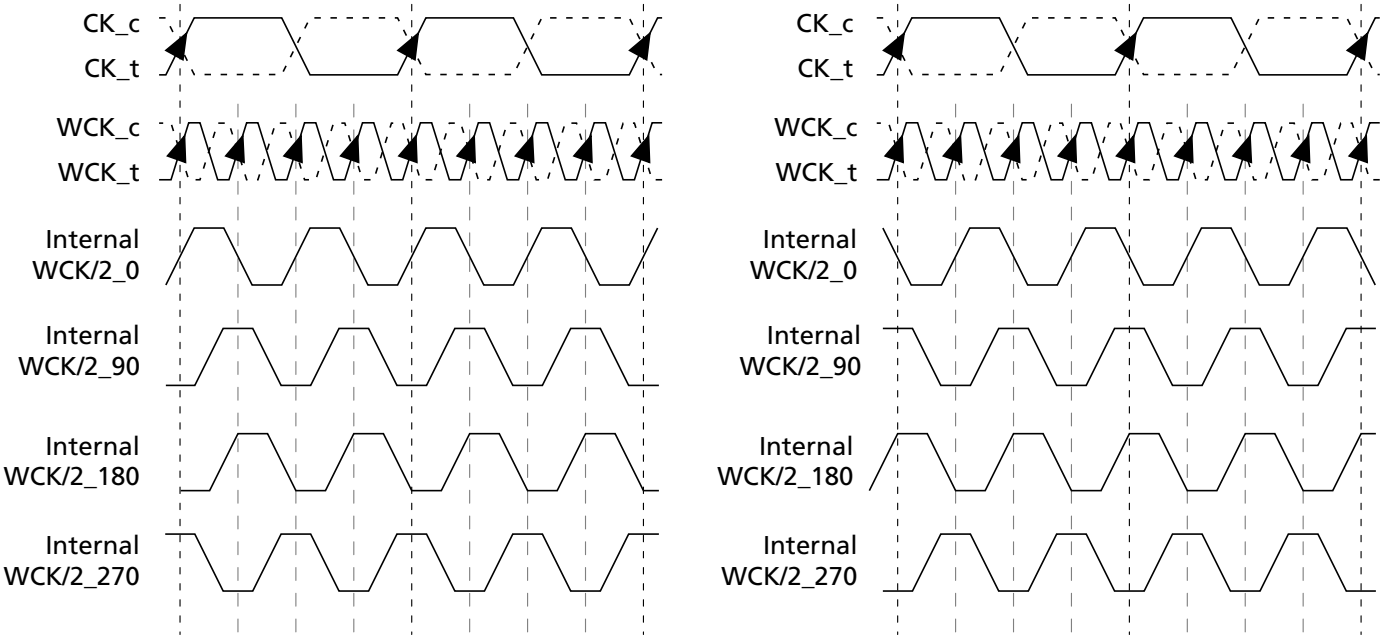
LPDDR5 WCK synchronization

WCK2CK Synchronization

LPDDR5 WCK frequency is four times or twice higher than CK frequency, requiring a device to have a clock divider in the WCK clock tree. By dividing WCK, the operation speed of the device's internal circuits in the WCK domain is reduced to half. However, the WCK divider initial state is unpredictable and results in two different states in device:

1. Aligned with CK state.
2. Misaligned with CK state.

Figure 2: WCK2CK Alignment (Left Figure is Aligned, Right Figure is Misaligned)



The latency control unit inside the device performs clock domain change of WRITE or READ commands from CK domain to WCK domain. For error-free latency control, the latency control circuit must know whether the device is in aligned with CK state or misaligned with CK state. A device is able to reset or detect its state by a process called WCK2CK synchronization. When a device controller issues a CAS command with WCK2CK sync selected, it must provide the device with half frequency WCK pulse to relax ISI (inter-symbol interference) and the timing margin. The device will then synchronize WCK to CK. This operation is defined as WCK2CK synchronization.

CAS Command With WCK2CK Synchronization Bits

The WCK2CK synchronization process is initiated by a CAS command with the appropriate bit enabled. A CAS command with WCK2CK synchronization should be issued before the WRITE or READ command. The Command Truth Table shows the CAS command with WCK2CK synchronization bits (WS_WR, WS_RD, WS_FS). A CAS command

with one set for any of the WCK2CK sync flag bits informs the device that WCK2CK sync is required.

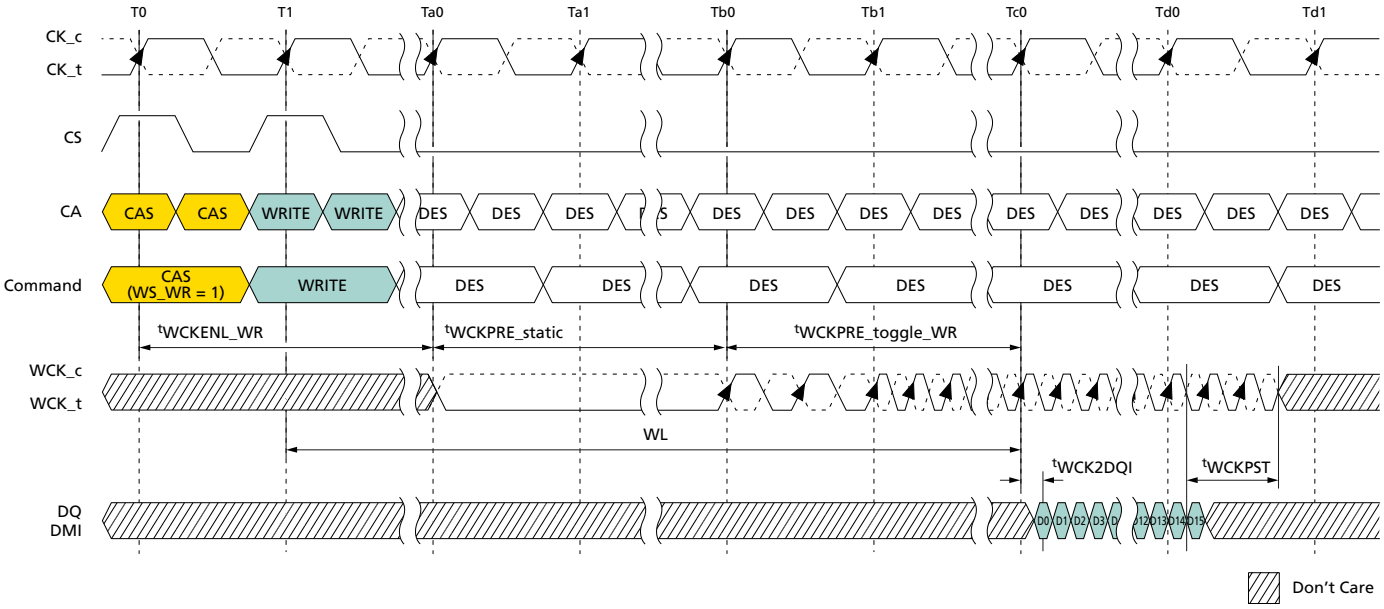
The reason there are 3 different WCK2CK synchronization bits is that WCK2CK synchronization pattern position is different between those 3 cases.

Table 3: CAS Command Truth Table

Command	BK ORG (BG/ 16B/8B)	SDR CMD Pin CS	DDR COMMAND PINS							CK Edge
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS	R1
	Any	X	DC0	DC1	DC2	DC3	WRX	WXS	B3	F1

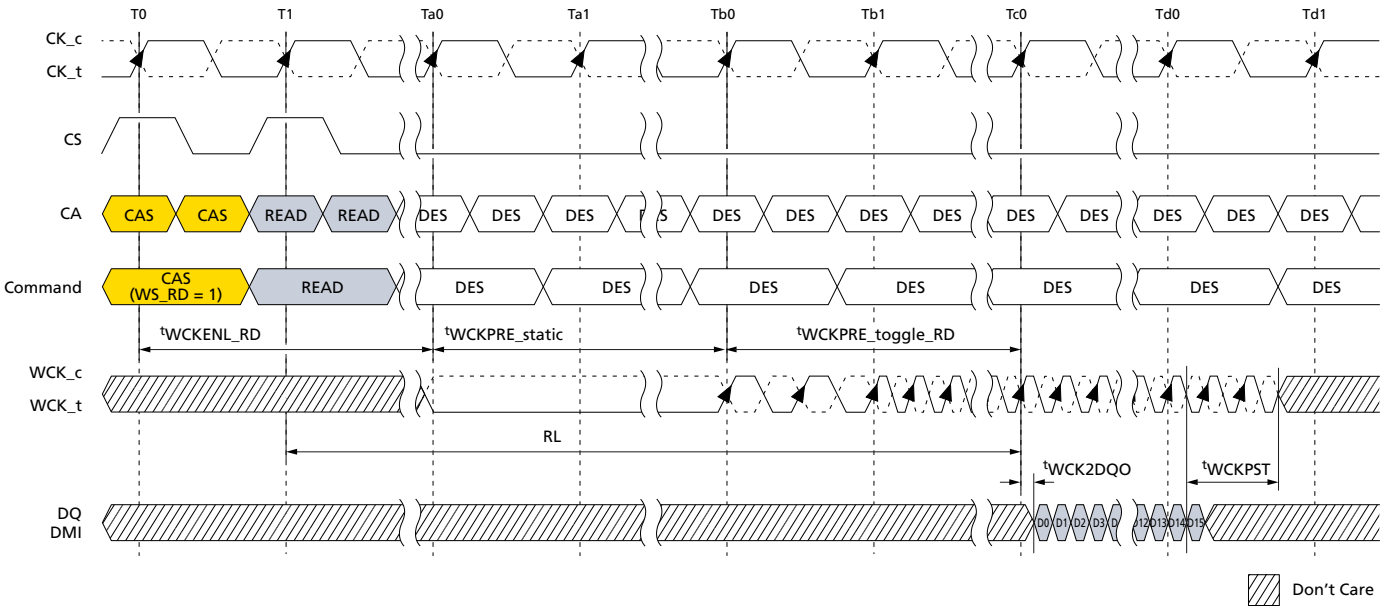
WCK2CK SYNC Operation Followed by a WRITE Command

Figure 3: WCK2CK Sync Followed by a WRITE Command



WCK2CK SYNC Operation Followed Immediately by a READ Command

Figure 4: WCK2CK Sync Followed by a READ Command



WCK2CK SYNC Operation With CAS(WS_FS = 1)

The WCK2CK SYNC operation is performed with minimum latency, ^{t}WCKENL_FS, when a CAS command with WS_FS = 1 is issued to a device. Using this command, the device controller can put the device into WCK2CK synchronized state as early as possible. CAS(WS_FS = 1) is used as a standalone command unlike CAS(WS_RD/WR) and can be issued to synchronize multi-ranks simultaneously.

After the CAS(WS_FS = 1) command is issued, READ/WRITE commands as well as other commands such as ACTIVE and REFRESH can also be issued.

Figure 5: Minimum Latency WCK2CK SYNC READ Operation With CAS(WS_FS = 1)

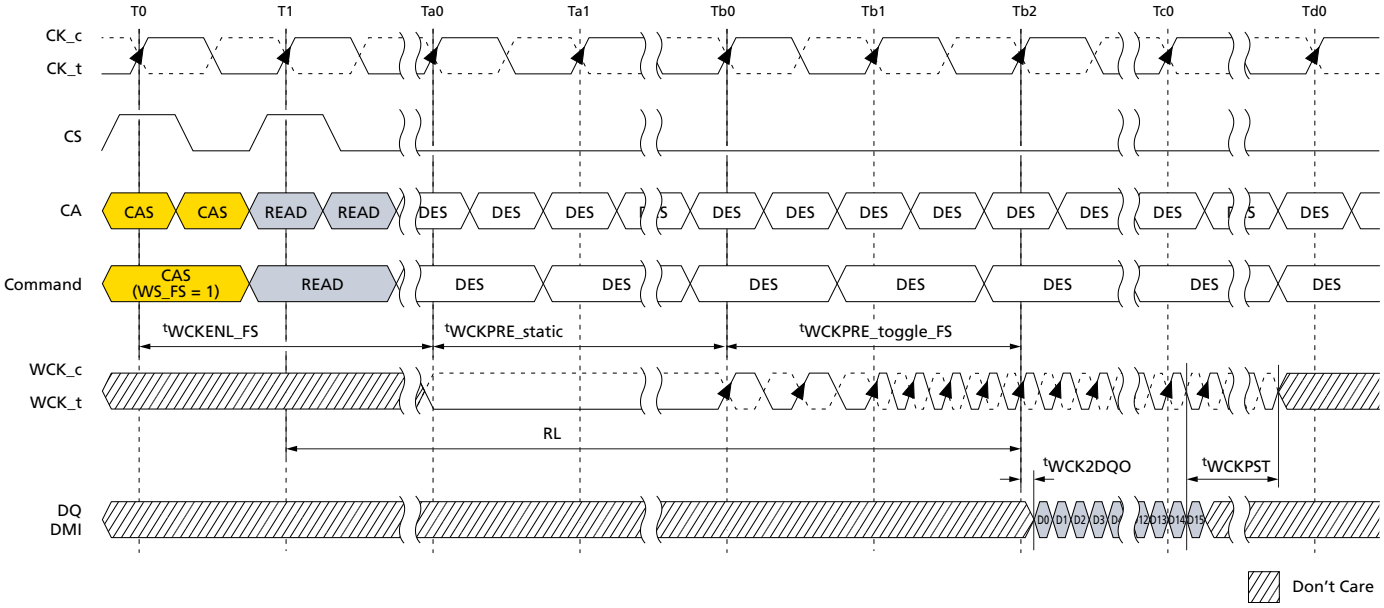
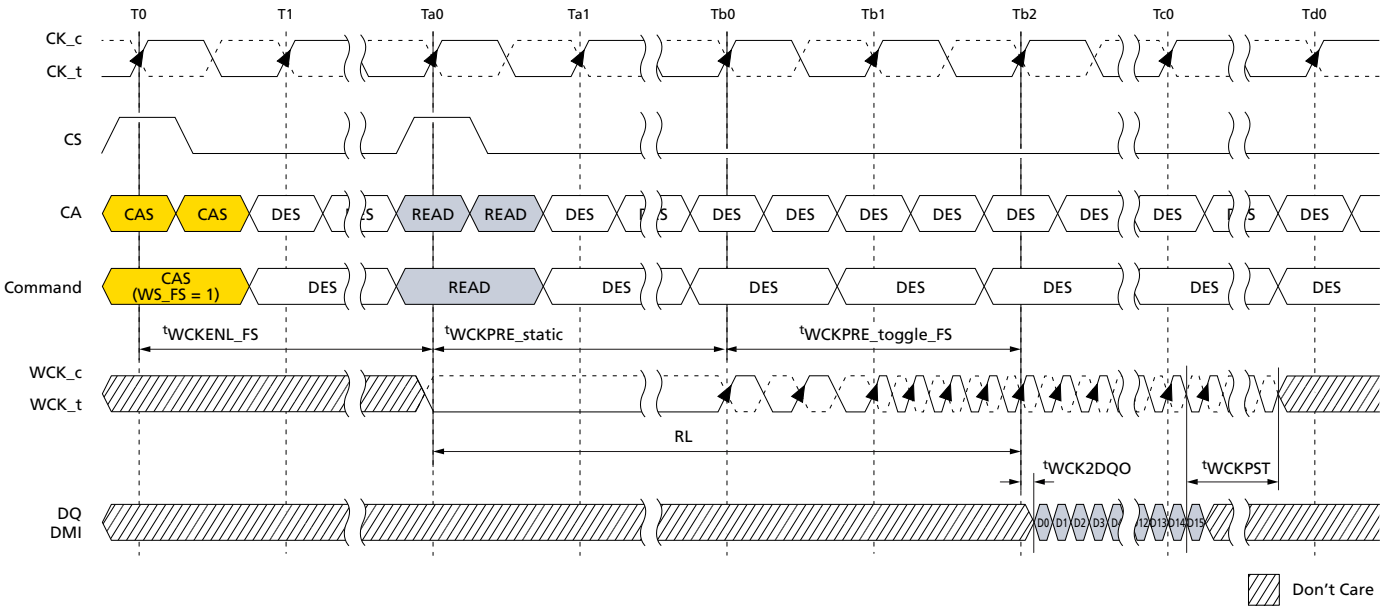


Figure 6: WCK2CK SYNC READ Operation With CAS(WS_FS = 1) and Command Gap



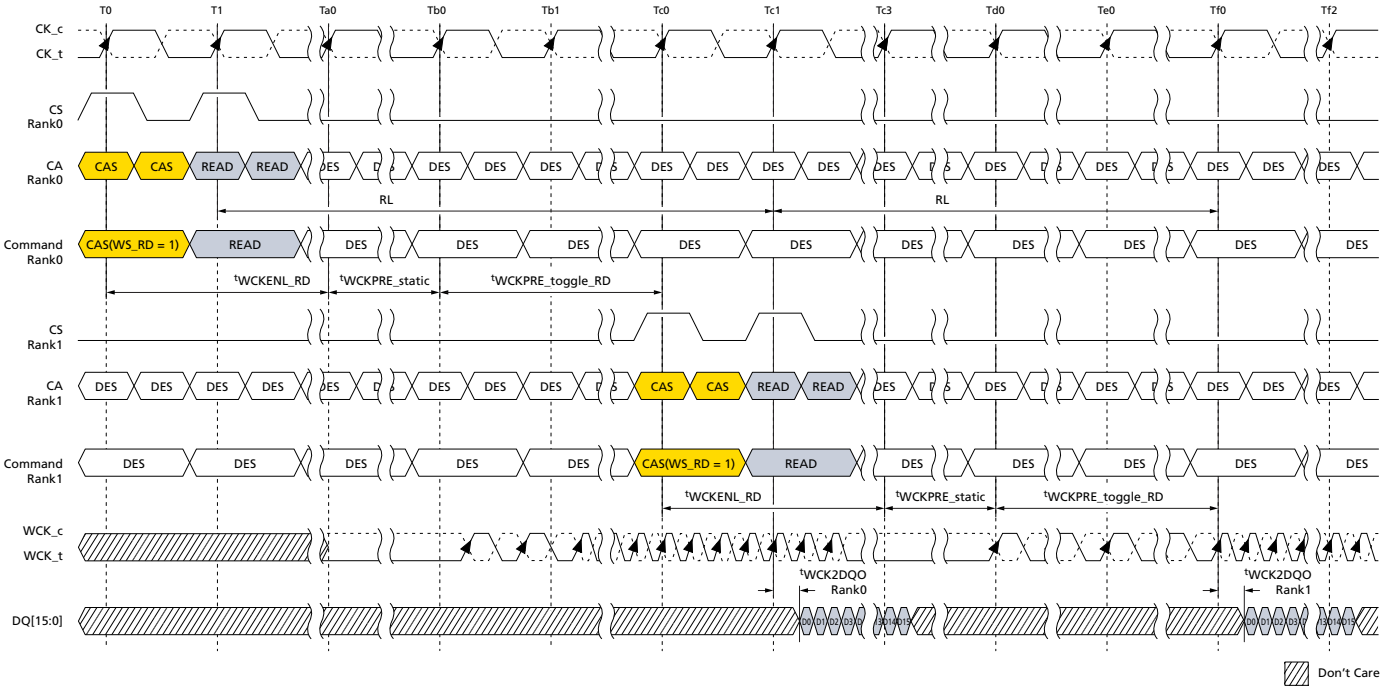
Rank-to-Rank WCK2CK SYNC Operation

There are two different methods to control WCK2CK sync state of a two rank device.

The first method is to start the WCK2CK sync process for rank 1 after completing a DQ data burst on rank 0. In this case, ^{t}WCKPSTof rank 0 and ^{t}WCKPRE of rank 1 should be

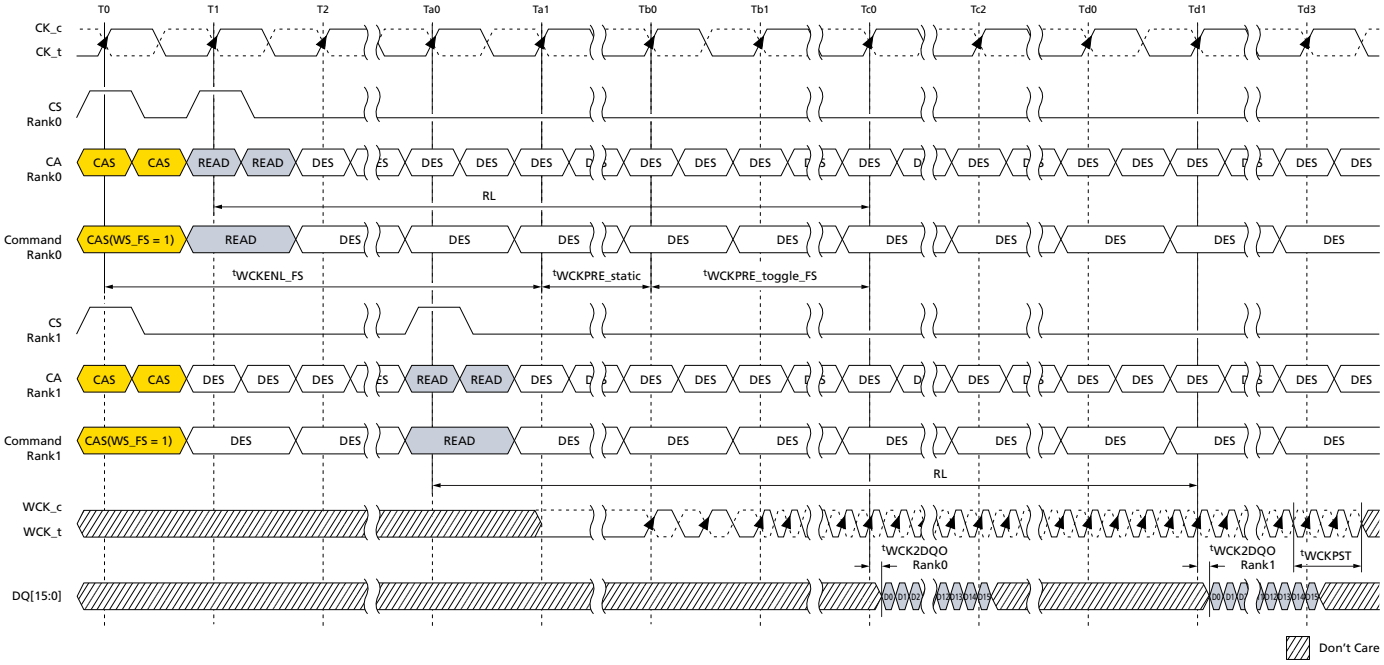
guaranteed for the correct RDQS postamble of the READ operation of rank 0 and for the correct WCK2CK synchronization of rank 1 respectively.

Figure 7: Minimum Gap Rank-to-Rank READ Operation With WCK2CK Sync After DQ Burst Complete in One Rank



The second method is to start the WCK2CK sync process for both ranks simultaneously. When both ranks are not in a WCK2CK synced state and DQ bursts between two ranks are closed, a simultaneous CAS command with WS_FS = 1 is recommended for efficient DQ bus utilization. If the subsequent DQ bursts of one rank are far from the preceding the burst of the other rank, extra power consumption due to WCK toggling should be considered. After synchronizing both ranks, if rank 0 is not used, CAS(WCK Sync off) command can be issued to rank 0 to save power.

Figure 8: Simultaneous WCK2CK Sync for Multi-ranks (Especially Two Ranks)



Revision History

Rev. A – 5/19

- Initial release

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