Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Quad SPI Flash
Palladium Memory Model
User Guide

Document Version: 4.0

Document Date: January 2018

Contents

List of Figures

List of Tables

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

Quad SPI Flash Memory Model

1. Introduction

The Cadence Palladium Quad SPI Flash Memory models are available with model sizes matching real Quad SPI flashes manufactured by Numonyx, Winbond, Macronix or Spansion. Different sizes are available; please consult the memory model catalog for the current available list.

Quad SPI Flash Memory models available in protected RTL (*.vhdp) formats:

- n25q032 : Numonyx 32Mbit N25Q032 series SPI flash
- n25q064 : Numonyx 64Mbit N25Q032 series SPI flash
- n25q128 : Numonyx 128Mbit N25Q128 series SPI flash
- n25q256a* : Numonyx 256Mbit N25Q256 series SPI flash
- n25q512 : Numonyx 512Mbit N25Q512 series SPI flash
- n25q00a : Numonyx 1Gbit N25Q00A series SPI flash

- s25fl032p : Spansion 32Mbit S25FL032P SPI flash
- s25fl064p : Spansion 64Mbit S25FL064P SPI flash
- s25fl129px0 : Spansion 128Mbit S25FL129P Uniform 64KB Sector SPI flash
- s25fl129px1 : Spansion 128Mbit S25FL129P Uniform 256KB Sector SPI flash
- s25fl128px0 : Spansion 128Mbit S25FL128P Uniform 64KB Sector SPI flash
- s25fl128px1 : Spansion 128Mbit S25FL128P Uniform 256KB Sector SPI flash
- s25fl128s : Spansion 128Mbit S25FL128S Uniform 256KB Sector SPI flash
- s25fl256s : Spansion 256Mbit S25FL256S Uniform 256KB Sector SPI flash
- s25fs128s : Spansion 128Mbit S25FS128S Uniform 256KB Sector SPI flash
- s25fs256s : Spansion 256Mbit S25FS256S Uniform 256KB Sector SPI flash
- s25fs512s : Spansion 512Mbit S25FS512S Uniform 256KB Sector SPI flash
- s70fs01gs : Spansion 1 Gbit S70FS01GS Uniform 256KB Sector SPI flash

- w25q40bv : Winbond 4Mbit W25Q40BV series SPI flash
- w25q80bv : Winbond 8Mbit W25Q80BV series SPI flash
- w25q16cv : Winbond 16Mbit W25Q16CV series SPI flash
- w25q32bv : Winbond 32Mbit W25Q32BV series SPI flash
- w25q64cv : Winbond 64Mbit W25Q64CV series SPI flash
- w25q128bv : Winbond 128Mbit W25Q128BV series SPI flash

- mx25u4035 : Macronix 4Mbit MX25L4035E series SPI Flash
- mx25u8035 : Macronix 8Mbit MX25L8035E series SPI Flash
- mx25u1635 : Macronix 16Mbit MX25L1635E series SPI Flash
- mx25u3235e : Macronix 32Mbit MX25L3235E series SPI Flash
- mx25u3235f : Macronix 32Mbit MX25L3235F series SPI Flash
- mx25u6435 : Macronix 64Mbit MX25L6435E series SPI Flash
- mx25u12835 : Macronix 128Mbit MX25L12835E series SPI Flash
- mx25u25635 : Macronix 256Mbit MX25L25635E series SPI Flash
- mx66u51235 : Macronix 512Mbit MX66L51235E series SPI Flash

- mx25u51245g : Macronix 512Mbit MX25U51245G series SPI Flash
- mx25u25645g : Macronix 256Mbit MX25U25645G series SPI Flash

Table 1: Datasheet and Revision Level References

Part Number	Rev.	Datasheet Date	Reference Datasheet
Micron (Numonyx)			
n25q032	E	JUN 2012	n25q_32mb_3v_65nm.pdf
n25q064	N	OCT 2014	n25q_64a_3v_65nm.pdf
n25q128	S	NOV 2014	n25q_128mb_3v_65nm.pdf
n25q256a*	J	JUN 2012	n25q_256mb_3v_65nm.pdf
n25q512	G	JUN 2012	n25q_512mb_1ce_3v_65nm.pdf
n25q00a	F	JUN 2012	n25q_1gb_3v_65nm.pdf
Spansion			
s25fl032p	6	DEC 2011	S25FL032P_00.pdf
s25fl064p	8	JAN 2013	S25FL064P_00.pdf
s25fl129px0	8	SEP 2012	S25FL129P_00.pdf
s25fl129px1	8	SEP 2012	S25FL129P_00.pdf
s25fl128px0	12	JAN 2013	S25FL128P_00.pdf
s25fl128px1	12	JAN 2013	S25FL128P_00.pdf
s25fl128s	7	MAR 2014	S25FL128S_256S_00.pdf
s25fl256s	7	MAR 2014	S25FL128S_256S_00.pdf
s25fs128s	6	NOV 2014	S25FS-S_00.pdf
s25fs256s	6	NOV 2014	S25FS-S_00.pdf
s25fs512s			S25FS512S_00.pdf
s70fs01gs	1	AUG 2015	S70FS01GS_00.pdf
Winbond			
w25q40bv	B	JUL 2010	W25Q40BV.pdf
w25q80bv	F	APR 2012	W25Q80BV.pdf
w25q16cv	C	APR 2011	W25Q16CV.pdf
w25q32bv	F	APR 2011	W25Q32BV.pdf
w25q64cv	C	APR 2011	W25Q64CV.pdf
w25q128bv	G	APR 2012	W25Q128BV.pdf
Macronix			
mx25u4035	1.4	JUL 2010	MX25U4035, 1.8V, 4Mb, v1.4.pdf
mx25u8035	1.4	JUL 2010	refer to MX25U4035, 1.8V, 4Mb, v1.4.pdf, size change only
mx25u1635	1.9	NOV 2013	MX25U1635E, 1.8V, 16Mb, v1.9.pdf
mx25u3235e	1.9	NOV 2013	MX25U3235E, 1.8V, 32Mb, v1.9.pdf
mx25u3235f	1.6	JUL 2017	MX25U3235F, 1.8V, 32Mb, v1.6.pdf
mx25u6435	1.3	FEB 2012	MX25U6435E, 1.8V, 64Mb, v1.3.pdf
mx25u12835	1.4	FEB 2014	MX25U12835F, 1.8V, 128Mb, v1.4.pdf
mx25u25635	1.2	NOV 2013	MX25U25635F, 1.8V, 256Mb, v1.2.pdf
mx66u51235	1.0	NOV 2013	MX66U51235F, 1.8V, 512Mb, v1.0.pdf
mx25u51245g	1.1	JUN 2017	MX25U51245G, 1.8V, 512Mb, v1.1.pdf
mx25u25645g	1.1	MAR 2017	MX25U25645G, 1.8V, 256Mb, v1.1.pdf

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Table 2: Release Level for MMP Models

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Features

Table 3: Feature List for Numonyx Models

Features		Support	Notes
Reset Operations	Reset Enable	Yes	
	Reset Memory	No	
Identification Operations	Read ID	Yes	1, 9
	Multiple I/O Read ID	Yes	
	Read Serial Flash Discovery Parameter (SFDP)	Yes	2
Read Operations	Read	Yes	
	Fast Read	Yes	
	Dual Output Fast Read	Yes	
	Dual I/O Fast Read	Yes	
	Quad Output Fast Read	Yes	
	Quad I/O Fast Read	Yes	
	Fast Read -DTR	Yes	
	Dual Output Fast Read -DTR	Yes	3
	Dual I/O Fast Read -DTR	Yes	3
	Quad Output Fast Read -DTR	Yes	3
	Quad I/O Fast Read -DTR	Yes	3
	4-Byte Read	Yes	4
	4-Byte Fast Read	Yes	4
	4-Byte Dual Output Fast Read	Yes	4
	4-Byte Dual I/O Fast Read	Yes	4
	4-Byte Quad Output Fast Read	Yes	4
	4-Byte Quad I/O Fast Read	Yes	4
	Burst16/32/64 wrap around	No	7
	Execute-in-place (XIP)	Yes	8
	Enter/Exit Quad I/O	Yes	
Write Operations	Write Enable	Yes	
	Write Disable	Yes	
Register Operations	Read Status Register	Yes	
	Write Status Register	Yes	
	Read Lock Register	Yes	
	Write Lock Register	Yes	
	Read Flag Status Register	Yes	
	Clear Flag Status Register	Yes	
	Read Non-volatile Configuration Register	Yes	
	Write Non-volatile Configuration Register	Yes	
	Read volatile Configuration Register	Yes	
	Write volatile Configuration Register	Yes	
	Read Enhanced Volatile Configuration Register	Yes	
	Write Enhanced Volatile Configuration Register	Yes	
	Read Extended Address Register	Yes	5
	Write Extended Address Register	Yes	5
Program Operations	Page Program	Yes	
	Dual Input Fast Program	Yes	

Features		Support	Notes
	Extended Dual Input Fast Program	Yes	10
	Quad Input Fast Program	Yes	
	Extended Quad Input Fast Program	Yes	
	4-Byte Page Program	Yes	4
	4-Byte Quad Input Fast Program	Yes	4
Erase Operations	Subsector Erase	Yes	
	Sector Erase	Yes	
	Bulk Erase	Yes	
	Program/Erase Suspend	Yes	
	Program/Erase Resume	Yes	
	4-Byte Subsector Erase	Yes	4
	4-Byte Sector Erase	Yes	4
OTP Operations	Read OTP array	Yes	
	Program OTP array	Yes	
4-Byte Address Mode Operations	Enter 4-Byte address mode	Yes	4
	Exit 4-Byte address mode	Yes	4
NVCR port support		Yes	6
Power Operations	Deep Power Down	Yes	11
	Release from Deep Power Down	Yes	11

Notes:

1. Model accepts command 0x9E and 0x9F to read identification, and these two commands just work in SPI mode according the datasheet.
2. The initial content of the SFDP area is all zeroes, the user can load an image file to the SFDP content in Palladium tools, the name of the SFDP area in the tool is called *mem_param*
3. DTR commands are supported for devices larger than 128Mbit according to the datasheet
4. 4-byte addressing commands are supported for devices larger than 128Mbit according to the datasheet
5. Extended address commands are supported for devices larger than 128Mbit according to the datasheet
6. The value of NVCR Non-volatile register can be passed to the model through the extra 16-bit port called *nvcr_init.* The value is used as the default configuration after power on. The user must provide a value to the *nvcr_init* port when instantiating the model. If the port is left unconnected, the model may not work correctly. The user can either connect *nvcr_init* to 0xFFFF or any other value, please find more information about this non-volatile configuration register in Numonyx datasheet
7. Wrap-around defined in volatile configuration register is not supported
8. XIP bit in volatile configuration register is required to set in order to enable model's XIP
9. Unique ID assigned by factory is set to all zeroes
10. Command (0x12) are used as Extended Dual Input Fast Program
11. This two commands are supported for devices n25q256a11 and n25q256a31.

Table 4: Feature List for Winbond Models

Features		Support	Notes
Write Operations	Write Enable	Yes	
	Write Disable	Yes	
	Write Enable for volatile status register	Yes	
Register Operations	Read Status Register 1	Yes	
	Write Status Register 1	Yes	
	Read Status Register 2	Yes	
	Write Status Register 2	Yes	
Program Operations	Page Program	Yes	
	Quad Page Program	Yes	
Erase Operations	4KB Sector Erase	Yes	
	32KB Block Erase	Yes	
	64KB Block Erase	Yes	
	Chip Erase	Yes	
	Program/Erase Suspend	Yes	
	Program/Erase Resume	Yes	
Power Operations	Power down	Yes	
	Release Power Down	Yes	
Read Operations	Read	Yes	
	Fast Read	Yes	
	Fast Read Dual Output	Yes	
	Fast Read Quad Output	Yes	
	Fast Read Dual I/O	Yes	
	Fast Read Quad I/O	Yes	
	Word Read Quad I/O	Yes	
	Octal Word Read Quad I/O	Yes	
	Burst with wrap around	Yes	
	Continuous Read Mode Execute-in-place (XIP)	Yes	
Identification Operations	Read Manufacturer/Device ID	Yes	
	Read Unique ID	Yes	1
	Read JEDEC ID	Yes	
	Dual I/O, Quad I/O read Manufacturer/Device ID	Yes	
	Read Serial Flash Discovery Parameter (SFDP)	Yes	2
Security Register Operations	Erase/Program/Read Security Registers	Yes	
NVCR port support		Yes	3

Notes:
1. The 64-bit factory set unique ID number is set to {x”01”,x”02”,x”03”,x”04” x”05”,x”06”,x”07”,x”08”} by default.
2. The SFDP inform for W25Q80BV and W25Q128BV is not provided in datasheet, the models use “FF” as reserved data
3. The value of NVCR Non-volatile register can be passed to the model through the extra 16-bit port called *nvcr_init.* The value is used as the default status register configure after power on. If the port is not use, the user must connect *nvcr_init* to 0x0000. *nvcr_init[15:8]* is used for status register 2, and

nvcr_init[7:0] is used for status register1. Please find more information about this non-volatile status register in Winbond datasheet

Table 5: Feature List for Macronix Models

Features		Support	Notes
Write Operations	Write Enable	Yes	
	Write Disable	Yes	
Register Operations	Read Status Register	Yes	
	Write Status Register	Yes	
	Read Extended Address Register	Yes	
	Write Extended Address Register	Yes	1
	4_byte Mode Enable/Disable	Yes	1
	Quad I/O Enable/Disable	Yes	
	Read Fast Boot Register	Yes	4
	Write Fast Boot Register	Yes	4
	Erase Fast Boot Register	Yes	4
	Read Configuration Register	Yes	
	Write Configuration Register	Yes	
	Read Configuration Register 2	Yes	5,8
	Write Configuration Register 2	Yes	5,8
Program Operations	Page Program	Yes	
	Quad Page Program	Yes	
Erase Operations	4KB Sector Erase	Yes	
	32KB Block Erase	Yes	
	64KB Block Erase	Yes	
	Chip Erase	Yes	
	Program/Erase Suspend	Yes	
	Program/Erase Resume	Yes	
Power Operations	Deep Power Down	Yes	
	Release Deep Power Down	Yes	
Read Operations	Read	Yes	
	Fast Read	Yes	
	Fast Read Dual Output	Yes	
	Fast Read Quad Output	Yes	
	2x I/O Read	Yes	
	4x I/O Read	Yes	
	4x I/O DTR Read	Yes	
	4-Byte Read	Yes	1
	4-Byte Fast Read	Yes	1
	4-Byte Fast Read Dual Output	Yes	1
	4-Byte Fast Read Quad Output	Yes	1
	4-Byte 2x I/O Read	Yes	1
	4-Byte 4x I/O Read	Yes	1
	4-Byte 4x I/O DTR Read	Yes	
	Burst with wrap around	Yes	
	Continuous Read Mode Execute-in-place (XIP)	Yes	
	Preamble for 1/2/4 I/O, DTR4 I/O	Yes	
Identification Operations	Read ID	Yes	
	Read Serial Flash Discovery Parameter (SFDP)	Yes	2
OTP Operations	OTP mode enter	Yes	
	OTP mode exit	Yes	
Security Register Operations	Read Security Registers	Yes	
	Write Security Registers	Yes	

Block Lock Operations	Single Block Lock/Unlock	Yes	3
	Gang Block Lock/Unlock	Yes	3
	Read/Write Lock Register	Yes	3
	Read/Write DPB	Yes	3
	Read/Write SPB	Yes	3
Password Register Operations	Read Password Register	Yes	6,7
	Write Password Register	Yes	6,7
	Password Unlock command	Yes	6,7
Reset Operations	Reset Enable	Yes	
	Reset Memory	No	

Notes:
1. Extended address, 4-byte addressing commands are supported for devices larger than 128Mbit according to the datasheet
2. The initial content of the SFDP area is all zeroes, the user can load an image file to the SFDP content in Palladium tools, the name of the SFDP area in the tool is called *mem_param*
3 The model will accept advanced section protection commands defined, but will not activate the protection, only protection defined in status register will be active
4 The default state for fast boot register is “FFFF_FFFF” after power-on
5 The model accepts this command, but the built-in ECC is not supported
6 These commands only are included in the datasheets of model MX25U25645G and model MX25U51245G.
7 The model will accept advanced passwords section protection commands defined, but will not activate the protection, only protection defined in status register will be active.
8 The model MX25U51245G and model MX25U25645G do not have the configuration register 2 according to the version 1.1 datasheet.

Table 6: Feature List for Spansion Models

Features		Support	Notes
Read Operations	Read	Yes	4
	Fast Read	Yes	4
	Fast Read Dual Output	Yes	4
	Fast Read Quad Output	Yes	4
	Dual I/O Read	Yes	4
	Quad I/O Read	Yes	4
	4-Byte Read	Yes	4
	4-Byte Fast Read	Yes	4
	4-Byte Dual Output	Yes	4
	4-Byte Quad Output	Yes	4
	4-Byte Dual I/O	Yes	4
	4-Byte Quad I/O	Yes	4
	3 or 4-Byte DDR Dual I/O	Yes	4
	3 or 4-Byte DDR Quad I/O	Yes	4
	Enter 4-byte address, Set burst length, Evaluate erase status	Yes	3
	Execute-in-Place (XIP)	Yes	
Identification Operations	Read ID	Yes	
	Read CFI	Yes	2
	Read Quad ID	Yes	3
	Read Serial Flash Discoverable Parameters	No	3
Write Operations	Write Enable	Yes	
	Write Disable	Yes	
Program Operations	Page Program	Yes	
	Quad Page Program	Yes	
	4-Byte Page Program	Yes	
	4-Byte Quad Page Program	Yes	
Erase Operations	4KB Sector Erase	Yes	
	8KB Block Erase	Yes	
	64KB Block Erase	Yes	
	256KB Block Erase	Yes	
	Bulk Erase	Yes	
	Program/Erase Suspend	Yes	
	Program/Erase Resume	Yes	
Register Operations	Read Status Register	Yes	
	Write Status/Configuration Register	Yes	
	Read Configuration Register	Yes	
	Reset Erase and Program Fail Flag	Yes	
	Read Auto Boot Register	Yes	1
	Write Auto Boot Register	Yes	1
	Read Bank Register	Yes	1
	Write Bank Register	Yes	1
	Bank Address Access	No	1
	Read Data Learning Pattern	Yes	
	Program/Write Data Learning Pattern	Yes	
Any Register Operations	Read Any Register	Yes	3,
	Write Any Register	Yes	3
	Any Register to config Wrap-around	Yes	3

Features		Support	Notes
	Any Register to config latency	Yes	3,5
	Any Register to config IO3 as Reset#	No	3
	Any Register to config address length	Yes	3
	Any Register to config QPI	Yes	3
	Any Register to config Status/Configuration Register	Yes	3
Power Operations	Deep Power Down	Yes	
	Release Deep Power Down	Yes	
OTP Operations	OTP Memory Program	Yes	
	OTP Memory Read	Yes	
Protection Operations	ASP Read	Yes	
	ASP Program	Yes	
	DYB Read	Yes	
	DYB Write	Yes	
	PPB Read	Yes	
	PPB Program	Yes	
	PPB Erase	Yes	
	PPB Lock Bit Read	Yes	
	PPB Lock Bit Write	Yes	
	Password Read	Yes	
	Password Program	Yes	
	Password Unlock	Yes	
Reset Operations	Software Reset	Yes	3
	Mode Bit Reset	Yes	
	Software Reset Enable	Yes	3
	Legacy Software Reset	Yes	

Notes:
1. This is s25flxxs family only feature
2. CFI table in the MMP models provide information from byte address 00h to byte address 30h
3. This is a s25fsxxs family and s70fsxxs part only feature
4. Read Latency are defined in SDR/DDR High Performance table for s25flxxs family datasheet
   Read Latency are defined in CR2V register for s25fsxxs family datasheet, the default is 8 cycles
5. Read/Write Any Register can access volatile Registers starting from address 0x00800000

4. Devices Supported

The following tables list some of the flashes supported by current models. Please consult the appropriate vendor site for details on the parts they offer.

Table 7: Numonyx N25Q Series

Part Number	Density	Feature
N25Q032Axxx	32M bit	Byte addressability, Hold pin
N25Q064Axxx	64M bit	Byte addressability, Hold pin
N25Q128Axxx	128M bit	Byte addressability, Hold pin
N25Q256Axxx	256M bit	Byte addressability, Hold pin
N25Q512Axxx	512M bit	Byte addressability, Hold pin
N25Q00AAxxx	1G bit	Byte addressability, Hold pin

Table 8: Spansion S25FL032P Series

Part Number	Density	Feature
S25FL032P0XMFIxxx	32M bit	Uniform 64KB Sectors
S25FL032P0XNFIxxx	32M bit	Uniform 64KB Sectors
S25FL032P0XMFVxxx	32M bit	Uniform 64KB Sectors
S25FL032P0XNFVxxx	32M bit	Uniform 64KB Sectors
S25FL032P0XBHIxxx	32M bit	Uniform 64KB Sectors
S25FL032P0XBHVxxx	32M bit	Uniform 64KB Sectors

Table 9: Spansion S25FL064P Series

Part Number	Density	Feature
S25FL064P0XMFIxxx	64M bit	Uniform 64KB Sectors
S25FL064P0XNFIxxx	64M bit	Uniform 64KB Sectors
S25FL064P0XMFVxxx	64M bit	Uniform 64KB Sectors
S25FL064P0XNFVxxx	64M bit	Uniform 64KB Sectors
S25FL064P0XBHIxxx	64M bit	Uniform 64KB Sectors
S25FL064P0XBHVxxx	64M bit	Uniform 64KB Sectors

Table 10: Spansion S25FL129P/ S25FL128P Series

Part Number	Density	Feature
S25FL129P0XMFI00x	128M bit	Uniform 64KB Sectors
S25FL129P0XMFI01x	128M bit	Uniform 256KB Sectors
S25FL129P0XNFI00x	128M bit	Uniform 64KB Sectors
S25FL129P0XNFI01x	128M bit	Uniform 256KB Sectors
S25FL129P0XMFV00x	128M bit	Uniform 64KB Sectors
S25FL129P0XMFV01x	128M bit	Uniform 256KB Sectors
S25FL129P0XNFV00x	128M bit	Uniform 64KB Sectors
S25FL129P0XNFV01x	128M bit	Uniform 256KB Sectors
S25FL129P0XBHI20x	128M bit	Uniform 64KB Sectors
S25FL129P0XBHI21x	128M bit	Uniform 256KB Sectors
S25FL129P0XBHI30x	128M bit	Uniform 64KB Sectors
S25FL129P0XBHI31x	128M bit	Uniform 256KB Sectors
S25FL129P0XBHV20x	128M bit	Uniform 64KB Sectors
S25FL129P0XBHV21x	128M bit	Uniform 256KB Sectors
S25FL129P0XBHV30x	128M bit	Uniform 64KB Sectors
S25FL129P0XBHV31x	128M bit	Uniform 256KB Sectors
S25FL128P0XMFI00x	128M bit	Uniform 64KB Sectors
S25FL128P0XMFI01x	128M bit	Uniform 256KB Sectors

Table 11: Spansion S25FLxxS/ S25FSxxS Series

Part Number	Density	Feature
S25FL128Sxx	128M bit	Uniform 256KB Sectors
S25FL256Sxx	256M bit	Uniform 256KB Sectors
S25FS128Sxx	128M bit	Uniform 256KB sectors
S25FS256Sxx	256M bit	Uniform 256KB sectors
S25FS512Sxx	512M bit	Uniform 256KB sectors
S70FS01GS	1G bit	Uniform 256KB sectors

Table 12: Winbond W25Q Series

Part Number	Density	Feature
W25Q40BVxxx	4M bit	4/32/64 KB Sector/Block
W25Q80BVxxx	8M bit	4/32/64 KB Sector/Block
W25Q16CVxxx	16M bit	4/32/64 KB Sector/Block
W25Q32BVxxx	32M bit	4/32/64 KB Sector/Block
W25Q64CVxxx	64M bit	4/32/64 KB Sector/Block
W25Q128BVxxx	128M bit	4/32/64 KB Sector/Block

Table 13: Macronix MX25Uxx35 Series

Part Number	Density	Feature
MX25U4035	4M bit	4/32/64 KB Sector/Block
MX25U8035	8M bit	4/32/64 KB Sector/Block
MX25U1635	16M bit	4/32/64 KB Sector/Block
MX25U3235E	32M bit	4/32/64 KB Sector/Block
MX25U3235F	32M bit	4/32/64 KB Sector/Block
MX25U6435	64M bit	4/32/64 KB Sector/Block
MX25U12835	128M bit	4/32/64 KB Sector/Block
MX25U25635	256M bit	4/32/64 KB Sector/Block
MX25U51235	512M bit	4/32/64 KB Sector/Block
MX25U51245G	512M bit	4/32/64 KB Sector/Block
MX25U25645G	2G bit	4/32/64 KB Sector/Block

***Note**: The tables don't list all the supported parts. To check whether a part is supported or not by the model, please take following conditions into account:*

1. *Only those parts with Hold pin are supported by the models.*

5. Model Block Diagrams

5.1 Interface Diagrams

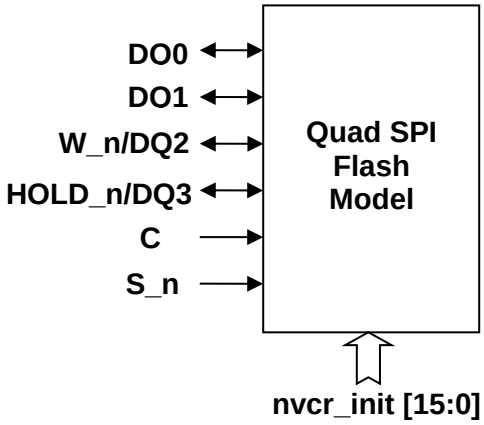

Figure 1: Numonyx/Winbond Quad SPI Flash Model Interface

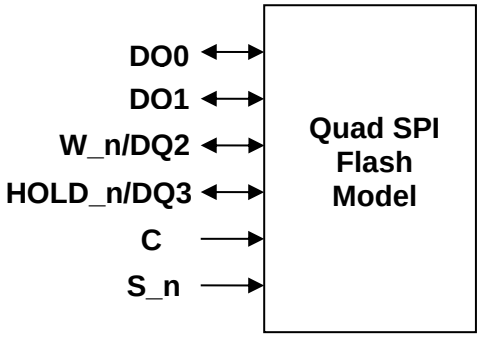

Figure 2: Spansion/Macronix Quad SPI Flash Model Interface

Table 14: Spansion/Macronix and Numonyx/Winbond Signal Names

Signal	I/O	Description
DQ0	I/O	Serial Input for single bit data commands. IO0 for Dual or Quad commands
DQ1	I/O	Serial Output for single bit data commands. IO1 for Dual or Quad commands.
W_n/DQ2	I/O	Write Protect. IO2 for Quad commands
HOLD_n/DQ3	I/O	Hold to pause the serial transfer. IO3 for Quad commands
C	Input	Serial Clock
S_n	Input	Chip Select
nvcr_init	Input	16-bit width NVCR initial value for Numonyx and Winbond devices

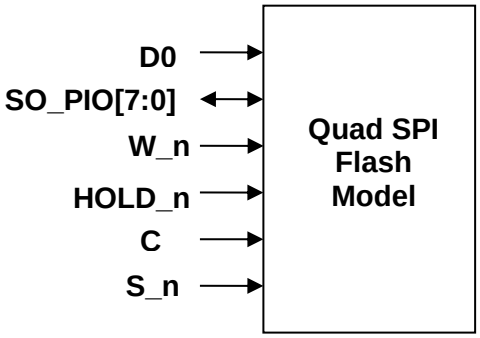

Figure 3: Spansion s25flxxpm Quad SPI Flash Model Interface

Table 15: S25FLxxPM Series Signal Names

Signal	I/O	Description
D0	Input	Serial Data input
SO_PIO[7:0]	I/O	Serial Data output, Parallel Data input/output When in serial mode, the highest bit (7th) would be used as serial output
W_n	Input	Write Protect
HOLD_n	input	Hold to pause the serial transfer
CLK	Input	Serial Clock
S_n	Input	Chip Select

5.2 Connection Diagram

For Numonyx Quad IO SPI models, there is an extra input port called *nvcr_init*. The port is used for setting the NVCR value at startup. The user needs to provide a value to the *nvcr_init* port. Otherwise, the model may not work correctly.

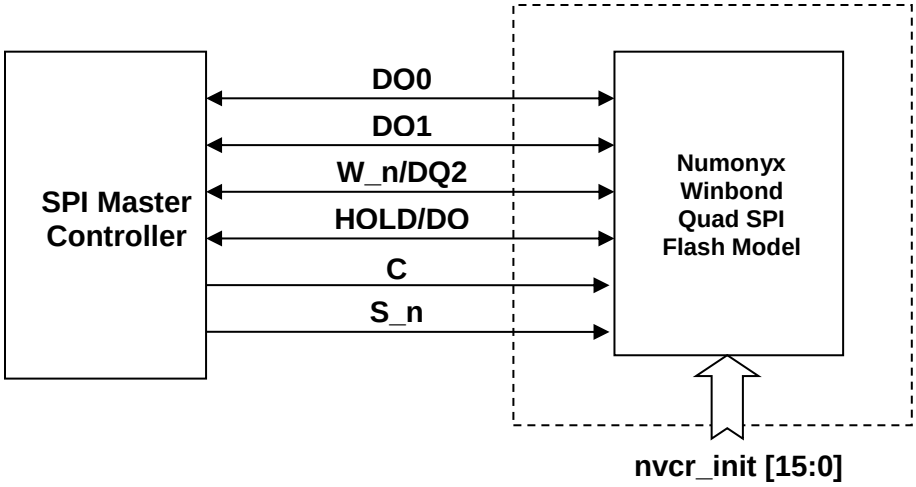

Figure 4: Numonyx/Winbond Flash Model Connection Diagram

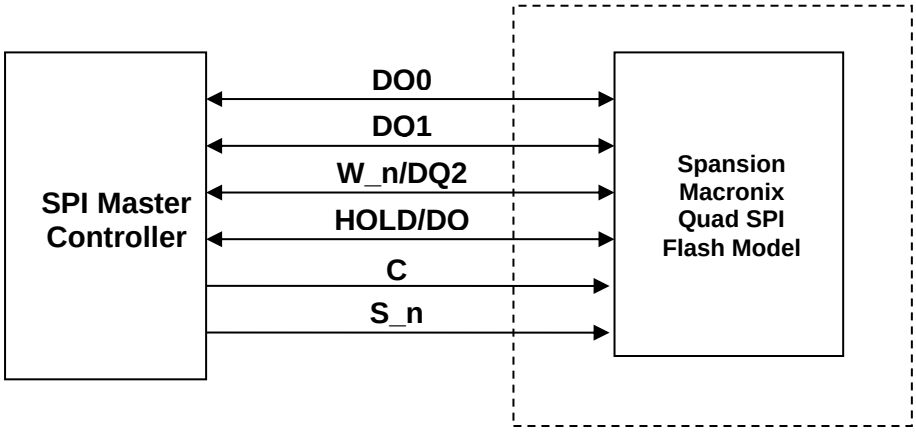

Figure 5: Spansion/Macronix Flash Model Connection Diagram

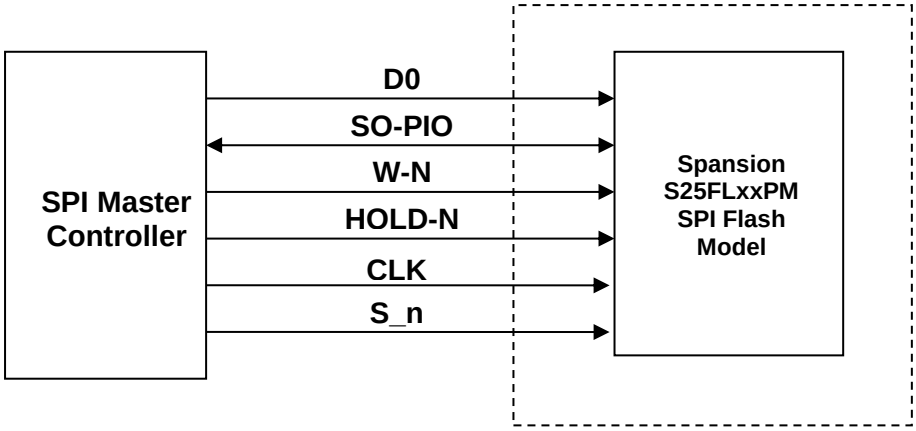

Figure 6: Spansion S25FLxxPM Series Flash Model Connection Diagram

6. Limitations

- These models do not support the RESET# pin except mx25u3235f model. All MMP QSPI models have power-on-reset logic inside and do not support the standard RESET# pin. For devices that share a pin for both RESET# and HOLD_N/DQ3 signals, the model uses this pin only for HOLD_N/DQ3 functionality.

- Flash Memory and OTP Memory Initial Content
  After download into the Palladium the initial value of the flash memory array is all 0's. Like real Flash parts the model only allows programming of 1's to 0's. The memory region of the Flash array being programmed must first either be erased with an erase command or initialized to all 1's through the user issuing a memory set command in Palladium runtime tools.

7. Model Emulation

7.1 Emulation Notes

Some things needed to be kept in mind when running emulation with the Quad SPI Flash model in Palladium.

- The Quad SPI Flash models are delivered as protected VHDL source with the top-level declaration unprotected and the core flash memory array and OTP memory array, if applicable to the model/part, unprotected.
  - The main data array is called *mem_array*
  - The OTP array is called *mem_otp*
    - *See features tables above for indication of models with OTP support. Winbond models do not have a mem_otp array.*

- The top-level module in the Quad SPI Flash modules is the part number, for example n25q032. To use the model in your design, just instantiate the top-level module n25q032 and map the ports to your actual wires. For more details of the top-level declaration, please open the protected vhdl source with a text viewer and search for the top-level module name. Please be careful that the 16-bit nvcr_init port needs to be set with a steady value for the Numonyx and Winbond models. Below is the port declaration of the top-level of the Numonyx model:

```
entity n25q032 is
    port (
        c           : in std_logic;
        s_n         : in std_logic;
        dq0         : inout std_logic;
        dq1         : inout std_logic;
        w_n_dq2     : inout std_logic;
        hold_n_dq3  : inout std_logic;
        nvcr_init   : in std_logic_vector(15 downto 0)
);
end entity n25q032;
```

- The initial content of flash memory and OTP memory (for models that have a mem_otp array) are all ‘0’ at start-up, which will cause the OTP memory to be locked after Palladium emulation is started, and program to the flash memory will not work. The content of flash memory and OTP can be initialized to all ‘1’ in Memory tab of questDebug GUI or by issuing commands in the questQel console as below:

```
QEL> memory -set <dspath>.mem_array
QEL> memory -set <dspath>.mem_otp
```

To check the full path of the *mem_array* or *mem_otp*, please go to the Memory tab in questDebug, or invoke the *memory* command in the questQEL console. Below is an example to get the memory path in the design.

```
QEL> memory
flash_tb.n25q032_i.n25q032_core_i.mem_array
flash_tb.n25q032_i.n25q032_core_i.mem_otp
flash_tb.n25q032_i.n25q032_core_i.mem_param
…
…
```

The user can also erase the flash memory to all '1' by invoking the Bulk Erase (BE) instruction after emulation has been started. Note that not all models have all three arrays. Winbond models, for example, do not have either a mem_otp or mem_param array.

- For Numonyx models, the initial value of the VECR register is "11011111" and the initial value of VCR register is "11111011".

- For Numonyx models, the operation mode at start-up can be Extended SPI, Dual IO SPI or Quad IO SPI, which is determined by the value of NVCR provided by the *nvcr_init* port.

- For Numonyx models, Protection bit in Flag Status Register may be set due to invalid write or invalid erase. Once the Protection bit is set, only the CLFSR, RDSR or RFSR instruction is acceptable for the model.

7.2 Emulation Example

Below is an example of the command list to synthesize the protected RTL files (*.vhdp) into the netlist (*.vgp):

```
vavlog   mmp_spi_clk_gen.v
vavhdl   n25q032.vhdp
vaelab   –keepRtlSymbol –keepAllFlipFlop –outputvlog n25q032.vgp n25q032
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

Below is an example of the command list for importing the Quad SPI Flash model to your design:

```
QEL> delimiterRule Verilog
QEL> importOption {mode full} {protection on} {library libf}
QEL> reflib qtref
QEL> netlistFile "verilog n25q032.vgp"
QEL> designImport
QEL> importOption {protection on} {library libf}
QEL> reflib qtref libf
QEL> netlistFile "verilog <your design netlists>"
QEL> designImport
```

7.3 IXCOM Notes

For the IXCOM the SPI model requires an internal clock generator. The module uses an IXCOM clock generator which is SystemVerilog based. As part of the IXCOM compile flow you must include the IXCOMClkGen.sv file from the UXE installation. The mmp_spi_clk_gen.v file can be found in the <MMP install>/common/ directory.

Below is an example.

```
vlan mmp_spi_clk_gen.v

vhan n25q032.vhdp

Other design files…

ixcom -ua -top tb +dut+n25q032
```

Note that for large memory models like n25q00a, which is 1Gbit in size, special switches are needed to compile successfully. The “-vhdlsparsearray 1000000” option should be provided for both compilation and elaboration phases. Without these switches an integer overflow error occurs.

```
ixcom -ua -top tb +dut+n25q00a –ncelabargs "-vhdlsparsearray
1000000" –ncvhdlargs "-vhdlsparsearray 1000000"
```

Several enhancements to the QSPI family compile are introduced. The enhanced compile flow for these memory models also requires changes to the user’s flow and are described below:

- For earlier versions of the models, the option +rtlCommentPragma was a required option for the IXCOM flow and as such was shown in the vhan command above. The +rtlCommentPragma option is no longer required.

- For earlier versions of the models, the top model name was “flash” and now the top model name is the same as the part name and file name. Thus, in the ixcom command example above +dut+flash is now +dut+n25q032.

- For earlier versions of the models, the –work command was used to specify a vhdlaux_lib as a separate logical library in which to compile instead of the default logical library called WORK. That separate logical library is no longer required. The model compile uses the default logical library WORK. Hence the option –work is removed from the example above.

- The previous requirement for a separate logical library also necessitated the –libmaprc option to specify a non-default libmaprc script to specify the vhdl_aux to path for vhdl_aux mapping (vhdlaux_lib => ./vhdlaux_lib). The removal of the separate logical library also means that the –libmaprc option is no longer required to specify this mapping. Hence the –libmaprc option has been removed from the example compile.

Revision History

The following table shows the revision history for this document

Date	Version	Revision
September 2010	1.0	Initial release
June 2011	1.1	Configurable Dummy Clock Cycle; Supporting NVCR non-volatile configuration register for Numonyx models.
August 2011	1.2	Minor update
March 2012	1.3	Add Numonyx N25Q 64M/256M/512M/1Gb models Add Winbond models W25Q
May 2013	1.4	Adding IXCOM instructions and Spansion S25FL128PX pinout information
September 2014	1.5	Update to IXCOM compile information
May 2014	1.6	Add Macronix models
July 2014	1.7	Repaired doc property title.
September 2014	1.8	Corrected minor word choice issue in format models delivered. Remove version from UG file name. Added info about fast_boot_reg.
December 2014	1.9	Rename top module from flash to flash part number +rtlCommentPragma not needed for IXCOM flow Updated IXCOM compile section. Update related publications list.
February 2015	2.0	Add Execution in Place(XIP) support for Numonyx parts Add new models for Spansion S25FL128S, S25FL256S
March 2015	2.1	Update supported feature information. Add notes about large memory vhdlsparsearray option.
April 2015	2.2	Add Spansion S25FSxxS family models
June 2015	2.3	Correct part number from mx25u51235 to mx66u51235
July 2015	2.4	Update Cadence naming on front page
August 2015	2.5	Add support for Macronix mx25u51245g
August 2015	2.6	Change the memory full path name in the example. Add synthesis options note.
September 2015	2.7	Update Spansion features table and notes.
January 2016	2.8	Update for Palladium-Z1 and VXE
February 2016	2.9	Update Spansion features table and notes. Add XIP support information. Add Spansion s70fs01gs (Includes Any Register & QPI under BETA conditions)
April 2016	3.0	Remove BETA warning for Any Register
July 2016	3.1	Add mmp_spi_clk_gen.v location information Remove hyphen from Palladium naming
October 2016	3.2	Add Enter/Exit command support information for Numonyx
March 2017	3.3	Add 4-byte program/erase support to Numonyx feature list

March 2017	3.4	Remove the beta statements for QPI in Spansion feature list
May 2017	3.5	Correct and add more information for port descriptions
July 2017	3.6	Clarify info about OTP and mem_otp array. Add new Numonyx model n25q256a11 and n25q256a31. Clarify info about RESET# pin.
September 2017	3.7	Rename mx25u3235 to mx25u3235e and add RESET_N pin to generate model mx25u3235f.
October 2017	3.8	Added datasheet revision references table
December 2017	3.9	(1)Added new Macronix model MX25U25645G (2) Updated the Macronix model MX25U51245G from version 0.02 (JUL 2015) to version 1.1 (June ,2017)
January 2018	1.8	Modify header and footer