Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Octal SPI Flash
Palladium Memory Model
User Guide

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

Octal SPI Flash Memory Model

1. Introduction

The Cadence Palladium Octal SPI Flash Memory models are based upon the Micron and Macronix Octal SPI flash datasheets listed below.

Table 1: Datasheet and Revision Level References

Part Number	Rev.	Datasheet Date	Reference Datasheet
Micron (Numonyx)			
mt35xu256	B	DEC 2016	MT35X_QLKA_U_256_ABA_0.pdf
mt35xu512	E	DEC 2016	MT35X_QLKA_U_512_ABA_0_REV_E.pdf
mt35xu01g	E	OCT 2017	MT35X_QLKA_U_01G_BBA_0.pdf
mt35xu02g	C	OCT 2017	MT35X_QLKA_U_02G_CBA_0.pdf
Macronix			
mx25um51245g	1.2	DEC 2016	MX25UM51245G, 1.8V, 512Mb, v1.2.pdf
mx66um1g45g	0.00	MAR 2017	MX66UM1G45G, 1.8V, 1Gb v0.00.pdf
Mx66um2g45g	0.00	MAR 2017	MX66UM2G45Gever000C1702141Cadence.pdf

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Table 2: Release Level for MMP Models

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Features

Table 3: Feature List for Micron Models

Features		Code	Support	Notes
Reset Operations	Reset Enable	66h	Yes	
	Reset Memory	99h	No	
Identification Operations	Read ID	9Eh/9Fh	Yes	1
	Read Serial Flash Discovery Parameter (SFDP)	5Ah	Yes	2
Read Operations	Read	03h	Yes	
	Fast Read	0Bh	Yes	7
	Octal Output Fast Read	8Bh	Yes	7
	Octal I/O Fast Read	CBh	Yes	7
	DDR Octal Output Fast Read	9Dh	Yes	7
	4-Byte Read	13h	Yes	5, 7
	4-Byte Fast Read	0Ch	Yes	5, 7
	4-Byte Octal Output Fast Read	7Ch	Yes	5, 7
	4-Byte Octal I/O Fast Read	CCh	Yes	5, 7
	4-Byte DDR Octal I/O Fast Read	FDh	Yes	5, 7
	Burst16/32/64 wrap around	------	No	
	Execute-in-place (XIP)	------	Yes	3
Write Operations	Write Enable	06h	Yes	
	Write Disable	04h	Yes	
Register Operations	Read Status Register	05h	Yes	
	Read Flag Status Register	70h	Yes	
	Read Non Volatile Configuration Register	B5h	Yes	
	Read Volatile Configuration Register	85h	Yes	
	Tuning Data Pattern Operation	48h/Attr	No	
	Write Status Register	01h	Yes	
	Write Non Volatile Configuration Register	B1h	Yes	4
	Write Volatile Configuration Register	81h	Yes	4
	Clear Flag Status Register	50h	Yes	
	Read/Write Protection Management Register	2Bh	No	
	Read General Purpose Register	96h	Yes	8
Program Operations	Page Program	02h	Yes	
	Octal Input Fast Program	82h	Yes	
	Extended Octal Input Fast Program	C2h	Yes	
	4-Byte Page Program	12h	Yes	5
	4-Byte Octal Input Fast Program	84h	Yes	5
	4-Byte Extended Octal Input Fast Program	8Eh	Yes	5
Erase Operations	32KB Subsector Erase	52h	Yes	
	4KB Sector Erase	20h	Yes	
	Sector Erase	D8h	Yes	
	Bulk Erase	C7h/60h	Yes	
	DIE Erase	C4h	Yes	9
	4-Byte 32KB Subsector Erase	5Ch	Yes	5
	4-Byte 4KB Sector Erase	21h	Yes	5
	4-Byte Sector Erase	DCh	Yes	5
	Program/Erase Suspend	75h	Yes	

Features		Code	Support	Notes
	Program/Erase Resume	7Ah	Yes	
OTP Operations	Read OTP array	4Bh	Yes	
	Program OTP array	42h	Yes	
4-Byte Address Mode Operations	Enter 4-Byte address mode	B7h	Yes	
	Exit 4-Byte address mode	E9h	Yes	
Deep Power Operations	Enter Deep Power Down	B9h	Yes	
	Release Deep Power Down	ABh	Yes	
Advanced Sector Protection Operations	Read Sector Protection	2Dh	Yes	6
	Program Sector Protection	2Ch	Yes	6
	Read Volatile Lock Bits	E8h	Yes	6
	Write Volatile Lock Bites	E5h	Yes	6
	Read Nonvolatile Lock Bits	E2h	Yes	6
	Write Nonvolatile Lock Bits	E3h	Yes	6
	Erase Nonvolatile Lock Bits	E4h	Yes	6
	4-Byte Read Volatile Lock Bits	E0h	Yes	6
	4-Byte Write Volatile Lock Bits	E1h	Yes	6
	Read Global Freeze Bit	A7h	No	
	Write Global Freeze Bit	A6h	No	
	Read Password	27h	No	
	Write Password	28h	No	
	Unlock Password	29h	No	
CRC Operations	CRC Check	-----	No	
Protocol Support	3-Byte Address Mode		Yes	
	4-Byte Address Mode		Yes	
	Extended SPI		Yes	
	Octal DDR SPI		Yes	

Notes:

1. Model accepts command 0x9F to read identification
2. The initial content of the SFDP area is all zeroes, the user can load an image file to the SFDP content in Palladium tools, the name of the SFDP area in the tool is called *mem_param*
3. XIP defined in nonvolatile configuration register is not supported, user can write volatile configuration register to enable XIP instead.
4. The programmable output drive strength is not writable. The programmable dummy cycle configuration is writable.
5. For 4-byte address commands, the model will use 4-byte addressing regardless of the address mode
6. The model will accept advanced section protection commands, but will not activate the protection, only protection defined in status register will be active.
7. For DDR output without DQS, the first data output at the falling clock edge.
8. The registers with general purpose defaults to all 0 as there's no CRC checking in the model.
9. This command is supported by model mt35xu02g and model mt35xu01g.

10. Table 4: Feature List for Macronix Models

Features		Command Code	Support	Notes
Write Operations (SPI & OPI)	Reset Enable	66h	Yes	
	Reset Memory	99h	No	
Identification Operations (SPI & OPI)	Read ID	9Fh	Yes	5,9
	Read Serial Flash Discovery Parameter (RDSFDP)	5Ah	Yes	5
	4-Byte Read (SPI)	13h	Yes	3,5
	4-Byte Fast Read (SPI)	0Ch	Yes	3,5
	8-Byte Octal IO Read (OPI)	ECh	Yes	5
	8-Byte Octal IO DT Read(OPI)	EEh	Yes	5
	READ3B (SPI)	03h	Yes	4,5
	FAST_READ3B (SPI)	0Bh	Yes	4,5
Write Operations (SPI & OPI)	Write Enable	06h	Yes	
	Write Disable	04h	Yes	
Register Operations (SPI & OPI)	Set Burst Length	C0h	Yes	
	Read Status Register	05h	Yes	5,9
	Write Status Register	01h	Yes	
	Read Configuration Register	15h	Yes	5,9
	Write Configuration Register	01h	Yes	
	Read Configuration Register 2	71h	Yes	1,5,9
	Write Configuration Register 2	72h	Yes	1,8
	Read fast boot register	16h	Yes	5,9
	Write fast boot register	17h	Yes	
	Erase fast boot register	18h	Yes	
	Read Security Register	2Bh	Yes	5,9
	Write Security Register	2Fh	Yes	
	Read Lock Register	2Dh	Yes	5,9
	Write Lock Register	2Ch	Yes	
Advanced Sector Protection Operations	Set the WPSEL bit	68h	Yes	4,7,10
	SPB bit program	E3h	Yes	2
	All SPB bit erase	E4h	Yes	2
	Read SPB bit	E2h	Yes	2
	Write the DPB bit	E1h	Yes	4,7
	Read the DPB status	E0h	Yes	4,5,7
	Gang block lock	7Eh	Yes	4,10
	Gang Block unlock	98h	Yes	4,10
	Read Password bit	27h	Yes	4,5,6
	Write Password bit	28h	Yes	4,6
	Unlock Password	29h	Yes	4,6
Program Operations (SPI & OPI)	Page Program (4B)	12h	Yes	
	3B Page Program(SPI)	02h	Yes	4
Erase Operations (SPI & OPI)	4KB Sector erase (4B)	21h	Yes	
	64KB Block Erase (4B)	DCh	Yes	
	4KB Sector erase (3B) (SPI)	20h	Yes	4
	64KB Block Erase (3B) (SPI)	D8h	Yes	4
	Chip Erase	60h/C7h	Yes	
	Program/Erase Suspend	B0h	Yes	
	Program/Erase Resume	30h	Yes	
OTP Operations	Enter secured OTP	B1h	Yes	

(SPI & OPI)	Exit secured OTP	C1h	Yes	
Power Operations (SPI & OPI)	Deep Power Down	B9h	Yes	
	Release from Deep Power Down	ABh	Yes	

Notes:

1. DQSPRC, DOS, DQSSKEW bits in configuration2 register are reserved.
2. These models can accept commands to access the SPB registers, but the protection function cannot be activated in this way.
3. Fast Boot Read is applicable in SPI mode.
4. These commands are added based on MX25UM51245G datasheet REV. 1.2 December 08, 2016.
5. Preamble Enable is not supported.
6. These models can accept commands to access the DPB registers, but the protection function cannot be activated in this way.
7. These models can accept commands to access the PASSWORD register, but the protection function cannot be activated in this way.
8. CRC check mode is not supported.
9. 4 dummy cycles in both STR/DTR.
10. The command can be accepted, but the functions are not supported.

4. Model Block Diagrams

4.1 Interface Diagrams

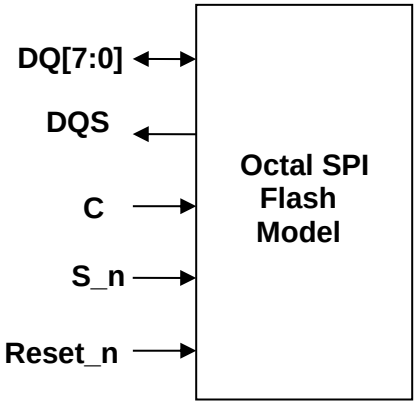

Figure 1: Macronix Octal SPI Flash Model Interface

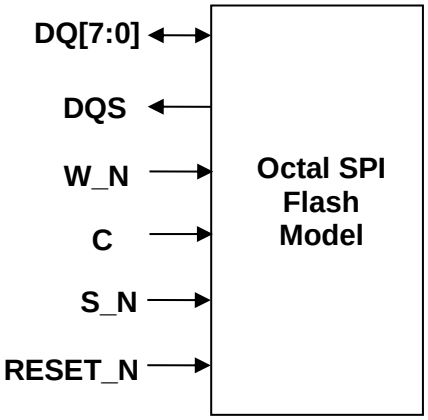

Figure 2: Micron Octal SPI Flash Model Interface

Table 5: Macronix/Micron Signal Names

Signal	Description	I/O
DQ[7:0]	Serial Data input and output	I/O
W_N	Write Protect (Micron Model Only)	In
DQS	Data Strobe for DDR modes	Out
C	Serial Clock	IN
S_N	Chip Select	IN
RESET_N	RESET PIN	IN

4.2 Connection Diagram

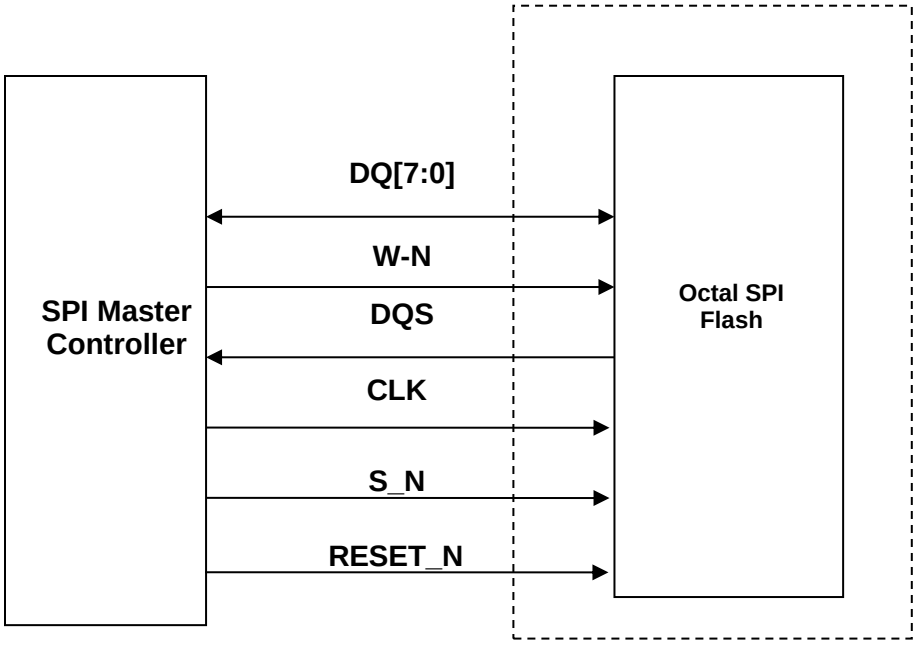

Figure 3: Macronix/Micron Flash Model Connection Diagram

5. Limitations

- Flash Memory and OTP Memory Initial Content
  After download into the Palladium the initial value of the flash memory array is all 0's. Like real Flash parts, the model only allows programming of 1's to 0's. The memory region of the Flash array being programmed must first either be erased with an erase command or initialized to all 1's through the user issuing a memory set command in Palladium runtime tools.

6. Model Emulation

6.1 Emulation Notes

Consider the following when running emulation with the Octal SPI Flash model in Palladium.

- The Octal SPI Flash models are delivered as protected VHDL source with the top-level declaration unprotected and the flash memory and OTP memory unprotected.
  - The main data array is called *mem_array*
  - The OTP array is called *mem_otp*

- The top-level module in the Octal SPI Flash modules is the part number, for example mt35xu512. To use the model in a design, instantiate the top-level module mt35xu512 and map the ports to actual wires. For more details of the top-level declaration, please open the protected VHDL source with a text viewer and search for the top-level module name. Below is the port declaration of the top-level of the Micron model:

```
entity mt35xu512 is
   port (
      c      : in       std_logic;
      dq     : inout  std_logic_vector(7 downto 0);
     dqs    : out     std_logic;
     w_n   : in        std_logic;
     s_n    : in       std_logic;
     reset_n : in    std_logic;
   );
end entity mt35xu512;
```

a

- The initial content of flash memory and OTP memory is all ‘0’s, which will cause the OTP memory to be locked after Palladium emulation is started, and program to the flash memory will not work. The content of flash memory and OTP can be initialize to all ‘1’ in the Memory tab of the questDebug GUI or by issuing commands in the questQel console as below:

```
QEL> memory -set <dspath>.mem_array
QEL> memory -set <dspath>.mem_otp
```

  The user can also erase the flash memory to all ‘1’s by invoking the Chip Erase (CE) instruction after emulation has been started.

  Another command can be used to initialize the memory array to any value. The command is ‘ memory -load %readmemh’， the specific usage format is as follows.

Memory -load %readmemh <full path of the array.array name> -file <full path of the preconfigured data.file name>

Before the command is run, a data file needs to be prepared in advance. The file requires that the beginning of each line be the address data, and then the configuration data that needs to be loaded. The specific format is as follows.

```
@<address1> data1
@<address2> data2
……
```

Using the configuration array in model mt35xu512 as an example, issue the memory -load command to initialize the flash_nv_confg array and the flash_v_confg array. the loading operation is shown as follows:

Step 1: create a data file and make sure all the configuration data is included in the it. Suppose this data file is named mt35xu512_flash_nv_confg.dat and mt35xu512_flash_v_confg.dat.

mt35xu512_flash_nv_confg.dat

```
@000 FF
@001 01
@002 00
@003 FF
@004 00
@005 FF
@006 FE
@007 FF
```

mt35xu512_flash_v_confg.dat

```
@000 FF 01 00 FF 00 FF FE FF
```

Step 2: To check the full path of the *mem_array* or *mem_otp*, please go to the Memory tab in questDebug, or invoke the *memory* command in the questQEL console. Below is an example to get the memory path in the design.

```
QEL> memory
flash_tb.mt35xu512_i.mt32xu512_core_i.mem_array
flash_tb.mt35xu512_i.mt32xu512_core_i.mem_otp
flash_tb.mt35xu512_i.mt32xu512_core_i.mem_param
```

Step 3: run the memory -load command.

```
QEL> memory -load %readmemh flash_tb.flash_i.mt35xu512_core_i.flash_nv_confg

                -file ../data/mt35xu512_flash_nv_confg.data

QEL> memory -load %readmemh flash_tb.flash_i.mt35xu512_core_i.flash_v_confg
```

```
-file ../data/mt35xu512_flash_v_confg.data
```

6.2 Emulation Example

Below is an example of the command list to synthesize the protected RTL files (*.vhdp) into the netlist (*.vgp):

```
vavlog   mmp_spi_clk_gen.v
vavhdl   mt35xu512.vhdp
vaelab   –keepRtlSymbol –keepAllFlipFlop –outputvlog mt35xu512.vgp mt35xu512
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

Below is an example of the command list for importing the Octal SPI Flash model to your design:

```
QEL> delimiterRule Verilog
QEL> importOption {mode full} {protection on} {library libf}
QEL> reflib qtref
QEL> netlistFile "verilog mt35xu512.vgp"
QEL> designImport
QEL> importOption {protection on} {library libf}
QEL> reflib qtref libf
QEL> netlistFile "verilog <your design netlists>"
QEL> designImport
```

6.3 IXCOM Notes

For the IXCOM flow, the Octal SPI model requires an internal clock generator. The module uses an IXCOM clock generator which is SystemVerilog based. As part of the IXCOM compile flow you must include the IXCOMClkGen.sv file from the UXE installation. The mmp_spi_clk_gen.v file can be found in the <MMP install>/common/ directory.

Below is an example.

```
vlan mmp_spi_clk_gen.v

vhan mt35xu512.vhdp

Other design files…

ixcom -ua -top tb +dut+ mt35xu512
```

7. Debugging

This model has several debugging options, techniques and tips that may assist the user may use in isolating a problem. .

- For issues that are may not be model specific please review the *Memory Model Portfolio FAQ for All Models User Guide.*

- **Debug signals:**

  The following signals can be monitored to examine command sequence:

  - cur_cmnd: the current command
  - cur_addr: the current operation address
  - str_oct: octal single transfer rate enabled when str_oct =1
  - dtr_oct: octal double transfer rate enabled when dtr_oct =1
  - mode_pp: program operation flag
  - mode_er: erase operation flag
  - mode_otp: operation OTP space flag
  - dummy_cycle: the dummy cycle number in the register.

  The cur_cmnd signal shows the command letter abbreviation in the simulation waveform, but the value displayed in the Palladium's waveform is not the value on the data sheet; instead, it is the position value of the corresponding command in the enumeration data type. For debug purposes the mapping is shown in the table below.

Table 6: Mapping From Command Code to Signal cur_cmnd for Micron Models

Command name	Command Code	Simulation Display Command Abbreviation	Palladium Display Command Number
Reset Enable	66h	RSTEN	01h
Reset Memory	99h	RSTMMRY	02h
Read ID	9Eh/9Fh	RDID	03h
Read Serial Flash Discovery Parameter (SFDP)	5Ah	RDSFDP	04h
Read	03h	READ	05h
Fast Read	0Bh	FREAD	06h
Octal Output Fast Read	8Bh	FREAD_OCT	07h
Octal I/O Fast Read	CBh	FREAD_OCT_IO	08h
DDR Octal Output Fast Read	9Dh	FREAD_OCT_DDR	09h
4-Byte Read	13h	READ4B	0Ah
4-Byte Fast Read	0Ch	FREAD4B	0Bh
4-Byte Octal Output Fast Read	7Ch	FREAD4B_OCT	0Ch
4-Byte Octal I/O Fast Read	CCh	FREAD4B_OCT_IO	0Eh
4-Byte DDR Octal I/O Fast Read	FDh	FREAD4B_OCT_DDR	0Fh
Write Enable	06h	WREN	10h
Write Disable	04h	WRDI	11h
Read Status Register	05h	RDSR	12h
Read Flag Status Register	70h	RFSR	13h
Read Non Volatile Configuration Register	B5h	RDNVCR	14h
Read Volatile Configuration Register	85h	RDVCR	15h
Write Status Register	01h	WRSR	16h
Write Non Volatile Configuration Register	B1h	WRNVCR	17h
Write Volatile Configuration Register	81h	WRVCR	18h
Clear Flag Status Register	50h	CLFSR	19h
Read General Purpose Register	96h	RDGP	31h
Page Program	02h	PP	1Ah
Octal Input Fast Program	82h	PP_OCT	1Bh
Extended Octal Input Fast Program	C2h	PP_OCT_IO	1Ch
4-Byte Page Program	12h	PP4B	1Dh
4-Byte Octal Input Fast Program	84h	PP4B_OCT	1Eh
4-Byte Extended Octal Input Fast Program	8Eh	PP4B_OCT_IO	1Fh
32KB Subsector Erase	52h	SE32K	22h
4KB Sector Erase	20h	SSE	21h
Sector Erase	D8h	SE	20h
Bulk Erase	C7h/60h	CE	23h
DIE Erase	C4h	CE	23h
4-Byte 32KB Subsector Erase	5Ch	SE32K4B	26h
4-Byte 4KB Sector Erase	21h	SSE4B	25h
4-Byte Sector Erase	DCh	SE4B	24h
Program/Erase Suspend	75h	PES	27h

Command name	Command Code	Simulation Display Command Abbreviation	Palladium Display Command Number
Program/Erase Resume	7Ah	PER	28h
Read OTP array	4Bh	ROTP	29h
Program OTP array	42h	POTP	2Ah
Enter 4-Byte address mode	B7h	ENT4B	2Bh
Exit 4-Byte address mode	E9h	EXT4B	2Ch
Enter Deep Power Down	B9h	DP	2Dh
Release Deep Power Down	ABh	RDP	2Eh
READ SECTOR PROTECTION	2Dh	RDSP	2Fh
PROGRAM SECTOR PROTECTION	2Ch	PSP	30h
READ VOLATILE LOCK BITS	E8h	RDVLB	32h
WRITE VOLATILE LOCK BITS	E5h	WRVLB	33h
READ NONVOLATILE LOCK BITS	E2h	RDNVLB	36h
WRITE NONVOLATILE LOCK BITS	E3h	WRNVLB	37h
ERASE NONVOLATILE LOCK BITS	E4h	ERNVLB	38h
4-BYTE READ VOLATILE LOCK BITS	E0h	RD4BVLB	34h
4-BYTE WRITE VOLATILE LOCK BITS	E1h	WR4BVLB	35h
READ GLOBAL FREEZE BIT	A7h	RDGFB	39h
WRITE GLOBAL FREEZE BIT	A6h	WRGLB	3Ah
READ PASSWORD	27h	RDPASD	3Bh
WRITE PASSWORD	28h	WRPASD	3Ch
UNLOCK PASSWORD	29h	UPASD	3Dh

Table 7: Mapping From Command Code to Signal cur_cmnd for Macronix Models

Command name	Command Code	Command Abbreviation in Simulation Waveform	Command Number in Palladium Waveform
Reset Enable	66h	RSTEN	1Fh
Reset Memory	99h	RSMMRY	20h
Read ID	9Fh	RDID	03h
Read Serial Flash Discovery Parameter (RDSFDP)	5Ah	RDSFDP	14h
4-Byte Read (SPI)	13h	READ4B	25h
4-Byte Fast Read (SPI)	0Ch	FREAD4B	26h
8-Byte Octal IO Read (OPI)	ECh	READ8	2Ah
8-Byte Octal IO DT Read(OPI)	EEh	DTRD8	55h
READ3B (SPI)	03h	READ	06h
FAST_READ3B (SPI)	0Bh	FREAD	07h
Write Enable	06h	WREN	01h
Write Disable	04h	WRDI	02h
Set Burst Length	C0h	SBL	3Bh
Read Status Register	05h	RDSR	04h
Write Status Register	01h	WRSR	05h
Read Configuration Register	15h	RDCR	3Ah
Write Configuration Register	01h	WRSR	05h
Read Configuration Register 2	71h	RDCR2	46h

Write Configuration Register 2	72h	WRCR2	47h
Read fast boot register	16h	RDFBR	3Dh
Write fast boot register	17h	WRFBR	3Eh
Erase fast boot register	18h	ESFBR	3Fh
Read Security Register	2Bh	RDSCUR	44h
Write Security Register	2Fh	WRSCUR	45h
Read Lock Register	2Dh	RDLR	49h
Write Lock Register	2Ch	WRLR	48h
SPB bit program	E3h	WRSPB	4Ah
All SPB bit erase	E4h	ESSPB	4Bh
Read SPB status	E2h	RDSPB	4Ch
Write the PASS Register	28h	WRPASS	53h
Read the PASS Register	27h	RDPASS	52h
Write the DPB bit	E1h	WRDPB	4Dh
Read the DPB status	E0h	RDDPB	4Eh
Set the WPSEL bit	68h	WPSEL	51h
Page Program (4B)	12h	PP4B	1Bh
3B Page Program(SPI)	02h	PP	0Ch
4KB Sector erase (4B)	21h	SSE4B	33h
64KB Block Erase (4B)	DCh	SE4B	35h
4KB Sector erase (3B) (SPI)	20h	SSE	10h
64KB Block Erase (3B) (SPI)	D8h	SE	0Fh
Chip Erase	60h/C7h	CE	11h
Program/Erase Suspend	B0h	PES	1Dh
Program/Erase Resume	30h	PER	1Ch
Enter secured OTP	B1h	ENSO	42h
Exit secured OTP	C1h	EXSO	43h
Deep Power Down	B9h	DP	12h
Release from Deep Power Down	ABh	RDP	13h

Revision History

The following table shows the revision history for this document

Date	Version	Revision
July 2015	1.0	Initial Release
August 2015	1.1	Change the memory path name in the example
August 2015	1.2	Change note for DQS timing for Micron models. Add synthesis options note.
January 2016	1.3	Update for Palladium-Z1 and VXE
July 2016	1.4	Add mmp_spi_clk_gen.v location information Remove hyphen from palladium naming
August 2016	1.5	Add more feature support info to feature list. Remove BETA watermark for general release.
September 2016	1.6	Add new feature support info from latest Micron datasheet to Model feature list
October 2016	1.7	Corrected naming for 4-Byte DDR Octal I/O Fast Read in Features Table
November 2016	1.8	Update Micron Protocol support information in Features Table
February 2017	1.9	Add dummy cycle configuration feature to Micron models Change the 4-byte address command descriptions to Micron models
July 2017	2.0	Clarify OSPI RESET# pin info
September 2017	2.1	Add reset_n pin for the models
September 2017	2.2	Add READ3B and FAST_READ3B commands for the model mx25um51245g based on the datasheet Version 1.2 dated December 2016.
November 2017	2.3	1. Add PP3B, SE3B,BE3B commands for the model mx25um51245g. 2. Add RDPASS, WRPASS, PASSULK, RDDPB,WRDPB and WPSEL commands for the model mx25um51245g. 3. Add the Password Register, Dynamic Write Protection Bits and 8 Configuration Register 2 for the model. 4. Updated the dummy cycle number from 2 to 4 under the STR-OPI model for these commands RDSR, RDCR,RDCR2,RDFBR,RDSCUR,RDLR,RDID . All of the effort toward 1 through 4 are based on the datasheet Version 1.2 dated December 2016. 5. Add note 5 through note 9 for the Macronix mx25um51245g model. 6. Add code number for the feature list table 3 and table 4.
December 2017	2.4	Added new micron model mt35xu02g.
December 2017	2.5	Added new micron model mt35xu01g and model mt35xu256.
January 2018	2.6	Modify header and footer
March 2018	2.7	Updated Emulation Notes, added loading methods, commands, and examples for loading data to memory array. Added Debugging section

May 2018	2.8	1.Added new macronix model mx66um1g45g and model mx66um2g45g. 2. Updated Feature List for Macronix Models table.