



**Hardware System Verification (HSV)  
Vertical Solutions Engineering (VSE)**

**OctaRAM  
Palladium Memory Model  
User Guide**

**Document Version: 1.1**

**Document Date: July 2018**

## OctaRAM Palladium Memory Model

**Copyright** © 2018 Cadence Design Systems, Inc. All rights reserved.  
Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

**Trademarks:** Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522. All other trademarks are the property of their respective holders.

**Restricted Permission:** This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

**Disclaimer:** Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

**Restricted Rights:** Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

# Contents

<b>GENERAL INFORMATION</b>	<b>4</b>
1.1 RELATED PUBLICATIONS	4
<b>OCTARAM MEMORY MODEL</b>	<b>5</b>
1. INTRODUCTION	5
2. MODEL RELEASE LEVELS	6
3. FEATURES	7
4. MODEL BLOCK DIAGRAM	8
5. I/O SIGNAL DESCRIPTION	8
6. MODEL PARAMETER DESCRIPTIONS	9
7. ADDRESS MAPPING	10
8. INITIALIZATION SEQUENCE	10
9. CONFIGURATION REGISTER	10
10. LIMITATIONS	11
11. COMPILE AND EMULATION	11
12. DEBUGGING	12
REVISION HISTORY	14

## List of Figures

FIGURE 1: JSC OCTARAM MODEL BLOCK DIAGRAM	8
---	---

## List of Tables

TABLE 1: RELEASE LEVEL FOR MMP MODELS	6
TABLE 2: FEATURE LIST FOR JSC OCTARAM MODELS	7
TABLE 4: JSC OCTARAM MODEL I/O SIGNALS	8
TABLE 6: USER ADJUSTABLE PARAMETERS	9
TABLE 7: VISIBLE NON-USER-ADJUSTABLE LOCALPARAM	9
TABLE 7: CONFIGURATION REGISTER	10

---

## General Information

---

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

### 1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

- UXE User Guide
- UXE Library Developer's Guide
- UXE Known Problems and Solutions
- UXE Command Reference Manual
- Palladium XP Planning and Installation Guide
- Palladium Target System Developer's Guide
- What's New in UXE

For Palladium Z1:

- VXE User Guide
- VXE Library Developer's Guide
- VXE Known Problems and Solutions
- VXE Command Reference Manual
- Palladium Z1 Planning and Installation Guide
- Palladium Target System Developer's Guide
- What's New in VXE

---

## OctaRAM Memory Model

---

### 1. Introduction

The Cadence Palladium OctaRAM Memory model is now available in Verilog based format (\*.vp) for some families with configurations matching real OctaRAM parts.

Various sizes are available. Please consult the memory model catalog for the currently available configurations list.

Vendor	Part Number	File Name of Reference Datasheet	Revision	Revision Date
JSC	jsc64ssp8agdy	JSC64SSP8AGDY_1.8V_Rev1.0_20170327.pdf	v1.0	03/27/2017
	jsc64ssu8agdy	JSC64SSU8AGDY_3V_Rev1.0_20170327.pdf	v1.0	03/27/2017
	jsc28ssp8agdy	JSC28SSP8AGDY_1.8V_Rev1.0_20170327.pdf	v1.0	03/27/2017
	jsc28ssu8agdy	JSC28SSU8AGDY_3V_Rev1.0_20170327.pdf	v1.0	03/27/2017

## 2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

**Table 1: Release Level for MMP Models**

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

### 3. Features

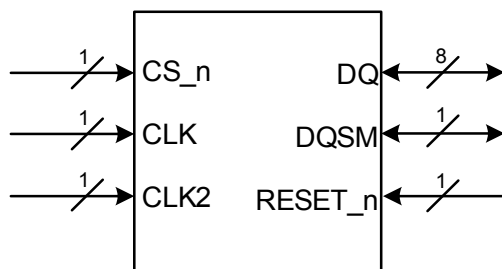
The JSC OctaRAM memory model supports all the features listed in the table below.

**Table 2: Feature List for JSC OctaRAM Models**

Features	Support	Notes
Memory Read with continuous burst	Yes	
Memory Read with wrapped burst	Yes	
Memory Write with continuous burst	Yes	
Memory Write with wrapped burst	Yes	
Identification Register (read only)	Yes	
Configuration Register Read	Yes	
Configuration Register Write	Yes	
Data Learning Pattern Read	Yes	

#### 4. Model Block Diagram

The following figure shows the OctaRAM model block diagram. The CLK2 is not required for jsc64ssp8agdy and jsc64ssu8agdy.



**Figure 1: JSC OctaRAM Model Block Diagram**

#### 5. I/O Signal Description

The table below lists and describes the model I/O signals.

**Table 3: JSC OctaRAM Model I/O Signals**

NAME	TYPE	DESCRIPTION
CS_n	Input	<b>Chip Select:</b> Activates the device when Low.
CLK	Input	<b>Clock:</b> Command, address and data information are sampled at the posedge or negedge of the CLK signal.
CLK2	Input	<b>Clock2:</b> 90-degree phase shifted clock input behind CLK for DQSM output.
DQ	I/O	<b>Data Input/Output:</b> During read and write operation, the command, address and data information are transferred on the DQ signals.
DQSM	I/O	<b>Read Data Strobe/Write Mask:</b> Variable data strobe operation for read. Used as data mask during write operation.
RESET_n	Input	<b>RESET:</b> Hardware reset device when low. RESET_n pin has internal pull up.



## 6. Model Parameter Descriptions

The following table provides details on the user adjustable parameters for the Palladium OctaRAM memory model. These parameters may be modified when instantiating a OctaRAM wrapper or, if necessary, by modifying the HDL parameter declarations and default values which are exposed for access and debug visibility.

**Table 4: User Adjustable Parameters**

User Adjustable Parameter	Default Value	Description
col_width	10	The column address width
row_width	14	The row address width
REFRESH_INTERVAL_CNT	800	Refresh interval default value
REFRESH_TIME_CNT	8	Refresh time value
init_banner_on	1	Display init banner control
model_name	-	Model name
num_of_die	1	Die number

The following table provides some information about exposed localparams that are NOT user adjustable. On rare occasion the user may find one of these localparam needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

**Table 5: Visible Non-User-Adjustable Localparam**

Localparam	Default Value	Description
model_version	-	Model Version
Mb_size	-	Model Size
CR_DEFAULT	jsc28ssp8agdy:16'hF052 jsc28ssu8agdy:16'hF022 jsc64ssp8agdy:16'hF052 jsc64ssu8agdy:16'hF022	Configuration register default value
DEVICE_ID	jsc28ssp8agdy:16'h6D9A jsc28ssu8agdy:16'h2D9A jsc64ssp8agdy:16'h6C9A jsc64ssu8agdy:16'h2C9A	Device ID value

Note that there are additional exposed localparams in the model HDL that are not described here nor intended to be described here. These additional localparams are exposed for debugging purposes only and will not be described herein.

## 7. Address mapping

The array of the OctaRAM model is mapped into the internal memory of the Palladium system. This array is a two-dimensional array of signals. The array width is 16bit and the address of the memory array is word address. The mapping of row and column addresses to the internal model array is as follows:

$$\text{ARRAY\_ADDR} = \{\text{RA}, \text{CA}\} \gg 1;$$

The array name in the model is: memcore

## 8. Initialization Sequence

The OctaRAM memory model does not have any requirement for initialization sequence.

## 9. Configuration Register

The OctaRAM memory model supports the configuration register as listed below.

**Table 6: Configuration register**

Fields	Name	Description
CR[15]	Deep Power down	0b: Deep Power down entry 1b: Normal (default)
CR[14:12]	Driver Strength	000b: 146 ohms 001b: 76 ohms 010b: 52 ohms 011b: 41 ohms 100b: 34 ohms 101b: 30 ohms 110b: 26 ohms 111b: 24 ohms (default)
CR[11:9]	Reserved	000b
CR[8]	DQSM Read Pre-cycle	0b: 0 clock (default) 1b: 1 clock
CR[7:4]	Latency counter	0000b: 3 clocks 0001b: 4 clocks 0010b: 5 clocks 0011b: 6 clocks 0100b: 7 clocks 0101b: 8 clocks (default) others: reserved
CR[3]	Initial Access Latency	0b: Variable Latency (default) 1b: Fixed Latency
CR[2]	CLK2 Input	0b: Not support (default) 1b: Support
CR[1:0]	Burst Wrap Length	00b: 128 bytes 01b: 64 bytes 10b: 32 bytes (default) 11b: 16 bytes

Note:

The CR[7:4] latency counter default value is 0101b (8 clocks) for jsc28ssp8agdy and jsc64ssp8agdy; default value is 0010b (5 clocks) for jsc28ssu8agdy and jsc64ssu8agdy. The CR[2] is reserved and must be set to '0b' for jsc64ssp8agdy and jsc64ssu8agdy.

## 10. Limitations

All the supported and unsupported features are listed in the Table 2: Feature List for JSC OctaRAM Models.

## 11. Compile and Emulation

The model is provided as protected RTL files (\*.vp). The files need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64bit -ua +sv +dut+jsc28ssp8agdy \  
    ./jsc28ssp8agdy.vp \  
    -incdir ../../../../utils/cdn_mmp_utils/sv \  
    ../../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \  
    .....  
  
xeDebug -64 --ncsim \  
    -sv_lib ../../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \  
    -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis. The first uses script commands and the second uses command line commands:

```
1)  
hdlInputFile jsc28ssp8agdy.vp  
hdlImport -full -2001 -l qtref  
hdlOutputFile -add -f verilog jsc28ssp8agdy.vg  
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -  
keepAllFlipFlop jsc28ssp8agdy  
.....  
  
2)  
vavlog jsc28ssp8agdy.vp  
  
vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog  
jsc28ssp8agdy.vg jsc28ssp8agdy  
.....
```

**NOTE:** It is common for Palladium flows to require `-keepallFlipFlop` since it removes optimizations that are in place by default. For example, without `-keepAllFlipFlop`, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode ( `-atb` ) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require `-keepRtlSymbol`. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as “.”, whenever possible. In other words, it maps VHDL RTL signal name `a.b` to the netlist entry, `\a.b`. Without this modifier, the signal name would otherwise be converted to `a_b` in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

## 12. Debugging

The OctaRAM model has several debugging options techniques and tips that may assist the user in isolating a problem.

- For issues that may not be OctaRAM specific please review the *Memory Model Portfolio FAQ for All Models User Guide*.
- **Golden waveform:** A package with a reference waveform is available which shows the following command sequence:

- (1) Hardware Reset operation
- (2) Read ID operation
- (3) Memory Write with continuous burst  
Memory Read with continuous burst
- (4) Memory Write with wrapped burst  
Memory Read with wrapped burst
- (5) Data Learning Pattern Read

- **Debug Display:** The Palladium OctaRAM memory model has available a built-in debug methodology called MMP Debug Display that is based on the Verilog system task `$display`. Please see the *Palladium Memory Model Debug Display User Guide* in the release docs directory for additional information.
- **Manual Configuring of this MMP Model Family**

This MMP model supports manual configuration by accompanying the model mode register or configuration register declarations with synthesis directives, such as `keep_net` directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing. For a general description of this support please see the user guide in the MMP release with path and filename `docs/MMP_FAQ_for_All_Models.pdf`.

While MMP strongly recommends following protocol-based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments.

The following table lists the internal register path and naming along with the specification or datasheet naming for model mode registers or configuration registers that are accompanied by `keep_net` synthesis directives in support of such manual configuration.

## OctaRAM Palladium Memory Model

ONLY writeable configuration registers or fields are supported thusly. Please read the relevant datasheet for details about individual register behavior and mapping to fields.

**Table 7: Writeable Mode Register / Configuration Register Info**

Hierarchical RTL Naming for Writeable Configuration Related Registers & Signals	Specification or Vendor Datasheet Naming for Configuration Related Registers	Access
<model_name>.cr	Configuration Register	R/W

## Revision History

The following table shows the revision history for this document

Date	Version	Revision
April 2018	0.1	Initial release
May 2018	1.0	Move from BETA to MR Add section for Manual configuration
July 2018	1.1	Update for new utility library