

Horizon X2A&J2A LPDDR4 & LPDDR4X System Simulation

Electrical Lab.

ASE Group Kaohsiung

Sep. 10, 2019



Outline

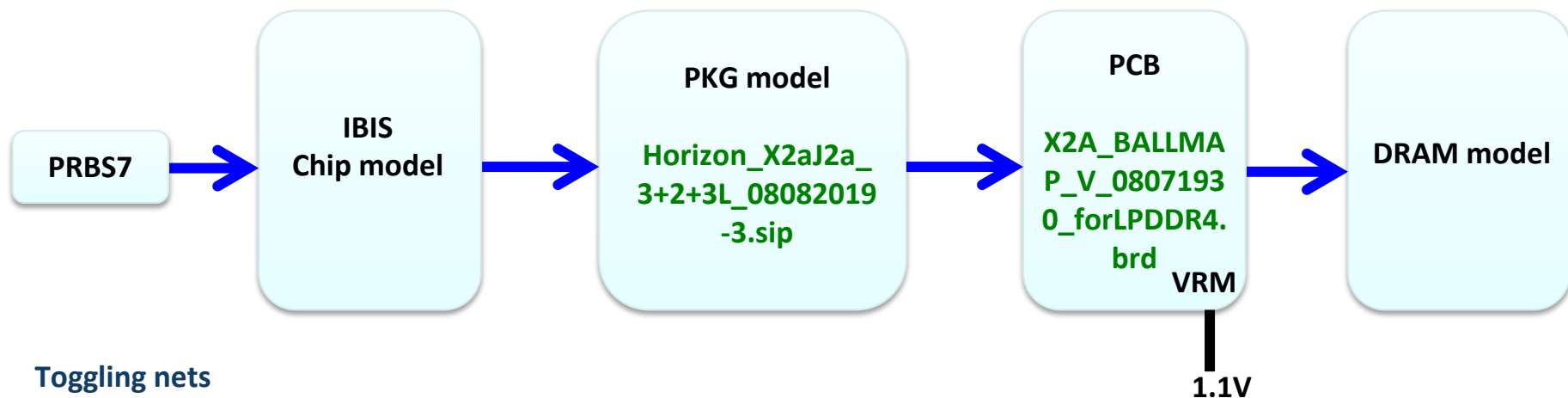
- **LPDDR4**
 - SI Part
 - PI Part
 - AR
- **LPDDR4X**
 - SI Part
 - PI Part



LPDDR4



Write mode Schematic



➤ Toggling nets

- Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A
- Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A
- Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B
- Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B
- CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A
- CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B

➤ Chip model : dwc_ddrphy_tbxrdq_ns_clipped_lpd4.ibs, dwc_ddrphy_tbxrdqs_ns_clipped_lpd4.ibs, dwc_ddrphy_tbxrca_ns_clipped_lpd4.ibs

- DQ : mal4drv27_dl4_40
- DQS: mal4drv27_dl4_40
- CA: mal4drv27_dl4_40
- CLK: mal4drv27_dl4_40

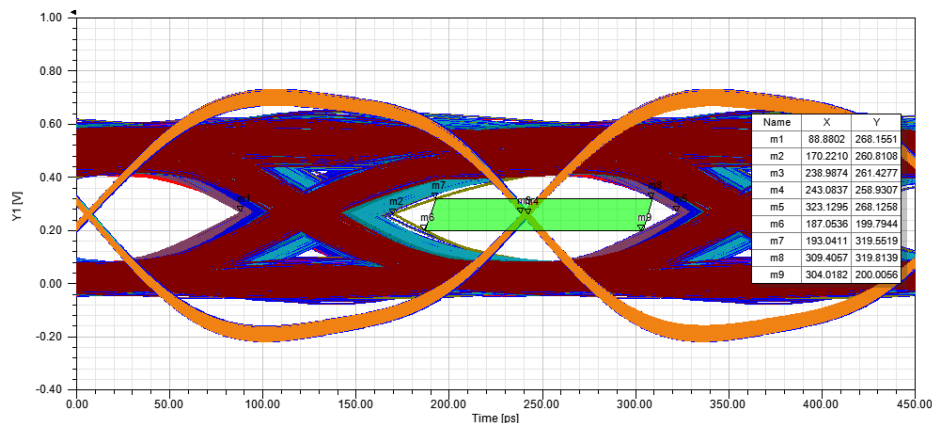
➤ On-die decap : 3.6nF & 4.4mohm

➤ DRAM model : z11m_1p1v_at.ibs

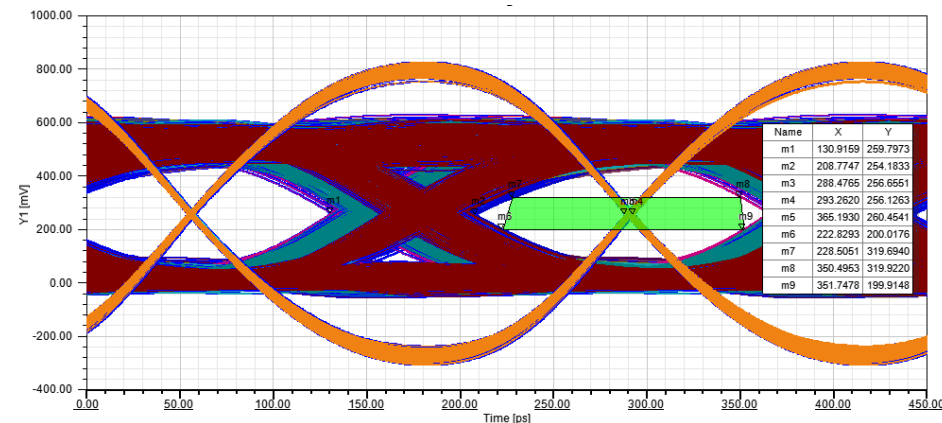
- | | |
|---------------------------|------------------------------|
| ➤ DQ_IN_ODT40_VOH25_4266 | ➤ CA_INPUT_ODT40_VOH25_4266 |
| ➤ DQS_IN_ODT40_VOH25_4266 | ➤ CLK_INPUT_ODT40_VOH25_4266 |

DQ Write Mode

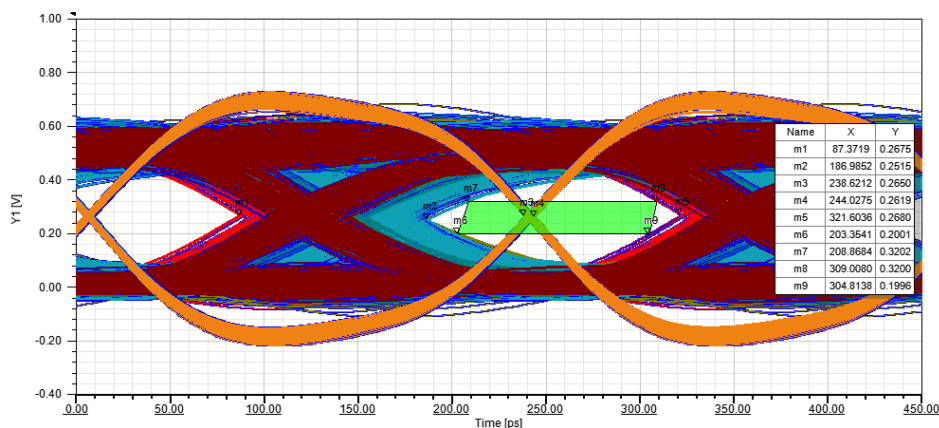
Vac & Vdc: 0.26 +/- 0.06V (320mv & 200mv)



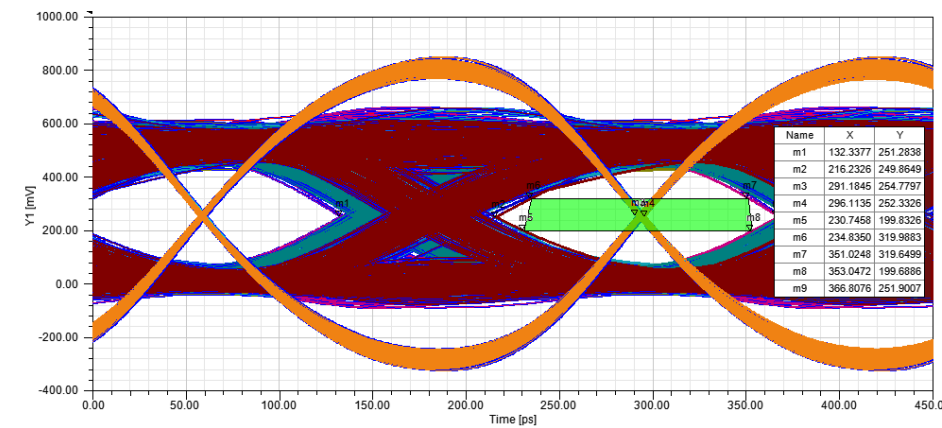
DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A



DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A



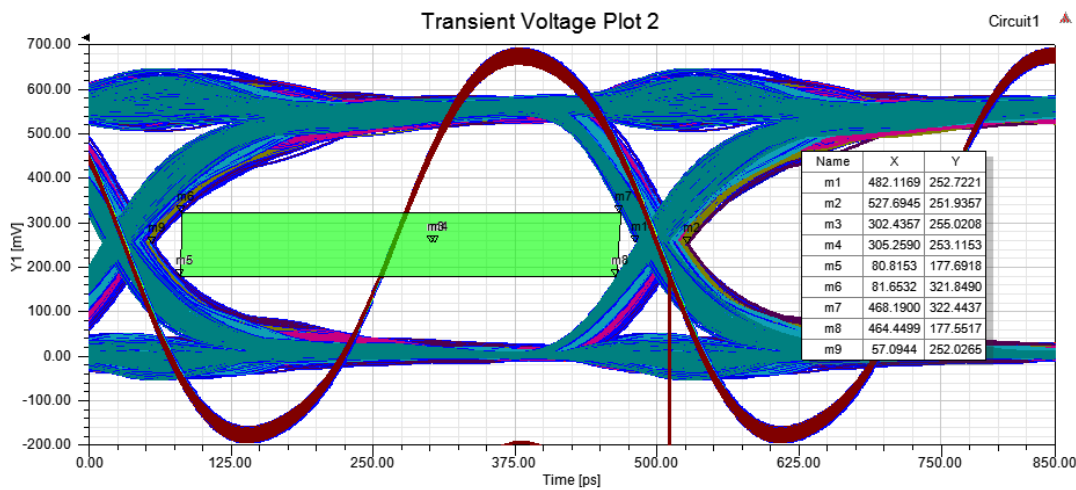
DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B



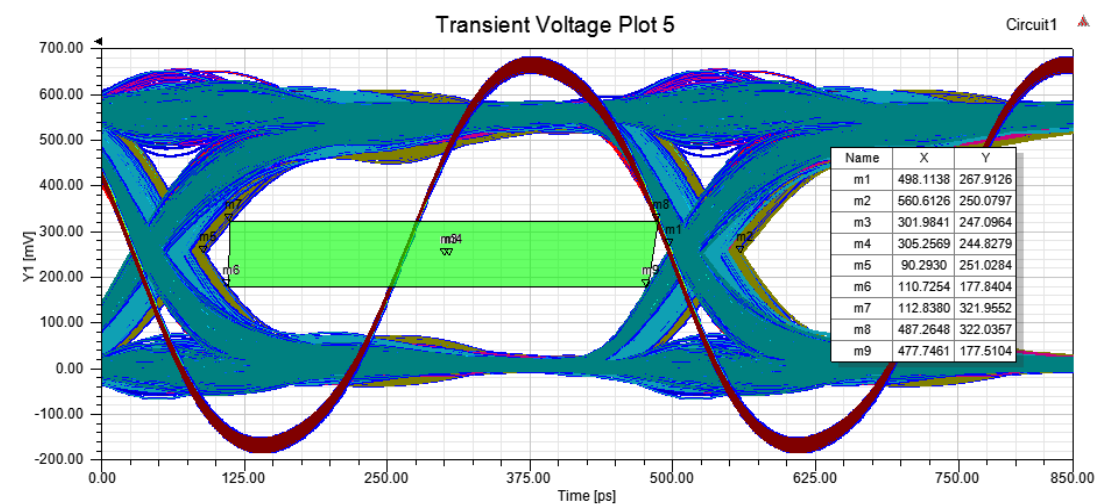
DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

CA Write Mode

Vac & Vdc: 0.25 +/- 0.0725V (322.5mv & 177.5mv)



CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A,
DRAM_CK_C_A, DRAM_CK_T_A



CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B,
DRAM_CK_C_B, DRAM_CK_T_B

Write Mode Simulation Result

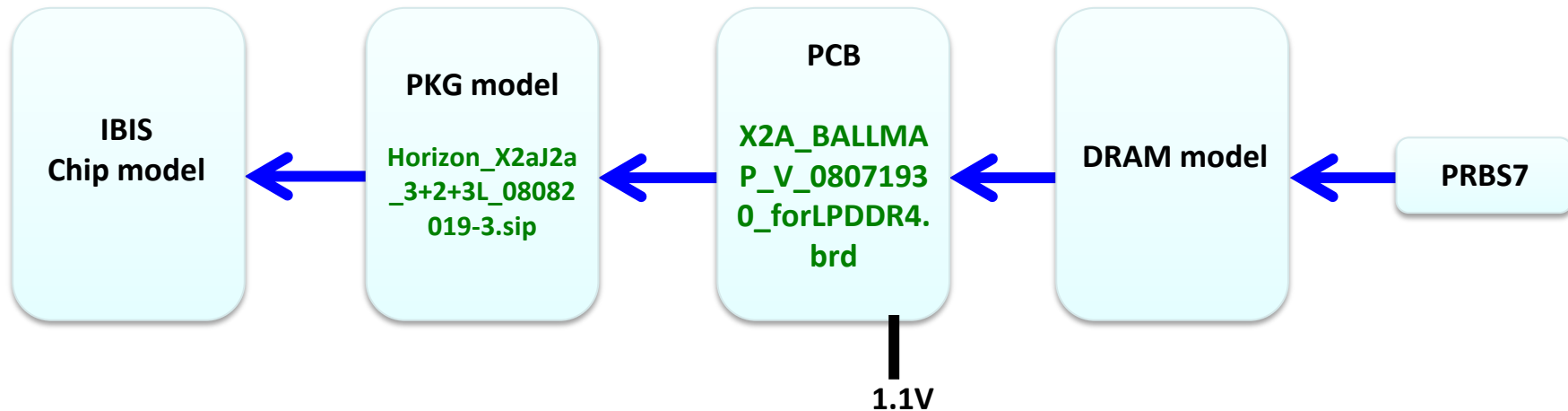
DQ Write Mode

Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	81	78	100	84	-
DQS Jitter (ps)	4	5	5	5	-
TdIPW_total (UI)	0.65	0.67	0.58	0.64	0.45
TdIVW_total (UI)	0.47	0.52	0.41	0.49	0.25

CA Write Mode

Items	CA_1	CA_2	SPEC
CA Skew+Jitter (ps)	46	63	-
CLK Jitter (ps)	3	3	-
TclPW_total (UI)	0.91	0.87	0.6
TclVW_total (UI)	0.81	0.78	0.3

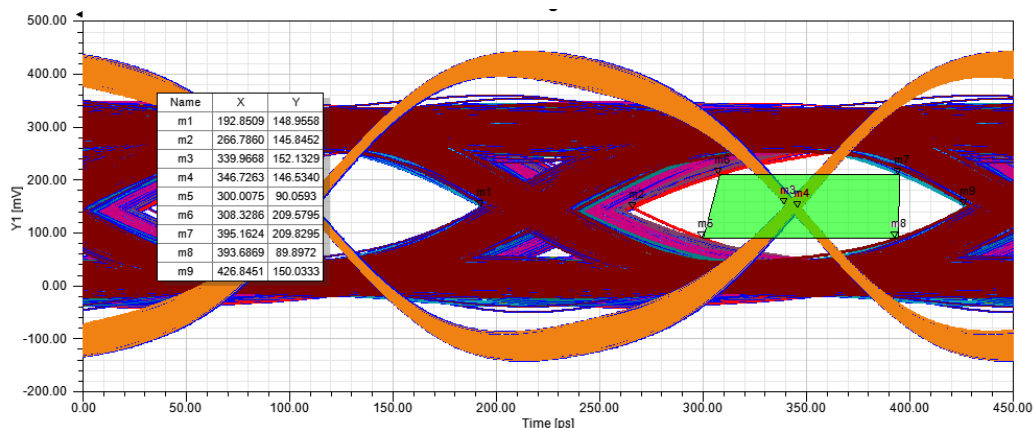
Read mode Schematic



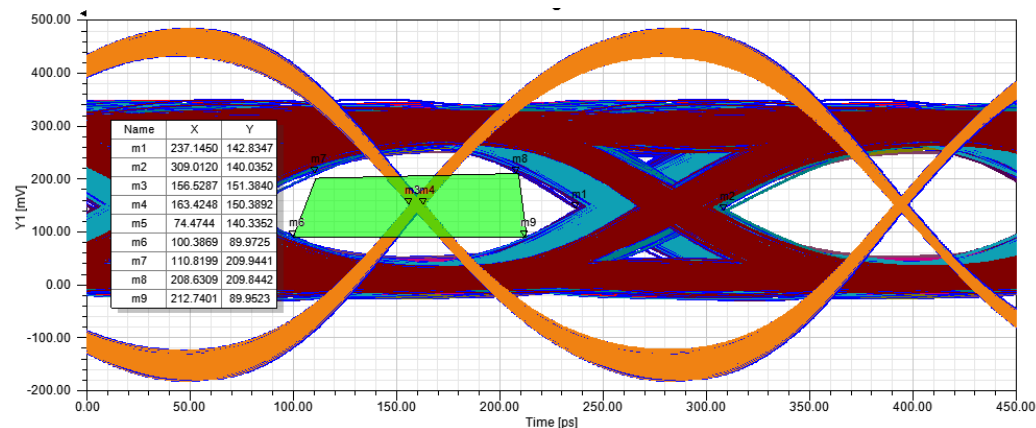
- **Toggling nets**
 - **Byte 1:** DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A
 - **Byte 2:** DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A
 - **Byte 3:** DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B
 - **Byte 4:** DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B
- **Chip model :** dwc_ddsphy_txrdq_ns_clipped_lpd4.ibs, dwc_ddsphy_txrdqs_ns_clipped_lpd4.ibs
 - DQ : mal4drv27_dl4_odt40
 - DQS: mal4drv27_dl4_odt40
- **On-die decap : 3.6nF & 4.4mohm**
- **DRAM model : z11m_1p1v_at.ibs**
 - DQ_PD40_ODTDIS_VOH25_4266
 - DQS_PD40_ODTDIS_VOH25_4266

DQ Read Mode

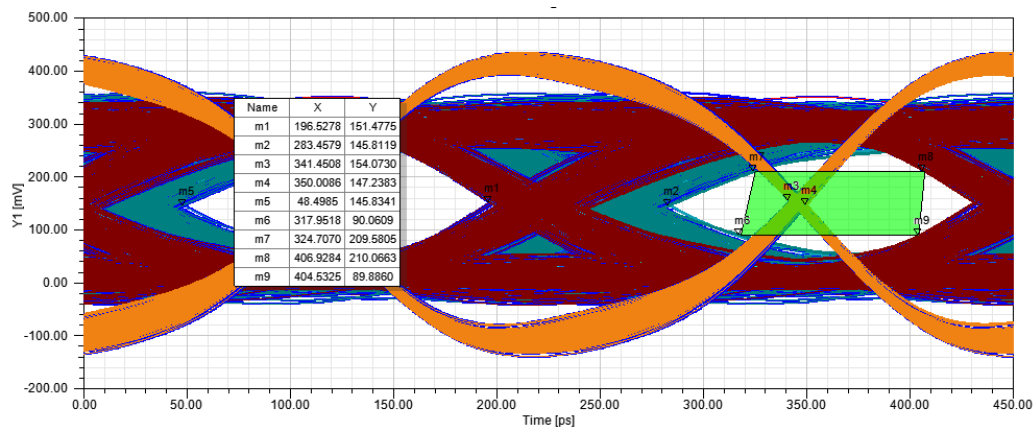
Vac & Vdc: 0.15 +/- 0.06V (210mv & 90mv)



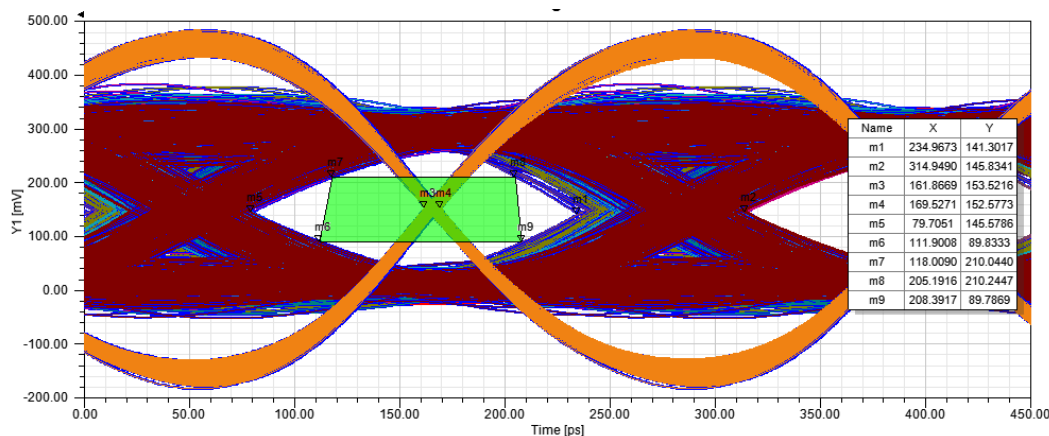
DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A



DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A



DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B



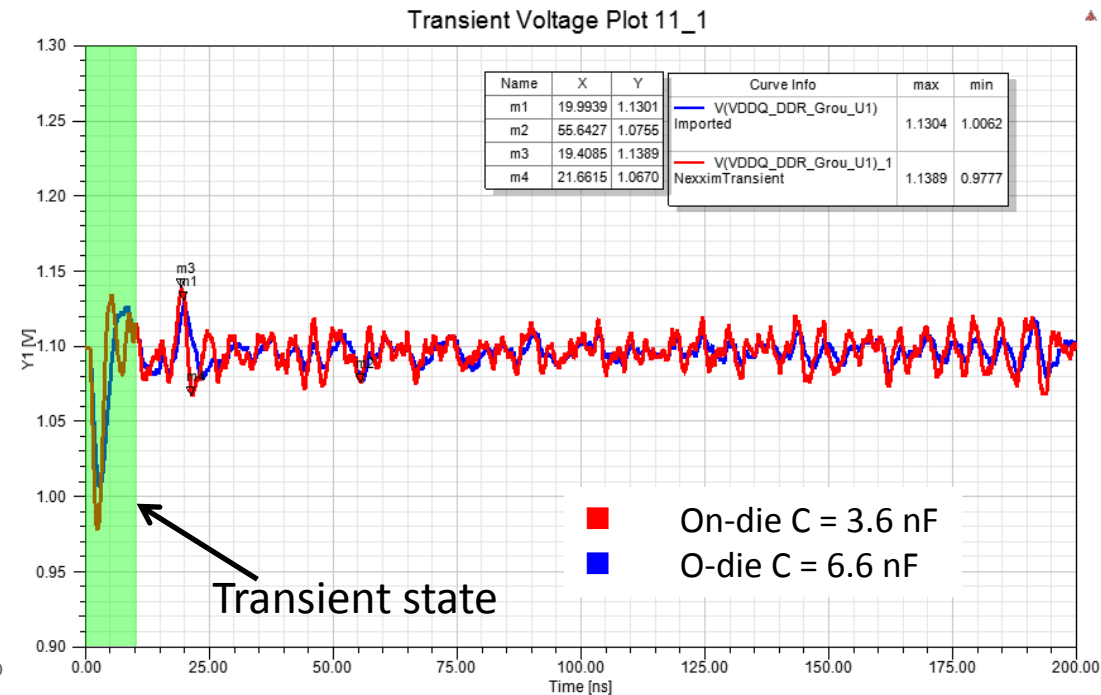
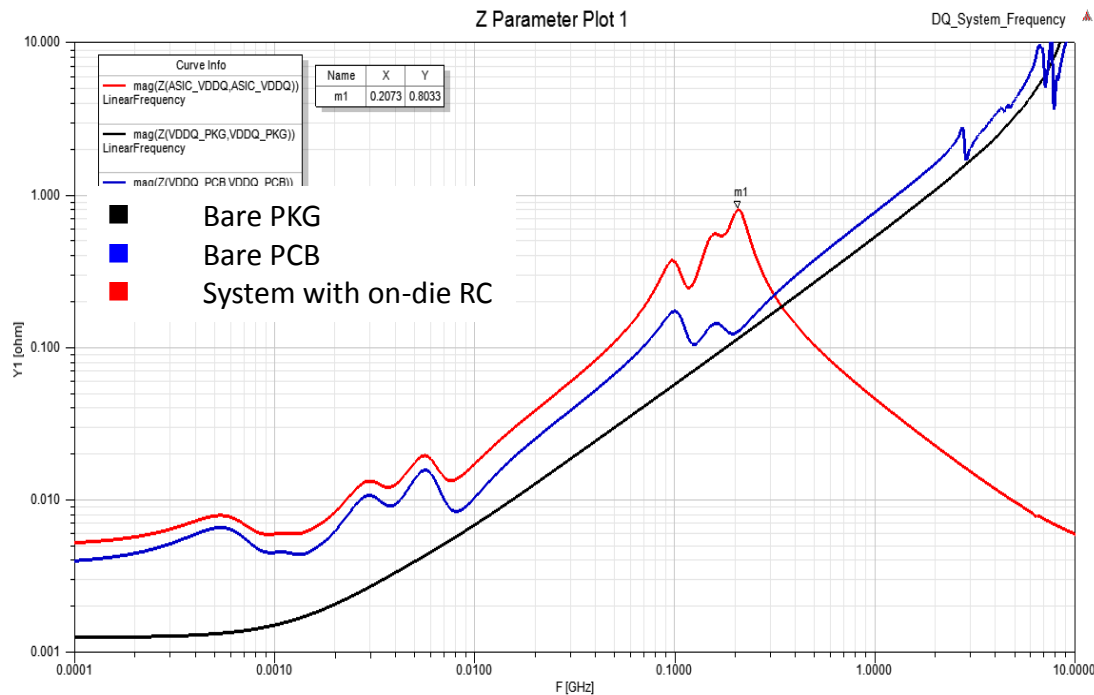
DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

Read Mode Simulation Result

DQ Read Mode

Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	73	72	86	80	-
DQS Jitter (ps)	7	7	9	8	-
TdIPW_total (UI)	0.68	0.7	0.63	0.66	0.45
TdIVW_total (UI)	0.37	0.41	0.35	0.37	0.25

VDDQ_DDR



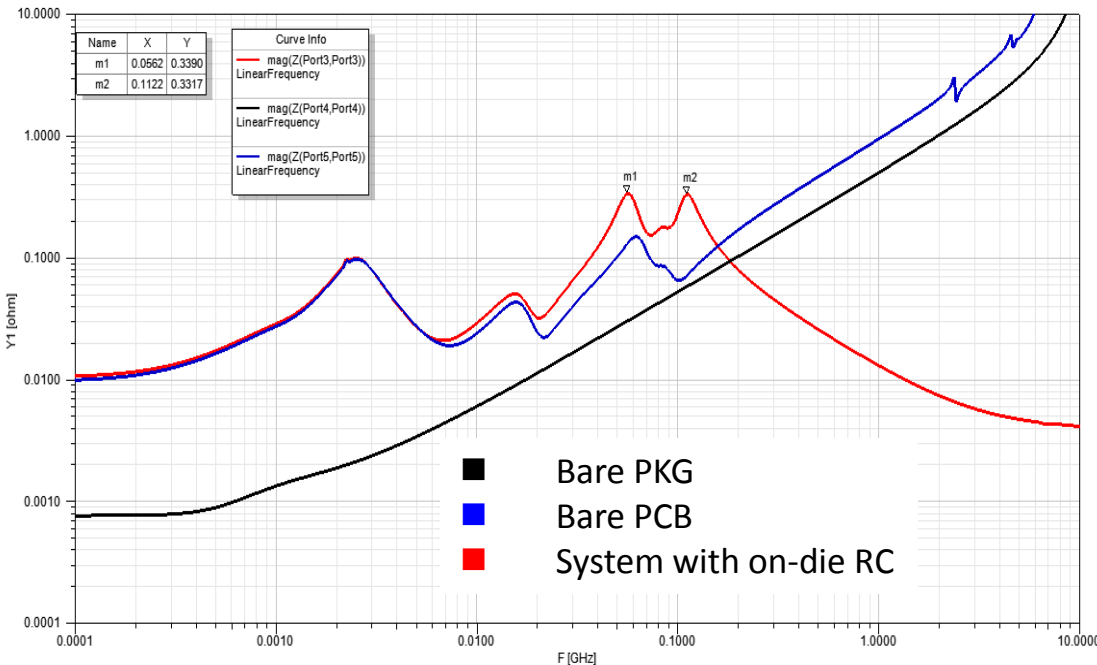
- Transient state (0 ~ 10ns):
 - On-die C => 3.6 nF: P2P Noise = 2.3% ~ -11%
 - On-die C => 6.6 nF: P2P Noise = 2.1% ~ -8.5%
- Steady state (10 ~ 200ns):
 - On-die C => 3.6nF: P2P Noise = 3% ~ -3%
 - On-die C => 6.6nF: P2P Noise = 2.7% ~ -2.3%

- SPEC: +/- 2.5% noise

VDD_DDR

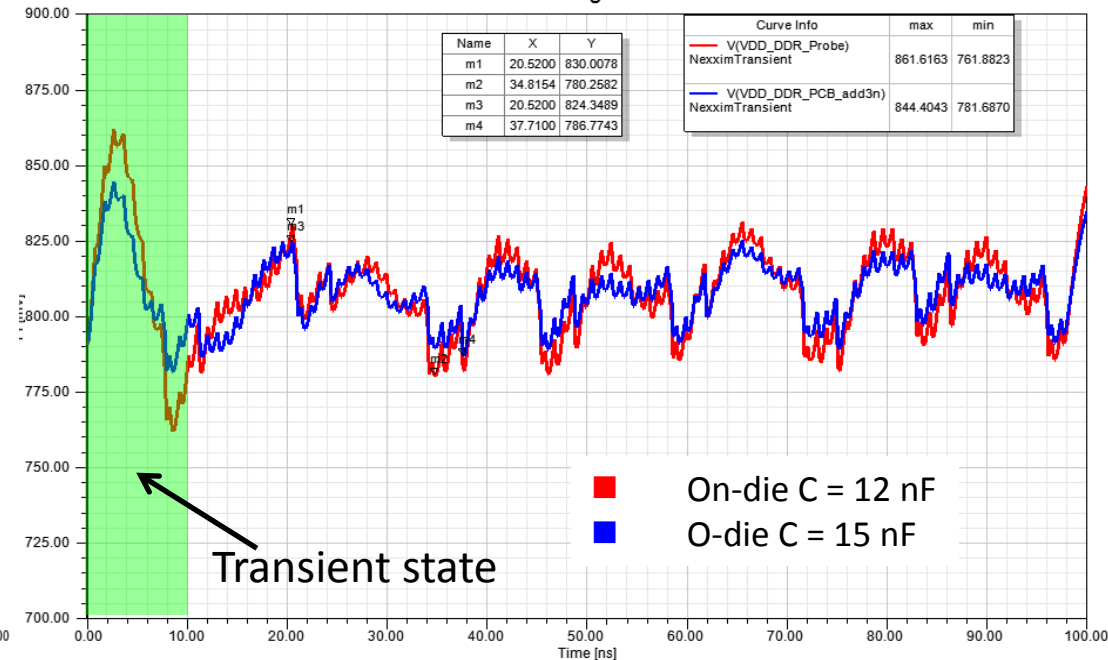
Z Parameter Plot 2

VDD_DDR



Transient Voltage Plot 6

VDD_DDR



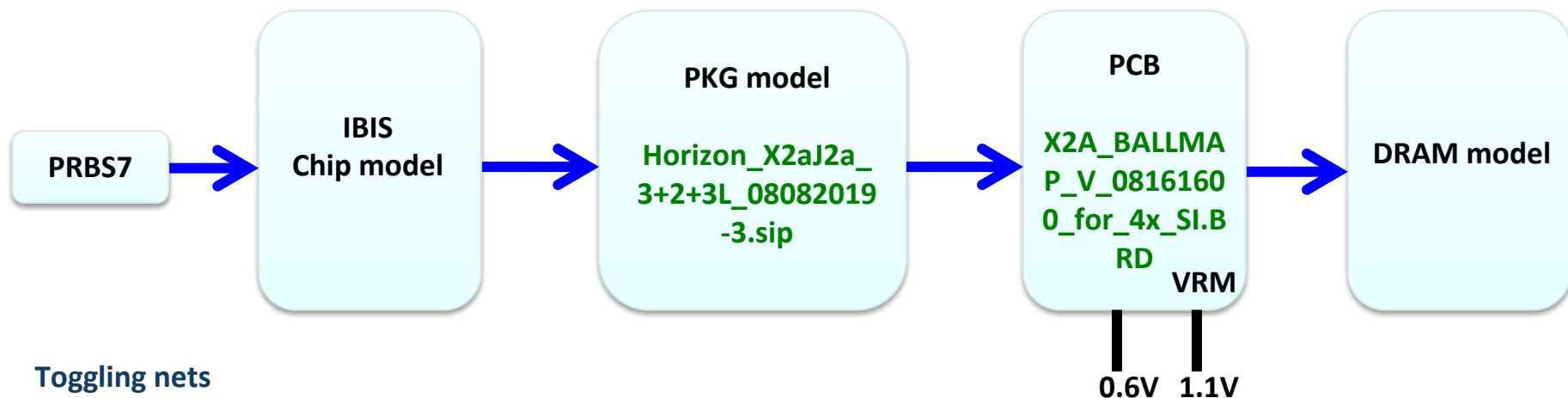
- Transient state (0 ~ 10ns):
 - On-die C => 12 nF: P2P Noise = 7.6% ~ -4.75%
 - On-die C => 15 nF: P2P Noise = 5.5% ~ -2.3%
- Steady state (10 ~ 200ns):
 - On-die C => 12 nF: P2P Noise = 3.8% ~ -2.5%
 - On-die C => 15 nF: P2P Noise = 3% ~ -1.6%

- SPEC: +/- 2% noise

LPDDR4X



Write mode Schematic



➤ Toggling nets

- Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A
- Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A
- Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B
- Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B
- CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A
- CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B

➤ Chip model : dwc_ddrphy_txrxdq_ns_clipped_lpd4x.ibs, dwc_ddrphy_txrxqs_ns_clipped_lpd4x.ibs, dwc_ddrphy_txrxca_ns_clipped_lpd4x.ibs

- DQ : mal4drv27_dl4x_40
- DQS: mal4drv27_dl4x_40
- CA: mal4drv27_dl4x_40
- CLK: mal4drv27_dl4x_40

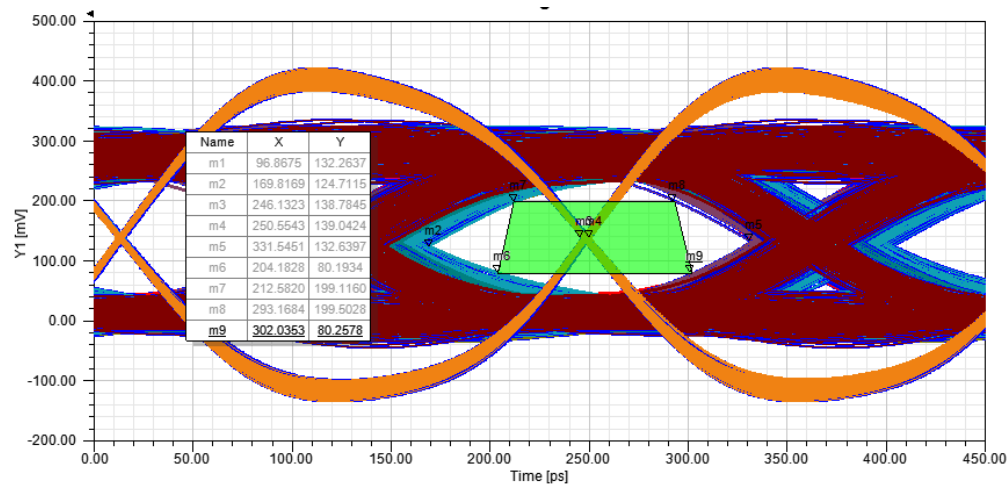
➤ On-die decap : 1nF & 24mohm, 3.6nF & 4.4mohm

➤ DRAM model : z11m_0p6v_at.ibs

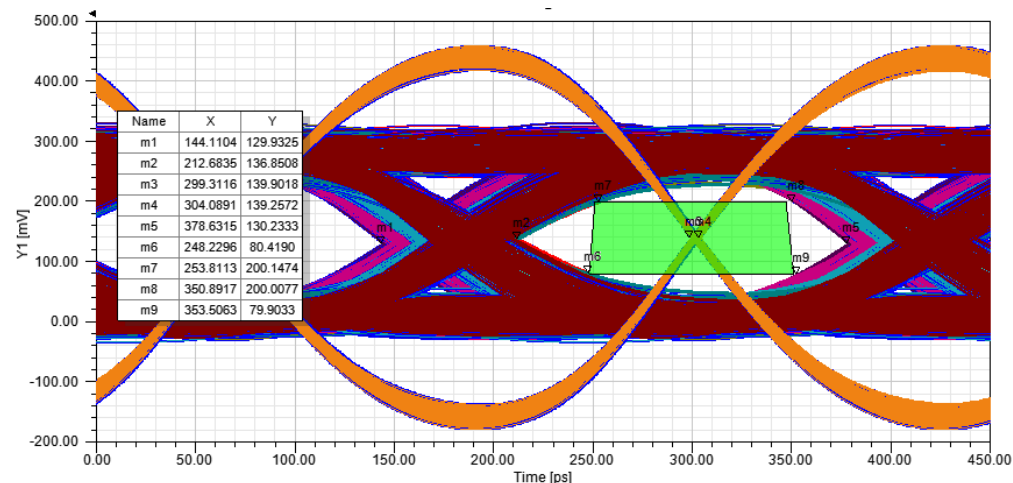
- | | |
|---------------------------|------------------------------|
| ➤ DQ_IN_ODT40_VOH60_4266 | ➤ CA_INPUT_ODT40_VOH60_4266 |
| ➤ DQS_IN_ODT40_VOH60_4266 | ➤ CLK_INPUT_ODT40_VOH60_4266 |

DQ Write Mode

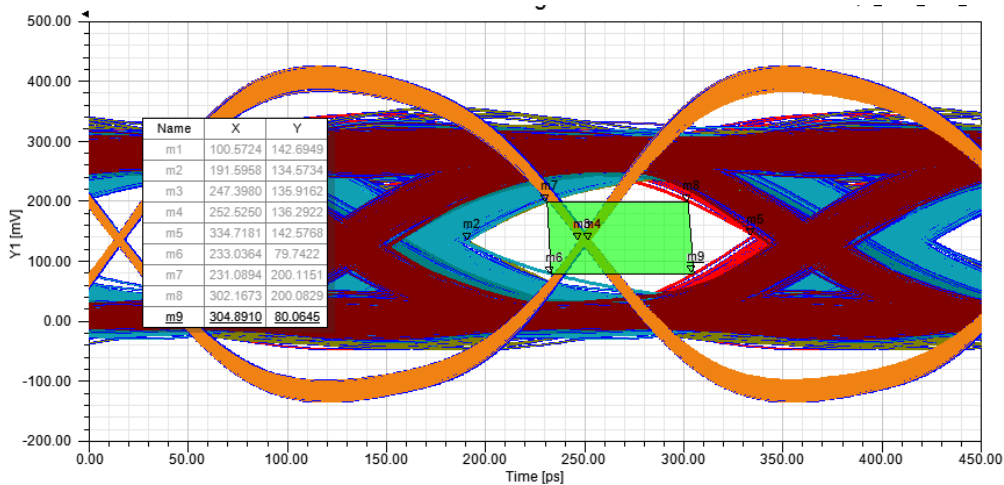
Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)



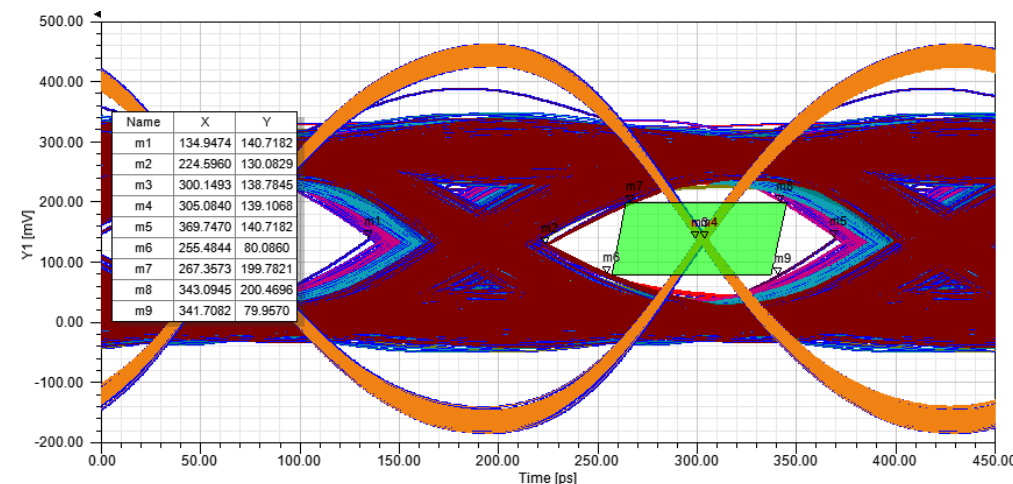
DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A



DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A



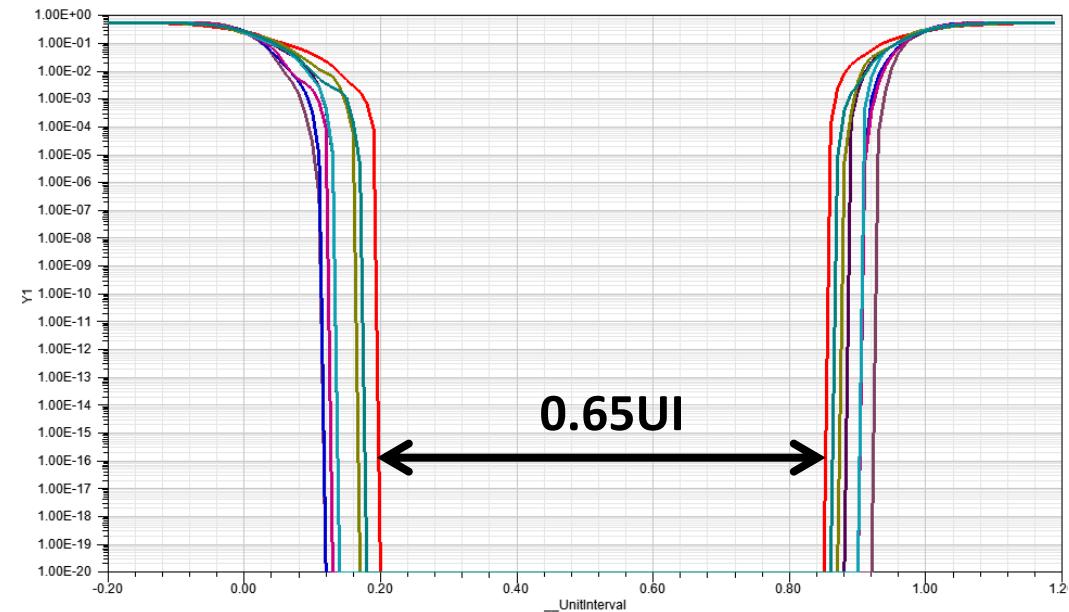
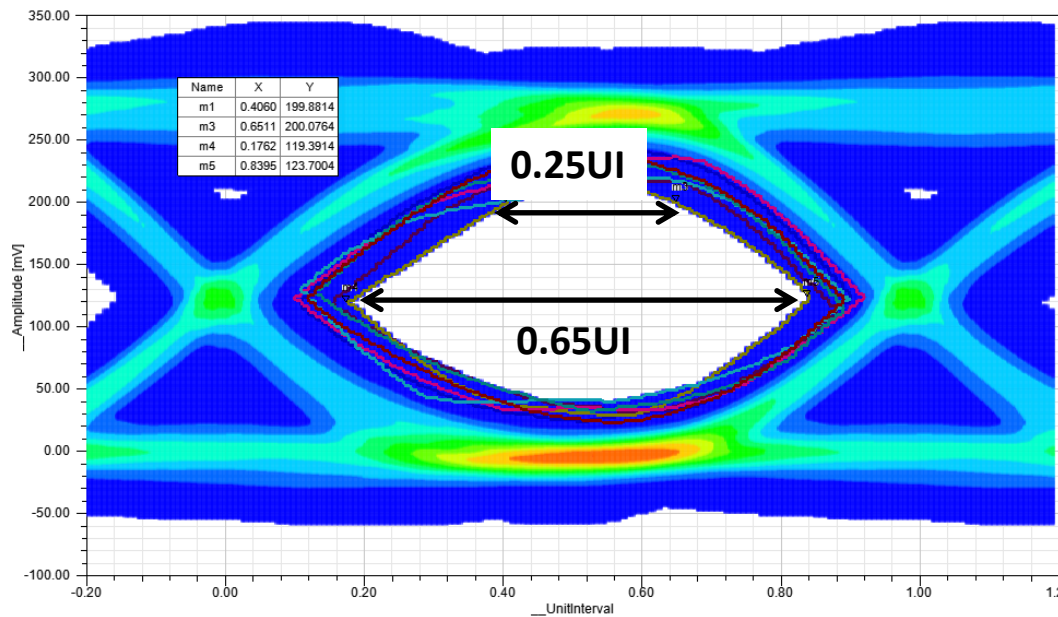
DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B



DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

DQ Write Mode - Byte3 (stat.)

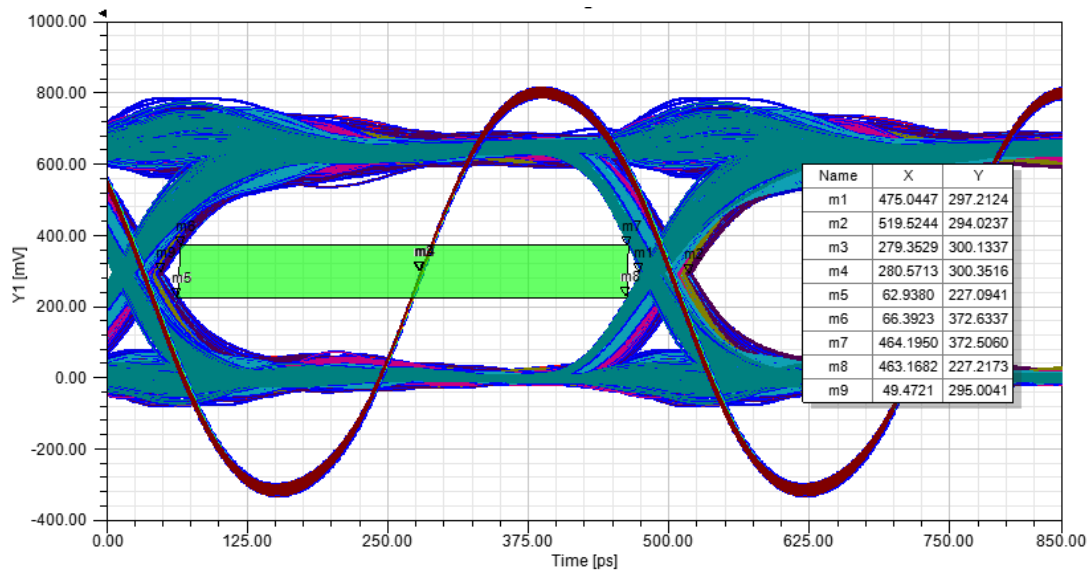
Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)



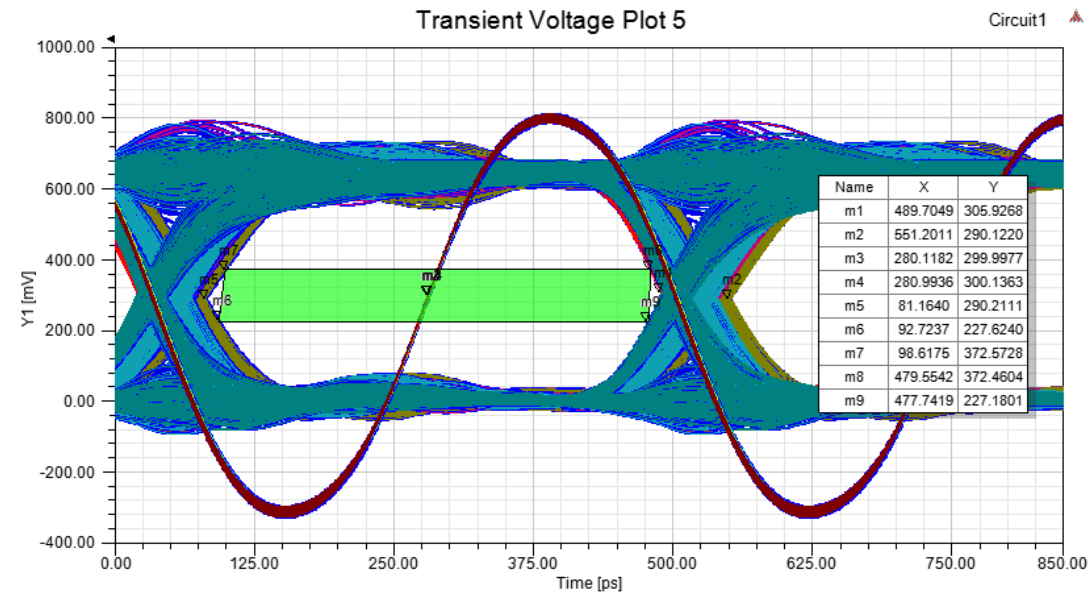
DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B

CA Write Mode

Vac & Vdc: 0.3 +/- 0.0725V (372.5mv & 227.5mv)



CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A



CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B

Write Mode Simulation Result

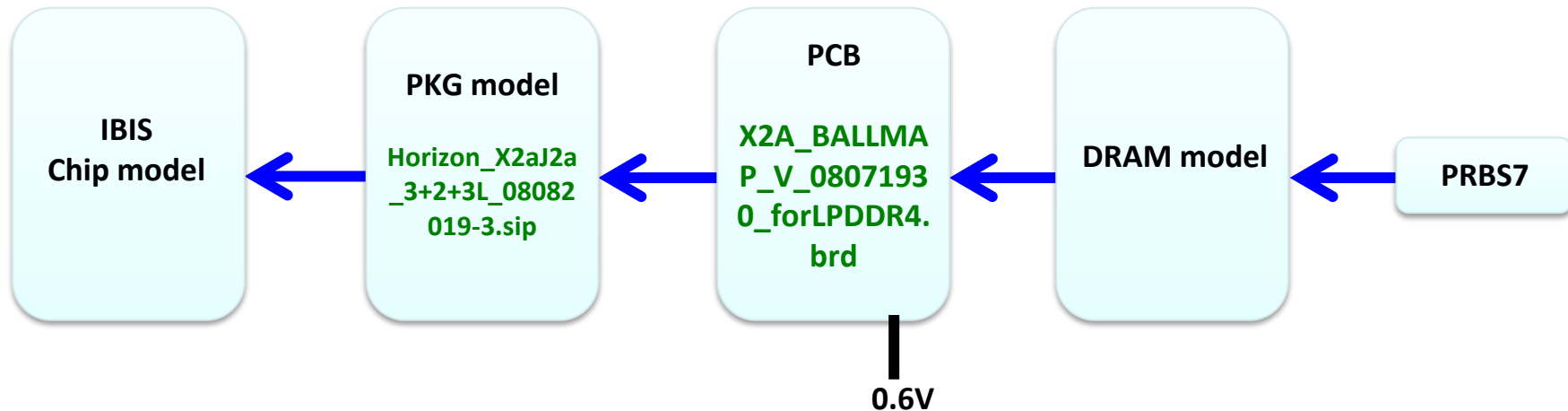
DQ Write Mode

Items	Byte 1	Byte 2	Byte 3	Byte 3 (stat.)	Byte 4	SPEC
DQ Skew+Jitter (ps)	72	68	91	-	90	-
DQS Jitter (ps)	5	5	5	-	4	-
TdIPW_total (UI)	0.69	0.71	0.61	0.65	0.62	0.45
TdIVW_total (UI)	0.35	0.41	0.29	0.25	0.32	0.25

CA Write Mode

Items	CA_1	CA_2	SPEC
CA Skew+Jitter (ps)	45	61	-
CLK Jitter (ps)	1	1	-
TcIPW_total (UI)	0.91	0.87	0.6
TcIVW_total (UI)	0.85	0.82	0.3

Read mode Schematic



➤ **Toggling nets**

- **Byte 1:** DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A
- **Byte 2:** DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A
- **Byte 3:** DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B
- **Byte 4:** DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

➤ **Chip model : dwc_ddsphy_txrdq_ns_clipped_lpd4x.ibs, dwc_ddsphy_txrdqs_ns_clipped_lpd4x.ibs**

- **DQ :** mal4drv27_dl4x_odt40
- **DQS:** mal4drv27_dl4x_odt40

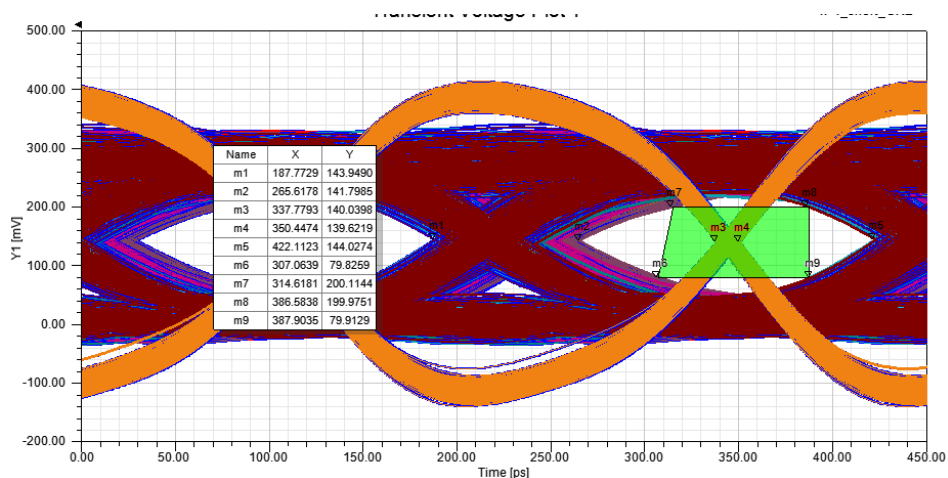
➤ **On-die decap : 1nF & 24mohm**

➤ **DRAM model : z11m_0p6v_at.ibs**

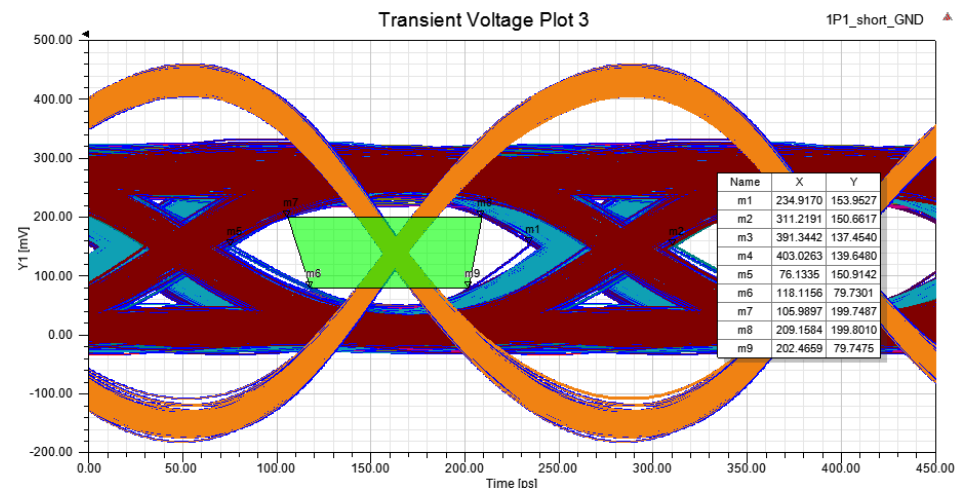
- **DQ_PD40_ODTDIS_VOH60_4266**
- **DQS_PD40_ODTDIS_VOH60_4266**

DQ Read Mode

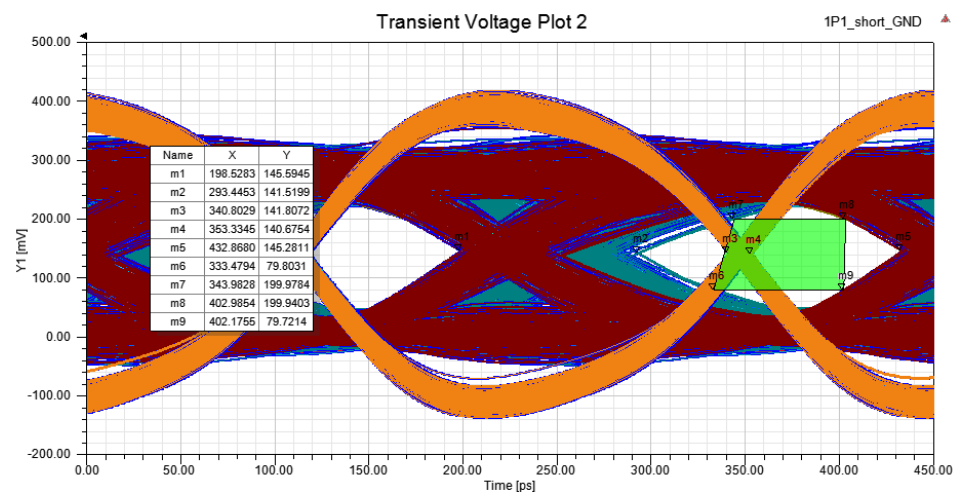
Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)



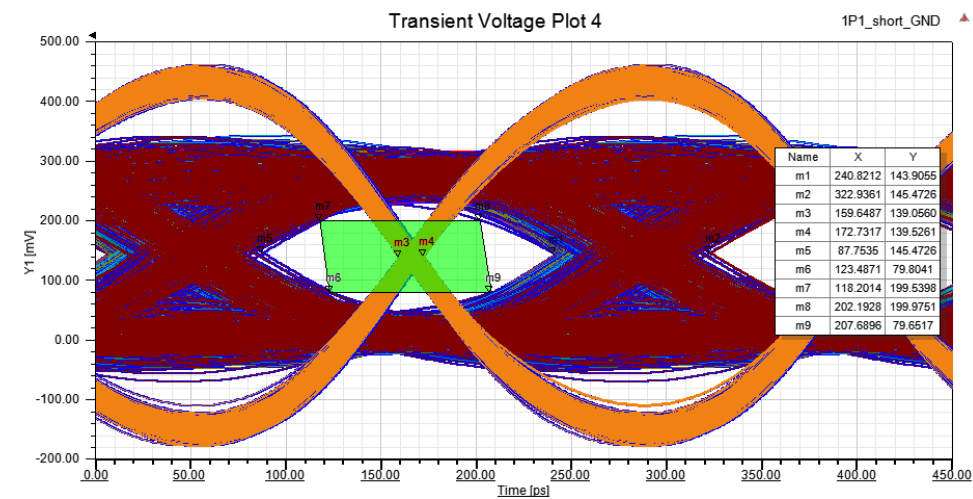
DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A



DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A



DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B



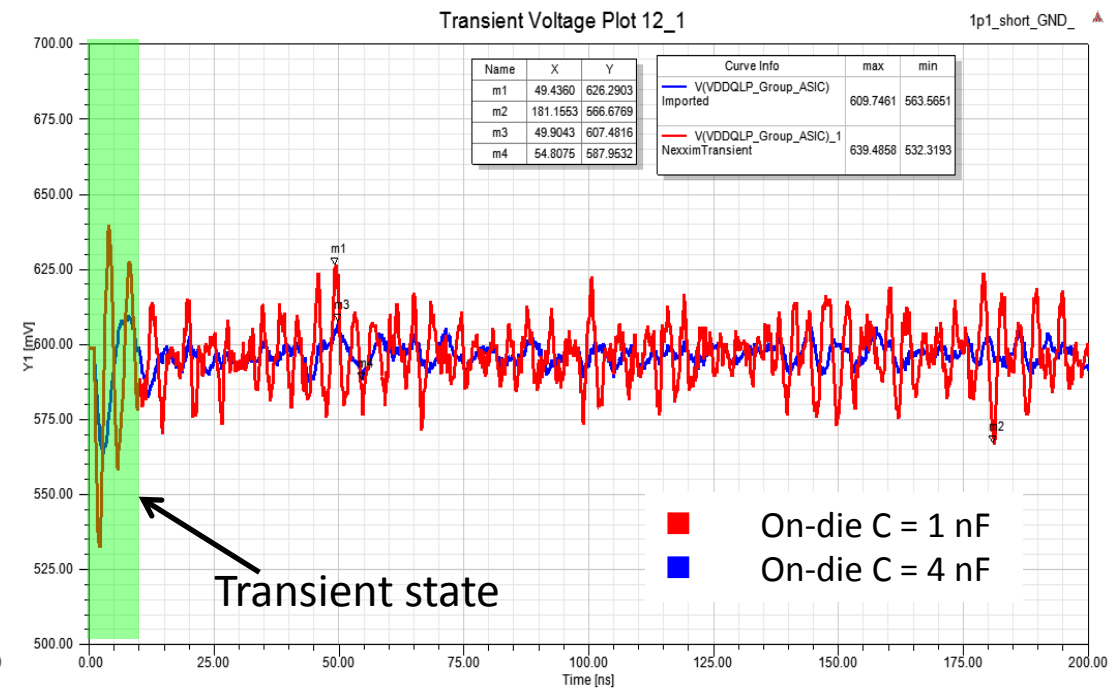
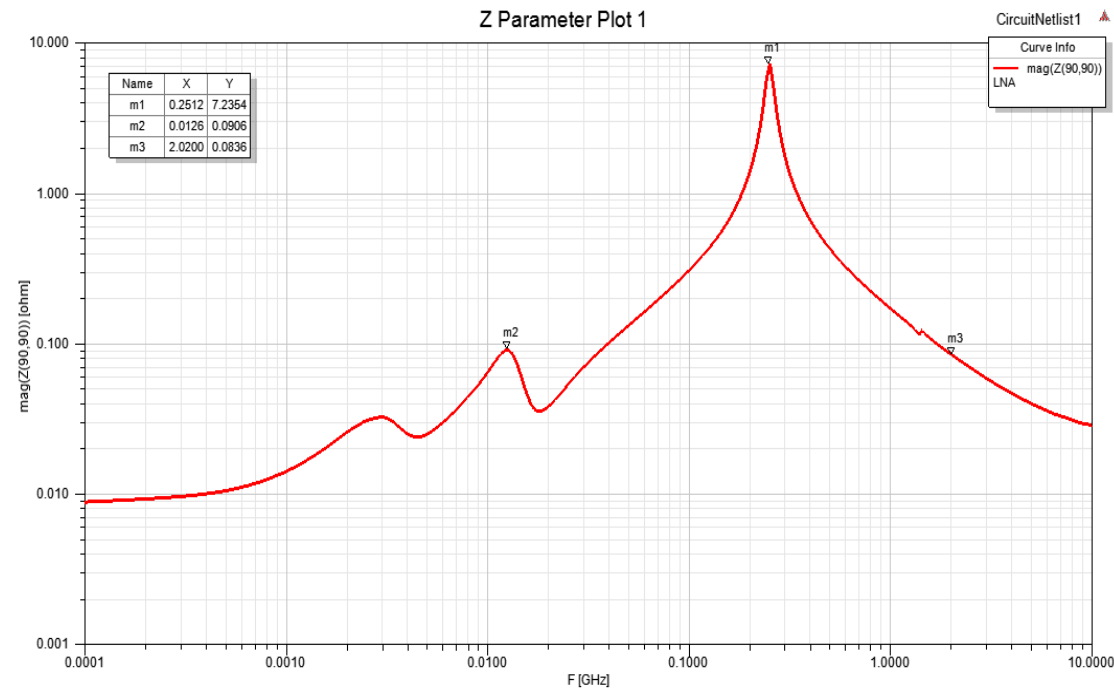
DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

Read Mode Simulation Result

DQ Read Mode

Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	78	76	94	82	-
DQS Jitter (ps)	12	12	12	12	-
TdIPW_total (UI)	0.67	0.68	0.6	0.65	0.45
TdIVW_total (UI)	0.31	0.36	0.25	0.34	0.25

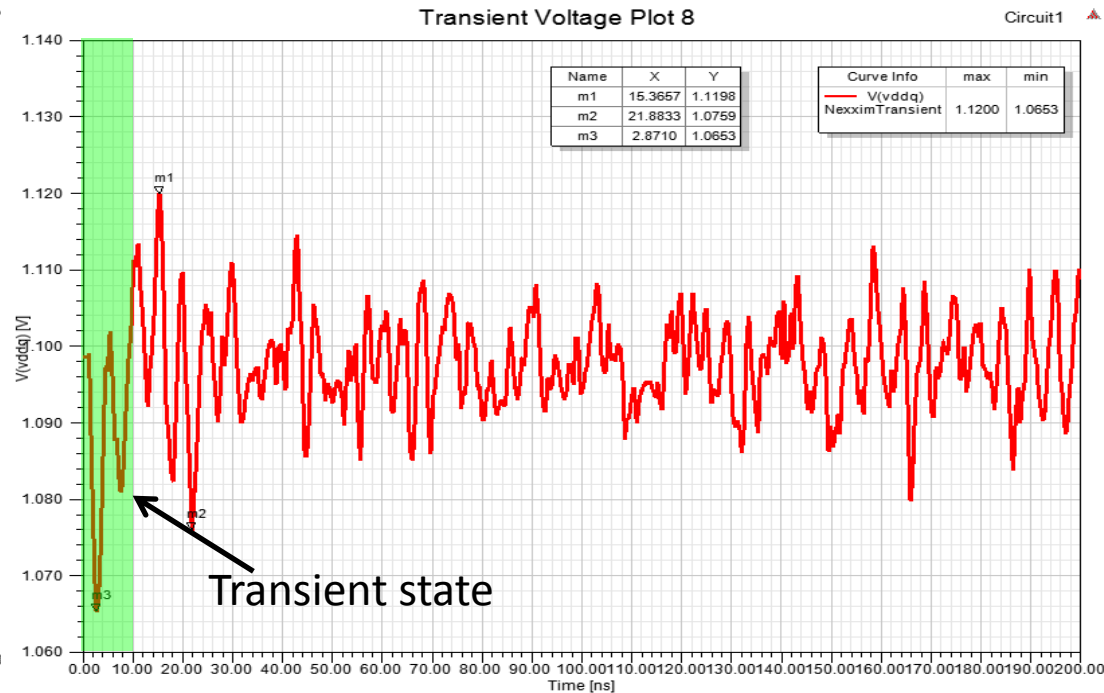
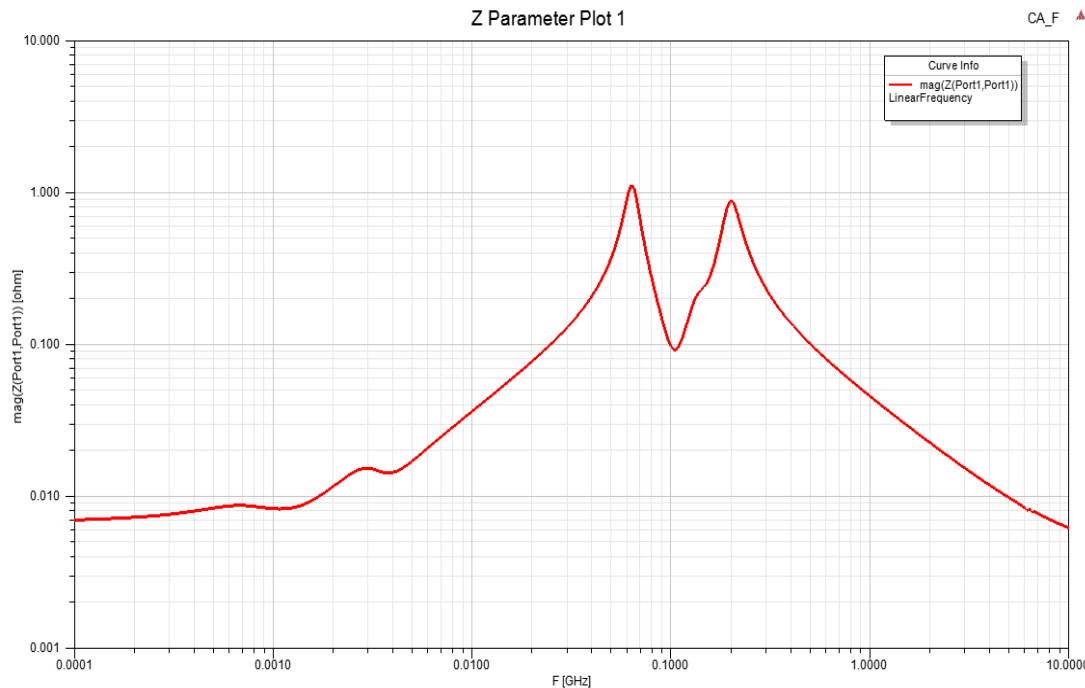
VDDQLP



- Transient state (0 ~ 10ns):
 - On-die C => 1 nF: P2P Noise = 6.5% ~ -11.3%
 - On-die C => 4 nF: P2P Noise = 1.6% ~ -6%
- Steady state (10 ~ 200ns):
 - On-die C => 1 nF: P2P Noise = 4.3% ~ -4.7%
 - On-die C => 4 nF: P2P Noise = 1.1% ~ -2%

- SPEC: +/- 2.5% noise

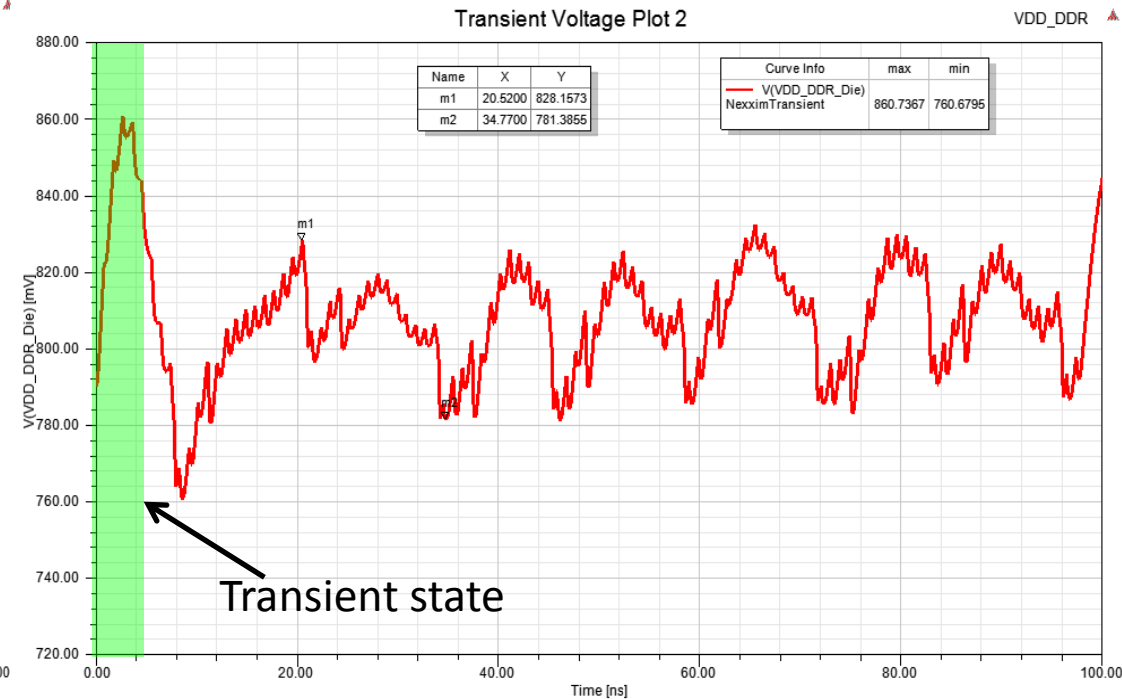
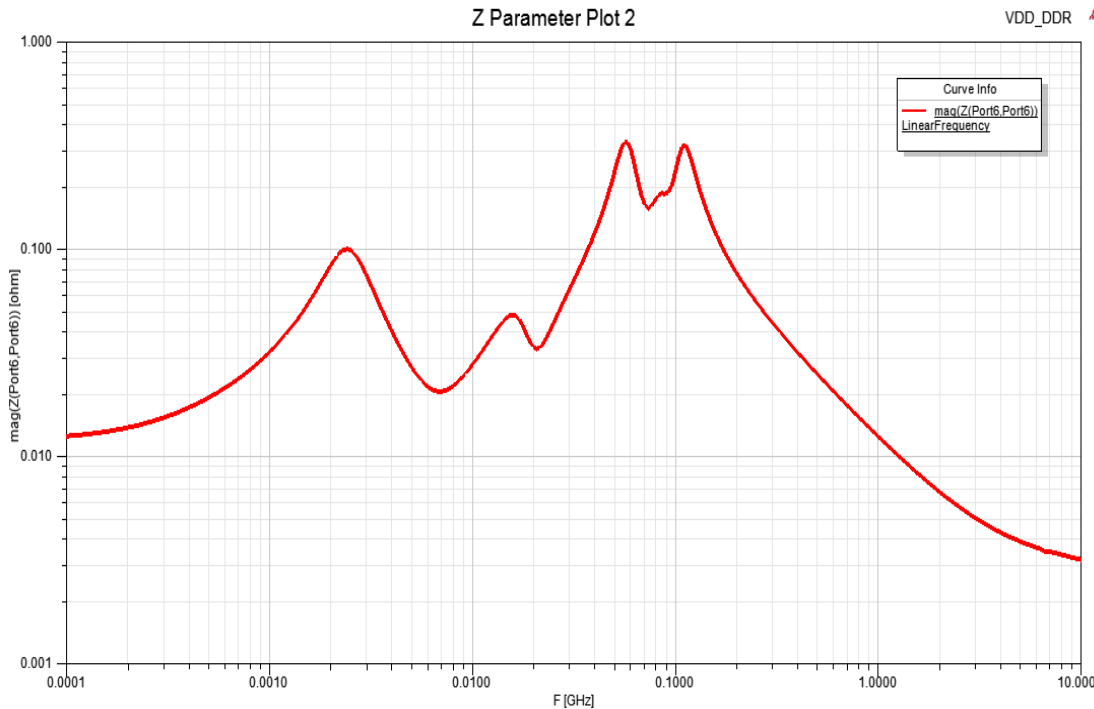
VDDQ_DDR



- Transient state (0 ~ 10ns):
 - On-die C => 3.6 nF: P2P Noise = 1.3% ~ -3.2%
- Steady state (10 ~ 200ns):
 - On-die C => 3.6 nF: P2P Noise = 1.8% ~ -2.2%

- SPEC: +/- 2.5% noise

VDD_DDR



- Transient state (0 ~ 10ns):
 - On-die C => 12nF: P2P Noise = 7.6% ~ -4.9%
- Steady state (10 ~ 200ns):
 - On-die C => 12 nF: P2P Noise = 3.5% ~ -2.4%

- SPEC: +/- 2% noise

Suggestion

- PCB routed skew limits:
 - ✓ Length control for each byte: 2mm

Thank You

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