Application Report
SPRAC36A–April 2016–Revised June 2017

EMIF Tools

ABSTRACT

At the center of every application is the need for memory. With limited on-chip processor memory, external memory serves as a solution for large software systems and data storage, and an unstable external memory interface can result in system failures or hinder software development. To prevent potential system level anomalies and ensure robust systems, hardware must be configured correctly and tested thoroughly.

The EMIF Tools application focuses on post layout activities, including configuring the Texas Instruments' processors for accessing external double data rate (DDR) memories and optimizing delay locked loop (DLL) ratios to compensate for skew. This application report provides a detailed description on how to use the associated application files. The document overview provides a complete list of processors and memory types supported by the EMIF Tools application.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/sprac36.

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1 Overview

This document provides detailed steps outlining the procedure to initialize Texas Instruments' processors to access external DDR memories using the accompanying tools included in the EMIF Tools application.

1.1 Supported Features of EMIF Tools

The EMIF Tools application supports the following features:

- TI SOCs: AM57x, DRA7x, TDA2x, TDA3x
- DDR Types: DDR2, DDR3, DDR3L, LPDDR2
- Basic EMIF configuration topics including:
  - Initializing the EMIF and DDR for basic read/write functionality
  - Compensating for signal skew
  - Enabling the error correction code (ECC) feature of the EMIF interface

The source code included in the EMIF Tools application is supported by the CPU targets listed in Table 1.

Table 1. Supported CPU Targets

CPU	TI SoC
Cortex-A15	AM57x, DRA7x, TDA2x
Cortex-M4	TDA3x

2 EMIF Configuration

The following section describes how to use the supporting application files to configure the EMIF controller for DDR memory accesses.

2.1 Preliminary Requirements

Before using the supporting application files, ensure that you have access to the following system application information:

- The data sheet of the selected DDR memory
- PCB trace lengths of the DDR clock and strobe signals (required when not utilizing the hardware leveling features of the TI Soc and DDR memory)

2.2 Generating EMIF Register Values

To assist you in defining the EMIF configuration register values, the EMIF Tools application provides an EMIF register configuration workbook. The workbook is divided into six worksheets, and requires specific information pertaining to the system application environment. The first worksheet should be reviewed; it will allow you to save and load custom configurations. The next three worksheets require your input; their tabs are red. The fifth worksheet provides calculated register values that should be used to configure the EMIF controller; its tab is green. The last worksheet also provides register values, but in GEL format.

Table 2. EMIF Register Configuration Worksheets

Worksheet	Description
Title-README	Informative; load/save custom configurations
Step1-SystemDetails	User input: system information
Step2-BoardDetails	User input: trace lengths of clock / strobe
Step3-DDRTimings	User input: timing requirements from DDR datasheet
Register Values (U-Boot)	Output: register values (u-boot format)
Register Values (GEL)	Output: register values (GEL format)

The following sections outline the procedure to complete the various required input parameters of the EMIF configuration workbook.

2.2.1 Step1 – System Details

The first worksheet requires you to input both high level system application details, as well as specific I/O settings for the DDR pins of the TI application processor and DDR memory.

Step 1A seeks system level details and is shown in Table 3 with populated example values.

Table 3. System Details

Detail	Description	Value	Units
1	Company / Board Name / Revision (Ex: TI_EVM_revC)	TI_EVM_revG3	-
2	TI Soc Part Number	DRA75x	-
3	SYS_CLK1 Frequency	20	MHz
4	Required EMIF Interfaces	2	-
5	DDR Memory Type	DDR3/L	-
6	DDR Memory Frequency	532	MHz
7	DDR Data Bus Width Per EMIF	32	Bits
8	Required Chip Select Lines	1	-
9	Leveling Technique: "S/W" or "H/W"	H/W	-
10	Max DRAM Operating Temperature	<=85	°C
11	Enable ECC (May not apply to all EMIFs)	Yes	-
12	ECC Region 1: System Start Address	80000000	Enabled
13	ECC Region 1: System End Address	8FFFFFFF	Enabled
14	ECC Region 2: System Start Address	90000000	Disabled
15	ECC Region 2: System End Address	90000000	Disabled

The table parameters are defined in detail in the bulleted list below:

- Detail 1 – Company/Board Name/Revision: This value is used as a unique identifier to name the structures of register values in the “Register Values” worksheet. Valid characters include: ‘a’-‘z’, ‘A’-‘Z’, ‘0’-‘9’, and ‘_’.
- Detail 2 – TI Soc Part Number: This value should be selected to match the TI application processor part number utilized in the system application. Pre-defined values of supported processors are provided in a drop-down menu list.
- Detail 3 – SYS_CLK1 Frequency: This value is used to determine the DDR PLL register settings. Pre-defined values of supported SYS_CLK1 frequencies are provided in a drop-down menu list.
- Detail 4 – Required EMIF Interfaces: This value should be selected based on the desired number of EMIF interfaces to configure. Pre-defined values are provided in a drop-down menu list.
- Detail 5 – DDR Memory Type: This value should be selected based on the DDR memory type connected to the TI processor. Pre-defined values are provided in a drop-down menu list based on the supported memory types.
- Detail 6 – DDR Memory Frequency: This value should be selected for the desired DDR clock frequency.
- Detail 7 – DDR Data Bus Width per EMIF: This value should be selected based on the bus width between the TI processor and the DDR memory. This value represents the bus width per EMIF channel. Pre-defined values are provided in a drop-down menu list.
- Detail 8 – Required Chip Select Lines: This value should be set to match the number of chip select lines utilized per EMIF channel in the system application. Pre-defined values are provided in a drop-down menu list.
- Detail 9 – Leveling Technique: This value should be set for the preferred leveling technique.

- Detail 10, Max DRAM Operating Temperature: This value should be set to match the maximum operating temperature that the DRAM will be subjected to in the end application environment. Pre-defined values are provided in a drop-down menu list.
- Detail 11 – Enable ECC: Setting this parameter to “Yes” enables the ECC functionality of the EMIF controller (may not apply to all EMIFs on a device). A physical DDR memory should be connected to the ECC pins of the application processor.
- Detail 12, ECC Region 1 System Start Address: This value should be set to a hexadecimal value between “80000000” and “FFFFFFFF”. Note that only numerical characters and letters ‘a'-'f’ are valid.
- Detail 13, ECC Region 1 System End Address: This value should be set to a hexadecimal value between the ECC region 1 system start address and “FFFFFFFF”. Note that only numerical characters and letters ‘a'-'f’ are valid. Setting this value less than or equal to the ECC region 1 system start address will disable the region.
- Detail 14, ECC Region 2 System Start Address: This value should be set to a hexadecimal value between “80000000” and “FFFFFFFF”, and outside of the ECC region 1 address range. Note that only numerical characters and letters ‘a'-'f’ are valid.
- Detail 15, ECC Region 2 System End Address: This value should be set to a hexadecimal value between the ECC region 2 system start address and “FFFFFFFF”, and outside of the ECC region 1 address range. Note that only numerical characters and letters ‘a'-'f’ are valid. Setting this value less than or equal to the ECC region 2 system start address, or within the ECC region 1 address range, will disable the region.

Care should be taken to provide details in order throughout the workbook. As the parameter values are selected, the drop-down menu lists of other parameters may change. In some instances, a previous selected value may no longer be available. In this case, the cell location turns red. Providing the details in order should avoid the necessity to re-select a parameter value. Table 4 shows an example in which the “TI Soc Part Number” parameter has been changed compared to Table 3. In this case, the fourth parameter is flagged because the new selected TI processor does not support two EMIF channels.

Table 4. System Details: Warnings

Detail	Description	Value	Units
1	Company / Board Name / Revision (Ex: TI_EVM_revC)	TI_EVM_revG3	-
2	TI Soc Part Number	DRA72x	-
3	SYS_CLK1 Frequency	20	MHz
4	Required EMIF Interfaces	2	-
5	DDR Memory Type	DDR3/L	-
6	DDR Memory Frequency	532	MHz
7	DDR Data Bus Width Per EMIF	32	Bits
8	Required Chip Select Lines	1	-
9	Leveling Technique: "S/W" or "H/W"	H/W	-
10	Max DRAM Operating Temperature	<=85	°C
11	Enable ECC (May not apply to all EMIFs)	Yes	-
12	ECC Region 1: System Start Address	80000000	Enabled
13	ECC Region 1: System End Address	8FFFFFFF	Enabled
14	ECC Region 2: System Start Address	90000000	Disabled
15	ECC Region 2: System End Address	90000000	Disabled

Step 1B requests specific details pertaining to the DDR memory utilized in the system application. These details are required for the workbook to determine the size and speed bin of the DDR memory. Table 5 shows an example.

Table 5. DDR Details

Detail	Description	Value	Units
16	Speed Bin: Data Rate	1066	MHz
17	Density	2	Gb
18	Width	16	Bits
19	Speed Bin: CAS Latency	7	ntCK

The table parameters are defined in detail in the bulleted list below:

- Detail 16 – Speed Bin (Data Rate): This value should be selected to match the data rate of the DDR memory connected to the TI processor.
- Detail 17 – Density: This value should be selected to match the density of a single DDR memory connected to the TI processor.
- Detail 18 – Width: This value should be selected to match the width of a single DDR memory connected to the TI processor.
- Detail 19 – Speed Bin (CAS Latency): This value should be selected to match the required CAS latency to ensure functional operation of the DDR memory at the data rate specified by the “Speed Bin: Data Rate” parameter.

Step 1C requires the user to provide the desired I/O settings for the DDR memory termination and output driver impedance. Table 6 illustrates an example configuration for DDR3.

Table 6. DDR IO Configuration (Memory Side)

Detail	Description	Value	Units
20	ODT / Rtt_Nom	RZQ/4	Ω
21	Dynamic ODT / Rtt_Wr	Disabled	Ω
22	Output Driver Impedance	RZQ/7	Ω

The table parameters are defined in detail in the bulleted list below:

- Detail 20 – ODT/Rtt_Nom: This value applies to the on-die termination of the DDR memory I/O pins. For more information, see the data sheet of the DDR memory. (1)
- Detail 21 – Dynamic ODT / Rtt_Wr: This value applies to on-die termination during DDR writes when the dynamic ODT mode is enabled. For more information, see the data sheet of the DDR memory. (1)
- Detail 22 – Output Driver Impedance: This value applies to the output driver impedance of the DDR memory I/O pins. For more information, see the see the data sheet of the DDR memory. (1)

(1) A recommendation is provided; however, board level simulations and signal integrity analysis should be performed to ensure the appropriate settings.

Step 1D allows you to modify the I/O settings for the DDR pins of the TI application processor. Table 7 illustrates the required input details.

Table 7. DDR IO Configuration (SoC Side)

Detail	Description	Value	Units
23	ODT	60	Ω
24	Slew Rate: Addr/Ctrl/Clk	Fastest: SR[2:0] = 0b000	–
25	Slew Rate: Data/Strobe	Fastest: SR[2:0] = 0b000	–
26	Output Driver Impedance: Addr/Ctrl/Clk	34	Ω
27	Output Driver Impedance: Data/Strobe	48	Ω

The table parameters are defined in detail in the bulleted list below:

- Detail 23 – ODT: This value applies to the on-die termination of the EMIF I/O pins on the Texas Instruments application processor.
- Detail 24 – Slew Rate (Addr/Ctrl/Clk): This value applies to the slew rate of the EMIF address, control, and clock I/O pins on the Texas Instruments application processor. (1)
- Detail 25 – Slew Rate (Data/Strobe): This value applies to the slew rate of the EMIF data and strobe I/O pins on the Texas Instruments application processor.
- Detail 26 – Output Driver Impedance (Addr/Ctrl/Clk): This value applies to the output driver impedance of the EMIF address, control, and clock I/O pins on the Texas Instruments application processor. (1)
- Detail 27 – Output Driver Impedance (Data/Strobe): This value applies to the output driver impedance of the EMIF data and strobe I/O pins on the Texas Instruments application processor. (1)

2.2.2 Step 2 – Board Details

The second worksheet requests you to enter the PCB trace lengths of the DDR clock and strobe signals from the TI application processor to the DDR memories for each byte lane. This information is pertinent for systems utilizing a fly-by topology to interface to DDR3/L memories. The PCB trace lengths are required to determine an approximation of the PCB flight skew of the signals, and serves as a starting point to the leveling algorithm. Full optimization is achieved from leveling.

Table 8 and Figure 1 illustrates the format for which the PCB trace lengths should be provided. Because a particular trace may be routed on more than one layer of the PCB, you should identify which portions of the trace are routed on the outer layers of the PCB and which portions are routed on the inner PCB layers between two planes.

Table 8. PCB DDR Trace Lengths

DRAMs Connected to EMIF1, Rank 0										
	PCB Trace Length in MILs (1/1000 inch)									
	Byte 0		Byte 1		Byte 2		Byte 3		Byte 4	
Signal	Microstrip	Stripline	Microstrip	Stripline	Microstrip	Stripline	Microstrip	Stripline	Microstrip	Stripline
CLK	A1	A2	B1	B2	C1	C2	D1	D2	E1	E2
DQSn	F1	F2	G1	G2	H1	H2	I1	I2	J1	J2

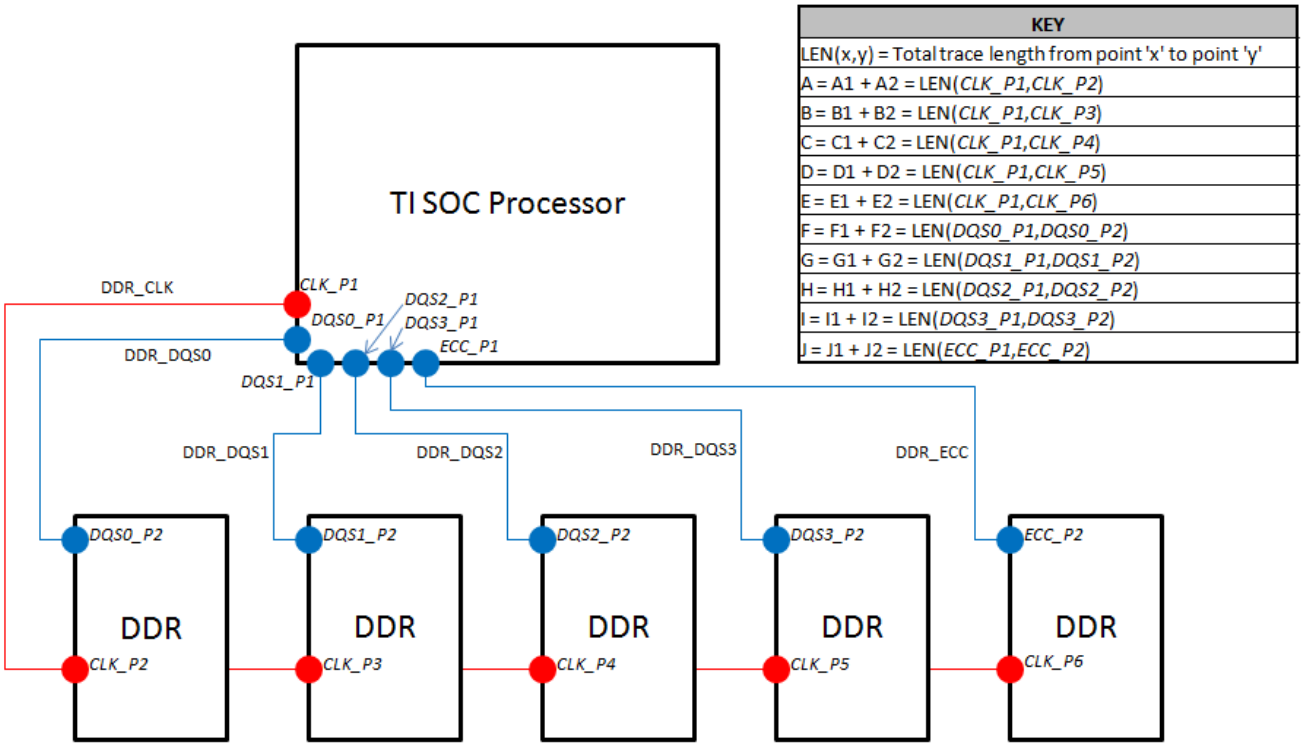

Figure 1. PCB DDR Trace Lengths

2.2.3 Step 3 – DDR Timings

The third worksheet requires you to input DDR timing values that can be found in the DDR memory data sheet. Figure 2 portrays the timing values required and is populated assuming a DDR3-1066F (2GB density, 2KB page size) memory operating at 532 MHz.

Parameter	Description	Datasheet Values		Final Bit Field Values		JEDEC Bit Field Values
		tCK	ns	Value	Units	(DDR3/L-1066 @ 532 MHz)
CAS Latency	Delay between internal READ command and data ready	7		7	tCK	7
CWL Latency	Delay between internal WRITE command and data ready	6		6	tCK	6
tRP	Precharge command period		13.125	6	tCK	6
tRCD	Active to read or write delay		13.125	6	tCK	6
tWR	Write recovery time		15	7	tCK	7
tRAS	Active to Precharge command period		37.5	19	tCK	19
tRC	Active to Active/Refresh command period		50.625	26	tCK	26
tRRD	Active Bank to Active Bank command period	4	10	6	tCK	6
tWTR	Internal Write to Read command delay	4	7.5	3	tCK	3
tXP	Exit power down mode to first valid command	3	7.5	3	tCK	3
tXSNR/tXS	Exit self refresh to commands not requiring a locked DLL	5	170	90	tCK	90
tXSRD/tXSDLL	Exit self refresh to commands requiring a locked DLL	512		511	tCK	511
tRTP	Internal Read to Precharge command delay	4	7.5	3	tCK	3
tCKE	CKE minimum pulse width	3	5.625	2	tCK	2
tCKESR	Minimum CKE low width for Self Refresh entry to exit	4		3	tCK	3
tZQCS	ZQ short calibration time	64		63	tCK	63
tRFC	Refresh to Active/Refresh command period		160	85	tCK	85
tRAS (max)	Active to Precharge command period (Max Value)		70200	8	tREFI intervals	8
tREFI	Average periodic refresh interval		7800	4149	tCK	4149
tFAW	Minimum Window for 4 Active Bank commands		50	See tRRD	-	6

Figure 2. DDR Timings

The following list describes the different columns in Figure 2:

- Parameter: The timing parameter name found in the DDR data sheet. All listed parameters require minimum timing values, except tRAS(max) and tREFI.
- Description: A description of the DDR timing parameter.
- Data Sheet Values: The corresponding DDR timing value found in the DDR data sheet. This value can either be defined in units tCK, ns, or the maximum of either a tCK or ns value. As illustrated in Figure 2, the worksheet calculates the bit field value based off of the maximum of either the tCK or ns value.
- Final Bit Field Value: The final bit field value programmed to the EMIF register. This value is typically in units of clock cycles.
- JEDEC Bit Field Values: This column's intended purpose is for reference only and is dynamically updated based off of the user's input from Section 2.2.1.

The workbook attempts to warn you if an input timing value is tighter than expected (based off of the JEDEC values populated for the memory device detailed in Section 2.2.1). In Figure 3, the timing parameters tWR and tREFI have been changed from that shown in Figure 2. However, a typical minimum write recovery time and average refresh interval for a DDR3 memory is 15 ns and 7.8 µs, respectively. The timing parameter tWR is flagged because the new tWR user input of 10 ns is less than a typical minimum value of 15 ns. In this case, the memory row may be pre-charged too early. The timing parameter tREFI is flagged because the new tREFI user input of 8 µs is larger than a typical average value of 7.8 µs. In this case, the memory may not be refreshed as often as necessary.

Parameter	Description	Datasheet Values tCK	Datasheet Values ns	Final Bit Field Values Value	Final Bit Field Values Units	JEDEC Bit Field Values (DDR3/L-1066 @ 532 MHz)
CAS Latency	Delay between internal READ command and data ready	7		7	tCK	7
CWL Latency	Delay between internal WRITE command and data ready	6		6	tCK	6
tRP	Precharge command period		13.125	6	tCK	6
tRCD	Active to read or write delay		13.125	6	tCK	6
tWR	Write recovery time		10	5	tCK	7
tRAS	Active to Precharge command period		37.5	19	tCK	19
tRC	Active to Active/Refresh command period		50.625	26	tCK	26
tRRD	Active Bank to Active Bank command period	4	10	6	tCK	6
tWTR	Internal Write to Read command delay	4	7.5	3	tCK	3
tXP	Exit power down mode to first valid command	3	7.5	3	tCK	3
tXSNR/tXS	Exit self refresh to commands not requiring a locked DLL	5	170	90	tCK	90
tXSRD/tXSDLL	Exit self refresh to commands requiring a locked DLL	512		511	tCK	511
tRTP	Internal Read to Precharge command delay	4	7.5	3	tCK	3
tCKE	CKE minimum pulse width	3	5.625	2	tCK	2
tCKESR	Minimum CKE low width for Self Refresh entry to exit	4		3	tCK	3
tZQCS	ZQ short calibration time	64		63	tCK	63
tRFC	Refresh to Active/Refresh command period		160	85	tCK	85
tRAS (max)	Active to Precharge command period (Max Value)		70200	7	tREFI intervals	8
tREFI	Average periodic refresh interval		8000	4256	tCK	4149
tFAW	Minimum Window for 4 Active Bank commands		50	See tRRD	-	6

Figure 3. DDR Timings (Warning)

Although the warnings may serve as a quick sanity check in the event that a timing parameter is accidentally input incorrectly, you should ultimately ensure the final bit field values comply with the timing values specified in their DDR data sheet.

2.2.4 Results – Register Values

After the system level, board level, and DDR timing details have been populated in their corresponding worksheets, you can access the fifth worksheet, “Register Values”, to obtain the calculated register settings based on the your input. The register values are output in u-boot format to allow for easy integration into a Linux environment. These values can also be utilized with the accompanying source files included in the EMIF Tools application.

In addition, a “Register Values (GEL)” worksheet is provided in the event that you wish to integrate the EMIF configuration values into a custom GEL file.

Note that the register values (GEL) and register values (u-boot) are output for a single EMIF channel in the results section. If utilizing multiple EMIF channels with the same DDR memory width and type, the same settings should be applied to the other EMIF channel.

In a scenario where multiple EMIF channels are used with different DDR memory widths and type - it is required to configure the tool per each EMIF channel to obtain the corresponding register settings.

2.2.5 Results – Saving/Loading Custom Configurations

As an additional feature of the Register Configuration workbook, you can save and load multiple custom configurations without having to create duplicate copies of the workbook.

From the 'README' worksheet, you can find a drop down box with existing configurations, as well as options to save or load a user configuration. This is illustrated in Figure 4.

Figure 4. User Defined Configurations

To save a custom user configuration, only click the 'Save User Config' push button. The configuration name is automatically generated based on your input, and is a combination of details 1, 2, 5, and 6 from worksheet discussed in Section 2.2.1. Invalid configurations may not successfully save, so it is important that you ensure that each worksheet requiring user input has been properly configured.

After the configuration has been successfully saved, the configuration name will appear from the drop down box, illustrated in Figure 5. Each time a unique configuration is saved, the EMIF Tools source code is automatically updated.

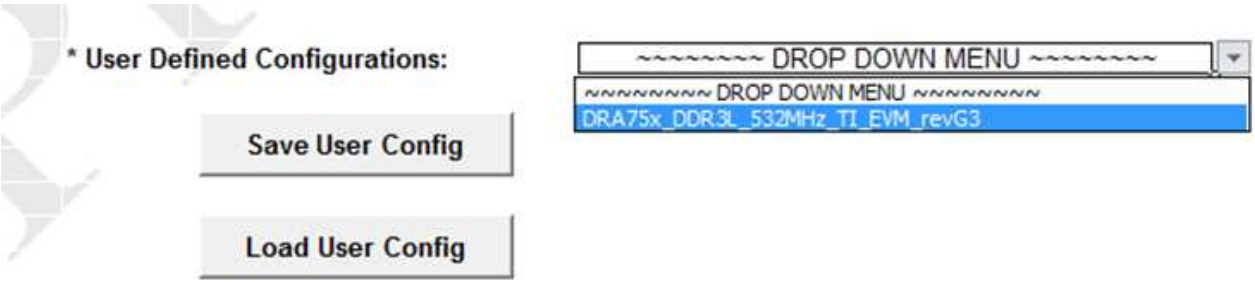

Figure 5. Saved User Configuration

NOTE: In addition to saving custom user configurations, you should also save the workbook!

If you create multiple configurations and later wish to recall the input from a previous saved configuration, you can select the configuration name from the drop down box and click the 'Load User Config' push button. This feature will only load your previous input to the Register Configuration workbook at the time in which the configuration was saved, and will NOT illustrate any changes that may have been made to the software manually.

3 References

DDR3 SDRAM Standard, JESD79-3F, 2012

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision **Page**

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