General LPDDR5/LPDDR5X Specifications 1

Mode Registers

Introduction

The three Micron general LPDDR5/LPDDR5X specifications listed below define minimum requirements for x16 or x8, single-channel, LPDDR5/LPDDR5X devices. They include general features, functionality, mode registers, AC and DC characteristics, and other device information.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

LPDDR5 and LPDDR5X devices support data rates per pin up to 6400 Mb/s and beyond 6400 Mb/s, respectively.

For specific device features, specifications, or details, refer to the product data sheets.

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Mode Register Assignments and Definitions

In the access column of the Mode Register Assignments table below, R indicates read-only, W indicates write-only, R/W indicates read-capable, write-capable, or enabled. The MODE REGISTER READ command (MRR) is used to read from a register, and the MODE REGISTER WRITE command (MRW) is used to write to a register.

Table 1: Mode Register Assignments

Notes apply to entire table

MR#	MA[6:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	R	RFU	Pre Emphasis	Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always on mode	Latency mode	NT ODT timing mode
1	01h	R/W	WL				CK mode	RFU		
2	02h	W	*n*WR				RL, *n*RBTP			
3	03h	R/W	DBI-WR	DBI-RD	WLS	BK/BG ORG		PDDS		
4	04h	R	TUF	ZQ master	ZQUF	Refresh multiplier				
5	05h	R	Manufacturer ID							
6	06h	R	Revision ID1							
7	07h	R	Revision ID2							
8	08h	R	I/O width		Density				Type	
9	09h	W	Vendor-specific test mode							
10	0Ah	W	RPST length		RDQS PRE		WCK PST		RFU	RPST mode
11	0Bh	R/W	RFU	CA ODT			NT-ODT enable	DQ ODT		
12	0Ch	R/W	VBS	$V_{REF(CA)}$						
13	0Dh	W	Dual V_{DD2}	CBT mode	DMD	DMI I/O control	RFU	VRO	Thermal offset	
14	0Eh	R/W	VDLC	V_{REF} (DQ[7:0])						
15	0Fh	R/W	RFU	V_{REF} (DQ[15:8])						
16	10h	R/W	CBT-phase	VRCG	CBT		FSP-OP		FSP-WR	
17	11h	R/W	x8ODTD upper	x8ODTD lower	ODTD -CA	ODTD -CS	ODTD -CK	SOC ODT		
18	12h	W	CKR	WCK2CK leveling	RFU	WCK ON	WCK FM	WCK ODT		
19	13h	W	RFU		WCK2DQ OSC FM support	WCK2DQ OSC FM	DVFSQ		DVFSC	
20	14h	W	RDC DQ mode	RDC DMI mode	MRWDU	MRWDL	WCK mode		RDQS	

Table 1: Mode Register Assignments (Continued)

Notes apply to entire table

MR#	MA[6:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
21	15h	R/W	WXS	WXFE	RDCFE	WDCFE	ODTD -CSFS	WXFS	RDCFS	WDCFS
22	16h	W	RECC		WECC		RFU			
23	17h	W	PASR segment mask							
24	18h	R/W	DFES	DFEQU			RFU	DFEQL		
25	19h	W	Optimized refresh mode	PARC	CA BUS TERM	CK BUS TERM	RFU			
26	1Ah	R/W	RDQSTFE	RDQSTFS	DCMU1	DCMU0	DCML1	DCML0	DCM Flip	DCM Start/ Stop
27	1Bh	R	RAAMULT		RAAIMT					RFM
28	1Ch	W	RFU		ZQ mode	RFU	ZQ Interval		ZQ Stop	ZQ Reset
29	1Dh	R	PPR resources							
30	1Eh	W	DCAU code				DCAL code			
31	1Fh	W	Lower-byte per-bit invert control register for DQ calibration							
32	20h	W	Upper-byte per-bit invert control register for DQ calibration							
33	21h	W	DQ calibration pattern A (default = 5Ah)							
34	22h	W	DQ calibration pattern B (default = 3Ch)							
35	23h	R	WCK2DQI oscillator count – LSB							
36	24h	R	WCK2DQI oscillator count – MSB							
37	25h	R/W	WCK2DQI interval timer run-time setting							
38	26h	R	WCK2DQO oscillator count – LSB							
39	27h	R	WCK2DQO oscillator count – MSB							
40	28h	R/W	WCK2DQO interval timer run-time setting							
41	29h	R/W	NT DQ ODT			PPRE	RFU			
42	2Ah	W	PPR key protection							
43	2Bh	R	DBE Flag	SBEC Rule	SBE Count					
44	2Ch	R	Data ECC syndrome[7:0]							
45	2Dh	R	Data ECC syndrome[8]	Error byte lane	DMI ECC syndrome					
46	2Eh	W	RFU					FIFO RDQS training	RDQS toggle	Enhanced RDQS
47–54	2Fh≈36h	R	Serial ID							
55	37h	-	Do not use							
56	38h	W	Reserved for testing purpose							
57	39h	R	Refresh Management							
58	3Ah	W	Pre Emphasis							
59	3Bh	-	Do not use							

Table 1: Mode Register Assignments (Continued)

Notes apply to entire table

MR#	MA[6:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
60	3Ch	-	Reserved for testing purpose							
61–127	3Dh≈7F	–	Do not use							

Notes:
1. The MRW command must not write to RFU bits other than to set them to 0. The MRR command reads RFU bits as 0.
2. The MRR command reads undefined data for mode registers that are specified as RFU or write-only.
3. A WRITE to a read-only register does not affect device functionality.
4. Colored cells indicate MR bits with three different physical registers: FSP0, FSP1, and FSP2 (Frequency Set Point).

MR0–MR2

MR0 Latency Mode

Table 2: MR0 Register Information (MA[6:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Pre Emphasis	Unified NT-ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT-ODT timing mode

Table 3: MR0 Op-Code Bit Definitions

Register Information	Type	OP	Definition	Notes
NT ODT timing mode	R	OP[0]	0b: Device supports the same NT-ODT latency for DQ and RDQS (default)	1
			1b: Device supports different NT-ODT latency for DQ and RDQS	
Latency mode	R	OP[1]	0b: Device supports x16 mode latency	2
			1b: Device supports byte mode latency	
Enhanced WCK always on mode	R	OP[2]	0b: Device does not support enhanced WCK always on mode	3
			1b: Device supports enhanced WCK always on mode	
Optimized refresh mode	R	OP[3]	0b: Device does not support optimized refresh mode	4
			1b: Device supports optimized refresh mode	
DMI output behavior mode	R	OP[4]	0b: Device only supports DMI behavior mode 1	5
			1b: Device supports both DMI behavior mode 1 and 2 and mode selection	

Table 3: MR0 Op-Code Bit Definitions (Continued)

Register Information	Type	OP	Definition	Notes
Unified NT-ODT behavior	R	OP[5]	0b: The NT-ODT behavior does not follow the unified NT-ODT behavior	6
			1b: The NT-ODT behavior follows the unified NT-ODT behavior	
Pre Emphasis	R	OP[6]	0b: Pre Emphasis mode not supported	
			1b: Pre Emphasis mode supported	

Notes:
1. The device supports separate DQ/RDQS NT-ODT timing as an optional feature. See the NT ODT Behavior for Read Operation section for more information.
2. Byte mode latency is supported only by a byte mode device.
3. Enhanced WCK always on mode is an optional feature. See the Enhanced WCK Always On Mode section for more information.
4. Optimized refresh is an optional feature for self refresh mode. See the Optimized Refresh section for more information.
5. Selection of DMI behavior mode 2 or DMI behavior mode at read FIFO and read DQ calibration is optional. DMI behavior mode can be selected using MR13 OP[4]. See the DMI Output Behavior Mode section for more information.
6. Unified NT-ODT behavior is an optional feature for LPDDR5. All LPDDR5X SDRAM(MR8 OP[1:0]=01b) supports only Unified NT-ODT behavior and MR0 OP[5] is don't care. See the NT-ODT Behavior Unification section for more information.

MR1 CK Mode and WL

Table 4: MR1 Register Information (MA[6:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WL				CK mode	RFU		

Table 5: MR1 OP[7:0] Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
CK mode	R/W	OP[3]	0b: Differential (default) 1b: Single ended from CK_t	1, 2, 3
WL		OP[7:4]	See the following latency tables for WL for each MR1 setting.	2, 3

Notes:
1. When MR1 OP[3] = 1b, CK_t is used as CK timing and CK_c is set to a valid logic state.
2. Three physical registers are assigned to each bit of this MR parameter, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.

Table 6: MR1 OP[7:4] Op-Code Bit Definitions: DVFSC Disabled

MR1 OP[7:4]	WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		WL (*n*CK)	
		Lower (>)	Upper (≤)	Lower (>)	Upper (≤)	Set A	Set B
0000	2:1	40	533	10	133	4	4
0001	2:1	533	1067	133	267	4	6
0010	2:1	1067	1600	267	400	6	8
0011	2:1	1600	2133	400	533	8	10
0100	2:1	2133	2750	533	688	8	14
0101	2:1	2750	3200	688	800	10	16
0000	4:1	40	533	5	67	2	2
0001	4:1	533	1067	67	133	2	3
0010	4:1	1067	1600	133	200	3	4
0011	4:1	1600	2133	200	267	4	5
0100	4:1	2133	2750	267	344	4	7
0101	4:1	2750	3200	344	400	5	8
0110	4:1	3200	3733	400	467	6	9
0111	4:1	3733	4267	467	533	6	11
1000	4:1	4267	4800	533	600	7	12
1001	4:1	4800	5500	600	688	8	14
1010	4:1	5500	6000	688	750	9	15
1011	4:1	6000	6400	750	800	9	16
1100	4:1	6400	7500	800	937.5	11	19
1101	4:1	7500	8533	937.5	1066.5	12	22

Notes:
1. Write latency applies for both x16 and x8 SDRAM.
2. Write latency applies regardless of the following function settings: (Disable/Enable) Byte mode, write DBI, write data copy, and link ECC.
3. The device must not be operated at a frequency above the upper frequency limit, or below the lower frequency limit shown for each WL value.
4. Write latency set A and set B are determined by MR3 OP[5]. When MR3 OP[5] = 0, then Write latency set A is used. When MR3 OP[5] = 1, then Write latency set B is used.

Table 7: MR1 OP[7:4] Op-Code Bit Definitions: DVFSC Enabled

MR1 OP[7:4]	WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		WL (*n*CK)	
		Lower (>)	Upper (≤)	Lower (>)	Upper (≤)	Set A	Set B
0000	2:1	40	533	10	133	4	4
0001	2:1	533	1067	133	267	4	6
0010	2:1	1067	1600	267	400	6	8
0000	4:1	40	533	5	67	2	2
0001	4:1	533	1067	67	133	2	3

Table 7: MR1 OP[7:4] Op-Code Bit Definitions: DVFSC Enabled (Continued)

MR1 OP[7:4]	WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		WL (*n*CK)	
		Lower (>)	Upper (≤)	Lower (>)	Upper (≤)	Set A	Set B
0010	4:1	1067	1600	133	200	3	4

Notes:
1. Write latency applies for both x16 and x8 SDRAM.
2. Write latency applies regardless of the following function setting: (Disable/Enable) Byte Mode, Write DBI, Write Data Copy and Link ECC.
3. The device must not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each WL value.
4. Write latency Set A and Set B are determined by MR3 OP[5]. When MR3 OP[5] = 0, then Write latency Set A is used. When MR3 OP[5] = 1, then Write latency Set B is used.

MR2 RL, *n*RBTP, and *n*WR

Table 8: MR2 Register Information (MA[6:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
*n*WR				RL, *n*RBTP			

Table 9: MR2 OP[7:0] Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RL, *n*RBTP	W	OP[3:0]	RL and *n*RBTP for DVFSC enabled and disabled are show in the following tables.	1, 2, 3, 5, 6
*n*WR	W	OP[7:4]	*n*WR for DVFSC enabled and disabled are show in the following tables.	1, 2, 3, 4

Notes:
1. The device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit shown for each RL and *n*RBTP and *n*WR value.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
4. The programmed value of *n*WR is the number of clock cycles that the device uses to determine the starting point of an internal PRE-CHARGE operation that follows a WRITE burst with AP (auto-precharge) enabled. It is determined by RU(^{t}WR/^{t}CK).
5. The programmed value of *n*RBTP is the number of clock cycles that the device uses to determine the starting point of an internal PRECHARGE operation that follows a READ burst with AP (auto-precharge). It is determined by RU(^{t}RBTP/^{t}CK).
6. Some operating features can affect Read latency: 1) Byte mode; 2) Read DBI and/or read data copy.
   - RL Set 0 applies when no features are enabled.

- RL Set 1 applies when one feature is enabled (#1 or #2).
- RL Set 2 applies when two features are enabled (#1 and #2).

The READ command and read timing latency begin at the rising edge of CK_t. Read latency is specified separately for DVFSC Disabled and DVFSC Enabled cases. For each MR2 OP[3:0] setting, device operation below CK lower limit or above CK upper limit is illegal.

Table 10: MR2 Op-Code Bit Definitions: DVFSC and ECC Disabled

WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		OP[7:4]	*n*WR (*n*CK)		OP[3:0]	RL Sets (*n*CK)			*n*RBTP (*n*CK)
	Lower (>)	Upper (≤)	Lower (>)	Upper (≤)		x16	x8		Set 0	Set 1	Set 2	
2:1	40	533	10	133	0000b	5	5	0000b	6	6	6	0
2:1	533	1067	133	267	0001b	10	10	0001b	8	8	8	0
2:1	1067	1600	267	400	0010b	14	15	0010b	10	10	12	0
2:1	1600	2133	400	533	0011b	19	20	0011b	12	14	14	0
2:1	2133	2750	533	688	0100b	24	25	0100b	16	16	18	2
2:1	2750	3200	688	800	0101b	28	29	0101b	18	20	20	2
4:1	40	533	5	67	0000b	3	3	0000b	3	3	3	0
4:1	533	1067	67	133	0001b	5	5	0001b	4	4	4	0
4:1	1067	1600	133	200	0010b	7	8	0010b	5	5	6	0
4:1	1600	2133	200	267	0011b	10	10	0011b	6	7	7	0
4:1	2133	2750	267	344	0100b	12	13	0100b	8	8	9	1
4:1	2750	3200	344	400	0101b	14	15	0101b	9	10	10	1
4:1	3200	3733	400	467	0110b	16	17	0110b	10	11	12	2
4:1	3733	4267	467	533	0111b	19	20	0111b	12	13	14	2
4:1	4267	4800	533	600	1000b	21	22	1000b	13	14	15	3
4:1	4800	5500	600	688	1001b	24	25	1001b	15	16	17	4
4:1	5500	6000	688	750	1010b	26	28	1010b	16	17	19	4
4:1	6000	6400	750	800	1011b	28	29	1011b	17	18	20	4
4:1	6400	7500	800	937.5	1100b	32	34	1100b	20	22	24	6
4:1	7500	8533	937.5	1066.5	1101b	37	39	1101b	23	25	26	6

Table 11: MR2 Op-Code Bit Definitions: DVFSC Enabled Link ECC Disabled

WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		OP[7:4]	*n*WR (*n*CK)		OP[3:0]	RL Sets (*n*CK)			*n*RBTP (*n*CK)
	Lower (>)	Upper (≤)	Lower (>)	Upper (≤)		x16	x8		Set 0	Set 1	Set 2	
2:1	40	533	10	133	0000b	6	6	0000b	6	6	6	0
2:1	533	1067	133	267	0001b	11	12	0001b	8	10	10	0
2:1	1067	1600	267	400	0010b	17	18	0010b	12	12	14	0
4:1	40	533	5	67	0000b	3	3	0000b	3	3	3	0

Table 11: MR2 Op-Code Bit Definitions: DVFSC Enabled Link ECC Disabled (Continued)

WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		OP[7:4]	*n*WR (*n*CK)		OP[3:0]	RL Sets (*n*CK)			*n*RBTP (*n*CK)
	Lower (>)	Upper (≤)	Lower (>)	Upper (≤)		x16	x8		Set 0	Set 1	Set 2	
4:1	533	1067	67	133	0001b	6	6	0001b	4	5	5	0
4:1	1067	1600	133	200	0010b	9	9	0010b	6	6	7	0

Table 12: MR2 Op-Code Bit Definitions: DVFSC Disabled, Link ECC Enabled

WCK:CK Ratio	Limits: Data Rate Range (Mb/s)		Limits: CK Frequency Range (MHz)		OP[7:4]	*n*WR (*n*CK)		OP[3:0]	RL Sets (*n*CK)		*n*RBTP (*n*CK)
	Lower (>)	Upper (≤)	Lower (>)	Upper (≤)		x16	x8		Set 0	Set 1	
4:1	3200	3733	400	467	0110b	18	19	0110b	12	13	2
4:1	3733	4267	467	533	0111b	21	22	0111b	13	14	2
4:1	4267	4800	533	600	1000b	23	24	1000b	15	16	3
4:1	4800	5500	600	688	1001b	27	28	1001b	17	18	4
4:1	5500	6000	688	750	1010b	29	31	1010b	18	20	4
4:1	6000	6400	750	800	1011b	31	32	1011b	19	21	4
4:1	6400	7500	800	937.5	1100b	36	38	1100b	23	24	6
4:1	7500	8533	937.5	1066.5	1101b	41	43	1101b	26	28	6

MR3–MR13

MR3 PDDS, BK/BG ORG, WLS, and DBI

Table 13: MR3 Register Information (MA[6:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	WLS	BK/BG ORG		PDDS		

Table 14: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PDDS (pull-down drive strength)	R/W	OP[2:0]	000b: RFU 001b: R_{ZQ}/1 010b: R_{ZQ}/2 011b: R_{ZQ}/3 100b: R_{ZQ}/4 101b: R_{ZQ}/5 110b:R_{ZQ}/6 (default) 111b: Reserved	1, 2, 3
BK/BG ORG (bank/bank group organization)		OP[4:3]	00b: BG mode 01b: 8B mode 10b: 16B mode (default) 11b: Reserved	2, 3
WLS (write latency set)		OP[5]	0b: Write latency set A (default) 1b: Write latency set B	2, 3
DBI-RD (DBI-RD select)		OP[6]	0b: Disabled (default) 1b: Read DBI enabled	2, 3
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default) 1b: Write DBI enabled	2, 3, 4

Notes:
1. All values are typical. The actual value after calibration is within the specified tolerance for a given voltage and temperature. Recalibration might be required as voltage and temperature vary.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
4. A MASKED WRITE command must use DBI-DC only. For more details concerning a MASKED WRITE with DBI enabled, refer to the Data Bus Inversion section.
5. 16B mode with seamless burst with DVFSC enabled can support up to 1600 Mb/s.
6. The supported operation data rate for each bank/bank group organization is as follows:
   - BG mode is supported for more than 3200 Mb/s (>3200 Mb/s).
   - 16B mode for equal to or less than 3200 Mb/s (≤3200 Mb/s).
   - 8B mode for all data rates.

MR4 Refresh and ZQ Calibration Information

Table 15: MR4 Register Information (MA[6:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	ZQ master	ZQUF	Refresh multiplier				

Table 16: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh multiplier (RM)	R	OP[4:0]	00000b: SDRAM low temperature operating limit exceeded 00001b: 8x refresh 00010b: 6x refresh 00011b: 4x refresh 00100b: 3.3x refresh 00101b: 2.5x refresh 00110b: 2.0x refresh 00111b: 1.7x refresh 01000b: 1.3x refresh 01001b: 1x refresh 01010b: 0.7x refresh 01011b: 0.5x refresh 01100b: 0.25x refresh, no derating 01101b: 0.25x refresh, with derating 01110b: 0.125x refresh, no derating 01111b: 0.125x refresh, with derating 11111b: SDRAM high-temperature operating limit exceeded. All others are reserved	1–4, 6, 7
ZQUF		OP[5]	0b: No change in calibration code since last ZQ LATCH command 1b: Changes in calibration code since last ZQ LATCH command	8
ZQ master		OP[6]	0b: Not a master die 1b: Master die for ZQ calibration purposes	9, 10
TUF (temperature update flag)		OP[7]	0b: No change in OP[4:0] since last MR4 read 1b: Change in OP[4:0] since last MR4 read (default)	5–7

Notes:
1. The refresh multiplier for each MR4 OP[4:0] setting applies to ^{t}REFI, ^{t}REFIpb, and ^{t}REFW. MR4 OP[4:0] = 01001b corresponds to a device temperature of 85°C. Other values require either a longer (1.3x, 8x) refresh interval at lower temperatures or a shorter (0.7x, 0.125x) refresh interval at higher temperatures. If MR4 OP[4:0] = 11111b, the device temperature is greater than 85°C.
2. At higher temperatures (>85°C), AC timing derating might be required. If derating is required, the device sets MR4 OP[4:0] = 01101b and 01111b. See Derating Timing Requirements in the AC Timing section.

3. DRAM vendors might not report all of the possible settings above the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device might not operate properly when MR4 OP[4:0] = 00000b or 11111b.
5. When MR4 OP[7] = 1b, the refresh multiplier reported in MR4 OP[4:0] has changed since the last MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.
6. MR4 OP[4:0] bits indicate the latest refresh rate whenever MR4 OP[7] = 1b.
7. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
8. After the power up initialization and reset sequences have been completed, ZQUF MR4 OP[5] = 0b.
9. In command-based calibration mode, ZQCAL START commands only need to be issued to the ZQ master die to maintain accurate calibration. ZQCAL START commands received by non-ZQ master die are ignored. All die which share ZQ pin resources with a ZQ master die that receives a valid ZQCAL START command are calibrated. ZQCAL LATCH commands can be issued to each of these die after ^{t}ZQCAL4, ^{t}ZQCAL8, or ^{t}ZQCAL16 has been met.
10. LPDDR5 packages with more than one ZQ pin might include more than one ZQ master die.

MR5–MR8 Device Information

Table 17: MR5 Register Information (MA[6:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 18: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	R	OP[7:0]	1111 1111b : Micron

Table 19: MR6 Register Information (MA[6:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 20: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	R	OP[7:0]	xxxx xxxxb: Revision ID1

Note: 1. MR6 is vendor-specific.

Table 21: MR7 Register Information (MA[6:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 22: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	R	OP[7:0]	xxxx xxxxb: Revision ID2

Note: 1. MR7 is vendor-specific.

Table 23: MR8 Register Information (MA[6:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 24: MR8 Op-Code Bit Definitions

Feature	Type	Op	Definition	
Type	R	OP[1:0]	00b:	S32 SDRAM (32*n* prefetch/8B mode), S16 SDRAM (16*n* prefetch/BG mode), S16 SDRAM (16*n* prefetch/16B mode)
			01b:	LPDDR5X SDRAM
			All others:	Reserved
Density		OP[5:2]	0000b:	2Gb
			0001b:	3Gb
			0010b:	4Gb
			0011b:	6Gb
			0100b:	8Gb
			0101b:	12Gb
			0110b:	16Gb
			0111b:	24Gb
			1000b:	32Gb
			All others:	Reserved
I/O width		OP[7:6]	00b:	x16
			01b:	x8
			All others:	Reserved

MR9 Test Mode

Table 25: MR9 Register Information (MA[6:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 26: MR9 Op-Code Bit Definitions

Feature	Type	OP	Definition
Test mode	W	OP[7:0]	0000000b; Vendor-specific test mode disabled(default)

MR10 Preamble/Postamble

Table 27: MR10 Register Information (MA[6:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RPST length		RDQS PRE		WCK PST		RFU	RPST mode

Table 28: MR10 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
RPST mode (RDQS postamble mode)	W	OP[0]	0b: Toggle mode (default) 1b: Static mode	1, 2, 3, 4
WCK PST (WCK postamble length)		OP[3:2]	00b: 2.5 × ^{t}WCK (default) 01b: 4.5 × ^{t}WCK 10b: 6.5 × ^{t}WCK 11b: Reserved	1, 2, 3, 4, 5
RDQS PRE (RDQS preamble length)		OP[5:4]	00b: Static: 4 × ^{t}WCK, toggle: 0 (default) 01b: Static: 2 × ^{t}WCK, toggle: 2 × ^{t}WCK 10b: Static: 0, toggle: 4 × ^{t}WCK 11b: Static:^{t}RDQS_PRE, toggle: 4 × ^{t}WCK	1, 2, 3, 6, 7
RPST length (RDQS postamble length)		OP[7:6]	00b: 0.5 × ^{t}WCK (default) 01b: 2.5 × ^{t}WCK 10b: 4.5 × ^{t}WCK 11b: Reserved	1, 2, 3, 4

Notes:
1. All units in ^{t}WCK.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.

4. ^{t}WCKPST length must be larger than ^{t}RPST length.
5. WCK PST OP[3:2] applies as same setting to both READ and WRITE operation timings.
6. OP[5:4] = 11b can be supported over 3200 Mb/s operation. ^{t}RDQS_PRE is Min 2 × ^{t}WCK and Max 4 × ^{t}WCK.
7. OP[5:4] = 00b/01b/10b can be supported over all frequency ranges.

MR11 ODT Control

Table 29: MR11 Register Information (MA[6:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA ODT			NT-ODT enable	DQ ODT		

Table 30: MR11 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
DQ ODT (DQ bus receiver on-die termination)	R/W	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3, 4
NT-ODT EN (non-target on-die termination enable)		OP[3]	0b: Target ODT mode (default) 1b: Non-target ODT mode	1, 2, 3, 4
CA ODT (CA bus receiver on-die termination)		OP[6:4]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3, 4

Notes:
1. All values are typical. The actual value after calibration is within the specified tolerance for a given voltage and temperature. Recalibration might be required as voltage and temperature vary.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
4. The device operates only according to values stored in the registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in the registers for the inactive set points are ignored by the device and can be changed without affecting device operation.

MR12 $V_{REF(CA)}$

Table 31: MR12 Register Information (MA[6:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
VBS	$V_{REF(CA)}$						

Table 32: MR12 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	R/W	OP[6:0]	0000000b–1111111b: See V_{REF} Settings table All others: Reserved	1–5, 7
VBS ($V_{REF(CA)}$ byte select)	W	OP[7]	0b: Write the $V_{REF(CA)}$ values to OP[6:0] for x16 device, and byte mode device which is assigned lower byte: DQ[7:0]. (default) 1b: Write the $V_{REF(CA)}$ values to OP[6:0] for byte-mode device which is assigned upper byte: DQ[15:8].	6, 7

Notes:
1. This register controls the $V_{REF(CA)}$ levels for frequency set point[2:0].
2. A read MRR to this register places the contents of OP[6:0] on DQ[6:0]. DQ[7] will read 0b.
3. A WRITE command to MR12 OP[6:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR16 OP[1:0] = 00b, for FSP[1] when MR16 OP[1:0] = 01b, or for FSP[2] when MR16 OP[1:0] = 10b. The time required for $V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(CA)}$ training section for more information.
4. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address or read with an MRR command from this address.
5. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
6. OP[7] is not a sticky bit.
7. For a byte mode device, the MRR command outputs each individual MR12 OP[6:0] on DQ[7:0] for the lower-byte device and on DQ[15:8] for the upper-byte device. OP[7] controls only the MRW operation.

Table 33: $V_{REF(CA)}$ Settings

Function	OP	$V_{REF(CA)}$ (% of V_{DDQ})			
V_{REF} Setting for MR12	OP[6:0]	0000000b: 10.0%[5]	0100000b: 26.0%	1000000b: 42.0%	1100000b: 58.0%
		0000001b: 10.5%[5]	0100001b: 26.5%	1000001b: 42.5%	1100001b: 58.5%
		0000010b: 11.0%[5]	0100010b: 27.0%	1000010b: 43.0%	1100010b: 59.0%
		0000011b: 11.5%[5]	0100011b: 27.5%	1000011b: 43.5%	1100011b: 59.5%
		0000100b: 12.0%[5]	0100100b: 28.0%	1000100b: 44.0%	1100100b: 60.0%
		0000101b: 12.5%[5]	0100101b: 28.5%	1000101b: 44.5%	1100101b: 60.5%
		0000110b: 13.0%[5]	0100110b: 29.0%	1000110b: 45.0%	1100110b: 61.0%
		0000111b: 13.5%[5]	0100111b: 29.5%	1000111b: 45.5%	1100111b: 61.5%
		0001000b: 14.0%[5]	0101000b: 30.0%	1001000b: 46.0%	1101000b: 62.0%
		0001001b: 14.5%[5]	0101001b: 30.5%	1001001b: 46.5%	1101001b: 62.5%
		0001010b: 15.0%	0101010b: 31.0%	1001010b: 47.0%	1101010b: 63.0%
		0001011b: 15.5%	0101011b: 31.5%	1001011b: 47.5%	1101011b: 63.5%
		0001100b: 16.0%	0101100b: 32.0%	1001100b: 48.0%	1101100b: 64.0%
		0001101b: 16.5%	0101101b: 32.5%	1001101b: 48.5%	1101101b: 64.5%
		0001110b: 17.0%	0101110b: 33.0%	1001110b: 49.0%	1101110b: 65.0%
		0001111b: 17.5%	0101111b: 33.5%	1001111b: 49.5%	1101111b: 65.5%
		0010000b: 18.0%	0110000b: 34.0%	1010000b: 50.0% (default)	1110000b: 66.0%
		0010001b: 18.5%	0110001b: 34.5%	1010001b: 50.5%	1110001b: 66.5%
		0010010b: 19.0%	0110010b: 35.0%	1010010b: 51.0%	1110010b: 67.0%
		0010011b: 19.5%	0110011b: 35.5%	1010011b: 51.5%	1110011b: 67.5%
		0010100b: 20.0%	0110100b: 36.0%	1010100b: 52.0%	1110100b: 68.0%
		0010101b: 20.5%	0110101b: 36.5%	1010101b: 52.5%	1110101b: 68.5%
		0010110b: 21.0%	0110110b: 37%	1010110b: 53.0%	1110110b: 69.0%
		0010111b: 21.5%	0110111b: 37.5%	1010111b: 53.5%	1110111b: 69.5%
		0011000b: 22.0%	0111000b: 38.0%	1011000b: 54.0%	1111000b: 70.0%
		0011001b: 22.5%	0111001b: 38.5%	1011001b: 54.5%	1111001b: 70.5%
		0011010b: 23.0%	0111010b: 39.0%	1011010b: 55.0%	1111010b: 71.0%
		0011011b: 23.5%	0111011b: 39.5%	1011011b: 55.5%	1111011b: 71.5%
		0011100b: 24.0%	0111100b: 40.0%	1011100b: 56.0%	1111100b: 72.0%
		0011101b: 24.5%	0111101b: 40.5%	1011101b: 56.5%	1111101b: 72.5%
		0011110b: 25.0%	0111110b: 41.0%	1011110b: 57.0%	1111110b: 73.0%
		0011111b: 25.5%	0111111b: 41.5%	1011111b: 57.5%	1111111b: 73.5%

Notes:
1. These values can be used for MR12 OP[6:0] to set the $V_{REF(CA)}$ levels in the device.
2. The MR12 register represents either FSP[0], FSP[1], or FSP[2]. Three frequency set points for CA and CK are provided to enable faster switching between terminated and unterminated operation.
3. Absolute $V_{REF(CA)}$ low level (%code × V_{DDQ}) must be higher than or equal to 75mV for normal operation. V_{REF} error is not included in this calculation.

4. Absolute $V_{REF(CA)}$ high level (%code × V_{DDQ}) must be lower than or equal to 350mV. V_{REF} error is not included in this calculation.
5. V_{REF} codes 0000000b to 0001001b can be used only for testing purposes, not for normal operation. V_{REF} accuracy is not guaranteed from 0000000b to 0001001b.

MR13 Thermal Offset, VRO, DMD, CBT Mode, and Dual V_{DD2}

Table 34: MR13 Register Information (MA[6:0] = 0Dh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Dual V_{DD2}	CBT mode	DMD	DMI I/O control	RFU	VRO	Thermal offset	

Table 35: MR13 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Thermal offset	W	OP[1:0]	00b: No offset, 0–5°C gradient (default) 01b: 5°C offset, 5–10°C gradient 10b: 10°C offset, 10–15°C gradient 11b: Reserved	
VRO (V_{REF} output)		OP[2]	0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits	1
DMI I/O control (DMI input/output behavior control mode)		OP[4]	0b: DMI output behavior follows MR settings read DBI, read link ECC, and read data copy (default) 1b: DMI outputs valid data if the READ FIFO command and READ DQ CALIBRATION commands are issued when a data mask and/or write DBI are/is enabled even when read DBI, read link ECC and read data copy are disabled	6
DMD (data mask disable)		OP[5]	0b: Data mask operation enabled (default) 1b: Data mask operation disabled	5
CBT mode		OP[6]	0b: Command bus training mode 1 (default) 1b: Command bus training mode 2	
Dual V_{DD2}		OP[7]	0b: Dual V_{DD2} rail (1.05V and 0.9V) used (default) 1b: Single 1.05V V_{DD2} rail used	2, 3, 4

Notes:
1. When set, the device outputs the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltages on DQ pins. Only the active frequency set point, as defined by MR16 OP[3:2], is output on the DQ pins. This function enables an external test system to measure the internal V_{REF} levels. It is recommended to test around 25°C. The DQ pins used for V_{REF} output are vendor-specific.
2. The device can be powered-up/initialized/reset using either a single or dual V_{DD2} configuration, regardless of the OP[7] setting. OP[7] should be set based on the V_{DD2} configuration during initialization before normal operation. It is illegal to change OP[7] setting during normal operation. See Voltage Ramp and Device Initialization section for additional information.
3. In the single V_{DD2} configuration (1.05V), the same voltage should be supplied to all V_{DD2L} and V_{DD2H} balls.

4. When enabled (OP[7] = 1b), MR19 OP[1:0] setting is ignored and DRAM operates in high-speed mode.
5. When enabled (OP[5] = 0b), data masking is enabled for the device. When disabled (OP[5] = 1b), the MASKED WRITE command is illegal. See the Data Mask (DM) and Data Bus Inversion (DBI) Function section.
6. DMI I/O control: MR13 OP[4] = 1b is optional. See the Read DQ Calibration Training section and the WCK-DQ Training section for more information.

MR14–MR25

MR14 $V_{REF(LDQ)}$

Table 36: MR14 Register Information (MA[6:0] = 0Eh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
VDLC	V_{REF} DQ[7:0]						

Table 37: MR14 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
V_{REF} DQ[7:0]	R/W	OP[6:0]	000000b–1111111b: See V_{REF} DQ[7:0] Settings table All others: Reserved	1–5
VDLC ($V_{REF(DQ)}$ lower-byte copy)		OP[7]	X16 device only 0b: V_{REF} DQ[15:8] follows MR15 OP[6:0] code (default) 1b: V_{REF} DQ[15:8] follows MR14 OP[6:0] code Byte mode devices ignore OP[7] setting	6, 7

Notes:
1. This register controls the V_{REF} DQ[7:0] levels for frequency set point[2:0].
2. An MRR command to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's are set to 0. See the MRR Operation section.
3. An MRW command to OP[6:0] sets the internal V_{REF} DQ[7:0] level for FSP[0] when MR16 OP[1:0] = 00b, for FSP[1] when MR16 OP[1:0] = 01b, or for FSP[2] when MR16 OP[1:0] = 10b. The time required for V_{REF} DQ[7:0] to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF} DQ[7:0] training for more information.
4. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address, or read with an MRR command from this address.
5. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
6. When OP[7] is 1b, MR14 MRR returns V_{REF} DQ[15:8] and the MR15 MRR value is undefined. To verify the V_{REF} code, refer MR14 OP[6:0].
7. A byte-mode device does not support the VDLC function. SOC needs to set MR14 and MR15 to individual devices.

Table 38: V_{REF} DQ[7:0] Settings

Function	OP	V_{REF} Values (% of V_{DDQ})			
V_{REF} SETTING for MR14	OP[6:0]	0000000b: 10.0% [5]	0100000b: 26.0%	1000000b: 42.0%	1100000b: 58.0%
		0000001b: 10.5%[5]	0100001b: 26.5%	1000001b: 42.5%	1100001b: 58.5%
		0000010b: 11.0%[5]	0100010b: 27.0%	1000010b: 43.0%	1100010b: 59.0%
		0000011b: 11.5%[5]	0100011b: 27.5%	1000011b: 43.5%	1100011b: 59.5%
		0000100b: 12.0%[5]	0100100b: 28.0%	1000100b: 44.0%	1100100b: 60.0%
		0000101b: 12.5%[5]	0100101b: 28.5%	1000101b: 44.5%	1100101b: 60.5%
		0000110b: 13.0%[5]	0100110b: 29.0%	1000110b: 45.0%	1100110b: 61.0%
		0000111b: 13.5%[5]	0100111b: 29.5%	1000111b: 45.5%	1100111b: 61.5%
		0001000b: 14.0%[5]	0101000b: 30.0%	1001000b: 46.0%	1101000b: 62.0%
		0001001b: 14.5%[5]	0101001b: 30.5%	1001001b: 46.5%	1101001b: 62.5%
		0001010b: 15.0%	0101010b: 31.0%	1001010b: 47.0%	1101010b: 63.0%
		0001011b: 15.5%	0101011b: 31.5%	1001011b: 47.5%	1101011b: 63.5%
		0001100b: 16.0%	0101100b: 32.0%	1001100b: 48.0%	1101100b: 64.0%
		0001101b: 16.5%	0101101b: 32.5%	1001101b: 48.5%	1101101b: 64.5%
		0001110b: 17.0%	0101110b: 33.0%	1001110b: 49.0%	1101110b: 65.0%
		0001111b: 17.5%	0101111b: 33.5%	1001111b: 49.5%	1101111b: 65.5%
		0010000b: 18.0%	0110000b: 34.0%	1010000b: 50.0% (default)	1110000b: 66.0%
		0010001b: 18.5%	0110001b: 34.5%	1010001b: 50.5%	1110001b: 66.5%
		0010010b: 19.0%	0110010b: 35.0%	1010010b: 51.0%	1110010b: 67.0%
		0010011b: 19.5%	0110011b: 35.5%	1010011b: 51.5%	1110011b: 67.5%
		0010100b: 20.0%	0110100b: 36.0%	1010100b: 52.0%	1110100b: 68.0%
		0010101b: 20.5%	0110101b: 36.5%	1010101b: 52.5%	1110101b: 68.5%
		0010110b: 21.0%	0110110b: 37%	1010110b: 53.0%	1110110b: 69.0%
		0010111b: 21.5%	0110111b: 37.5%	1010111b: 53.5%	1110111b: 69.5%
		0011000b: 22.0%	0111000b: 38.0%	1011000b: 54.0%	1111000b: 70.0%
		0011001b: 22.5%	0111001b: 38.5%	1011001b: 54.5%	1111001b: 70.5%
		0011010b: 23.0%	0111010b: 39.0%	1011010b: 55.0%	1111010b: 71.0%
		0011011b: 23.5%	0111011b: 39.5%	1011011b: 55.5%	1111011b: 71.5%
		0011100b: 24.0%	0111100b: 40.0%	1011100b: 56.0%	1111100b: 72.0%
		0011101b: 24.5%	0111101b: 40.5%	1011101b: 56.5%	1111101b: 72.5%
		0011110b: 25.0%	0111110b: 41.0%	1011110b: 57.0%	1111110b: 73.0%
		0011111b: 25.5%	0111111b: 41.5%	1011111b: 57.5%	1111111b: 73.5%

Notes:
1. Values can be used for MR14 OP[6:0] to set the V_{REF} DQ[7:0] levels in the device.
2. The MR14 register represents either FSP[0], FSP[1], or FSP[2]. Three frequency set points for each DQ are provided to enable faster switching between terminated and unterminated operations, or between different high-frequency settings, which might use different termination values.

3. Absolute DQ[7:0] V_{REF} low level (%code × V_{DDQ}) must be higher than or equal to 75mV. V_{REF} error is not included in this calculation.
4. Absolute DQ[7:0] Vref high level (%code * V_{DDQ}) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[7:0] V_{REF} high level (%code * V_{DDQ}) must be lower than or equal to 225mV when WCK is higher than 1600MHz and less than or equal to 3200MHz. Absolute DQ[7:0] V_{REF} high level (%code * V_{DDQ}) must be lower than or equal to 180mV when WCK is higher than 3200MHz. V_{REF} error including a receiver offset and a training error is not included this calculation. Higher V_{REF} level code can be used for testing and training purposes
5. V_{REF} codes from 0000000B to 0001001B can be used only for testing purpose and not for normal operation. V_{REF} accuracy are not guaranteed from 0000000B to 0001001B.

MR15 $V_{REF(UDQ)}$

Table 39: MR15 Register Information (MA[6:0] = 0Fh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	V_{REF} DQ[15:8]						

Table 40: MR15 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
V_{REF} DQ[15:8]	R/W	OP[6:0]	000000b–1111111b: See V_{REF} DQ[15:8] Settings table All others: Reserved	1–6

Notes:
1. This register controls the V_{REF} DQ[15:8] levels for frequency set point[2:0].
2. An MRR command to this register places the contents of OP[7:0] on DQ[15:8]. Any RFU bits and unused DQ's are set to 0. See the MRR operation section.
3. An MRW command to OP[6:0] sets the internal V_{REF} DQ[15:8] level for FSP[0] when MR16 OP[1:0] = 00b, for FSP[1] when MR16 OP[1:0] = 01b, or for FSP[2] when MR16 OP[1:0] = 10b. Time required for V_{REF} DQ[15:8] to reach the set level depends on the step size from the current level to the new level. See the section on $V_{REF(DQ)}$ training for more information.
4. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address, or read with an MRR command from this address.
5. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
6. The MR15 MRR value is undefined when MR14 OP[7] is 1b. When MR14 OP[7] is 1b, V_{REF} DQ[15:8] can be read from MR14.

Table 41: V_{REF} DQ[15:8] Settings

Function	OP	V_{REF} Values (% of V_{DDQ})			
V_{REF} Setting for MR15	OP[6:0]	0000000b: 10.0% [5]	0100000b: 26.0%	1000000b: 42.0%	1100000b: 58.0%
		0000001b: 10.5%[5]	0100001b: 26.5%	1000001b: 42.5%	1100001b: 58.5%
		0000010b: 11.0%[5]	0100010b: 27.0%	1000010b: 43.0%	1100010b: 59.0%
		0000011b: 11.5%[5]	0100011b: 27.5%	1000011b: 43.5%	1100011b: 59.5%
		0000100b: 12.0%[5]	0100100b: 28.0%	1000100b: 44.0%	1100100b: 60.0%
		0000101b: 12.5%[5]	0100101b: 28.5%	1000101b: 44.5%	1100101b: 60.5%
		0000110b: 13.0%[5]	0100110b: 29.0%	1000110b: 45.0%	1100110b: 61.0%
		0000111b: 13.5%[5]	0100111b: 29.5%	1000111b: 45.5%	1100111b: 61.5%
		0001000b: 14.0%[5]	0101000b: 30.0%	1001000b: 46.0%	1101000b: 62.0%
		0001001b: 14.5%[5]	0101001b: 30.5%	1001001b: 46.5%	1101001b: 62.5%
		0001010b: 15.0%	0101010b: 31.0%	1001010b: 47.0%	1101010b: 63.0%
		0001011b: 15.5%	0101011b: 31.5%	1001011b: 47.5%	1101011b: 63.5%
		0001100b: 16.0%	0101100b: 32.0%	1001100b: 48.0%	1101100b: 64.0%
		0001101b: 16.5%	0101101b: 32.5%	1001101b: 48.5%	1101101b: 64.5%
		0001110b: 17.0%	0101110b: 33.0%	1001110b: 49.0%	1101110b: 65.0%
		0001111b: 17.5%	0101111b: 33.5%	1001111b: 49.5%	1101111b: 65.5%
		0010000b: 18.0%	0110000b: 34.0%	1010000b: 50.0% (default)	1110000b: 66.0%
		0010001b: 18.5%	0110001b: 34.5%	1010001b: 50.5%	1110001b: 66.5%
		0010010b: 19.0%	0110010b: 35.0%	1010010b: 51.0%	1110010b: 67.0%
		0010011b: 19.5%	0110011b: 35.5%	1010011b: 51.5%	1110011b: 67.5%
		0010100b: 20.0%	0110100b: 36.0%	1010100b: 52.0%	1110100b: 68.0%
		0010101b: 20.5%	0110101b: 36.5%	1010101b: 52.5%	1110101b: 68.5%
		0010110b: 21.0%	0110110b: 37%	1010110b: 53.0%	1110110b: 69.0%
		0010111b: 21.5%	0110111b: 37.5%	1010111b: 53.5%	1110111b: 69.5%
		0011000b: 22.0%	0111000b: 38.0%	1011000b: 54.0%	1111000b: 70.0%
		0011001b: 22.5%	0111001b: 38.5%	1011001b: 54.5%	1111001b: 70.5%
		0011010b: 23.0%	0111010b: 39.0%	1011010b: 55.0%	1111010b: 71.0%
		0011011b: 23.5%	0111011b: 39.5%	1011011b: 55.5%	1111011b: 71.5%
		0011100b: 24.0%	0111100b: 40.0%	1011100b: 56.0%	1111100b: 72.0%
		0011101b: 24.5%	0111101b: 40.5%	1011101b: 56.5%	1111101b: 72.5%
		0011110b: 25.0%	0111110b: 41.0%	1011110b: 57.0%	1111110b: 73.0%
		0011111b: 25.5%	0111111b: 41.5%	1011111b: 57.5%	1111111b: 73.5%

Notes:
1. These values can be used for MR15 OP[6:0] to set the V_{REF} DQ[15:8] levels in the device.
2. MR15 registers represent either FSP[0], FSP[1], or FSP[2]. Three frequency-set-points each for DQ are provided to enable faster switching between terminated and unterminated operations, or between different high-frequency settings, which might use different terminations values.

3. Absolute DQ[15:8] V_{REF} low level (%code × V_{DDQ}) must be higher than or equal to 75mV for normal operation. V_{REF} error is not included in this calculation.
4. Absolute DQ[15:8] V_{REF} high level (%code * V_{DDQ}) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[15:8] V_{REF} high level (%code * V_{DDQ}) must be lower than or equal to 225mV when WCK is higher than 1600MHz and less than or equal to 3200MHz. Absolute DQ[15:8] V_{REF} high level (%code * V_{DDQ}) must be lower than or equal to 180mV when WCK is higher than 3200MHz. V_{REF} error including a receiver offset and a training error is not included this calculation. Higher V_{REF} level code can be used for testing and training purposes.
5. V_{REF} codes 0000000b to 0001001b can be used only for testing purposes, not for normal operation. V_{REF} accuracy is not guaranteed from 0000000b to 0001001b.

MR16 FSP, CBT, and VRCG

Table 42: MR16 Register Information (MA[6:0] = 10h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CBT-phase	VRCG	CBT		FSP-OP		FSP-WR	

Table 43: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
FSP-WR (frequency set point write/read)	R/W	OP[1:0]	00b: Frequency set point [0] (default) 01b: Frequency set point [1] 10b: Frequency set point [2] 11b: Reserved	1
FSP-OP (frequency set point operation mode)	R/W	OP[3:2]	00b: Frequency set point [0] (default) 01b: Frequency set point [1] 10b: Frequency set point [2] 11b: Reserved	2
CBT (command bus training)	R/W	OP[5:4]	00b: Normal operation (default) 01b: Command bus training mode enabled FSP[0] 10b: Command bus training mode enabled FSP[1] 11b: Command bus training mode enabled FSP[2]	3, 5
VRCG (V_{REF} current generator)	R/W	OP[6]	0b: Normal operation (default) 1b: V_{REF} fast response (high-current) mode	4
CBT-phase	R/W	OP[7]	0b: DQ outputs CA pattern latched by CK rising edge (default) 1b: DQ outputs CA pattern latched by CK falling edge	

Notes:
1. FSP-WR determines which frequency set point registers are accessed with MRW commands for functions such as $V_{REF(CA)}$ and $V_{REF(DQ)}$ settings. For more information, refer to Frequency Set Point section.
2. FSP-OP determines which frequency set point register values are currently used to specify device operation for functions such as $V_{REF(CA)}$ and $V_{REF(DQ)}$ settings. For more information, refer to the Frequency Set Point section.
3. An MRW command that sets OP[5:4] = 01b, 10b, or 11b causes the device to enter the command bus training mode. When OP[5:4] = 01b, 10b, or 11b, commands are ignored,

and the contents of CA[6:0] are mapped to the DQ bus. See the Command Bus Training section for more information.

4. When OP[6] = 1, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
5. A command-bus, training-mode-enabled FSP must be different from FSP-OP.

MR17 ODT

Table 44: MR17 Register Information (MA[6:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X8ODTD upper	X8ODTD lower	ODTD-CA	ODTD-CS	ODTD-CK	SOC ODT		

Table 45: MR17 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
SOC ODT (controller ODT value for V_{OH} calibration)	R/W	OP[2:0]	000b: Disabled (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3, 6
ODTD-CK (CK ODT termination)		OP[3]	0b: ODTD-CK enabled 1b: ODTD-CK disabled (default)	2, 3, 4
ODTD-CS (CS ODT termination)		OP[4]	0b: ODTD-CS enabled RZQ/3 1b: ODTD-CS disabled (default)	2, 3, 5, 7
ODTD-CA (CA ODT termination)		OP[5]	0b: ODTD-CA enabled 1b: ODTD-CA disabled (default)	2, 3, 4
X8ODTD lower (CA/CK ODT termination disable, lower-byte select)		OP[6]	x8 per ch only, lower-byte selected device 0b: ODTD-CA/CK follows MR17 OP[4:3] and MR11 OP[6:4] (default) 1b: ODTD-CA/CK disabled	7
X8ODTD upper (CA/CK ODT termination disable, upper-byte select)		OP[7]	x8 per ch only, upper-byte selected device 0b: ODTD-CA/CK follows MR17 OP[4:3] and MR11 OP[6:4] (default) 1b: ODTD-CA/CK disabled	7

Notes:
1. All values are typical.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.

3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
4. To ensure proper operation in a multi-rank configuration, when CA, CK ODT is enabled via MR11 OP[6:4], MR17 OP[3] and OP[5], the rank providing ODT will continue to terminate in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Idle Power-down.
5. To ensure proper operation in a multi-rank configuration, when CS is enabled via MR17 OP[4], the rank providing ODT will continue to terminate in all DRAM states except Idle Power-down, Active Power-down, Self-refresh Power-down and Deep Sleep Mode. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.
6. The device pull-up driver strength is controlled by OP[2:O] SOC ODT setting when DQ termination is disabled.
7. When MR21 OP[3] = 0b, the device ignores all CS ODT settings, and CS remains unterminated at all times.

MR18 WCK

Table 46: MR18 Register Information (MA[6:0]=12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CKR	WCK2CK leveling	RFU	WCK ON	WCK FM	WCK ODT		

Table 47: MR18 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
WCK ODT	W	OP[2:0]	000b: ODT disabled (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b:RZQ/6 111b: RFU	1, 2, 4
WCK FM (WCK Frequency mode)		OP[3]	0b: WCK Low frequency mode (default) 1b: WCK High frequency mode	1, 2, 5
WCK ON (WCK always on mode)		OP[4]	0b: WCK always on mode disabled (default) 1b: WCK always on mode enabled	1, 2
WCK2CK Leveling		OP[6]	0b: WCK2CK leveling mode disable (default) 1b: WCK2CK leveling mode enabled	
CKR (WCK to CK frequency ratio)		OP[7]	0b: 4:1 ratio 1b: 2:1 ratio (default)	1, 2, 3

Notes:
1. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
3. 2:1 CKR can support up to 3200 Mb/s.
4. The device continues to terminate WCK in all states if termination is enabled by MR18 OP[2:0].
5. tWCK2DQ AC parameters can be changed by MR18 OP[3]. Refer to tWCK2DQ AC parameter table. WCK single-ended mode (MR20 OP[3:2]) can be allowed during Low frequency mode only.

MR19 WCK2DQ OSC and DVFS

Table 48: MR19 Register Information (MA[6:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		WCK2DQ OSC FM support	WCK2DQ OSC FM	DVFSQ		DVFSC	

Notes:
1. ^{t}WCK2DQ AC parameters can be changed by MR19 OP[4]. Refer to ^{t}WCK2DQ AC parameter table. WCK single-ended mode (MR20 OP[3:2]) can be enabled during low-frequency mode only.
2. When operating in WCK low-frequency mode (MR19 OP[4] = 0b), WCK2DQ oscillator for WCK high-frequency mode (MR18 OP[5] = 1b) can be enabled and vice versa.

Table 49: MR19 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
DVFSC	W	OP[1:0]	00b: High-speed mode (only V_{DD2H}: 1.05V rail) (default) 01b: Low-speed mode (use V_{DD2L}: 0.9V rail) All others : Reserved	1, 2
DVFSQ	W	OP[3:2]	00b: V_{DDQ} = 0.5V (default) 01b: V_{DDQ} = 0.3V All others: Reserved	1, 2, 3
WCK2DQ OSC FM	W	OP[4]	0b: WCK2DQ oscillator for WCK low-frequency mode (default) 1b: WCK2DQ oscillator for WCK high-frequency mode	1, 2, 4, 5
WCK2DQ OSC FM support	R	OP[5]	0b: WCK2DQ OSC FM not supported 1b: WCK2DQ OSC FM supported	

Notes:
1. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
3. When DVFSQ OP[3:2] is 01b, the device will turn off all ODT DQ, CS, CA, CK and WCK; DQ NT-ODT turns off regardless of the ODT and NT ODT MR setting.
4. MR19 OP[4] is "Don't Care" when MR19 OP[5] = 0B (LPDDR5 WCK2DQ OSC FM not supported) and WCK2DQ OSC follows MR18 OP[3] WCK frequency mode.
5. When operating in WCK low frequency mode (MR18 OP[3]=0B), WCK2DQ oscillator for WCK high frequency mode (MR19 OP[4]=1B) can be enabled and vice versa.

MR20 RDQS, WCK Mode, MRW Byte Control, and RDC Mode

Table 50: MR20 Register Information (MA[6:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RDC DQ mode	RDC DMI mode	MRWDU	MRWDL	WCK mode		RDQS	

Table 51: MR20 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RDQS (read DQS)	W	OP[1:0]	00b: RDQS_t and RDQS_c disabled 01b: RDQS_t enabled and RDQS_c disabled (default) 10b: RDQS_t and RDQS_c enabled 11b: RDQS_t disabled and RDQS_c enabled	1, 2, 3, 6, 7, 9, 11
WCK MODE		OP[3:2]	00b: Differential (default) 01b: Single-ended from WCK_t 10b: Single-ended from WCK_c 11b: Reserved	1, 2, 4, 5, 8
MRWDL (mode register write disable, lower byte)		OP[4]	0b: Lower-byte MRW is enabled (default) 1b: Lower-byte MRW is disabled	10
MRWDU (mode register write disable, upper byte)		OP[5]	0b: Upper-byte MRW is enabled (default) 1b: Upper-byte MRW is disabled	10
RDC DMI Mode		OP[6]	In Read DQ calibration, DMI output pattern is controlled as: 0b: DMI pattern will be decided by MR33/34 (default) 1b: DMI pattern will be fixed LOW	
RDC DQ MODE		OP[7]	In Read DQ calibration, DQ output pattern is controlled by the MR33/34 (pattern) and MR31/32 (per-bit control), where, MR31/32 function is defined as : 0b: MR31/32 decides whether invert or not (default) 1b: MR31/32 decides whether LOW-fixed or not	

Notes:
1. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
3. WCK clocking generates RDQS_t and RDQS_c.
4. When MR20 OP[3:2] = 01b, WCK_t is used as WCK timing, and WCK_c shall be maintained at a valid logic level.
5. When MR20 OP[3:2] = 10b, WCK_c is used as WCK timing, and WCK_t shall be maintained at a valid logic level.
6. When MR20 OP[1:0] = 01b, RDQS_t is used as RDQS timing, and RDQS_c is High-Z state.
7. When MR20 OP[1:0] = 11b, RDQS_c is used as RDQS timing, and RDQS_t is High-Z state.
8. When MR20 OP[3:2] = 01b, WCK_t polarity is the same as WCK_t in MR20 OP[3:2] = 00b, and when MR20 OP[3:2] = 10b, WCK_c polarity is the same as WCK_c in MR20 OP[3:2] = 00b.
9. When MR20 OP[1:0] = 01b, RDQS_t polarity is the same as RDQS_t in MR20 OP[1:0] = 10b, and when MR20 OP[1:0] = 11b, RDQS_c polarity is the same as RDQS_c in MR20 OP[1:0] = 10b.
10. Enabling this OP bit is not valid for x16 die.
11. Changing MR20 OP[1:0] is not allowed during RDQS toggle mode or enhanced RDQS training mode.

MR21 Data Copy and Write X

Table 52: MR21 Register Information (MA[6:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WXS	WXFE	RDCFE	WDCFE	ODTD-CSFS	WXFS	RDCFS	WDCFS

Table 53: MR21 Op-Code Bit Definitions

Feature	Type	OP	Definition	Note
WDCFS (WRITE DATA COPY function support)	R	OP[0]	0b: WRITE DATA COPY function not supported 1b: WRITE DATA COPY function supported	4
RDCFS (READ DATA COPY function support)		OP[1]	0b: READ DATA COPY function not supported 1b: READ DATA COPY function supported	4
WXFS (WRITE X function support)		OP[2]	0b: WRITE X function not supported 1b: WRITE X function supported	4
ODTD-CSFS (ODTD-CS function support)		OP[3]	0b: Device ODTD-CS not supported 1b: Device ODTD-CS supported	4
WDCFE (WRITE DATA COPY function enable)	W	OP[4]	0b: WRITE DATA COPY function disable (default) 1b: WRITE DATA COPY function enable	1
RDCFE (READ DATA COPY function enable)		OP[5]	0b: READ DATA COPY function disable (default) 1b: READ DATA COPY function enable	2
WXFE (WRITE X function enable)		OP[6]	0b: WRITE X function disable (default) 1b: WRITE X function enable	3
WXS (SELECTION function of data to be written by the WRITE X function)	R	OP[7]	0b: Data to be written is 0 only 1b: Data to be written can be selected with 0 and 1 with per-byte control	4

Notes:
1. MR21 OP[4] is "Don't Care" when MR21 OP[0] = 0b (WRITE DATA COPY function is not supported).
2. MR21 OP[5] is "Don't Care" when MR21 OP[1] = 0b (READ DATA COPY function is not supported).
3. MR21 OP[6] is "Don't Care" when MR21 OP[2] = 0b (WRITE X function is not supported).
4. DATA COPY, WRITE X, and ODTD-CS functions are optional. Refer to vendor's data sheet.

MR22 Link ECC

Table 54: MR22 Register Information (MA[6:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RECC		WECC		RFU			

Table 55: MR22 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
WECC (write link ECC control)	W	OP[5:4]	00b: Write link ECC disable (default) 01b: Write link ECC enable 10b: Reserved 11b: Reserved	1, 2, 3
RECC (read link ECC control)		OP[7:6]	00b: Read link ECC disable (default) 01b: Read link ECC enable 10b: Reserved 11b: Reserved	1, 2, 3

Notes:
1. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
3. Refer to Link ECC descriptions.

MR23 PASR Segment Mask

Table 56: MR23 Register Information (MA[6:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 57: MR23 Op-Code Bit Definitions

Feature	Type	OP	Data	Note
PASR segment mask	W	OP[7:0]	0: Segment refresh enable (default) 1: Segment refresh disabled	1, 2

Table 58: Row Address of Masked Segment for x16 Mode

Segment	OP[n]	Segment Mask	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R[12:10]	R[13:11]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]
0	0	xxxxxxx1	000b								
1	1	xxxxxx1x	001b								
2	2	xxxxx1xx	010b								
3	3	xxxx1xxx	011b								
4	4	xxx1xxxx	100b								

Table 58: Row Address of Masked Segment for x16 Mode (Continued)

Segment	OP[n]	Segment Mask	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R[12:10]	R[13:11]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]
5	5	xx1xxxxx	101b								
6	6	x1xxxxxx	110b	Not Allowed	110b	Not Allowed	110b	Not Allowed	110b	Not Allowed	110b
7	7	1xxxxxxx	111b		111b		111b		111b		111b

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is "Don't Care" for a particular segment.
2. For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (= 00b).

Table 59: Row Address of Masked Segment for x8 Mode

Segment	OP[n]	Segment Mask	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R[13:11]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]	R[17:R15]
0	0	xxxxxxx1	000b								
1	1	xxxxxx1x	001b								
2	2	xxxxx1xx	010b								
3	3	xxxx1xxx	011b								
4	4	xxx1xxxx	100b								
5	5	xx1xxxxx	101b								
6	6	x1xxxxxx	110b	Not Allowed	110b	Not Allowed	110b	Not Allowed	110b	Not Allowed	110b
7	7	1xxxxxxx	111b		111b		111b		111b		111b

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (= 00b).

MR24 DFE

Table 60: MR24 Register Information (MA[6:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DFES	DFEQU			RFU	DFEQL		

Table 61: MR24 Op-Code Bit Definitions

Feature	Type	OP	Data	Note
DFEQL (DFE quantity for lower byte)	W	OP[2:0]	000b: DFE disabled (default) 001b: Minimum negative feedback quantity 010b: Mid-range negative feedback quantity 011b: Maximum negative feedback quantity All others: Reserved	1, 2, 3
DFEQU (DFE quantity for upper byte)		OP[6:4]	000b: DFE disabled (default) 001b: Minimum negative feedback quantity 010b: Mid-range negative feedback quantity 011b: Maximum negative feedback quantity All others: Reserved	1, 2, 3
DFES (DFE support)	R	OP[7]	0b: DFE is not supported 1b: DFE is supported	

Notes:
1. DFE quantity is vender specific.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.

MR25 CA/CK TERM, PARC

Table 62: MR25 Register Information (MA[6:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Optimized refresh mode	PARC	CA BUS TERM	CK BUS TERM	RFU			

Table 63: MR25 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
CK BUS TERM (other shared die CK ODT information)	W	OP[4]	0b: All ranks sharing the CK pair are unterminated (default) 1b: One of the ranks sharing the CK pair is terminated	1, 2
CA BUS TERM (other shared die CA ODT information)		OP[5]	0b: All ranks sharing the CA Inputs are unterminated (default) 1b: One of the ranks sharing the CA inputs are terminated	1, 2
PARC (partial array refresh control)		OP[6]	0b: PARC disable (default) 1b: PARC enable	3
Optimized refresh mode		OP[7]	0b: Optimized refresh mode disabled 1b: Optimized refresh mode enabled (default)	4, 5

Notes:
1. MR25 OP[5]/[4] is set to notify the CA/CK ODT status of other shared dies.
2. When CK and CA ODT status are different (for example, CK is terminated and CA is unterminated) and MR25 OP[5] is disabled, the unterminated CA input buffer uses the fixed level reference voltage.
3. MR23 PASR segment mask is applied to the PARC operation if PARC is enabled.
4. When the device does not support Optimized Refresh mode (MR0 OP[3]=0b), MR25 OP[7] is don't care. In case of MR0 OP[3]=0b or MR25 OP[7]=0b, Refresh operation needs to follow the refresh requirement which is defined in Refresh Requirement section.
5. SoC which does not support the optimized refresh mode can use the device without changing MR OP[7] to 0b, if the SoC follows the Refresh Requirement.

MR26–MR42

MR26 DCM

Table 64: MR26 Register Information (MA[6:0] = 1Ah)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RDQSTFE	RDQSTFS	DCMU1	DCMU0	DCML1	DCML0	DCM Flip	DCM Start/Stop

Table 65: MR26 Op-Code Bit Definition

Feature	Type	OP	Data	
DCM Start/Stop	W	OP[0]	0b: Stop (default) 1b: Start	
DCM Flip (flip inputs to cancel offset)		OP[1]	0b: No flip (default) 1b: Flip	

Table 65: MR26 Op-Code Bit Definition (Continued)

Feature	Type	OP	Data	
DCML0 (duty cycle result for lower byte when DCM Flip = 0)	R	OP[2]	0b: High duty cycle <50% for lower byte 1b: High duty cycle ≥50% for lower byte	
DCML1 (duty cycle result for lower byte when DCM Flip = 1)		OP[3]	0b: High duty cycle <50% for lower byte 1b: High duty cycle ≥50% for lower byte	
DCMU0 (duty cycle result for upper byte when DCM Flip = 0)		OP[4]	0b: High duty cycle <50% for upper byte 1b: High duty cycle ≥50% for upper byte	
DCMU1 (duty cycle result for upper byte when DCM Flip = 1)		OP[5]	0b: High duty cycle <50% for upper byte 1b: High duty cycle ≥50% for upper byte	
RDQSTFS (read/write based WCK-RDQS_t TRAINING function support)		OP[6]	0b: Read/write-based WCK-RDQS_t TRAINING mode not supported 1b: Read/write-based WCK-RDQS_t TRAINING mode supported	
RDQSTFE (read/write based WCK-RDQS_t TRAINING function enable)	W	OP[7]	0b: Read/write-based WCK-RDQS_t TRAINING mode disabled (default) 1b: Read/write-based WCK-RDQS_t TRAINING mode enabled	1, 2

MR27 Refresh Management

Table 66: MR27 Register Information (MA[6:0] = 1Bh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RAAMULT		RAAIMT					RFM

Table 67: MR27 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
RFM Required	R	OP[0]	0b: RFM not required 1b: RFM required	1. 3
Rolling Accumulated ACT Initial Management Threshold (RAAIMT)		OP[5:1]	00000b: Invalid 00001b: 8 00010b: 16 - - - - (step +8) 11110b: 240 11111b: 248	1
Rolling Accumulated ACT Multiplier (RAAMULT)		OP[7:6]	00b: 2X 01b: 4X 10b: 6X 11b: 8X	1, 2

Notes:
1. Vendor programmed
2. RAAMMT = RAAMULT * RAAIMT
3. Specific attempts to by-pass the on-die circuitry designed to protect data integrity may result in data disturb.

MR28 ZQ

Table 68: MR28 Register Information (MA[6:0] = 1Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ZQ mode	RFU	ZQ Interval		ZQ Stop	ZQ Reset

Table 69: MR28 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
ZQ Reset	W	OP[0]	0b: Normal operation (default) 1b: ZQ reset	1, 2
ZQ Stop		OP[1]	0b: Normal operation (default) 1b: Background ZQ calibration is halted after ^{t}ZQSTOP	3, 4
ZQ Interval		OP[3:2]	00b: Background calibration Interval ≤32ms 01b: Background calibration Interval ≤64ms (default) 10b: Background calibration Interval ≤128ms 11b: Background calibration Interval ≤256ms	5
ZQ mode		OP[5]	0b: Background ZQ calibration (default) 1b: Command-based ZQ calibration	5

Notes:
1. See ZQCAL timing parameters for calibration latency and timing.
2. Asserting ZQ Reset sets the calibration values to their default setting.

3. When ZQ Stop is enabled, the ZQ resource is available for use by other devices.
4. In command-based calibration mode ZQCAL START commands are ignored when MR28 OP[1] = 1b.
5. ZQ Interval and ZQ mode MR settings are only applicable to ZQ master die. These settings are ignored by ZQ slave die.

MR29 PPR Resource

Table 70: MR29 Register Information (MA[6:0] = 1Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PPR resource bank 7	PPR resource bank 6	PPR resource bank 5	PPR resource bank 4	PPR resource bank 3	PPR resource bank 2	PPR resource bank 1	PPR resource bank 0

Table 71: MR29 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
PPR RESOURCE BANK 0	R	OP[0]	0b: PPR resource is not available 1b: PPR resource is available	1
PPR RESOURCE BANK 1		OP[1]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 2		OP[2]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 3		OP[3]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 4		OP[4]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 5		OP[5]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 6		OP[6]	0b: PPR resource is not available 1b: PPR resource is available	
PPR RESOURCE BANK 7		OP[7]	0b: PPR resource is not available 1b: PPR resource is available	

Note: 1. During the ACTIVATE command, the bank address is specified by CA[0:2] and is valid for a single PPR sequence. Valid combinations for 8B mode include CA[0:2] = 000b, 001b, 010b, 011b, 100b, 101b, 110b, and 111b. CA[3] is required to be valid (V). The BG/Bank address mapping on PPR is shown in the PPR Resource for CA Input table.

Table 72: PPR Resource

PPR Resource		MR29							
		OP[0]	OP[1]	OP[2]	OP[3]	OP[4]	OP[5]	OP[6]	OP[7]
8Bank	Bank	0	1	2	3	4	5	6	7
16Bank	Bank	0, 8	1, 9	2, 10	3, 11	4, 12	5, 13	6, 14	7, 15

Table 72: PPR Resource (Continued)

PPR Resource		MR29							
		OP[0]	OP[1]	OP[2]	OP[3]	OP[4]	OP[5]	OP[6]	OP[7]
BG	BG	0, 2	0, 2	0, 2	0, 2	1, 3	1, 3	1, 3	1, 3
	Bank	0	1	2	3	0	1	2	3

MR30 DCA

Table 73: MR30 Register Information (MA[6:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DCAU				DCAL			

Table 74: MR30 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
DCAL (duty cycle adjuster lower byte)	W	OP[3:0]	0000b: 0 step (default no adjustment) 0001b: –1step 0010b: –2 steps 0011b: –3 steps 0100b: –4 steps 0101b: –5 steps 0110b: –6 steps 0111b: –7 step	1, 3, 4, 5
			1000b: RFU	
			1001b: +1 step 1010b: +2 steps 1011b: +3 steps 1100b: +4 steps 1101b: +5 steps 1110b: +6 steps 1111b: +7 steps	2, 3, 4, 5
DCAU (duty cycle adjuster upper byte)		OP[7:4]	0000b: 0 step (default no adjustment) 0001b: –1 step 0010b: –2 steps 0011b: –3 steps 0100b: –4 steps 0101b: –5 steps 0110b: –6 steps 0111b: –7 steps	1, 3, 4, 5
			1000b: RFU	
			1001b: +1 step 1010b: +2 steps 1011b: +3 steps 1100b: +4 steps 1101b: +5 steps 1110b: +6 steps 1111b: +7 steps	2, 3, 4, 5

Notes:
1. The DCA reduces the internal WCK duty cycle in this range (0001b to 0111b).
2. The DCA increases the internal WCK duty cycle in this range (1000b to 1111b).
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
4. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16

OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.

5. With a byte-mode device, OP[3:0] applies to a lower-byte device and OP[7:4] applies to an upper-byte device. Unused operands (OP[7:4] for a lower-byte device and OP[3:0] for an upper-byte device) are valid (0b or 1b) and are ignored by the device.

MR31 – MR 34 DQ CAL

Table 75: MR31 Register Information (MA[6:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-byte per-bit invert control register for DQ calibration							

Table 76: MR31 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
Invert control register for DQ calibration (lower-byte per-bit)	W	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0b: Do not invert 1b: Invert the DQ calibration patterns in MR33 and MR34 Default value for OP[7:0] = 55h	1, 2, 3, 4

Notes:
1. This register inverts the DQ calibration pattern found in MR33 and MR34 for any single DQ or any combination of DQ's. For example, in the case of DQ inversion mode, if MR32 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[7,6,5,3,1] are not inverted, but the DQ calibration patterns transmitted on DQ[4, 2, 0] are inverted.
2. DMI[0] is not inverted and always transmits the true data contained in MR33/MR34.
3. No DATA BUS INVERSION (DBI) function is enacted during a READ DQ CALIBRATION operation, even if DBI is enabled in MR3 OP[6].
4. In the case of byte mode, MR31 is valid only for upper-byte selected device.

Table 77: MR32 Invert Register Pin Mapping

Pin	DQ0	DQ1	DQ2	DQ3	DMIO	DQ4	DQ5	DQ6	DQ7
MR31	OP[0]	OP[1]	OP[2]	OP[3]	NO-Invert	OP[4]	OP[5]	OP[6]	OP[7]

Table 78: MR32 Register Information (MA[6:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-byte per-bit invert control register for DQ calibration							

Table 79: MR32 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
Invert control register for DQ calibration (upper-byte per-bit)	W	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0b: Do not invert 1b: Invert the DQ calibration patterns in MR33 and MR34 (Default value for OP[7:0] = 55h)	1, 2, 3, 4

Notes:
1. This register inverts the DQ calibration pattern found in MR33 and MR34 for any single DQ or any combination of DQ's. For example, in the case of DQ inversion mode, if MR32 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[15, 14, 13, 11, 9] are not inverted, but the DQ calibration patterns transmitted on DQ[12, 10, 8] are inverted.
2. DMI[1] is not inverted and always transmits the true data contained in MR33/MR34.
3. No DATA BUS INVERSION (DBI) function is enacted during READ DQ CALIBRATION, even if DBI is enabled in MR3 OP[6].
4. In case of byte mode, MR32 is valid only for an upper-byte-selected device.

Table 80: MR32 Invert Register Pin Mapping

Pin	DQ0	DQ1	DQ2	DQ3	DMI1	DQ4	DQ5	DQ6	DQ7
MR32	OP[0]	OP[1]	OP[2]	OP[3]	NO-invert	OP[4]	OP[5]	OP[6]	OP[7]

Table 81: MR33 Register Information (MA[6:0] = 21h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern A							

Table 82: MR33 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
DQ calibration pattern MR33 + MR34	W	OP[7:0]	Xb: DQ calibration pattern A (default = 5Ah)	1, 2, 3, 4

Notes:
1. The READ DQ CALIBRATION command (RDC) causes the device to return the DQ calibration pattern contained in this register, followed by the contents of MR34. When RDC is initiated, the pattern contained in MR33 is transmitted on DQ[15:0] and DMI[1:0]. The big-endian pattern is transmitted serially on each data lane such that a byte's low-order bit is transmitted first. If the data pattern in MR33 is 27H, then the first bit transmitted is a 1, followed by 1, 1, 0, 0, 1, 0, 0. The bit stream will be 11100100b. A default pattern 5Ah is loaded at power-up or reset; otherwise, the pattern may be overwritten with an MRW command to this register. The contents of MR31 and MR32 will invert the data pattern for a given DQ (See MR31 for more information).
2. MR31 and MR32 can be used to invert the MR33/MR34 data patterns on the DQ pins. See MR31 and MR32 for more information. Data is never inverted on the DMI[1:0] pins.

3. When DBI-RD is disabled via MR3 OP[6], the data pattern is not transmitted on the DMI[1:0] pins.
4. No DATA BUS INVERSION (DBI) function is enacted during a read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 83: MR34 Register Information (MA[6:0] = 22h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern B							

Table 84: MR34 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
DQ calibration pattern MR33 + MR34	W	OP[7:0]	Xb: DQ calibration pattern B (default = 3Ch)	1, 2, 3, 4

Notes:
1. READ DQ CALIBRATION command (RDC) causes the device to return the DQ calibration pattern contained in MR33, followed by the contents of this register. When RDC is initiated, the pattern contained in MR34 is concatenated to the end of MR33 and transmitted on DQ[15:0] and DMI[1:0]. The big-endian pattern is transmitted serially on each data lane such that a byte's low-order bit is transmitted first. If the data pattern in MR33 is 27h , then the first bit transmitted is a 1, followed by 1, 1, 0, 0, 1, 0, 0. The bit stream will be 11100100b. A default pattern 3Ch is loaded at power-up or reset; otherwise the pattern may be overwritten with an MRW command to this register. See MR33 for more information.
2. MR31 and MR32 can be used to invert the MR33/MR34 data patterns on the DQ pins. See MR31 and MR32 for more information. Data is never inverted on the DMI[1:0] pins.
3. When DBI-RD is disabled via MR3 OP[6], the data pattern is not transmitted on the DMI[1:0] pins.
4. No DATA BUS INVERSION (DBI) function is enacted during a read DQ calibration, even if DBI is enabled in MR3 OP[6].

MR35, MR36 WCK2DQI Oscillator Count

Table 85: MR35 Register Information (MA[6:0] = 23h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQI oscillator count – LSB							

Table 86: MR35 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
WCK2DQI oscillator count (DQ input training WCK oscillator)	R	OP[7:0]	0–255 LSB device WCK2DQI oscillatory count	1, 2, 3, 4

Notes:
1. MR35 reports the LSB bits of the device WCK2DQI oscillator count. The device WCK2DQI oscillator count value is used to train WCK to the DQ data valid window. The value re-

ported by the device in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.
2. Both MR35 and MR36 must be read by the MRR command and combined to get the value of the WCK2DQI oscillator count.
3. A new MPC[START WCK2DQI OSCILLATOR] command could be issued to reset the contents of MR35/MR36.
4. WCK2DQI and WCK2DQO commands cannot be operated simultaneously.

Table 87: MR36 Register Information (MA[6:0] = 24h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQI oscillator count – MSB							

Table 88: MR36 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
WCK2DQI oscillator count (DQ input training WCK oscillator)	R	OP[7:0]	0–255 MSB device WCK2DQI oscillatory count	1, 2, 3, 4

Notes:
1. MR36 reports the MSB bits of the device WCK2DQI oscillator count. The device WCK2DQI oscillator count value is used to train WCK to the DQ data valid window. The value reported by the device in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.
2. Both MR35 and MR36 must be read by the MRR command and combined to get the value of the WCK2DQI oscillator count.
3. A new MPC[START WCK2DQI OSCILLATOR] can be issued to reset the contents of MR35/MR36.
4. WCK2DQI and WCK2DQO cannot be operated simultaneously.

MR37 WCK2DQI Interval Timer Run Time Setting

Table 89: MR37 Register Information (MA[6:0] = 25h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQI interval timer run time setting							

Table 90: MR37 Op-Code Bit Definition

Feature	Type	OP	Data
WCK2DQI interval timer run time setting	R/W	OP[7:0]	00000000b: WCK2DQI interval timer stop via MPC command (default) 00000001b: WCK2DQI timer stops automatically at 16th clocks after timer start 00000010b: WCK2DQI timer stops automatically at 32nd clocks after timer start 00000011b: WCK2DQI timer stops automatically at 48th clocks after timer start 00000100b: WCK2DQI timer stops automatically at 64th clocks after timer start ⋮ 00111111b: WCK2DQI timer stops automatically at (63X16)th clocks after timer start 01xxxxxxb: WCK2DQI timer stops automatically at 2048th clocks after timer start 10xxxxxxb: WCK2DQI timer stops automatically at 4096th clocks after timer start 11xxxxxxb: WCK2DQI timer stops automatically at 8192nd clocks after timer start

Notes:
1. The MPC command with OP[6:0] = 10000010b, (STOP WCK2DQI INTERVAL OSCILLATOR) stops WCK2DQI interval timer in case of MR37 OP[7:0] = 00000000b.
2. The MPC command with OP[6:0] = 10000010b, (STOP WCK2DQI INTERVAL OSCILLATOR) is illegal with non-zero values in MR37 OP[7:0].

MR38, MR39 WCK2DQO Oscillator Count

Table 91: MR38 Register Information (MA[6:0] = 26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQO oscillator count – LSB							

Table 92: MR38 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
WCK2DQO oscillator count (DQ output training WCK oscillator)	R	OP[7:0]	0–255 LSB device WCK2DQO oscillator count	1, 2, 3

Notes:
1. MR38 reports the LSB bits of the device WCK2DQO oscillator count. The device WCK2DQO oscillator count value is used to train WCK to the DQ data valid window. The value reported by the device in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.

2. Both MR38 and MR39 must be read by the MRR command and combined to get the value of the WCK2DQO oscillator count.
3. A new MPC[START WCK2DQO OSCILLATOR] can be issued at any time before sending MPC[STOP WCK2DQO OSCILLATOR]. A new MPC[START WCK2DQO OSCILLATOR] resets the contents of MR38/MR39.

Table 93: MR39 Register Information (MA[6:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQO oscillator count – MSB							

Table 94: MR39 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
WCK2DQO oscillator count (DQ output training WCK oscillator)	R	OP[7:0]	0–255 MSB device WCK2DQO oscillator count	1, 2, 3

Notes:
1. MR39 reports the MSB bits of the device WCK2DQO oscillator count. The device WCK2DQO oscillator count value is used to train WCK to the DQ data valid window. The value reported by the device in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.
2. Both MR38 and MR39 must be read by the MRR command and combined to get the value of the WCK2DQO oscillator count.
3. AA new MPC[START WCK2DQO OSCILLATOR] can be issued at any time before sending MPC[STOP WCK2DQO OSCILLATOR]. A new MPC[START WCK2DQO OSCILLATOR] resets the contents of MR38/MR39.

MR40 WCK2DQO Interval Timer Run-Time Setting

Table 95: MR40 Register Information (MA[6:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WCK2DQO interval timer run-time setting							

Table 96: MR40 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
WCK2DQO interval timer run-time setting	R/W	OP[7:0]	00000000b: WCK2DQO interval timer stop via MPC command (default) 00000001b: WCK2DQO timer stops automatically at 16th clocks after timer start 00000010b: WCK2DQO timer stops automatically at 32nd clocks after timer start 00000011b: WCK2DQO timer stops automatically at 48th clocks after timer start 00000100b: WCK2DQO timer stops automatically at 64th clocks after timer start ⋮ 00111111b: WCK2DQO timer stops automatically at (63X16)th clocks after timer start 01XXXXXXXb: WCK2DQO timer stops automatically at 2048th clocks after timer start 10XXXXXXb: WCK2DQO timer stops automatically at 4096th clocks after timer start 11XXXXXXb: WCK2DQO timer stops automatically at 8192nd clocks after timer start	1, 2

Notes:
1. The MPC command with OP[7:0] = 10000100b, (STOP WCK2DQO INTERVAL OSCILLATOR) stops WCK2DQO interval timer in case of MR40 OP[7:0] = 00000000b.
2. The MPC command with OP[7:0] = 10000100b, (STOP WCK2DQO INTERVAL OSCILLATOR) is illegal with non-zero values in MR40 OP[7:0].

MR41 PPRE and NT DQ ODT

Table 97: MR41 Register Information (MA[6:0] = 29h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
NT DQ ODT			PPRE	RFU			

Table 98: MR41 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
PPRE (post package repair enable)	W	OP[4]	0b: PPR disable (default) 1b: PPR enable	
NT DQ ODT (non-target DQ bus receiver on-die termination)		OP[7:5]	000b: Disable 001b: RZQ/1 010b RZQ/2 011b: RZQ/3 (default) 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3, 4

Notes:
1. All values are typical. The actual value after calibration is within the specified tolerance for a given voltage and temperature. Recalibration might be required as voltage and temperature vary.
2. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. Only registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) are written with an MRW command to this MR address.
3. Three physical registers are assigned to each MR parameter bit, designated as set points 0, 1, and 2. The device operates only according to the values stored in registers for the active set point, such as the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). Values in registers for the inactive set point are ignored by the device and can be changed without affecting device operation.
4. The non-target device ODT function is enabled by MR11 OP[3] = 1b and its ODT value is set by MR41 OP[7:5].

MR42 PPR Key Protection

Table 99: MR42 Register Information (MA[6:0] = 2Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PPR key protection							

Table 100: MR42 Op-Code Bit Definition

Function	Type	OP	Data	Notes
PPR key protection	W	OP[7:0]	PPR protection code	1

Note:
1. PPR entry and exit sequence details are described in the Post Package Repair section.

MR43–MR127

MR43–MR45 Link ECC Information

Table 101: MR43 Register Information (MA[6:0] = 2Bh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBE Flag	SBEC Rule	SBE Count					

Table 102: MR43 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
SBE Count	R	OP[5:0]	The number of times single-bit errors have been seen on the DRAM interface	1, 2, 3, 4, 5
SBEC Rule		OP[6]	0b: Simultaneous SBE on each DQ byte and DMI are counted as one error 1b: Simultaneous SBE on each DQ byte and DMI are independently counted	3
DBE Flag		OP[7]	0b: No double-bit errors seen on the DRAM interface 1b: One or more double-bit errors seen on the DRAM interface	1, 2, 4, 6

Notes:
1. These bits are cleared when the following occur: on power-up, DRAM reset, any power-down exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4] = 00b (Link ECC disabled). Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be ^{t}MRR + ^{t}MRW (rather than simply ^{t}MRR as required on most registers).
2. The DRAM disables detection and recording of Link ECC errors during WRITE-FIFO commands because these commands are used for training purposes, during which some errors are expected.
3. In x16 mode, up to four single-bit errors could potentially be detected in a single BL16 burst (byte 0 data SBE, byte 0 DMI SBE, byte 1 data SBE, and byte 1 DMI SBE). SBEC rule 0b: Any combination of these four simultaneous errors is considered a single SBE occurrence, and would only increment the SBE count by 1. A BL32 burst can have up to three such SBE occurrences, and could increment the SBE count by up to two. In x8 device, any simultaneous combination of data SBE and DMI SBE is considered a single SBE occurrence, and would only increment the SBE count by one (up to two in a BL32 burst). SBEC rule 1b: Each of the maximum four simultaneous errors is considered an independent error and would increment the SBE count up to four. A BL32 burst can have up to eight such SBE occurrences, and could increment the SBE count by up to eight. In x8 device, any simultaneous combination of data SBE and DMI SBE is considered a independent SBE occurrence, and would only increment the SBE count by up to two (up to four in a BL32 burst).
4. In x16 mode, errors from either interface byte are stored in a single register per DRAM (SBE count is the number of SBE occurrences on both bytes, and the DBE flag indicates a DBE on either byte). In x8 mode, errors are stored for a single interface byte, and MRR returns both copies of this register, each on its corresponding byte lane.
5. SBE count should be a saturating counter.
6. When set, the DBE flag bit remains set until explicitly cleared by one of the conditions described in note 1 above.

Table 103: MR44 Register Information (MA[6:0] = 2Ch)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Data ECC Syndrome[7:0]							
S[7]	S[6]	S[5]	S[4]	S[3]	S[2]	S[1]	S[0]

Table 104: MR44 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Data ECC syndrome[7:0]	R	OP[7:0]	Bits 7:0 of the data ECC syndrome from the most recent single-bit error	1, 2, 3, 4, 5, 6

Notes:
1. These bits are cleared when the following occur: on power-up, DRAM reset, any power-down exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4] = 00b (Link ECC disabled). Because time is required for the device to perform the clear on reads, the delay after reading this mode register should be ^{t}MRR + ^{t}MRW. (rather than simply ^{t}MRR as required on most registers)
2. The DRAM disables detection and recording of Link ECC errors during WRITE-FIFO commands because these commands are used for training purposes, during which some errors are expected.
3. In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte, and MRR returns both copies of this register, each on its corresponding byte lane.
4. In x16 mode, it is possible for errors to occur on both bytes simultaneously. In this rare case, only the syndrome from DQ[7:0] is stored.
5. Regardless of the detection of a data ECC error or an DMI ECC error, both syndromes are stored at either error occurrence.
6. The error syndrome is not affected by a DBE and retains its previous value.

Table 105: MR45 Register Information (MA[6:0] = 2Dh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Data ECC syndrome[8]	Error byte lane	DMI ECC syndrome					
		DS[5]	DS[4]	DS[3]	DS[2]	DS[1]	DS[0]

Table 106: MR45 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
DMI ECC syndrome	R	OP[5:0]	The DMI ECC syndrome from the most recent single-bit error	1, 2, 3, 4, 5, 7
Error byte lane		OP[6]	0b: The most recent single-bit error occurred on DQ[7:0] or DMI0 1b: The most recent single-bit error occurred on DQ[15:8] or DMI1	1, 2, 3, 4, 5, 6, 8
Data ECC syndrome[8]		OP[7]	Bit 8 of the data ECC syndrome from the most recent single-bit error	1, 2, 3, 4, 5, 7

Notes:
1. These bits are cleared when the following occur: on power-up, DRAM reset, any POWER-DOWN EXIT, and on each read of this mode register.
2. The DRAM disables detection and recording of Link ECC errors during WRITE-FIFO commands because these commands are used for training purposes, during which some errors are expected.
3. In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte, and MRR returns both copies of this register, each on its corresponding byte lane.
4. In x16 mode, it is possible for errors to occur on both bytes simultaneously. In this rare case, only the error syndromes from byte 0 (DQ[7:0] and DMI0) should be stored, regardless of the error types on the two bytes.
5. Regardless of the detection of a data ECC error or an ECC DMI error, both syndromes shall be stored at either error occurrence.
6. In x8 mode, this bit is unused and is always read as 0.
7. These syndrome fields are not affected by a DBE and retain their previous values.
8. The error byte lane is only updated by an SBE.

The following table is provided to help clarify when and how each field is updated.

Table 107: Updating ECC Syndromes and Error Byte Lane

Errors at Byte 0	Errors at Byte 1	Syndromes (MR44 and MR45 OP[7] and OP[5:0])	Error Byte Lane (MR45 OP[6])
None	None	No change	No change
SBE	None	Byte 0	Byte 0
DBE	None	No change	No change
None	SBE	Bye 1	Bye 1
SBE	SBE	Byte 0	Byte 0
DBE	SBE	Byte 1	Byte 1
None	DBE	No change	No change
SBE	DBE	Byte 0	Byte 0
DBE	DBE	No change	No change

MR46 Training Features

Table 108: MR46 Register Information (MA[6:0] = 2Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					FIFO RDQS training	RDQS toggle	Enhanced RDQS

Table 109: MR46 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Enhanced RDQS (enhanced RDQS training mode)	W	OP[0]	0b: Disabled (default) 1b: Enhanced RDQS training mode enabled	
RDQS toggle (RDQS toggle mode)		OP[1]	0b: Disabled (default) 1b: Enhanced RDQS toggle mode enabled	
FIFO RDQS training (WCK-RDQS_t/parity training)		OP[2]	0b: Disabled (default) 1b: WCK-RDQS_t/parity training enabled	1

Note: 1. When MR46 OP[2] = 1b, the WRITE-FIFO command enables data to be written through the RDQS_t pin. The data written via the RDQS_t pin can then be read back via the DMI by a READ-FIFO command.

MR47–MR54 Serial ID

Table 110: MR47 Register Information (MA[6:0] = 2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-1							

Table 111: MR47 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-1	R	OP[7:0]	Serial ID-1	1

Note: 1. MR47 is vendor-specific.

Table 112: MR48 Register Information (MA[6:0] = 30h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-2							

Table 113: MR48 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-2	R	OP[7:0]	Serial ID-2	1

Note: 1. R48 is vendor-specific.

Table 114: MR49 Register Information (MA[6:0] = 31h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-3							

Table 115: MR49 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-3	R	OP[7:0]	Serial ID-3	1

Note: 1. MR49 is vendor-specific.

Table 116: MR50 Register Information (MA[6:0] = 32h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-4							

Table 117: MR50 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-4	R	OP[7:0]	Serial ID-4	1

Note: 1. MR50 is vendor-specific.

Table 118: MR51 Register Information (MA[6:0] = 33h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-5							

Table 119: MR51 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-5	R	OP[7:0]	Serial ID-5	1

Note: 1. MR51 is vendor-specific.

Table 120: MR52 Register Information (MA[6:0] = 34h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-6							

Table 121: MR52 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-6	R	OP[7:0]	Serial ID-6	1

Note: 1. MR52 is vendor-specific.

Table 122: MR53 Register Information (MA[6:0] = 35h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-7							

Table 123: MR53 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-7	R	OP[7:0]	Serial ID-7	1

Note: 1. MR53 is vendor-specific.

Table 124: MR54 Register Information (MA[6:0] = 36h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial ID-8							

Table 125: MR54 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Serial ID-8	R	OP[7:0]	Serial ID-8	1

Note: 1. MR54 is vendor-specific.

MR57 Refresh Management

Table 126: MR57 Register Information (MA[6:0] = 39h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RFMSBC		RFMSB		RAADEC	

Table 127: MR57 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
RAA count decrement per RFM command (RAADEC)	R	OP[1:0]	00b: RAAIMT 01b: RAAIMT * 1.5 10b: RAAIMT * 2 11b: RAAIMT * 4	
RFM allowable single banks (RFMSB)		OP[3:2]	00b: 1= Does not support single-bank mode 01b: 2 = Supports single-bank mode 10b: RFU 11b: RFU	1, 2
RFM single-bank counters implemented (RFMSBC)	W	OP[5:4]	00b: 1 = One RAA counter per two banks (1 of 8)(default) 01b: 2 = One RAA counter per one bank (1 of 16) 10b: RFU 11b: RFU	

Notes:
1. If MR57 OP[3:2] = 00b, it is not allowed to set MR57 OP[5:4] = 01b
2. MR57 OP[5:4] = 01b is not supported for 8B mode.

MR58 Pre Emphasis

Table 128: MR58 Register Information (MA[6:0] = 3Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Dn Emphasis Upper		Up Emphasis Upper		Dn Emphasis Lower		Up Emphasis Lower	

Table 129: MR58 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Up Emphasis Lower (output pin pull-up pre-emphasis lower byte)	W	OP[1:0]	00b: Pull-up pre-emphasis disabled (default) 01b: Pull-up pre-emphasis enabled: Weak 10b: Pull-up pre-emphasis enabled: Middle 11b: Pull-up pre-emphasis enabled: Strong	1, 2, 3, 4, 5, 6
Dn Emphasis Lower (output pin pull-down pre-emphasis lower byte)		OP[3:2]	00b: Pull-down pre-emphasis disabled (default) 01b: Pull-down pre-emphasis enabled: Weak 10b: Pull-down pre-emphasis enabled: Middle 11b: Pull-down pre-emphasis enabled: Strong	1, 2, 3, 4, 5, 6
Up Emphasis Upper (output pin pull-up pre-emphasis upper byte)		OP[5:4]	00b: Pull-up pre-emphasis disabled (default) 01b: Pull-up pre-emphasis enabled: Weak 10b: Pull-up pre-emphasis enabled: Middle 11b: Pull-up pre-emphasis enabled: Strong	1, 2, 3, 4, 5, 6
Dn Emphasis Upper (output pin pull-down pre-emphasis upper byte)		OP[7:6]	00b: Pull-down pre-emphasis disabled (default) 01b: Pull-down pre-emphasis enabled: Weak 10b: Pull-down pre-emphasis enabled: Middle 11b: Pull-down pre-emphasis enabled: Strong	1, 2, 3, 4, 5, 6

Notes:
1. Output pins are DQ, RDQS_t (parity), RDQS_c and DMI
2. There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.
3. There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. Active MR bit which is selected by FSP-OP: MR16 OP[3:2] cannot be changed directly by MRW command except per the reset and initialization procedure.
5. Each MR bit can be enabled only by FSP procedure.
6. The Pre Emphasis applies more than 6400 Mb/s.

MR56,MR60 Reserved for testing purpose

Table 130: MR56 Register Information (MA[6:0] = 38h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 131: MR56 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Device will ignore	W	OP[7:0]	Don't care	1

Note: 1. This register is reserved for testing purpose. The logical data values written to OP[7:0] shall have no effect on device operation, however timings need to be observed as for any other MR access command.

Table 132: MR60 Register Information (MA[6:0] = 3Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 133: MR60 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
Device will ignore	W	OP[7:0]	Don't care	1

Note: 1. This register is reserved for testing purpose. The logical data values written to OP[7:0] shall have no effect on device operation, however timings need to be observed as for any other MR access command.

MR55,59,61-63,64-127 RFU

Table 134: MR55,58-59,61-63,64-127 Register Information (MA[6:0] = 37h,40h-41h,3Dh-3Fh,40h-7Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Revision History

Rev. F– 02/2021

- Note 6 update for MR0 Op-Code Bit Definitions
- Note 4 update for VREF DQ[7:0] Settings
- Note 4 update for VREF DQ[15:8] Settings

Rev. E– 12/2020

- Mode Register Assignments and Definitions table update
- MR0 OP[6] update
- MR1 OP[7:4] Op-Code Bit Definitions Table update
- MR2 Op-Code Bit Definitions Table update
- MR8 OP[1:0] update
- Note for MR13 Op-Code Bit Definitions table updated. Notes for VREF DQ[7:0] / DQ[15:8] Settings updated
- MR25 typo correction: PAAR --> PARC
- MR26 typo correction: Read/write-based TRAINING --> Read/write-based WCK-RDQS_t TRAINING
- MR27 Op-Code Bit Definition Table update
- MR29 PPR Resource table update
- MR57 Refresh Management table update
- Added MR58 Op-Code Bit Definitions Table

Rev. D– 04/2020

- Changed MR26 OP[5:2] description
- Added Note 3 to MR27
- Typo correction for MR37 Note 1,2
- MR45 OP6 description update
- Added table: Updating ECC Syndromes and Error Byte Lane
- MR57 OP[3:2],OP[5:4] value update

Rev. C – 02/2020

- Added description for MR0 OP2 Enhanced WCK Always On mode,OP3 Optimized Refresh mode, OP3 DMI Output behavior mode,OP4 Unified NT ODT behavior
- MR17 notes updated
- Added description for MR19 OP[3:2] DVFSQ
- Added MR57 RFM,MR56/60 reserved for test
- Added description for MR25 OP7 Optimized refresh mode
- Updated legal status to Production

Rev. B – 04/2019

- MR0 OP0 NT ODT timing mode added
- MR17 notes updated
- MR18,MR19,MR27 update

- added MR57 RFM,MR56/60 reserved for test

Rev. A – 01/2019

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.