Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

LBA-NAND Flash
Palladium Memory Model
User Guide

9

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

LBA-NAND Flash Palladium Memory Models

1. Introduction

The Cadence Palladium LBA-NAND Flash Models are based on data sheet Rev. 0.97 dated 2007-11-29 of the following Toshiba devices:

mobileLBA-NAND Flash memory

Please note that Rev. 0.97 of the data sheet does not specify part numbers for these devices. The generic model numbers listed below are based on density, bus width, and the optional power-on mode or nand access mode of the boot block. Model names ending with a ‘p’ denotes power-on mode. Model names ending with an ‘s’ denotes standard or lba access mode only models. In lba (Logical Block Address) access mode the data transfer unit is a sector, which is 528 bytes or 264 words for x16 devices. In nand access mode the page size is 2112 bytes or 1056 words for x16 devices, and it is only for accessing the optional boot block. These devices’ unique feature is that the user can adjust the size of the SLC and MLC data areas (SDA and MDA) by setting the size of SDA. One sector of SDA space reduces MDA space by two sectors. For maximum capacity set SDA to zero. The optional boot block is 4096 sectors or 2MB in SDA.

The models are available in several configurations with model sizes to match real devices manufactured by the following vendor: Toshiba.

Currently only a few different sizes are available, please consult the memory model catalog for the current available list.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

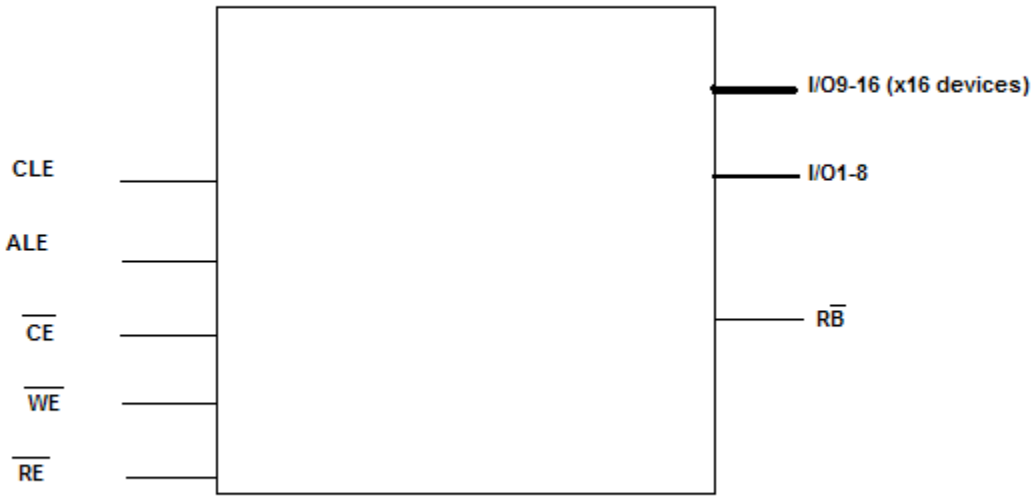
3. Configurations

The following table lists the configurations specified in the data sheet listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Model number	Density	I/O Bus Width	Boot block sectors	Max # of SDA sectors	Max # of MDA sectors @SDA=0	Access Modes
mlba32g16p	**32Gb**	**16**	**4096**	**2093056**	**7954432**	**NAND, LBA**
mlba32g8p	**32Gb**	**8**	**4096**	**2093056**	**7954432**	**NAND, LBA**
mlba32g16s	**32Gb**	**16**	**0**	**2097152**	**7962624**	**LBA only**
mlba32g8s	**32Gb**	**8**	**0**	**2091752**	**7962624**	**LBA only**
mlba16g16p	**16Gb**	**16**	**4096**	**1964032**	**3928064**	**NAND, LBA**
mlba16g8p	**16Gb**	**8**	**4096**	**1964032**	**3928064**	**NAND, LBA**
mlba16g16s	**16Gb**	**16**	**0**	**1968128**	**3936256**	**LBA only**
mlba16g8s	**16Gb**	**8**	**0**	**1968128**	**3936256**	**LBA only**
mlba08g16p	**8Gb**	**16**	**4096**	**977920**	**1955840**	**NAND, LBA**
mlba08g8p	**8Gb**	**8**	**4096**	**977920**	**1955840**	**NAND, LBA**
mlba08g16s	**8Gb**	**16**	**0**	**982016**	**1964032**	**LBA only**
mlba08g8s	**8Gb**	**8**	**0**	**982016**	**1964032**	**LBA only**
mlba04g16p	**4Gb**	**16**	**4096**	**484864**	**969728**	**NAND, LBA**
mlba04g8p	**4Gb**	**8**	**4096**	**484864**	**969728**	**NAND, LBA**
mlba04g16s	**4Gb**	**16**	**0**	**488960**	**977920**	**LBA only**
mlba04g8s	**4Gb**	**8**	**0**	**488960**	**977920**	**LBA only**
mlba02g16p	**2Gb**	**16**	**4096**	**232960**	**465920**	**NAND, LBA**
mlba02g8p	**2Gb**	**8**	**4096**	**232960**	**465920**	**NAND, LBA**
mlba02g16s	**2Gb**	**16**	**0**	**237056**	**474112**	**LBA only**
mlba02g8s	**2Gb**	**8**	**0**	**237056**	**474112**	**LBA only**

Suffix: p = optional power-on mode model
s = standard model

4. Model Logic Diagram



5. Address Mapping

The array of the LBA-NAND Flash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. In NAND mode the mapping of column and page addresses to the internal model array is as follows:

ARRAY_ADDR = page address * 2112 + column address

In LBA mode:

ARRAY_ADDR = sector address * 528

The minimum sector address for MDA is 200000h. The minimum sector address for SDA is 0 for standard models and 1000h for models with optional power-on mode. The optional boot block starts at 0. The maximum SDA size is 2097152 sectors which includes the optional boot block of 4096 sectors. One sector of SDA reduces MDA by two sectors.

6. Spare Data Area

The Data sheet lists three formats for outputting data from the spare area:

Type a: Smart Media Format
Type b: ECC Pass or Error
Type c: All 1 Read (except the extended 4 Bytes)

Currently the models do not support these formats. Also ECC data is not generated or checked for pass or fail.

The user may use any 4 of the 16 spare area bytes as the extended 4 Bytes. However the model does not check if the correct 4 bytes were previously selected using the Set_Transfer_Protocol_2 command.

7. ID Operation

7.1. ID Read

The Manufacturer and Device codes have been hardcoded into each model. Therefore user data file is not required.

7.2. Read CFI Query

The LBA-NAND flash devices do not support the Common Flash Interface.

8. Commands

The LBA-NAND flash model accepts the following commands. However Set_Transfer_Protocol_1 and Set_Transfer_Protocol_2 are not fully supported as explained in Section 5 concerning the spare data area.

- Read: SDA or Boot Code Block
- Read: MDA
- Program: SDA or Boot Code Block
- Program: MDA
- Continuance Command for Type B Read
- Continuance Command for Type B Write
- Set_SDA_Unit
- Get_SDA_Unit
- Get_MDA_Unit
- Set_Transfer_Protocol_1
- Get_Transfer_Protocol_1
- Set_Transfer_Protocol_2
- Get_Transfer_Protocol_2
- Set_Minimum_Busy_Time
- Get_Minimum_Busy_Time
- Program Protect
- ID Read
- Safety Power Down
- Status Read (Normal)
- Status Read (Optional read for mobileLBA)
- Terminate Read&Write / Sequence Clear (LBA mode)
- NOP (Block Erase command during LBA mode)
- Block Erase (NAND mode)
- NOP in Standard device <FFh>
- Terminate Read&Write / Sequence Clear in Optional Power-On device
- Reset
- Emergency Command

Status register read during program and erase operations is supported. The R/B# pin can be monitored for Ready/Busy status.

9. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compilation. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64 +sv -ua +dut+<model_name> \
    ./<model_name>.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……
```

```
xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis:

```
1)
hdlInputFile <model_name>.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog <model_name>.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
<model_name>
……

2)
vavlog <model_name>.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog <model_name>.vg
<model_name>
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations which are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

10. Initialization Sequence

The LBA-NAND Flash model does not require a special initialization sequence. When R/B# is high the model is ready for normal operation.

11. Model Size

To reduce memory utilization each device supports only 128MB or 256K sectors (which is 64MB or 128K sectors if all were partitioned to SDA). If larger size is needed please contact Customer Support.

12. Limitations

1. Spare data area output formats and ECC generation and detection are not supported.
2. Model does not check illegal sequence of command cycles.
3. Model does not check for attempts to program a bit to 1, user should make sure the block is erased before program.

13. Revision History

The following table shows the revision history for this document

Date	Version	Revision
December 2010	1.0	Initial release
June 2011	1.1	Added “Related Docs” Info
July 2014	1.2	Repaired doc property title. Updated legal. Added revision history.
September 2014	1.3	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.4	Remove emulation capacity info. Update related publications list.
July 2015	1.5	Update Cadence naming on front page
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming
January 2018	1.8	Modify header and footer
July 2018	1.9	Update for new utility library