



# Technical Note

## LPDDR4/LPDDR4X Point-to-Point, Non-PoP, Design Guidelines

### Introduction

LPDDR4 SDRAM products require a well-designed system board environment to reliably support high-speed/low-power applications.

Proven layout and routing techniques are required for embedded and mobile designs using point-to-point DRAM interfaces in side-by-side (non-PoP) configurations. Derived from transmission line theory and Micron design experience, the guidelines presented in this technical note can enhance signal integrity (SI) and reduce noise for point-to-point (as well as point-to-multipoint) designs.

The guidelines and examples in this technical note represent one of several acceptable methods and may not be applicable for all designs.

For more information, refer to these additional Micron technical notes that also focus on point-to-point SDRAM design, layout and simulation techniques:

- TN-52-02: Point-to-Point System Design: Layout and Routing Tips for LPDDR2 and LPDDR3 Devices
- TN-41-13: DDR3 Point-to-Point Design Support

**Table 1: Definitions**

Term	Definition
DDP	Dual-die package
Power delivery	Power and ground layout and decoupling techniques used to improve signal integrity
SDP	Single-die package
SSO	Simultaneous switching outputs
$V_{DDQ}$	DQ and I/O signal power; the two are equivalent unless otherwise noted
$V_{DD}$	Digital power for the device core
$V_{REFDQ}$	Reference for DQ input buffers
$V_{SS}$	Digital ground
$V_{SSQ}$	DQ and signal ground; the two are equivalent unless otherwise noted



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines LPDDR4-to-LPDDR3 Comparison

### LPDDR4-to-LPDDR3 Comparison

Substantial architecture differences exist between LPDDR4 and LPDDR3 technologies. Both LPDDR4 and LPDDR3 products support a source-synchronous data strobe where data is transferred on both the leading and trailing strobe edges.

When designing a point-to-point memory system, the major differences to be aware of between LPDDR4 and LPDDR3 products are:

- LPDDR4 products increase in bandwidth from 1866 MT/s to 3733 MT/s and beyond using newer LVSTL signaling techniques
- LPDDR4 products are configured as one or more x16 channels

The following table provides a highlighted comparison of the devices.

**Table 2: Key Feature Comparison**

Feature	LPDDR4	LPDDR3
Density	Up to 32Gb	Up to 32Gb
Prefetch size	16n (512-bit total)	8n (256-bit total)
Core voltage ( $V_{DD}$ )	1.1V	1.2V
	1.8V	1.8V
I/O voltage	1.1V or 0.6V	1.2V
Maximum clock frequency/data rate	2133 MHz/DDR4266	800 MHz/DDR1600; 933 MHz/DDR1866
Burst lengths	16, 32	8
Configurations	2 channel x16 per die, 1 channel x16 per die	x16, x32
Address command signals	CA[5:0]	14 pins (multiplexed command and address)
Address/command data rate	SDR (rising clock edge only)	DDR (rising and falling clock edge)
PASR	Full-, half- or quarter-array with individual bank and segment masking for partial bank modes	Individual bank and segment masking for partial bank modes
Drive strength	RZQ/6	34 ohm
	RZQ/5	40 ohm
	RZQ/4	48 ohm
	RZQ/3	–
	RZQ/2	–
	RZQ/1	–
	ZQ calibration for $\pm$ xx% accuracy (TBD)	ZQ calibration for $\pm$ 10% accuracy
Per bank refresh	Yes	Yes
Output driver	LVSTL, $V_{SSQ}$ terminated	HSUL_12
DPD	No	Yes
DLL/ODT	No/Yes (ODT on DQ, DQS, DM and CA)	No/Yes (ODT on DQ, DQS, DM)
Package options	POP, MCP, discrete	POP, MCP, discrete

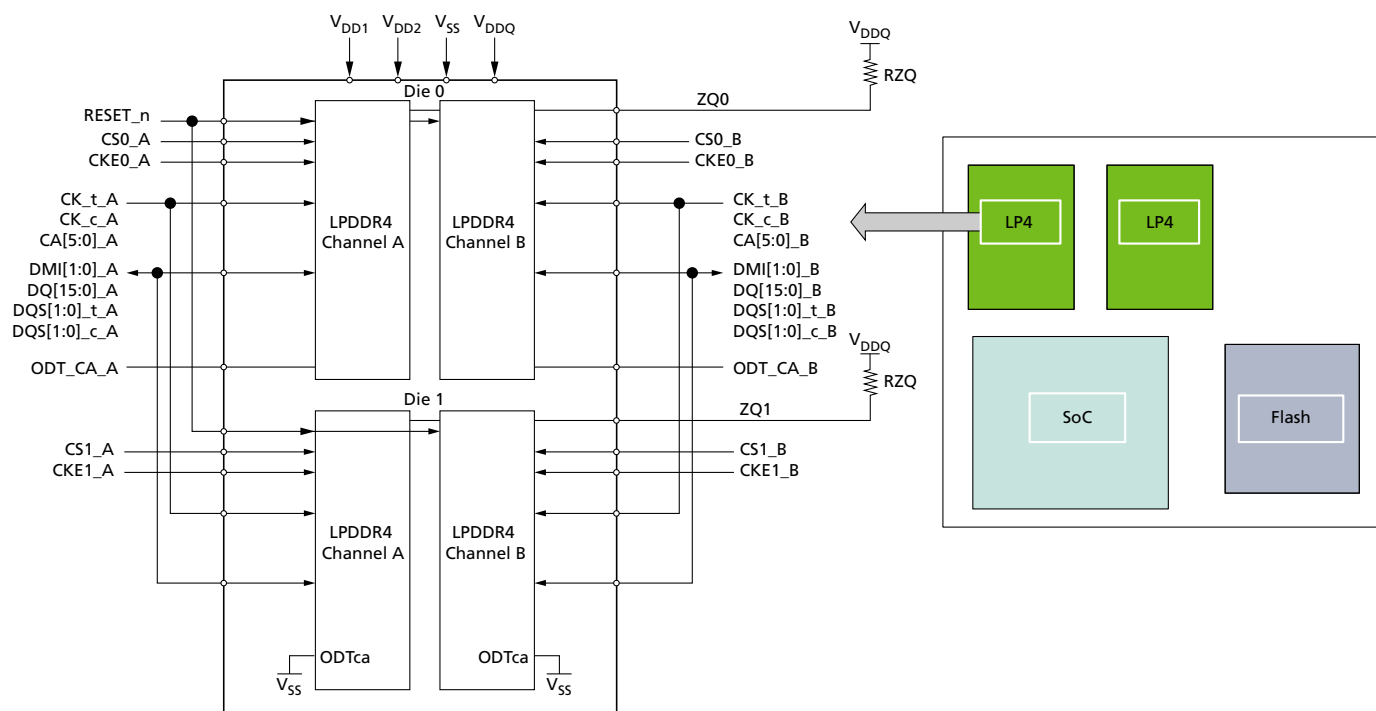


## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines LPDDR4 Block Diagrams

### LPDDR4 Block Diagrams

The following block diagrams illustrate the basic data bus topology used for the simulation examples presented in this guide. The guidelines derived from these simulations on the DDR data bus can then easily be applied to the SDR command/address (CA) bus. Only one of the two 2GB DDP LPDDR4 components is simulated; the other 2GB component will be the same. Also, only the READ cycle is simulated. The WRITE cycle should have similar values, assuming that the memory controller data bus drivers are well matched to the DRAM drivers.

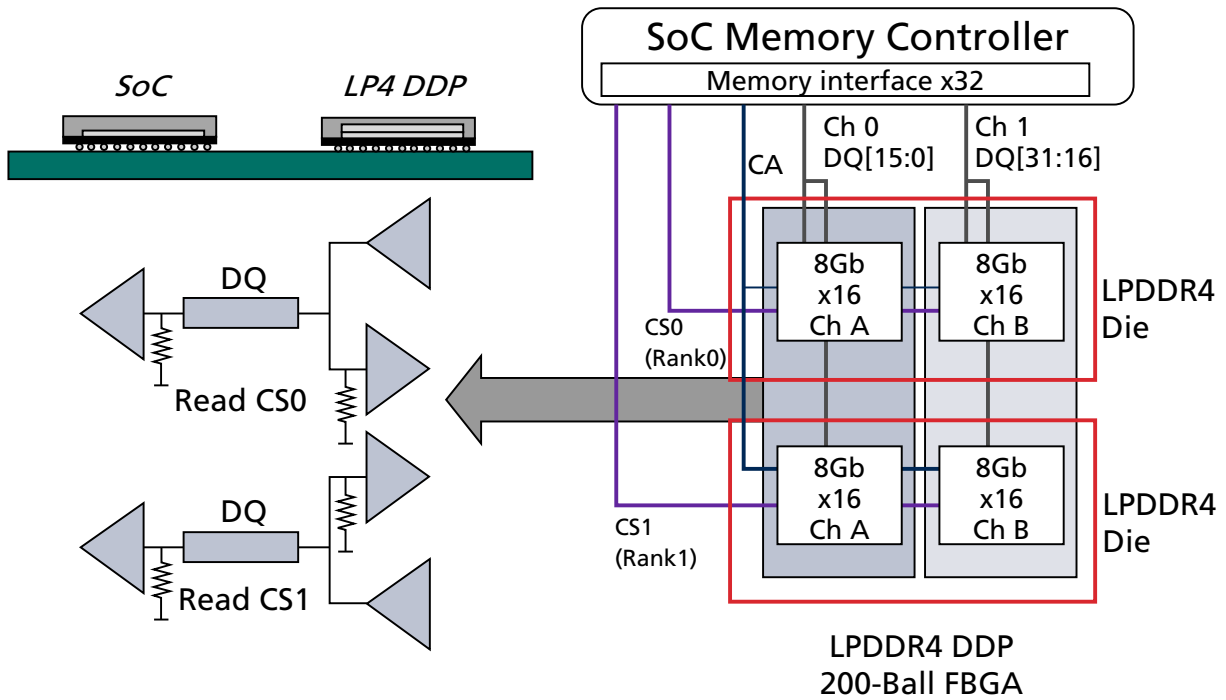
**Figure 1: Example DRAM Subsystem Arrangement – Two 2GB DDP 200-Ball Components**





## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines LPDDR4 Block Diagrams

**Figure 2: Dual 2GB (16Gb) = 4GB LP4 Subsystem (Read Only)**





## Programmable Drive Strength and Bus Topology

Because LPDDR4 products are designed for point-to-point topology applications, a programmable drive strength option is provided to match memory DQ/DQS drive strength to the impedance of the data bus traces, eliminating the need for a termination voltage supply ( $V_{\text{TERM}}$ ) and a series-termination resistor.

Six drive strengths are supported: RZQ/6 $\Omega$ , RQZ/5 $\Omega$ , RZQ/4 $\Omega$ , RZQ/3 $\Omega$ , RZQ/2 $\Omega$ , and RZQ/1 $\Omega$ .

In low-power, short-channel-trace, point-to-point systems, termination (ODT) can often be eliminated if the trace  $Z_0$  and drive impedance are carefully matched.

This section contains simulation results for READ operations that assess signal integrity [Data Bus DQ Read Eye Diagrams With ODT (Clock = 1600 MHz)]. The figure shows results for the controller and DRAM positioned 10mm, 20mm, 30mm and 45mm apart. The interconnect between the controller and the DRAM should be designed so that its characteristic impedance is approximately 50 $\Omega$ , nominally. The set up and models used are detailed below:

- Databus configuration: Point-to-two-point (controller to DDP package)
- DRAM driver model: version 5.0 Power Aware IBIS model
- DRAM package model: 200-ball RLC model extracted by Apex Quasi-Static 3D field solver
- DRAM driver  $V_{\text{OH}}$  setting:  $V_{\text{DDQ}}/3.0$
- PCB model: HSPICE frequency dependent W-element model with 10 coupled lines
- PCB target impedance: 50 $\Omega \pm 10\%$
- Controller package model: 200-ball RLC model (no controller package model available yet)
- Controller input capacitance load: 1.5pF
- Byte simulated: DQ[7:0], DQS0/DQS0# of the top die (which has the highest level of crosstalk)
- Eye measurement method: Aperture DC window ( $V_{\text{REF}} \pm 60\text{mV}$ ) with  $V_{\text{REF}}$  centering
- Pass/Fail criteria: Aperture DC  $\geq 60\%$  UI, voltage margin  $\geq 15\text{mV}$
- Simulation methodology: Design of experiment (DOE) with JMP statistical analysis tool
- Simulation tool: Synopsys HSPICE 2014.09-SP2 ver. J (latest version)

Because LPDDR4 products are used in point-to-point applications, data eye apertures for WRITE operations will be similar to those shown for READ operations, providing that the drivers for the memory controller have similar characteristics to the DRAM drivers. System engineers can also take advantage of on-die termination (ODT) options ( $R_{\text{TT}} = 120/240$ ) for higher speed or for more heavily loaded point to multipoint systems to improve signal integrity.

For the figures in this section:

- AptACDC is the AC DC aperture (the opening of the data eye)
- RailOShoot is the rail overshoot (measures peak distortion)
- RailUShoot is the rail undershoot (measures peak distortion)

Analysis covers all components in the memory/controller signaling channel (including I/O driver, memory package, PCB traces, controller package and receiver).



## **TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Programmable Drive Strength and Bus Topology**

Signal quality and integrity can be degraded because of many factors, including:

- Crosstalk (within the DRAM and controller packages, as well as with signal bus/traces on the system board)
- Intersymbol interference (ISI), which is related to impedance and bus topology
- Simultaneous switching outputs (SSO)/power delivery noise (SSO-induced power supply noise)
- The rising and falling edges of the signal can become distorted in electrically long structures due to dispersion and losses
- Coupling from neighboring conductors can introduce additional noise
- Mismatches can occur and the less than ideal nature of the source and load ends of the interconnect structure can affect results
- Power supply noise and simultaneous switching outputs can affect results

To assess signal integrity at a system-level, these factors are included in the simulation results.

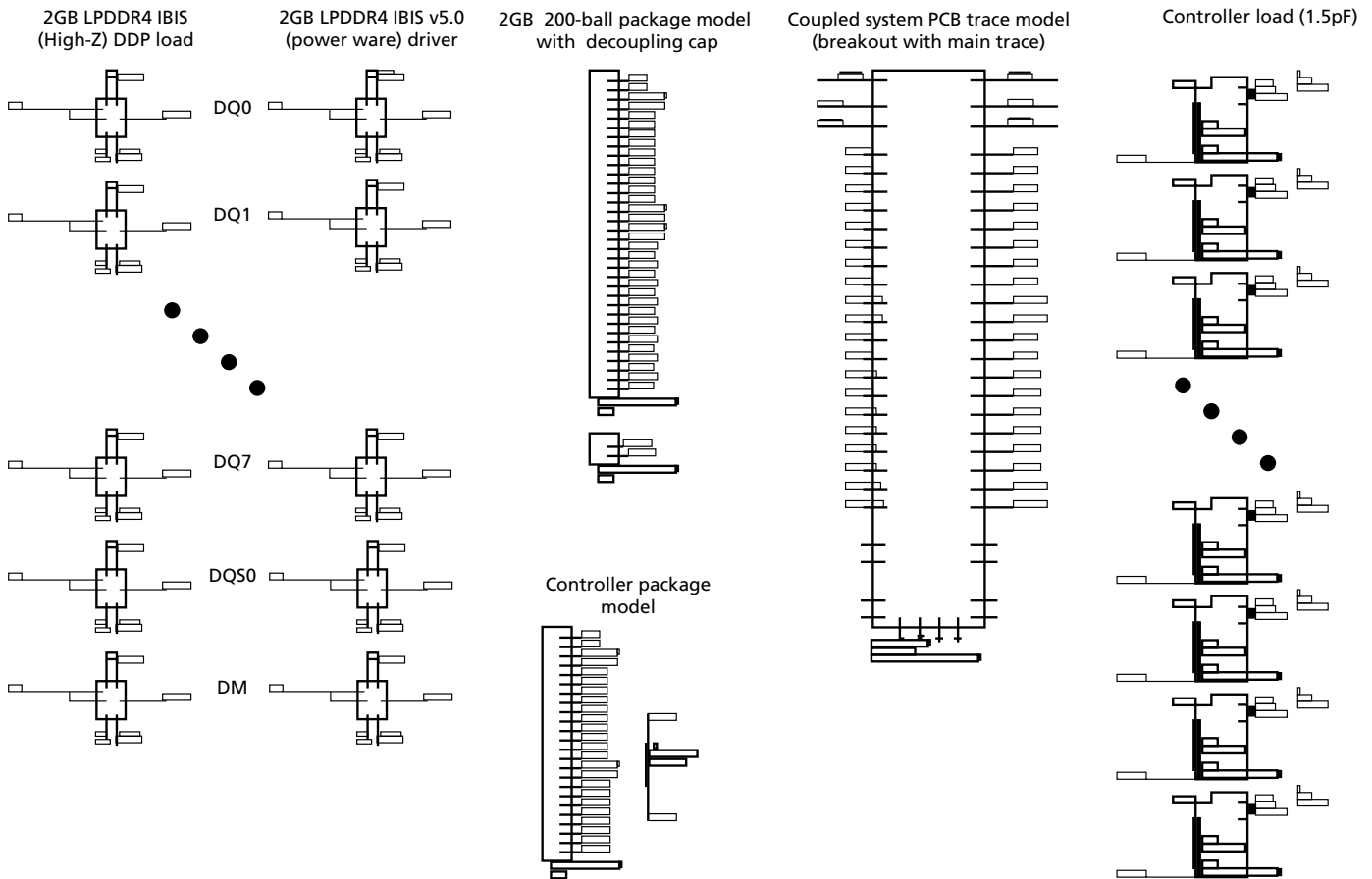
Because this technical note is intended for system board designers, various bus topologies (see the following figures) are presented to illustrate their impact on overall system performance:

- Bus length: 10mm/20mm/30 mm/45mm
- Bus/traces spacing: 0.1mm (2X dielectric thickness ~ distance to signal power reference plane)
- Load at receiver end: DDP—2GB LPDDR4 dual-die product model load used to emulate a typical SoC memory controller receiver load
- DQ bus termination: sweep LPDDR4 programmable values to represent typical SoC memory controller termination values

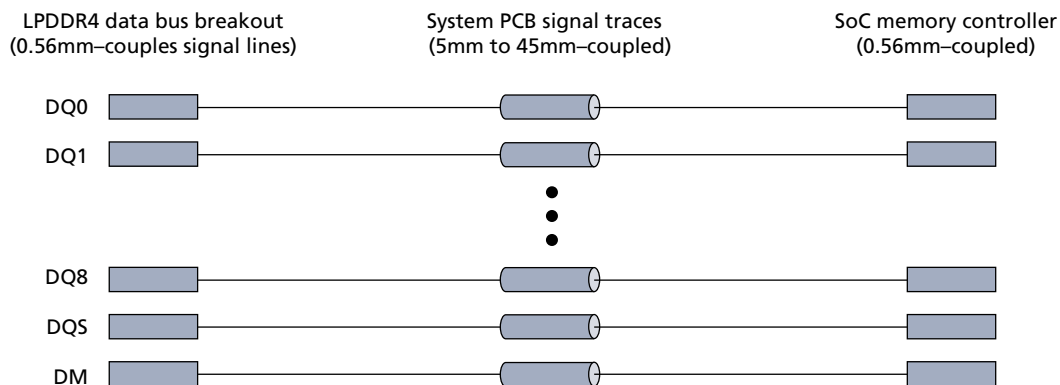


## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Programmable Drive Strength and Bus Topology

**Figure 3: System Simulation Model Topology Details**



**Figure 4: System PCB Topology Details**



Trace-to-trace spacing: 2X distance to signal reference. A via model is not included because vias in customer boards from the top and bottom layers to the inner layer are assumed to be short (1mm MAX), and therefore, the via impact is insignificant. We recommend routing all DQ nets on the same layer. If there are DQ net layer transitions, we recommend routing ground vias next to signal vias for good shielding and to maintain



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Programmable Drive Strength and Bus Topology

constant impedance. All layers where DQ nets are routed have to reference the same plane (preferably the ground plane). Data Bus DQ Read Eye Diagrams with ODT Clock shows a simulation for various data bus trace lengths (with  $Z_0 = 50\Omega$ , nominally). The eye diagrams show reasonable aperture and voltage margin; signal integrity looks good for this theoretical system and serves as a baseline.

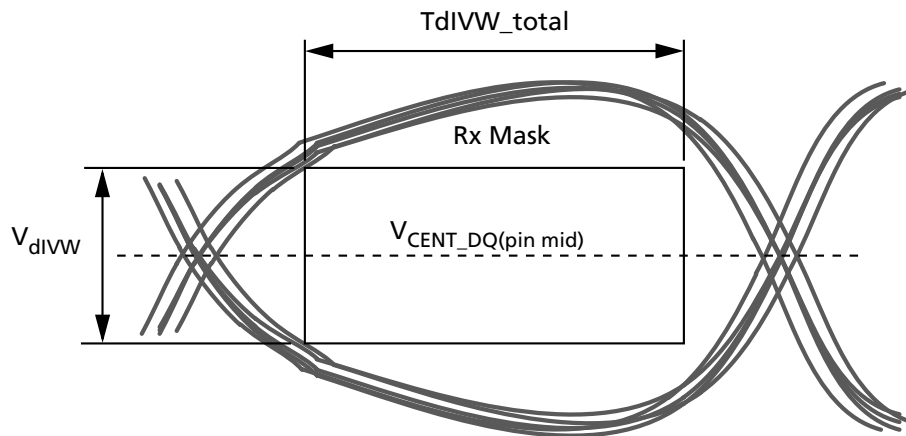
Because it is difficult to design a board system with only 10–20mm signal length, we recommend that signal length be kept somewhere between 30mm and 45mm to reduce signal noise and crosstalk.

Eye Diagrams Without ODT shows less than ideal channels and coupled lines with variable channel lengths on a DDP LPDDR4 platform without termination. As shown, the signals are degraded and the eye diagrams do not look optimal. As discussed earlier, signal integrity can be degraded for a number of reasons.

### DQ RX Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask ( $V_{dIVW\_total}$ ,  $T_{dIVW\_total}$ ) defines the area that the input signal must not encroach upon in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.  $V_{CENT\_DQ(pin\_mid)}$  is defined as the midpoint between the largest and the smallest  $V_{CENT\_DQ}$  voltage levels across all DQ pins for a given DRAM component. Each  $V_{CENT\_DQ}$  is defined by the center, which is the widest opening of the cumulative data input eye as shown Figures 5 and 6. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level  $V_{REF}$  will be set by the system to account for  $R_{ON}$  and ODT settings.

**Figure 5: Data Bus DQ Receiver (RX) Mask**

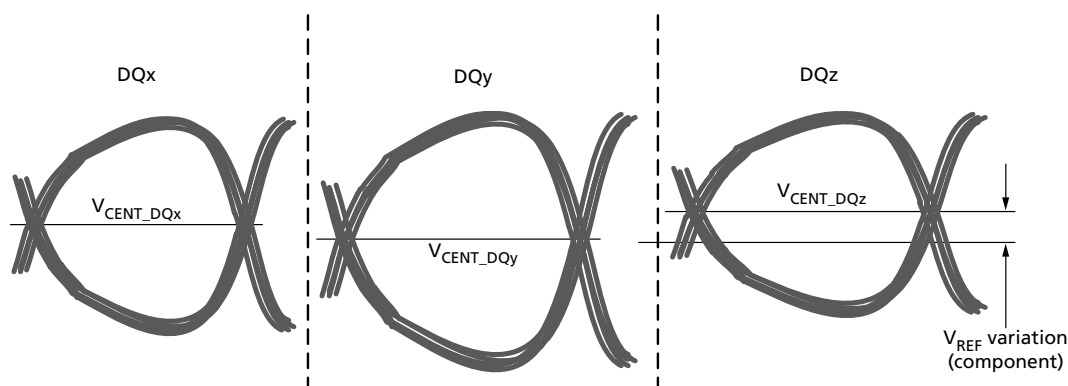






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**Figure 6: DQ Across Pin  $V_{REF}$  Voltage Variation**



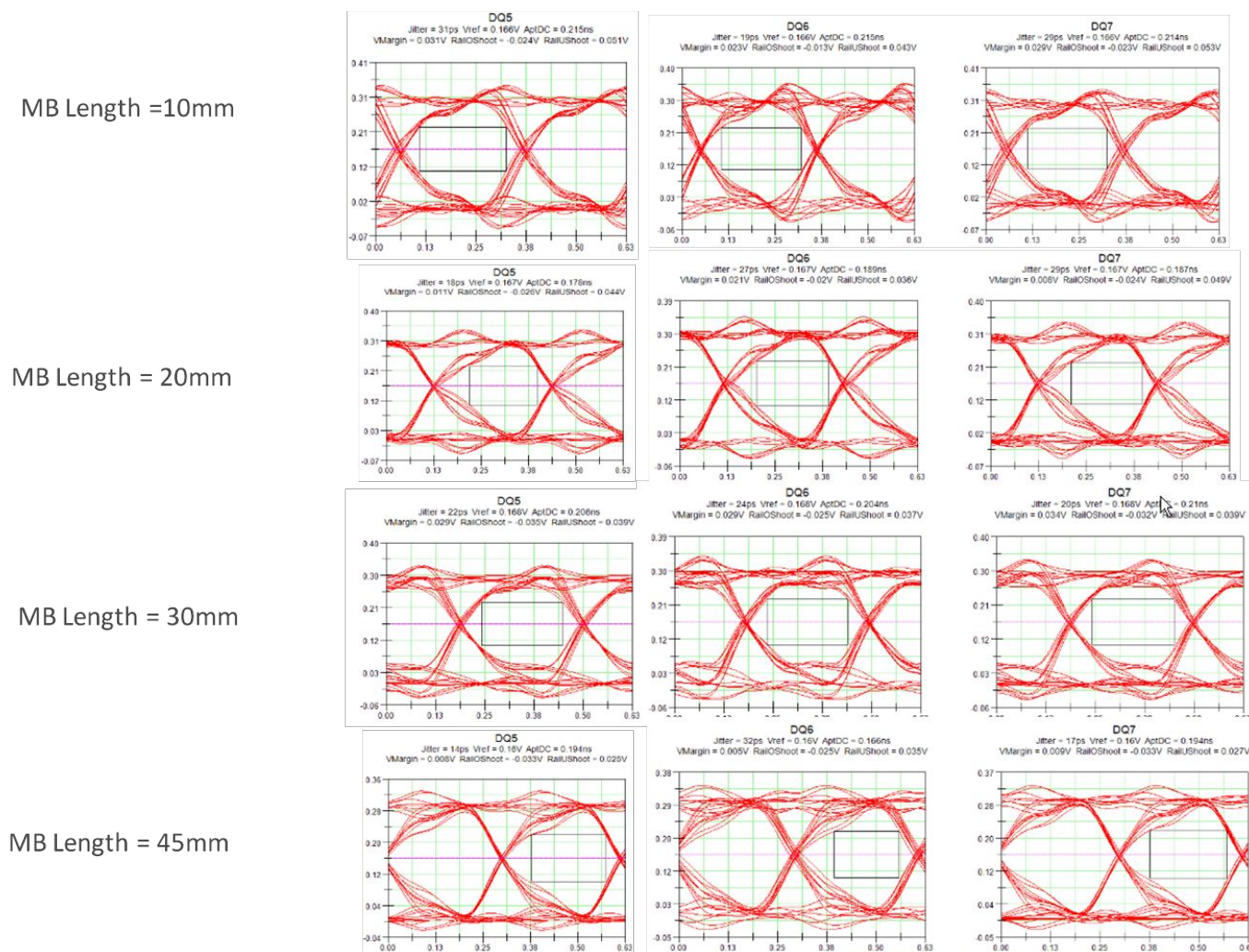
The following Data Bus DQ Read Eye Diagrams with ODT (Clock = 1600 MHz) indicates the effects of DQ5 and DQ7 on DQ6 across a range of signal trace lengths (10mm to 45mm). Table following shows a solution space summary for this figure. As would be expected, the best aperture and voltage margin values are achieved for the higher  $R_{ON}$  and ODT settings on the longer (more typical) signal trace lengths. The strongest pull-down  $R_{ON}$  [RZQ/6 (40 ohm)] and strongest termination (40 ohm) yields the largest data eye aperture, while weaker pull-down  $R_{ON}$  and weaker termination reduces the aperture.



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### Programmable Drive Strength and Bus Topology

**Figure 7: Data Bus DQ Read Eye Diagrams with ODT (Clock = 1600 MHz)**



**Table 3: Solution Space Table with ODT**

Notes 1–3 apply to entire table

Signal Trace Length	Memory PD $R_{ON}$	Controller ODT	Worst Case					Aperture DC (% UI)	Voltage Margin (mV)
			$V_{DDQ}$	Memory PKG Z	Controller PKG Z	Mother Board Z	Memory PVT		
5mm–10mm	40	40, 48, 60	1.06	37	37	55	Fast	68	27
	48	40, 48, 60	1.06	37	37	55	Fast	65	24
	60	40, 48, 60	1.06	37	37	55	Fast	62	19
	80	40, 48	1.06	37	37	55	Fast	62	20



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines

### Programmable Drive Strength and Bus Topology

**Table 3: Solution Space Table with ODT (Continued)**

Notes 1–3 apply to entire table

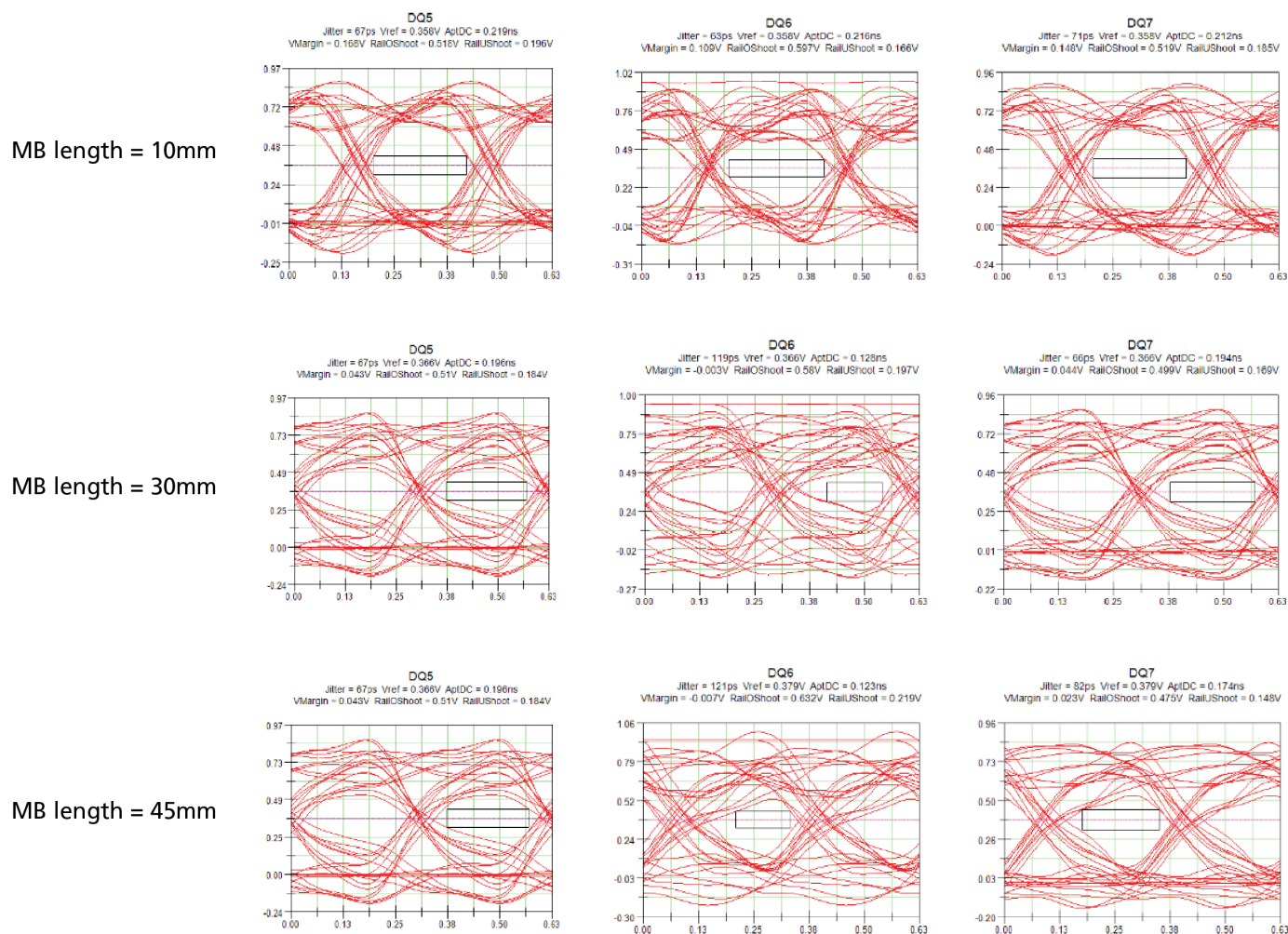
Signal Trace Length	Memory PD R <sub>ON</sub>	Controller ODT	Worst Case					Aperture DC (% UI)	Voltage Margin (mV)
			V <sub>DDQ</sub>	Memory PKG Z	Controller PKG Z	Mother Board Z	Memory PVT		
11mm–20mm	40	40, 48	1.06	37	37	55	Fast	69	20
	48	40, 48	1.06	37	37	55	Fast	67	17
	60	40	1.06	37	37	55	Fast	68	19
	80	NR	NR	NR	NR	NR	NR	NR	NR
21mm–30mm	40	40, 48	1.06	37	37	55	Fast	66	14
	48	40, 48	1.06	37	37	55	Fast	68	15
	60	NR	NR	NR	NR	NR	NR	NR	NR
	80	NR	NR	NR	NR	NR	NR	NR	NR
31mm–45mm	40	40, 48	1.06	37	37	55	Fast	61.76	16.69
	48	40, 48	1.06	37	37	55	Fast	59.35	14.07
	60	NR	NR	NR	NR	NR	NR	NR	NR
	80	NR	NR	NR	NR	NR	NR	NR	NR

- Notes:
1. NR = Not recommended.
  2. Passing criteria = Aperture DC (%UI) ≥60%.
  3. Voltage margin ≥15mV.



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Programmable Drive Strength and Bus Topology

**Figure 8: Eye Diagrams without ODT**



**Table 4: DOE Sweep Variables**

Parameter	Description	DOE Variable Type	Topology Parameter Values	Unit
V <sub>DDQ</sub>	V <sub>DDQ</sub>	Continuous	10.6, 1.1, 1.17	V
mblen	MB length	Continuous	5, 15, 25, 35, 45	mm
mempkgz	Memory package Z	Discrete numeric	37, 40, 43	Ohm
cntpkgz	Controller package Z	Discrete numeric	37, 40, 43	Ohm
mbz	MB impedance	Discrete numeric	45, 50, 55	Ohm
mempd	Memory driver PD impedance	Discrete numeric	40, 48, 60, 80, 120, 240	Ohm
mempvt	Memory driver PVT	Categorical	TYP, slow, fast	
cntodt	Controller ODT	Categorical	40, 48, 60, 80, 120, 240, DIS	Ohm



## Power Delivery

As clock frequencies increase, timing and noise margins shrink.

LPDDR4 products are high-frequency, low-power SDRAM with data buses that experience simultaneous switching outputs (SSO). When SSO occurs, large amounts of current are sourced from or sunk to the power delivery network (PDN), especially on  $V_{DDQ}$  and  $V_{SSQ}$  lines. If the PDN is not well designed, the SSO will create significant noise on power supply rails causing transistor performance degradation which can translate into timing issues, particularly when full drive strength is selected for the interface. In extreme cases, the power supply can collapse leading to system failures.

Memory vendors should ensure a robust PDN within the memory package, and controller vendors should ensure a robust PDN within controller packages. System engineers should design a robust PDN for the system board to power all components on the board.

To design a good, solid PDN on a system board:

- Ensure the path impedance from voltage regulator module (VRM) to the LPDDR4 component(s) and platform processor are as low as possible. Lower path impedance results in lower voltage ripple on the board.
- Use partial plane structures. If not possible, ensure the power deliver routes for the  $V_{DDQ}/V_{SSQ}$  and  $V_{DD}/V_{SS}$  lines are as wide as possible.
- Ensure sufficient decoupling capacitors on board are closely placed to the system processor and the LPDDR4 component(s) to absorb high frequency current spikes.
- Run full system simulation to ensure the PDN is robust enough to sustain the peak current demand with adequate margin.

## Decoupling

Adequate power decoupling on the PCB is necessary to prevent excessive  $V_{DD}$  noise and the resulting memory data transfer errors in applications where power-supply draw can change by magnitudes in a single clock cycle.

Decoupling serves two purposes:

- Maintains stable supply voltages for the components
- Provides a return path for signal currents

Normal practice is to decouple the power planes around the components (as close as possible) because the planes provide a low inductance path between the decoupling capacitors and the components. (See the Recommended Decoupling Capacitor Placement for 200-Ball LPDDR4 Package figure.)

For decoupling of internal functions, such as REFRESH, lower frequencies are involved (around the 1 MHz range). For providing a return path for signals, higher frequencies are involved (up to 50 MHz). Above 50 MHz, external decoupling is less effective because the components rely on internal decoupling, which is part of all components.

For internal functions, capacitance is an important consideration; for return currents, inductance is a primary concern. Both require suitable capacitors in 0202 (standard)/0505 (metric) or 0201 (standard)/0603 (metric) packages, which provide low enough inductance and will meet the requirements for the full frequency range. Having separate capacitors for each range is not required.







## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Layout: Trace Widths, Intragroup Spacing, Intergroup Spacing

### Layout: Trace Widths, Intragroup Spacing, Intergroup Spacing

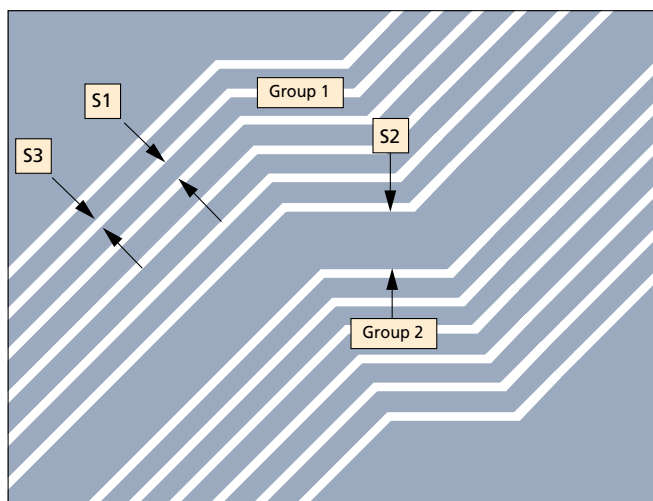
Two types of trace spacings influence system signal integrity: intragroup spacing and intergroup spacing.

Intragroup spacing (S1) is the distance between two adjacent traces within a related set of signals having similar or equivalent functionality. The clocks, CA bus and data bus byte lanes are all signal sets. Each data bus is separated into data bytes (sets of eight DQ signals) and the associated strobe and mask signals (for ten signals total).

Intergroup spacing (S2) is the distance between the two outermost signals of different signal sets.

The difference between trace spacing S1, S2, and trace width (S3) is shown in the figure below where group1 and group 2 could be different data bus byte lanes for example.

**Figure 10: S1, S2 Trace Spacing and S3 Trace Width**



**Note:** White lines indicate copper traces.

Recommended spacing is dependent on dielectric thickness and routing pitch. Generally, the minimum routing spacing should be 2X the dielectric thickness, which is assumed to be approximately 0.15mm for a FR-4 type PCB. This means at least 0.3 mm for the trace S1/S2 spacing. Closer spacing than the recommended minimum for S1 or S2 can increase crosstalk.

If all signals are routed tighter than the recommended spacing for their full length, crosstalk is likely to disrupt SI; however, if spacing limits are not met for short segments, the effect on SI is likely to be minimal.

Crosstalk is a function of trace spacing, dielectric height, and slew rate; for systems with slew rates <1 V/ns, trace spacing can be closer. Lower-speed systems generally have more timing budget, which accommodates more crosstalk without affecting SI.



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Layout: Trace Widths, Intragroup Spacing, Intergroup Spacing

### Trace Width (S3) Design Guidelines

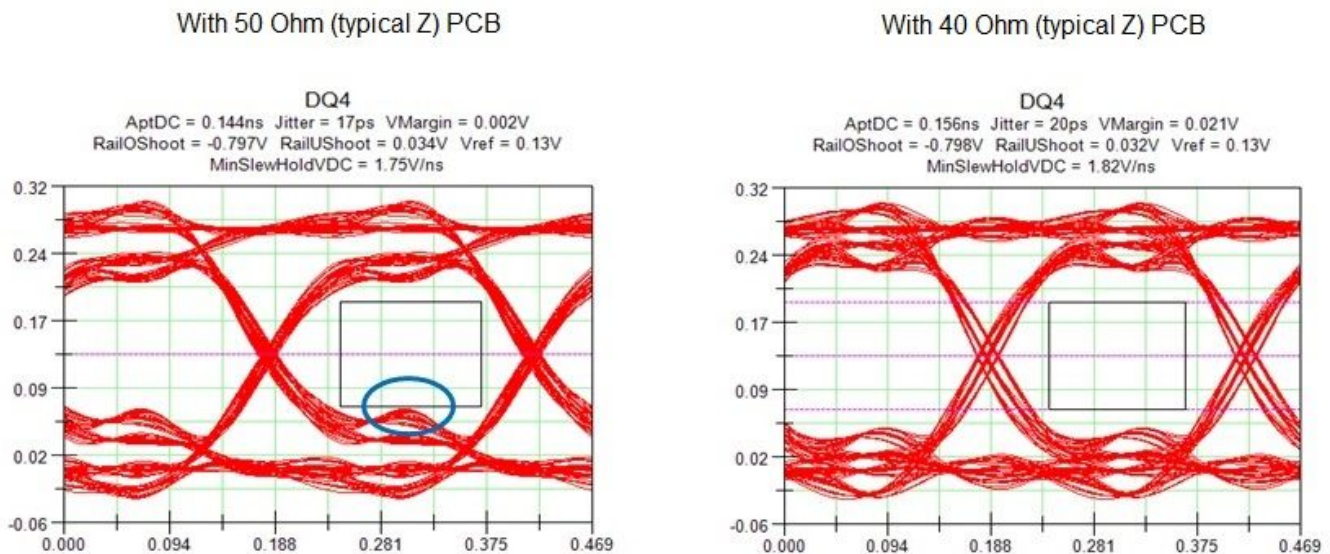
Recommended minimum trace width, S3, for functional signal sets (SI simulation on data bus used for this example):

- DQ/DQS/DM lines = 0.1mm
- CA lines = 0.1mm
- Clock lines = 0.1mm

Supply voltages  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ , and  $V_{SSQ}$  must be composed of planes as much as possible. Short connections ( $< 0.2\text{mm}$ ) are commonly used to attach vias to planes in Micron designs. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance. We recommend the trace width match the via size at the decoupling capacitors (0.3mm for both S1 and S2 trace spacing).

For operation of LPDDR4x non-Pop (200b package, etc.) products at up to 4266 Mbps with worst-case dual-rank layout topology, Micron recommends designing data bus PCB traces for lower  $Z_0$ . The recommended  $Z_0$  would be 40 ohm (+/-10%). DQ trace lengths (with zero mismatch) up to 45mm were simulated for the design guide example. This is no guarantee of what maximum tolerable trace lengths for a particular system design can be. The maximum trace length is highly dependent on several parameters of the system such as trace topologies, transmitter driver strengths, terminations, etc. Accurate post-layout SI/PI simulations are the best way to ensure adequate voltage and timing margins on any particular system design.

**Figure 11: Improved Voltage Margin with Lower Trace Impedance**







## PCB Stackup

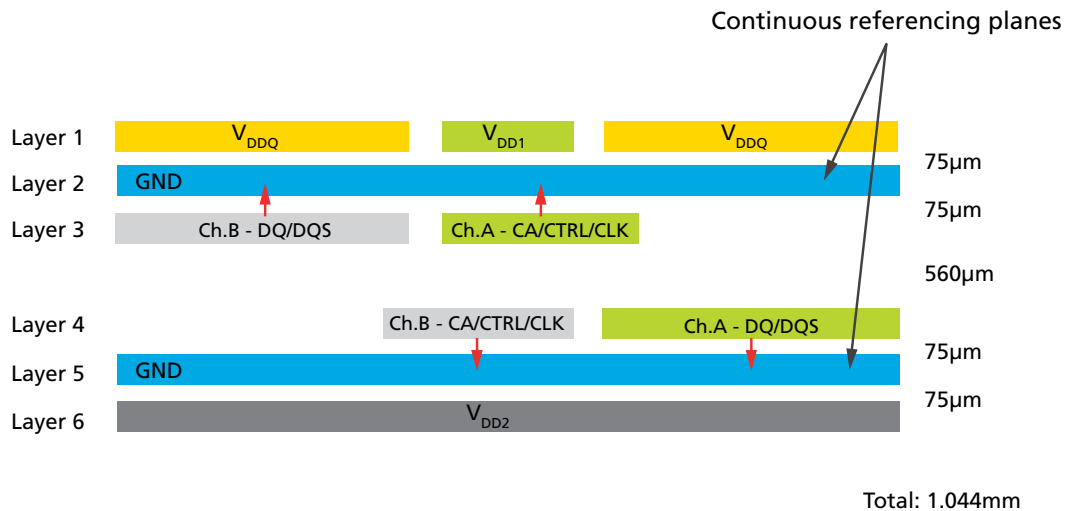
A well-designed PCB stackup is critical in eliminating digital switching noise. The ground plane must provide a low-impedance (Low-Z) return path for digital circuits.

We recommend using a PCB design with a minimum of six layers for good SI and PI performance.

- Layers 3 and 4 for signals (see the figure below)
- Layers 2 and 5 for ground ( $V_{SS}$ )
- Layers 1 and 6 for power ( $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DDQ}$ )

The required number of signal layers is determined by the number of signal groups being routed and the required isolation between them. The number of devices being routed and the size of the PCB dictate the number of signal layers required. Simulation should be done to provide feedback on signal integrity for a given application. The following figure shows a six-layer PCB example with four internal layers.

**Figure 12: Example Six-layer PCB with Four Internal Layers**



## PCB Dielectric

The dielectric constant of PCB materials for most memory applications is 3.6 to 4.5, varying with frequency, temperature, material and the resin-to-glass ratio. FR-4, a commonly used dielectric material, averages 4.1 with signaling at 1 GHz. FR-4 is a copper-clad laminate that is adequate for most applications.



## Design With Timing Budget

Common practice is looking at the design from a timing budget standpoint to provide flexibility in the routing portion of the design, if there is suitable margin. This starts with simulation. By referencing the eye diagrams in Programmable Drive Strength and Bus Topology, a setup and hold time can be established. From there, the parameters not included in the simulation must be added.

Typical routing for LPDDR4 components requires two internal signal layers, two surface signal layers, and four other layers ( $2 V_{DD}$  and  $2 V_{SS}$ ) as solid reference planes.

LPDDR4 memories have  $V_{DD}$  and  $V_{DDQ}$  pins, which are both typically tied to the PCB  $V_{DD}$  plane. Likewise, component  $V_{SS}$  and  $V_{SSQ}$  pins are tied to the PCB  $V_{SS}$  plane. Each plane provides a low-impedance path to the memory devices to deliver  $V_{SSQ}$ . Sharing a single plane for both power and ground does not provide strong signal referencing. With careful design, it is possible for a split-plane design to work adequately:

- Designs should reference data bus signals to  $V_{SS}$ .
- CA bus and clock should reference  $V_{DD}$ .
- Signals should never reference  $V_{DD1}$ .

## Return Path

A reference plane is required for all high-speed signals. Minimizing loop area reduces transient current noise and electromagnetic interference (EMI). Loop areas may be minimized by having the return path directly next to the signal trace and by using a single layer as much as possible for the return path of a specific signal. For example, with a six-layer PCB, if layer 2 or 5 is the reference plane for a specific signal routing, routing signals on layer 3 or 4, respectively, would be a good choice.

Components always have a number of  $V_{SS}$  and  $V_{DD}$  vias, so this issue is usually not a concern. If there is a switch from  $V_{SS}$  to  $V_{DD}$  referencing, the path will need to include a capacitor for the plane-to-plane transition. This usually results in a larger increase in loop area and should be avoided.

## Routing

Standard characteristic impedance ( $Z_0$ ) of no more than  $50\Omega$ , nominally, is recommended for all traces. The  $50\Omega$  level also provides a good match to the output impedance of the SoC/FPGA memory controller drivers. Designers are advised to specify  $Z_0$ , enabling board manufacturers to adjust dielectric thickness and line width to achieve the specification.

Though there are many signals on LPDDR4 components, most of them have similar functionality and work together. Groups of I/O signals have one of four purposes:

- Carry a binary address (CA)
- Transmit or receive data (DQ)
- Relay a command to the device (CA)
- Latch in data or a command (DQ)

Command and address inputs are provided according in the data sheet command truth table. The control group includes chip select (CS#) and clock enable (CKE). Each data group/lane contains 10 signals: eight DQ (DQ[7:0]), strobe (DQS) and data mask (DM).



## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Design With Timing Budget

Devices with x8 bus widths have only one data group, while x16 and x32 bus-width devices have two and four lanes, respectively.

Related functionality makes minimizing skew critical. This requires the signals of each group to be routed to similar electrical lengths assuming the loads are equivalent. Routing entire bus groups on single layers minimizes skew.

A timing budget only requires the margin be positive for a system to work, assuming all parameters are accounted for. Meeting a timing budget is dependent on many factors. The higher the speed or more complex a system, the more difficult it is to meet the timing budget. Allowed skew should be considered in terms of whether there is plenty of margin in a timing budget. Twenty five millimeters of trace is approximately 165ps of delay. For a component operating at an 1600 MHz clock rate, the bit period is 312.5ps. It may be more meaningful to consider skew as a percentage of the period:  $1\% = 3.125\text{ps}$ ;  $3.125\text{ps} = \text{approximately } 0.5\text{mm}$ . To match lengths to within 1% of the clock period, match the traces to within 0.5mm.

For simple point-to-point systems (one LPDDR4 component), there should be sufficient margin in the timing budget. Consider matching to 5% or 2.75mm. For the more complex point-to-multipoint systems (four LPDDR4 components), use 1% or 0.5mm. For two components, something between those values (such as 3% or 1.5mm) may be acceptable.

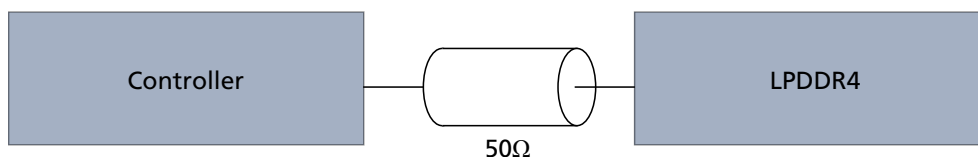
Serpentine trace patterns contribute the desired delay, but there is some self-coupling that can change the propagation delay for a signal. Use simulations that include coupling to validate timing.

Vias contribute to timing error. If each signal in a bus group contains the same vias transitioning between the same layers, the vias may be ignored. If there is a mismatch, the additional delay may push the timing margin to the negative side. Simulations will take vias into account; therefore, if the entire bus is simulated, all vias are accounted for. If the simulations do not include the entire bus, additional delay to compensate for the vias should be considered. One formula for the additional delay is 2X the actual via barrel length that the signal uses to change layers.

### Point-to-Point Topology

Placing the clock signals on an internal layer minimizes EMI noise. Match CK trace length to CK# trace length  $\pm 0.5\text{mm}$ . If multiple clock pairs are transmitted from the controller to components, all clock-pair traces should be equivalent within  $\pm 0.5\text{mm}$ .

**Figure 13: Point-to-Point Topology**



Matching CK to data bus will likely result in some skew due to the different loads, even with the same trace length. To determine the skew requires simulations. The slew rate between the CK and the DQ will be different. This alone will affect the timing relationship between CK and DQ. If the termination is different, the timing relationship will be affected.



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Matching CK to the CA bus requires simulations as well. Differences in slew rate and termination cause skew between CK and the CA bus signals.

From simulations for a simple point-to-point configuration, it may be determined there is sufficient margin to allow 3–5% skew in some groups.

For a point-to-point configuration example (see Point-to-Point Topology above), the trace impedance is  $50\Omega$  and the routed length is 5cm. With a 1600 MHz clock, the resulting waveforms for DQS and DQ are as shown in Data Bus DQ Read Eye Diagrams with ODT (Clock = 1600 MHz).

### Point-to-Two-Point Configurations

When the system becomes more complex, additional guidelines help ensure an adequate system:

- With two loads, control reflections to minimize their impact on signaling.
- For address and clock, where signals are always in the same direction, balance the route. After the signal from the controller splits to connect with each LPDDR4 component, control the timing so that the signal reaches each LPDDR4 component at the same time.

Typically, the trunk and the branches are the same impedance (for example,  $60\Omega$ ). The branches represent a  $30\Omega$  impedance so there is a reflection that returns to the controller. If the controller is the same impedance as the transmission line, there will not be an additional reflection. Making the branches equal in length helps to control reflections. It is best to have the reflections from the open circuit, which the LPDDR4 component represents, return to the branch point at the same time (they actually add at this point). If the impedance in the trunk is not half the impedance of the branches, there will be another reflection back toward the components; however, there will not be additional reflections. Any signal that continues down the trunk will eventually reach the driver. If the driver impedance matches the transmission line impedance of the trunk, there will not be an additional reflection. If the branches are kept short, the reflection that returns to the component from the mismatch in impedance between the trunk and branches will occur during the rise time and will not be observed as a separate event.

- In practice, the driver should be within  $20\Omega$  of transmission line impedance of the trunk. The closer the match, the better the result. Simulations should be used to verify adequate results.
- With two LPDDR4 components, all of the interfaces may not be point-to-two point. The data bus may still be point-to-point. If this is the case, refer to the point-to-point section for the data bus. Also, if there are two clocks available from the controller, one may be dedicated to each LPDDR4 component. In some cases the clock is terminated and the address and DQ bus are not. This will shift the timing and require simulations.
- Slew rate is dependent on the capacitance at the load and the source impedance. The source impedance is the driver impedance plus the transmission line impedance (mostly the trunk). To improve slew rate, consider shading the driver impedance to and the trunk impedance on the low side. A  $40\Omega$  driver with  $50\Omega$  trunk and  $60\Omega$  branches may be a good choice. Obviously, wider traces require more space.



## Point-to-Four-Point Configurations

Point-to-four-point configurations contain the heaviest load and lowest bandwidth. If the address is the only bus that requires this configuration, it sets the speed limit for the system. If the DQ bus must be point-to-four point, it also sets the speed limit for the system. This is because the capacitance of the DQ pins is higher, which forces a lower slew rate. Clock has a similar capacitance to an address. If the clock is point-to-four-point, it will perform similarly as address. Being only two traces, it is more likely that it could be improved with a lower impedance or termination near the load.

Symmetry is required. Each signal may have different lengths; however, within one signal, related branches must be the same length. To have similar timing, the total length from the controller to LPDDR4 component should match across all signals. If the branches are different for different signals, the trunks must also be different so that the total is a constant. This formula is an approximation; simulations are required to verify that the result is acceptable.

## Clock Routing with Multiple LPDDR4 Devices

LPDDR4 devices require differential master CK and CK# clock inputs. All CA input signals are sampled on the rising edge of CK. CS and CKE input signals are sampled at the rising edge of CK as well. Therefore, it is important for LPDDR4 devices to have a clean differential clock input.

Ideally, CK and CK# are 180° out-of-phase such that CK and CK# cross  $V_{REF}$  at the same point. This balances the output data so that each data word has the same valid time. These signals may be generated directly by the controller chip or by a separate clock chip. Best system margins will be obtained when CK and CK# are exactly 180° out of phase.

Proper terminations on the lines may provide clean differential clock input to the LPDDR4 devices.

- $R_{TT} = 150\Omega$  and  $R_{TT} = 200\Omega$  provide good clean eyes and adequate voltage swing.
- $R_{TT} = 150\Omega$  is recommended for best results.

**Note:**  $R_{TT} = 1M\Omega$  (open) may cause too much reflection and is not recommended. Choose unterminated differential CK/CK# at your own discretion.

For LPDDR4 systems, match CK trace length to CK# trace length  $\pm 0.25mm$ . If multiple clock pairs are transmitted from the controller to the components, all clock-pair traces should be equivalent within  $\pm 0.25mm$ . Simulations should be run to determine an appropriate relationship between CK and DQS length. After an optimal number is determined, a tolerance of  $\pm 0.635mm$  is acceptable.

Recommended LPDDR4 routing topology for clock pairs is shown in the following figures.

If the trace lengths from the split-point to the LPDDR4 components are less than approximately 25mm, use a single 150–200 $\Omega$  resistor ( $R_{TT}$ ) at the split-point, as shown in Single CK/CK# Differential Resistor Placement at Split-Point.

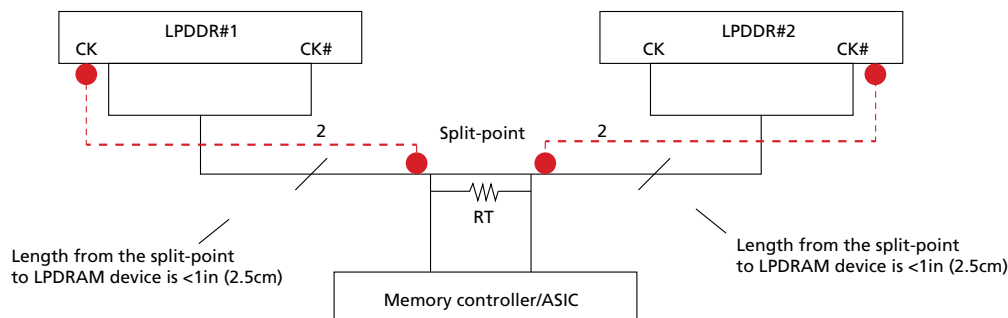
If the trace lengths from the split-point to the LPDDR4 components are greater than approximately 25mm, use two resistors located near the respective components, as shown in Dual CK/CK# Differential Resistor Placement at Component. These resistors are in parallel, so each  $R_{TT}$  should be 300–400 $\Omega$  to keep the effective resistance near 150 $\Omega$ .



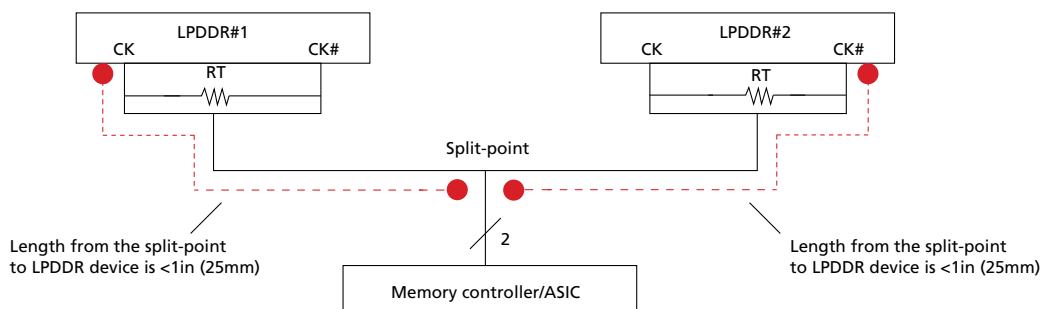
## TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Design With Timing Budget

Use simulations to determine the optimal relationship between CK and address. Select a tolerance based on the margin in the timing budget. Little margin is available at clock rates of 667 MHz and above.

**Figure 14: Single CK/CK# Differential Resistor Placement at Split-Point**



**Figure 15: Dual CK/CK# Differential Resistor Placement at Component**



### Control/Address (CA), and Data Routing to Multiple LPDDR4 Components

If an application requires additional memory, multiple devices can be used. The additional load and routing will affect signal integrity. Standard LPDDR4 applications may need the ODT option on the LPDDR4 CA bus.

When routing the interconnect between the controller and the memory devices, using a balanced T topology is recommended. This will maintain an equal flight time for the signals going to each of the devices. The drive strength selection should still be chosen to match the trace impedance; however, signal integrity and timing margins could improve if the drive strength is set to a lower impedance.

It is important to simulate any design. When defining the source impedance, the selections available may not be ideal for your application. In such cases, it may be necessary to implement the programmable LPDDR4 CA bus ODT.

In a multi-point system design, address and control lines can take advantage of the uni-directional bus. The equivalence simplification of circuits applies to transmission lines, so at the point of the T where the trace splits, the equivalent impedance of the parallel combined trace is one half that of the original impedance. This impedance discontinuity will cause some disturbance on the signals. To reduce this effect, the impedance of the trace from the split to the device can be increased so that the parallel combination



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of the traces is closer to the original impedance of the trace. This reduces noise on the signal and improves signal integrity.

### Miscellaneous Routing Recommendations

A 1mm difference in CA or data bus signal-group trace lengths equates to a skew of approximately 6.7ps. If the timing budget can absorb this minor amount of lane-to-lane skew and other routing delays, the system will perform normally. Total routing-based delays must meet  $t_{DQSCK}$ , controller DQS recovery limits and other data sheet AC timing parameters.

Regardless of bus type, all signal groups must be properly referenced to a solid  $V_{SSQ}$  or  $V_{DDQ}$  plane. For both READ and WRITE operations, the key relationship is between CK/CK#, DQ, DM and DQS signals (the LPDDR4 data group), which operates at twice the speed of other signal groups and makes SI more critical. DQ, DQS and clock lines are best referenced to  $V_{SSQ}$  to minimize noise. If a  $V_{SSQ}$  layer is not easily accessible, address and command lines can reference a  $V_{DDQ}$  layer.

Keep traces as short as possible. If trace length (from controller pad to SDRAM pad) is <2.5cm for both LPDDR4 point-to-point applications, routing is simpler and signal quality usually increases in proportion. In most cases, trace lengths >5cm lead to more signal undershoot, overshoot and ringing—all of which are detrimental to SI.

### Additional Trace-Length Design Guidelines

- Within a byte lane, match all DQ and DQS trace lengths as close to zero mismatch as possible and route data groups next to a  $V_{SS}$  plane to minimize the return path/loop length.
- Maintain a solid ground reference (no split planes, and so on) for each group to provide a low-impedance return path; high-speed signals must not cross a plane split.
- It's strongly recommended for high speed nets to maintain the same reference plane (either ground or power) all the way from Controller ball to DRAM ball and avoid reference plane change in order to keep continuous return path.
- It's strongly recommended that reference vias (ground or power) to be placed as close by to each DQ via as possible in order to keep a continuous return path.

### Write and Read Training

The figure below shows the recommended LPDDR4 training steps for booting up the system. Part of the process is the write training step. For the data bus write path, Micron LPDDR4 products use an unmatched data strobe-to-data (DQS-to-DQ) path to enable high-speed performance and save power. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye for writes to the memory. Recommended write training sequence:

#### 1. Booting

Use the WR/RD FIFO method (or relevant SoC-defined write training to define initial  $t_{DQS2DQ}$  delay) + DQS oscillator (to confirm MR18/19 as reference)

#### 2. Periodic training during normal operation

Use the DQS oscillator method (to compensate the  $t_{DQS2DQ}$  delay owing to PVT). The DQS oscillator is to adjust the DQS/DQ delay by PVT; however, without previ-



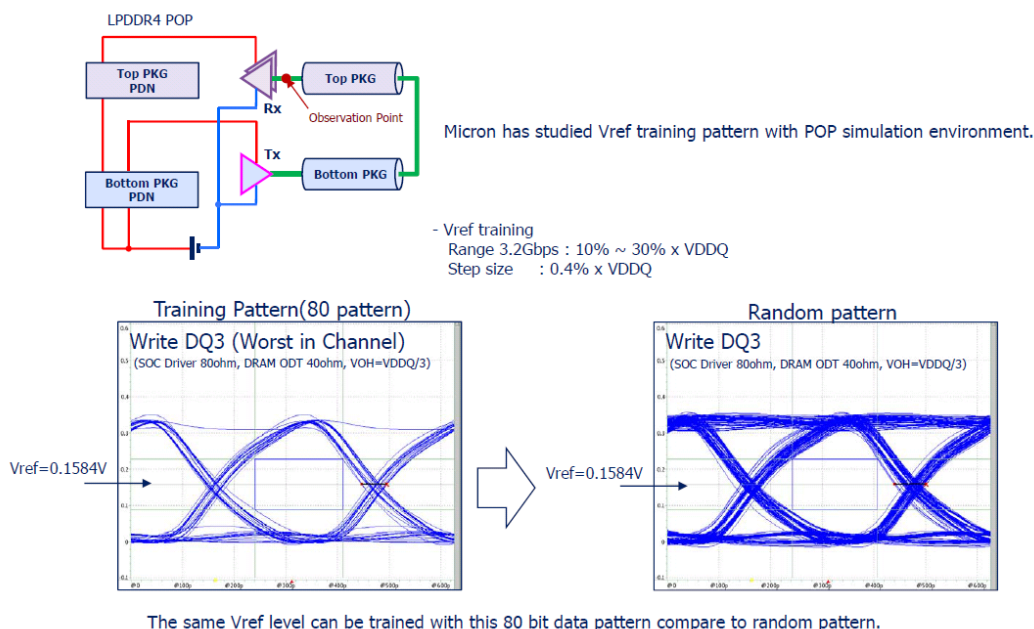






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**Figure 18: DQ Bus Training Pattern**



## Simulation

For a new or revised design, we strongly recommend simulating I/O performance at regular intervals (pre- and post-layout for example). Optimizing an interface through simulation can help decrease noise and increase timing margins before building prototypes. Issues are often resolved more easily when found in simulation, as opposed to those found later, which can require expensive and time consuming board redesigns or factory recalls.

Micron has created many types of simulation models to match the different tools in use. Component simulation models currently on [micron.com](http://micron.com) include IBIS, Verilog, VHDL, HSPICE, Denali and Synopsys.

Verifying all simulated conditions is impractical, but there are a few key areas to focus on: DC levels, signal slew rates, undershoot, overshoot, ringing, and waveform shape. Also, verifying the design has sufficient signal-eye openings to meet both timing and AC input voltage levels is extremely important. For additional general information on the simulation process see Micron's technical note, TN-46-11: DDR SDRAM Point-to-Point Simulation Process.



## Conclusion

Signal integrity, power delivery, routing and decoupling are all major concerns when designing LPDDR4 applications.

LPDDR4 designs provide an attractive alternative to traditional DRAM designs when used for embedded applications. The option to control the drive strength to match the impedance of the memory bus enables removal of the termination voltage ( $V_{\text{TERM}}$ ) and series termination resistors. LPDDR4 products can be used to optimize performance and reduce power consumption in embedded applications.

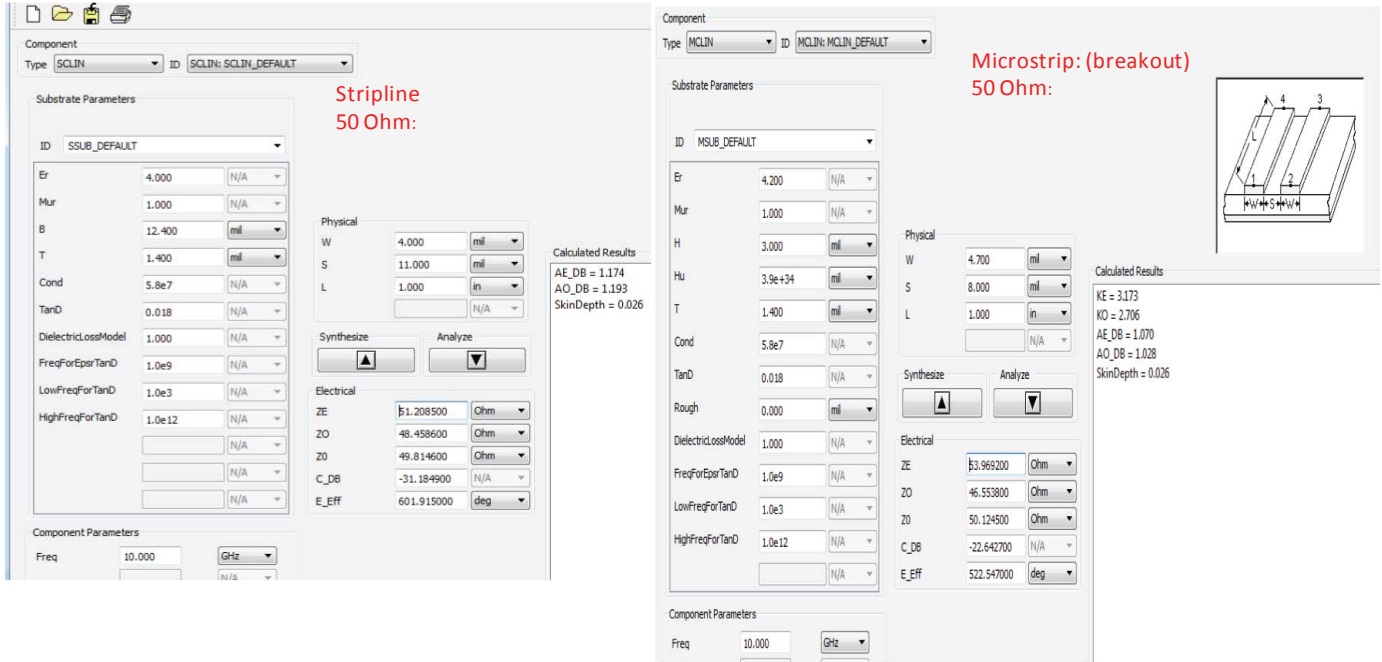
High-end LPDDR4-based embedded applications, when properly designed and validated through simulations, can realize superior functionality and stability.



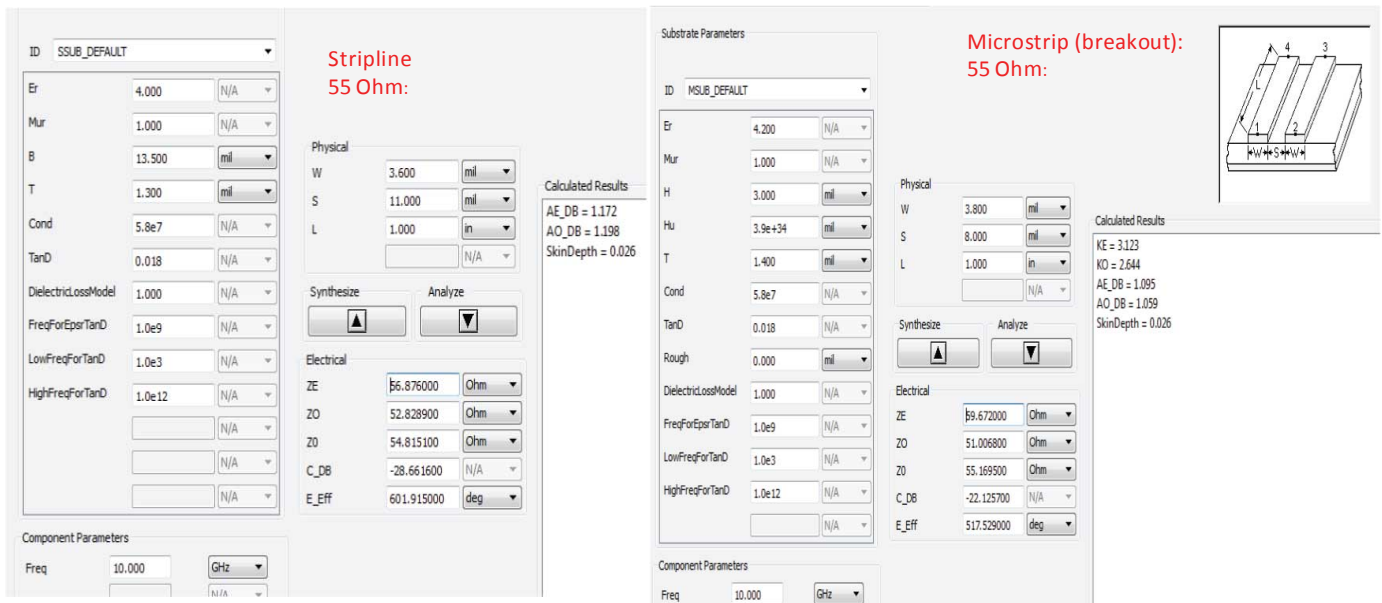
# TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Appendix A

## Appendix A

**Figure 19: PCB Stackup Target 50 Ohm ( $\pm 10\%$ )**



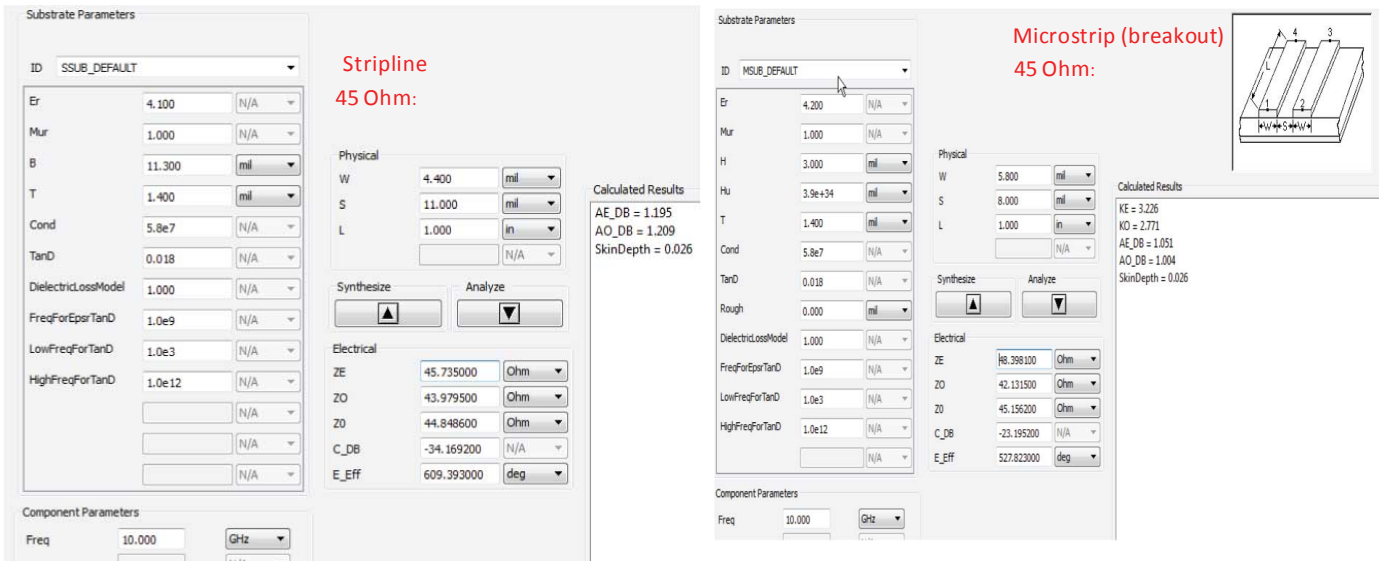
**Figure 20: PCB Stackup Target 50 Ohm (+10%)**



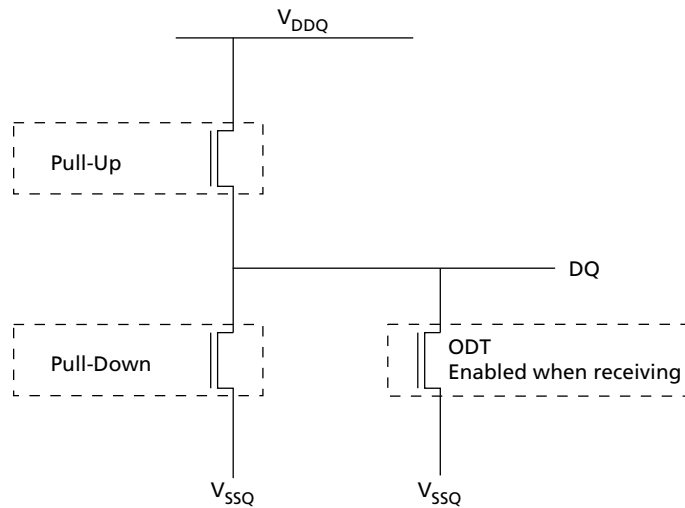


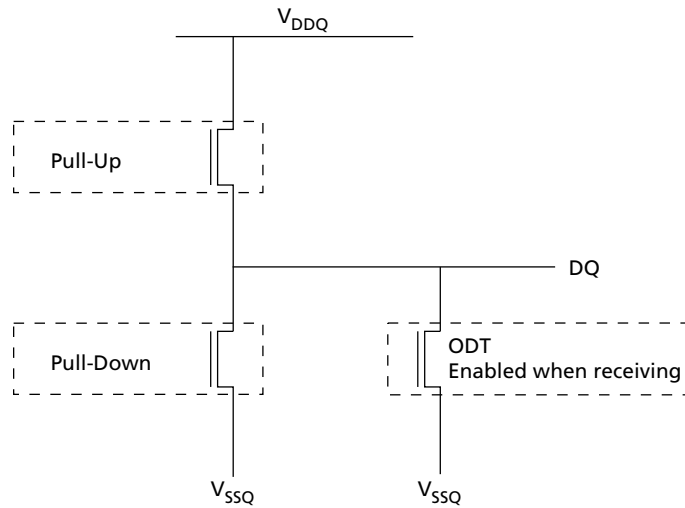
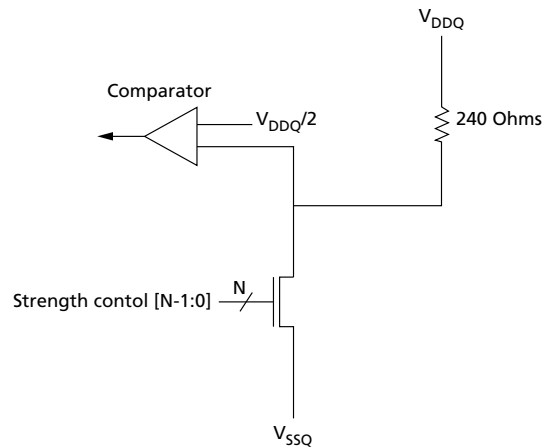
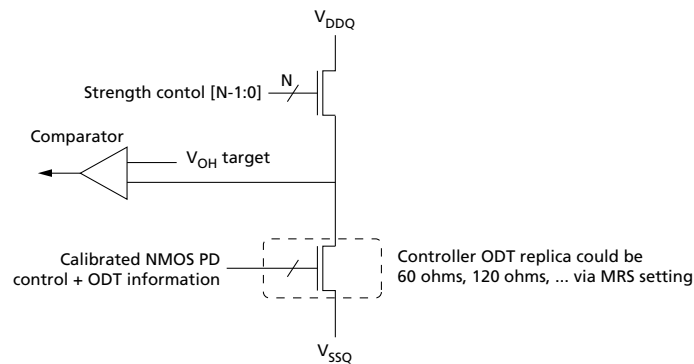
# TN-53-06: LPDDR4/LPDDR4X Point-to-Point Design Guidelines Appendix A

**Figure 21: PCB Stackup Target 50 Ohm (-10%)**



**Figure 22: PCB Stackup Target 50 Ohm (-10%)**



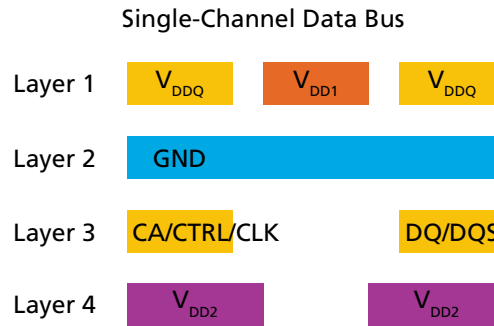

**Figure 23: LVSTL I/O Cell**

**Figure 24: Pull-Down Calibration**

**Figure 25: Pull-Up Calibration**




## Appendix B

For applications where the DQ bus is limited to a single channel x16 configuration, a simpler four-layer PCB routing stack could be possible.

**Figure 26: Example Four-Layer PCB Routing Stack**





## Revision History

### Rev. F – 3/18

- Added eye diagrams in Trace Width (S3) Design Guidelines section
- Additional updates for 4266 operation, trace impedance and length mismatch guidance

### Rev. E – 2/18

- Update for DQ Byte to Byte trace length mismatch guidance

### Rev. D – 12/17

- Updates for 4266 Data rate operation
- Draft removed

### Rev. C – 3/17

- Added training guidelines, incorporated various updates

### Rev. B – 9/15

- Corrected typos and verified Ck/CK# Rtt values still good through additional simulation

### Rev. A – 6/15

- Initial draft release

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