Horizon PCB Review: X2A

dwc_ap_lpddr4x_multiphy_tsmc16ffc18 : LPDDR4/4x,DDR4 at 4266MT/s

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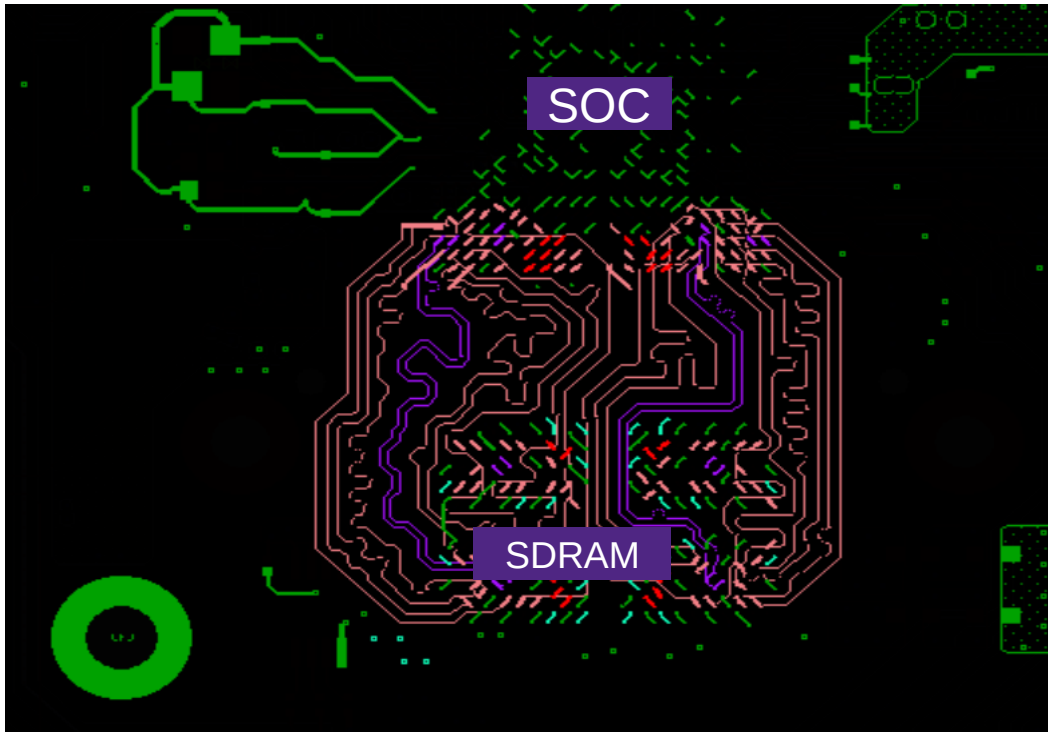
Reference documentation

- Documents used in the review:
  - dwc_lpddr4x_multiphy_signal_integrity_application_note.pdf
  - dwc_ap_lpddr4x_multiphy_tsmc16ffc18_databook.pdf

- Data provided by customer
  - SIPI_review_request_form_from_Horizon_20200320.xlsx
  - X2A CVB PCB Stackup.pptx
  - 1070098-X2AJ2A_CVB_V1_0_pcb.brd
  - 2A-CV-BB-01_V.pdf

Interface Overview

- Signal routing: L03, L05, L08, L10
- SOC, DRAM placement: Top
- Protocols used: LPDDR4/4X, DDR4
- Bus Width: 32b
- Rank: 2
- Data rate : 4266Mbps
- Interface details :
  1. Discrete LPDDR4/LPDDR4x x32 on board or
  2. Discrete DDR4 x16 on board
- List of signals:
  - Dram A/B_Ca[0:5]
  - Dram A/B _Cke 0/1
  - Dram A/B _Ncs0/1
  - Dram A/B _CK_N/P
  - Dram A/B _D[0:15]
  - Dram A/B _DQS[0:1] _P/N
  - Dram A/B _Dm/Dbi[0:1],CS,CKE
- List of Supply nets
  - VDDQ_DDR_1V1, VDDQLP_DDR_0V6/1V1, VDD_DDR_0V8, VAA_DDR, VSS



PCB review

- Stack-up
- Impedance matching
- Spacing guidelines
- Signal spacing
- Signal routing
- Power distribution
- Conclusion

Stack-up

Stackup Information:

Layer	Info	Thickness	MaterialInfo
TOP	==========	0.5+Plating	
	PP TU-87P SLK SP 2113	3.750(mil)	|58
L2	==========	1 Oz	
	Core TU-872 SLK SP 0.1	3.937(mil)	106*2|RTF
L3	==========	1 Oz	
	PP TU-87P SLK SP 2116	4.118(mil)	|57
L4	==========	1 Oz	
	Core TU-872 SLK SP 0.1	3.937(mil)	106*2|RTF
L5	==========	1 Oz	
	PP TU-87P SLK SP 2116	4.118(mil)	|57
L6	==========	1 Oz	
	Core TU-872 SLK SP 0.38	14.961(mil)	2116*3|RTF
L7	==========	1 Oz	
	PP TU-87P SLK SP 2116	4.118(mil)	|57
L8	==========	1 Oz	
	Core TU-872 SLK SP 0.1	3.937(mil)	106*2|RTF
L9	==========	1 Oz	
	PP TU-87P SLK SP 2116	4.118(mil)	|57
L10	==========	1 Oz	
	Core TU-872 SLK SP 0.1	3.937(mil)	106*2|RTF
L11	==========	1 Oz	
	PP TU-87P SLK SP 2113	3.750(mil)	|58
BOT	==========	0.5+Plating	

Finished PCB thickness:	70.866(7.087/-7.087) mil	1.8(+0.18/-0.18) MM

PCB		
Material	Dk	Df
2116	3.24	0.0072
106	2.9	0.0072
Green oil	4	0.026

Stack up looks okay!

Impedance matching

- Signals should have a proper reference plane to define a controlled characteristic impedance and the line impedance should be according to standard requirements
  - For signals within the same group, differential impedance should be twice the impedance of the single-ended ones.
- Signals should have a proper reference plane: routing over plane gaps and/or plane splits should be avoided
  - Impedance mismatches will lead to unwanted reflections.

Spacing guidelines

- Synopsys recommendation for trace spacing is:
  - 2 times the distance to the reference plane, for signals within the same group
  - 3 times the distance to the reference plane, for signals of different groups

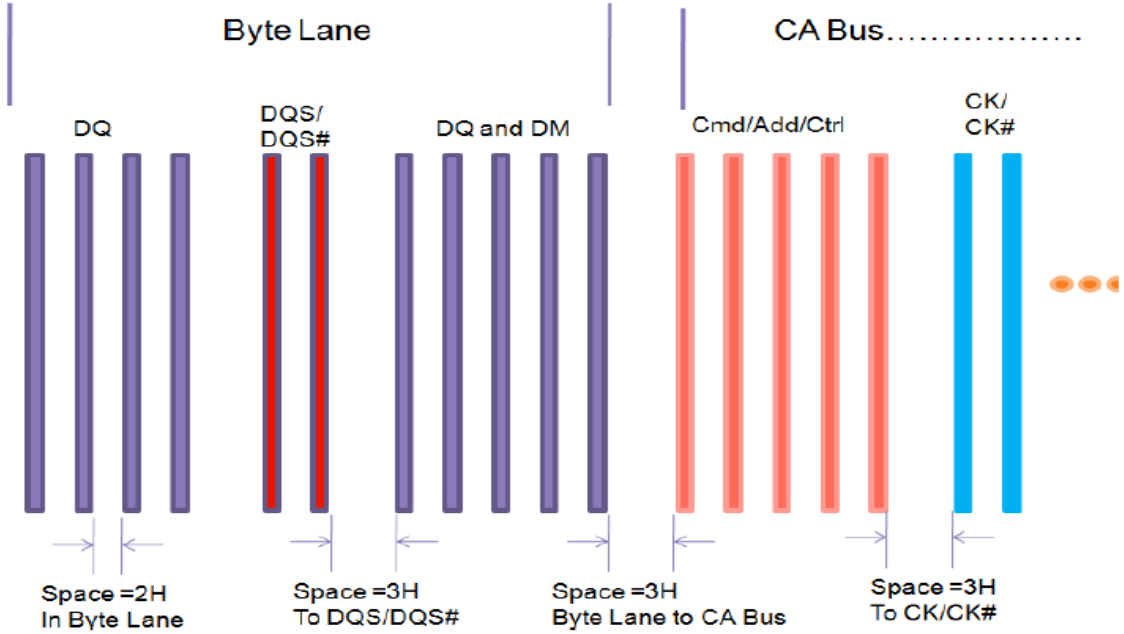


Figure 18: Spacing between Different Signal Groups (Relative to height from reference plane)

Note *If possible, spacing greater that 2H between signals should be used. This will further reduce the impact of crosstalk on timing in microstrip structures. In stripline, however, narrower spacing than 2H may be acceptable as the impact on timing is much reduced since mode velocities are equal.*

Signal spacing

- Guidelines for separation of signals within same group (≥2H) and from different group (≥3H) should be followed
- The signal spacing between DQ and DQS within a byte should also be >=3H
  - Signal Integrity of the signals will be affected due to crosstalk
- H is the distance to closest reference plane
- Based on measured spacing between signals within same group and different groups, Signal Integrity will be affected due to small spacing between traces
- Impact of the crosstalk on the performance of the interface should be confirmed by simulations with extracted model

Signal routing

- Signals should have a proper reference plane: routing over plane gaps and/or plane splits should be avoided. Routing over splits can lead to,
  - Reflections due to impedance mismatches over the splits.
  - Excessive crosstalk due to absence of proper reference.
  - DQ/DQS are double data rate signals and usually have smaller timing margins and it's preferable to route them over the VSS planes where there are no splits.
  - ADD/CMD/CTRL are single rate signals and can have a combination of both VDDQ and VSS layers as reference. Clock also has to be routed on the same layer since it's synchronous with ADD/CMD/CTRL group. However a sign off on this should be done only after simulation run and quantifying whether the impact of the split/noise is acceptable on the eye margins.

Power Distribution Considerations

- The power BGA balls should well distributed around the interface
- There should not be any excessive slotting of the power planes
- Add GND vias next to power vias to minimize loop inductance

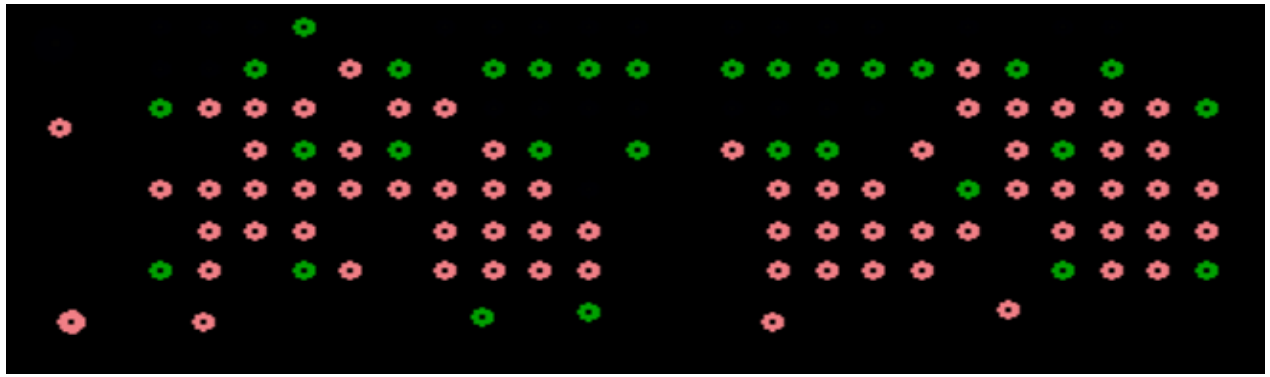
Power vias

- Via count at PHY side
  - VDDQ_DDR_1V1– 6
  - VDDQLP_DDR_0V6/1V1– 2
  - VDD_DDR_0V8 - 11
- The number of Power vias & the distribution plays a vital role to reduce the loop inductance of the PDN network.
- The sufficiency of the power vias need to quantified through the PDN simulations!
- Add GND vias next to power vias to minimize loop inductance

- VDDQ_DDR_1V1–6
- VDDQLP_DDR_0V6/1V1–2
- VDD_DDR_0V8 -11
- GND vias

Reference vias

- The GND vias can be more uniformly distributed around the signal vias to have a proper return path and minimize crosstalk.
- Recommended to prioritize DQ Signal to GND Via distribution.
- Need to run simulations to quantify the impact in the current configuration.



- GND
- DDR Signals [Data & CAA Bus]

Summary

- PI analysis is advised on all Supply nets and it should meet the Synopsys Guideline.
- SNPS has identified potential improvements on the PCB design. However, by visual inspection alone, it is not possible to determine whether the design is robust enough to meet all system specifications

  The design must be signed off based on design extraction, modeling and system level SI/PI simulation

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