Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Enhanced ClearNAND Flash
Palladium Memory Model
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

Enhanced ClearNAND Flash Palladium Memory Models

1. Introduction

The Cadence Palladium Enhanced ClearNAND Flash Models are based on data sheet specifications of the following Micron devices:

MT29FEN Enhanced ClearNAND Flash memory with MLC technology (8GB per die)
MT29FEN Enhanced ClearNAND Flash memory with SLC technology (4GB per die)

Many of the models support both asynchronous and synchronous or DDR interface however some models may support asynchronous interface only. Please check the part number section in the data sheet for more details.

The models are available in several configurations with model sizes to match real devices manufactured by the following vendor: Micron.

Currently only a few different sizes are available, please consult the memory model catalog for the current available list.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations

The following tables list the configurations specified in the data sheets listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

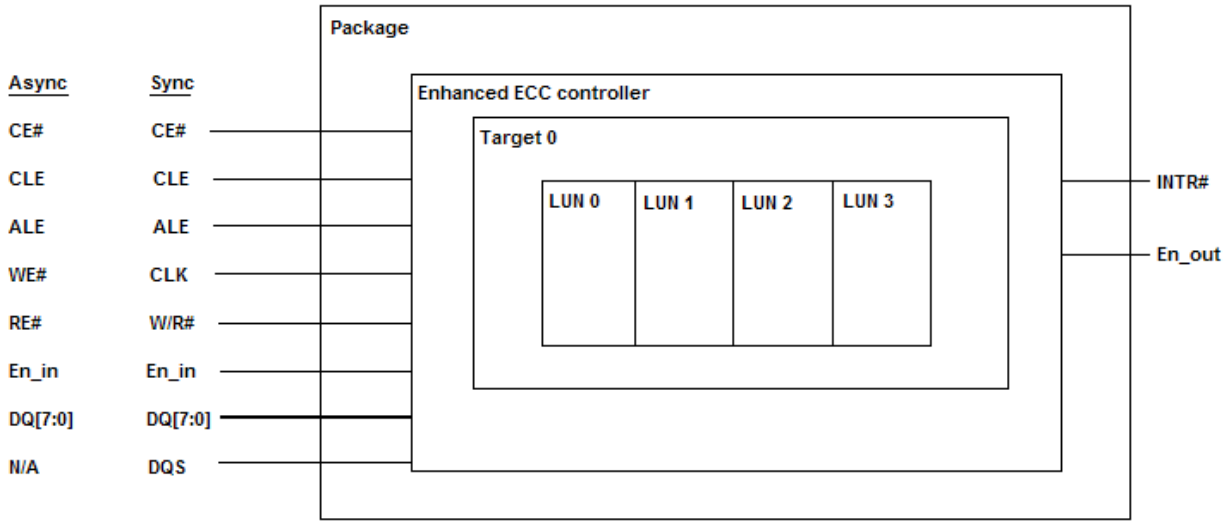
Model	Density	Level	# of Die	# of CE#	I/O	Interface
MT29FEN64GDKBAA	**64GB**	**MLC**	**8**	**1**	**Common**	**Sync/Async**
MT29FEN32GDEBAA	**32GB**	**MLC**	**4**	**1**	**Common**	**Sync/Async**
MT29FEN32GGKBAA	**32GB**	**SLC**	**8**	**1**	**Common**	**Sync/Async**
MT29FEN16GGEBAA	**16GB**	**SLC**	**4**	**1**	**Common**	**Sync/Async**

Notes: MLC = 2bits/cell, 256 pages per block, 4K blocks per die
SLC = 1bit/cell, 128 pages per block, 4K blocks per die
Separate I/O = 2 sets of pins
Common I/O = 1 set of pins
(pin set: ALE,CLE,DQ,DQS,RE#,WE#,INTR#)
Die and LUN are used interchangeably
Target and CE# are used interchangeably
Synchronous, DDR, and perhaps Toggle may refer to the same interface
Enhanced ClearNAND models have 8KB (8192+128 bytes) per page

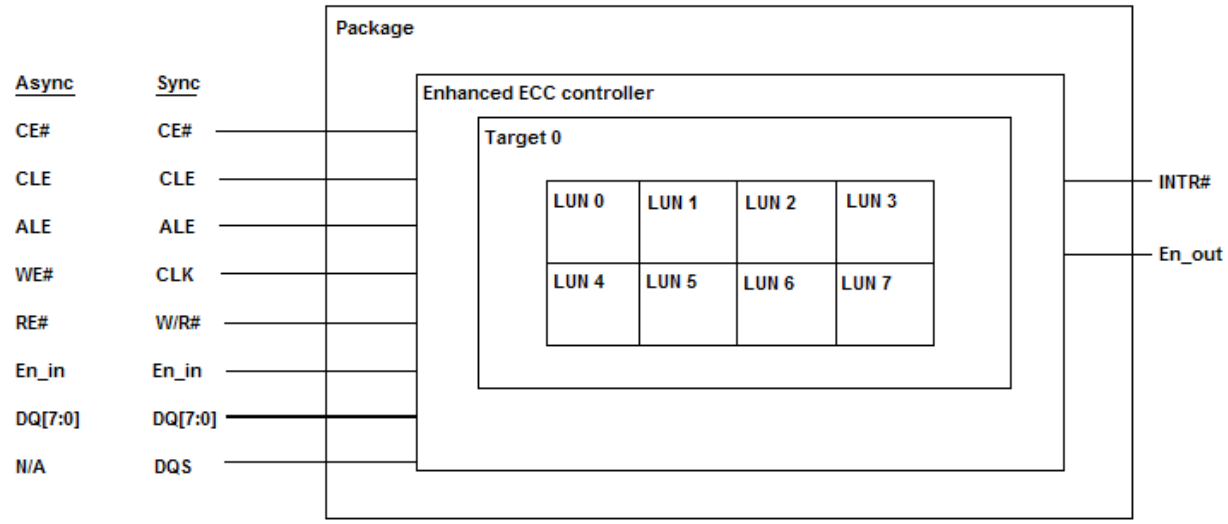
4. Model Block Diagram

These models are implemented modularly based on the LUN core, which is instantiated as many times as needed within each model. The user does not need to instantiate the core directly. The user instantiate the model based on the model's number of dies.

A block diagram of a model that has 4 dies or LUNs is shown below.



The following block diagram shows a model that has 8 LUNs.



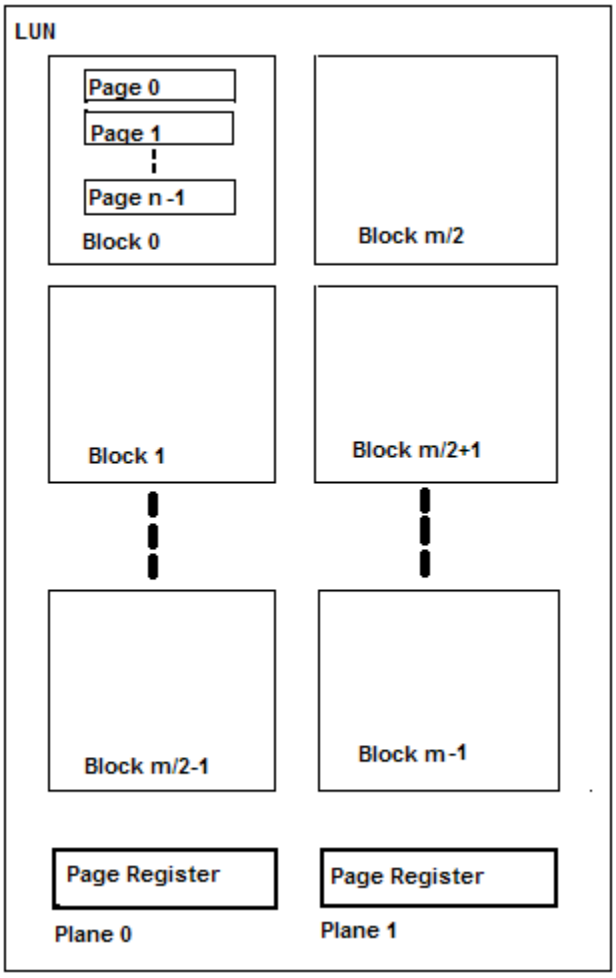
5. Address mapping

The array of the Enhanced ClearNAND Flash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The mapping of lun, block, page and column addresses to the internal model array is as follows:

ARRAY_ADDR = { LA, BA, PA, CA}

This information is required if the memory needs to be preloaded with user data. Here are the array organization and addressing cycle table for MLC models, followed by SLC models. Note that SLC models have one less page address bit.

Array Organization for MLC Array



1 page = (8K + 128 bytes)

1 block = (8K + 128) bytes x 256 pages
= (2048K + 32K) bytes

1 plane = (2048K + 32K) bytes x 2048 blocks
= 33,280Mb

1 LUN = 33,280Mb x 2 planes
= 66,560Mb

MLC Array Organization Per Logical Unit (LUN)

Address Cycle Table for MLC Array

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LA3	LA2	LA1	LA0	BA19	BA18	BA17	BA16

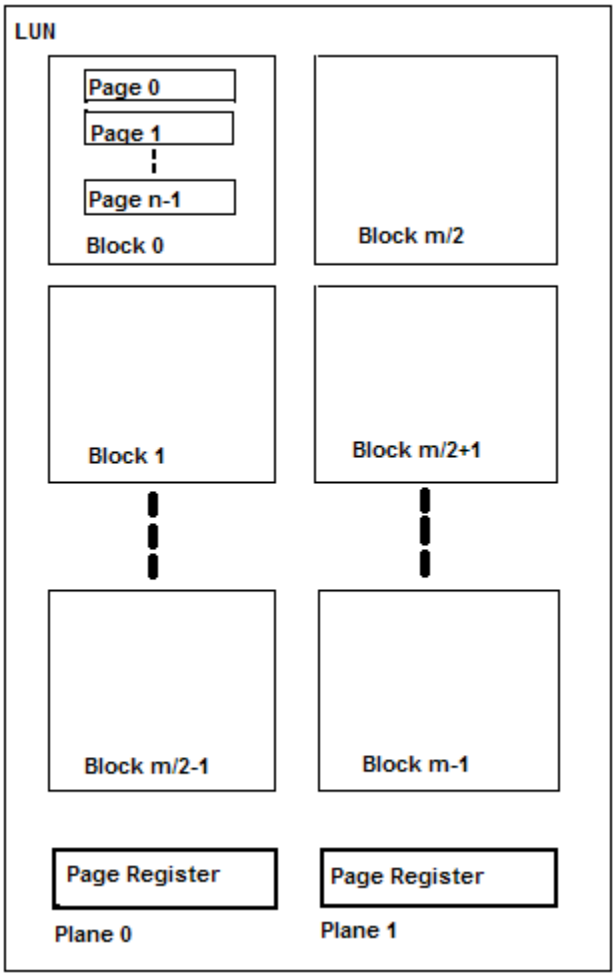
Notes from Micron data sheet:
CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

Column addresses 8320 (2080h) through 16383 (3FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

BA[19] is the plane-select bit:
Plane 0: BA[19] = 0
Plane 1: BA[19] = 1

Array Organization for SLC Array



1 page = (8K + 128 bytes)

1 block = (8K + 128) bytes x 128 pages
= (1024K + 16K) bytes

1 plane = (1024K + 16K) bytes x 2048 blocks
= 16,640Mb

1 LUN = 16,640Mb x 2 planes
= 33,280Mb

SLC Array Organization for Logical Unit (LUN)

Address Cycle Table for SLC Array

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LA2	LA1	LA0	BA18	BA17	BA16

Notes from Micron data sheet:
CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

Column addresses 8320 (2080h) through 16383 (3FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

BA[18] is the plane-select bit:
Plane 0: BA[18] = 0
Plane 1: BA[18] = 1

6. Feature Address Definitions

In the Enhanced ClearNAND Flash data sheets there are up to 256 feature addresses defined – a 256 x 32 array. The Palladium models implement the entire array. However the only features that can be activated is the synchronous interface and volume address. Other addresses can be written to and read back using the Set and Get Feature commands but the set features will not be active. For example timing mode change and OTP are not supported. The following table shows the feature address definitions as described in the Micron data sheet.

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h-0Fh	Reserved
10h	Programmable output drive strength
11h-20h	Reserved
21h	Appoint volume address
22h-7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable INTR# pull-down strength
82h-98h	Reserved
99h	Controller Auto Sleep
9Bh-FFh	Reserved

7. ID Operations

7.1. READ ID

The READ ID parameters for addresses 00h and 20h have been hardcoded into each model. Therefore user data file is not required.

7.2. READ PARAMETER PAGE

The data for the parameter page is provided in the <model_name>x<package_code>_param.dat file. The package_code is two characters. This data file should be preloaded into the model if the user wants to read ONFI information from the model. The path to each model's parameter page is as follows:

<path.to.model.inst>.param_page

7.3. READ UNIQUE ID

The READ UNIQUE ID command is used to read a unique identifier programmed into the target. Preloading the uid_page is similar to preloading the param_page mentioned in the previous section. The path to each model's unique id page is as follows:

<path.to.model.inst>.uid_page

8. Commands

The NAND flash model accepts the following commands:

- Reset
- Synchronous Reset
- Reset LUN
- Volume Select
- Read ID
- Read Parameter Page
- Read Unique ID
- Get Feature
- Set Feature
- Legacy Status
- LUN Status
- Device Status
- Get Next Operation Status
- Operation Status
- Queue Page Read
- Page Read
- Read Mode
- Program Page
- Program Page Delayed
- Program Page Pause
- Program Page Resume
- Change Write Column
- Change Row Address
- Erase Block
- Erase Block Multi-Plane
- Copyback Read
- Copyback Program
- Change Read Column

The following table shows the command set as described in the Micron data sheet.

Command	Com-mand Cycle #1	Fields in Address	# of Valid Address Cycles	Data Input Cycles	Command Cycle #2	INTR# Pulse Generated?	Notes
Reset Commands							
RESET	FFh	-	0	-	-	Yes	
SYNCHRONOUS RESET	FCh	-	0	-	-	Yes	
RESET LUN	FAh	Row	3	-	-	Yes	
Identification Commands							
VOLUME SELECT	E1h	Volume address	1	-	-	No	
READ ID	90h	00h or 20h	1	-	-	No	3
READ PARAMETER PAGE	ECh	00h	1	-	-	Yes	3
READ UNIQUE ID	EDh	LUN	1	-	-	Yes	3
Configuration Commands							
GET FEATURES	EEh	Feature address	1	-	-	Yes	3
SET FEATURES	EFh	Feature address	1	4	-	Yes	3
Status Commands							
LEGACY STATUS	70h	-	0	-	-	No	4
LUN STATUS	71h	Row	3	-	-	No	
DEVICE STATUS	72h	-	0	-	-	No	
GET NEXT OPERATION STATUS	77h	Row	3	-	-	No	
OPERATION STATUS	7Dh	-	0	-	-	No	
Read Commands							
QUEUE PAGE READ	07h	Row or Column ,Row, Length	3 or 7	-	37h	Yes	5
PAGE READ	00h	Column , Row	5	30h	30h-	Yes	
READ MODE	00h or 7Ah	-	-	-	-	No	
Program Commands							
PROGRAM PAGE	80h	Row	Yes	10h		Yes	6
PROGRAM PAGE DELAYED	80h	Row	Yes	11h		Yes	6
PROGRAM PAGE PAUSE	85h / 80h	Column or Row	2 or 3	Optional	13h	No	
PROGRAM PAGE RESUME	85h	Column	2	Optional	10h/11h/ 13h	Yes	7
CHANGE WRITE COLUMN	85h	Column	2	Optional	10h/11h	No	7
CHANGE ROW ADDRESS	85h	Column , Row	5	Optional	10h/11h	No	7
Erase Commands							
ERASE BLOCK	60h	Row	3	-	D0h	Yes	
ERASE BLOCK MULTI-PLANE	60h	Row	3	-	D1h	Yes	
Copyback Commands							
COPYBACK READ	00h	Column , Row	5	-	35h	Yes	
COPYBACK PROGRAM	85h	Column , Row	5	-	10h	Yes	6
CHANGE READ COLUMN	05H	Column	2	-	E0h	No	
CHANGE WRITE COLUMN	85h	Column	2	Yes	-	No	

Notes from Micron data sheet:

1. No new command can be accepted while RESET/SYNCHRONOUS RESET, or device identification/configuration commands are in progress.
2. Only one command can be queued by the device at any given time for an identical row address. Check LUN status prior to issuing program or copyback commands.
3. Valid only if no commands that require row addresses are pending (that is, commands that require 3-, 5-, 7-byte addresses).

4. LEGACY STATUS (70h) is only valid following or in conjunction with RESET (FFh), SYNCHRONOUS RESET (FCh), GET FEATURE (EEh), and SET FEATURE (EFh) commands. LEGACY STATUS (70h) is required as the first command issued after the initial RESET (FFh) command in order to configure device DQ pinout.
5. Use 7-address cycle for partial-page reads.
6. Issuing too few address cycles during a program operation will cause device to suspend the device and will require a new program operation or FFh command to resume device operation. If this command must be aborted by the host, the only command allowed is RESET (FFh).
7. 85h command will not produce INTR# pulse, though INTR# will pulse upon array program operation completion following the 10h or 11h confirm command.

9. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compilation. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64 +sv -ua +dut+<model_name> \
    ./<model_name>.vp \
    ./ecn_8.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis:

```
1)
hdlInputFile <model_name>.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog <model_name>.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
<model_name>
……

2)
vavlog <model_name>.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog <model_name>.vg
<model_name>
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations which are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

10. Initialization Sequence

The Enhanced ClearNAND Flash model requires that the memory controller or host follows the initialization sequence as documented in the specification. The sequence basically entails the following steps.

For Single Volume (one package per CE# or target):

1. The asynchronous interface is active by default for each target.
2. The RESET (FFh) command must be the first command issued to the target (CE#). The target will become busy. The RESET busy time can be monitored with the INTR# pin or checked by polling the status register with the 70h status command.
3. Read configuration data from the model using READ ID, READ PARAMETER PAGE, etc.
4. The model is now initialized and ready for normal operation.

For Volume Addressing (multiple packages per CE# or target):

1. The asynchronous interface is active by default for each target.
2. Only the first volume or device will be enabled to accept commands.
3. The RESET (FFh) command must be the first command issued to the enabled volume. The target will become busy. The RESET busy time can be monitored with the INTR# pin or checked by polling the status register with the 70h status command.
4. Read configuration data from the model using READ ID, READ PARAMETER PAGE, etc.
5. Appoint the device volume address with the appoint volume address SET FEATURE (EFh) command sequence. Wait for the completion by monitoring the INTR# pulse.
6. The first volume is now initialized and ready for normal operation. The volume En_out signal will drive HIGH to enable the next volume in the chain. Repeat steps 3 through 5 for the remaining volumes.
7. After all volumes on the target have an appointed volume address, set CE# HIGH. To enable a select volume use the VOLUME SELECT (E1h) command; else, all volumes will remain deselected.

The model requires that these steps are performed in the correct sequence in order to complete initialization. The model will not respond to any others commands unless this sequence is completed.

11. Model Size

To reduce memory utilization each LUN has only 32 blocks (blocks 0 to 15 in plane 0, blocks 2048 to 2063 in plane 1) but the actual device has 4096 blocks. If larger size is needed please contact Customer Support.

12. Limitations

1. Set Feature command supports activating synchronous mode and appointing volume address only.
2. Mirrored DQ pinout configuration is not supported.
3. Pause during copyback is not supported.
4. ECC is not supported.
5. Model does not check illegal sequence of command cycles.
6. Model does not check for attempts to program a bit to 1, user should make sure the block is erased before program.
7. Model does not support timing parameters, except tRHOH.
8. The time to program a page or erase a block is 1 fclk (fast clock) per address location.

13. Timing Parameter tRHOH

The model does not generally support timing parameters because it is cycle based. However tRHOH (an asynchronous mode parameter that controls RE# HIGH to output hold) is supported in number of fclks (fast clocks). The user may define a macro at compile time to hold the data by a number of fclks after RE# goes high. Use this macro only if data output is not already held long enough. The model holds the data valid for 2 fclks by default. The data can be held 3 additional fclks by using the following example command line option in ixcom flow:

```
vlan +define+tRHOH=3
```

14. Revision History

The following table shows the revision history for this document

Date	Version	Revision
March 2012	1.0	Initial Version
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.3	Remove emulation capacity info. Update related publications list.
March 2015	1.4	Add timing parameter limitation and a section on tRHOH.
July 2015	1.5	Update Cadence naming on front page
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming. Remove BETA watermark.
January 2018	1.8	Modify header and footer
July 2018	1.9	Update for new utility library