Journey 3
DDR4 & LPDDR4/4X
Board Design & Layout Guideline

Rev. 1.1

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
0.1	2020/12/20	Initial draft
1.0	2020/12/22	Initial release and Add: 1) 4.4 SI Simulation Topology 2) 4.6 Specification for SI Simulation (LPDDR4-3200)
1.1	2021/01/12	Add Appendix B Add 2.1.3 Dram Power Supply

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1 Overview

The Journey 3 SOC supports the DDR4/LPDDR4/4X memory interface. Customer board designs should follow the design rules depicted in this application note to ensure extreme memory bandwidth demanded by heavy AI oriented computing.

2 Interface Schematics

This section describes the basic signal connections between the Journey 3 SOC and memory.

2.1 DDR Signal Definition

2.1.1 Address/Command/Data Signal Definition

Journey 3 supports 32bit width data lines. Signals for DDR4/LPDDR4/LPDDR4X are multiplexed. The following table depicts the DDR interface signal multiplexing.

Table 2-1 Journey 3 DDR Ball Multiplexing

BALL NAME	Signal		
	DDR4	LPDDR4	LPDDR4x
BP_D0	DQ[0]	DQ[0]	DQ[0]
BP_D1	DQ[1]	DQ[1]	DQ[1]
BP_D2	DQ[2]	DQ[2]	DQ[2]
BP_D3	DQ[3]	DQ[3]	DQ[3]
BP_D4	DQ[4]	DQ[4]	DQ[4]
BP_D5	DQ[5]	DQ[5]	DQ[5]
BP_D6	DQ[6]	DQ[6]	DQ[6]
BP_D7	DQ[7]	DQ[7]	DQ[7]
BP_D8	DM[0]	DM[0]	DM[0]
BP_D9	DQS_T[0]	DQS_T[0]	DQS_T[0]
BP_D10	DQS_C[0]	DQS_C[0]	DQS_C[0]
BP_D12	DQ[8]	DQ[8]	DQ[8]
BP_D13	DQ[9]	DQ[9]	DQ[9]
BP_D14	DQ[10]	DQ[10]	DQ[10]
BP_D15	DQ[11]	DQ[11]	DQ[11]
BP_D16	DQ[12]	DQ[12]	DQ[12]
BP_D17	DQ[13]	DQ[13]	DQ[13]
BP_D18	DQ[14]	DQ[14]	DQ[14]
BP_D19	DQ[15]	DQ[15]	DQ[15]
BP_D20	DM[1]	DM[1]	DM[1]
BP_D21	DQS_T[1]	DQS_T[1]	DQS_T[1]

BALL NAME	Signal		
	DDR4	LPDDR4	LPDDR4x
BP_D22	DQS_C[1]	DQS_C[1]	DQS_C[1]
BP_D24	DQ[16]	DQ[16]	DQ[16]
BP_D25	DQ[17]	DQ[17]	DQ[17]
BP_D26	DQ[18]	DQ[18]	DQ[18]
BP_D27	DQ[19]	DQ[19]	DQ[19]
BP_D28	DQ[20]	DQ[20]	DQ[20]
BP_D29	DQ[21]	DQ[21]	DQ[21]
BP_D30	DQ[22]	DQ[22]	DQ[22]
BP_D31	DQ[23]	DQ[23]	DQ[23]
BP_D32	DM[2]	DM[2]	DM[2]
BP_D33	DQS_T[2]	DQS_T[2]	DQS_T[2]
BP_D34	DQS_C[2]	DQS_C[2]	DQS_C[2]
BP_D36	DQ[24]	DQ[24]	DQ[24]
BP_D37	DQ[25]	DQ[25]	DQ[25]
BP_D38	DQ[26]	DQ[26]	DQ[26]
BP_D39	DQ[27]	DQ[27]	DQ[27]
BP_D40	DQ[28]	DQ[28]	DQ[28]
BP_D41	DQ[29]	DQ[29]	DQ[29]
BP_D42	DQ[30]	DQ[30]	DQ[30]
BP_D43	DQ[31]	DQ[31]	DQ[31]
BP_D44	DM[3]	DM[3]	DM[3]
BP_D45	DQS_T[3]	DQS_T[3]	DQS_T[3]
BP_D46	DQS_C[3]	DQS_C[3]	DQS_C[3]
BP_A0	CKE0	CKEA0	CKEA0
BP_A1	CKE1	CKEA1	CKEA1
BP_A2	CS_N0	CSA0	CSA0
BP_A3	N/A	CSA1	CSA1
BP_A4	BG0	CLKA_T	CLKA_T
BP_A5	BG1	CLKA_C	CLKA_C
BP_A6	ACT_N	N/A	N/A
BP_A7	A9	N/A	N/A
BP_A8	A12	CAA0	CAA0
BP_A9	A11	CAA1	CAA1
BP_A10	A7	CAA2	CAA2
BP_A11	A8	CAA3	CAA3
BP_A12	A6	CAA4	CAA4
BP_A13	A5	CAA5	CAA5
BP_A14	A4	N/A	N/A
BP_A15	A3	N/A	N/A

BALL NAME	Signal		
	DDR4	LPDDR4	LPDDR4x
BP_A16	CLK0_T	N/A	N/A
BP_A17	CLK0_C	N/A	N/A
BP_A20	CLK1_T	CKEB0	CKEB0
BP_A21	CLK1_C	CKEB1	CKEB1
BP_A22	N/A	CSB1	CSB1
BP_A23	N/A	CSB0	CSB0
BP_A24	A2	CLKB_T	CLKB_T
BP_A25	A1	CLKB_C	CLKB_C
BP_A26	BA1	N/A	N/A
BP_A27	PAR	N/A	N/A
BP_A28	A13	CAB0	CAB0
BP_A29	BA0	CAB1	CAB1
BP_A30	A10	CAB2	CAB2
BP_A31	A0	CAB3	CAB3
BP_A32	N/A	CAB4	CAB4
BP_A33	CAS_N	CAB5	CAB5
BP_A34	WE_N	N/A	N/A
BP_A35	RAS_N	N/A	N/A
BP_A36	ODT0	N/A	N/A
BP_A37	ODT1	N/A	N/A
BP_A38	CS_N1	N/A	N/A

2.1.2 J3 Power Supply

Table 2-2 depicts the basic parameters of power rails needed by the Journey 3's DDR PHY and controller.

Table 2-2 Journey 3 DDR Interface Power Supply

Ball Name	Description	Min.	Typ.	Max.	Unit	ramp rate	Note
VDDQ_DDR	DDR4 IO domain power	1.164	1.2	1.236	V	<5mV/us	1,2
	LPDDR4/4X IO domain power	1.067	1.1	1.133	V	<5mV/us	2
VDDQLP_DDR	LPDDR4X IO domain Power.	0.582	0.6	0.63	V	<5mV/us	1,2
VDD_DDR	DDR Controller & PHY core power	0.776	0.8	0.84	V	<18mV/us	2
VAA_DDR	DDR PHY internal PLL analog power	1.746	1.8	1.89	V	<5mV/us	2

Note:

1. When in DDR4&LPDDR4 mode design, VDDQLP_DDR should be tied together with VDDQ_DDR and supplied by the same DCDC power supply.
2. The maximum ramp up rate of DDR power supply should be within the limit listed in Table 2-2.
3. Please refer to the HW Design Guide for the power on/off sequence of J3.

2.1.3 DRAM Power Supply

LPDDR4 has 3 power supplies: VDD1 (1.8V), VDD2 (1.1V), VDDQ (1.1V). Special consideration is needed for power on/off sequence. The following requirement is extracted from Dram datasheet.

Voltage ramp

While applying power after Ta, VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table 2-3 LPDDR4 Power Ramp Sequence

After…	Applicable conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Note: Ta is the point when any power supply firstly reaches 300mV.

Power-Off Sequence

Table 2-4 LPDDR4 Power Off Sequence

Between…	Applicable conditions
Tx and Tz	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Note:

1. Tx is the point where any power supply drops below the minimum value specified in the minimum DC Operating Condition.
2. Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

2.1.4 Other Signals

There are several other signals needed for DDR interface as depicted in Table 2-5.

Table 2-5 Journey 3 other signals for DDR

Ball Name	Description	Note
BP_MEMRESET_L	DRAM reset signal, connect to DRAM.	
BP_ZN	Calibration external reference resistor, connect a 120Ω %1	

	resistor from this signal to ground	
BP_VREF	Voltage reference for receivers and analog test point for debug	
BP_ALERT_N	DDR4 Alert, used only in DDR4 mode	

2.2 LPDDR4 Interface Schematics

The signal connections for LPDDR4 interface should follow the following figure.

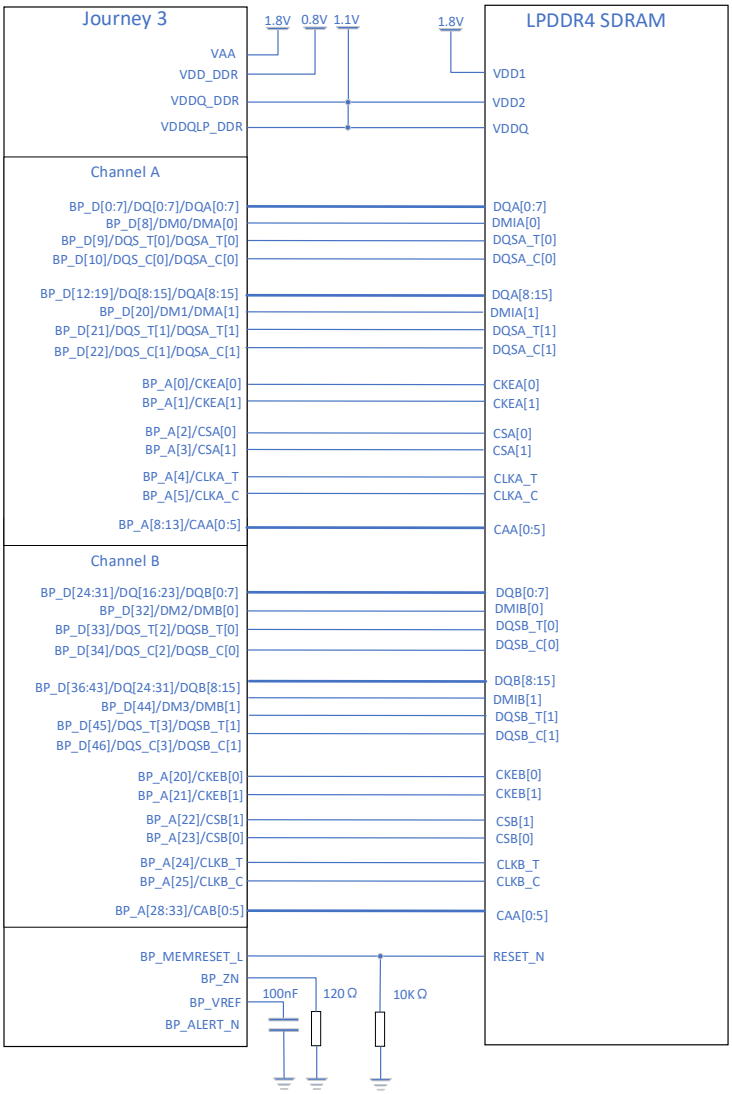


Figure 2-1 Journey 3 LPDDR4 Connection

Note:

1. DQ signals could be swapped within the same DQ byte group.
2. The whole byte group could be swapped with each other.
3. It is strongly suggested to follow the DQ map of reference design 2A-DV-SM-02C (J3 SOM LPDDR4) to save the extra software effort.
4. Power supply decaps are not shown in this figure, please refer to the PCB layout section.
5. Externally BP_VREF on PCB is not needed, and Vref is generated internally in J3.
6. A 120 Ohm +/-1% resistor should be connected from BP_ZN to ground for calibration.

2.3 LPDDR4X Interface Schematics

The signal connections for LPDDR4X interface should follow the following figure. It is almost the same connection as LPDDR4 except that the Journey 3 VDDQLP_DDR and memory's VDDQ should connect to 0.6V.

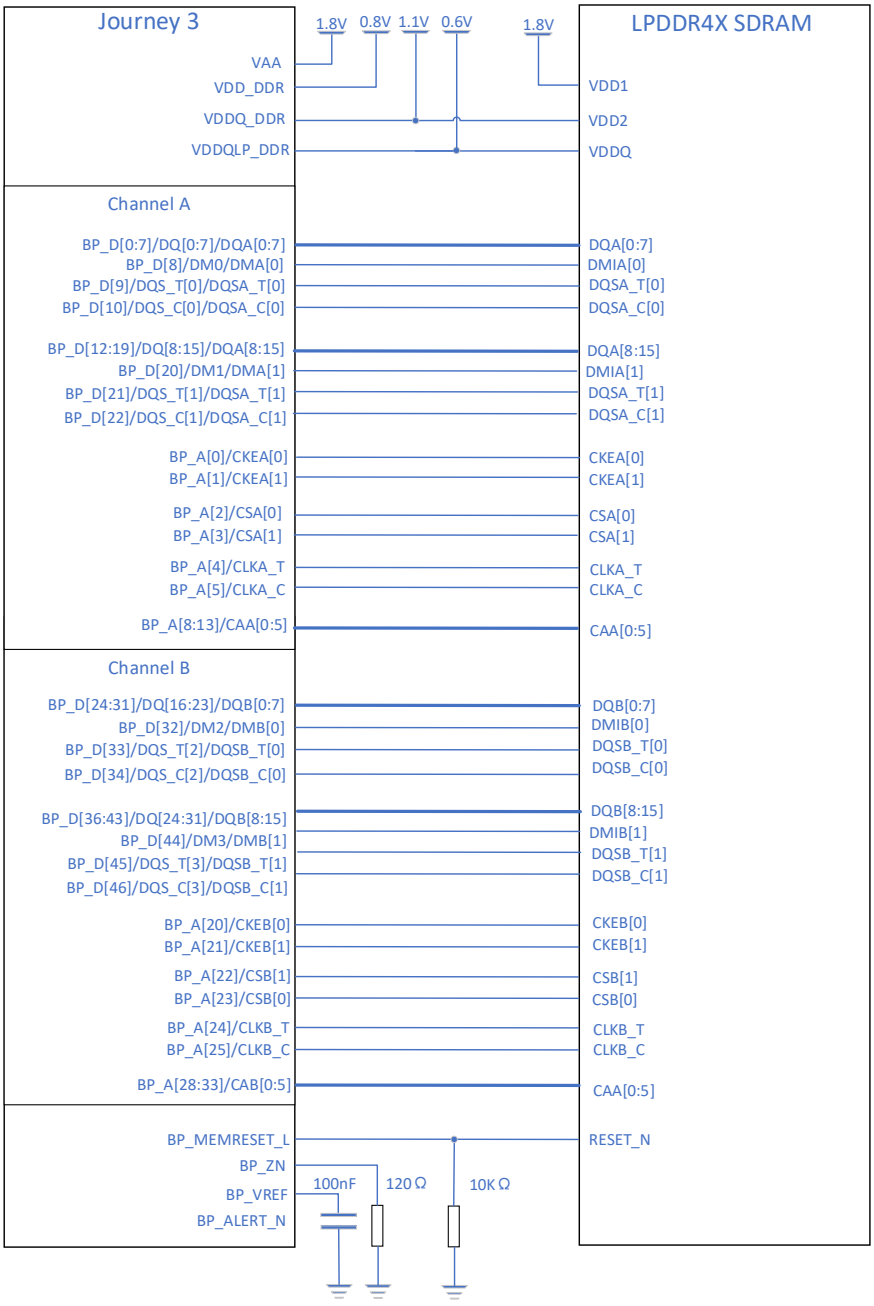


Figure 2-2 Journey 3 LPDDR4X Connection

2.4 DDR4 Interface Schematics

Journey 3 also supports DDR4 memory, and the signals for DDR4 are multiplexed with LPDDR4/4X signals. 2 pieces of 16 bit width DDR4 memory are needed to match Journey 3's 32bit-width DDR4 interface.

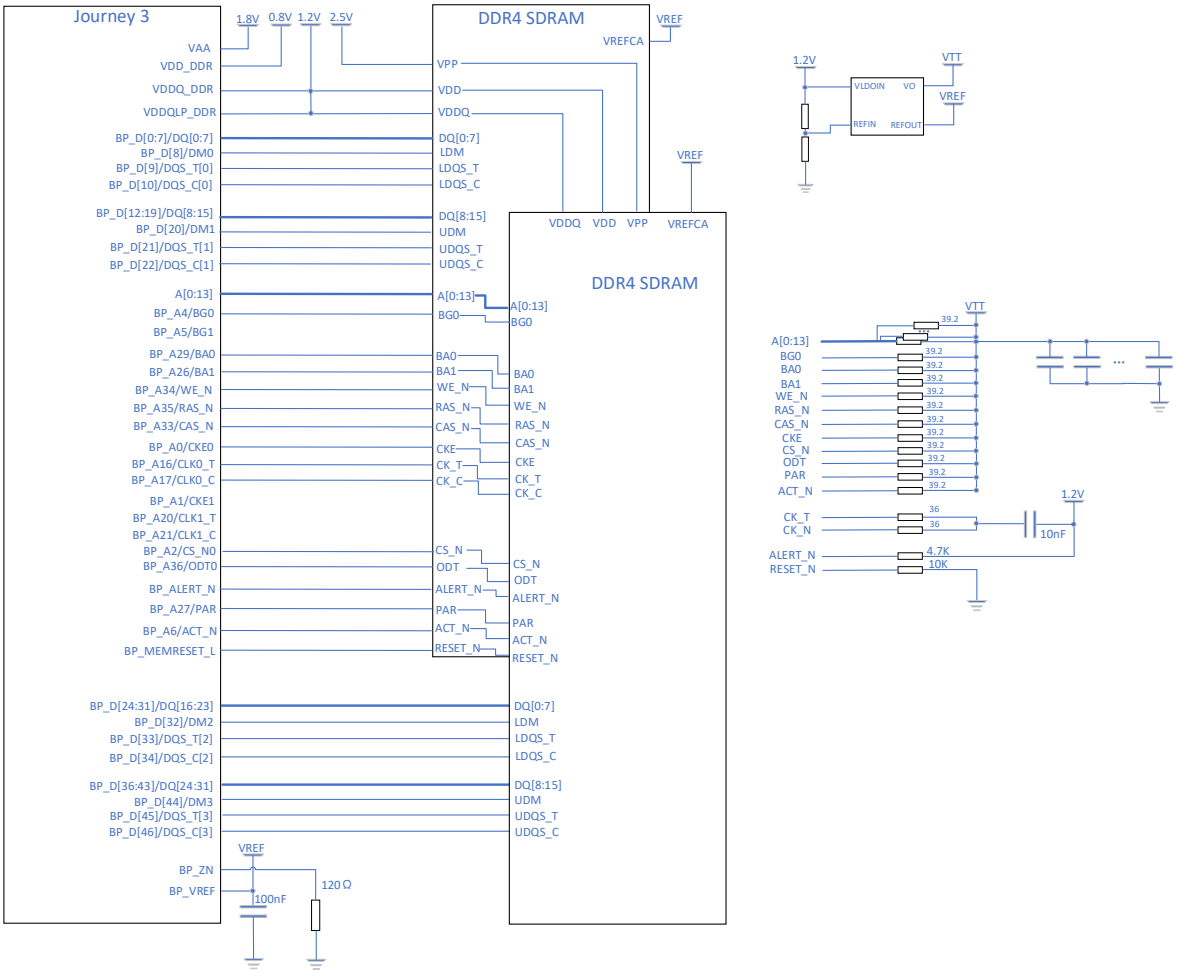


Figure 2-3 Journey 3 DDR4 Connection

1. DQ signals could be swapped within the same DQ byte group.
2. The whole byte group could be swapped with each other.
3. It is strongly suggested to follow the DQ map of reference design 2A-DV-SM-02B (J3 SOM DDR4) to save the extra software effort.
4. Power supply decaps are not shown in this figure, please refer to the PCB layout section.
5. A 120 Ohm +/-1% resistor should be connected from BP_ZN to ground for calibration.
6. Use 36Ω resistor & 10nF capacitor RC termination for differential clock.
7. Use 39Ω pulling up resistor to VTT for all address & command signals.

3 PCB layout guide

3.1 PCB Stackup

A 8-layer board stackup is shown in this section. The goal is to provide with the customers a reasonable trade-off between signal integrity vs. cost. The stackup are driven by DDR routing requirements, other high-speed IO routing requirements and power delivery network. PCBA made with higher class materials, well balanced stripline signal layers, and careful routing typically produce a higher performance of DDR data rate with enough margin.

Implementation must ensure that the DDR memory bus and other high speed IO signals are not referenced to power but ground planes, especially the 12V power plane and the plane with high di/dt transient, which will couple noise onto the signals. Dual stripline routing is not recommended, as crosstalk can increase the chance of errors on high speed buses. The constrains of the trace width is dependent on factors such as the board stackup, associated dielectric parameters and copper thickness, required impedance, and required current (for power traces). The stackup also determines the constraints for routing and spacing. Consider the following points when design the stackup and selecting board material:

- Preplan impedance of critical traces and the routing space;
- High-speed signals must have reference to clean planes on adjacent layers to minimize crosstalk;
- PCB material used in reference stackup is IT180/IT180A, customer board should use at least better material with lower DK/DF.

The Journey 3 8-Layers reference stackup as shown in the table below.

Table 3-1 Reference PCB Stackup 8 Layers

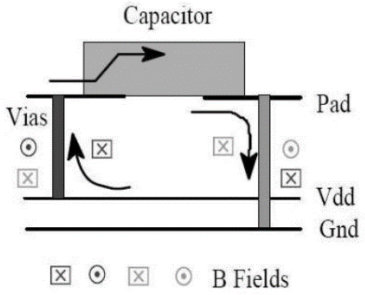
Subclass Name	Type	Thickness (Mil)	Cu (Oz)	Dielectric Constant	Ref Plane
	Solder Mask	0.5		4	
Top	Signal	1.9	1/3+Plating		L2
	Prepreg	2.76		4.11	
L2	Plane	1.2	1		
	Core	4.33		4.33	
L3	Signal	1.2	1		L2&L4
	Prepreg	7.06		4.34	
L4	Plane	1.2	1		
	Core	20.07		4.58	
L5	Plane	1.2	1		
	Prepreg	7.06		4.34	
L6	Signal	1.2	1		L5&L7
	Core	4.33		4.33	
L7	Plane	1.2	1		
	Prepreg	2.76		4.11	
Bottom	Signal	1.9	1/3+Plating		L7
	Solder Mask	0.5		4	

The PCB factory needs to control the impedance during the manufacturing process. Microstrip impedance tolerance is generally controlled within ±15%, and need to be more strictly controlled to 10% for critical high speed differential signals. Stripline impedance tolerance is generally controlled within ±10%.

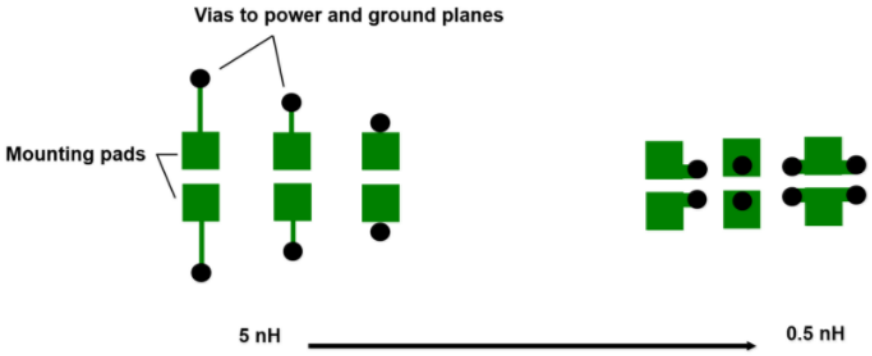
Taking into account the trace topology and the link's condition, the material of the reference stackup is FR4 with RTF copper foil. If the customer's topology is more complex, a higher class of material can be selected. Furthermore, temperature and humidity have a great impact on the material and different PCB material may have different temperature/humidity sensitivities. Check with PCB supplier or material vendor to figure out the impact and evaluate the design risk.

3.2 Power Supply Decaps

To increase the effectiveness of capacitors, the parasitic inductance of capacitor fan-out trace must be minimized. Parasitic inductance is mostly in the pad and via structure and inductance is minimized by minimizing the area of the current loop.



Different capacitor PCB footprints have different loop area and the resulting mounting inductance. Via-in-pad method has smallest inductance and become more popular in nowadays application. We strongly recommend via-in-pad design for DDR application.



Furthermore, place decoupling caps on the top layer and use higher layer in the PCB stackup for power planes to which connect the decoupling cap's power vias. This further reduce inductance again by minimizing loop area of the power network.

3.2.1 VDD_DDR

The recommended decoupling capacitors' combination for VDD_DDR is (10uF x 1 + 4.7uF x 1 + 1uF x 1 + 100nF x 2 + 4.7nF x 2 + 3.3nF x 1). Place these capacitors close to J3's power balls.

CAUTION: Table 3-2 shows the recommended decoupling capacitors part numbers for VDD_DDR. Capacitors with value below 1uF should have higher priority to be placed as close as possible to the J3's balls.

Table 3-2 Decoupling Capacitors for VDD_DDR

Quantity	Capacitance	Part Number
1	10uF	GCM188D70J106ME36#
1	1uF	GRT033C81A105ME13#
2	100nF	GRT033C81A104KE01#
2	4.7nF	GCM033R71A472KA03#
1	3.3nF	GCM033R71A332KA03#

3.2.2 VDDQ_DDR

The recommended decoupling capacitor combination of the VDDQ_DDR power domain is (10uF x 1 + 1uF x 7 + 10nF x 1 + 3.3nF x 3 + 2.2nF x 2 + 1.5nF x 2 + 1.2nF x 1). Place these capacitors close to J3's power balls.

CAUTION: Table 3-3 shows the recommended decoupling capacitors for VDDQ_DDR. Capacitors below 1uF should have higher priority to be placed as close as possible to J3's balls.

Table 3-3 Decoupling Capacitors for VDDQ_DDR

Quantity	Capacitance	Part Number
1	10uF	GCM188D70J106ME36#
7	1uF	GRT033C81A105ME13#
1	10nF	GCM033R71A103KA03#
3	3.3nF	GCM033R71A332KA03#
2	2.2nF	GCM033R71E222KE02#
2	1.5nF	GCM033R71E152KA03#
1	1.2nF	GCM033R71E122KA03#

3.2.3 VDDQLP_DDR

The decoupling capacitor combination of the VDDQLP power domain is (10uF x 1 + 1uF x 1 + 100nF x 1 + 3.3nF x 1 + 2.2nF x 1 + 1.5nF x 4 + 1.2nF x 2). Place these capacitors close to their corresponding pins. The smaller capacitors (1.2nF, 1.5nF, 2.2nF, 3.3nF, and 100nF) should be located closer to the chip.

CAUTION: Table 3-4 shows the recommended decoupling capacitors for VDDQLP_DDR. The capacitors below 1uF should be placed as close as possible to the balls.

Table 3-4 Filtering Capacitors for VDDQLP_DDR

Quantity	Capacitance	Part Number
1	10uF	GCM188D70J106ME36#
1	1uF	GRT033C81A105ME13#
1	100nF	GRT033C81A104KE01#
1	3.3nF	GCM033R71A332KA03#
1	2.2nF	GCM033R71E222KE02#
4	1.5nF	GCM033R71E152KA03#
2	1.2nF	GCM033R71E122KA03#

3.2.4 VAA

The decoupling capacitor combination of the VAA power domain is (10uF x 1 + 1uF x 1 + 100nF x 1). Place these capacitors close to the pin T17. The smaller capacitor (100nF) should be located closer to the chip.

Note: refer to Appendix B for special consideration of power decaps placement.

3.3 Digital signals layout

The section describes the J3 DDR signal layout rules. These rules should be followed to ensure a robust design at high data rate under different loading conditions.

Considering the signal routing from the J3 pin to DRAM pin, the route passes through three regions. Each of these regions have different routing rules and requirements. The regions are defined as:

- Breakout——This is the region where signals are fanned out away from the processor. Due to the ball pith of the processor package, the spacing rules of the signals in this area are relaxed that signals are allowed to be closer to each other.
- Bus Channel——This is the region where signals travel from the processor breakout to the DRAM Field area. While in Bus Channel, the spacing and impedance rules are more stringent. Bus Channel routing rules are specified in terms of a target trace impedance and relative "H" spacing. "H" is a multiple of the dielectric height.
- DRAM Field——This is the region where signals are routed to the vias which connect to the DRAM balls. Due to the ball pith of the DRAM package, the signals are allowed to route with reduced trace width and spacing for a limited length.

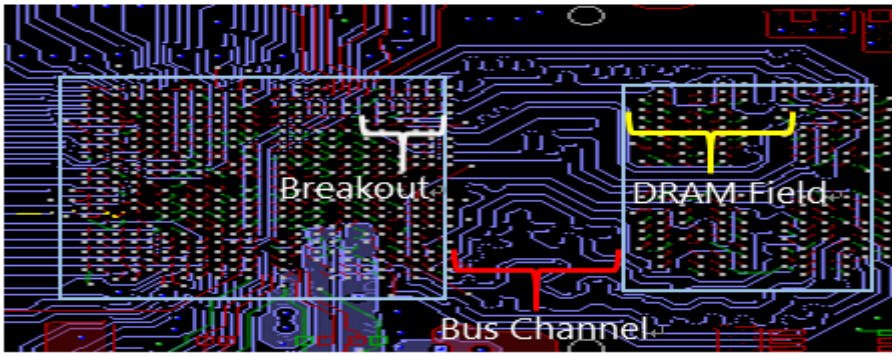


Figure 3-1 Routing Region of DDR Signals

3.3.1 Line Width and Space

For LPDDR4/4x applications that exceed 1866Mbps, it is highly recommended to avoid using microstrip trace. If microstrip must be used, it should be confined to short length with spacing that is greater than 3X the height to the reference plane.

Please note that narrower spacing within byte groups could be used with stripline applications. If necessary, spacing can be as small as 2X the height to the nearest reference plane.

Serpentine traces having closely spaced parallel routes will exhibit shorter delays than expected. Increase space of adjacent serpentine traces to 3X height over nearest reference plane.

Table 3-5 Line Space Rule Summary (Stripline)

Net Name	Breakout Region		Channel Bus			DRAM Field	
	Others	Self	Others(same group)	Others(other groups)	Self	Others	Self
DQ/DM	4mil	NA	2H	3H	3H	4mil	NA
DQS	4mil	NA	3H	3H	3H	4mil	NA
CLK	4mil	NA	3H	3H	3H	4mil	NA
CMD/ADD/CTL	4mil	NA	2H	3H	3H	4mil	NA

Crosstalk between different function groups will introduce unpredictable timing effects and should be avoided. It is recommended that the spacing between byte lanes and the CA region should be a minimum of 3X the height above the reference plane. It is better to route the CLK signal on top layer with no via transition and keep over than 5W spacing from other signals.

3.3.2 Via Space

At a data rate of 4266Mbps, signal vias can be a significant source of crosstalk. If not properly handled, it will introduce crosstalk larger than that from other trace. To minimize via crosstalk, place at least one ground stitching via within 40mils to signal via when switching reference planes. Moreover, DDR vias should be kept at a certain distance from other high noise vias in system.

3.3.3 Impedance

Characteristic impedance of LPDDR4/4x on 8-layer PCB is 50 Ohm/100 Ohm for single /differential signals in stackup depicted in Section 3.1. However, if possible on PCB design, we recommend that the impedance of DQ and DMI signal traces should be controlled to 40Ω instead of 50Ω to maximize the timing margin.

Crosstalk and characteristic impedance of an array of traces are interrelated. In order to minimize the crosstalk, the characteristic impedance of a trace should be determined predominantly by the distance of the reference plane and not the distance to the neighboring traces. To achieve this, the space between traces should be 2X the height of the trace above the ground plane.

3.3.4 LPDDR4/4x Routing Rule

Table 3-6 LPDDR4/4X Design Rule

Item	Design Rules	
	Layer 3	Layer 6
DQ: DQ[31:0] **DQS: DQS_T[3:0]/ DQS_C[3:0]** **DM: DM[3:0]**		
Zdiff /Zo [**DQS_T** / **DQS_C**]	100Ω±10%	100Ω±10%
Zdiff /Zo [**DQ, DM**]	50Ω±10%	50Ω±10%
Skew Specification	• The differential signals are made pair pattern • The length difference of DQS_T/DQS_C are within **±1 ps** • The delay difference of DQS_T/DQS_C from CLK edge position are within **±50 ps** • The delay difference of DQ,DM to DQS in same byte group are within **±5 ps** • It is not recommended to exchange the net of same byte group of DQ (Refer the Group Definition) based on reference design • The signal length should be as short as possible	
Group Definition	Group1: DM[0], DQ[7:0], DQS_T[0], DQS_C[0] Group2: DM[1], DQ[15:8], DQS_T[1], DQS_C[1] Group3: DM[2], DQ[23:16], DQS_T[2], DQS_C[2] Group4: DM[3], DQ[31:24], DQS_T[3], DQS_C[3]	
ADR: CA[5:0]A, CA[5:0]B **CMD: CKE[1:0]A, CKE[1:0]B, CS[1:0]A, CS[1:0]B, RESET_N**		
Zo	50Ω±10%	50Ω±10%
Skew Specification	The length difference of ADR / CMD from CLK are within **±20 ps** (except RESET_N)	
CLK: CLKA_T/CLKA_C, CLKB_T/CLKB_C		
Zdiff	100Ω±10%	-
Skew Specification	• The differential signals are made pair pattern and shielded by VSS • The length difference of CLK_T/CLK_C are within **±1 ps** • The length difference between CLKA and CLKB is within **±1 ps**	

	• The signal length should be as short as possible

There is training process during system booting for the LPDDR4/4x interface that can remove skew. The layout designer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is rational engineering practice and can simplify debugging.

When signals are routed in a surface microstrip, differential signals travel slightly faster than single-ended signals, about 5% to 10%. Consequently, a small increase in length of the differential signals may be required.

3.3.5 DDR4 Routing Rule

Table 3-7 DDR4 Design Rule

Item	Design Rules	
	Layer 3	Layer 6
DQ: DQ[31:0] **DQS: DQS_T[3:0]/ DQS_C[3:0]** **DM: DM[3:0]**		
Zdiff /Zo [**DQS_T** / **DQS_C**]	100Ω±10%	100Ω±10%
Zdiff /Zo [**DQ, DM**]	50Ω±10%	50Ω±10%
Skew Specification	• The differential signals are made pair pattern • The length difference of DQS_T/DQS_C are within **±1 ps** • The delay difference of DQS_T/DQS_C from CLK edge position are within **±80 ps** • The delay difference of DQ,DM to DQS in same byte group are within **±5 ps** • It is not recommended to exchange the net of same byte group of DQ (Refer the Group Definition) based on reference design • The signal length should be as short as possible	
Group Definition	Group1: DM[0], DQ[7:0], DQS_T[0], DQS_C[0] Group2: DM[1], DQ[15:8], DQS_T[1], DQS_C[1] Group3: DM[2], DQ[23:16], DQS_T[2], DQS_C[2] Group4: DM[3], DQ[31:24], DQS_T[3], DQS_C[3]	
ADR/CMD: A[13:0], BG[1:0], BA[1:0], RAS_N, CAS_N, WE_N, ACT_N **CONTROL: CS_N[1:0], CKE[1:0], ODT[1:0], PAR, RESET_N**		
Zo	50Ω±10%	50Ω±10%
Skew Specification	The length difference of ADR / CMD / CONTROL from CLK	

	are within **±20 ps** (except RESET_N)	
CLK: CLK[1:0]_T/CLK[1:0]_C		
Zdiff	100Ω±10%	-
Skew Specification	• The differential signals are made pair pattern and shielded by VSS • The length difference of CLK_T/CLK_C are within **±1 ps** • The length difference between CLK1 and CLK0 is within **±1 ps** • The signal length should be as short as possible	

There is training process during system booting for the DDR4 interface that can remove skew. The layout designer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is rational engineering practice and can simplify debugging.

When signals are routed in a surface microstrip, differential signals travel slightly faster than single-ended signals, about 5% to 10%. Consequently, a small increase in length of the differential signals may be required.

4 PCB Simulation

The section is intended to provide an overview of the system-level PCB AC impedance extraction, and AC impedance optimization for high-speed LPDDR4/4X/DDR4 interfaces. This is an essential step to ensure the PCB design meets all the requirements to operate at the target data rate.

4.1 AC Impedance Extraction

The board level extraction guidelines are intended to work in any EDA extraction tool and are not tool-specific.

- Extract power (VDDQLP、VDDQ and VDD_DDR) in a 3D-EM (at least 2.5D) solver.
- Use wide-band models. It is recommended to extract from DC to at least 6x the Nyquist frequency (for example, for LPDDR4-4266 extract the model at least till 12.8 GHz).
- Check the board stack-up for accurate layer thickness and material properties. (Djordjevic-Sarkar models is recommended)
- Use accurate etch profiles and surface roughness for the signal traces across all layers in the stack-up.
- If the board layout is cut prior to extraction (to reduce simulation time), please define a cut boundary that is at least 0.25 inch away from the power nets.
- Check the via pad stack definitions. Ensure that the non-functional internal layer pads on

signal vias are modeled the same way they would be fabricated.

- Use wide-band Spice/S-parameter models (typically available from the vendor) for modeling all passives (especially the capacitors) in the system

4.2 Model Validation

The extracted board models need to be checked for the following properties:

- Passivity: This ensures that the board model is a passive network and does not generate energy
- Causality: This ensures that the board model obeys the causal relationship i.e. output follows input.

These checks can be performed in any standard EDA simulator or extraction engine.

4.3 AC Impedance Optimization

Once the extracted S-parameters have been verified as causal and passive, the S-parameter plots should be inspected.

PCB-PDN design faces challenge of reducing noise margins. One aspect of PDN design is to find the number of decoupling capacitors required for each power rail. As more capacitors are added, the mid frequency equivalent inductance in the impedance of the PCB-PDN converges to a minimum value for each placement pattern. This convergence is studied for different placement patterns to find the least number of capacitors required to satisfy a certain convergence criteria.

For each power supply, you must choose a network of bulk and ceramic decoupling capacitors. By determining the optimal set of decoupling capacitors (with experience or EDA tool) for a given design, you can save board space and ease the board layout process.

To achieve optimal performance, the composite impedance must meet the target impedance up until the PCB cutoff frequency. If the design impedance exceeds the target impedance, there will be SSN problems, which will affect the signal integrity.

4.4 SI Simulation Topology

4.4.1 SI Write

The Figure 4-1 represents the full channel model for SI write, including J3&DRAM ibis model and package model. The eye probe should be at DRAM ibis model side.

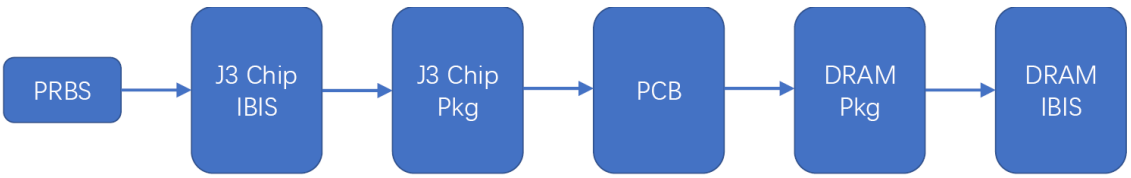


Figure 4-1 Simulation Topology for SI Write

4.4.2 SI Read

The Figure 4-2 represents the full channel model for SI read, including J3&DRAM ibis model and package model. The eye probe should be at J3 ibis model side.

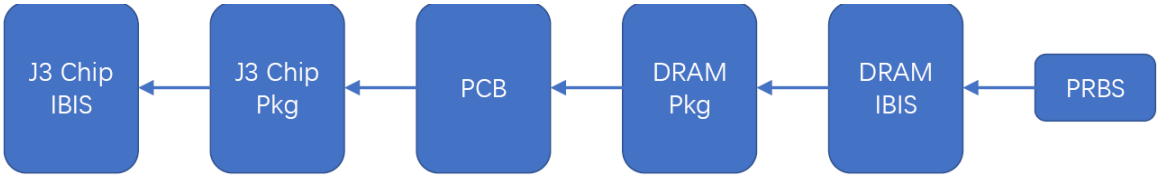


Figure 4-2 Simulation Topology for SI Read

4.4.3 SI ADDR and CLK Jitter

The Figure 4-3 represents the full channel model for SI ADDR and CLK Jitter, including J3&DRAM ibis model and package model. The eye probe should be at DRAM ibis model side.

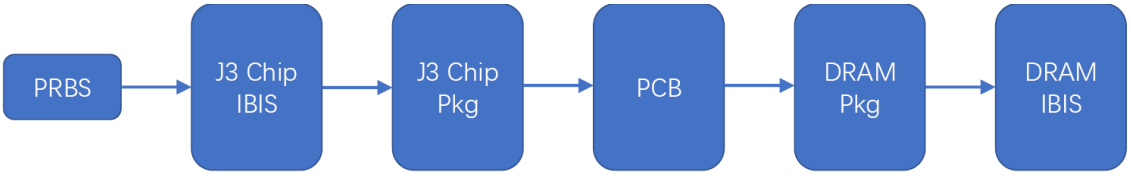


Figure 4-3 Simulation Topology for SI ADDR and CLK Jitter

4.5 PDN Impedance Target

The section specify the AC impedance targets for LPDDR4/4X/DDR4 power rails. Decoupling capacitors placements, values and power plane should be optimized to achieve the target to ensure the interface have enough margin to operate at the intended data rate.

4.5.1 PCB Targets for DDR4

Table 4-1 PCB Targets for DDR4 Power Supplies

PARAMETERS	PDN IMPEDANCE CHARACTERISTCS		PCB DC RESISTANCE (mOhm) 0~200KHz	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WO ESL)(nH)
	IMPEDANCE TARGET(mOhm)	FREQUENCY OF INTEREST(MHz)		
VDDQ_DDR	43	30	6	0.5
	84	160		
VDD_DDR	44	30	12	0.5

	76	70		

Figure 4-4 represents the target impedance response of the VDDQ_DDR net on J3 DDR4 SOM board.

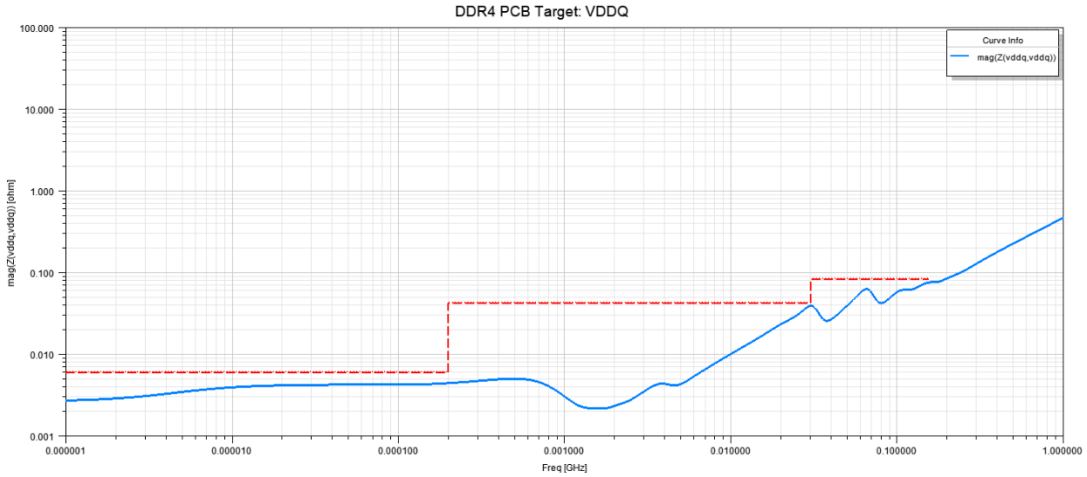


Figure 4-4 VDDQ_DDR PDN on J3 DDR4 SOM board

Figure 4-5 represents the target impedance response of the VDD_DDR net on J3 DDR4 SOM board.

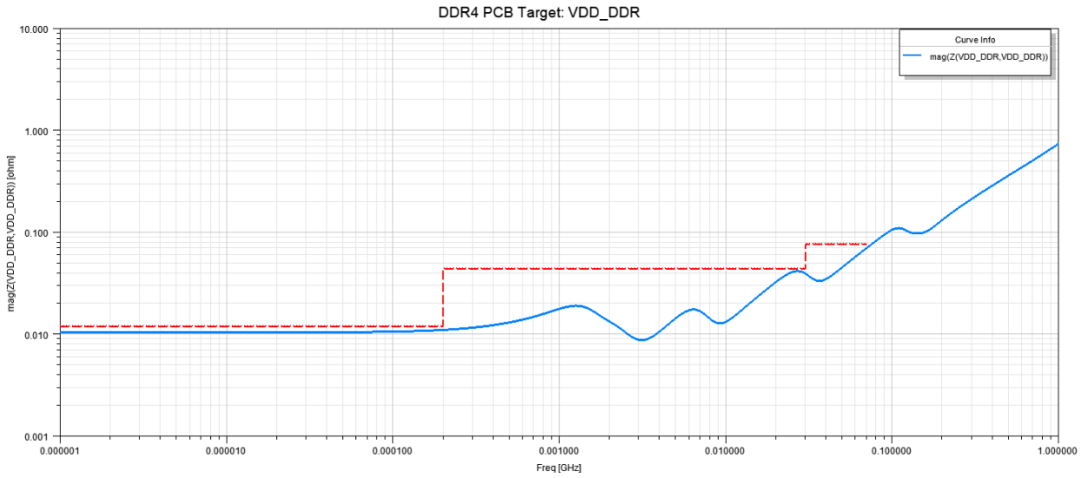


Figure 4-5 VDD_DDR PDN on J3 DDR4 SOM board

4.5.2 PCB Targets for LPDDR4

Table 4-2 PCB Targets for LPDDR4 Power Supplies

PARAMETERS	PDN IMPEDANCE CHARACTERISTCS		PCB DC RESISTANCE 0~200KHz (mOhm)	MAXIMUM LOOP INDUCTANCE PER CAPACITOR(WOESL)(nH)
	IMPEDANCE TARGET(mOhm)	FREQUENCY OF INTEREST(MHz)		

VDDQ_DDR	37.4	30	6	0.5
	105	160		
VDD_DDR	44	30	12	0.5
	76	70		

Figure 4-6 represents the target impedance response of the VDDQ_DDR net on J3 LPDDR4 SOM board.

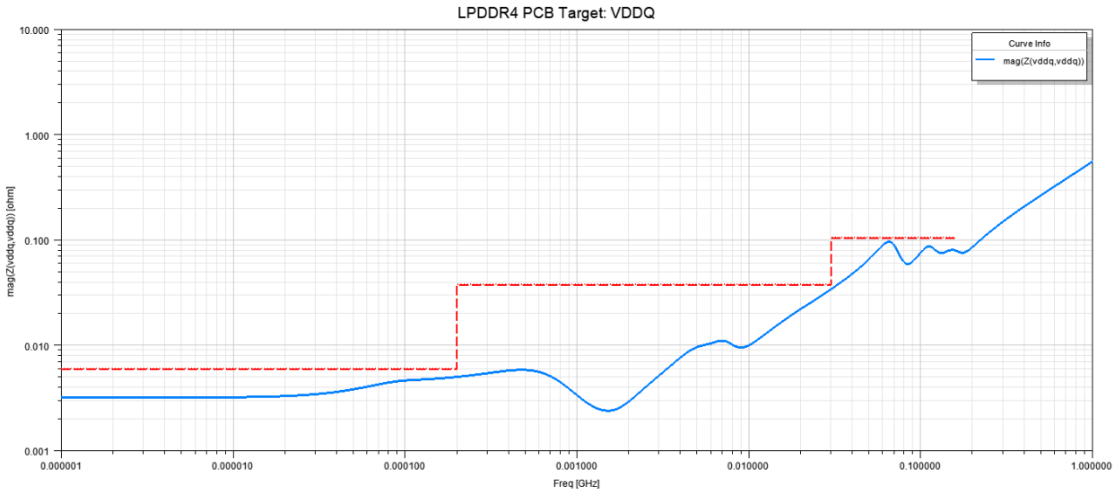


Figure 4-6 VDDQ_DDR PDN on J3 LPDDR4 SOM board

Figure 4-7 represents the target impedance response of the VDD_DDR net on J3 LPDDR4 SOM board.

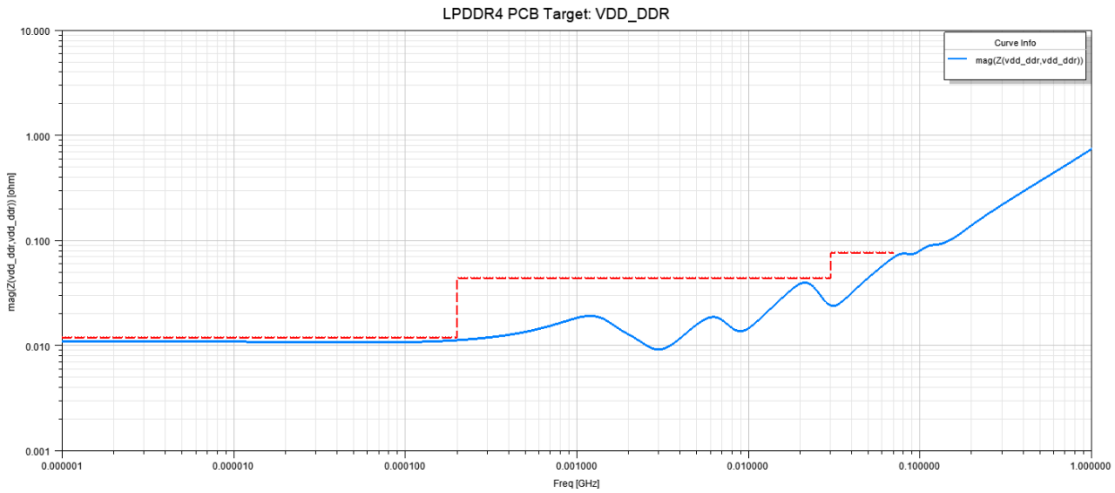


Figure 4-7 VDD_DDR PDN on J3 LPDDR4 SOM board

4.5.3 PCB Targets for LPDDR4x

Table 4-3 PCB Targets for LPDDR4x Power Supplies

PARAMETERS	PDN IMPEDANCE CHARACTERISTCS	PCB DC	MAXIMUM

	IMPEDANCE TARGET(mOhm)	FREQUENCY OF INTEREST(MHz)	RESISTANCE 0~200KHz (mOhm)	LOOP INDUCTANCE PER CAPACITOR(WO ESL)(nH)
VDDQ_DDR	37.4	30	6	0.5
	105	160		
VDDQLP_DDR	90	30	10	0.5
	400	200		
VDD_DDR	44	30	12	0.5
	76	70		

Figure 4-8 represents the target impedance response of the VDDQLP net on J3 LPDDR4x SOM board.

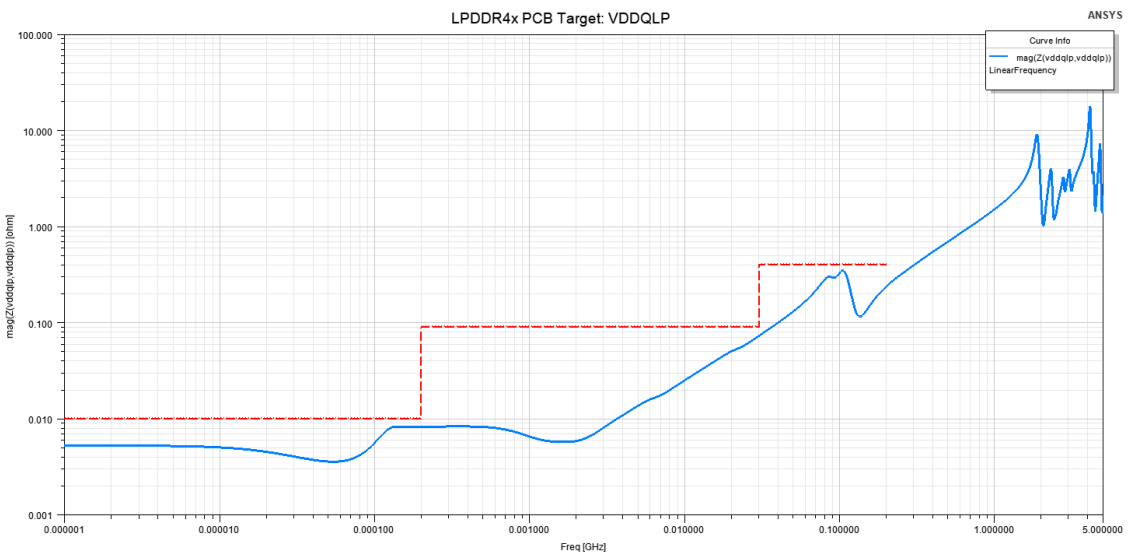


Figure 4-8 VDDQLP PDN on J3 LPDDR4x SOM board

4.6 Specification for SI simulation

4.6.1 LPDDR4 3200

Table 4-4 represents the eye mask for LPDDR4-3200 based on the topology from Figure 4-1 to Figure 4-3.

Table 4-4 Eye Mask for LPDDR4-3200

LPDDR4-3200	Eye Mask	Note
SI Write	156.25 ps	1

SI Read	149.1 ps	2
SI Addr	442 ps	1

Note1: When measuring the Write/Addr eye, the corresponding threshold levels must be taken into account, as defined in the JEDEC spec.

Note2: When measuring the Read eye, we measure around VREF where we define read timing.

Figure 4-9 represents the SI Write Eye Measurement for LPDDR4-3200 of J3 LPDDR4 board.

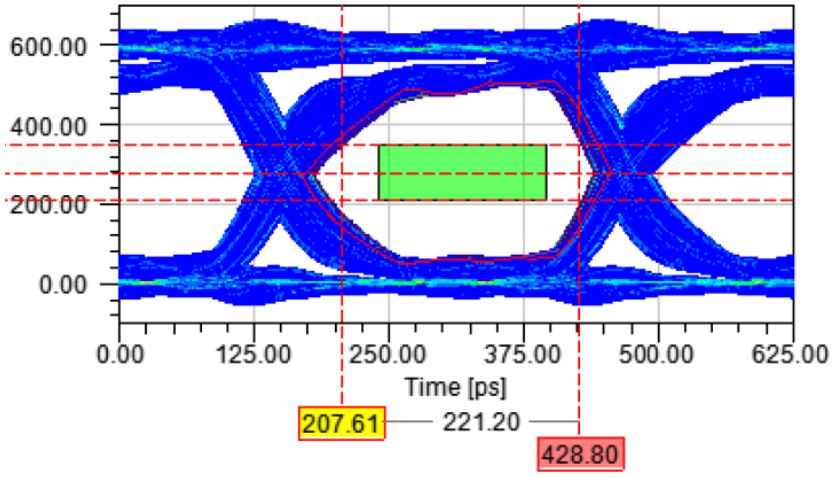


Figure 4-9 SI Write Eye Measurement for LPDDR4-3200

Figure 4-10 represents the SI Read Eye Measurement for LPDDR4-3200 of J3 LPDDR4 board.

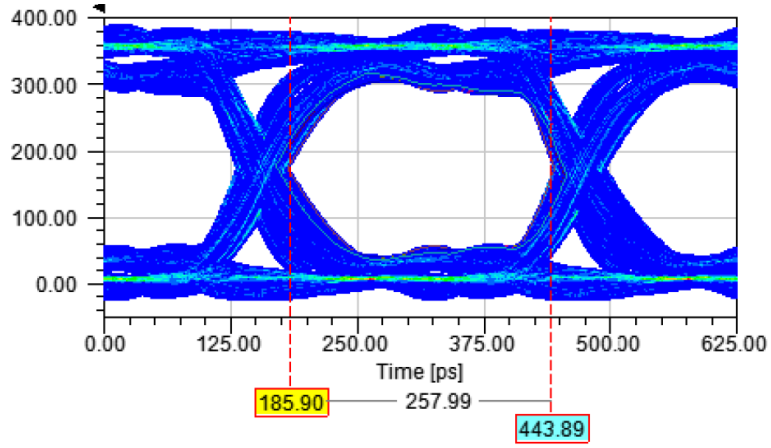


Figure 4-10 SI Read Eye Measurement for LPDDR4-3200

Figure 4-11 represents the SI ADDR Eye Measurement for LPDDR4-3200 of J3 LPDDR4 board.

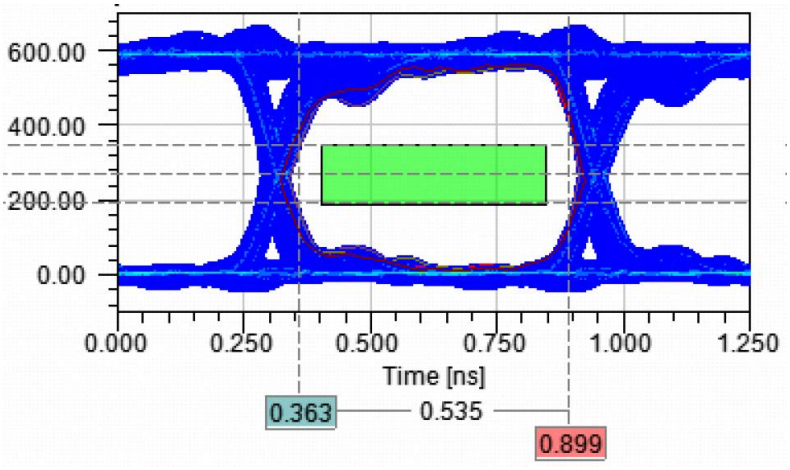


Figure 4-11 SI ADDR Eye Measurement for LPDDR4-3200

Table 4-5 represents the CLK Jitter Spec for LPDDR4-3200 based on the topology from Figure 4-3 SI Addr Simulation.

Table 4-5 CLK Jitter Spec for LPDDR4-3200

LPDDR4-3200	Spec	Note
CLK Jitter	<8 ps	Note1

Note1: Simulation result is from SI ADDR simulation and signal CK/CK# should be taken differentially.

Figure 4-12 represents the CLK Jitter Measurement for LPDDR4-3200 of J3 LPDDR4 board.

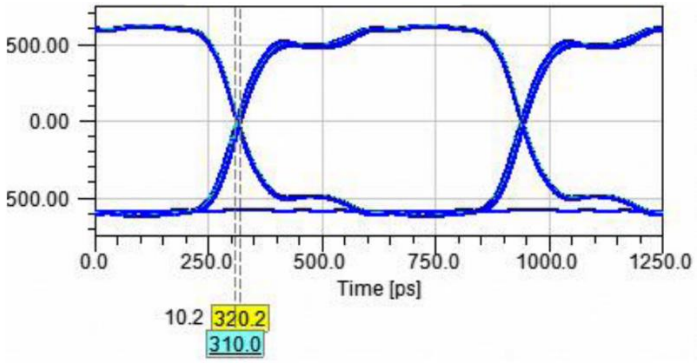


Figure 4-12 CLK Jitter Eye Measurement for LPDDR4-3200

5 Memory Components Selection

Carefully choose the LPDDR4/4X/DDR4 components used with Journey 3 according to the following rules:

- Choose memory components with suitable data rates and temperature range.

Table 5-1 Memory Components Spec

Mode	Memory Data rates spec	Temperature range	Note
LPDDR4	>= 3733Mbps	Wider than -40 ~ 105 degC	1,2
LPDDR4X	>= 3733Mbps	Wider than -40 ~ 105 degC	1,2
DDR4	>= 3200Mbps	Wider than -40 ~ 105 degC	1,2

Note1: Automotive AEC-Q100 grade 2

Note2: data rates finally set in firmware is dependent on the memory bandwidth needed by the customer scenario. Choose 3200Mbps as default for both LPDDR4/4X and DDR4 application, as 3200Mbps is widely tested. Discuss with Horizon for application with 3600Mbps or data rates lower than 3200Mbps.

- Choose LPDDR4/4X components with 32bit width and DDP package, avoid to use QDP components.

6 Appendix A Verified Memory Components

The section lists the components which have been verified with Journey 3. Customers are encouraged to choose memory component for their own application in the list of table 6-1.

Table 6-1 Verified DDR Components

Item	Vendor	Part Number	Description	Note
1	Hynix	H54G46BYYQX053N	16Gb LPDDR4 4266Mbps, -40~105 degC, DDP	
2	Micron	MT53D512M32D2DS-046AAT	16Gb LPDDR4 4266Mbps, -40~105 degC, DDP	
3	Micron	MT40A256M16LY-062E AIT	4Gb DDR4 3200Mbps, -40~95 degC	

The components in table 6-2 has not been verified, but those components are in the verification plan, and the status will be updated.

Table 6-2 Components under planning

Item	Vendor	Part Number	Description	Note
1	Micron	MT53E1G32D2FW-046 AAT:A	32Gb 4266Mbps, -40~105 degC, DDP	
2	Micron	MT53E256M32D2DS-053AAT:B	8Gb 3733Mbps, -40~105 degC, DDP	
3	Samsung	K4F8E3S4HD-GHCLT2V	8Gb 4266Mbps, -40~105 degC, DDP	

7 Appendix B Design note for decaps

Specific customers may have concerns on decaps of 0201 footprint due to the reason of DFM (Design for Fabrication). It is still applicable for those customers to use 0402 decaps on the back side of the Journey 3 PCB footprint. Please refer to the following rules when choose to use 0402 decaps.

- Decaps with values equals to or lower than 1uF still need to be placed as close as possible to the Journey 3 power pin. As the J3's ball pitch is 0.65mm, special consideration is needed to put the 0402 decap close enough to the power pin. The Figure 7-1 gives suggested pad design for 0402 decap. Figure 7-2 gives suggestion for 0402 decap placement on the back side of J3's PCB footprint..

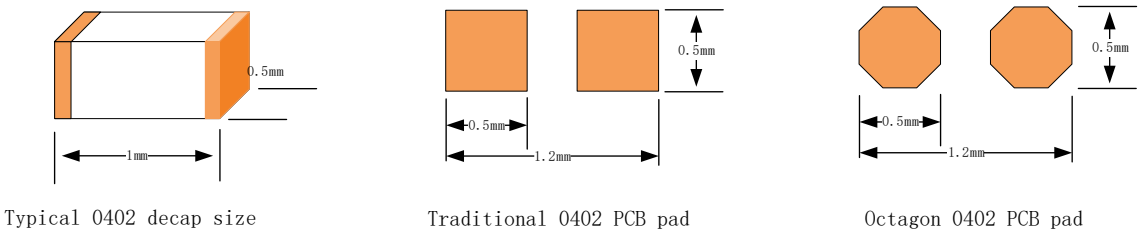


Figure 7-1 0402 Component size and PCB pad size

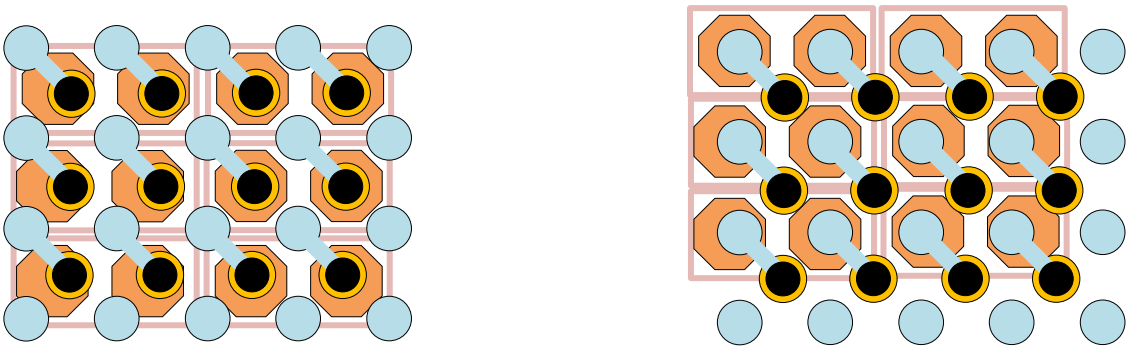


Figure 7-2 Octagon 0402 decaps placement

- Power integrity simulation needs to be conducted to ensure the AC impedance of the PDN fulfills the target depicted in Section 4.5. The PDNs which need to be simulated for DDR design are VDDQ_DDR, VDD_DDR and VDDQLP_DDR(4X only). For other PDNs in addition to DDR, refer to the HW Design Guide.

For decap part numbers listed in section 3.2, please be noted the facts described below. Decap reselection needs to be considered based on the customer scenario. Meanwhile, conduct power integrity simulation to ensure the PDN impedance target is fulfilled.

- Murata GRT serial is for Vehicle-mounted Infotainment System, and not suitable for autonomous driving system higher than L2.
- Murata GCM serial is suitable for autonomous driving system higher than L2. GCM serial generally has bigger footprint than GRT serial.