DesignWare® Cores LPDDR5/4/4x PHY for Automotive Grade 2 (AP) TSMC7FF18

Databook

dwc_ap_lpddr54_phy_tsmc7ff18 - Product Code: D771-0

PHY Version: 2.20a_d1
September 29, 2021

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Contents

Revision History

The following tables lists the revision history of the PHY from release to release. Refer to the PHY release notes for a detailed description of PHY component updates.

Note

- Links and references to section, table, figure, and page numbers in this table are only assured to be valid for the version in which the change is made
- In some instances, documentation-only updates occur. The DesignWare IP product information (http://www.designware.com) has the latest documentation
- Documentation only updates are designated using the following numbering structure <phy_version>_d<x>.

PHY Version	SE/SEC/ DIFF Version	MASTER Version	Repeater Blocks Version	Utility Blocks Version	CTB Version	Firmware Version	Phyinit Version	PUB/PHY _TOP Version	Databook Date	Description
2.20a _d1	3.20a / 3.11a / 3.20a	3.20a	3.10a	3.20a	C-2020. 11-SP1	C-2020.11	C-2020.11	1.02a_patch3 / 1.02a_patch4	September 29, 2021	Updated: ■ "PCLK Construction" on page 293

PHY Version	SE/SEC/ DIFF Version	MASTER Version	Repeater Blocks Version	Utility Blocks Version	CTB Version	Firmware Version	Phyinit Version	PUB/PHY_TOP Version	Databook Date	Description
2.20a	3.20a / 3.11a / 3.20a	3.20a	3.10a	3.20a	C-2020.11-SP1	C-2020.11	C-2020.11	1.02a_patch3 / 1.02a_patch4	May 17, 2021	Updated: ■ "Preface" on page 15 ■ "Process Information" on page 43 ■ "PHY Key Features" on page 29 ■ "PHY Cell Dimensions" on page 44 ■ "Used Devices" on page 47 ■ "DWC AP LPDDR5/4/4x PHY Deliverables" on page 48 ■ "System Clocking Configuration" on page 78 ■ "Optimal PLL Settings" on page 82 ■ "DDRPHYMASTER Signal Descriptions" on page 101 ❑ Updates to several descriptions for clarity and link corrections but no functional updates. ■ "DDRPHYDIFF Signal Descriptions" on page 137 ❑ Updates to several descriptions for clarity and link corrections but no functional updates. ■ "DDRPHYSE Signal Descriptions" on page 163 ❑ Updates to several descriptions for clarity and link corrections but no functional updates. ■ "DDRPHYSEC Signal Descriptions" on page 185 ❑ Updates to several descriptions for clarity and link corrections but no functional updates. ■ "Recommended Operating Conditions" on page 204 ■ "Common DC Input Conditions for Flyover Bypass" on page 211 ■ "Common DC Output Parameters" on page 217 ■ "Common DC Output Conditions for SEC" on page 219 ■ "Build-It-Yourself ESD Protection" on page 229 ■ "Power Supply Capacitance" on page 231 ■ "SE_IO Pin List" on page 259 ■ "DIFF_IO Pin List" on page 265 ■ "Pull-down drive strength control" on page 276 ■ "Layout Design Guidelines" on page 291 ❑ Extensive chapter updates. A full review is advised.

PHY Version	SE/SEC/ DIFF Version	MASTER Version	Repeater Blocks Version	Utility Blocks Version	CTB Version	Firmware Version	Phyinit Version	PUB/PHY _TOP Version	Databook Date	Description
2.00a	3.00a	3.00a	3.00a	3.00a	A-2019. 08-BETA	A-2019.08 -BETA	A-2019.08 -BETA	1.02a_patch3	July 9, 2020	Updated: ■ “The DWC LPDDR5/4/4x PHY Features” on page 29 ■ “PHY DQS2DQ Delay Drift” on page 223 ■ “PHY Compiler Output” on page 237 ■ “ZCALANA Pin List” on page 242 ■ “POR Pin List” on page 246 ■ “SE_IO Pin List” on page 259 ■ “DIFF_IO Pin List” on page 258 ■ “SE_IO/DIFF_IO Output Drive Strength Option” on page 273 ■ “SEC_IO Pin List” on page 272 Added: ■ “Layout Exceptions” on page 306
2.00a _pre2	3.00a_pre2	3.00a_pre2	3.00a_pre 2	3.00a_pre 2	A-2019. 08-BETA	A-2019.08 -BETA	A-2019.08 -BETA	1.02a_patch2	June 18, 2020	Updated: ■ “Preface” on page 15 ■ “Product Overview” on page 23 ❑ Extensive chapter updates. A full review is advised. ■ “POR Circuit Diagram” on page 73 ■ “Electrical Specifications” on page 203 ❑ Extensive chapter updates. A full review is advised. ■ “CLK Distribution and CLK Macros” on page 242 ■ “MASTER Macros” on page 249 ■ “DDR IO TX/RX Cells” on page 257 ■ “Layout Design Guidelines” on page 291 ❑ Extensive chapter updates. A full review is advised.
1.00b	2.00a	2.00a	2.00a	2.00a	A-2019. 08-BETA	A-2019.08 -BETA	A-2019.08 -BETA	1.02a / 1.02a_patch1	January 23, 2020	Updated: ■ Component Versions ■ Copyright information

PHY Version	SE/SEC/ DIFF Version	MASTER Version	Repeater Blocks Version	Utility Blocks Version	CTB Version	Firmware Version	Phyinit Version	PUB/PHY _TOP Version	Databook Date	Description
1.00a	2.00a	2.00a	2.00a	2.00a	A-2019. 08-BETA	A-2019.08 -BETA	A-2019.08 -BETA	1.02a / 1.02a_patch1	December 3, 2019	Updated: ■ "I/O Features" on page 22 ■ "Process Information" on page 34 ■ "PHY Cell Dimensions" on page 35 ■ "DWC LPDDR5/4/4x PHY Deliverables" on page 39 ■ "System Clocking Configuration" on page 79 ■ "LPDDR5 Input Slew Rates Versus Data Rate (in MT/s)" on page 214 ■ "Common DC Output Parameters" on page 219 ■ "Hard Macro Abutment and Spacing Requirements" on page 299 Added: ■ "Optimal PLL Settings" on page 83
0.80a	0.80a	0.80a	0.80a	0.80a	A-2019. 08-BETA	A-2019.08 -BETA	A-2019.08 -BETA	1.02a	October 7, 2019	Initial Release

Preface

This databook describes the DWC AP LPDDR5/4/4x PHY.

Databook Organization

The chapters of this databook are organized as follows:

- Chapter 1, “Product Overview”: provides an overview of the PHY, block diagrams, a list of functional features, and licensing information.
- Chapter 2, “Architectural and Functional Description”: describes the functional operation of the PHY.
- Chapter 3, “Signal Overview” provides an overview on the list of the hard-macros present in the PHY.
- Chapter 4, “DDRPHYMASTER Signal Descriptions”: describes the signals in the Master hard-macro.
- Chapter 5, “DDRPHYDIFF Signal Descriptions”: describes the signals in the DIFF hard-macro.
- Chapter 6, “DDRPHYSE Signal Descriptions”: describes the signals in the SE hard-macro.
- Chapter 7, “DDRPHYSEC Signal Descriptions”: describes the signals in the SEC hard-macro.
- Chapter 8, “Electrical Specifications”: provides electrical specifications for the Synopsys DWC LPDDR5/4 PHY.
- Chapter 9, “Integrated I/O Functionality”: describes the Synopsys DWC LPDDR5/4 I/O component.
- Chapter 10, “Layout Design Guidelines”: describes the DWC LPDDR5/4 layout design guidelines.
- Chapter 11, “Automotive Grade 2 Support”: describes the DWC LPDDR5/4 Automotive guidelines.

Recommended Reading

The following documentation provides essential information about the IP to create a complete solution:

- DesignWare Cores LPDDR5/4/4x PHY Utility Block (PUB) Databook, Synopsys, Inc.
- DesignWare Cores LPDDR5/4/4x PHY Implementation Guide, Synopsys, Inc.

Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNetPlus: http://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

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Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file <core tool startup directory>/debug.tar.gz.

- For simulation issues outside of coreConsultant or coreAssembler:
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  - Identify the hierarchy path to the DesignWare instance
  - Identify the timestamp of any signals or locations in the waveforms that are not understood
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- Product: Designware Cores
- Sub Product: LPDDR54_PHY
- Tool Version:
- Problem Type:
- Priority:
- Title: Provide a brief summary of the issue or list the error message you have encountered
- Description: For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

After creating the case, attach any debug files you created in the previous step.

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
- Include the Product name, Sub Product name, and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
- For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
- Attach any debug files you created in the previous step.
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  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
- All other countries:
  http://www.synopsys.com/Support/GlobalSupportCenters

1

Product Overview

The following sections are included in this chapter:

1.1 Quick Reference

Features
- High-performance DDR PHY - Flexible two-channel architecture - Low standby and VDDQ signaling power down to 0.3V operation - PHY independent, firmware-based training using an embedded calibration processor - Supports LPDDR4/LPDDR4X up to 2 trained states/frequencies in hardware with switch times of 2560 MEMCLK plus PLL lock time - Support for LPDDR5 in 1:4 CK:WCK mode - All registers related to signaling and DRAM controls are P-state-able, enabling many opportunities for power savings (impedance values, IO performance options such as equalization, strobe operation as differential/single-ended/strobe-less, DRAM DVFS, etc.) - VT compensated delay lines for DQS centering, read/write leveling, and per bit deskew - Controller interface compliant with Synopsys expectations for the DFI 5.0 interface, with option for dual DFI Channels - Designed for rapid integration with Synopsys memory or protocol controllers for a complete DDR interface solution - Flexible implementation to support Package-On-Package (PoP) style SoCs - Built-in anti-aging features to mitigate effects of NBTI & HCI

Data Rates	Junction Temperature	Process Technology
■ 6400 Mbps	■ -40 to 125 ºC	■ TSMC7FF

Power Supplies	Test Modes Supported
■ Core supply voltage (VDD): 0.75V -7% + 10% ■ IO supply voltage: (VDDQ_DRAM) LPDDR4 Mode: 1.06V / 1.1V /1.17V ■ IO supply voltage: (VDDQ) LPDDR4 Mode: VDD Min/Typ/Max ■ IO supply voltage: (VDDQ) LPDDR4X Mode: 0.57V / 0.6V / 0.65V ■ IO supply voltage: (VDDQ) LPDDR5 Mode: 0.47V / 0.5V / 0.57V ■ IO supply voltage: (VDDQ) LPDDR5 Mode: 0.27V / 0.3V / 0.37V ■ PLL supply voltage: (VAA_VDD2H): 1.8 V -7% + 10% ■ PLL supply voltage: (VAA_VDD2H(VDD2H)): See VDD2H (per mode)	- At-speed loopback testing on both the address and data channels - Delay line BIST via built-in macro delay line oscillator - MUX-scan ATPG (stuck-at SCAN) - RX and TX asynchronous paths support a maximum bit rate of 400 Mb/s (200MHz) when controlled via bypass interface - PLL lock test - ZQ Calibration test

ESD	Metal Stack and Package Configuration
■ CDM = 6A peak discharge currentt ■ HBM = (+/-)2000V ■ Latchup = (+/-) 100mA	■ 13M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2R

Compatible Standards
■ Refer to the associated DesignWare Cores LPDDR5/4/4x PHY Utility Block (PUB) Databook

1.2 Product Overview

The DWC LPDDR5/4/4x PHY SDRAM interface solution is a combination of hard and soft IP that is used to provide a physical interface to JEDEC standard LPDDR4/LPDDR4X/LPDDR5 SDRAM memories. This solution provides logical support for all JEDEC DRAM devices compatible with the system design and PHY hard macro components.

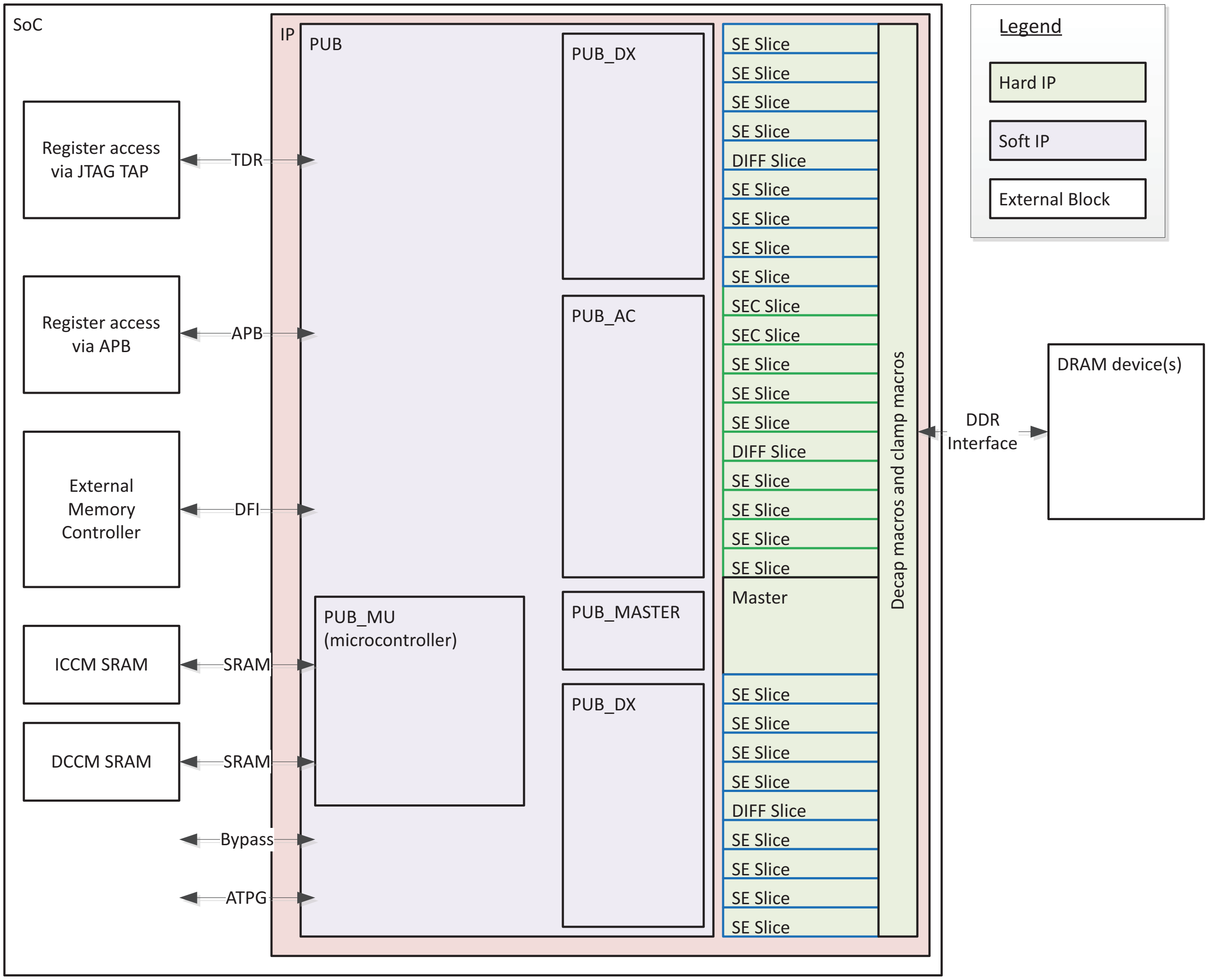
The full PHY IP solution consists of both hard IP components and soft IP components. The hard IP components include:

- A DIFF Slice macro implementing a differential input/output signal pair, including IO functionality
- An SE Slice macro implementing a single-ended input/output signals, including IO functionality
- An SEC Slice macro implementing a single-ended CMOS output signal, including IO functionality
- The PHY MASTER block, which includes the high-speed PLL, impedance calibration resistor connection, power-on-reset functionality, and CMOS output for DRAM RESET
- Clock repeater blocks, used to assist in distribution of high-speed clocks from the MASTER block to endpoints in SE, SEC, and DIFF slices.
- Physical-only clamp blocks
- Physical-only decap blocks

The soft IP consists of a single soft macro, the PHY Utility Block (DDRPHY_PUB or PUB), which provides configuration and control for all the PHY hard macros.

The Figure 1-1 shows how the PHY is used in a typical SDRAM system.

Figure 1-1 System Overview



The DWC PHY Utility Block (PUB) is an IP component to be used with the DWC PHY. It provides control features to ease the customer implementation of digitally controlled functions of the PHY such as initialization, DRAM interface training, delay line calibration and VT compensation, impedance calibration and VT compensation, and programmable configuration controls. It also provides a DFI interface to the PHY.The PUB includes configuration registers that are accessible through a configuration port. The configuration port is compatible with an APB interface.

1.2.1 System Components

The full DWC LPDDR5/4/4x PHY IP solution consists of multiple components, including a combination of the following hard IP and soft IP:

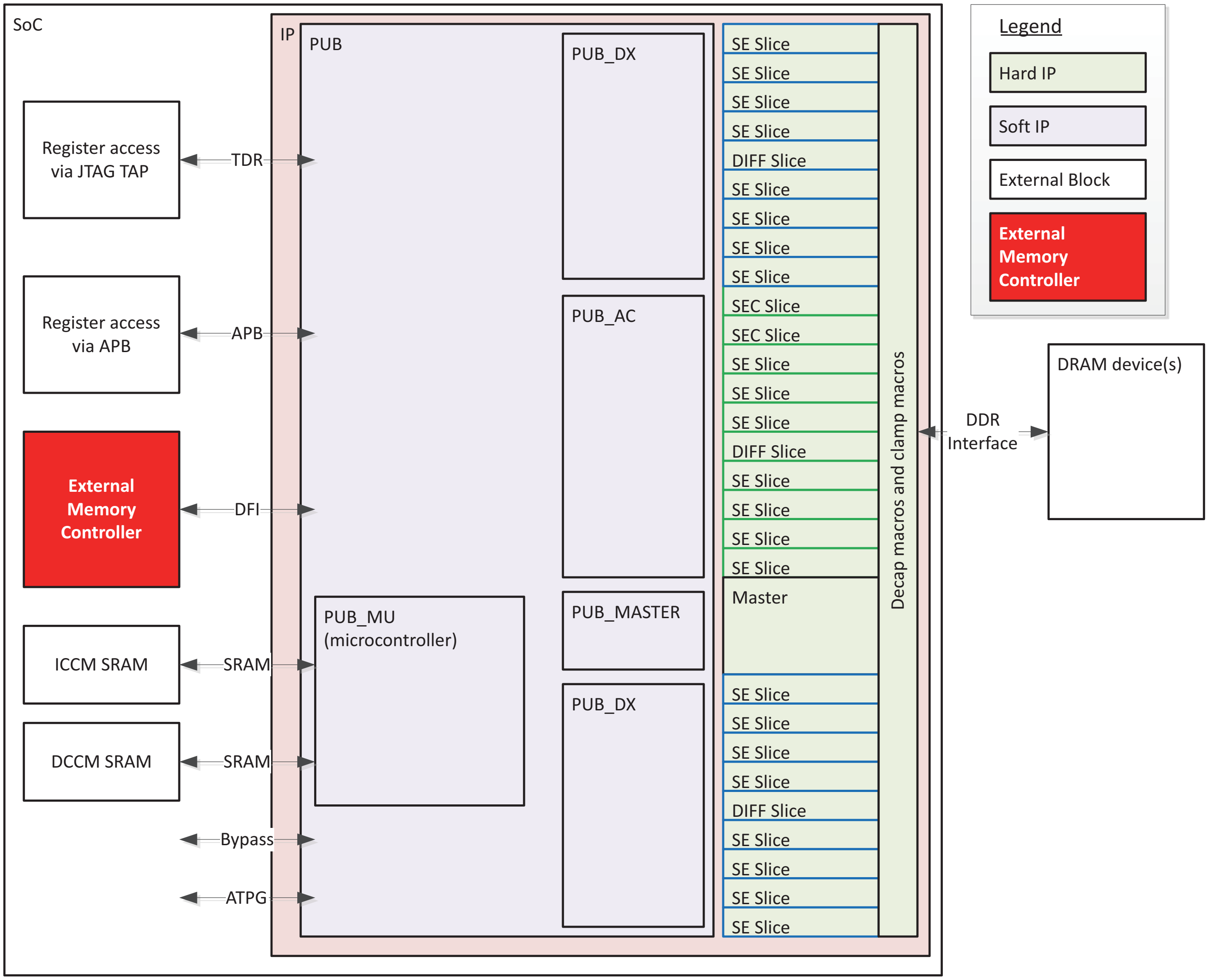
- SE Slice: The SE Slice is used for all high-speed single-ended signals, including DQ, DMI, CA, and LPDDR4 CS. Features of the SE Slices are documented in section "SE Slice" on page 56.
- SEC Slice: the SEC Slice is used for CMOS outputs to SDRAM: namely LPDDR4 CKE and LPDDR5 CS. Features of the SEC Slice are documented in section "SEC Slice" on page 61.
- DIFF Slice: The DIFF slice is used to implement differential IO pairs: CK_t/CK_c, (LPDDR4) DQS_t/DQS_c, (LPDDR5) WCK_t/WCK_c, and (LPDDR5) RDQS_t/RDQS_c. Features of the DIFF slice are documented in section "DIFF Slice" on page 58.
- MASTER PHY: The MASTER PHY is the location of the high speed PLL used to generate the high-speed clocks for data transmit and high speed digital pipelines. The PLL is capable of generating an output that is 4X or 8X the input reference clock frequency.
- Clock repeater blocks
- Clamp blocks (physical only)
- Decap blocks (physical only)
- PHY Utility Block (PUB)— a soft IP Verilog RTL block that provides configuration, control, and other utility functions for all PHY hard components. This block handles a variety of functions for the PHY, including driving initialization sequences, providing all training functions, implementing the DFI protocol, and implementing registers and a register access bus.

1.2.2 Memory Controller Solution

A memory controller solution is required for PHY applications. The solution uses the PUB's DFI interface to connect between the PHY and the memory controller (see Figure 1-2 on page 28).

Note For minimum latency, the PHY should be placed within close proximity to the memory controller.

Figure 1-2 DDR Memory Controller and PHY IP



1.3 The DWC LPDDR5/4/4x PHY Features

1.3.1 Highlights

- Supports JEDEC standard LPDDR4, LPDDR4X, and LPDDR5 SDRAMs
- High-performance DDR PHY
- Flexible two-channel architecture
- Low standby and VDDQ signaling power down to 0.3V operation
- PHY independent, firmware-based training using an embedded calibration processor
- Supports LPDDR4/LPDDR4X up to 2 trained states/frequencies in hardware with switch times of 2560 MEMCLK plus PLL lock time
- Support for LPDDR5 in 1:4 CK:WCK mode
- All registers related to signaling and DRAM controls are P-state-able, enabling many opportunities for power savings (impedance values, IO performance options such as equalization, strobe operation as differential/single-ended/strobe-less, DRAM DVFS, etc.)
- VT compensated delay lines for DQS centering, read/write leveling, and per bit deskew
- Controller interface compliant with Synopsys expectations for the DFI 5.0 interface, with option for dual DFI Channels
- Designed for rapid integration with Synopsys memory or protocol controllers for a complete DDR interface solution
- Flexible implementation to support Package-On-Package (PoP) style SoCs
- Built-in anti-aging features to mitigate effects of NBTI & HCI

1.3.2 Target Applications

- Smart phones
- Tablets
- Embedded mobile computing
- Ultraportable laptops
- Automotive (when using the specifically-targeted automotive product variant only)

1.3.3 Technology

- 7nm and below

1.3.4 PHY Key Features

- Low latency, small area, low power
- Compatible with JEDEC standard LPDDR4, LPDDR4X and, LPDDR5 SDRAMs
  - Up to LPDDR4-4267, LPDDR4X-4267, and LPDDR5-6400, process dependent
- Predicted DFI 5.0 compliant interface to the memory controller
  - DFI 1:2 and 1:4 mode support (selected at boot time)
  - LPDDR5 will always operate as 1:1 DFI:CK; DRAM CK:WCK ratio will be FSP-switchable.

  - Optional dual channel DFI
- Flexible channel architecture
  - Support for 1 or 2 independent LPDDR4/4X/5 channels
  - Supports 16-bit data path widths per channel
    - Total up to 32-bits data path using two channels
  - CA/CS/CK outputs drive 1 DRAM channel or 2 parallel DRAM channels
- PHY supports many DRAM packaging options, including:
  - SDRAM components soldered directly to PCB
  - Package-on-Package (PoP) devices
- 1 or 2 memory ranks comprised of x16 and/or x8 (“byte mode”) DRAM devices, including packages using x8 devices on one rank and x16 devices on another
- Flexible configuration options: up to 2 DQ loads, 8 CA loads, and 4 CS loads
- PHY independent, firmware-based training using an embedded microcontroller
  - Utilizes specialized hardware acceleration engines
  - Automatic periodic retraining through DFI PHY Master Interface
    - PHY may initiate this training based on either an internal timer or a request from the controller provided via dfi_ctrlmsg bus
    - Controller may also initiate periodic retraining directly via DFI frequency change protocol (without changing frequencies, if desired)
- LVSTL IO calibration and ODT calibration with:
  - Pullup drive, pulldown drive, and pulldown ODT settings for DQ/DMI/parity bits
  - Pullup drive, pulldown drive, and pulldown ODT settings for differential DQS/(LPDDR5) WCK pairs
  - Pullup drive and pulldown drive for differential CK pairs
  - Pullup drive and pulldown drive for CA/(LPDDR4) CS
  - Supports RZQ/N drive strength and termination down to a 40 ohm driver
  - 3 different uncalibrated drive strength settings for CMOS outputs plus OFF
- Can be trained for up to two distinct frequency set points (“FSP”s) to permit fast frequency changes between two frequencies
  - Fully-independent PHY control settings for each frequency, including all impedances, VREF values, and timing information
  - Each trained state is maintained across voltage and temperature variation
  - Frequency changes are initiated by the DFI interface without software involvement
- Four inactive idle states:
  - DFI_LP Mode: most clocks and delay lines gated, including clock gating the majority of PUB logic. Includes 2 usage modes:
    - 2-DFI-clock fast-exit mode and
    - 4-DFI-clock exit time with DRAM CK stopped and clocks to CA slices gates

  - PHY Inactive: leakage only
  - PHY Retention: Core power removed, most I/Os powered down, SDRAMs held in self-refresh
- Voltage and temperature compensated delay lines used for:
  - Centering each DQ/DMI/parity/CA bit's eye around a clock/strobe
  - Read/write leveling
- Includes a low-jitter PLL for both PHY clock generation and SDRAM clock generation
  - Only one PLL is required per DDR PHY, supporting 667 to 6400 Mbps operation
  - Integrated PLL bypass to support 50 to 666 MT/s
- Support for a SW controllable DQ bit and CA bit swizzling
  - SW-defined mapping of CA bits within a channel
  - SW-defined mapping of DQ bits within a byte
  - SW-defined byte swap support for swapping 2 bytes within a 16-bit DRAM channel for PHY training purposes only
    - DFI byte swaps must be handled by the memory controller
- Support for 7nm-nm and below poly orientation rules
- Macrocells can be instantiated on orthogonal sides
- Includes the PHY Utility Block (PUB)
  - Soft IP Verilog design that includes PHY control features, such as read/write leveling and data eye training
  - APB and JTAG interfaces for register access
  - DFI interface for communicating with controller
- Test support:
  - At-speed loopback testing on both the address and data channels
  - Delay line BIST via built-in macro delay line oscillator
  - MUX-scan ATPG (stuck-at SCAN)
  - RX and TX asynchronous paths support a maximum bit rate of 400 Mb/s (200MHz) when controlled via bypass interface
  - PLL lock test
  - ZQ calibration test
- TDR interface to PHY registers for easy test access
- Firmware-based 2D eye mapping diagnostic tool allows measuring 2D eye for every DQ bit of the bus at both DRAM and host receivers
- Direct override programming available for all VREF, ODT, drive strength, and timing delays to facilitate debug and characterization

1.3.5 LPDDR4/4X-Specific Features

- Support for the following training features:

  - Command Bus delay training for CA relative to CK, including CA bit deskew at user-selected CA-VREF
  - Write Leveling to compensate for CK-DQS timing skew
  - Write Training:
    - Per-bit DQS to DQ centering including compensation of DRAM tDQS2DQ delay
    - Per-rank VREFDQ training on DRAM DQ bits
  - Read training:
    - Per bit DQS to DQ eye centering training using a combination of DRAM array and MPCs
    - Data bus VREFDQ training on each PHY DQ per bit
- All JEDEC-defined DRAM addressing modes
- Single-Ended mode Support
- When DRAM supports it, PHY can support single-ended mode on CK, write DQS, and read DQS.
- Each of these can be independently enabled/disabled
- LPDDR4X DRAMs support single-ended mode only at 1600 Mbps or lower
- Flexible pre and postamble
  - LPDDR4 support for all write preamble settings defined by JEDEC
  - LPDDR4 support for all write postamble settings defined by JEDEC
  - LPDDR4 support for toggling 2 tCK read preamble only
  - LPDDR4 support for toggling 1.5 tCK read postamble only
- Data bus inversion and DMI supported in pass-through mode (controller to encode/decode)
- Periodic retraining for DRAM write (tDQS2DQ) and read (tDQSCK) drift
- DFI Interface:
  - DFI may select 1:2 or 1:4 mode at boot time
- DRAM device support:
  - Support all LPDDR4/4X compliant devices, including those following the addendum for byte-mode and single die-per-channel devices
    - DRAM device limitation of sharing single ZQ resistor across both channels prevent single die-per-channel LPDDR4/4X DRAM devices from being used if both DRAM channels are connected to a single set of CA/CS PHY output pins.
- DRAM packages that mix x16 devices on one rank with byte-mode devices on another rank are supported

1.3.6 LPDDR5-Specific Features

- Support for the following training features:
  - Command Bus delay training for CA relative to CK, including CA bit deskew at user-selected CA-VREF
  - Write Leveling to compensate for CK-DQS timing skew
  - Write Training:

    - Per-bit DQS to DQ centering including compensation of DRAM tDQS2DQ delay
    - Per-rank VREFDQ training on DRAM DQ bits
    - PUB will train DRAM-side WCK duty cycle correction (DCC).
  - Read training:
    - Per bit DQS to DQ eye centering training using a combination of DRAM array and MPCs
    - Data bus VREFDQ training on each PHY DQ per bit
    - Host DFE will be trained as a part of 2-D read eye training
- All JEDEC-defined DRAM addressing modes
- Data bus inversion, data mask, DMI, link protection, and low power data copy supported in pass-through mode (controller to encode/decode)
  - Assuming all of these features make it into the final LPDDR5 spec. Any feature dropped from the LPDDR5 JEDEC will, of course, not be supported by the IP.
- DVFSC and DVFSQ, if enabled in the platform
- LPDDR5 1:1:4 DfiClk:CK:WCK operation
- LPDDR5 CK:WCK ratio must always match the number of data phases in use on the DFI bus. DFI bus frequency must always match DRAM CK frequency in LPDDR5 mode.
- Automatic training of DQ VREF level setting separately for PHY per bit and for SDRAM per channel per rank (or per pair-of-channels per rank if 2 SDRAM channels are connected to a single PHY CA/CS output channel.)
- Periodic retraining for DRAM write (tWCK2DQI) and read (tWCK2DQO) drift
- By default, read data capture using differential RDQS strobe pair
- Single-Ended mode Support
  - When DRAM supports it, PHY can support single-ended mode on CK, WCK, and read DQS.
  - Each of these can be independently enabled/disabled
  - LPDDR5 DRAMs support single-ended mode only at 3200 Mbps or lower
- Support for strobe-less read mode to capture read data at lower speed.

1.3.7 I/O Features

- LPDDR4, LPDDR4X, and LPDDR5 operating modes.
- LPDDR5 DRAM DVFSQ support when external VDDQ adjustment is provided
- I/Os are integrated within the PHY Macrocells
- Programmable input on-die termination (ODT)
- Programmable output impedance with slew rate options
- Programmable VREF level with 1-tap DFE
- PVT-compensated ODT and output impedance
- Separate driver and receiver I/O power-down control
- Embedded boundary scan support logic and bypass with secondary input & output ports

  - Includes support logic for implementation JTAG SAMPLE instruction during mission-mode operation
  - Since receivers include samplers, non-mission-mode sampling uses a dedicated input clock pin per slice
- PAD and internal loopback modes
- Supports flip chip packaging
- Retention IO added to enable full power-down of VDD without power sequence issues during retention entry/exit
- Power on clear (POC) function renders library power supply sequence-agnostic
- Embedded VDDQ-VSS decoupling capacitance plus optional “SnapCap” cells to add additional VDDQ-VSS decoupling capacitance

Note

Features and System Configurations

- Not all system configurations listed here are supported in every release of the PHY. Please consult your release notes or Synopsys support to determine which configuration is enabled for a particular release
- Features implied through CSR or other low-level descriptions are not supported unless indicated in “The DWC LPDDR5/4/4x PHY Features” on page 29 and the release notes.

1.4 Supported System Configurations

The supported configurations for the PHY are dependent on the following programmed parameters:

- Number of channels: determined by setting one of the following:
  - DWC_DDRPHY_NUM_CHANNELS_1
  - DWC_DDRPHY_NUM_CHANNELS_2
- LPDDR5 support enabled by setting DWC_DDRPHY_LPDDR5_ENABLED
- Bytes per channel determined by setting one of the following:
  - DWC_DDRPHY_NUM_DBYTES_PER_CHANNEL_2
  - DWC_DDRPHY_NUM_DBYTES_PER_CHANNEL_4
- DMI/DBI support enabled by setting DWC_DDRPHY_DYBTE_DMI_ENABLED
- Number of ranks determined by setting one of the following:
  - DWC_DDRPHY_NUM_RANKS_1
  - DWC_DDRPHY_NUM_RANKS_2

For more information on parameter programming refer to "Architectural and Functional Description" on page 55.

The following table shows the supported configurations.

Table 1-1 Supported Configurations

Number of Channel	DWC_DDRPHY_LPDDR5_ENABLED	DWC_DDRPHY_NUM_DBYTESPER_CHANNEL	DWC_DDRPHY_DBYTE_DMI_ENABLED	Supported Rank Define	Define File CONFIG
1	undefined	2	defined	DWC_DDRPHY_NUM_RANKS_1	lp4cs1dq18ch1
1	undefined	2	undefined	DWC_DDRPHY_NUM_RANKS_1	lp4cs1dq16ch1
1	undefined	2	defined	DWC_DDRPHY_NUM_RANKS_2	lp4cs2dq18ch1
1	undefined	2	undefined	DWC_DDRPHY_NUM_RANKS_2	lp4cs2dq16ch1
1	defined	2	defined	DWC_DDRPHY_NUM_RANKS_1	lp54cs1dq18ch1
1	defined	2	undefined	DWC_DDRPHY_NUM_RANKS_1	lp54cs1dq16ch1
1	defined	2	defined	DWC_DDRPHY_NUM_RANKS_2	lp54cs2dq18ch1
1	defined	2	undefined	DWC_DDRPHY_NUM_RANKS_2	lp54cs2dq16ch1

Number of Channel	DWC_DDRPHY_LPDDR5_ENABLED	DWC_DDRPHY_NUM_DBYTESPER_CHANNEL	DWC_DDRPHY_DBYTE_DMI_ENABLED	Supported Rank Define	Define File CONFIG
2	undefined	2	defined	DWC_DDRPHY_NUM_RANKS_1	lp4cs1dq18ch2
2	undefined	2	undefined	DWC_DDRPHY_NUM_RANKS_1	lp4cs1dq16ch2
2	undefined	2	defined	DWC_DDRPHY_NUM_RANKS_2	lp4cs2dq18ch2
2	undefined	2	undefined	DWC_DDRPHY_NUM_RANKS_2	lp4cs2dq16ch2
2	defined	2	defined	DWC_DDRPHY_NUM_RANKS_1	lp54cs1dq18ch2
2	defined	2	undefined	DWC_DDRPHY_NUM_RANKS_1	lp54cs1dq16ch2
2	defined	2	defined	DWC_DDRPHY_NUM_RANKS_2	lp54cs2dq18ch2
2	defined	2	undefined	DWC_DDRPHY_NUM_RANKS_2	lp54cs2dq16ch2

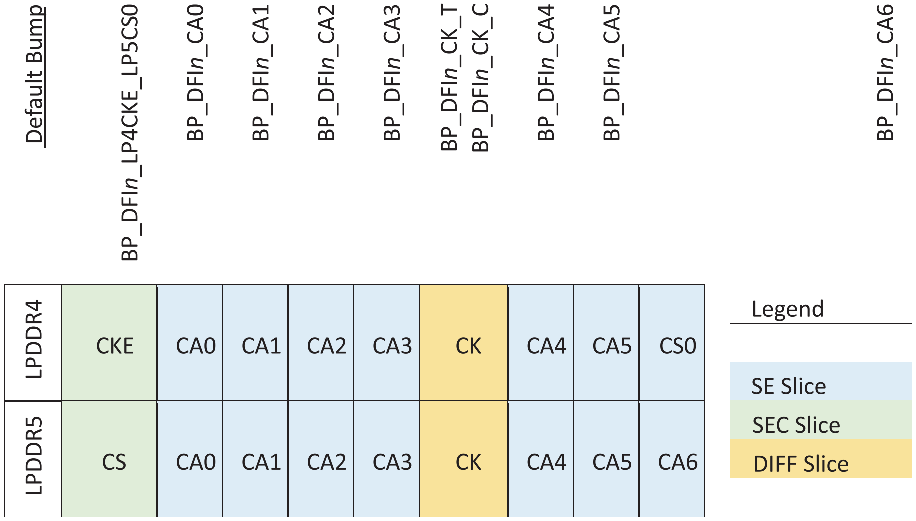
1.4.1 PHY AC Configurations

1.4.1.1 PHY AC Configuration: Single-Rank (LPDDR4 and/or LPDDR5)

The slices in the AC section for a single-rank configuration are shown below. Configurations with two channels will include two copies of this AC section.

The top row of the diagram shows the signals mapping to those slices in LPDDR4 mode; the bottom row shows signals mapping to each slices in LPDDR5 mode.

Figure 1-3 Single-rank AC Channel Slices



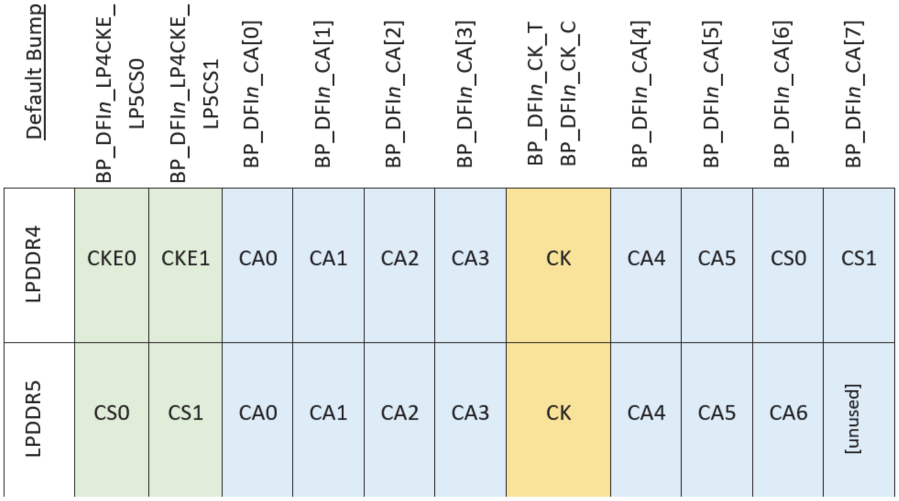
Default Bump	BP_DFI*n*_LP4CKE_LP5CS0	BP_DFI*n*_CA0	BP_DFI*n*_CA1	BP_DFI*n*_CA2	BP_DFI*n*_CA3	BP_DFI*n*_CK_T BP_DFI*n*_CK_C	BP_DFI*n*_CA4	BP_DFI*n*_CA5	BP_DFI*n*_CA6
LPDDR4	CKE	CA0	CA1	CA2	CA3	CK	CA4	CA5	CS0
LPDDR5	CS	CA0	CA1	CA2	CA3	CK	CA4	CA5	CA6

1.4.1.2 PHY AC Configuration: Dual-Rank (LPDDR4 and/or LPDDR5)

The slices in the AC section for a dual-rank configuration are shown below. Configurations with two channels will include two copies of this AC section.

The top row of the diagram shows the signals mapping to those slices in LPDDR4 mode; the bottom row shows signals mapping to each slices in LPDDR5 mode.

Figure 1-4 Dual-rank AC Channel Slices



Default Bump	BP_DFI*n*_LP4CKE_ LP5CS0	BP_DFI*n*_LP4CKE_ LP5CS1	BP_DFI*n*_CA[0]	BP_DFI*n*_CA[1]	BP_DFI*n*_CA[2]	BP_DFI*n*_CA[3]	BP_DFI*n*_CK_T BP_DFI*n*_CK_C	BP_DFI*n*_CA[4]	BP_DFI*n*_CA[5]	BP_DFI*n*_CA[6]	BP_DFI*n*_CA[7]
LPDDR4	CKE0	CKE1	CA0	CA1	CA2	CA3	CK	CA4	CA5	CS0	CS1
LPDDR5	CS0	CS1	CA0	CA1	CA2	CA3	CK	CA4	CA5	CA6	[unused]

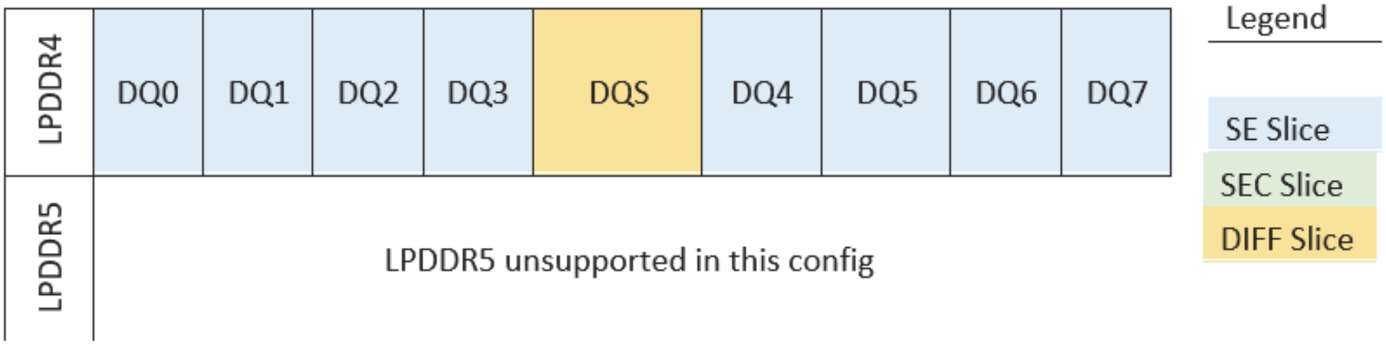
1.4.2 PHY Data Byte Configurations

Different parameters affect the data byte construction than those that affect the AC construction. Therefore, these two configurations are orthogonal – any AC configuration can be used with any data byte configuration.

1.4.2.1 PHY Configuration: LPDDR4-Only, no DMI pin

This configuration will have 8 SE Slices and one DIFF slice per byte. LPDDR5 is not supported in this configuration.

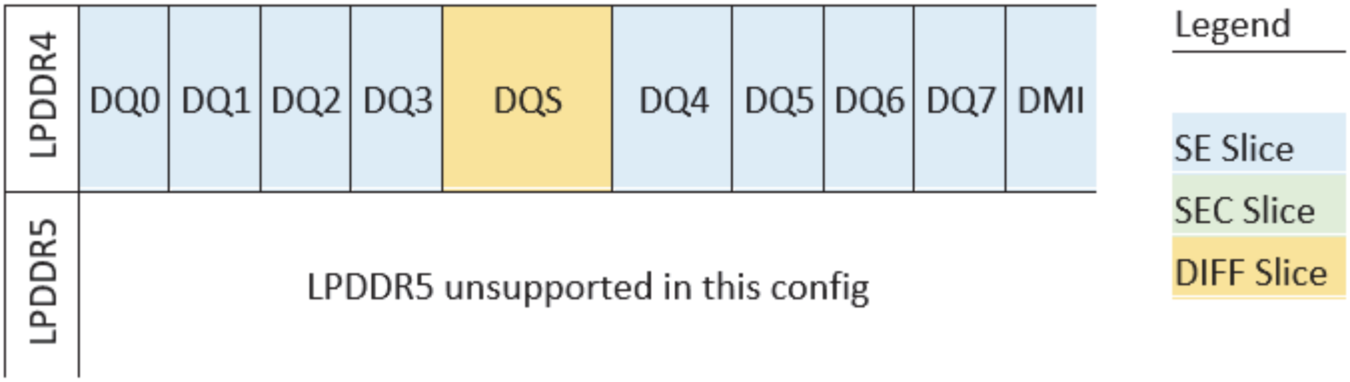
Figure 1-5 Data Byte Configuration for LPDDR4-only without DMI



1.4.2.2 PHY Configuration: LPDDR4-Only with DMI pin

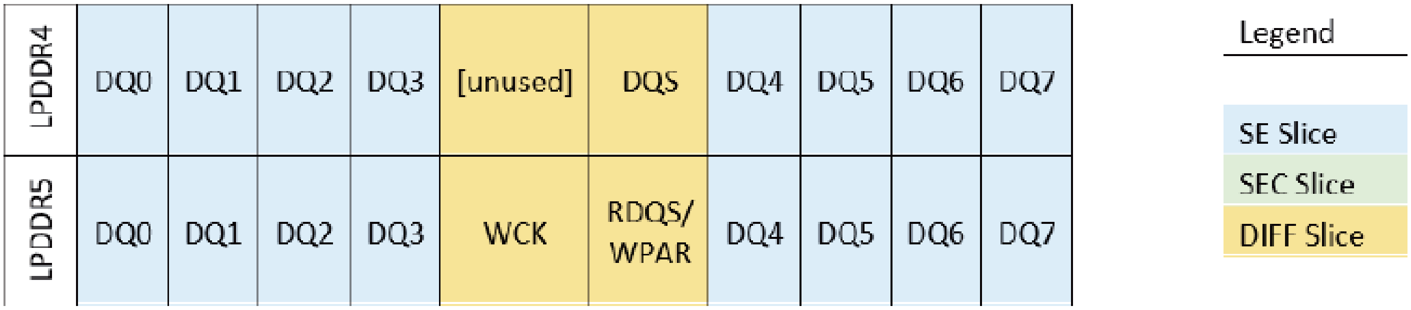
This configuration will have 9 SE Slices and one DIFF slice per byte. LPDDR5 is not supported in this configuration.

Figure 1-6 Data Byte Configuration for LPDDR4-only with DMI



1.4.2.3 PHY Configuration: LPDDR4/LPDDR5, no DMI pin

Figure 1-7 Data Byte Configuration supporting LPDDR4/LPDDR5 without DMI or read parity



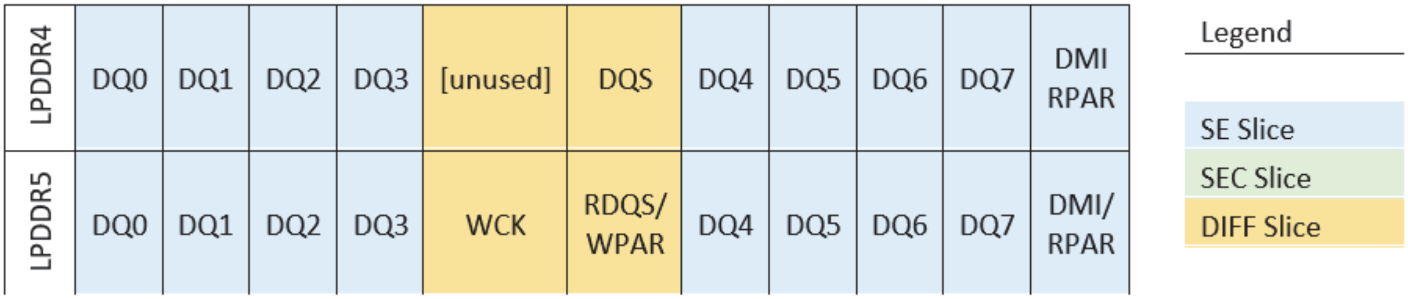
LPDDR4	DQ0	DQ1	DQ2	DQ3	[unused]	DQS	DQ4	DQ5	DQ6	DQ7
LPDDR5	DQ0	DQ1	DQ2	DQ3	WCK	RDQS/ WPAR	DQ4	DQ5	DQ6	DQ7

Legend

- SE Slice
- SEC Slice
- DIFF Slice

1.4.2.4 PHY Configuration: LPDDR4/LPDDR5, with DMI pin

Figure 1-8 Data Byte Configuration supporting LPDDR4/LPDDR5 with DMI



LPDDR4	DQ0	DQ1	DQ2	DQ3	[unused]	DQS	DQ4	DQ5	DQ6	DQ7	DMI RPAR
LPDDR5	DQ0	DQ1	DQ2	DQ3	WCK	RDQS/ WPAR	DQ4	DQ5	DQ6	DQ7	DMI/ RPAR

Legend

- SE Slice
- SEC Slice
- DIFF Slice

1.5 Achievable Speeds in Customer End-application

There are many factors that combine to affect the achievable speed using this IP in a customer's end-application. Proper planning of the entire memory subsystem (die, package, PCB, and external SDRAM configuration) in addition to early physical-based synthesis trials of the on-die implementation are key factors of a successful design, accompanied by visual reviews facilitated by Synopsys. At the die level, the choices made for floor-planning, compile options, standard cell libraries, and timing sign-off conditions play a large role in the achievable performance.

The following list of factors and Synopsys recommendations should be considered when designing an application to achieve the maximum supported speeds:

- Die, package, and PCB design:
    - The supported performance of a DDR memory system is greatly influenced by the design of the die (that is, the I/O pad frame), the package, the PCB, and the configuration of the external SDRAM on the PCB. Many factors impact the design, such as characteristic impedance of transmission lines, selections of drive and termination impedance, reflections, signal over-shoot and under-shoot, delay variance due to simultaneously switching outputs (SSO) or simultaneously switching inputs (SSI), signal cross-talk within package and PCB, Inter-Symbol Interference, etc.

      Careful design of the die, package, and PCB with associated SPICE-level signal integrity (SI) and power integrity (PI) analysis are primary methods to be able to accurately predict what to expect from a proposed system design.

      Synopsys provides documentation and models to assist in this work, offers a visual review to help look for potential issues, and can even be commissioned to perform the SI/PI analysis.
- External SDRAM configuration:
    - There are many possible configurations of external SDRAM that could be designed by a customer, although it does not mean they all work well especially at high speed.
        - For example, placing four DIMM slots on the PCB and populating with four single-rank DIMMs is not going to permit high speed operation as this loading is excessively high and the address/command lane will have an equivalent termination of four DIMM-mounted terminations in parallel, which may cause too great a reduction in the signal swing.
        - For example, a single-slot 2-rank UDIMM may provide superior signaling that would lead to greater probability to reach highest speed versus, for example, two DIMM slots each containing a single rank UDIMM.

      The configuration should be modeled and analyzed as part of the memory subsystem (die, package, PCB) design activities.
- Die floor-plan:
    - A successful physical implementation starts with the planning. In the case of Synopsys DDR PHY there is a soft-IP block (called the PHY Utility Block (PUB)) provided with the hard-IP blocks. The memory controller communicates with the PUB, and the PUB communicates with the PHY hard-IP blocks.

      A 72-bit PHY is very wide so signals need to traverse some distance. If, for example, the memory controller is placed far away from the PHY and/or the PUB is placed far from the PHY hard-IP blocks it may limit the achievable speed.

      Synopsys highly recommends customers provide proposed floor plans early in the project start to help provide recommendations.

- Choices of compile options:
  - The DDR PHY is highly flexible, providing many optional features to the SoC designers which are controlled by user-configurable verilog compile options. Some of these features may increase gate count which may lead to added congestion, or increase the depth of logic cones which may reduce timing slack.

    SoC designers should carefully consider what optional features are needed for their application versus enabling non-critical features because they might be useful at some point in the future. There are also many compile options related to pipe-line insertion to aid in timing closure, if required. If the SoC designer is unsure of the potential impact of some options, trial synthesis using the Synopsys-supplied synthesis environment can help collect comparative data, otherwise Synopsys can help by providing feedback.
- Choices of standard cell libraries:
  - There may be a variety of choices for standard cell library providers, and for any one provider there may be different types of libraries such as high-speed or high-density, and within these options there may be different threshold voltage options such as RVT or LVT, and there may be further choices of gate lengths to balance performance against leakage power.

    The DDR PHY (and possibly the associated memory controller) is a high-speed interface which may be a considerable component of the SoC area. This must be considered when choosing options available for the physical implementation. It is common to find the speed performance of some library providers to be higher than others, which must be considered the type of speeds being targeted when making library provider selections.

    Synopsys recommends access to LVT, and where applicable uLVT (sometimes called sLVT) in addition to RVT (sometimes called SVT) threshold libraries to help balance speed versus power consumption. Access to minimum gate length libraries is also recommended for high-speed implementations.

    The choice of high-density versus high-speed libraries is not always clear, since high-speed libraries are traditionally larger so a congested design may actually achieve superior results with a high-density library. This must be evaluated for the specific customer end-application.
- Choices of timing sign-off conditions:
  - Sign-off conditions include core voltage levels, fixed margins per cent on chip variation allowance, and other related parameters. In some companies there are guidelines presented to design teams for STA sign-off criteria of general logic designs (i.e. more aggressive margins to reduce chance to see any issues), which are not normally used for high-speed design. Some companies have a reduced set of sign-off criteria (i.e. less aggressive margins to enable timing closure) for high-speed design. Other companies apply less aggressive sign-off criteria (i.e. suitable for high-speed design) to their entire SoC.

    For implementing the DDR PHY at high speed, it is highly recommended to apply the less aggressive sign-off criteria. Core voltage can also aid in timing closure at high speed. The DDR PHY may be designed to support a range of core voltages, which in some cases may include some overdrive core voltage allowance.

    Check the applicable DDR PHY databook for its required specifications. If optionally supported by the DDR PHY, core overdrive voltage may be considered to help close timing on the critical paths of the logic circuits.

1.6 Timing Closure

The PHY can accommodate a wide variety of compile options to allow the user to set the desired configuration and functionality. The LPDDR5/4/4x PHY also permits the user to implement various floor plan styles. This LPDDR5/4/4x PHY is designed for very high data rates and the maximum attainable performance may be affected by the user's selected floor plan and PUB compile options. Enabling both a wide interface and many optional features simultaneously may result in timing closure difficulties. A non-optimal floor plan, especially for a very wide interface, may also impact timing closure capability.

It is strongly recommended the user perform preliminary physical-based synthesis using such EDA tools as Synopsys' Design Compiler Graphical to estimate the timing closure capability of both the estimated floor plan and the selected LPDDR5/4/4x PHY configuration at the start of the project before deciding on the desired floor plan and compile options for the LPDDR5/4/4x PHY.

In order to vet in advance possible timing closure issues, margining should be imposed during synthesis so as to emulate non-ideal circumstances (for example, clock skew, parasitics that vary from those described in wire models, path length-dependent derates, etc.) that will likely be encountered during downstream construction activities.

1.7 Process Information

Table 1-2 describes the process information for the DWC LPDDR5/4/4x PHY.

Note Contact your Synopsys sales representative for availability in alternate process nodes/variants

Table 1-2 Process Information

Foundry	Process	Variant	Core Voltage	I/O Oxide	Dielectric	Used Devices	Metal Layers
TSMC	7nm	FF	0.75V	1.8V	low-K	"Used Devices" on page 47	■ Metal layers used for the hard IP macrocells: ❑ 13M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2R

Note

- The hard-macros in this release include all metal layers up to and including MTOP which is the top-most thick copper layer. They do not include RDL or C4 bumps which would be added as part of the PHY hardening.
- Contact Synopsys for support when other Metal Stacks are required in the design.

1.8 PHY Cell Dimensions

Note Dimensions are as drawn. Apply process dependent scaling factor to generate dimensions on silicon.

Table 1-3 PHY Area

Macro	Width	Height	Units
dwc_ddrphyse_top_ew	195.168	41.04	um
dwc_ddrphydiff_top_ew	195.168	82.08	um
dwc_ddrphysec_top_ew	195.168	41.04	um
dwc_ddrphymaster_top_ew	365.598	328.32	um
dwc_ddrphyse_top_ns	41.04	195.12	um
dwc_ddrphydiff_top_ns	82.08	195.12	um
dwc_ddrphysec_top_ns	41.04	195.12	um
dwc_ddrphymaster_top_ns	328.32	368.88	um
dwc_ddrphy_decapvdd_1by4x1_ns	10.26	28.8	um
dwc_ddrphy_decapvdd_1x1_ns	41.04	28.8	um
dwc_ddrphy_decapvdd_4x1_ns	164.16	28.8	um
dwc_ddrphy_decapvddhd_1by4x1_ns	10.26	28.8	um
dwc_ddrphy_decapvddhd_1x1_ns	41.04	28.8	um
dwc_ddrphy_decapvddhd_4x1_ns	164.16	28.8	um
dwc_ddrphy_decapvddq_1by4x1_ns	10.26	28.8	um
dwc_ddrphy_decapvddq_1x1_ns	41.04	28.8	um
dwc_ddrphy_decapvddq_4x1_ns	164.16	28.8	um
dwc_ddrphy_decapvddqhd_1by4x1_ns	10.26	28.8	um
dwc_ddrphy_decapvddqhd_1x1_ns	41.04	28.8	um
dwc_ddrphy_decapvddqhd_4x1_ns	164.16	28.8	um
dwc_ddrphy_decap_ac1r_ns	410.4	28.8	um
dwc_ddrphy_decap_ac2r_ns	492.48	28.8	um
dwc_ddrphy_decap_master_ns	328.32	28.8	um
dwc_ddrphy_clamp_dbyte10_ns	410.4	57.6	um

Macro	Width	Height	Units
dwc_ddrphy_clamp_dbyte11_ns	451.44	57.6	um
dwc_ddrphy_clamp_dbyte12_ns	492.48	57.6	um
dwc_ddrphy_clamp_dbyte13_ns	533.52	57.6	um
dwc_ddrphy_clamp_ac1r_ns	410.4	57.6	um
dwc_ddrphy_clamp_ac2r_ns	492.48	57.6	um
dwc_ddrphy_clamp_master_ns	328.32	57.6	um
dwc_ddrphy_vaaclamp_master_ns	164.16	28.8	um
dwc_ddrphy_endcell_ns	10.26	252.72	um
dwc_ddrphy_rpt1ch_ns	10.26	252.72	um
dwc_ddrphy_rpt2ch_ns	10.26	252.72	um
dwc_ddrphy_decapvdd_1by4x1_ew	29.64	13.68	um
dwc_ddrphy_decapvdd_1x1_ew	29.64	41.04	um
dwc_ddrphy_decapvdd_4x1_ew	29.64	164.16	um
dwc_ddrphy_decapvddhd_1by4x1_ew	29.64	13.68	um
dwc_ddrphy_decapvddhd_1x1_ew	29.64	41.04	um
dwc_ddrphy_decapvddhd_4x1_ew	29.64	164.16	um
dwc_ddrphy_decapvddq_1by4x1_ew	29.64	13.68	um
dwc_ddrphy_decapvddq_1x1_ew	29.64	41.04	um
dwc_ddrphy_decapvddq_4x1_ew	29.64	164.16	um
dwc_ddrphy_decapvddqhd_1by4x1_ew	29.64	13.68	um
dwc_ddrphy_decapvddqhd_1x1_ew	29.64	41.04	um
dwc_ddrphy_decapvddqhd_4x1_ew	29.64	164.16	um
dwc_ddrphy_decap_ac1r_ew	29.64	410.4	um
dwc_ddrphy_decap_ac2r_ew	29.64	492.48	um
dwc_ddrphy_decap_master_ew	29.64	328.32	um
dwc_ddrphy_clamp_dbyte10_ew	59.28	410.4	um
dwc_ddrphy_clamp_dbyte11_ew	59.28	451.44	um
dwc_ddrphy_clamp_dbyte12_ew	59.28	492.48	um
dwc_ddrphy_clamp_dbyte13_ew	59.28	533.52	um

Macro	Width	Height	Units
dwc_ddrphy_clamp_ac1r_ew	59.28	410.4	um
dwc_ddrphy_clamp_ac2r_ew	59.28	492.48	um
dwc_ddrphy_clamp_master_ew	59.28	328.32	um
dwc_ddrphy_vaaclamp_master_ew	29.64	164.16	um
dwc_ddrphy_endcell_ew	254.448	13.68	um
dwc_ddrphy_rpt1ch_ew	254.448	13.68	um
dwc_ddrphy_rpt2ch_ew	254.448	13.68	um

1.9 Used Devices

Table 1-4 lists the primitive devices used by this IP

Table 1-4 Used Devices

LVS Model	Description
nch_18_mac	I/O 1.8V VT NMOS
nch_18ud12_mac	Thick Oxide UnderDrive 1.2V NMOS
nch_18ud15_mac	Thick Oxide UnderDrive 1.5V NMOS
nch_lvt_mac	CORE Low VT NMOS
nch_svt_mac	CORE Standards VT NMOS
nch_ulvt_mac	CORE Ultra Low VT NMOS
ndio_18_mac	IO N+/PW Junction DIODE
ndio_hia18_mac	CORE 2T ESD diode N+/PW
ndio_mac	N+/PW Junction DIODE
nmoscap	NMOS in N-Well Varactor
nmoscap_18	1.8V MOSCAP Varactor
pch_18_mac	I/O 1.8V VT PMOS
pch_18ud12_mac	Thick Oxide UnderDrive 1.2V PMOS
pch_lvt_mac	CORE Low VT PMOS
pch_svt_mac	CORE Standard VT PMOS
pch_ulvt_mac	CORE Ultra Low VT PMOS
pdio_hia18_mac	CORE 2T ESD diode P+/NW
rhim_nw	Poly Resistor
rm0w	M0 Resistor
rm1w	M1 resistor
rm2w	M2 resistor
rm3w	M3 resistor
rm4w	M4 resistor
rm5w	M5 resistor
rm6w	M6 resistor

1.10 DWC AP LPDDR5/4/4x PHY Deliverables

The following tables explain the structure of the deliverables directory.

Figure 1-9 DWC LPDDR5/4/4x PHY Deliverables Directory Structure

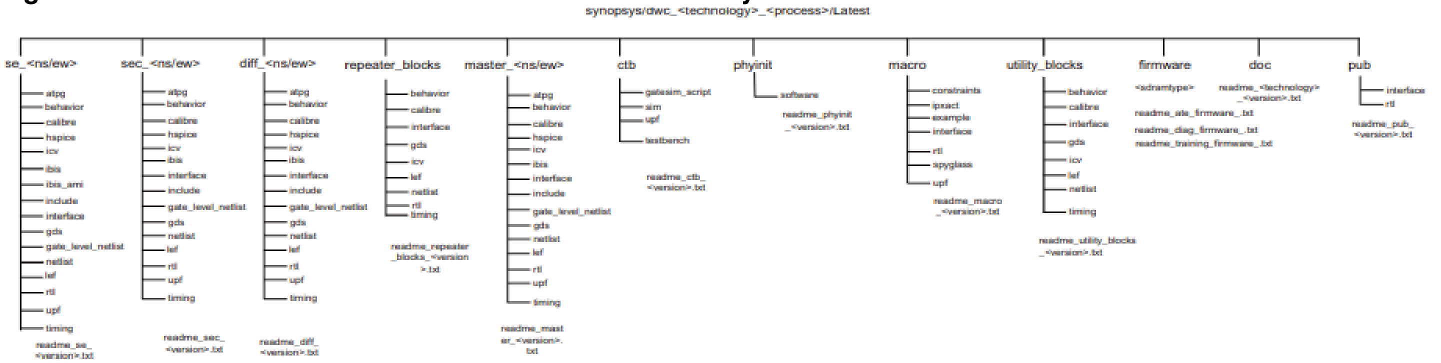


Table 1-5 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/se_<ns/ew>/Latest

Location in Download	Deliverable	Description
atpg	DFT files	Design for test files
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS
include	Verilog	Verilog include files
icv	Log files	ICV Log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
gds	GDSII	Layout of AC components
gate_level_netlist	Gate Level Netlist	Verilog format netlist
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
hspice	HSPICE Model	Encrypted HSPICE models of the I/O drivers
ibis	IBIS Model	IBIS model of the I/O drivers
ibis_ami	IBIS AMI Model files	IBIS AMI Simulation model and testbench files
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages
rtl	Verilog Model	Parameterized Verilog PUB source files
upf	UPF files	Power and power control intent files

Location in Download	Deliverable	Description
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-6 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/sec_<ns/ew>/Latest

Location in Download	Deliverable	Description
atpg	DFT files	Design for test files
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS
include	Verilog	Verilog include files
icv	Log files	ICV Log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
gate_level_netlist	Gate Level Netlist	Verilog format netlist
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
gds	GDSII	Layout of AC components
hspice	HSPICE Model	Encrypted HSPICE models of the I/O drivers
ibis	IBIS Model	IBIS model of the I/O drivers
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages
rtl	Verilog Model	Parameterized Verilog PUB source files
upf	UPF files	Power and power control intent files
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-7 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/diff_<ns/ew>/Latest

Location in Download	Deliverable	Description
atpg	DFT files	Design for test files
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS

Location in Download	Deliverable	Description
include	Verilog	Verilog include files
icv	Log files	ICV Log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
gate_level_netlist	Gate Level Netlist	Verilog format netlist
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
gds	GDSII	Layout of AC components
hspice	HSPICE Model	Encrypted HSPICE models of the I/O drivers
ibis	IBIS Model	IBIS model of the I/O drivers
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages
rtl	Verilog Model	Parameterized Verilog PUB source files
upf	UPF files	Power and power control intent files
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-8 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/master_<ns/ew>/Latest

Location in Download	Deliverable	Description
atpg	DFT files	Design for test files
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS
include	Verilog	Verilog include files
icv	Log files	ICV Log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
gate_level_netlist	Gate Level Netlist	Verilog format netlist
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
gds	GDSII	Layout of AC components
hspice	HSPICE Model	Encrypted HSPICE models of the I/O drivers
ibis	IBIS Model	IBIS model of the I/O drivers

Location in Download	Deliverable	Description
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages
rtl	Verilog Model	Parameterized Verilog PUB source files
upf	UPF files	Power and power control intent files
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-9 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/repeater_blocks/Latest

Location in Download	Deliverable	Description
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
icv	Log files	ICV Log files for DRC and LVS
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
gds	GDSII	Layout of AC components
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages
rtl	Verilog Model	Parameterized Verilog PUB source files
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-10 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/macro/Latest

Location in Download	Deliverable	Description
ipxact	xml	■ ipxact ❑ xEtensible Markup Language (XML) schema for meta-data documenting IP registers
example	Example	This folder includes the following folders: ■ syn: Design Compiler Synthesis scripts
rtl	phy_top rtl	Parameterized Verilog top level PHY netlist files
upf	UPF files	Power and power control intent files
constraints	tcl	Generic tcl constraints used in PrimeTime and Design Compiler

Location in Download	Deliverable	Description
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
spyglass	Spyglass files	Spyglass lint and cdc log files

Table 1-11 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/ctb/Latest

Location in Download	Deliverable	Description
gatesim_ script	Compilation Scripts	Gate level netlists compilation/annotation support
sim	Simulation Script	RTL simulation scripts
upf	UPF files	Power and power control intent files
testbench	Verification Environment	This folder includes the following folders: ■ models: PHY components and SDRAM models ■ tb: Testbench Verilog files ■ tc: Testcases Verilog files

Table 1-12 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/phyinit/Latest

Location in Download	Deliverable	Description
software	C code	Host processor PHY initialization code

Table 1-13 Documentation Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/utility_blocks/Latest

Location in Download	Deliverable	Description
behavior	Verilog Model	Verilog behavioral model
calibre	Log Files	Calibre log files for DRC and LVS
interface	Verilog	Contains a bounding box only description, in Verilog (i.e. pins only)
icv	Log files	ICV Log files for DRC and LVS
netlist	LVS Netlists	SPICE format netlist used in conjunction with the GDSII to run LVS
gds	GDSII	Layout of AC components
lef	LEF Files	File contains AC component size, signal sizes and locations, and metal blockages

Location in Download	Deliverable	Description
timing	Timing Models	Synopsys .lib and .db format timing models for different operating modes, which are provided for standard process, temperature, and voltage corners. If applicable, Standard Delay Format (SDF) timing file for multiple corners

Table 1-14 Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/firmware/Latest

Location in Download	Deliverable	Description
ate	Firmware Images	ATE Firmware images for multiple SDRAM types
diagnostic	Firmware Images	Diagnostic Firmware images for multiple SDRAM types
training	Firmware Images	Training Firmware images for multiple SDRAM types

Table 1-15 Documentation Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/pub/Latest

Location in Download	Deliverable	Description
interface	Verilog	Contains a bounding box only description, in Verilog (that is, pins only)
rtl	Verilog Model	Parameterized Verilog PUB source files

1.11 Definition of Terms and Acronyms

Table 1-16 Definition of Terms and Acronyms

Term	Description
AC	Address/command
ACSM	Address Command State Machine
CSR	Control and Status Registers
DFI	DDR PHY Interface
DFICLK	DDR PHY Interface Clock Clock reference for all mission mode interface signals.
DTSM	Data Training State Machine
MC	Memory Controller – Interfaces with the PHY to provide operational commands, address and data.
PMU	PHY microcontroller unit, same as uCtl
PUB	DWC PHY Utility Block
PRBS	Pseudo Random Binary Sequence
PState	The PHY supports multiple power states, both Active and Standby. A power state (or PState) is a combination of memory clock frequency, driver strengths, termination and timing. The PHY supports 2 active power states, labelled PS0 and PS1. The PHY also supports 5 standby (inactive) power states, labelled DFI LP (3 states) Fast Standby (LP2), and IO Retention(LP3). Active power states are changed by utilizing the DFI Frequency Change protocol, via the "dfi_init_start", "dfi_frequency[]", and "dfi_init_complete" signals.
SE Slice	Single-ended highs-speed PHY+IO signal block
SEC Slice	Single-ended CMOS PHY+IO signal block
DIFF Slice	Differential PHY+IO signal pair block
uCtl	Micro-Controller
FSP	Frequency Set Point – Stored, trained values for specific operational frequencies

2

Architectural and Functional Description

The following sections are included in this chapter:

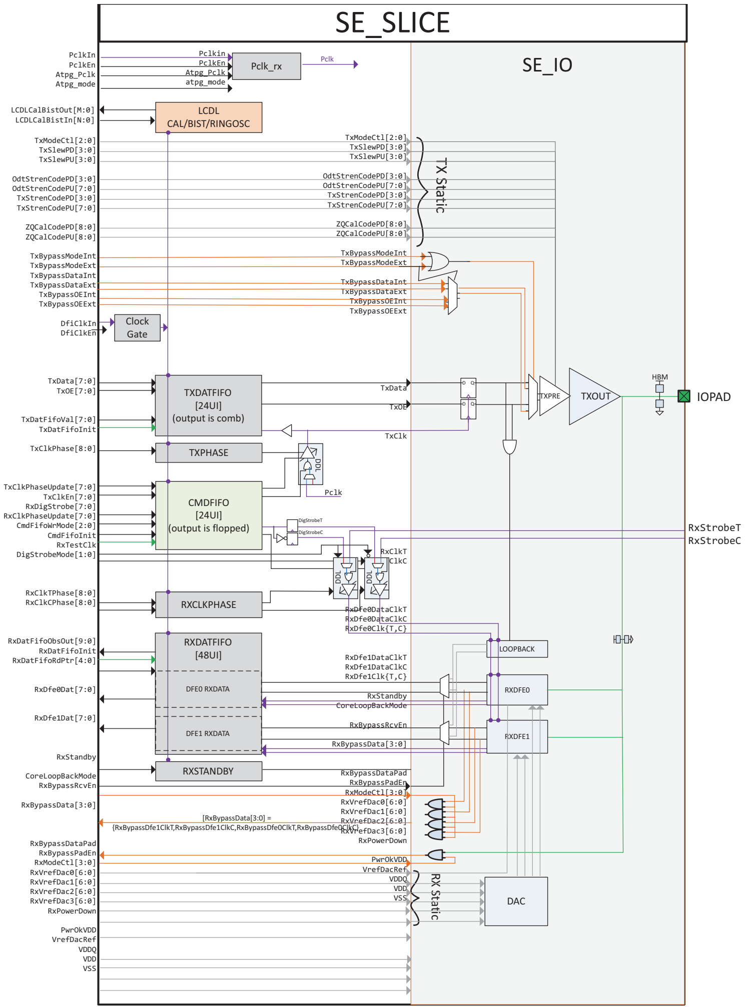
2.1 Bit Slices

2.1.1 SE Slice

The SE Slice (short for Single-Ended Slice) is a macro used to implement a serializer/de-serializer (SerDes) for a single-ended IO on the interface to DRAM. The Table 2-1 on page 57 summarizes use cases for the SE Slice.

Figure 2-1 shows a diagram of the SE Slice.

Figure 2-1 SE Slice Diagram



IMPL DETAIL ::
* DFICLK skew across slice
Must be <0.5*PCLK_period
* All muxes on bypass paths must
be glitchless when the non-
selected input changes

RxModeCtl[3:0]
XXX0– DFE Disabled
XXX1– DFE Enabled

SE Slice is comprised of the SE_IO cell, Rx and Tx Data FIFO, Cmd FIFO interface and logic for LCDL calibration, BIST and Ring Oscillator.

Table 2-1 SE Slice Usage

Region	LPDDR4 Use	LPDDR5 Use
Address/Command	CA[5:0], CS[n]	CA[6:0]
Byte Lane	DQ[7:0]	DQ[7:0]
Byte Lane	DMI	DBI pin (DRAM-programmable functions)

Transmit data from the DfiClk domain needs to be passed on the PClk_in domain. (Cmd FIFO and Tx Data Lane FIFO are serializer FIFOs which converts the signal from the DfiClk Domain to PClk_in domain.

DRAM read data is returned to the PUB via RX Data FIFOs. RxRcvDataEven is written into the FIFOs on the positive edges of RxDllClk, which corresponds to beats 0, 2, 4 and 6 of the DQS signal. RxRcvDataOdd is written on the positive edges of RxDllClkx, for beats 1, 3, 5 and 7. Data is removed from the FIFO on a positive edge of DFICLK when RxDatVal[0]=1; this indicates that the max-read-latency counter in the PUB has expired.

Table 2-2 Data Carried in SE Slice CmdFifo

Command FIFO (CMDFIFO)		
DFICLK domain	PClk_in domain	Output signal function
Input from PUB	Output FIFO signal in Slice	
TxClkPhaseUpdate[7:0]	TxClkPhaseEn	Used to load the fine delay values into the TX LCDL.
TxClkEn[7:0]	TxPclkEn	Causes a DRAM write to occur. Allows the pclk to enter the LCDL and ultimately drive write signals to the IO pins. This also acts as a read clock for TXDATAFIFO.
RxDigStrobe[7:0]	RxStrb	Internal Read DQS Strobe used in lieu of Read DQS strobe from DRAM when CDR is enabled (Use only supported for LPDDR5 mode in PUB 1.0 only)
RxClkPhaseUpdate[7:0]	RxClkPhaseEn	Used to load the fine delay values into the RX LCDL, RDQSt and RDQSc. This input can be tied off when the slice is used for AC lanes because RxClk LCDL is unused in AC lanes.

In the CmdFifo, there is an asynchronous path from the data flops, clocked by DfiClk, to a FIFO output on PClk. The max_delay on this path is an important timing constraint for PHY performance. Call this value DfiClkToPclkDelay. Initial target for DfiClkToPclkDelay is 250 ps.

Table 2-3 Data carried in SE Slice TxDataFifo

Data Lane FIFO (TXDATAFIFO)		
DFICLK domain	**PClk_in domain**	**Output Signal Function**
Input from PUB	**Output FIFO signal in slice**	
TxDataLn0[7:0]	TxData[0]	The value to be driven to the IO.
TxEnLn0[7:0]	TxEn[0]	The drive-enable for the lane. If this is zero, the output pin will be tri-stated.

In the TxDataFifo, there is an asynchronous path from the data flops, clocked by DfiClk, to a FIFO output on PClk. The max_delay on this path is an important timing constraint for PHY performance. Call this value DfiClkToPclkDelay.

Table 2-4 Data carried in SE Slice RxDataFifo

Read Data FIFO (RXDATAFIFO)		
PClk_in domain	PClk_in domain	Output signal function
FIFO Input from Slice	Output to PUB	
RxRcvDataClkT RxRcvDataClkC	RxDat0 [7:0]	Parallelized read data. This FIFO typically contains data captured by useful strobe edges as well as non-useful strobe (i.e., edges that do not capture real DQ data from DRAM); it also captures from 2 receivers for each bit, assuming the PUB will implement a DFE function to choose between those. The PUB is responsible for discarded unmeaningful data captured here.

External transmit bypass (signals name TxBypass*Ext) paths provide the SoC with direct transmit access to the IOs. Internal transmit bypass (signals named TxBypass*Int) provide the SoC with direct transmit access to the IOs for. Muxes that select amongst external transmit bypass, internal transmit bypass, and mission-mode paths must all be glitchless with the non-selected input(s) transition.

2.1.1.1 SE Slice Pin List

For more details on SE Slice pin list, refer to "Signal Overview" on page 99.

2.1.2 DIFF Slice

The Diff Slice (short for Differential Slice) is a macro used to implement a serializer/de-serializer for differential IOs on the interface to DRAM. There is also an option to use it as two single-ended outputs. There are 3 use cases for this macro, as described in Table 2-5 on page 58.

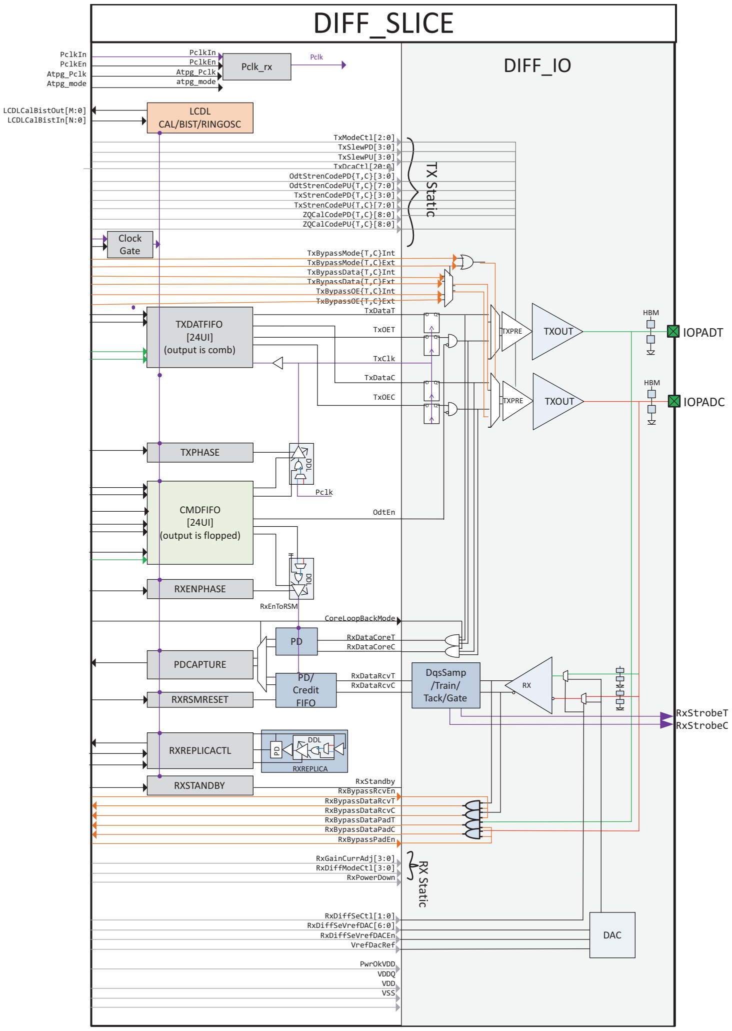
Table 2-5 Diff Slice Usage

Region	LPDDR4 Use	LPDDR5 Use
Address/Command	CK_t/CK_c	CK_t/CK_c

Region	LPDDR4 Use	LPDDR5 Use
Byte Lane	DQS_t/DQS_c	RDQS_t/RDQS_c / [one DRAM-programmable single-ended output function]
Byte Lane	[not instantiated in LPDDR4-only designs; unused in designs supporting LPDDR5]	WCK_t/WCK_c

Figure 2-2 shows a diagram of the DIFF Slice.

Figure 2-2 Diff Slice Diagram



DIFF Slice is comprised of the DIFF_IO cell, Tx Data FIFO, Cmd FIFO, RxStrobeEn interface, replica receiver (with associated LCDL and phase detector), and logic for LCDL calibration, BIST and Ring Oscillator.

Transmit Data interface is similar to the SE Slice. There are two instances of the Transmit Data Interface for each of DQSt and DQSc. Cmd FIFO is a free running FIFO generates the RxStrobeEn signal which causes the DQS to enter in the read data capture mode and delay update for to latch the delay for the RxStrobeEn Signal.

The replica receiver and associated phase detector will be used by the PUB to track VT drift in all single-ended unbalanced receivers.

Table 2-6 Data carried in DIFF Slice CmdFifo

Command FIFO (CMDFIFO)		
DFICLK domain	PClk_in domain	Output signal function
Input from PUB	Output FIFO signal in Slice	
TxClkPhaseUpdate[7:0]	TxClkPhaseEn	Used to load the fine delay values into the TX LCDL.
TxClkEn[7:0]	TxPclkEn	Causes a DRAM write to occur. Allows the pclk to enter the LCDL and ultimately drive write signals to the IO pins. This also acts as a read clock for TXDATAFIFO.
OdtEn[7:0]	OdtEn	Enables read signal termination within the PHY
RxStrobeEn[7:0]	RcvEn	Read DQS Gate.
RxStrobeEnPhaseUpdate[7:0]	RxStrobeEnPhase En	Used to load the fine delay values into the RxStrobeEn LCDL. This input can be tied off when the slice is used for AC lanes because RxEn LCDL is unused in AC lanes.

In the CmdFifo, there is an asynchronous path from the data flops, clocked by DfiClk, to a FIFO output on PClk. The max_delay on this path is an important timing constraint for PHY performance. Call this value DfiClkToPclkDelay.

Table 2-7 Data carried in DIFF Slice TxDataFifo_0

Data Lane FIFO (TXDATAFIFO_0)		
DFICLK domain	PClk_in domain	Output signal function
Input from PUB	Output FIFO signal in slice	
TxDataLn0[7:0]	TxData[0]	The value to be driven to the IO. This will be used to Tx DQS_t.
TxEnLn0[7:0]	TxEn[0]	The drive-enable for the lane. If this is zero, the output pin will be tri-stated.

In the TxDataFifo, there is an asynchronous path from the data flops, clocked by DfiClk, to a FIFO output on PClk. The max_delay on this path is an important timing constraint for PHY performance. Call this value DfiClkToPclkDelay.

Table 2-8 Data carried in DIFF Slice TxDataFifo_1

Data Lane FIFO (TXDATAFIFO_1)		
DFICLK domain	PClk_in domain	Output signal function
Output FIFO signal in slice	Input from PUB	
TxDataLn1[7:0]	TxData[1]	The value to be driven to the IO. This will be used to Tx DQS_c.
TxEnLn1[7:0]	TxEn[1]	The drive-enable for the lane. If this is zero, the output pin will be tri-stated.

In the TxDataFifo, there is an asynchronous path from the data flops, clocked by DfiClk, to a FIFO output on PClk. The max_delay on this path is an important timing constraint for PHY performance. Call this value DfiClkToPclkDelay.

External transmit bypass (signals name TxBypass*Ext) paths provide the SoC with direct transmit access to the IOs. Internal transmit bypass (signals named TxBypass*Int) provide the SoC with direct transmit access to the IOs for. Muxes that select amongst external transmit bypass, internal transmit bypass, and mission-mode paths must all be glitchless with the non-selected input(s) transition.

2.1.2.1 DIFF Slice Pin List

For more details on DIFF pin list, refer to "Signal Overview" on page 99.

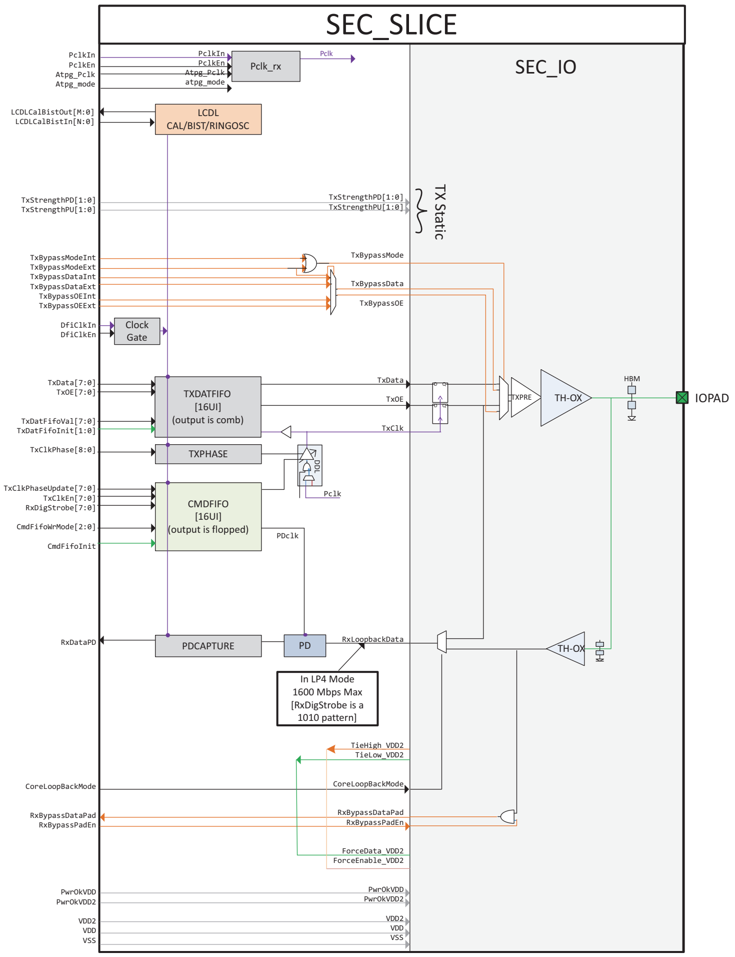
2.1.3 SEC Slice

The SEC slice (short for single-ended CMOS) is a macro used to implement a serializer for a single-ended CMOS output on the DRAM interface. Table 2-9 summarizes use cases for the SE Slice. A diagram of the SEC Slice is shown Figure 2-3 on page 62:

Table 2-9 SEC Slice Usage

Region	PHY Bump	LPDDR4 Use	LPDDR5 Use
Embedded in Master macro	BP_MEMRESET_L	Reset_n	Reset_n
Address/Command	BP_DFI0_LP4CKE_LP5CS[n] BP_DFI1_LP4CKE_LP5CS[n]	CKE[n]	CS[n]

Figure 2-3 SEC Slice Diagram



SEC Slice will be comprised of the SEC_IO cell, Tx Data FIFO, Cmd FIFO interface and logic for LCDL calibration, BIST and Ring Oscillator.

Transmit data from the in the DfiClk domain needs to be passed on the PClk_in domain. Cmd FIFO and Tx Data Lane FIFO are serializer FIFO which converts the signal from the DfiClk Domain to PClk_in domain.

Table 2-10 Data carried in SEC Slice TxdataFif

Data Lane FIFO (TXDATAFIFO)		
DFICLK domain	PClk_in domain	Output signal function
Input from PUB	Output FIFO signal in slice	
TxDataLn0[7:0]	TxData[0]	The value to be driven to the IO.
TxEnLn0[7:0]	TxEn[0]	The drive-enable for the lane. If this is zero, the output pin will be tri-stated.

Table 2-11 Data carried in SEC Slice CmdFifo

Command FIFO (CMDFIFO)		
DFICLK domain	PClk_in domain	Output signal function
Input from PUB	Output FIFO signal in Slice	
TxClkPhaseUpdate[7:0]	TxClkPhaseEn	Used to load the fine delay values into the TX LCDL.
TxClkEn[7:0]	TxPclkEn	Causes a DRAM write to occur. Allows the pclk to enter the LCDL and ultimately drive write signals to the IO pins. This also acts as a read clock for TXDATAFIFO.
RxDigStrobe[7:0]	RxStrb	Internal Strobe to capture the Loopback data.

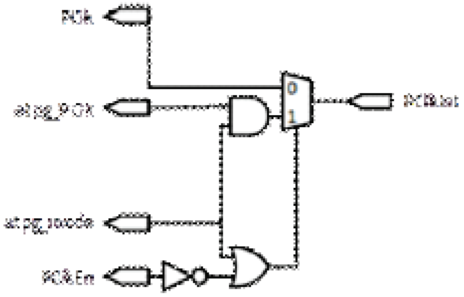
External transmit bypass (signals name TxBypass*Ext) paths provide the SoC with direct transmit access to the IOs. Internal transmit bypass (signals named TxBypass*Int) provide the SoC with direct transmit access to the IOs for. Muxes that select amongst external transmit bypass, internal transmit bypass, and mission-mode paths must all be glitchless with the non-selected input(s) transition.

2.1.3.1 SEC Slice Pin List

For more details on SEC Slice pin list, refer to "Signal Overview" on page 99.

2.1.4 Bit Slice component: Pclk_RX CKT

Figure 2-4 Pclk_RX CKT Diagram



2.1.5 Bit Slice component: Tx Data FIFO module "dwc_ddrphy_dlanetxfifo"

This module is the 8 to 1 serialize FIFO, with write entries populated based on the enable bit set. It is used to transfer data from the DFI clock domain to the PClk_in domain in all slices (DIFF, SE, and SEC). It is designed to be used in any arbitrary ratio of DfiClk:PClk from 1:1 to 1:8.

2.1.5.1 Ports

Table 2-12 Ports of Bit Slice TxDataFifo (dwc_ddrphy_dlanetxfifo)

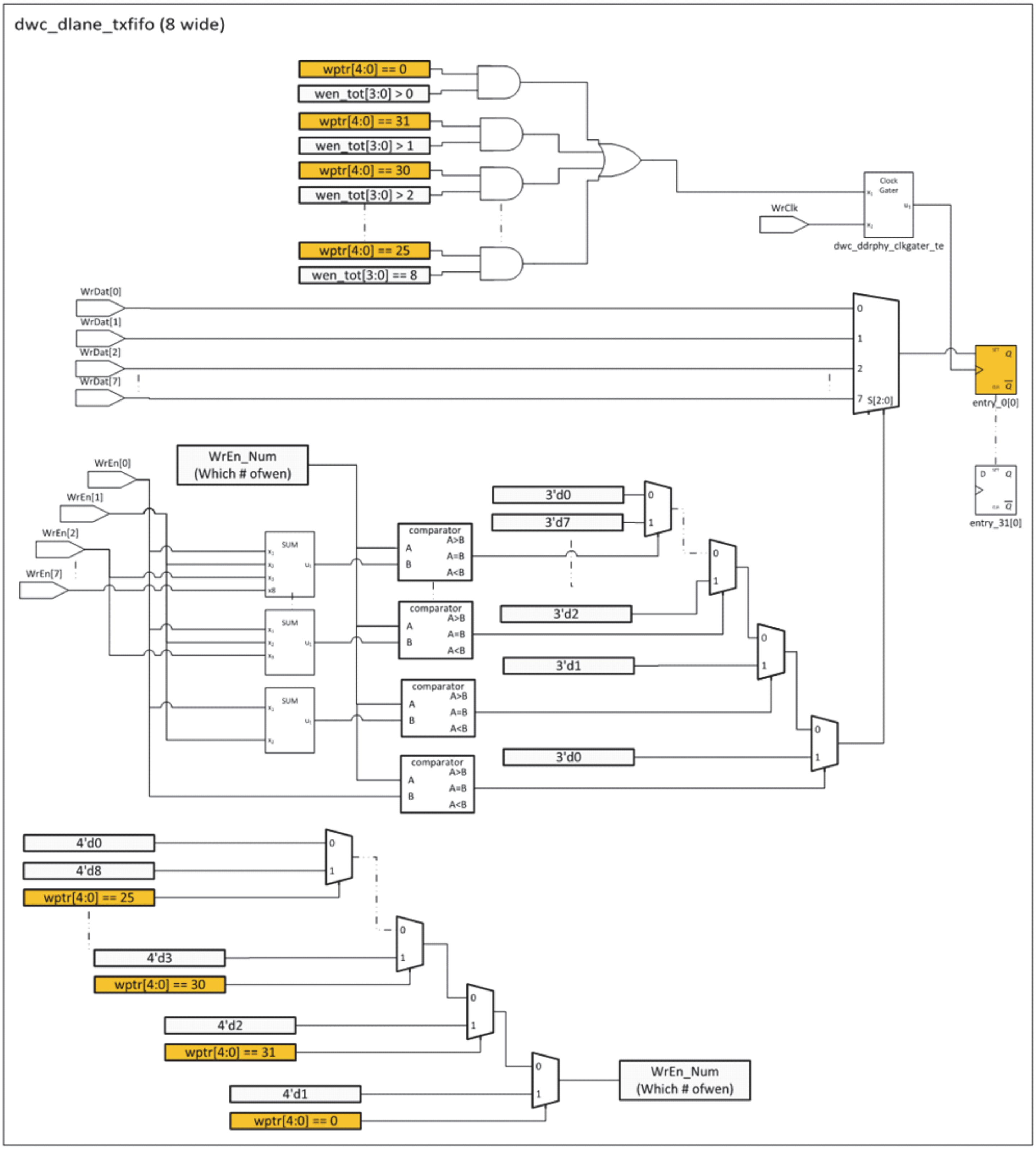
Port Name		Width	Direction	Description
	Write Interface			
WrClk		1	input	Write FIFO Clock
WrDat*		8	input	Write Data
WrEn		8	input	Write Data Enable
WrPtrInit		1	input	Async Write Pointer Reset
	Read Interface			
RdClk		1	input	Read FIFO Clock
RdDat[a]		1	output	Read Data, serialized 8 bit Write Data.
RdPtrInit		1	input	Async Read Pointer Reset

a. There can be more than one set of WrDat and RdDat.

2.1.5.2 Implementation

- FIFO entry needs to be populated for each WrDat bit corresponding to valid WrEn bit.
- 1 FIFO entry needs to be read at each RdClk
- FIFO Depth:
- 16 entries. 4dficlk * 4UI/dficlk = 16 entries. 16 Flops.
- FIFO Depth:
- 16 entries. 2dficlk * 8UI/dficlk = 16 entries. 16 Flops.
- Write Pointer: Traditional Binary Counter
- Read Pointer: One Hot - Shift register.
- Example:
  - If WrEn = 8'hF0 and WrPtr is at 0
  - Four Entries needs to be populated.
  - Entry 0 must contain value corresponding to UI4 and so on.
  - When there is read from the FIFO, Entry0 will be read with the UI4 data and not the invalid data at UI0.

Figure 2-5 TxDataFifo (dwc_ddrphy_dlanetxfifo) Write Structure Block Diagram



2.1.6 Bit slice component: Cmd FIFO module “dwc_ddrphy_cmdfifo”

This module is the 8 to 1 serialize FIFO, with write entries populated with write clock. It is used to transfer data from the DFI clock domain to the PClk_in domain in all slices (DIFF, SE, and SEC). It is designed to be used in any arbitrary ratio of DfiClk:PClk from 1:1 to 1:8.

2.1.6.1 Ports

Table 2-13 Ports of Bit Slice CmdFifo (dwc_ddrphy_cmdfifo)

Port Name	Width	Direction	Description
Write Interface			
WrClk	1	input	Write FIFO Clock
WrDat	8	input	Write Data
WrPtrInit	1	input	Async Write Pointer Reset
WrMode	3	input	‘b001: This is 1:2 Mode, only lower 2 bit of WrDat are valid ‘b010: This is 1:4 Mode, only lower 4 bit of WrDat are valid ‘b100: This is 1:8 Mode, 8 bit of WrDat are valid
Read Interface			
RdClk	1	input	Read FIFO Clock
RdDat	1	output	Read Data, serialized 8 bit Write Data.
RdPtrInit	1	input	Async Read Pointer Reset

2.1.6.2 Implementation

- FIFO entry needs to be populated for each Write FIFO Clock.
  - For example: Only lower 2 bits of the WrDat needs to be populated in the FIFO entry (2 entries) if WrMode = 3’b00 1.
- One FIFO entry needs to be read at each RdClk
- FIFO Depth: 16 entries. 2dficlk * 8UI/dficlk = 16 entries. 16 Flops.
- Write Pointer: Traditional Binary Counter
- Read Pointer: Traditional Binary Counter.
- This is Standard FIFO implementation, where 8 entries are populated with WrDat[7:0] at each WrClk and each entry is read at the RdClk to RdDat.

2.1.7 Bit slice component: RXDATA FIFO module “dwc_ddrphy_rxdatafifo”

2.1.7.1 Ports

Table 2-14 Ports of Bits Slice RxDataFifo (dwc_ddrphy_rxdatafifo)

Port Name	Width	Direction	Description
Write Interface			
WrClk	2	input	Write FIFO Clock
dq_data_odd	1	input	Odd Write Data
dq_data_even	1	input	Even Write Data
RxDatVal	4	input	Value program indicates the number UI entries to be read from the FIFO. Value of 0 indicates no read access. Value of N indicates RxDat[N-1:0] are read.
Read Interface			
RdClk	1	input	Read FIFO Clock
RxDat	12	output	Read Data, Maximum 12 UI data.
RxPtrInit	1	input	Async Read Pointer Reset
Read FIFO Snooping			
csrRxFifoRdPtrOvr	1	input	Enabls seeding of the RdPtr with value csrRxFifoRdPtr
csrRxFifoRdPtr	4	input	Seed value of the RdPtr
csrRxFifoRdLoc	5	output	Current location of the read pointer
csrRxFifoWrLocOdd	5	output	Current location of the write pointer odd-phase UI
csrRxFifoWrLocEvn	5	output	Current location of the write pointer odd-phase UI

2.1.7.2 Implementation

- 2 Bits of WrClk are {WrClkEvn, WrClkOdd}
- WrClkOdd is inverted and used. “WrClkOddX”
- 2 sets of write pointer are maintained for even/odd and incremented with WrClkEven and WrClkOddX respectively.
    - Write pointers 0 to 23
- FIFO Detpth or number of entries = 48 UI = 24 * 2 UI. (even/odd)
- Each entry will have its own clock so it can be gated.
- At a given time only 2 entries will be populated.

  - If WrEPtr = 0, Entry 0 will be populated with dq_data_even at WrClkEven
  - If WrOPtr = 0, Entry 1 will be populated with dq_data_odd at WrClkOddX
  - If WrEPtr = 1, Entry 2 will be populated with dq_data_even at WrClkEven
  - If WrOPtr = 1, Entry 3 will be populated with dq_data_odd at WrClkOddX
  - Now, of the 48 entries 4 entries have valid data populated with {odd,even,odd,even}
- Read Data interface is 12UI wide where maximum of 12 FIFO entries can be read.
- Value programmed in RxDatVal defines number of entries to pop.

2.1.8 Bit slice component: LCDL “dwc_ddrphy_lcdl”

LCDL ("local calibrated delay line") delay cells are used in the DIFF/SE/SEC slices to achieve fractional UI timing of the DRAM interface signals and doubles the purpose in measuring the steps required for 1UI shift.

DIFF Slice has two LCDL for Transmit DQS and Timing the gate for read DQS. SE Slice has 3 LCDL for Read DQSt, Read DQSc and Transmit Single ended DQ/DM or CA signal. SEC Slice has 1 LCDL for transmit Single ended signal.

The delay provided by an LCDL consists of two parts:

1. A non-configurable delay that is "zerodelay" (also known as “insertion delay”)
2. A configurable delay “delay_sel”[9:0]

The total delay is given by: LCDL_delay = (delay_sel[9:0] * stepsize) + zerodelay;

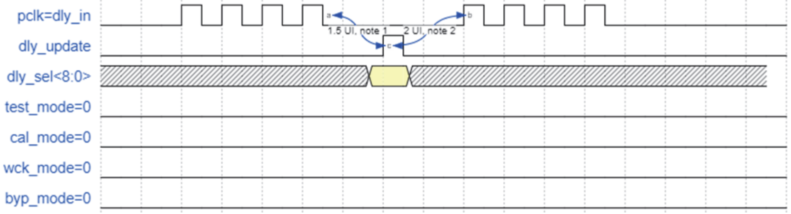
2.1.8.1 Functional Modes Truth Table

Table 2-15 LCDL Functional Mode truth Table

wck_mode	test_mode	cal_mode	LCDL input	Mode of Operation	dly_out	dto
0	0	0	dly_in	Mission (DQS output)	dly_in	0
1	X	X	wck_in	WCK (Write Clock output)	wck_in	0
0	1	X	dti	Test	dti	dti
0	0	1	cal_clk	Calibration	cal_clk	cal_clk

2.1.8.2 LCDL Timing to update Phase for TxDQ/TxDQS LCDLs

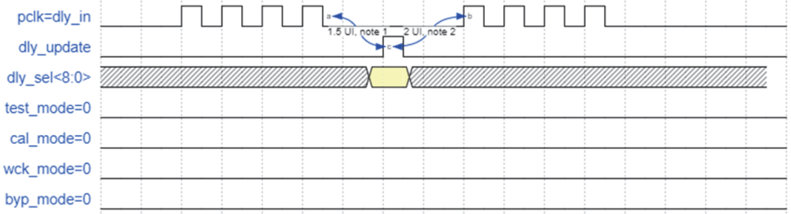
Figure 2-6 Timing Diagram for LCDL Phase Updates for TxDQ/TxDQS



- Note 1. The last falling edge of dly_in must pass through the LCDL before updating phase. We have 1.5UI from the last falling edge of dly_in -> rising edge of dly_update. This must account for the worst case 1 UI phase setting, so we have to meet Insertion delay < 0.5UI.
- Note 2. We have 2 UI from the rising edge of dly_update to the first valid edge of dly_in. Out of this 2 UI, the circuit takes 1.5UI for the decoder delay and the rest 0.5UI is for Implementation.
- Note 3. “dly_in_en” pulse width is not accurate representation of any transaction. Timing diagram above is addressing the spacing between rise/fall edges of “dly_in_en” wrt rising edge of “dly_update

2.1.8.3 LCDL Timing to update Phase for RxDQS_t/_c

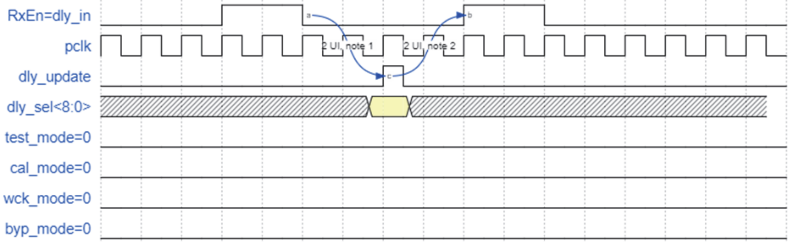
Figure 2-7 Timing Diagram for LCDL Phase Upates for RxDQS_t/_c



- Note 1. The last falling[rising] edge of DQS_t[c] has to pass through the LCDL before updating phase. We have 2UI from the last falling edge of dly_in(DQS_t/c) -> rising edge of dly_update. This has to account for the worst case 1 UI phase setting.
- Note 2. We have 2 UI from the rising edge of dly_update to the first valid edge of dly_in(DQS_t/c). Out of this 2 UI, the circuit takes 1.5UI for the decoder delay and the rest 0.5UI is for Implementation.

2.1.8.4 LCDL Timing for RxStrobeEn LCDL Phase Update

Figure 2-8 Timing Diagram for LCDL Phase Update for RxStrobeEn



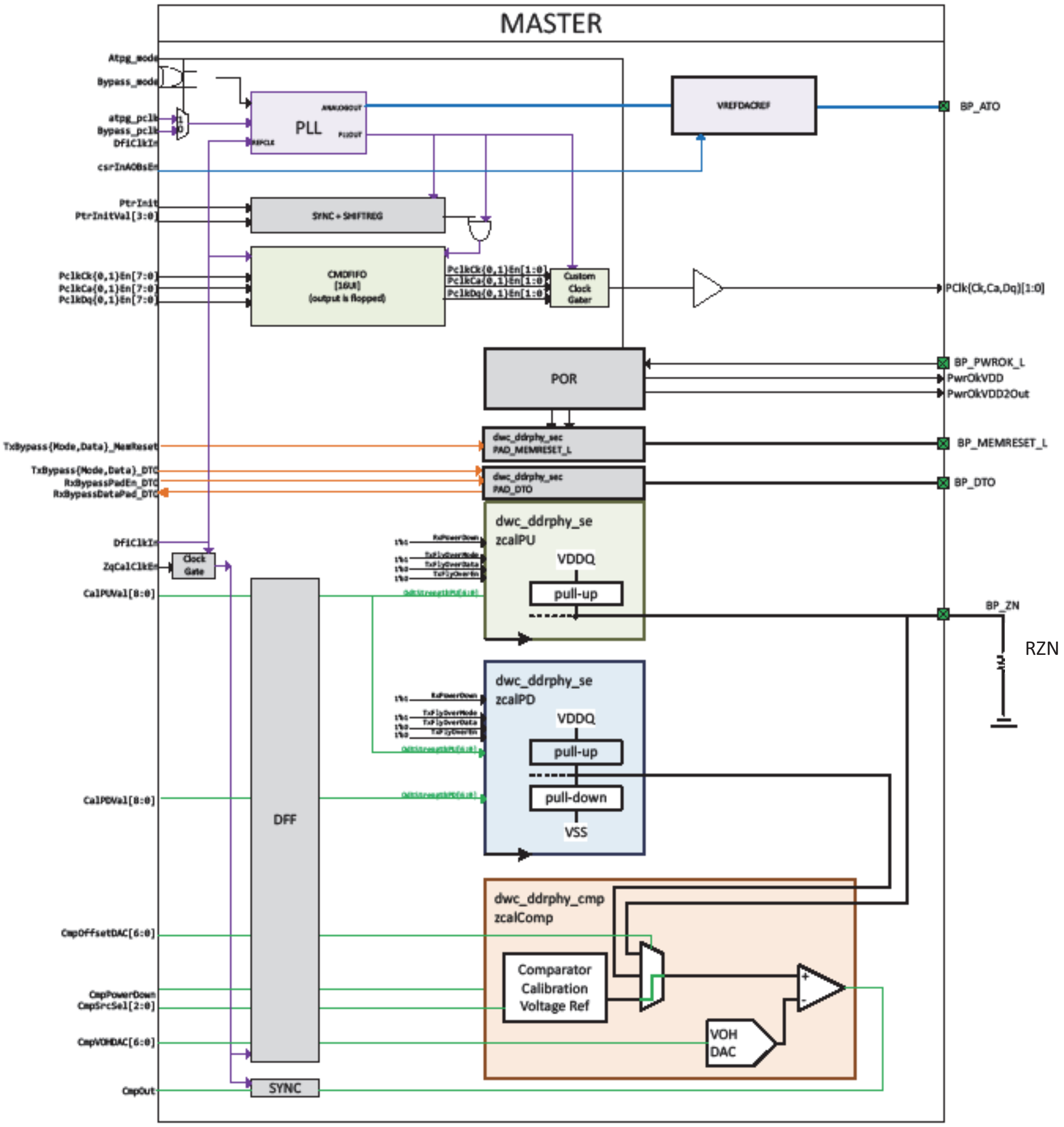
- Note 1. The last falling edge of RxStrobeEn has to pass through the LCDL before updating phase. We have 2UI from the last falling edge of RxStrobeEn -> rising edge of dly_update. This has to account for the worst case 1 UI phase setting.
- Note 2. We have 2 UI from the rising edge of dly_update to the first valid edge of dly_in(RxStrobeEn). Out of this 2 UI, the circuit takes 1.5UI for the decoder delay and the rest 0.5UI is for Implementation.
- Note 3. “dly_in_en” pulse width is not accurate representation of any transaction. Timing diagram above is addressing the spacing between rise/fall edges of “dly_in_en” wrt rising edge of “dly_update”

2.2 Master

The master is a single macro instantiated just once for each PHY instance. The Master includes:

- Custom subcircuits to support clock generation, including one PLL and Initialization logic to generate PclkCa and PclkDq, out from PllRefClk or PllBypClk or Atpg_pclk.
- Custom subcircuits to support Impedance Calibration, including two SE slices and one dwc_ddrphy_cmpana instance.
- Custom sub-circuits to support power-on Reset (POR).
- IO bumps for: BP_ZN, BP_PWROK (optional), BP_ATO, BP_DTO and BP_MEMRESET_L

Figure 2-9 Master HardIP



2.2.1 Master Pin List

For more details on Master pin list, refer to "Signal Overview" on page 99.

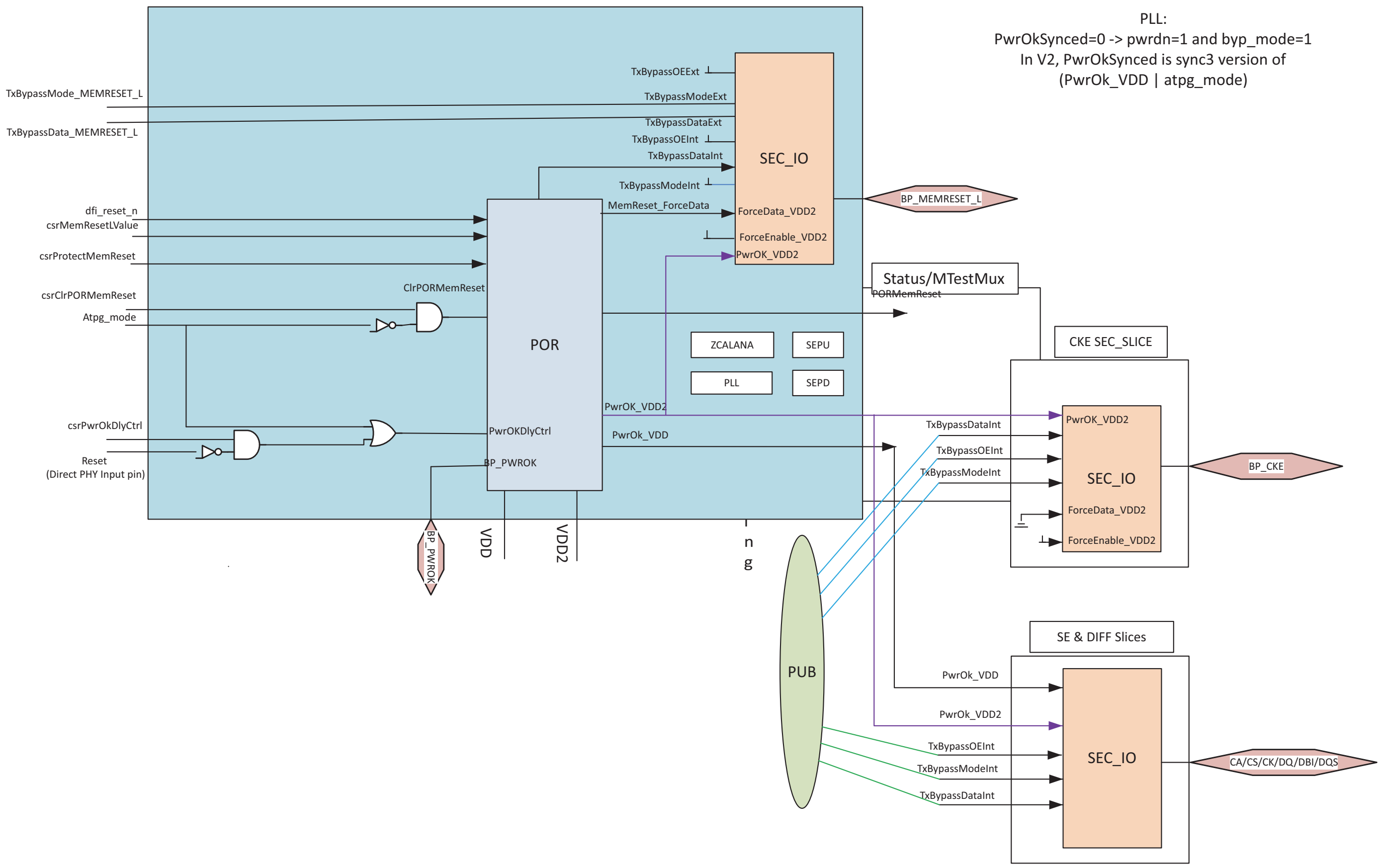
2.2.2 Power-Up Initialization

The Master HardIP is responsible for generating PwrOK signals to all Slices in PHY and ensuring the MEMRESET_L and CKE pins in a known valid state during power-up and retention.

2.2.2.1 Block Diagram

High level logic block diagram is shown in Figure 2-10.

Figure 2-10 BP_MEMRESET_L Generation Circuit Diagram



2.2.2.2 POR CKT

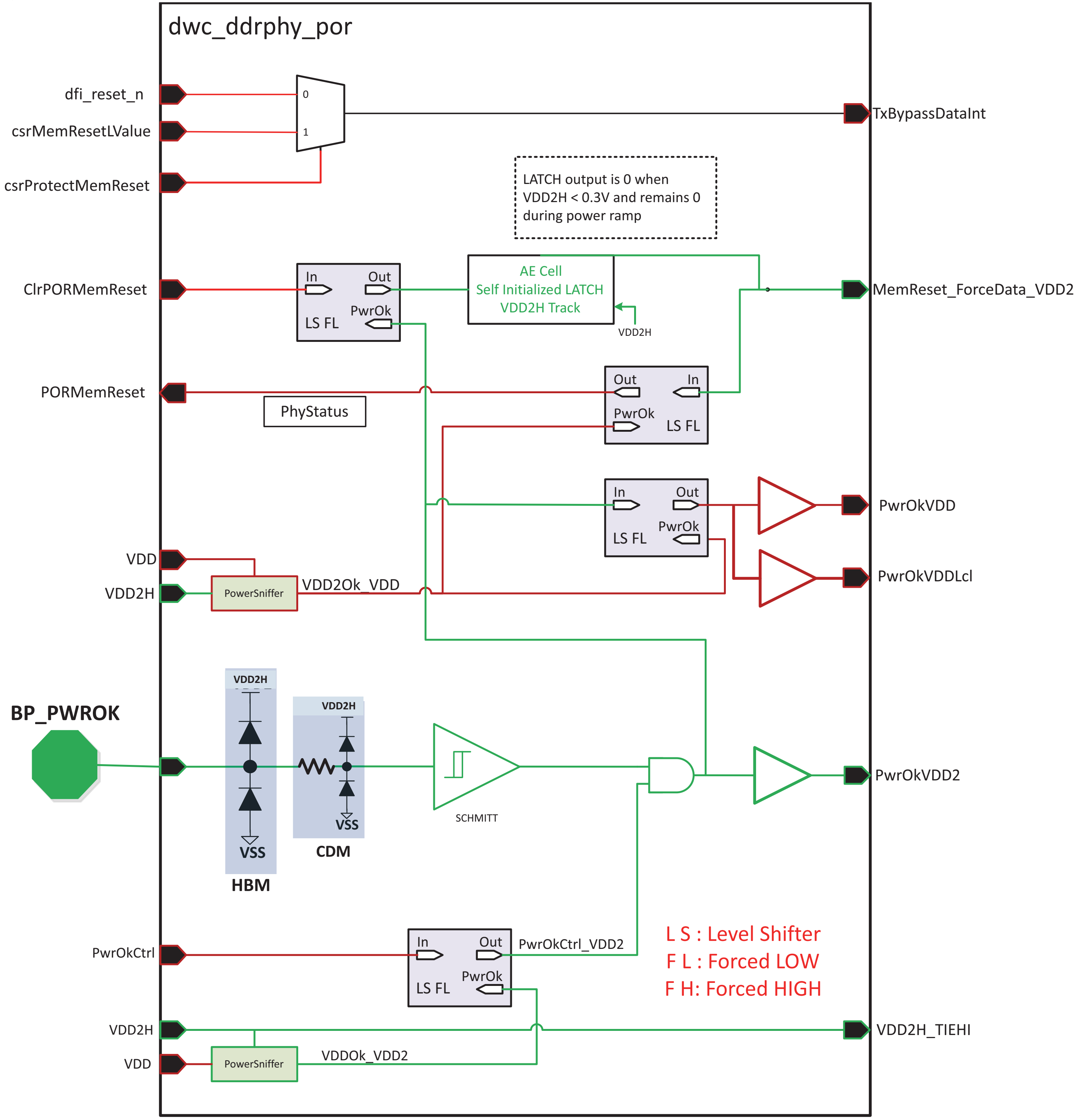
The POR CKT performs following functions:

- Senses voltage ramp on VDD/VDD2 power rails and generates AllPwrOK signal when all rails have reached threshold of power sniffers.
- Level shifters to generate PwrOK_VDD2/PwrOK_VDD for each power domain

- Self-Initialized LATCH to track VDD2 power ramp
  - Generates PwrOn_ForceHigh=0 and PwrOn_ForceLow=1 to force MEMRESET_L 0 during power-up.
- CSR ClrPorMemReset
  - Used to switch the Self-Inialized LATCH state so that PwrOn_ForceHigh changes to 1 and PwrOn_ForceLo changes to 0.
  - Done during "PHY Reset Exit" step of PHY Initialization as described in section 6.4.4.5.
  - When PwrOK_VDD2 changes to 0 after power-up due to retention, MEMRESET_L is forced to 1 state.

The POR CKT logic diagram is shown in the "POR Circuit Diagram" on page 73.

Figure 2-11 POR Circuit Diagram



Note

- The PwrOk_VDDQ is not needed since, in order to support 0.3V VDDQ we cannot distribute it
- Also, still for the 0.3V support, we cannot sniff VDDQ. We need to rely on the SOC/platform to assert the phy pwrok and/or deassert the BP_RET pin when VDDQ is sane
- PwrOkVDD2=~BP_RET&PwrOkCtrl_VDD2
- PwrOkCtrl_VDD2=LS(PwrOkCtrl,VDDOk_VDD2)
- VDDOk_VDD2=sniff(VDD,VDD2H)
- PwrOkVDD=LS(PwrOkVDD2,VDD2Ok_VDD)
- VDD2Ok_VDD = sniff(VDD2H,VDD)
- PORMemReset = LS(MemReset_ForceData, VDD2Ok_VDD)

2.2.2.3 PHY Outputs

SEC IOs have ForceData_VDD2 inputs which forces the PAD into a known state

when PwrOK input is 0 and ForceEnable_VDD2 input is 1.

SE IOs PAD will be in tri-state when PwrOK input is 0.

All IOs will driven by Bypass Driver/Tx drivers when PwrOK input is 1.

Table 2-16 shows the MEMRESET_L output value in different states.

Note:

1. PwrGood (VDD2OK/VDDOk)=1 indicates power sniffers have detected the power up.
2. The dfi_* indicates data from Controller or PUB mode.
3. When atpg_mode=1, TxBypassMode=0 is not supported.
4. The default value of csrProtectMemReset must be changed to 1.

Table 2-16 BP_MEMRESET_L Pad State

State/Mode	Inputs					MEMRESET_L Output
	BP_PWROK	TxBypassMode	atpg_mode	Reset	csrProtectMemReset	
Power ramp	0	X	X	X	X	Forced LOW
Retention	0	X	X	X	X	Forced HIGH
Bypass	1	1	X	X	X	BypassOutData
Mission - DFI	1	0	0	0	0	dfi_reset_n
Mission - CSR	1	0	0	0	1	csrMemResetLValue
Reset	1	0	0	1	1	csrMemResetLValue default

Table 2-17 shows the CKE and all other PHY output values in different states.

Table 2-17 PHY Output Pad States

State/Mode	Inputs					CKE Output	All other Outputs (except CKE/MEMRESET_L)
	PwrGood	BP_PWROK	TxBypassMode	atpg_mode	Reset		
Power ramp	0	X	X	X	X	Forced LOW	Hi-Z
Retention	1	1	X	X	X	Forced LOW	Hi-Z
Bypass	1	0	1	X	X	BypassOutData	BypassOutData
Mission	1	0	0	0	0	dfi_cke	dfi_*
Reset	1	0	0	0	1	Forced LOW	Hi-Z

When Reset is High:

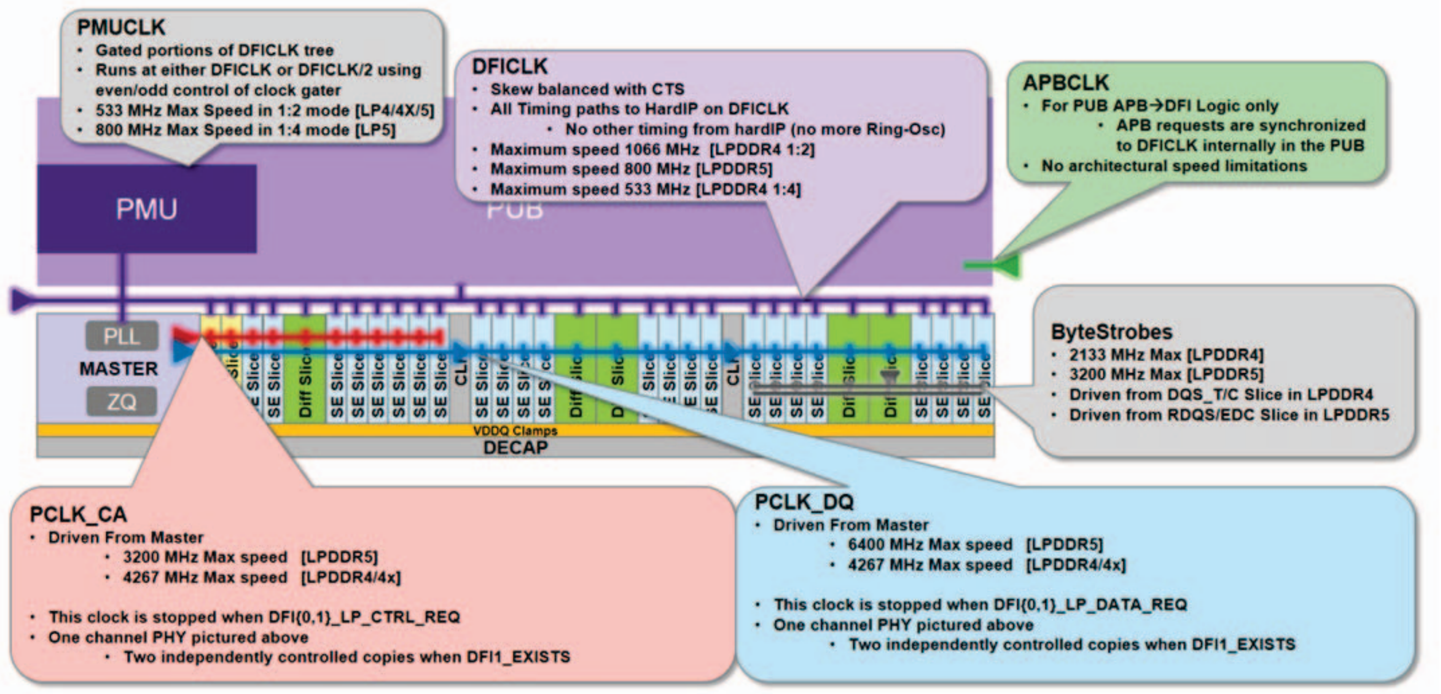
- PUB internally forces TxBypassMode=1 and TxBypassOE=0 internally for all IOs except CKE.
- PUB internally forces TxBypassMode=1 and TxBypassOE=1 and TxBypassData=0 internally for CKE.

2.2.3 Clocking

2.2.3.1 PHY Clocking

Figure 2-12 on page 76 represents the top-level view of clock distribution for LPDDR5/4 PHY and clock signals names:

Figure 2-12 PHY Clock Distribution


PMUCLK
• Gated portions of DFICLK tree
• Runs at either DFICLK or DFICLK/2 using even/odd control of clock gater
• 533 MHz Max Speed in 1:2 mode [LP4/4X/5]
• 800 MHz Max Speed in 1:4 mode [LP5]
DFICLK
• Skew balanced with CTS
• All Timing paths to HardIP on DFICLK
• No other timing from hardIP (no more Ring-Osc)
• Maximum speed 1066 MHz [LPDDR4 1:2]
• Maximum speed 800 MHz [LPDDR5]
• Maximum speed 533 MHz [LPDDR4 1:4]
APBCLK
• For PUB APB→DFI Logic only
• APB requests are synchronized to DFICLK internally in the PUB
• No architectural speed limitations
PMU
PUB
PLL
MASTER
ZQ
SE Slice
Diff Slice
CLK
VDDQ Clamps
DECAP
ByteStrobes
• 2133 MHz Max [LPDDR4]
• 3200 MHz Max [LPDDR5]
• Driven from DQS_T/C Slice in LPDDR4
• Driven from RDQS/EDC Slice in LPDDR5
PCLK_CA
• Driven From Master
• 3200 MHz Max speed [LPDDR5]
• 4267 MHz Max speed [LPDDR4/4x]
• This clock is stopped when DFI{0,1}_LP_CTRL_REQ
• One channel PHY pictured above
• Two independently controlled copies when DFI1_EXISTS
PCLK_DQ
• Driven From Master
• 6400 MHz Max speed [LPDDR5]
• 4267 MHz Max speed [LPDDR4/4x]
• This clock is stopped when DFI{0,1}_LP_DATA_REQ
• One channel PHY pictured above
• Two independently controlled copies when DFI1_EXISTS

2.2.4 Master Clocking

Inside the Master top, DFICLK is multiplied by a PLL to generate an internal master clock signal, master_pclk, that is 4x or 8x the DfiClk frequency.

If atpg_mode is enabled, then the master_pclk signal is sourced from atpg_pclk. If Bypass_mode is asserted, then the master_pclk signal is sourced from PllBypClk.

The master_pclk clock signal is then passed through one clock divider and gater module, dwc_ddrphy_pclk_master, to generate PclkCa{0,1} and PclkDq{0,1}. PclkCa will be routed to the CA SE/SEC/DIFF slices. PclkDq will be routed to the DQ/DQS SE/DIFF slices.

Figure 2-13 Master Hard IP Clocking Overview Diagram

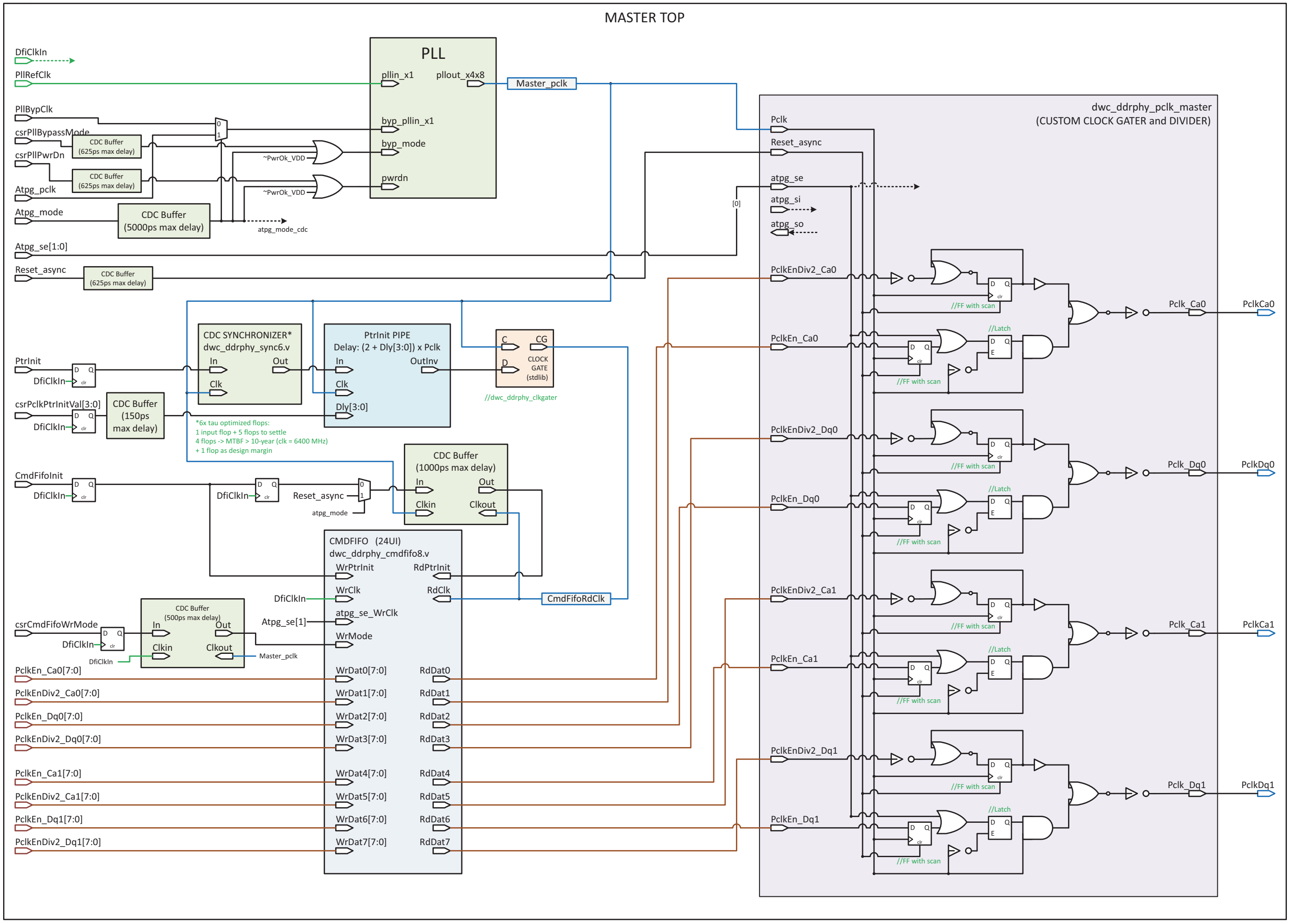


Table 2-18 PclkCa and PclkDq Generation

atpg_mode	Bypass_mode	PLL mult ratio	master_pclk	CA clock divider	DQ clock divider	PclkCa	PclkDq
1	x	x	Atpg_pclk	N_CA[a]	N_DQ[b]	Atpg_pclk/N_CA	Atpg_pclk/N_DQ
0	1	x	PllBypClk			PllBypClk/N_CA	PllBypClk/N_DQ
0	0	N_PLL[c]	PllRefClk x N_PLL			PllRefClk x (N_PLL/N_CA)	PllRefClk x (N_PLL/N_DQ)

[a] N_PLL = {4, 8}
[b] N_DQ = {1,2}
[c] N_CA = {1,2}

One CMDFIFO is used to serialize the dwc_ddrphy_pclk_master controls, from DFICLK domain into Pclk domain. PclkEn_{Ca,Dq} is used.

CMDFIFO RdClk is gated every time PtrInit is asserted. One CDC synchronizer is used to synchronize PtrInit from DFICLK domain to PClk domain. One programmable Pipeline is used to specify the amount of time between the moment

Maximum clock frequencies for DFICLK, PclkCa and PclkDq, per DRAM device is described in the following table.

Table 2-19 Frequency Limits

Max Frequency			
DRAM device	**LPDDR4/4X**	**LPDDR5**	
DFICLK	1066	800	MHz
PclkCa	4267	3200	MHz
PclkDq	4267	6400	MHz

Considering the constraints per PUB version, the target maximum frequencies are the ones listed in the following table.

Table 2-20 System Clocking Configuration

	Device	**LPDDR4/4X**	**LPDDR4/4X**		**LPDDR5**	**LPDDR5**	**Units**
DFI[a]	DFI freq ratio	2	2	4	4	2	1:2 or 1:4
	DfiClk freq	1066	533	533	800	800	MHz
PLL[b]	Pllout ratio	4	8	8	8	8	4x or 8x
	pllin	1066	533	533	800	800	MHz
	pllout	4264	4264	4264	6400	6400	MHz
Clock Divider CK and CA	Clock divisor CA	1	2	1	2	2	1/1 or 1/2 or 1/4
	PclkCa	4264	2133	4264	3200a	3200[c]	MHz
Clock Divider DQ/DQS	Clock divisor DQ	1	2	1	1	2	1/1 or 1/2 or 1/4
	PclkDq	4264	2133	4264	6400	3200	MHz
DRAM interface rates	CK bit rate	4264	2133	4264	1600	1600	Mbps
	CK frequency	2132	1066	2132	800	800	MHz
	CA bit rate	2132	1066	2132	800	800	Mbps
	DQS bit rate	4264	2133	4264	6400	3200	Mbps
	DQS frequency	2132	1066	2132	3200	1600	MHz

[a] This option supports full LPDDR4/4X data rates in DFI 1:2 mode, provided controller can close timing at higher DfiClk frequency.

[b] Supported for date rates < 3200 Mbps. This option support fast-switching between DFI 1:2 and 1:4 without PLL re-lock

c. PUB must send same data every 2 PclkCa to effectively reduce the bit rate in half. This eliminates the need of divde-by 4 logic.

Table 2-21 LP4 vs LP5 CSR Programming

List of CSR	LP4 Mode		LP5 Mode	
	DFI 1:2 Mode	DFI 1:4 Mode	DFI 1:2 Mode	DFI 1:4
DfiFreqRatio	01	01	10	01
CKRatio (WCK:CK)	NA	NA	NA	2:1
PllDivSel, PllV2IMode, PllVcoLowFreq	x4 ratio	X8 ratio	x8 ratio	x8 ratio
CmdFifoWrMode	0	1	1	1
PclkDivCa0	1	2	1	2
PclkDivCa1	1	2	1	2
PclkDivDq0	1	2	1	2
PclkDivDq1	1	2	1	2

2.2.5 Master top component: Phase-Locked Loop (PLL)

One single PLL macro is instantiated inside the Master top module to multiply DFICLK signal and create an internal clock with a frequency that is four or eight times the DFICLK frequency.

The PLL requirements are:

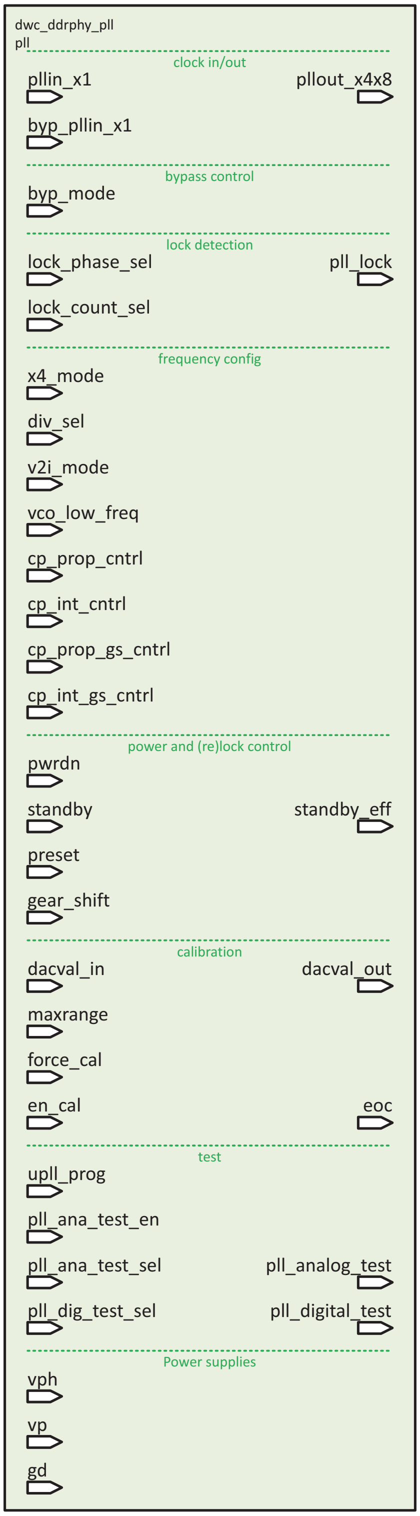
- Custom sub-circuit
- Macro name: dwc_lpddr5phy_pll_<orientation>
- Single instance in the whole PHY, to be located in master_top hardip block
    - Only one orientation required
- Single pllout, selectable to be 4x or 8x the input frequency

Note The master adds output dividers after the PLL to generate PclkCa and PclkDq from the single PLL output.

-
    - Note: master macro will add output dividers after the PLL to generate PclkCa and PclkDq from the single PLL output.
- Mission mode [excluding bypass] input frequency: 83 MHz – 1066 MHz
- Mission mode [excluding bypass] output frequency: 667 MHz – 6400 MHz
    - 4X range: 166 – 1066 MHz input; 667 MHz – 4266 MHz output
    - 8X range: 83 MHz – 800 MHz input; 667 MHz – 6400 MHz output
- Bypass mode input frequency: 50 MHz – 666 MHz
- No background locking feature
- No Syncbus logic in the PLL

    - DfiClk to PllClk* clock domain crossing is done using synchronizers in Master hard IP, outside of PLL
- Keep all features not explicitly mentioned here, analog and digital test points, fast relock, gear_shift, lock indicator, standby, and pwrdn mode
- Reduced lock time

Figure 2-14 PLL symbol and ports overview



2.2.5.1 Optimal PLL Settings

The following tables detail the Mission Mode Frequency Bins.

Table 2-22 Mission Mode Frequency Bins – Normal mode (Ratio x4)

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtr l	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
166	178.8	2	4	4	01 01 10 00 10’b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
178.8	212	2	4	4	01 01 10 00 10’b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
212	260.5	2	4	4	01 01 10 00 10’b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
260.5	312.5	2	4	4	01 01 10 01 10’b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
312.5	357.6	4	2	4	10 10 01 01 10’b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
357.6	424	4	2	4	10 10 01 01 10’b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
424	521	4	2	4	10 10 01 01 10’b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
521	625	4	2	4	10 10 01 10 10’b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
625	715.2	8	1	4	11 11 00 10 10'b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
715.2	848	8	1	4	11 11 00 10 10'b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
848	1042	8	1	4	11 11 00 10 10'b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
1042	1067	8	1	4	11 11 00 11 10'b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
1067	1250	8	1	4	11 11 00 11 10'b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b

Table 2-23 Mission Mode Frequency Bins – Normal mode (Ratio x8)

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtr l	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
83	89.4	1	4	8	00 00 10 00 11'b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
89.4	106	1	4	8	00 00 10 00 11'b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
106	130.25	1	4	8	00 00 10 00 11'b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
130.25	156.25	1	4	8	00 00 10 01 11'b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
156.25	178.8	2	2	8	01 01 01 01 11'b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
178.8	212	2	2	8	01 01 01 01 11'b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
212	260.5	2	2	8	01 01 01 01 11'b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
260.5	312.5	2	2	8	01 01 01 10 11'b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
312.5	357.6	4	1	8	10 10 00 10 11'b	010'b	011'b	0001000’b	0000100’b	0100100’b	1111100’b
357.6	424	4	1	8	10 10 00 10 11'b	010'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
424	521	4	1	8	10 10 00 10 11'b	010'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b
521	625	4	1	8	10 10 00 11 11'b	010'b	000'b	0000110’b	0000100’b	0100100’b	1111100’b
625	675	4	1	8	10 10 00 11 11'b	011'b	010'b	0001000’b	0000100’b	0100100’b	1111100’b
675	822.5	4	1	8	10 10 00 11 11'b	011'b	001'b	0001000’b	0000100’b	0100100’b	1111100’b

Table 2-24 Mission Mode Frequency Bins – Fast relock mode (Ratio x4)

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtr l	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
166	178.8	1	4	4	00 00 10 00 10’b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtr l	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
178.8	212	1	4	4	00 00 10 00 10’b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
212	260.5	1	4	4	00 00 10 00 10’b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b
260.5	312.5	1	4	4	00 00 10 01 10’b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
312.5	357.6	1	2	4	00 00 01 01 10’b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b
357.6	424	1	2	4	00 00 01 01 10’b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
424	521	1	2	4	00 00 01 01 10’b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b
521	625	1	2	4	00 00 01 10 10’b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
625	715.2	1	1	4	00 00 00 10 10'b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b
715.2	848	1	1	4	00 00 00 10 10'b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
848	1042	1	1	4	00 00 00 10 10'b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b
1042	1067	1	1	4	00 00 00 11 10'b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
1067	1250	1	1	4	00 00 00 11 10'b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b

Table 2-25 Mission Mode Frequency Bins – Fast relock mode (Ratio x8)

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtr l	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
83	89.4	1	4	8	00 00 10 00 11'b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b
89.4	106	1	4	8	00 00 10 00 11'b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
106	130.25	1	4	8	00 00 10 00 11'b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b

pllin min (MHz)	pllin max (MHz)	1x/Input divider	1x/VCO divider	1x/Range divider	PllCtrl5_pX<9:0>. PllDivSel	PllCtrl5_pX <12:10>. PllV2IMode	PllCtrl5_pX <15:13>. PllVcoLow Freq	PllCtrl1_pX <14:8>.Pll CpPropCtrl	PllCtrl1_pX <6:0>. PllCpIntCtrl	PllCtrl4_pX <14:8>.Pll CpPropGs Ctrl	PllCtrl4_pX <6:0>. PllCpIntGs Ctrl
130.25	156.25	1	4	8	00 00 10 01 11'b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
156.25	178.8	1	2	8	00 00 01 01 11'b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b
178.8	212	1	2	8	00 00 01 01 11'b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
212	260.5	1	2	8	00 00 01 01 11'b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b
260.5	312.5	1	2	8	00 00 01 10 11'b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
312.5	357.6	1	1	8	00 00 00 10 11'b	010'b	011'b	0011100’b	1111100’b	0011100’b	1111100’b
357.6	424	1	1	8	00 00 00 10 11'b	010'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
424	521	1	1	8	00 00 00 10 11'b	010'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b
521	625	1	1	8	00 00 00 11 11'b	010'b	000'b	0011100’b	1111100’b	0011100’b	1111100’b
625	675	1	1	8	00 00 00 11 11'b	011'b	010'b	0011100’b	1111100’b	0011100’b	1111100’b
675	822.5	1	1	8	00 00 00 11 11'b	011'b	001'b	0011100’b	1111100’b	0011100’b	1111100’b

2.2.6 Master top component: PClk Dividers “dwc_ddrphy_pclk_master”

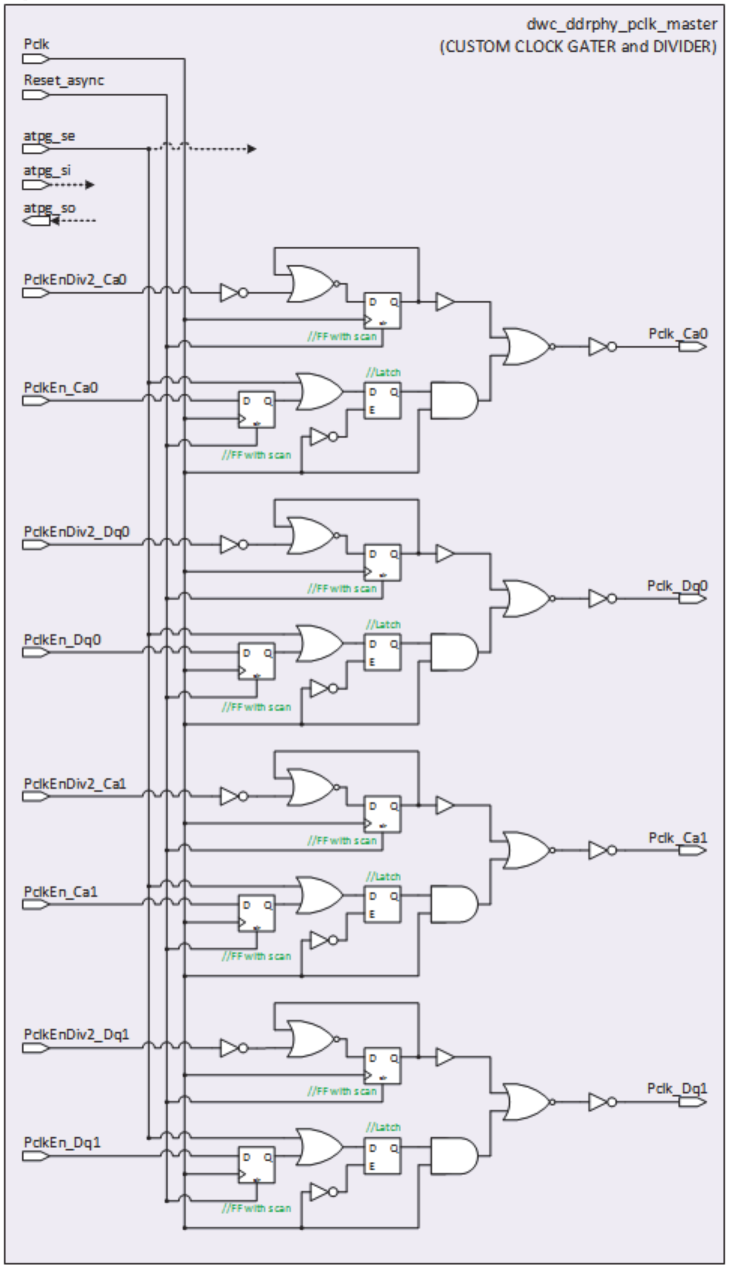
One single custom macro is instantiated inside the Master top module, with 8 clock dividers, each one to generate PclkCa{0,1} and PclkDq{0,1}.

2.2.6.1 Implementation

- Custom subcircuit
- Macro name: dwc_ddrphy_pclk_master
- 8 individual clock dividers
    - Common input clock: Pclk
    - Individual output clocks: PclkCa{0,1} and PclkDq{0,1}

    - Individual divide ratios control: PclkEn{Div2}_Ca{0,1} and PclkEn{Div2}_Dq{0,1}
- Divide ratios: 1:1 and 1:2
    - PclkEn_* = 1 -> enable divide ratio 1:1
        - Freq_Pclk{Ca,Dq}{0,1} = freq_Pclk
    - PclkEnDiv2_* = 1 -> enable divide ratio 1:2
        - Freq_Pclk{Ca,Dq}{0,1} = freq_Pclk / 2
- If PclkEn_* = 0 and PclkEnDiv2_*=0 -> Pclk{Ca,Dq}{0,1} = 1’b0
- Scan logic and flops

Figure 2-15 pclk_master simplified schematic



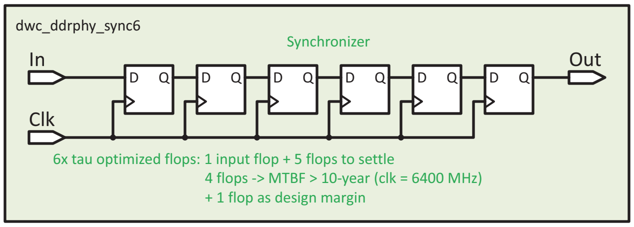
2.2.7 Master top component: PclkPtrInit CDC Synchronizer

One clock domain crossing synchronizer is needed inside master top, to synchronize PclkPtrInit signal from DFICLK domain tp PCLK

2.2.7.1 Implementation

- Macro Name: dwc_ddrphy_sync6
- To synchronize a signal from DFICLK domain to PClk_in domain
  - DFICLK frequency up to 1066 MHz
  - PCLK frequency up to 6400 MHz
- Unsynchronized input: In
- Synchronized input: Out
- Synchronization clock input: Clk
- Uses τ - optimized flip-flops
- 6x flip-flops synchronizer
  - 1 input flop
  - 4 input flops for the signal to settle
    - Designed to have a MTBF higher than 10 years (Clk = 6400 MHz)
  - 1 final flop as a design margin
- Tau optimized flops

Figure 2-16 PclkPtrInit Synchronizer Overview Diagram



6x tau optimized flops: 1 input flop + 5 flops to settle
4 flops -> MTBF > 10-year (clk = 6400 MHz)
+ 1 flop as design margin

2.2.8 Master top component: pclkdiv Cmd FIFO module "dwc_ddrphy_pclkdiv_cmdfifo"

This module encorporates 8 x 8 to 1 serialize FIFOs, with write entries populated with write clock. It is used to transfer control data for pclk Clock Dividers, from the DFICLK clock domain to the PCLK clock domain. It is designed to be used in any arbitrary ratio of DFICLK:PCLK from 1:1 to 1:8.

Table 2-26 PClkDiv CmdFifo (dwc_ddrphy_pcldiv_cmdfifo) Ports

Port Name	Width	Direction	Description
Write Interface			
WrClk	1	input	Write FIFO Clock

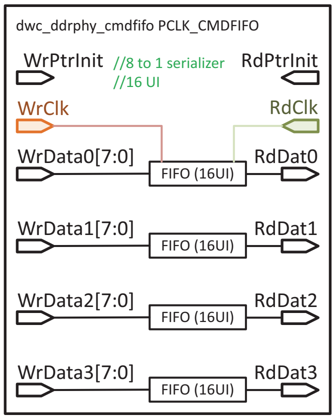
Port Name	Width	Direction	Description
WrDat0	8	input	Write Data
WrDat1	8	input	Write Data
WrDat2	8	input	Write Data
WrDat3	8	input	Write Data
WrDat4	8	input	Write Data
WrDat5	8	input	Write Data
WrDat6	8	input	Write Data
WrDat7	8	input	Write Data
WrPtrInit	1	input	Async Write Pointer Reset
WrMode	3	input	‘b001: This is 1:2 Mode, only lower 2 bit of WrDat are valid ‘b010: This is 1:4 Mode, only lower 4 bit of WrDat are valid ‘b100: This is 1:8 Mode, 8 bit of WrDat are valid
Read Interface			
RdClk	1	input	Read FIFO Clock
RdDat0	1	output	Read Data, serialized 8 bit Write Data.
RdDat1	1	output	Read Data, serialized 8 bit Write Data.
RdDat2	1	output	Read Data, serialized 8 bit Write Data.
RdDat3	1	output	Read Data, serialized 8 bit Write Data.
RdDat4	1	output	Read Data, serialized 8 bit Write Data.
RdDat5	1	output	Read Data, serialized 8 bit Write Data.
RdDat6	1	output	Read Data, serialized 8 bit Write Data.
RdDat7	1	output	Read Data, serialized 8 bit Write Data.
RdPtrInit	1	input	Async Read Pointer Reset

2.2.8.1 Implementation

- FIFO entry needs to be populated for each Write FIFO Clock.
  - For example: Only lower 2 bit of the WrDat needs to be populated in the FIFO entry (2 entries) if WrMode = 3’b001.
- 1 FIFO entry needs to be read at each RdClk
- FIFO Depth: 24 Flops
- Write Pointer: Traditional Binary Counter

- Read Pointer: Traditional Binary Counter.
- Implementation
  - This is Standard FIFO implementation, where 8 entries are populated with WrDat[7:0] at each WrClk and each entry is read at the RdClk to RdDat.

Figure 2-17 PClkDiv CmdFifo Overview Diagram

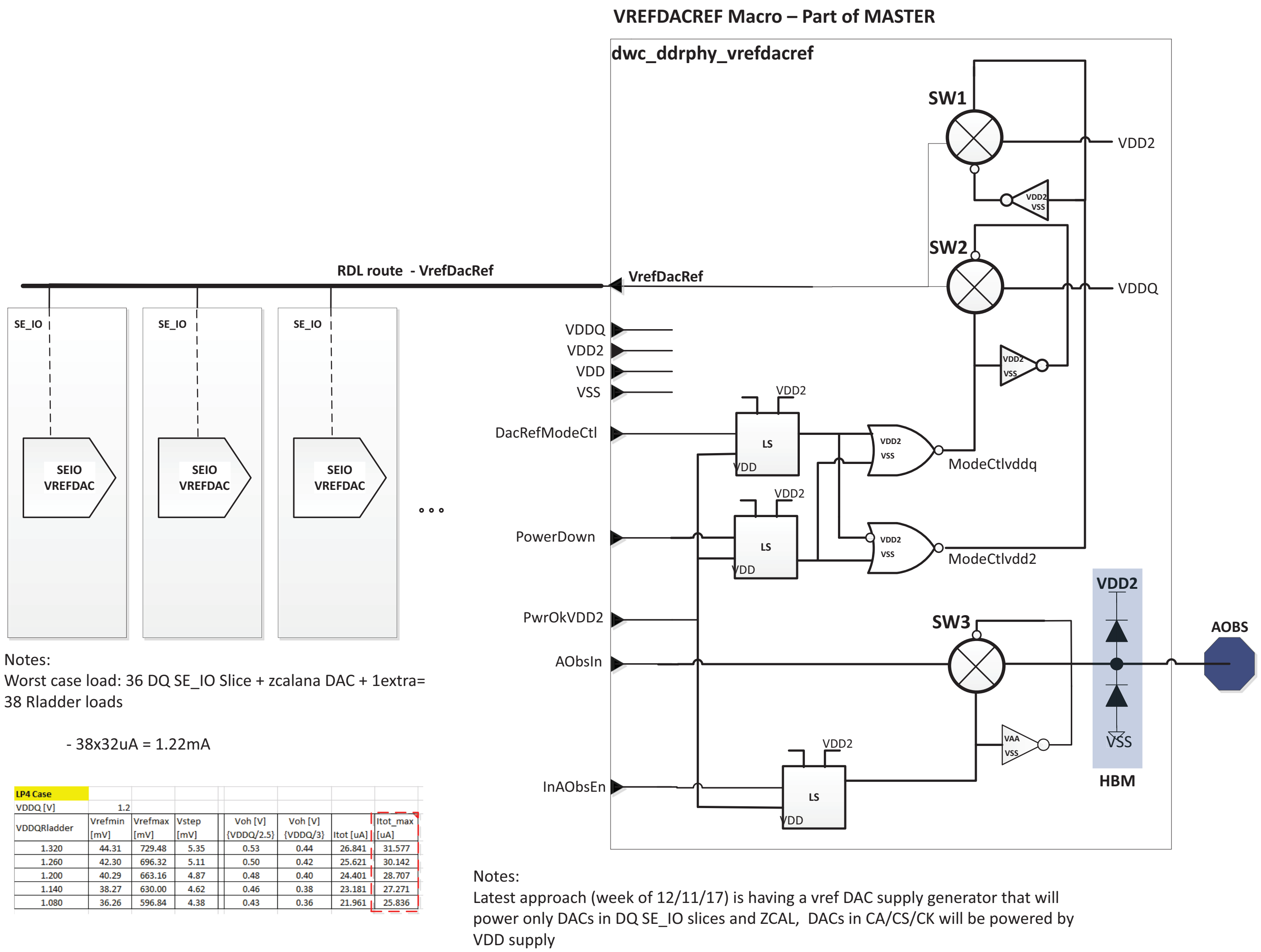


2.2.9 Master top Component: VREFDACREF Module

The dwc_ddrphy_vrefdacref macro is the VrefDacRef supply distribution macro implemented for LPDDR5/4/4x PHY. It supplies the power for all SE_IO and zcalana DAC Rladders. This macro is part of the MASTER and the VrefDacRef supply gets distributed to all SE_IOs in DQ slices across the PHY in RDL. `

The dwc_ddrphy_vrefdacref macro block diagram is shown in Figure dwc_ddrphy_vrefdacref macro Block Diagram.

Figure 2-18 dwc_ddrphy_vrefdacref macro Block Diagram



Notes:
Worst case load: 36 DQ SE_IO Slice + zcalana DAC + 1extra=
38 Rladder loads

- 38x32uA = 1.22mA

LP4 Case							
VDDQ [V]	1.2						
VDDQRladder	Vrefmin [mV]	Vrefmax [mV]	Vstep [mV]	Voh [V] {VDDQ/2.5}	Voh [V] {VDDQ/3}	Itot [uA]	Itot_max [uA]
1.320	44.31	729.48	5.35	0.53	0.44	26.841	31.577
1.260	42.30	696.32	5.11	0.50	0.42	25.621	30.142
1.200	40.29	663.16	4.87	0.48	0.40	24.401	28.707
1.140	38.27	630.00	4.62	0.46	0.38	23.181	27.271
1.080	36.26	596.84	4.38	0.43	0.36	21.961	25.836

Notes:
Latest approach (week of 12/11/17) is having a vref DAC supply generator that will power only DACs in DQ SE_IO slices and ZCAL, DACs in CA/CS/CK will be powered by VDD supply

The following tables show the functional behavior of the Macro.

The AObsIn is the analog observability input from PLL and AOBS should be connected to BP_ATO.

Table 2-27 Functional Behavior

PwrOkVDD2	PowerDown	DacRefModeCtl	VrefDacRef	InAObsEn	AOBS
1	0	0	VDDQ	-	-
1	0	1	VDD2	1	AObsIn
1	1	X	Z	0	Z
0	X	X	Z	X	Z

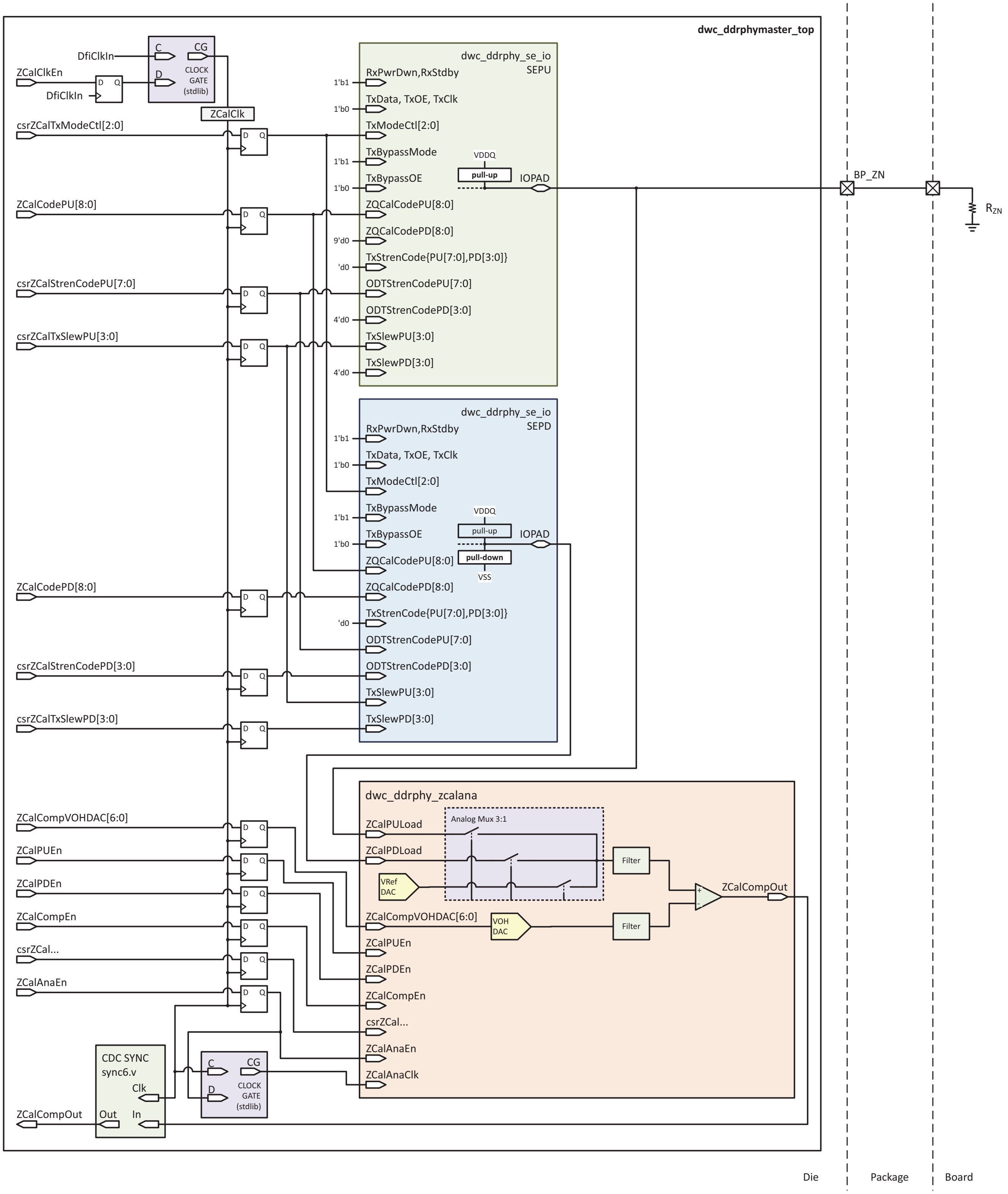
2.2.10 Master Impedance Calibration

The Master includes the analog blocks used for impedance calibration.

2.2.10.1 Implementation

- 1x dwc_ddrphy_se instance, named sepu
  - Instantiated inside master top
  - For pull-up calibration
  - VIO_PAD connects to BP_ZN IO pad and to ZCalPULoad (dwc_ddrphy_zcalana's input pin)
  - The RX path is not used and must not be enabled.
  - Drive Strength codes and mission mode data path are not used and must be disabled
    - TxEn = 0
  - ODTStrengthPU[6:0] is used to set the pull-up impedance value during pull-up calibration
  - ODTStrengthPD[6:0] must be set to have pull-down be Hi-Z.
- 1x dwc_ddrphy_se instance, named sepd
  - Instantiated inside master top
  - For pull-down calibration
  - VIO_PAD connects to ZCalPDLoad (dwc_ddrphy_zcalana's input pin)
  - The RX path is not used and must not be enabled.
  - Drive Strength codes and mission mode data path are not used and must be disabled
    - TxEn = 0
  - ODTStrengthPU[6:0] must get the pull-up code from pull-up calibration.
  - ODTStrengthPD[6:0] is used to set the pull-down impedance value during pull-down calibration.
- 1x dwc_ddrphy_zcalana instance, named dwc_ddrphy_zcalana
  - Instantiated inside master top
  - With the comparator circuit and calibration DACs, needed to support pull-up and pull-down calibration
  - External "sync6" synchronizer for zcalana comparator output
  - External clock gater to gate the ZCalAnaClk clock when ZcalAnaEn is deasserted.
- BP_ZN bump, to connect to an external reference resistor, for impedance calibration
  - Master must support 120 Ohms +- 1% tolerance, external resistor.
- Input flops
  - for ZCal control inputs
  - clocked by ZCalClk, a gated version of DfiClk

Figure 2-19 Impedance Calibration blocks in Master Hard IP



From lpddr4v2, hardip changes includes modules/instances and port changes proposed in the following tables.

Table 2-28 Impedance Calibration Sub-Module Names

lpddr4v2 ckt names	lpddr54 ckt names	Observations
cmpmeas	*zcalmeas*	
cmpana	*zcalana*	Custom analog circuits for ZCAL

Table 2-29 Impedance Calibration Sub-Module Instance Names

module where the instance is called (lpddr54)	lpddr4v2 instance name	lpddr54 instance name
dwc_ddrphymaster_top	dwc_ddrphy_cmpmeas	dwc_ddrphy_zcalmeas
dwc_ddrphy_zcalmeas	txzqext	SEPU
dwc_ddrphy_zcalmeas	txzqint	SEPD
dwc_ddrphy_zcalmeas	dwc_ddrphy_cmpana	dwc_ddrphy_zcalana

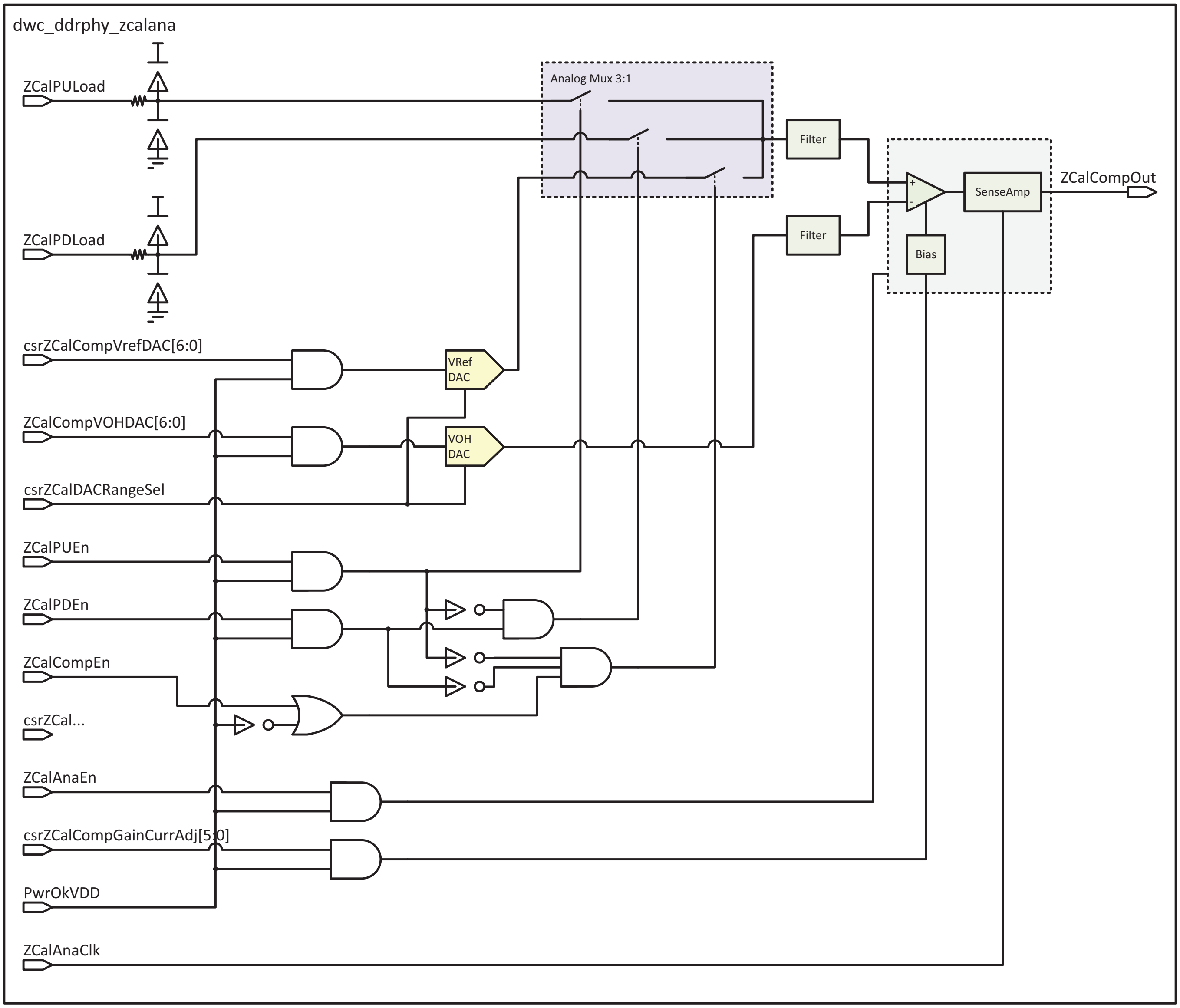
2.2.11 Analog Impedance Calibration Block

The analog impedance calibration block macro has the analog circuits required to support pull-up and pull-down calibration. How this macro is used for impedance calibration is described in Analog Impedance Calibration Block

This macro requirements are:

- One zero-current sense input, to be connected to BP_ZN bump: ZCalPULoad
- One zero-current sense input, to be connected to sepd instance IOPAD pin: ZCalPDLoad
- One DAC to be used as voltage reference (VRef DAC), when calibrating the comparator to cancel it's offset voltage. Input to control the DAC: csrZCalCompVrefDAC[6:0]
- One DAC to set the pull-up and pull-down calibration threshold voltage point in the comparator (VOH DAC). This DAC voltage value is calibrated against the voltage set by the VRef DAC. Input to control the DAC: ZCalCompVOHDAC[6:0]
- One Analog 3:1 Mux, to select which one of ZCalPULoad, ZCalPDLoad or VRef DAC nodes is connected to the comparator's input. The Mux select input pins are: ZCalCompEn, ZCalPUEn and ZCalPDEn. Only one of them must be asserted at a time.
- One Comparator, with one input connected to the Mux output (let's call it comparator input) and the other input connected to the VOH DAC output. The comparator's offset voltages are canceled by a calibration process that adjusts the VOH DAC code so that the comparator's output toggles when the voltage at the comparator's input swings around a VOH voltage.
    - The comparator output is sampled with a clock in the DfiClk domain.
- Analog filtering plus shielding at the comparator's inputs, to reduce noise effects in the comparator's operation.
- ESD and overvoltage protection clamps should be placed at ZCalPULoad
- Overvoltage protection clamps should be placed at ZCalPDLoad

Figure 2-20 dwc_ddrphy_zcalana overview block diagram



From lpddr4v2, hardip changes includes port changes proposed in Table 2-30.

Port updates to dwc_ddrphy_zcalana (previous dwc_ddrphy_cmpdig):

Table 2-30 ZCalAna (dwc_ddrphy_zcalana) Ports

	lpddr4v2		lpddr54		Observations
Directio n	widt h	Name	widt h	Name	
input		PwrOk		PwrOkVDD	To follow updates suggest in SE/SEC/DIFF slices

	lpddr4v2		lpddr54		Observations
Direction	width	Name	width	Name	
input		PwrOk_VIO		PwrOkVDDQ	To follow updates suggest in SE/SEC/DIFF slices
input		Cmpdig_CmpanaClk		ZCalAnaClk	Sampler clock (DfiClk domain). Is a gated DfiClk signal.
input		Cmpdig_CmpanaEn		ZCalAnaEn	Enables the analog circuitry for impedance calibration, including the VOH and Vref DACs.
input		Csr_CmprBiasPowerUp		csrZCalCompBiasPowerUp	Failsafe pin to pulse and stimulate bias feedback loop to kick it out of any weird state. Not used anymore as of SyncC
input		Csr_CmprBiasBypassEn		csrZCalCompBiasBypassEn	Bypass the bias generated from bias feedback ckt and instead switch to a simpler backup bias ckt
input	[7:0]	Csr_CmprGainCurrAdj	[7:0]	csrZCalCompGainCurrAdj	Trim bits for bias currents
input		Csr_CmprGainResAdj		csrZCalCompGainResAdj	Trim bit for load resistor in front-end amplifier
input		ExternalLoad		ZCalPULoad	Analog input node to be probed during pull-up calibration, by the comparator
input		InternalLoad		ZCalPDLoad	Analog input node to be probed during pull-down calibration, by the comparator
input		Cmpdig_CalCmpr		ZCalCompEn	1’b1 – Enable comparator's offset calibration. The active calibration node, connected to the Comparator's input, is the internal VRef DAC output.
input		Cmpdig_CalExt		ZCalPUEn	1’b1 – Enables pull-up impedance calibration. The active calibration node, connected to the Comparator's input, is ZCalPULoad input
input		Cmpdig_CalInt		ZCalPDEn	1’b1 – Enables pull-down impedance calibration. The active calibration node, connected to the Comparator's input, is ZCalPDLoad input
input	[1:0]	Cmpdig_CalRef	[6:0]	csrZCalCompVrefDAC	Digital input code for the Vref DAC , whose output is to be used as the voltage reference for comparator’s offset calibration

	lpddr4v2		lpddr54		Observations
Direction	width	Name	width	Name	
input	[7:0]	Cmpdig_CalDac	[6:0]	ZCalCompVOHDAC	Digital input code for the VOH DAC, whose output is to be used as the VOH reference voltage when doing pull-up and pull-down calibrations.
output		Cmpana_Out		ZCalCompOut	Comparator's digital output
input		VDDQ		VDDQ	
input		VDD		VDD	
input		VSS		VSS	

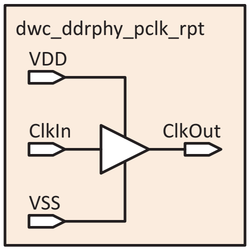
2.3 Clock Repeaters

Clock repeater macros are used to distribute high-speed clocks (PclkCa, PclkDq) across large distances. Each repeater should be a simple large buffer that the customer can instantiate to redrive PclkCa and PclkDq clocks. The customer will insert these in the back end when required, so there's no need to instantiate them in the PHY Top.

The Clock Repeater requirements are:

- Macro name: dwc_ddrphy_pclk_rpt
- Simple Large Buffer.
  - Port list: ClkIn, ClkOut, VDD, VSS
- Capable to drive a 6400 MHz signal 1 mm distance.
- To be instantiated by the customers as needed, between the slice macros.
- These are *not* instantiated in the Verilog we provide.

Figure 2-21 Clock Repeater Hard IP



2.4 Physical-Only Blocks

Physical-only blocks are macros that have only a physical impact and no logical function. These are delivered as GDS without Verilog views.

2.4.1 VDDQ Decap

VDDQ Decap macros provide decoupling capacitance for the VDDQ power rail. These are typically instantiated around the periphery of the die, outside of the slice macros; this physical arrangement is a common use case, not a requirement.

2.4.2 VDDQ Clamps

VDDQ Clamp macros provide ESD protection for the VDDQ power rail. These are typically instantiated around the periphery of the die, outside of the slice macros; this physical arrangement is a common use case, not a requirement.

3

Signal Overview

This chapter details all possible I/O signals in the PHY. Inputs are on the left of the signal diagrams; outputs are on the right.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- Active State: Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the in-active state (opposite of the active state).
- Registered: Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of No does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- Synchronous to: Indicates which clock(s) in the IP sample this input (drive for an output) when considering all possible configurations. A particular configuration might not have all of the clocks listed. This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- Exists: Name of configuration parameter(s) that populates this signal in your configuration.
- Validated by: Assertion or de-assertion of signal(s) that validates the signal being described.

The I/O signals are grouped as follows:

- "DDRPHYMASTER Signal Descriptions" on page 101
- "DDRPHYDIFF Signal Descriptions" on page 137
- "DDRPHYSE Signal Descriptions" on page 163
- "DDRPHYSEC Signal Descriptions" on page 185

4

DDRPHYMASTER Signal Descriptions

This chapter details all possible I/O signals in the IP. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the controller. It is for reference purposes only.

When you configure the controller in coreConsultant, you must access the I/O signals for your actual configuration at workspace/report/IO.html or workspace/report/IO.xml after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the I/O signals that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the widths might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- **Active State:**Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the inactive state (opposite of the active state).
- **Registered:**Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of *No*does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:**Indicates which clocks in the IP sample this input (drive for an output). This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- **Exists:**Name of configuration parameter that populates this signal in your configuration.

The I/O signals are grouped as follows:

- "Interface to Global Signals" on page 103
- "Interface to PLL Bypass Signals" on page 104
- "Interface to ATPG Mode Signals" on page 105
- "Test Signals" on page 106
- "Interface to DTO Configuration Signals" on page 107
- "Interface to DTO Signals" on page 108
- "Slice Control Signals" on page 109
- "Version ID Signals" on page 110
- "Interface to PLL Control Signals" on page 111
- "Interface to PLL Configuration Signals" on page 112
- "Interface to PLL status Signals" on page 114
- "Interface to CMDFIFO control Signals" on page 115
- "Interface to CMDFIFO Configuration Signals" on page 116
- "Interface to PCLK control Signals" on page 117
- "Interface to PCLK Signals" on page 118
- "Interface to MEMRESET DFI Signals" on page 119
- "Interface to MEMRESET Configuration Signals" on page 120
- "Asynchronous IO Test Signals" on page 121
- "Interface to ZCAL control Signals" on page 123
- "Interface to ZCAL Configuration Signals" on page 125
- "Interface to ZCAL Signals" on page 127
- "Interface to VrefDacRef macro Configuration Signals" on page 128
- "Interface to VrefDacRef macro Control Signals" on page 129
- "VrefDacRef supply Signals" on page 130
- "Interface to POR Control Signals" on page 131
- "Power and Ground Supplies Signals" on page 132
- "Interface to POR CKT Signals" on page 133
- "Interface to SDRAM Signals from IO Cells" on page 134
- "Interface to TEST bumps Signals" on page 135
- "Interface to ZCAL bumps Signals" on page 136

4.1 Interface to Global Signals

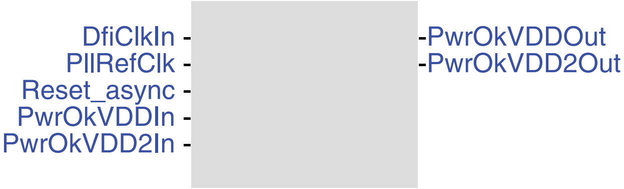


Table 4-1 Interface to Global Signals

Port Name	I/O	Description
DfiClkIn	I	DFI Input Clock **Exists:**Always **Synchronous To:**DfiClk
PllRefClk	I	Input Clock to be used as PLL reference clock **Exists:**Always **Synchronous To:**DfiClk
Reset_async	I	Async Reset from phy top **Exists:**Always **Synchronous To:**Async
PwrOkVDDOut	O	Indicator from POR ckt that all power rails are up. Transmitted asynchronously in the VDD power domain. **Exists:**Always **Synchronous To:**Async
PwrOkVDDIn	I	Input indicator from Master Hard IP that all power rails are up. Transmitted asynchronously in the VDD power domain. **Exists:**Always **Synchronous To:**Async
PwrOkVDD2Out	O	Indicator from POR ckt inside Master Hard IP, that all power rails are up. Transmitted asynchronously in the VDD2H power domain. **Exists:**Always **Synchronous To:**Async
PwrOkVDD2In	I	Input indicator from Master Hard IP that all power rails are up. In VDD2H power domain. Connects directly to PwrOk_VDD2Out in Master Top instance. **Exists:**Always **Synchronous To:**Async

4.2 Interface to PLL Bypass Signals

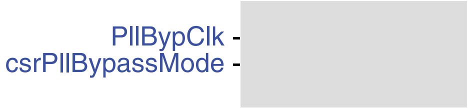


Table 4-2 Interface to PLL Bypass Signals

Port Name	I/O	Description
PllBypClk	I	Bypass clock for Pclk **Exists:**Always **Synchronous To:**Async
csrPllBypassMode	I	Bypass mode for Pclk. Refer to CSR description **Exists:**Always **Synchronous To:**Async

4.3 Interface to ATPG Mode Signals

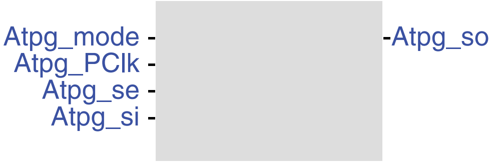


Table 4-3 Interface to ATPG Mode Signals

Port Name	I/O	Description
Atpg_mode	I	ATPG Mode Select. When asserted, scan mode is enabled. **Exists:**Always **Synchronous To:**DfiClk
Atpg_PClk	I	Scan clock for Pclk Logic. Must be 0 during mission mode. **Exists:**Always **Synchronous To:**atpg_pclk
Atpg_se[1:0]	I	ATPG Scan Enable **Exists:**Always **Synchronous To:**DfiClk/Atpg_pclk
Atpg_si[4:0]	I	ATPG Scan Chain Input **Exists:**Always **Synchronous To:**DfiClk/Atpg_pclk
Atpg_so[4:0]	O	ATPG Scan Chain Output **Exists:**Always **Synchronous To:**DfiClk/Atpg_pclk

4.4 Test Signals

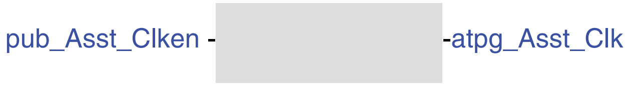


Table 4-4 Test Signals

Port Name	I/O	Description
pub_Asst_Clken	I	ASST clock enable **Exists:**Always **Synchronous To:**atpg_Asst_Clk
atpg_Asst_Clk	O	ASST Clock **Exists:**Always **Synchronous To:**atpg_Asst_Clk

4.5 Interface to DTO Configuration Signals

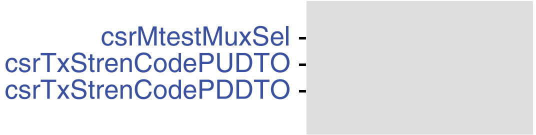


Table 4-5 Interface to DTO Configuration Signals

Port Name	I/O	Description
csrMtestMuxSel[5:0]	I	Digital test output select control. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrTxStrenCodePUDTO[1:0]	I	Pull-up DTO drive strength code. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrTxStrenCodePDDTO[1:0]	I	Pull-down DTO drive strength code. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk

4.6 Interface to DTO Signals

Table 4-6 Interface to DTO Signals

Port Name	I/O	Description
MtestMuxOut	O	Digital test output, for debug **Exists:**Always **Synchronous To:**DfiClk

4.7 Slice Control Signals

csrReserved -

Table 4-7 Slice Control Signals

Port Name	I/O	Description
csrReserved[2:0]	I	Reserved for future use **Exists:**Always **Synchronous To:**DfiClkIn

4.8 Version ID Signals

Table 4-8 Version ID Signals

Port Name	I/O	Description
csrPHYREV[15:0]	O	Hardware version of this PHY. Refer to CSR description **Exists:**Always **Synchronous To:**Async

4.9 Interface to PLL Control Signals

Table 4-9 Interface to PLL Control Signals

Port Name	I/O	Description
csrPllPwrDn	I	PLL Power Down. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllPreset	I	PLL Preset Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllStandby	I	PLL Standby Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllGearShift	I	PLL Control GearShift Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllEnCal	I	PLL EnCal Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk

4.10 Interface to PLL Configuration Signals

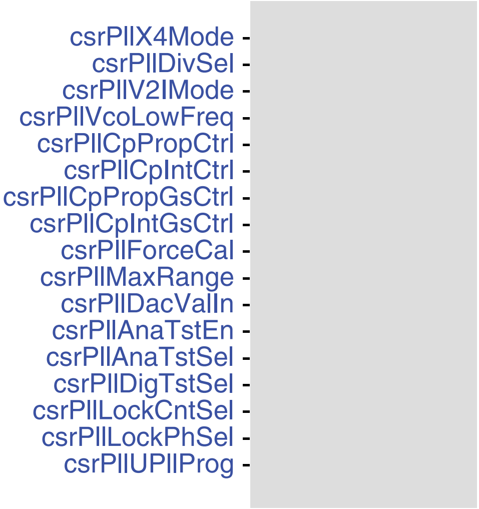


Table 4-10 Interface to PLL Configuration Signals

Port Name	I/O	Description
csrPllX4Mode	I	PLL X4Mode Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllDivSel[9:0]	I	PLL DivSel Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllV2IMode[2:0]	I	PLL V2IMode Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllVcoLowFreq[2:0]	I	PLL VcoLowFreq Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllCpPropCtrl[6:0]	I	PLL CpProp Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllCpIntCtrl[6:0]	I	PLL CpInt Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllCpPropGsCtrl[6:0]	I	PLL CpPropGs Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk

Port Name	I/O	Description
csrPllCpIntGsCtrl[6:0]	I	PLL CpIntGs Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllForceCal	I	PLL ForceCal Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllMaxRange[4:0]	I	PLL MaxRange Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllDacValIn[4:0]	I	PLL DacValIn Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllAnaTstEn	I	PLL AnaTstEn Testing Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllAnaTstSel[5:0]	I	PLL AnaTstSelTesting Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllDigTstSel[5:0]	I	PLL DigTstSel Testing Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllLockCntSel	I	PLL LockCntSel Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllLockPhSel[1:0]	I	PLL LockPhSel Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrPllUPllProg[63:0]	I	PLL UPllProg Control Register. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk

4.11 Interface to PLL status Signals

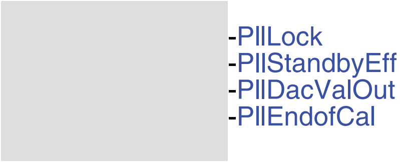


Table 4-11 Interface to PLL status Signals

Port Name	I/O	Description
PllLock	O	PLL lock indicator **Exists:**Always **Synchronous To:**Async
PllStandbyEff	O	PLL Standby state indicator **Exists:**Always **Synchronous To:**Async
PllDacValOut[4:0]	O	PLL Calibration DAC current setting output value **Exists:**Always **Synchronous To:**Async
PllEndofCal	O	PLL End of calibration flag **Exists:**Always **Synchronous To:**Async

4.12 Interface to CMDFIFO control Signals

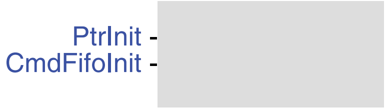


Table 4-12 Interface to CMDFIFO control Signals

Port Name	I/O	Description
PtrInit	I	Enables CMDFIFO RdClk **Exists:**Always **Synchronous To:**DfiClk
CmdFifoInit	I	Initializes the CMDFIFO pointer **Exists:**Always **Synchronous To:**DfiClk

4.13 Interface to CMDFIFO Configuration Signals

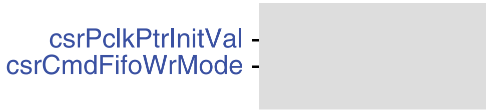


Table 4-13 Interface to CMDFIFO Configuration Signals

Port Name	I/O	Description
csrPclkPtrInitVal[3:0]	I	Controls the phase offset between read and write pointers of CMDFIFO **Exists:**Always **Synchronous To:**DfiClk
csrCmdFifoWrMode	I	Selects the valid width for CmdFIFO write inputs. (inputs are always 8 bit wide). Valid values are: 1'b0: Only lower 4 bits will be written in Fifo on each DfiClk. 1'b1: All 8 bits will be written on each DfiClk. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk

4.14 Interface to PCLK control Signals

Table 4-14 Interface to PCLK control Signals

Port Name	I/O	Description
PclkEn_Ca0[7:0]	I	Enable of PClkCa0 with by-1 clock divider (no division) **Exists:**Always **Synchronous To:**DfiClk
PclkEnDiv2_Ca0[7:0]	I	Enable of PClkCa0 with by-2 clock divider **Exists:**Always **Synchronous To:**DfiClk
PclkEn_Ca1[7:0]	I	Enable of PClkCa1 with by-1 clock divider (no division) **Exists:**Always **Synchronous To:**DfiClk
PclkEnDiv2_Ca1[7:0]	I	Enable of PClkCa1 with by-2 clock divider **Exists:**Always **Synchronous To:**DfiClk
PclkEn_Dq0[7:0]	I	Enable of PClkDq0 with by-1 clock divider (no division) **Exists:**Always **Synchronous To:**DfiClk
PclkEnDiv2_Dq0[7:0]	I	Enable of PClkDq0 with by-2 clock divider **Exists:**Always **Synchronous To:**DfiClk
PclkEn_Dq1[7:0]	I	Enable of PClkDq1 with by-1 clock divider (no division) **Exists:**Always **Synchronous To:**DfiClk
PclkEnDiv2_Dq1[7:0]	I	Enable of PClkDq1 with by-2 clock divider **Exists:**Always **Synchronous To:**DfiClk

4.15 Interface to PCLK Signals

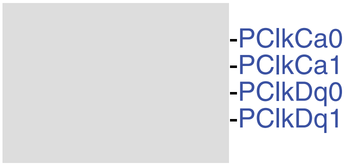


Table 4-15 Interface to PCLK Signals

Port Name	I/O	Description
PClkCa0	O	Pclk for all slices used in DRAM channel 0 command interface **Exists:**Always **Synchronous To:**Pclk_Ca0
PClkCa1	O	Pclk for all slices used in DRAM channel 1 command interface **Exists:**Always **Synchronous To:**Pclk_Ca1
PClkDq0	O	Pclk for all slices used in DRAM channel 0 data interface **Exists:**Always **Synchronous To:**Pclk_Dq0
PClkDq1	O	Pclk for all slices used in DRAM channel 1 data interface **Exists:**Always **Synchronous To:**Pclk_Dq1

4.16 Interface to MEMRESET DFI Signals

Table 4-16 Interface to MEMRESET DFI Signals

Port Name	I/O	Description
dfi_reset_n	I	Dfi Reset input directly from controller **Exists:**Always **Synchronous To:**DfiClk

4.17 Interface to MEMRESET Configuration Signals

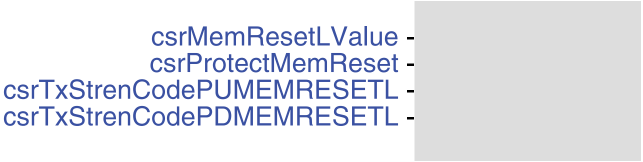


Table 4-17 Interface to MEMRESET Configuration Signals

Port Name	I/O	Description
csrMemResetLValue	I	BP_MEMRESET_L pad value when csrProtectMemReset=1. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrProtectMemReset	I	When asserted, BP_MEMRESET_L pad gets the value from csrMemResetLValue input. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrTxStrenCodePUMEMRESETL[1:0]	I	Pull-up MEMRESET drive strength code. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk
csrTxStrenCodePDMEMRESETL[1:0]	I	Pull-down MEMRESET drive strength code. Refer to CSR description **Exists:**Always **Synchronous To:**DfiClk

4.18 Asynchronous IO Test Signals

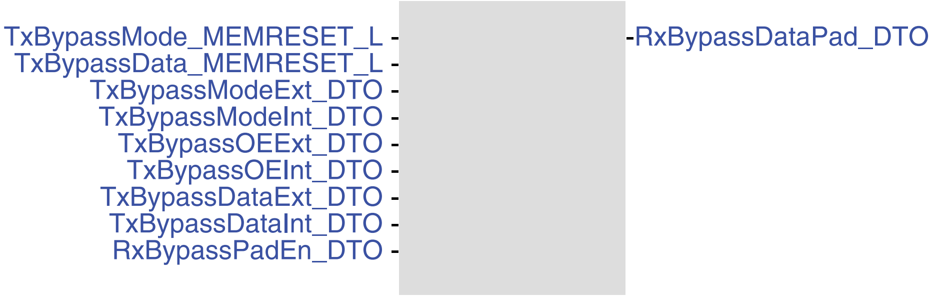


Table 4-18 Asynchronous IO Test Signals

Port Name	I/O	Description
TxBypassMode_MEMRESET_L	I	When asserted, enables the setting of data of the BP_MEMRESET_L pad asynchronously using TxBypassData_MEMRESET_L PHY input. **Exists:**Always **Synchronous To:**Async
TxBypassData_MEMRESET_L	I	Asynchronous data to be sent on MemResetL pad, when TxBypassMode_MEMRESET_L is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassModeExt_DTO	I	Connected to phytop TxBypassData_DTO. When asserted, enables the setting of data and OE of the DTO pad asynchronously using TxBypassData_DTO and TxBypassOE_DTO phytop inputs. **Exists:**Always **Synchronous To:**Async
TxBypassModeInt_DTO	I	Connected through an inverter to phytop TxBypassData_DTO. When asserted PUB will have control of the DTO IO circuit bypass path during MTest debug.This signal is asserted when TxBypassModeExt_DTO is deasserted. **Exists:**Always **Synchronous To:**Async
TxBypassOEExt_DTO	I	Connected to phytop TxBypassOE_DTO. Asynchronous setting of output enable (OE) of DTO pad when phytop TxBypassMode_DTO is asserted. PUB will control during function mode for MTest debug. **Exists:**Always **Synchronous To:**Async
TxBypassOEInt_DTO	I	Connected through an inverter to phytop TxBypassMode_DTO. Assert output enable (OE) of DTO pad when phytop TxBypassMode_DTO is deasserted. **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
TxBypassDataExt_DTO	I	Connected to phytop TxBypassData_DTO. Asynchronous data to be sent on DTO pad when phytop TxBypassMode_DTO is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassDataInt_DTO	I	Connected to PUB MtestCombo. MTest data to be sent on the DTO pad when phytop TxBypassMode_DTO is deasserted. **Exists:**Always **Synchronous To:**Async
RxBypassPadEn_DTO	I	When asserted, enables CMOS input path from IO. **Exists:**Always **Synchronous To:**Async
RxBypassDataPad_DTO	O	Bypass (RX-DAT (cmos)). When RxBypassPadEn is asserted: asynchronously sampled receive data is returned on this output. When RxBypassPadEn is de-asserted: this output is forced 0. **Exists:**Always **Synchronous To:**Async

4.19 Interface to ZCAL control Signals

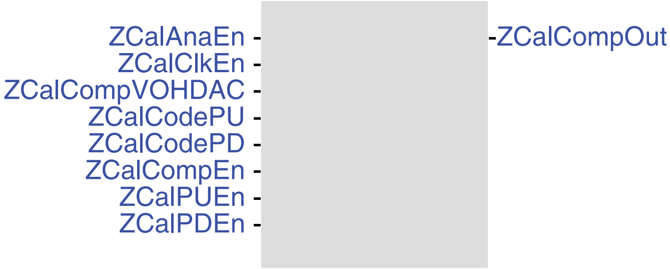


Table 4-19 Interface to ZCAL control Signals

Port Name	I/O	Description
ZCalAnaEn	I	When asserted, enables the impedance calibration analog circuit. **Exists:**Always **Synchronous To:**DfiClk
ZCalClkEn	I	When asserted, enables the clock (DfiClk) for impedance calibration logic inside Master top. **Exists:**Always **Synchronous To:**DfiClk
ZCalCompVOHDAC[6:0]	I	Digital input code for the VOH DAC, whose output is to be used as the VOH reference voltage when doing pull-up and pull-down calibrations. **Exists:**Always **Synchronous To:**DfiClk
ZCalCodePU[8:0]	I	Controls pull-up calibration net in the impedance calibration replica drivers. Bits 7-0: Calibration code. Bit 9: Calibration base leg enable **Exists:**Always **Synchronous To:**DfiClk
ZCalCodePD[8:0]	I	Controls pull-down calibration net in the impedance calibration replica drivers. Bits 7-0: Calibration code. Bit 9: Calibration base leg enable **Exists:**Always **Synchronous To:**DfiClk
ZCalCompEn	I	When asserted, comparator offset calibration is enabled. Connects the dwc_ddrphy_zcalana VREF DAC analog output to the calibration comparator input **Exists:**Always **Synchronous To:**DfiClk
ZCalPUEn	I	When asserted, pull-up calibration is enabled. Connects both the SEPU VIO_PAD and phytop BP_ZN pad to the calibration comparator input **Exists:**Always **Synchronous To:**DfiClk

Port Name	I/O	Description
ZCalPDEn	I	When asserted, pull-down calibration is enabled. Connects the SEPD VIO_PAD to the calibration comparator input **Exists:**Always **Synchronous To:**DfiClk
ZCalCompOut	O	Digital output from calibration comparator sampler. **Exists:**Always **Synchronous To:**DfiClk

4.20 Interface to ZCAL Configuration Signals

csrZCalCompVrefDAC
csrZCalDACRangeSel
csrZCalStrenCodePU
csrZCalStrenCodePD
csrZCalTxSlewPU
csrZCalTxSlewPD
csrZCalTxModeCtl
csrZCalCompBiasPowerUp
csrZCalCompBiasBypassEn
csrZCalCompGainCurrAdj
csrZCalCompGainResAdj

Table 4-20 Interface to ZCAL Configuration Signals

Port Name	I/O	Description
csrZCalCompVrefDAC[6:0]	I	Calibration code for the Vref DAC, whose output is to be used as the voltage reference for comparator?s offset calibration. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalDACRangeSel	I	DAC Range Selection. 0=LP5/LP4X Mode. 1=LP4 Mode **Exists:**Always **Synchronous To:**DfiClk
csrZCalStrenCodePU[7:0]	I	Pull-up strength code for the impedance calibration replica drivers. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalStrenCodePD[3:0]	I	Pull-down strength code for the impedance calibration replica drivers. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalTxSlewPU[3:0]	I	Pull-up slew rate control for the impedance calibration replica drivers. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalTxSlewPD[3:0]	I	Pull-down slew rate control for the impedance calibration replica drivers. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalTxModeCtl[2:0]	I	Tx Mode Control for impedance calibration replica Ios **Exists:**Always **Synchronous To:**DfiClk

Port Name	I/O	Description
csrZCalCompBiasPowerUp	I	Reserved for future use field ZCalCompBiasPowerUp **Exists:**Always **Synchronous To:**DfiClk
csrZCalCompBiasBypassEn	I	Reserved for future use field ZCalCompBiasBypassEn **Exists:**Always **Synchronous To:**DfiClk
csrZCalCompGainCurrAdj[7:0]	I	Bias Current Trim and Comparator gain control. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrZCalCompGainResAdj	I	Reserved for future use ZCalCompGainResAdj field **Exists:**Always **Synchronous To:**DfiClk

4.21 Interface to ZCAL Signals

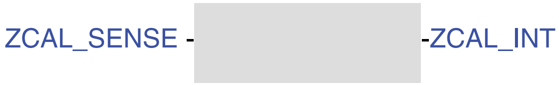


Table 4-21 Interface to ZCAL Signals

Port Name	I/O	Description
ZCAL_SENSE	I	Connect to BP_ZN. Sense input connected to zcalana ZCalPULoad to probe BP_ZN voltage **Exists:**Always **Synchronous To:**Async
ZCAL_INT	O	To be always left Unconnected. Connects to zcalana ZcalPDLoad **Exists:**Always **Synchronous To:**Async

4.22 Interface to VrefDacRef macro Configuration Signals

Table 4-22 Interface to VrefDacRef macro Configuration Signals

Port Name	I/O	Description
csrDacRefModeCtl	I	VrefDacRef Mode Control. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk
csrInAObsEn	I	Analog Observability Enable. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk

4.23 Interface to VrefDacRef macro Control Signals

csrDacRefPwrDn -

Table 4-23 Interface to VrefDacRef macro Control Signals

Port Name	I/O	Description
csrDacRefPwrDn	I	VrefDacRef Power Down. Refer to CSR description. **Exists:**Always **Synchronous To:**DfiClk

4.24 VrefDacRef supply Signals

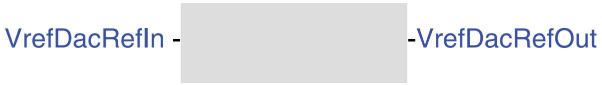


Table 4-24 VrefDacRef supply Signals

Port Name	I/O	Description
VrefDacRefOut	O	From VrefDacRef ckt **Exists:**Always **Synchronous To:**None
VrefDacRefIn	I	Supply for SE_IO and zcalana DAC Rladders **Exists:**Always **Synchronous To:**None

4.25 Interface to POR Control Signals

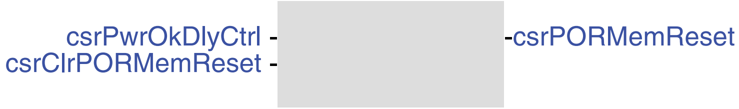


Table 4-25 Interface to POR Control Signals

Port Name	I/O	Description
csrPwrOkDlyCtrl	I	POR control to delay PwrOkVDD, and PwrOkVDD2 assertion. **Exists:**Always **Synchronous To:**DfiClk
csrClrPORMemReset	I	POR control to switch POR self-initialized latch to 1 **Exists:**Always **Synchronous To:**DfiClk
csrPORMemReset	O	POR status signal with MEMRESET_L value. When PwrOk_VDD2 = 1'b0. **Exists:**Always **Synchronous To:**Async

4.26 Power and Ground Supplies Signals

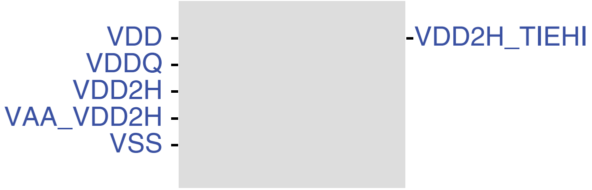


Table 4-26 Power and Ground Supplies Signals

Port Name	I/O	Description
VDD2H_TIEHI	O	Tie high output **Exists:**Always **Synchronous To:**None
VDD	I	Core supply **Exists:**Always **Synchronous To:**None
VDDQ	I	IO buffer power. Connected to VDD in LPDDR4 mode. **Exists:**Always **Synchronous To:**None
VDD2H	I	CMOS driver power, for MEMRESET DTO **Exists:**Always **Synchronous To:**None
VAA_VDD2H	I	PLL supply **Exists:**Always **Synchronous To:**None
VSS	I	Core ground **Exists:**Always **Synchronous To:**None

4.27 Interface to POR CKT Signals

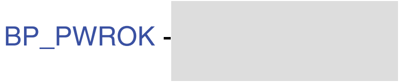


Table 4-27 Interface to POR CKT Signals

Port Name	I/O	Description
BP_PWROK	I	When BP_PWROK (VDD2H domain) is deasserted, PwrOK_VDD2 deasserts and MEMRESET_L/CKE pins are forced in retention state. **Exists:**Always **Synchronous To:**Async

4.28 Interface to SDRAM Signals from IO Cells

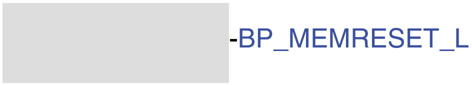


Table 4-28 Interface to SDRAM Signals from IO Cells

Port Name	I/O	Description
BP_MEMRESET_L	O	SEC_IO output pad for MEMRESET_L. **Exists:**Always **Synchronous To:**Async

4.29 Interface to TEST bumps Signals

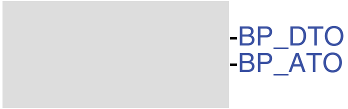


Table 4-29 Interface to TEST bumps Signals

Port Name	I/O	Description
BP_DTO	IO	SEC_IO bi-directional pad for DTO (Digital Test Output) **Exists:**Always **Synchronous To:**Async
BP_ATO	O	Analog pad for ATO. **Exists:**Always **Synchronous To:**Async

4.30 Interface to ZCAL bumps Signals

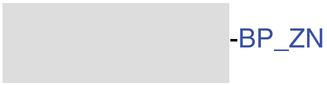


Table 4-30 Interface to ZCAL bumps Signals

Port Name	I/O	Description
BP_ZN	IO	SE_IO pad for Impedance Calibration external reference resistor **Exists:**Always **Synchronous To:**Async

5 DDRPHYDIFF Signal Descriptions

This chapter details all possible I/O signals in the IP. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the controller. It is for reference purposes only.

When you configure the controller in coreConsultant, you must access the I/O signals for your actual configuration at workspace/report/IO.html or workspace/report/IO.xml after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the I/O signals that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the widths might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- **Active State:**Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the inactive state (opposite of the active state).
- **Registered:**Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of *No*does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:**Indicates which clocks in the IP sample this input (drive for an output). This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- **Exists:**Name of configuration parameter that populates this signal in your configuration.

The I/O signals are grouped as follows:

- "Clock Signals" on page 139
- "Reset Signals" on page 140
- "ATPG Signals" on page 141
- "Asynchronous IO Test Signals" on page 142
- "Slice Control Signals" on page 143
- "Bypass mode Signals" on page 144
- "Interface to Transmit Signals" on page 147
- "Command FIFO Control Signals" on page 148
- "IO Control Signals" on page 149
- "Interface to Receiver Signals" on page 152
- "Duty Cycle Adjuster Signals" on page 156
- "BIST Signals" on page 157
- "LCDL Calibration Signals" on page 158
- "Interface to Internal Vref DAC Signals" on page 160
- "Bump Signals" on page 161
- "Power and Ground Supplies Signals" on page 162

5.1 Clock Signals

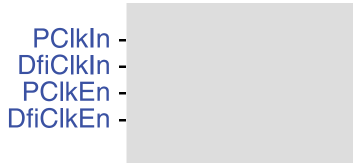


Table 5-1 Clock Signals

Port Name	I/O	Description
PClkIn	I	Pclk input from MASTER slice **Exists:**Always **Synchronous To:**PclkIn
DfiClkIn	I	Dfi Clock input. **Exists:**Always **Synchronous To:**DfiClkIn
PClkEn	I	When asserted, enable PclkIn nside HardIP **Exists:**Always **Synchronous To:**DfiClkIn
DfiClkEn	I	When asserted, enable DfiClkIn nside HardIP **Exists:**Always **Synchronous To:**DfiClkIn

5.2 Reset Signals

Reset_Async -

Table 5-2 Reset Signals

Port Name	I/O	Description
Reset_Async	I	When asserted: ring oscillator flops are reset during atpg_mode **Exists:**Always **Synchronous To:**Atpg_DlyTestClk and Atpg_Pclk

5.3 ATPG Signals

Atpg_PClk -
Atpg_RDQSClk -
Atpg_TxDllClk -
Atpg_DlyTestClk -
Atpg_mode -
Atpg_se -
Atpg_si -
BurnIn -
-Atpg_so

Table 5-3 ATPG Signals

Port Name	I/O	Description
Atpg_PClk	I	ATPG clock for Pclk. Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_PClk
Atpg_RDQSClk	I	Atpg clock for receive DQS clock **Exists:**Always **Synchronous To:**Atpg_RDQSClk
Atpg_TxDllClk	I	Atpg clock for TxDrv clock **Exists:**Always **Synchronous To:**Atpg_TxDllClk
Atpg_DlyTestClk	I	Atpg clock for DlyTestClk **Exists:**Always **Synchronous To:**Atpg_DlyTestClk
Atpg_mode	I	When asserted: scan mode is enabled **Exists:**Always **Synchronous To:**Async
Atpg_se[4:0]	I	SE for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_si[7:0]	I	SI for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_so[7:0]	O	SO for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
BurnIn	I	When asserted: enables the Burn-In mode **Exists:**Always **Synchronous To:**Async

5.4 Asynchronous IO Test Signals

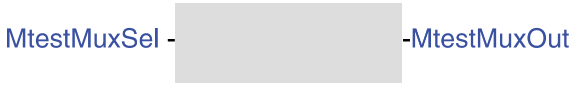


Table 5-4 Asynchronous IO Test Signals

Port Name	I/O	Description
MtestMuxOut	O	Digital test output for debug **Exists:**Always **Synchronous To:**DfiClkIn
MtestMuxSel[5:0]	I	Digital test output select control **Exists:**Always **Synchronous To:**DfiClkIn

5.5 Slice Control Signals

csrReserved -

Table 5-5 Slice Control Signals

Port Name	I/O	Description
csrReserved[3:0]	I	Reserved for future use **Exists:**Always **Synchronous To:**DfiClkIn

5.6 Bypass mode Signals

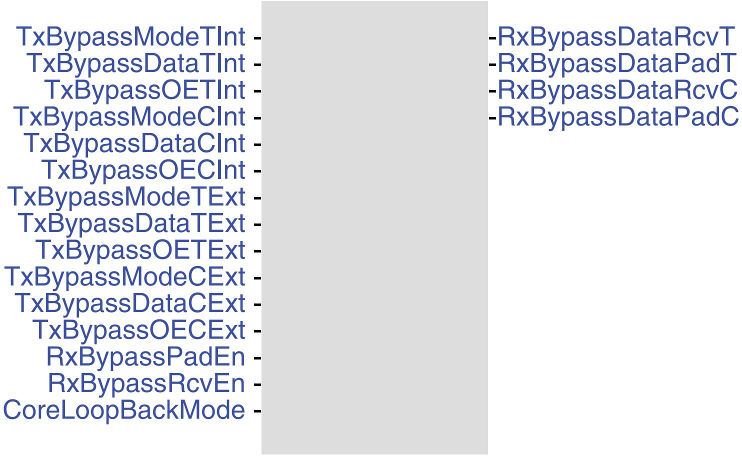


Table 5-6 Bypass mode Signals

Port Name	I/O	Description
TxBypassModeTInt	I	When asserted: enables the setting of data and OE of the TX IOPADT asynchronously using TxBypassDataTInt and TxBypassOETint inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataTInt	I	Asynchronous data to be sent on IOPADT when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassOETInt	I	Asynchronous setting of output enable (OE) for IOPADT when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassModeCInt	I	When asserted: enables the setting of data and OE of the TX IOPADC asynchronously using TxBypassDataCInt and TxBypassOECint inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataCInt	I	Asynchronous data to be sent on IOPADC when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassOECInt	I	Asynchronous setting of output enable (OE) for IOPADC when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
TxBypassModeTExt	I	When asserted: enables the setting of data and OE of the TX IOPADT asynchronously using TxBypassData and TxBypassEn inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataTExt	I	Asynchronous data to be sent on IOPADT when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassOETExt	I	Asynchronous setting of output enable (OE) for IOPADT when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassModeCExt	I	When asserted: enables the setting of data and OE of the TX IOPADC asynchronously using TxBypassData and TxBypassEn inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataCExt	I	Asynchronous data to be sent on IOPADC when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassOECExt	I	Asynchronous setting of output enable (OE) for IOPADC when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
RxBypassPadEn	I	Enable CMOS bypass paths from pad **Exists:**Always **Synchronous To:**Async
RxBypassRcvEn	I	Enable receiver bypass paths **Exists:**Always **Synchronous To:**Async
RxBypassDataRcvT	O	When RxBypassMode is asserted: differentially-sampled true receiver output and 0 when RxBypassRcvEn is not asserted. **Exists:**Always **Synchronous To:**Async
RxBypassDataPadT	O	When RxBypassMode is asserted: asynchronous CMOS input from IOPADT and 0 when RxBypassPadEn is not asserted **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
RxBypassDataRcvC	O	When RxBypassMode is asserted: asynchronous differentially-sampled complement receiver output and 0 when RxBypassRcvEn is not asserted. **Exists:**Always **Synchronous To:**Async
RxBypassDataPadC	O	When RxBypassMode is asserted: asynchronous CMOS input from IOPADC and 0 when RxBypassPadEn is not asserted **Exists:**Always **Synchronous To:**Async
CoreLoopBackMode	I	Enables the loopback MUX in RX path. **Exists:**Always **Synchronous To:**DfiClkIn

5.7 Interface to Transmit Signals

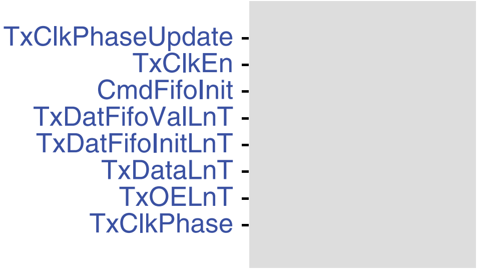


Table 5-7 Interface to Transmit Signals

Port Name	I/O	Description
TxClkPhaseUpdate[7:0]	I	Enables the loading of TxClkPhase into TxClk LCDL **Exists:**Always **Synchronous To:**DfiClkIn
TxClkEn[7:0]	I	Enables the read clock(TxClk) for TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
CmdFifoInit	I	Initializes the CMD fifo pointers **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoValLnT[3:0]	I	Each asserted bit indicates corresponding bit of TxDat/TxEn should be written in TxDatFifo. Used to control IOPADT pin. **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoInitLnT	I	When asserted: Initializes the pointers of TxDatFifo. Used to control IOPADT pin. **Exists:**Always **Synchronous To:**DfiClkIn
TxDataLnT[7:0]	I	TX data input to TxDatFifo. Used to control IOPADT pin. **Exists:**Always **Synchronous To:**DfiClkIn
TxOELnT[7:0]	I	TX Data enable input to TxDatFifo. Used to control IOPADT pin. **Exists:**Always **Synchronous To:**DfiClkIn
TxClkPhase[8:0]	I	TxClk LCDL delay control **Exists:**Always **Synchronous To:**DfiClkIn

5.8 Command FIFO Control Signals

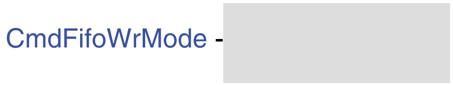


Table 5-8 Command FIFO Control Signals

Port Name	I/O	Description
CmdFifoWrMode	I	Selects the valid width for CMD FiFO write inputs (inputs are always 8 bit wide). Valid values are: 3'b001: Only lower 2 bits will be written in Fifo on each DfiClk. 3'b010: Only lower 4 bits will be written in Fifo on each DfiClk. 3'bb100: All 8 bits will be written on each DfiClk. **Exists:**Always **Synchronous To:**DfiClkIn

5.9 IO Control Signals

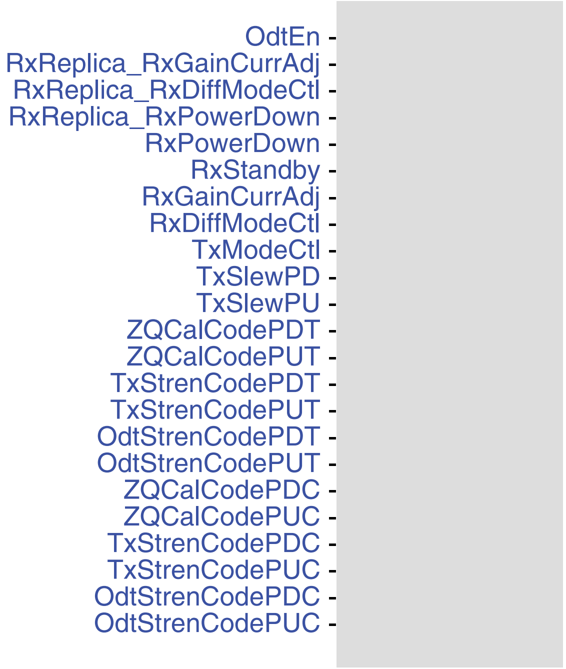


Table 5-9 IO Control Signals

Port Name	I/O	Description
OdtEn	I	When asserted: IOPADT/IOPADC driver is forced in tr-st state and receiver ODT enabled. 1'b0: TxEn controls the driver.1'b1: Forces driver in tri-state mode and enable receiver ODT. Used to implement LPDDR4X / Hynix mode. **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_RxGainCurrAdj[3:0]	I	Gain control for RxReplica RX amplifier **Exists:**Always **Synchronous To:**Async
RxReplica_RxDiffModeCtl[3:0]	I	RxRepl RxDiffModeCtl CSR control bits. Can be used for any static function. **Exists:**Always **Synchronous To:**Async
RxReplica_RxPowerDown	I	When asserted: enables the Powerdown mode of RxReplica Vref (sense-amp currents if any) DACs in receiver. **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
RxPowerDown	I	When asserted: enables the Powerdown mode of Vref (sense-amp currents if any) DACs in receiver. **Exists:**Always **Synchronous To:**Async
RxStandby	I	When asserted: Enables the Standby mode of Vref (sense-amp currents if any) DACs in receiver. **Exists:**Always **Synchronous To:**DfiClkIn
RxGainCurrAdj[3:0]	I	Gain control for RX amplifier **Exists:**Always **Synchronous To:**Async
RxDiffModeCtl[3:0]	I	RxDiffModeCtl CSR control bits. Can be used for any static function. **Exists:**Always **Synchronous To:**Async
TxModeCtl[2:0]	I	Control Pre-Driver (TXPRE) in DIFF_IO. **Exists:**Always **Synchronous To:**Async
TxSlewPD[3:0]	I	Slew rate controls for DIFF_IO PullDown **Exists:**Always **Synchronous To:**Async
TxSlewPU[3:0]	I	Slew rate controls for DIFF_IO PullUp **Exists:**Always **Synchronous To:**Async
ZQCalCodePDT[8:0]	I	IOPADT Pull-down ZQ calibration code **Exists:**Always **Synchronous To:**Async
ZQCalCodePUT[8:0]	I	IOPADT Pull-up ZQ calibration code **Exists:**Always **Synchronous To:**Async
TxStrenCodePDT[3:0]	I	IOPADT Pull-Down drive strength value. **Exists:**Always **Synchronous To:**Async
TxStrenCodePUT[7:0]	I	IOPADT Pull-Up drive strength value. **Exists:**Always **Synchronous To:**Async
OdtStrenCodePDT[3:0]	I	IOPADT Pull-down ODT strength **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
OdtStrenCodePUT[7:0]	I	IOPADT Pull-up ODT strength-Zero in mission mode used in ZQCAL slice to enable and pulldown simultaneously **Exists:**Always **Synchronous To:**Async
ZQCalCodePDC[8:0]	I	IOPADC Pull-down ZQ calibration code **Exists:**Always **Synchronous To:**Async
ZQCalCodePUC[8:0]	I	IOPADC Pull-up ZQ calibration code **Exists:**Always **Synchronous To:**Async
TxStrenCodePDC[3:0]	I	IOPADC Pull-Down drive strength value. **Exists:**Always **Synchronous To:**Async
TxStrenCodePUC[7:0]	I	IOPADC Pull-Up drive strength value. **Exists:**Always **Synchronous To:**Async
OdtStrenCodePDC[3:0]	I	IOPADC Pull-down ODT strength **Exists:**Always **Synchronous To:**Async
OdtStrenCodePUC[7:0]	I	IOPADC Pull-up ODT strength-Zero in mission mode used in ZQCAL slice to enable and pulldown simultaneously **Exists:**Always **Synchronous To:**Async

5.10 Interface to Receiver Signals

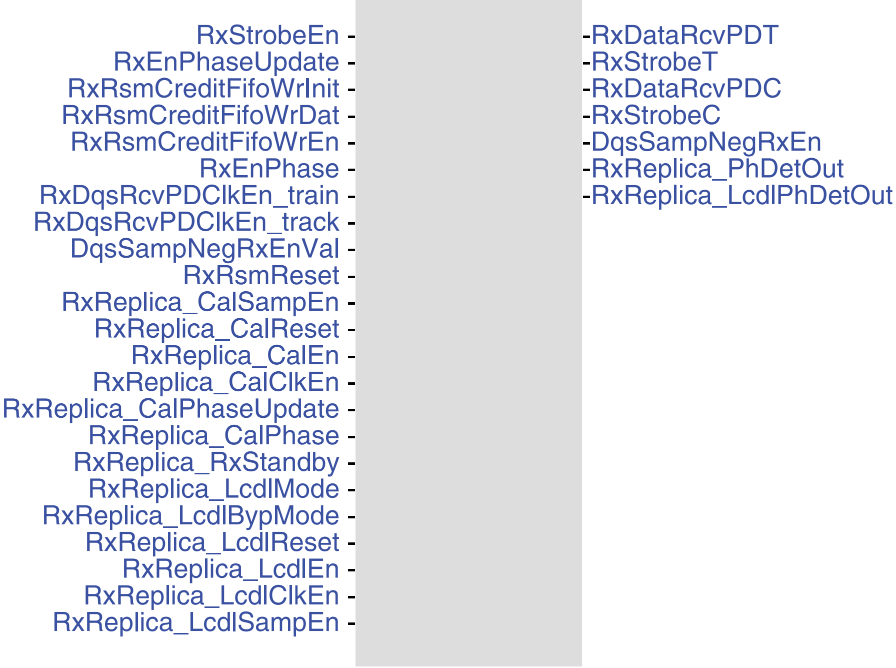


Table 5-10 Interface to Receiver Signals

Port Name	I/O	Description
RxStrobeEn[7:0]	I	Enables differential read strobe from IOPADT/IOPADC to propagate to RxStrobeT/RxStrobeC for read data capture in SE slices **Exists:**Always **Synchronous To:**DfiClkIn
RxEnPhaseUpdate[7:0]	I	Enables the loading of RxStrobeEnPhase into RxStrobeEn LCDL **Exists:**Always **Synchronous To:**DfiClkIn
RxRsmCreditFifoWrInit	I	RxEn RsmCreditFifoWrInit control **Exists:**Always **Synchronous To:**DfiClkIn
RxRsmCreditFifoWrDat[3:0]	I	RxEn RsmCreditFifoWrDat control **Exists:**Always **Synchronous To:**DfiClkIn
RxRsmCreditFifoWrEn[3:0]	I	RxEn RsmCreditFifoWrEn control **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
RxDataRcvPDT	O	Received Core Loop back phase detector data (True) **Exists:**Always **Synchronous To:**DfiClkIn
RxStrobeT	O	Received DQS strobe (True) **Exists:**Always **Synchronous To:**Async
RxDataRcvPDC	O	Received Core Loop back phase detector data (complement) **Exists:**Always **Synchronous To:**DfiClkIn
RxStrobeC	O	Received DQS strobe (Complement) **Exists:**Always **Synchronous To:**Async
RxEnPhase[8:0]	I	Phase input to RxEn LCDL **Exists:**Always **Synchronous To:**DfiClkIn
RxDqsRcvPDClkEn_train	I	when asserted, enables the training of RxEn wrt to receive DQS **Exists:**Always **Synchronous To:**DfiClkIn
RxDqsRcvPDClkEn_track	I	when asserted, enables the tracking of receive DQS phase wrt to RxEn **Exists:**Always **Synchronous To:**DfiClkIn
DqsSampNegRxEnVal	I	RxEnVal control **Exists:**Always **Synchronous To:**DfiClkIn
DqsSampNegRxEn	O	RxEn control **Exists:**Always **Synchronous To:**DfiClkIn
RxRsmReset	I	Resets the Read State Machine logic **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_CalSampEn	I	RxReplica CalSampEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_CalReset	I	RxReplica CalReset Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
RxReplica_CalEn	I	RxReplica CalEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_CalClkEn	I	RxReplica CalClkEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_CalPhaseUpdate	I	RxReplica CalPhaseUpdate Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_CalPhase[8:0]	I	RxReplica CalPhase Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_PhDetOut[4:0]	O	RxReplica PhDetOut Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_RxStandby	I	RxReplica RxStandby Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlMode	I	RxReplica LcdlMode Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlBypMode	I	RxReplica BypMode Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlReset	I	RxReplica LcdlReset Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlEn	I	RxReplica LcdlEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlClkEn	I	RxReplica LcdlClkEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn
RxReplica_LcdlSampEn	I	RxReplica LcdlSampEn Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
RxReplica_LcdlPhDetOut	O	RxReplica LcdlPhDetOut Circuit Control **Exists:**Always **Synchronous To:**DfiClkIn

5.11 Duty Cycle Adjuster Signals

Table 5-11 Duty Cycle Adjuster Signals

Port Name	I/O	Description
TxDcaFinePDT[3:0]	I	IOPADT Fine control for Duty Cycle Pull-down Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaFinePUT[3:0]	I	IOPADT Fine control for Duty Cycle Pull-up Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaCoarseT[1:0]	I	IOPADT Coarse control for Duty Cycle Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaFinePDC[3:0]	I	IOPADC Fine control for Duty Cycle Pull-down Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaFinePUC[3:0]	I	IOPADC Fine control for Duty Cycle Pull-up Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaCoarseC[1:0]	I	IOPADC Coarse control for Duty Cycle Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaMode	I	Enable Duty Cycle Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn

5.12 BIST Signals

Table 5-12 BIST Signals

Port Name	I/O	Description
DlyTestEn	I	When asserted: delay elements become part of a ring oscillator. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestMuxSel[1:0]	I	Selects one of the LCDLs in the slice during ring oscillator testing **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestRun	I	When asserted: ring oscillator starts running and counting.\n[0] : Run TxClk LCDL ring oscillator\n[1] : Run RxStrobeEnLCDL ring oscillator **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntLoad	I	When asserted: ring oscillator counter value is captured into output DlyTestCnt{0/1}. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntInit	I	Resets the ring oscillator counter value. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCnt[15:0]	O	Ring Oscillator count value for TxClk LCDL/RxStrobeEn LCDL based on DlyTestMuxSel **Exists:**Always **Synchronous To:**DfiClkIn

5.13 LCDL Calibration Signals

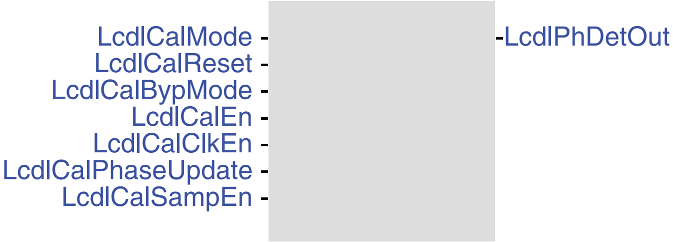


Table 5-13 LCDL Calibration Signals

Port Name	I/O	Description
LcdlCalMode	I	When asserted: the delay line is in calibration mode. In this mode: the delay line is used to measure the clock period **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalReset	I	Asynchronous reset pin to reset the calibration logic **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalBypMode	I	When asserted: the input byp_in of LCDL is chosen to be the output at dly_out. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalEn	I	When asserted: enables the measurement for the selected delay value. This signal is sampled by the calibration clock. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalClkEn	I	When asserted: enables the calibration clock. This is an asynchronous signal and is synchronized inside the delay line to produce an internal glitch-free controlled calibration clock. Valid values are: 0 = Internal calibration clock 1 = Internal calibration clock = cal_clk **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalPhaseUpdate	I	When asserted: delay line coarse and fine delay selects are latched in. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalSampEn	I	When asserted: LCDL calibration status is latched to LcdlPhDetOut output of the HardIP. **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
LcdlPhDetOut[1:0]	O	LCDL calibration status[0] : TxClk LCDL Calibration Status [1] : RxStrobeEnLCDL Calibration Status **Exists:**Always **Synchronous To:**DfiClkIn

5.14 Interface to Internal Vref DAC Signals

Table 5-14 Interface to Internal Vref DAC Signals

Port Name	I/O	Description
RxDiffSeCtl[1:0]	I	Select signal for input Muxes **Exists:**Always **Synchronous To:**DfiClkIn
RxDiffSeVrefDAC[6:0]	I	DAC control for internal Vref **Exists:**Always **Synchronous To:**DfiClkIn
RxDiffSeVrefDACEn	I	Enable signal for Vref DAC **Exists:**Always **Synchronous To:**DfiClkIn

5.15 Bump Signals

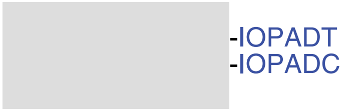


Table 5-15 Bump Signals

Port Name	I/O	Description
IOPADT	IO	DIFF_IO bi-directional pad (True). **Exists:**Always **Synchronous To:**Async
IOPADC	IO	DIFF_IO bi-directional pad (Compliment). **Exists:**Always **Synchronous To:**Async

5.16 Power and Ground Supplies Signals

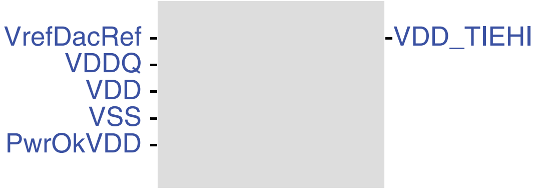


Table 5-16 Power and Ground Supplies Signals

Port Name	I/O	Description
VrefDacRef	I	Reference Voltage **Exists:**Always **Synchronous To:**none
VDD_TIEHI	O	I/O power feedback loop **Exists:**Always **Synchronous To:**none
VDDQ	I	I/O Power Supply **Exists:**Always **Synchronous To:**none
VDD	I	Digital Logic Power Supply **Exists:**Always **Synchronous To:**none
VSS	I	Ground **Exists:**Always **Synchronous To:**none
PwrOkVDD	I	Indicator from Master Hard IP that all power rails are up. Transmitted asynchronously in the VDD power domain. **Exists:**Always **Synchronous To:**none

6

DDRPHYSE Signal Descriptions

This chapter details all possible I/O signals in the IP. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the controller. It is for reference purposes only.

When you configure the controller in coreConsultant, you must access the I/O signals for your actual configuration at workspace/report/IO.html or workspace/report/IO.xml after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the I/O signals that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the widths might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as **<functionof>**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the controller in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- **Active State:**Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the inactive state (opposite of the active state).
- **Registered:**Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of *No*does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:**Indicates which clocks in the IP sample this input (drive for an output). This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- **Exists:**Name of configuration parameter that populates this signal in your configuration.

The I/O signals are grouped as follows:

- “Clock Signals” on page 165
- “Reset Signals” on page 166
- “ATPG Signals” on page 167
- “Asynchronous IO Test Signals” on page 169
- “Slice Control Signals” on page 170
- “Bypass mode Signals” on page 171
- “Interface to Transmit Signals” on page 173
- “Interface to Receiver Signals” on page 174
- “Command FIFO Control Signals” on page 176
- “IO Control Signals” on page 177
- “Duty Cycle Adjuster Signals” on page 179
- “BIST Signals” on page 180
- “LCDL Calibration Signals” on page 181
- “Bump Signals” on page 183
- “Power and Ground Supplies Signals” on page 184

6.1 Clock Signals

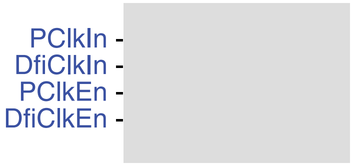


Table 6-1 Clock Signals

Port Name	I/O	Description
PClkIn	I	Pclk input from MASTER slice **Exists:**Always **Synchronous To:**PclkIn
DfiClkIn	I	Dfi Clock input **Exists:**Always **Synchronous To:**DfiClkIn
PClkEn	I	Enables the PclkIn input inside the slice **Exists:**Always **Synchronous To:**DfiClkIn
DfiClkEn	I	Enables the DfiClkIn input inside the slice **Exists:**Always **Synchronous To:**DfiClkIn

6.2 Reset Signals

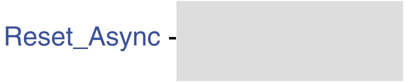


Table 6-2 Reset Signals

Port Name	I/O	Description
Reset_Async	I	When asserted: ring oscillator flops are reset during atpg_mode **Exists:**Always **Synchronous To:**Atpg_DlyTestClk and Atpg_Pclk

6.3 ATPG Signals

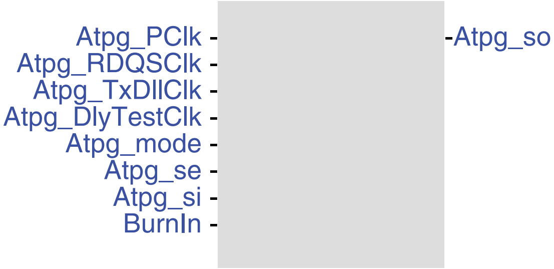


Table 6-3 ATPG Signals

Port Name	I/O	Description
Atpg_PClk	I	ATPG clock for Pclk. Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_DlyTestClk
Atpg_RDQSClk	I	ATPG clock input used for Read DQS read clock(RDQS). Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_RDQSClk
Atpg_TxDllClk	I	ATPG clock input used for TxData FIFO read clock(TxClk). Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_TxDllClk
Atpg_DlyTestClk	I	ATPG clock input used for Delay line ring oscillator scan chain . Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_PClk
Atpg_mode	I	When asserted: scan mode is enabled **Exists:**Always **Synchronous To:**Async
Atpg_se[4:0]	I	Scan Enable inputs for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_si[8:0]	I	Scan In inputs for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_so[8:0]	O	SO for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk

Port Name	I/O	Description
BurnIn	I	When asserted: enables the Burn-In mode **Exists:**Always **Synchronous To:**Async

6.4 Asynchronous IO Test Signals

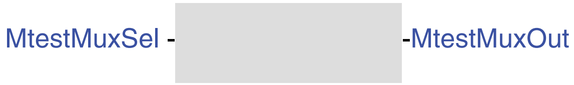


Table 6-4 Asynchronous IO Test Signals

Port Name	I/O	Description
MtestMuxOut	O	Digital test output for debug **Exists:**Always **Synchronous To:**DfiClkIn
MtestMuxSel[5:0]	I	Digital test output select control **Exists:**Always **Synchronous To:**DfiClkIn

6.5 Slice Control Signals

csrReserved -

Table 6-5 Slice Control Signals

Port Name	I/O	Description
csrReserved[1:0]	I	Reserved for future use **Exists:**Always **Synchronous To:**DfiClkIn

6.6 Bypass mode Signals

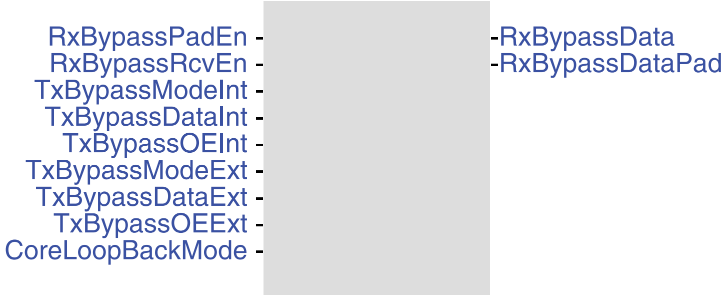


Table 6-6 Bypass mode Signals

Port Name	I/O	Description
RxBypassPadEn	I	Enable CMOS bypass paths from pad **Exists:**Always **Synchronous To:**Async
RxBypassRcvEn	I	Enable bypass outputs from receivers **Exists:**Always **Synchronous To:**Async
RxBypassData[3:0]	O	Bypass (RX-DAT (cmos)). When RxBypassRcvEn is asserted then synchronously sampled receive data output is returned on this output. When RxBypassRcvEn is de-asserted then this output is forced 0. **Exists:**Always **Synchronous To:**Async
RxBypassDataPad	O	Bypass (RX-DAT (cmos)). When RxBypassRcvEn is asserted then asynchronously sampled receive data for IOPAD is returned on this output. When RxBypassRcvEn is de-asserted then this output is forced 0. **Exists:**Always **Synchronous To:**Async
TxBypassModeInt	I	When asserted: enables the settting of data and OE of the TX pad asynchronously using TxBypassDataInt and TxBypassEnInt inputs **Exists:**Always **Synchronous To:**Async
TxBypassDataInt	I	Asynchronous data to be sent on TX pad when TxBypassModeInt is asserted **Exists:**Always **Synchronous To:**Async
TxBypassOEInt	I	Asynchronous setting of OE of TX pad when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
TxBypassModeExt	I	When asserted: enables the settting of data and OE of the TX pad asynchronously using TxBypassDataExt and TxBypassExt inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataExt	I	Asynchronous data to be sent on TX pad when TxBypassModeExt is asserted **Exists:**Always **Synchronous To:**Async
TxBypassOEExt	I	Asynchronous setting of OE of TX pad when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
CoreLoopBackMode	I	Enables the loopback MUX in RX path **Exists:**Always **Synchronous To:**DfiClkIn

6.7 Interface to Transmit Signals

TxClkPhaseUpdate
TxClkEn
TxData
TxOE
TxDatFifoVal
TxDatFifoInit
TxClkPhase

Table 6-7 Interface to Transmit Signals

Port Name	I/O	Description
TxClkPhaseUpdate[7:0]	I	Enables the loading of TxClkPhase into TxClk LCDL **Exists:**Always **Synchronous To:**DfiClkIn
TxClkEn[7:0]	I	Enables the read clock(TxClk) for TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
TxData[7:0]	I	TX data input to TxDatFifo **Exists:**Always **Synchronous To:**DfiClkIn
TxOE[7:0]	I	TX Data enable input to TxDatFifo **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoVal[3:0]	I	Each asserted bit indicates corresponding bit of TxDat/TxEn should be written in TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoInit	I	When asserted: Initializes the pointers of TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
TxClkPhase[8:0]	I	TxClk LCDL delay control. **Exists:**Always **Synchronous To:**DfiClkIn

6.8 Interface to Receiver Signals

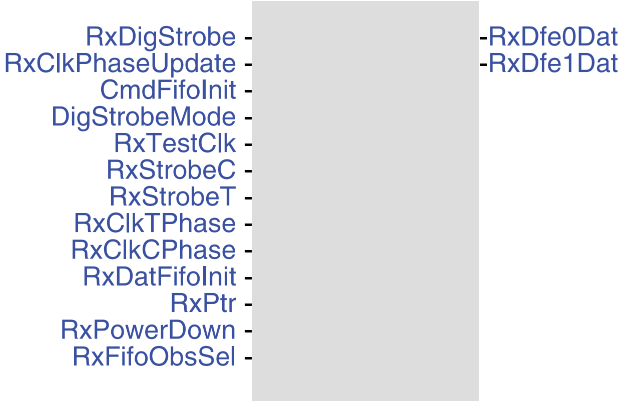


Table 6-8 Interface to Receiver Signals

Port Name	I/O	Description
RxDigStrobe[7:0]	I	Generates internal strobe for Rx data capture in LPDDR5 strobe-less mode. **Exists:**Always **Synchronous To:**DfiClkIn
RxClkPhaseUpdate[7:0]	I	Enables the loading of RxClkTPhase into Rx True Strobe LCDL and RxClkCPhase into Rx Compliment Strobe LCDL. **Exists:**Always **Synchronous To:**DfiClkIn
CmdFifoInit	I	Initializes the CMD fifo pointers. **Exists:**Always **Synchronous To:**DfiClkIn
DigStrobeMode[1:0]	I	Selects the strobe used for RxDatFifo capture. 0x: External read DQS (RxByteStrobe inputs from DIFF slice) 10: Internally generated strobe. 11: BypassRxClk **Exists:**Always **Synchronous To:**DfiClkIn
RxTestClk	I	Used for latch receive data for RxBypassDataEven (rising edge) and RxBypassDataOdd (falling edge) when not in mission mode. In mission mode this clock is not used. RDQS or CDR will perform this function. This signals intended used is for VIL/VIH testing or non-mission-mode JTAG SAMPLE. **Exists:**Always **Synchronous To:**RxTestClk
RxStrobeC	I	Gated read DQS strobe (complimentary) from DIFF Slice. **Exists:**Always **Synchronous To:**RxStrobeC

Port Name	I/O	Description
RxStrobeT	I	Gated read DQS strobe (true) from DIFF slice. **Exists:**Always **Synchronous To:**RxStrobeT
RxClkTPhase[8:0]	I	Rx true Strobe LCDL delay control. Same encoding as TxClk LCDL control. **Exists:**Always **Synchronous To:**DfiClkIn
RxClkCPhase[8:0]	I	Rx Compliment Strobe LCDL delay control. Same encoding as TxClk LCDL control. **Exists:**Always **Synchronous To:**DfiClkIn
RxDatFifoInit	I	Initializes the RXFIFO read pointer to zero. **Exists:**Always **Synchronous To:**DfiClkIn
RxPtr[5:0]	I	Read pointer of RxData FIFO **Exists:**Always **Synchronous To:**DfiClkIn
RxDfe0Dat[7:0]	O	Dfe0 Rx Data from capture FIFO in terms of UI. **Exists:**Always **Synchronous To:**DfiClkIn
RxDfe1Dat[7:0]	O	Dfe1 Rx Data from capture FIFO in terms of UI. **Exists:**Always **Synchronous To:**DfiClkIn
RxPowerDown	I	When asserted it enables the Powerdown mode of Vref (sense-amp currents if any) DACs in receiver. **Exists:**Always **Synchronous To:**DfiClkIn
RxFifoObsSel	I	Select the RxData FIFO write pointers for observation **Exists:**Always **Synchronous To:**DfiClkIn

6.9 Command FIFO Control Signals

CmdFifoWrMode -

Table 6-9 Command FIFO Control Signals

Port Name	I/O	Description
CmdFifoWrMode	I	Selects the valid width for CMD FiFO write inputs (inputs are always 8 bit wide). Valid values are: 3`b001: Only lower 2 bits will be written in Fifo on each DfiClk. 3`b010: Only lower 4 bits will be written in Fifo on each DfiClk. 3`b100: All 8 bits will be written on each DfiClk. **Exists:**Always **Synchronous To:**DfiClkIn

6.10 IO Control Signals

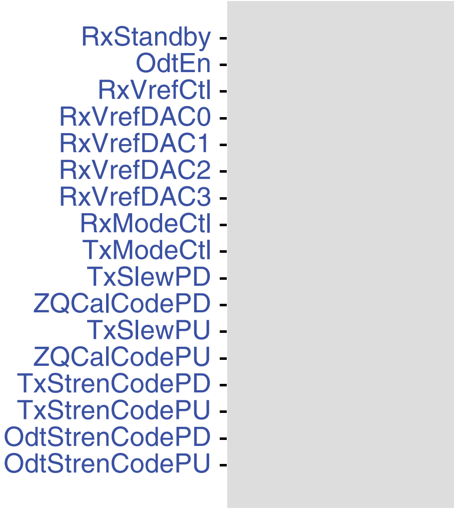


Table 6-10 IO Control Signals

Port Name	I/O	Description
RxStandby	I	when asserted, receiver is in sandby mode to save power **Exists:**Always **Synchronous To:**DfiClkIn
OdtEn	I	When asserted, it enables the ODT strength of the receiver **Exists:**Always **Synchronous To:**DfiClkIn
RxVrefCtl[1:0]	I	DFE controls to enable forcing of DFE on and forcing Vref for DFE channel0 and forcing Vref of DFE channel1 Also used for DFE training (or also per-rank VREF if we enable that feature): 2`b00: DFE 0 on / DFE 1 off (DFE Off) 2`b01: DFE 0 on / DFE 1 on (DFE On) 2`b10: DFE 0 on / DFE 1 off (Force DFE 0) 2`b11: DFE 0 off / DFE 1 on (Force DFE) **Exists:**Always **Synchronous To:**Async
RxVrefDAC0[6:0]	I	Internal Vref value for DFE channel0 Receiver. **Exists:**Always **Synchronous To:**Async
RxVrefDAC1[6:0]	I	Internal Vref value for DFE channel1 Receiver. **Exists:**Always **Synchronous To:**Async
RxVrefDAC2[6:0]	I	Vref value for Compensation of DFE channel0 Receiver. **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
RxVrefDAC3[6:0]	I	Vref value for Compensation of DFE channel1 Receiver. **Exists:**Always **Synchronous To:**Async
RxModeCtl[3:0]	I	[0] Kickback correction disable [3:1] RFU **Exists:**Always **Synchronous To:**Async
TxModeCtl[2:0]	I	Control Pre-Driver (TXPRE) in SE_IO. **Exists:**Always **Synchronous To:**Async
TxSlewPD[3:0]	I	Slew rate Pull-down controls for SE_IO **Exists:**Always **Synchronous To:**Async
ZQCalCodePD[8:0]	I	Pull-down ZQ calibration code **Exists:**Always **Synchronous To:**Async
TxSlewPU[3:0]	I	Slew rate Pull-up controls for SE_IO **Exists:**Always **Synchronous To:**Async
ZQCalCodePU[8:0]	I	Pull-up ZQ calibration code **Exists:**Always **Synchronous To:**Async
TxStrenCodePD[3:0]	I	Pull-Down drive strength value. **Exists:**Always **Synchronous To:**Async
TxStrenCodePU[7:0]	I	Pull-Up drive strength value. **Exists:**Always **Synchronous To:**Async
OdtStrenCodePD[3:0]	I	Pull-down ODT strength **Exists:**Always **Synchronous To:**Async
OdtStrenCodePU[7:0]	I	Pull-up ODT strength Zero in mission mode?used in ZQCAL slice to enable and pulldown simultaneously **Exists:**Always **Synchronous To:**Async

6.11 Duty Cycle Adjuster Signals

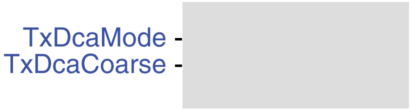


Table 6-11 Duty Cycle Adjuster Signals

Port Name	I/O	Description
TxDcaMode	I	Enable Duty Cycle Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn
TxDcaCoarse[1:0]	I	Coarse control for Duty Cycle Adjustment. **Exists:**Always **Synchronous To:**DfiClkIn

6.12 BIST Signals

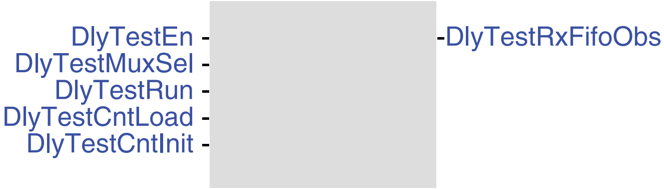


Table 6-12 BIST Signals

Port Name	I/O	Description
DlyTestEn	I	When asserted: delay elements become part of a ring oscillator. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestMuxSel[1:0]	I	Selects one of the LCDLs in the slice during ring oscillator testing **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestRun	I	When asserted: ring oscillator starts running and counting. [0] : Run TxClk LCDL ring oscillator [1] : Run Rx True Strobe LCDL ring oscillator [2]: Run Rx Compliment Strobe LCDL ring oscillator **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntLoad	I	When asserted: ring oscillator counter value is captured into output DlyTestCnt{0/1/2}. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntInit	I	Resets the ring oscillator counter value. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestRxFifoObs[15:0]	O	RxFIFO write pointers or ring oscillator counter value **Exists:**Always **Synchronous To:**DfiClkIn

6.13 LCDL Calibration Signals

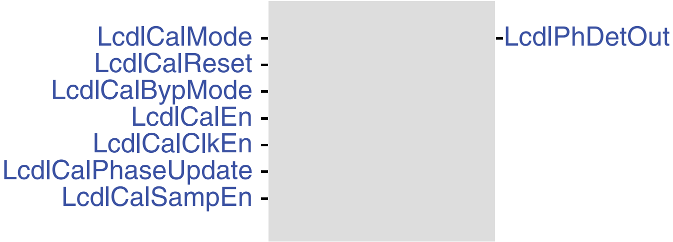


Table 6-13 LCDL Calibration Signals

Port Name	I/O	Description
LcdlCalMode	I	When asserted: the delay line is in calibration mode. In this mode the delay line is used to measure the clock period **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalReset	I	Asynchronous reset pin to reset the calibration logic **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalBypMode	I	When asserted: the input byp_in of LCDL is chosen to be the output at dly_out. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalEn	I	When asserted: enables the measurement for the selected delay value. This signal is sampled by the calibration clock. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalClkEn	I	When asserted: enables the calibration clock. This is an asynchronous signal and is synchronized inside the delay line to produce an internal glitch-free controlled calibration clock. Valid values are: 0 = Internal calibration clock 1 = Internal calibration clock = cal_clk **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalPhaseUpdate	I	When asserted: delay line coarse and fine delay selects are latched in **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalSampEn	I	When asserted: LCDL calibration status is latched to LcdlPhDetOut output of the HardIP **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
LcdlPhDetOut[2:0]	O	LCDL calibration status [0] : TxClk LCDL Calibration Status [1] : Rx True Strobe LCDL Calibration Status [2]: Rx Compliment Strobe LCDL calibration Status **Exists:**Always **Synchronous To:**DfiClkIn

6.14 Bump Signals

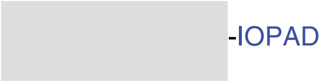


Table 6-14 Bump Signals

Port Name	I/O	Description
IOPAD	IO	SE_IO bi-directional pad. **Exists:**Always **Synchronous To:**Async

6.15 Power and Ground Supplies Signals

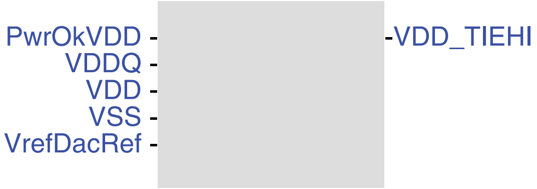


Table 6-15 Power and Ground Supplies Signals

Port Name	I/O	Description
PwrOkVDD	I	Indicator from Master Hard IP that all power rails are up. Transmitted asynchronously in the VDD power domain. **Exists:**Always **Synchronous To:**none
VDDQ	I	I/O Power Supply **Exists:**Always **Synchronous To:**none
VDD	I	Digital Logic Power Supply **Exists:**Always **Synchronous To:**none
VSS	I	Ground **Exists:**Always **Synchronous To:**none
VrefDacRef	I	Reference Volatge **Exists:**Always **Synchronous To:**none
VDD_TIEHI	O	I/O power feedback loop **Exists:**Always **Synchronous To:**none

7

DDRPHYSEC Signal Descriptions

This chapter details all possible I/O signals in the IP. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the controller. It is for reference purposes only.

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In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

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- **Registered:**Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of *No*does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:**Indicates which clocks in the IP sample this input (drive for an output). This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- **Exists:**Name of configuration parameter that populates this signal in your configuration.

The I/O signals are grouped as follows:

- "Clock Signals" on page 187
- "Reset Signals" on page 188
- "ATPG Signals" on page 189
- "Asynchronous IO Test Signals" on page 190
- "Slice Control Signals" on page 191
- "Bypass mode Signals" on page 192
- "Interface to Transmit Signals" on page 194
- "Interface to Receiver Signals" on page 195
- "Command FIFO Control Signals" on page 196
- "IO Control Signals" on page 197
- "BIST Signals" on page 198
- "LCDL Calibration Signals" on page 199
- "Bump Signals" on page 201
- "Power and Ground Supplies Signals" on page 202

7.1 Clock Signals

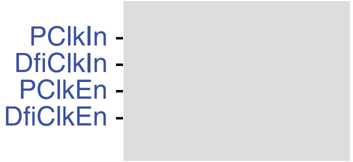


Table 7-1 Clock Signals

Port Name	I/O	Description
PClkIn	I	Pclk input from MASTER slice **Exists:**Always **Synchronous To:**PClkIn
DfiClkIn	I	Dfi Clock input **Exists:**Always **Synchronous To:**DfiClkIn
PClkEn	I	Enables the PclkIn input inside the slice **Exists:**Always **Synchronous To:**DfiClkIn
DfiClkEn	I	Enables the DfiClkIn input inside the slice **Exists:**Always **Synchronous To:**DfiClkIn

7.2 Reset Signals

Reset_Async -

Table 7-2 Reset Signals

Port Name	I/O	Description
Reset_Async	I	Asynchronous Reset used during atpg_mode **Exists:**Always **Synchronous To:**Async

7.3 ATPG Signals

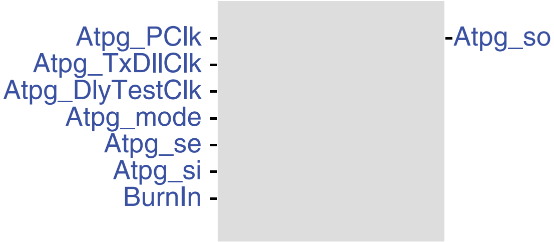


Table 7-3 ATPG Signals

Port Name	I/O	Description
Atpg_PClk	I	ATPG clock input used for PclkIn scan chains. Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_PClk
Atpg_TxDllClk	I	ATPG clock input used for TxData FIFO read clock(TxClk). Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_TxDllClk
Atpg_DlyTestClk	I	ATPG clock input used for Delay line ring oscillator scan chain . Must be 0 during mission mode. **Exists:**Always **Synchronous To:**Atpg_DlyTestClk
Atpg_mode	I	When asserted: scan mode is enabled **Exists:**Always **Synchronous To:**Async
Atpg_se[3:0]	I	Scan Enable inputs for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_si[4:0]	I	Scan In inputs for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
Atpg_so[4:0]	O	Scan Out for scan chains **Exists:**Always **Synchronous To:**Atpg_*clk
BurnIn	I	When asserted: enables the Burn-In mode **Exists:**Always **Synchronous To:**Async

7.4 Asynchronous IO Test Signals

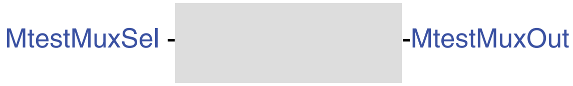


Table 7-4 Asynchronous IO Test Signals

Port Name	I/O	Description
MtestMuxOut	O	Digital test output for debug **Exists:**Always **Synchronous To:**Async
MtestMuxSel[5:0]	I	Digital test output select control **Exists:**Always **Synchronous To:**DfiClkIn

7.5 Slice Control Signals

csrReserved -

Table 7-5 Slice Control Signals

Port Name	I/O	Description
csrReserved[2:0]	I	Reserved for future use **Exists:**Always **Synchronous To:**DfiClkIn

7.6 Bypass mode Signals

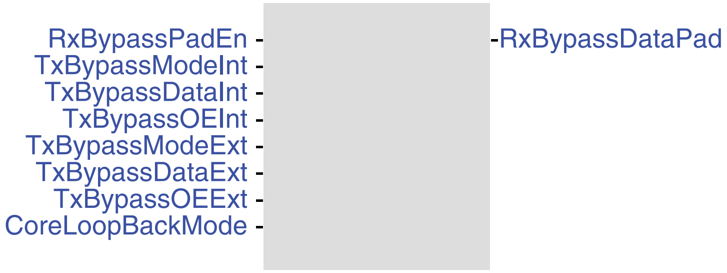


Table 7-6 Bypass mode Signals

Port Name	I/O	Description
RxBypassPadEn	I	Enable CMOS bypass paths from pad **Exists:**Always **Synchronous To:**Async
RxBypassDataPad	O	Bypass (RX-DAT (cmos)). When RxBypassPadEn is asserted then asynchronously sampled receive data for IOPAD is returned on this output. When RxBypassPadEn is de-asserted then this output is forced 0. **Exists:**Always **Synchronous To:**Async
TxBypassModeInt	I	When asserted: enables the settting of data and OE of the TX pad asynchronously using TxBypassDataInt and TxBypassEnInt inputs **Exists:**Always **Synchronous To:**Async
TxBypassDataInt	I	Asynchronous data to be sent on TX pad when TxBypassModeInt is asserted **Exists:**Always **Synchronous To:**Async
TxBypassOEInt	I	Asynchronous setting of OE of TX pad when TxBypassModeInt is asserted. **Exists:**Always **Synchronous To:**Async
TxBypassModeExt	I	When asserted: enables the settting of data and OE of the TX pad asynchronously using TxBypassDataExt and TxBypassExt inputs. **Exists:**Always **Synchronous To:**Async
TxBypassDataExt	I	Asynchronous data to be sent on TX pad when TxBypassModeExt is asserted **Exists:**Always **Synchronous To:**Async

Port Name	I/O	Description
TxBypassOEExt	I	Asynchronous setting of OE of TX pad when TxBypassModeExt is asserted. **Exists:**Always **Synchronous To:**Async
CoreLoopBackMode	I	When asserted, Enables the loopback MUX in RX path **Exists:**Always **Synchronous To:**DfiClkIn

7.7 Interface to Transmit Signals

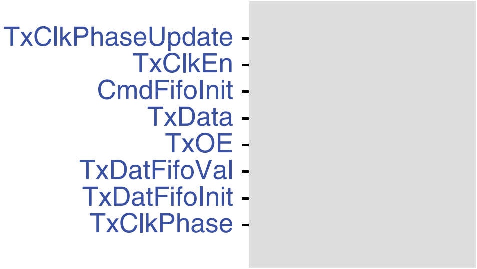


Table 7-7 Interface to Transmit Signals

Port Name	I/O	Description
TxClkPhaseUpdate[7:0]	I	When asserted, Enables the loading of TxClkPhase into TxClk LCDL **Exists:**Always **Synchronous To:**DfiClkIn
TxClkEn[7:0]	I	When asserted, Enables the read clock(TxClk) for TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
CmdFifoInit	I	When asserted, Initializes the CMD fifo pointers. **Exists:**Always **Synchronous To:**DfiClkIn
TxData[7:0]	I	TX data input to TxDatFifo **Exists:**Always **Synchronous To:**DfiClkIn
TxOE[7:0]	I	TX Data enable input to TxDatFifo **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoVal[3:0]	I	Each asserted bit indicates corresponding bit of TxDat/TxEn should be written in TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
TxDatFifoInit	I	When asserted: Initializes the pointers of TxDatFifo. **Exists:**Always **Synchronous To:**DfiClkIn
TxClkPhase[8:0]	I	TxClk LCDL delay control. **Exists:**Always **Synchronous To:**DfiClkIn

7.8 Interface to Receiver Signals

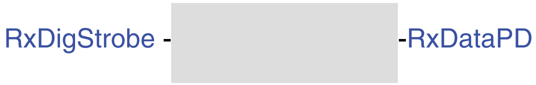


Table 7-8 Interface to Receiver Signals

Port Name	I/O	Description
RxDigStrobe[7:0]	I	Generates internal strobe for Rx data capture during loopback test mode **Exists:**Always **Synchronous To:**DfiClkIn
RxDataPD	O	Asynchronous Phase Detector output **Exists:**Always **Synchronous To:**Async

7.9 Command FIFO Control Signals

CmdFifoWrMode -

Table 7-9 Command FIFO Control Signals

Port Name	I/O	Description
CmdFifoWrMode	I	Selects the valid width for CMD FiFO write inputs (inputs are always 8 bit wide). 1`b0: Only lower 4 bits will be written in the FIFO on each DfiClk. 1`b1: All 8 bits will be written in the FIFO each DfiClk. **Exists:**Always **Synchronous To:**DfiClkIn

7.10 IO Control Signals

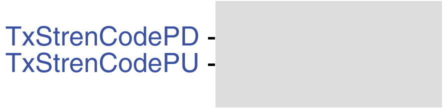


Table 7-10 IO Control Signals

Port Name	I/O	Description
TxStrenCodePD[1:0]	I	Pull-Down drive strength value. **Exists:**Always **Synchronous To:**Async
TxStrenCodePU[1:0]	I	Pull-Up drive strength value. **Exists:**Always **Synchronous To:**Async

7.11 BIST Signals

DlyTestEn -
DlyTestMuxSel -
DlyTestRun -
DlyTestCntLoad -
DlyTestCntInit -
-DlyTestCnt

Table 7-11 BIST Signals

Port Name	I/O	Description
DlyTestEn	I	When asserted: delay elements become part of a ring oscillator. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestMuxSel[1:0]	I	Selects one of the LCDLs in the slice during ring oscillator testing **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestRun	I	When asserted: ring oscillator starts running and counting. [0] : Run TxClk LCDL ring oscillator [1] : Run Rx True Strobe LCDL ring oscillator [2]: Run Rx Compliment Strobe LCDL ring oscillator **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntLoad	I	When asserted: ring oscillator counter value is captured into output DlyTestCnt{0/1/2}. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCntInit	I	Resets the ring oscillator counter value. **Exists:**Always **Synchronous To:**DfiClkIn
DlyTestCnt[15:0]	O	Ring oscillator counter output **Exists:**Always **Synchronous To:**DfiClkIn

7.12 LCDL Calibration Signals

LcdlCalMode -
LcdlCalReset -
LcdlCalBypMode -
LcdlCalEn -
LcdlCalClkEn -
LcdlCalPhaseUpdate -
LcdlCalSampEn -
-LcdlPhDetOut

Table 7-12 LCDL Calibration Signals

Port Name	I/O	Description
LcdlCalMode	I	When asserted: the delay line is in calibration mode. In this mode: the delay line is used to measure the clock period **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalReset	I	Asynchronous reset pin to reset the calibration logic **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalBypMode	I	When asserted: the input byp_in of LCDL is chosen to be the output at dly_out. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalEn	I	When asserted: enables the measurement for the selected delay value. This signal is sampled by the calibration clock. **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalClkEn	I	When asserted: enables the calibration clock. This is an asynchronous signal and is synchronized inside the delay line to produce an internal glitch-free controlled calibration clock. Valid values are: 0 = Internal calibration clock 1 = Internal calibration clock = cal_clk **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalPhaseUpdate	I	When asserted: delay line coarse and fine delay selects are latched in **Exists:**Always **Synchronous To:**DfiClkIn
LcdlCalSampEn	I	When asserted: LCDL calibration status is latched to LcdlPhDetOut output of the HardIP **Exists:**Always **Synchronous To:**DfiClkIn

Port Name	I/O	Description
LcdlPhDetOut	O	LCDL calibration status [0] : TxClk LCDL Calibration Status [1] : Rx True Strobe LCDL Calibration Status [2]: Rx Compliment Strobe LCDL calibration Status **Exists:**Always **Synchronous To:**DfiClkIn

7.13 Bump Signals

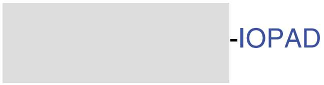


Table 7-13 Bump Signals

Port Name	I/O	Description
IOPAD	IO	SE_IO bi-directional pad. **Exists:**Always **Synchronous To:**Async

7.14 Power and Ground Supplies Signals

VDD2H -
VDD -
VSS -
PwrOkVDD -
PwrOkVDD2 -

Table 7-14 Power and Ground Supplies Signals

Port Name	I/O	Description
VDD2H	I	CMOS IO Power Supply **Exists:**Always **Synchronous To:**none
VDD	I	Digital Logic Power Supply **Exists:**Always **Synchronous To:**none
VSS	I	Ground **Exists:**Always **Synchronous To:**none
PwrOkVDD	I	Indicator from Master Hard IP that all power rails are up. Transmitted asynchronously in the VDD power domain. **Exists:**Always **Synchronous To:**none
PwrOkVDD2	I	Indicator from Master Hard IP that all power rails are up. Transmitted asynchronously in the VDD2H power domain. **Exists:**Always **Synchronous To:**none

8

Electrical Specifications

The following chapters are included in this section:

8.1 Operating Conditions

All voltages are referenced to VSS.

8.1.1 Recommended Operating Conditions

The following table shows the PHY operating conditions, including supply voltages and temperature.

Note Correct operation of the IP is not guaranteed if the recommended operating conditions for VDD, VDDQ, VDD2H, and VAA_VDD2H are exceeded.

Table 8-1 Recommended Operating Conditions

Symbol[1]	Description	Minimum	Typical	Maximum	Units
V_{DD}[2,3,4,5]	Core Voltage - Supports data rates of 6400 Mbps and below	V_{DD}(Typ) -7%	0.75	VDD(Typ) +10%	V
VRIP_VDD (pk-pk)	Core power/ground supply rail peak-to-peak ripple			4	%VDD(Typ)
VDDQ_DRAM[6]	SDRAM VDDQ supply: LPDDR4 mode	1.06	1.1	1.17	V
V_{DDQ}[2,7]	PHY VDDQ supply: LPDDR4 mode, DC average[8]	VDD(Min)	VDD(Typ)	VDD(Max)	V
V_{DDQ}[2,7]	PHY VDDQ supply: LPDDR4X mode, DC average[8]	0.57	0.6	0.65	V
V_{DDQ}[2,7]	PHY VDDQ supply: LPDDR5 mode, DC average[8,9]	0.47	0.5	0.57	V
V_{DDQ}[2,7]	PHY VDDQ supply: LPDDR5 mode, DC average[8,10]	0.27	0.3	0.37	V
VRIP_VDDQ (pk-pk)	I/O power/ground supply rail peak-to-peak ripple: LPDDR4 mode			10	%VDDQ(Typ)
VRIP_VDDQ (pk-pk)	I/O power/ground supply rail peak-to-peak ripple: LPDDR4X mode			10	%VDDQ(Typ)
VRIP_VDDQ (pk-pk)	I/O power/ground supply rail peak-to-peak ripple: LPDDR5 mode			10	%VDDQ(Typ)
Vrange_VDDQ[2]	PHY VDDQ supply LPDDR4 mode, allowed range[11]	VDDQ (LPDDR4 Typ) -10%		VDDQ (LPDDR4 Typ) +10%	V
Vrange_VDDQ[2]	PHY VDDQ supply LPDDR4X mode, allowed range[11]	VDDQ (LPDDR4X Typ) -10%		VDDQ (LPDDR4X Typ) +10%	V

Symbol[1]	Description	Minimum	Typical	Maximum	Units
Vrange_VDDQ [2]	PHY VDDQ supply LPDDR5 mode, allowed range[11]	VDDQ (LPDDR5 Typ) -10%		0.57[9] or 0.37[10]	V
V_{DD2H}[2]	V_{DD2H} supply: LPDDR4 mode[8] [12]	1.06	1.1	1.17	V
V_{DD2H}[2]	V_{DD2H} supply: LPDDR4X mode[8]	1.06	1.1	1.17	V
V_{DD2H}[2]	V_{DD2H} supply: LPDDR5 mode[8]	1.01	1.05	1.12	V
VRIP_VDD2H (pk-pk)	VDD2H power/ground supply rail peak-to-peak ripple: LPDDR4 mode			10	% VDD2H(Typ)
VRIP_VDD2H (pk-pk)	VDD2H power/ground supply rail peak-to-peak ripple: LPDDR4X mode			10	% VDD2H(Typ)
VRIP_VDD2H (pk-pk)	VDD2H power/ground supply rail peak-to-peak ripple: LPDDR5 mode			10	% VDD2H(Typ)
Vrange_VDD2H [2]	PHY VDD2H supply LPDDR4 mode, allowed range[11]	VDD2H (LPDDR4 Typ) -10%		VDD2H (LPDDR4 Typ) +10%	V
Vrange_VDD2H [2]	PHY VDD2H supply LPDDR4X mode, allowed range[11]	VDD2H (LPDDR4X Typ) -10%		VDD2H (LPDDR4X Typ) +10%	V
Vrange_VDD2H [2]	PHY VDD2H supply LPDDR5 mode, allowed range[11]	VDD2H (LPDDR5 Typ) -10%		VDD2H (LPDDR5 Typ) +10%	V
VAA_VDD2H[2]	PLL supply voltage connected to independent 1.8 V supply VAA_VDD2H	VAA_VDD2H(Typ) -7%	1.8	VAA_VDD2H(Typ) +10%	V
VRIP_VAA_VDD2H (pk-pk)	PLL power/ground supply rail peak-to-peak ripple when connected to VAA_VDD2H = 1.8 V			5	%VAA_VDD2H(Typ)
VAA_VDD2H (VDD2H)[2]	PLL supply voltage VAA_VDD2H connected to VDD2H[13]	See Minimum V_{DD2H} (per mode above)	See Typical V_{DD2H} (per mode above)	See Maximum V_{DD2H} (per mode above)	V
VRIP_VAA_VDD2H(VDD2H)(pk-pk)	PLL power/ground supply rail peak-to-peak ripple when connected VDD2H			2	%VAA_VDD2H(VDD2H(Typ))
RVDDQ RVAA	Supply power-up ramp rate for VDDQ, VDD2H, VAA_VDD2H[14]			5	mV/us
RVDD	Supply power-up ramp rate for V_{DD}[15]			150	mV/us

Symbol[1]	Description	Minimum	Typical	Maximum	Units
TJ	Junction Temperature	-40		125	°C

1. Correct operation of the IP is not guaranteed if the recommended operating conditions for VDD, VDDQ, VDD2H, and VAA_VDD2H are exceeded.
2. Voltages VDD, VDDQ, VDD2H, and VAA_VDD2H are measured at the pins of the hard IP macrocells.
3. Core voltage range (VDD) includes ripple.
4. Power, jitter, and aging analysis are performed at DC average VDD levels of +/- 5%
5. Electromigration conditions can be found in section "EM Conditions" on page 228
6. This supply is referenced to the DRAM supply for IO spec purposes. It is not a supply used in the PHY.
7. Power and jitter analysis are performed at DC average of VDDQ(min) and VDDQ(max) = JEDEC min/max voltages, plus ripple of +/-(VRIP_VDDQ/2)
8. Voltage range is for DC voltage only. DC is inclusive of all noise up to 20 Mhz.
9. Intended for IO operation with both ODT enabled and disabled.
10. Intended for IO operation with ODT disabled.
11. Vrange_* includes DC plus ripple
12. Connect VDD2H supply to DRAM's VDDQ(VDDQ_DRAM) for receiver VREF tracking purposes.
13. PLL power supply VAA_VDD2H is allowed to be connected to either VAA_VDD2H or VDD2H voltage levels. When VAA_VDD2H of PLL is connected to VDD2H, VDD2H needs to be filtered on the package or board in order to provide clean supply for PLL. Noise limit for VDD2H filtered is same as when it is connected to VAA_VDD2H, which is VRIP_VAA_VDD2H in "Operating Conditions" on page 204
14. The VDDQ, VDD2H and VAA_VDD2H power supplies are limited to a maximum supply ramp rate listed in "Operating Conditions" on page 204 above. This limit prevents triggering of the internal clamps on those power supplies. All IP designs must make a trade-off around protecting from ESD events. A super-fast power rail ramp rate during normal operation looks significantly like an ESD discharge that has the potential to damage the chip. Our power rail requirements are linked to our trade-offs between allowing power rails to be driven by a wide variety of sources with different characteristics, versus having ESD clamps which trigger at conservative rates to ensure the chip is not damaged.
15. VDD power supplies are limited to a maximum supply ramp rate of 150mV/us. This limit is required for proper operation of the Power-On-Reset custom circuit. A super-fast power rail ramp rate during normal operation could create glitching on reset signals.

8.1.1.1 Core Voltage Tolerance

The following images show the core voltage tolerance, allowable jitter, and relationship to PVT points for both minimum and maximum voltages.

Figure 8-1 Core Voltage Tolerance for Minimum VDD Voltage

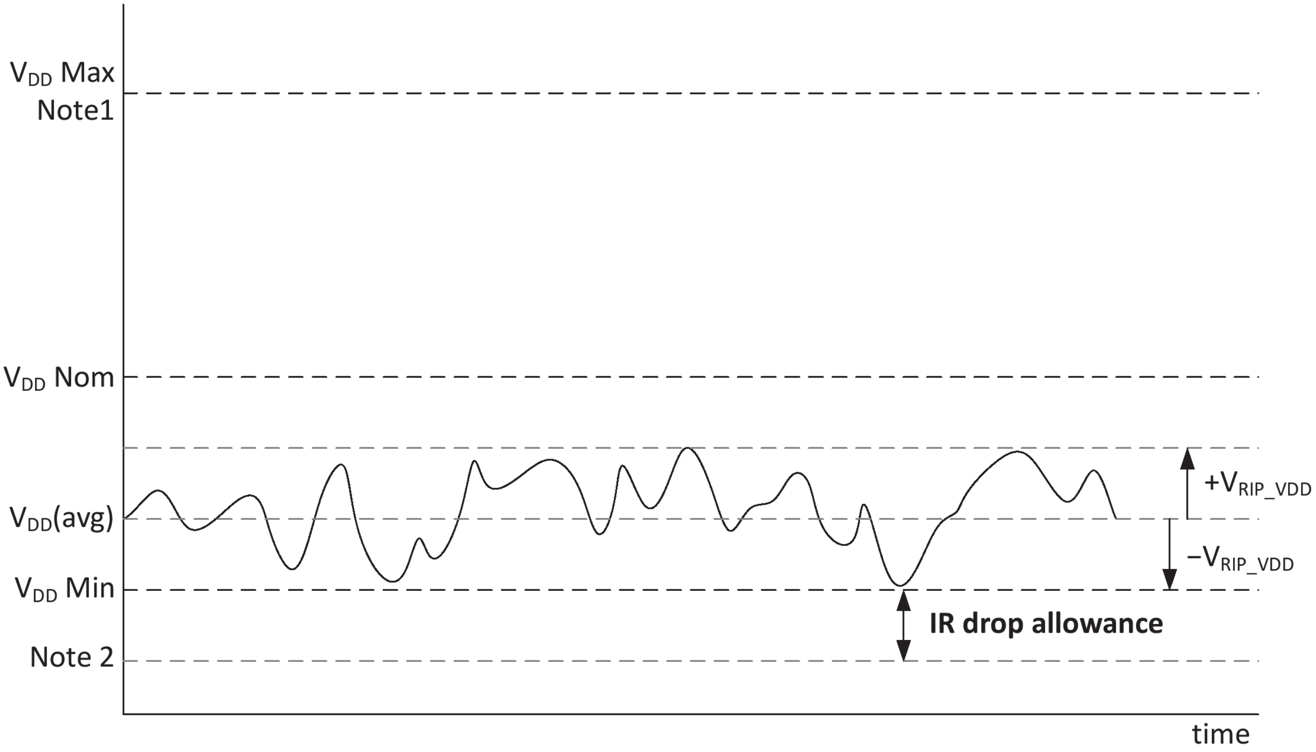


Figure 8-2 Core Voltage Tolerance for Maximum VDD Voltage

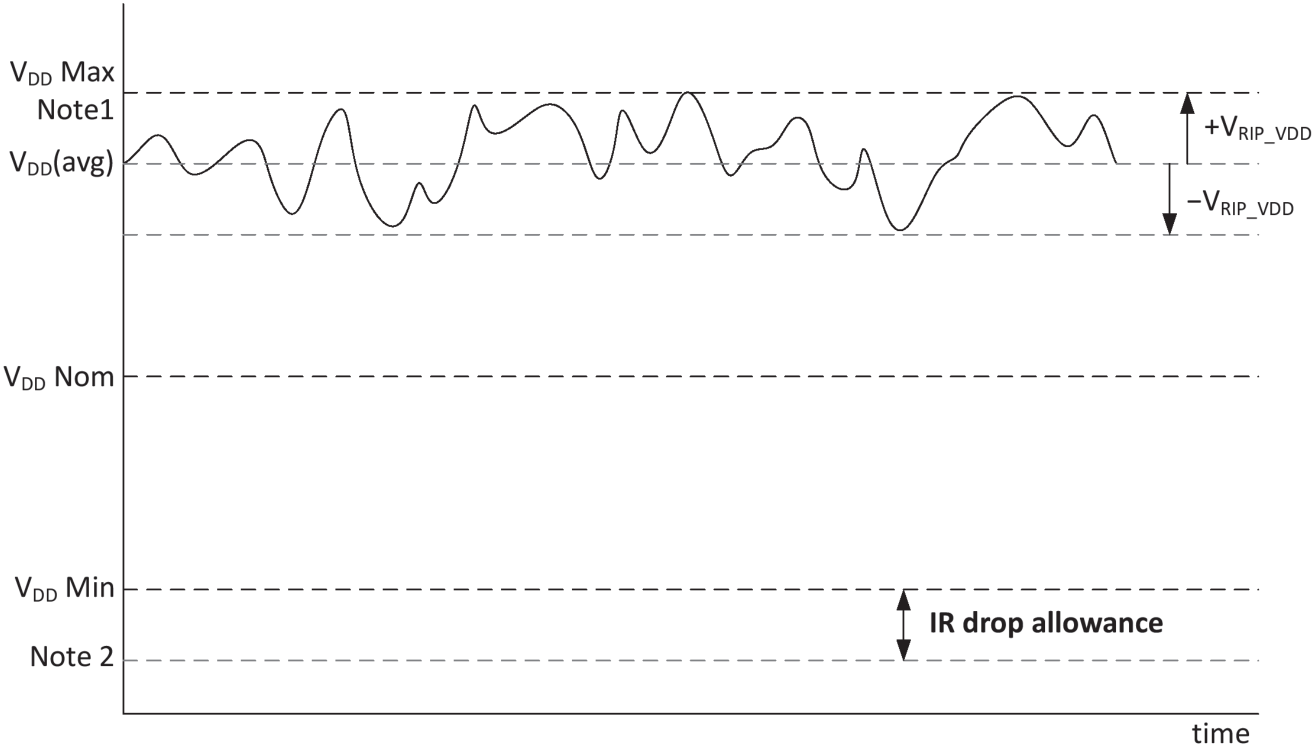


Figure Notes:

1. VDDMax is also the maximum voltage used in the timing .lib files
2. As shown in the figures, there is an IR drop allowance for the supply voltage to the individual transistors in the hard IP macrocells between VDDMin and the minimum voltage used in the timing .lib files.

Note It is strongly recommended to isolate the PHY's core VDD supply from that of the other components in the SOC in order to minimize noise on the PHY core VDD supply and reduce IO-related jitter and timing margin degradation, The supply can be shared between these regions in the package if one or more package bypass caps are used, with the bypass caps of sufficient value to isolate the noise from the non-PHY region.

8.1.2 Library PVT Corners

The following table describes the standard PVT points for the .lib and .db files provided with the PHY.

Table 8-2 Standard PVT Points for the .lib and .db Files for the PHY

Process	VDD (V)	VAA_VDD2H (V)	VDDQ (V) / VDD2H (V)	Temperature	Extraction Point
TT	0.75	1.80	Nominal for DDR Protocol	25	typical
SS	0.675	1.62	Minimum for DDR Protocol	-40 / 0 / 125	cworst_CCworst, rcworst_CCworst, cbest_CCbest, rcbest_CCbest
FF	0.825	1.98	Maximum for DDR Protocol	-40 / 0 / 125	cworst_CCworst, rcworst_CCworst, cbest_CCbest, rcbest_CCbest

8.1.3 Power-on Characteristics

This section describes the characteristics of the Power Supply Level Sensor. This circuit forces known values onto the level shifter outputs when VDD is too low to propagate signals internally. For more information on the Power Supply Level Sensor refer to "Power On Reset: POR (dwc_ddrphy_por)" on page 252

Table 8-3 VDD Power Supply Level Sensor Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Power Supply Ramp Up Trip Value	Trip_rup_sen	%	35		85	1
Power Supply Ramp Down Trip Value	Trip_rdn_sen	%	15		75	1
Hysteresis	Vtrip_hys_sen	mV	50			

Table Notes:

1. Percentage of all typical VDD values from "Operating Conditions" on page 204

Table 8-4 VDD2H Power Supply Level Sensor Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Power Supply Ramp Up Trip Value	Trip_rup_sen	%	20		80	1
Power Supply Ramp Down Trip Value	Trip_rdn_sen	%	15		75	1
Hysteresis	Vtrip_hys_sen	mV	50			

Table Notes:

1. Percentage of all typical VDD2H values from "Operating Conditions" on page 204

8.2 Electrical Parameters

8.2.1 Common Input Conditions

The following tables list the parameters that are common across all memory interface standards. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins.

Subsequent sections list parameters for specific memory interface standards.

Table 8-5 Common DC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
BP_DAT input leakage current	IIZ	uA			173	1
Input high voltage for BP_DAT	VIH-DC	V	Vref + 0.020			2,3
Input low voltage for BP_DAT	VIL-DC	V			Vref – 0.020	2,3
Differential input voltage for abs(DQS_t – DQS_c)	VID-DC	V	0.1			4

Table Notes:

1. Leakage current is measured when the pin is configured to a high-impedance state with all on-die termination disabled. Leakage is valid for any input except for Vref over the range:0 <= VIN <+= VDDQ. All pins not under test = VSS or VDDQ.
2. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined.
3. After running offset cancellation training sequence
4. The differential voltage VID is the difference between the true and complement signals. Absolute value taken so that minimum spec applies to both high and low differential inputs.

Table 8-6 Common AC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Input capacitance SE	CpadSE	pF	1.195		1.230	1, 2
Input capacitance DIFF	CpadDIFF_T	pF	1.207		1.240	1, 2
	CpadDIFF_C	pF	1.208		1.240	1, 2

Table Notes:

1. This is specified at the top level of the SE and DIFF hard-macros. It does not include any customer-supplied routing between these blocks and the C4 bump.
2. Effective parallel capacitance when ODT of 40 ohm is enabled.

Table 8-7 Common DC Input Conditions for Flyover Bypass

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Input high voltage	VIH_DC	V	0.7 * VDD			1
Input low voltage	VIL_DC	V			0.3* VDD	1

Table Notes:

1. BP_MEMRESET_L and BP_ZN do not support Flyover Bypass mode

Table 8-8 Common DC Input Conditions for BP_PWROK

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Input high voltage	VIH_DC	V	0.7 * VDD2H			
Input low voltage	VIL_DC	V			0.3* VDD2H	

8.2.1.1 LPDDR5 Input Conditions

Table 8-9 LPDDR5 DC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
On-die termination (ODT) programmable resistances	RTT	ohm		open, 120, 60, 40, 30		1, 2
ODT low-level (0.2*VDDQ) large-signal resistance	RODT-L / RTT		0.8	1.0	1.1	3
ODT mid-level (0.5*VDDQ) large-signal resistance	RODT-M / RTT		0.9	1.0	1.1	3, 4
ODT high-level (0.75*VDDQ) large-signal resistance	RODT-H / RTT		0.9	1.0	1.3	3

Table Notes:

1. ODT is configurable based on DIMM and DRAM configuration.
2. For LPDDR5, ODT is a pull-down to VSS.
3. ODT large-signal resistance is defined for an applied input voltage VIN and a measured input current of IIN as:

$$R_{ODT} = \frac{V_{IN}}{I_{IN}}$$

4. Calibrated large signal resistance targets RODT-L/RTT = 1.0 across PVT. Min/Max values account for calibration resolution, mismatch, and other effects.

Table 8-10 LPDDR5 AC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Low-speed Input high voltage for BP_DAT (logic 1)	VIH-ACLS	V	Vref + 0.050		VDDQ + 0.150	1, 2, 6, 8
Low-speed Input low voltage for BP_DAT (logic 0)	VIL-ACLS	V	–0.150		Vref - 0.050	1, 2, 6, 8
High-speed input high voltage for BP_DAT (logic 1)	VIH-ACHS	V	Vref + 0.050		VOH	1, 3, 7, 8
High-speed input low voltage for BP_DAT (logic 0)	VIL-ACHS	V	0		Vref - 0.050	1, 3, 7, 8
ODT low-level (0.2*VDDQ) small-signal resistance	RODTss-L / RTT		0.75		1.05	4
ODT mid-level (0.5*VDDQ) small-signal resistance	RODTss-M / RTT		0.85		1.05	4
ODT high-level (0.75*VDDQ) small-signal resistance	RODTss-H / RTT		0.95		1.75	4
Input crossing voltage for differential signals DQS*	VIX	mV	VDQSavg – 75	VDQSavg	VDQSavg + 75	5

Table Notes:

1. This is the voltage at which the input receiver must be able to discriminate a high or a low input during a transient switching event.
2. The wider signal swing allowance causes a timing penalty due to the larger amount of cap charging and discharging in the receiver.
3. This narrower signal swing range incurs no timing penalty. Timing budgets are built using this signal swing.
4. Small-signal resistance is defined, for measured input current IIN as a function of applied voltage VIN, as the first derivative of the V-I plot:

$$R_{ODTss} = \frac{dV_{IN}}{dI_{IN}}$$

5. VDQSavg is defined as the average of 0.5*(DQS_t + DQS_c).
6. Low-speed refers to data rates less than or equal to 1600 Mbps.
7. High-speed refers to data rates greater than 1600 Mbps.
8. The Vref value is dependent on pull-up/VOH and pull-down/ODT. PHY Vref is internally generated and programmed through local Vref generation at each receiver.

Table 8-11 LPDDR5 Input Slew Rates Versus Data Rate (in MT/s)

			3200		3733		4267		6400		
Parameter	**Symbol**	**Units**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
Input slew rate: Single-ended signals	Sin	V/ns	1.67	9	1.67	9	1.67	9	1.67	9	1
Input slew rate: Differential signals	Sin	V/ns	3.3	18	3.3	18	3.3	18	3.3	18	2
Input slew rate mismatch between related BP_DAT pins	Smismatch	V/ns		0.6		0.6		0.6		0.6	1, 3

Table Notes:

1. This parameter applies to all single-ended memory input signals to the processor. The input slew rate is measured at the CPU pin between minimum VIH-AC – Vref for rising edge and Vref – maximum VIL-AC for the falling edge, where Vref is the programmed level for the internal reference voltage.
2. This parameter applies to all differential input signals to the processor. The differential input slew rate is measured differentially at the CPU pin between ±90mV for rising and falling edges.
3. These are the BP_DAT* pins associated with the same timing group, corresponding to all pins in a byte.

8.2.1.2 LPDDR4X Input Conditions

Table 8-12 LPDDR4X DC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
On-die termination (ODT) programmable resistances	RTT	Ohm		open, 120, 60, 40, 30		1, 2
ODT mid-level (0.2*VDDQ) large-signal resistance	RODT-L / RTT		0.8	1.0	1.1	3
ODT high-level (0.5*VDDQ) large-signal resistance	RODT-M / RTT		0.9	1.0	1.1	3, 4
ODT high-level (0.75*VDDQ) large-signal resistance	RODT-H / RTT		0.9	1.0	1.3	3

Table Notes:

1. The ODT level is programmable based on DIMM and DRAM configuration.
2. For LPDDR4X, ODT is a pull-down to VSS.
3. ODT large-signal resistance is defined for an applied input voltage VIN and a measured input current of IIN as

$$R_{ODT} = \frac{V_{IN}}{I_{IN}}$$

4. Calibrated large signal resistance targets RODT-L/RTT = 1.0 across PVT. Min/Max values account for calibration resolution, mismatch, and other effects.

Table 8-13 LPDDR4X AC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Low-speed Input high voltage for BP_DAT (logic 1)	VIH-ACLS	V	Vref + 0.050		VDDQ + 0.150	1, 2, 6, 8
Low-speed Input low voltage for BP_DAT (logic 0)	VIL-ACLS	V	–0.150		Vref - 0.050	1, 2, 6, 8
High-speed input high voltage for BP_DAT (logic 1)	VIH-ACHS	V	Vref + 0.050		VOH	1, 3, 7, 8
High-speed input low voltage for BP_DAT (logic 0)	VIL-ACHS	V	0		Vref - 0.050	1, 3, 7, 8
ODT low-level (0.2*VDDQ) small-signal resistance	RODTss-L / RTT		0.75		1.05	4
ODT mid-level (0.5*VDDQ) small-signal resistance	RODTss-M / RTT		0.85		1.05	4
ODT high-level (0.75*VDDQ) small-signal resistance	RODTss-H / RTT		0.95		1.75	4
Input crossing voltage for differential signals DQS*	VIX	mV	VDQSavg – 75	VDQSavg	VDQSavg + 75	5

Table Notes:

1. This is the voltage at which the input receiver must be able to discriminate a high or a low input during a transient switching event.
2. The wider signal swing allowance causes a timing penalty due to the larger amount of cap charging and discharging in the receiver.
3. This narrower signal swing range incurs no timing penalty. Timing budgets are built using this signal swing.
4. Small-signal resistance is defined, for measured input current IIN as a function of applied voltage VIN, as the first derivative of the V-I plot:

$$R_{ODTss} = \frac{dV_{IN}}{dI_{IN}}$$

5. VDQSavg is defined as the average of 0.5*(DQS_t + DQS_c).
6. Low-speed refers to data rates less than or equal to 1600 Mbps.
7. High-speed refers to data rates greater than 1600 Mbps.
8. The Vref value is dependent on pull-up/VOH and pull-down/ODT. PHY Vref is internally generated and programmed through local Vref generation at each receiver.

Table 8-14 LPDDR4X Input Slew Rates Versus Data Rate (in MT/s)

			2400		2667		3200		3733		4267		
Parameter	Symbol	Units	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Input slew rate: Single-ended signals	Sin	V/ns	1.25	9	1.4	9	1.67	9	1.67	9	1.67	9	1
Input slew rate: Differential signals	Sin	V/ns	2.5	18	2.8	18	3.3	18	3.3	18	3.3	18	2
Input slew rate mismatch between related BP_DAT pins	Smismatch	V/ns		0.8		0.6		0.6		0.6		0.6	1, 3

Table Notes:

1. This parameter applies to all single-ended memory input signals to the processor. The input slew rate is measured at the CPU pin between minimum VIH-AC – Vref for rising edge and Vref – maximum VIL-AC for the falling edge, where Vref is the programmed level for the internal reference voltage.
2. This parameter applies to all differential input signals to the processor. The differential input slew rate is measured differentially at the CPU pin between ±90mV for rising and falling edges.
3. These are the BP_DAT* pins associated with the same timing group, corresponding to all pins in a byte.

8.2.1.3 LPDDR4 Input Conditions

Table 8-15 LPDDR4 DC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
On-die termination (ODT) programmable resistances	RTT	Ohm		120, 60, 40, 30		1, 2, 3
ODT mid-level (0.1*VDDQ) large-signal resistance	RODT-L / RTT		0.8	1.0	1.1	4
ODT high-level (0.33*VDDQ) large-signal resistance	RODT-M / RTT		0.9	1.0	1.1	4, 5
ODT high-level (0.5*VDDQ) large-signal resistance	RODT-H / RTT		0.9	1.0	1.3	4

Table Notes:

1. The ODT level is programmable based on DIMM and DRAM configuration.
2. For LPDDR4, ODT is a pull-down to VSS.
3. IO operation is supported only with ODT enabled.
4. ODT large-signal resistance is defined for an applied input voltage VIN and a measured input current of IIN as

$$R_{ODT} = \frac{V_{IN}}{I_{IN}}$$

5. Calibrated large signal resistance targets RODT-L/RTT = 1.0 across PVT. Min/Max values account for calibration resolution, mismatch, and other effects.

Table 8-16 LPDDR4 AC Input Conditions

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Low-speed input high voltage for BP_DAT (logic 1)	VIH-ACLS	V	Vref + 0.050		VDDQ + 0.150	1, 2, 6, 8, 9
Low-speed input low voltage for BP_DAT (logic 0)	VIL-ACLS	V	–0.150		Vref – 0.050	1, 2, 6, 8, 9
High-speed input high voltage for BP_DAT (logic 1)	VIH-ACHS	V	Vref + 0.050		VOH	1, 3, 7, 8, 9
High-speed input low voltage for BP_DAT (logic 0)	VIL-ACHS	V	0		Vref – 0.050	1, 3, 7, 8, 9
ODT mid-level (0.1*VDDQ) small-signal resistance	RODTss-M / RTT		0.75		1.05	4
ODT high-level (0.33*VDDQ) small-signal resistance	RODTss-H / RTT		0.85		1.05	4
ODT high-level (0.5*VDDQ) small-signal resistance	RODTss-H / RTT		0.95		1.75	4
Input crossing voltage for differential signals DQS*	VIX	mV	VDQSavg – 75	VDQSavg	VDQSavg + 75	5

1. This is the voltage at which the input receiver must be able to discriminate a high or a low input during a transient switching event.
2. The wider signal swing allowance causes a timing penalty due to the larger amount of cap charging and discharging in the receiver.
3. This narrower signal swing range incurs no timing penalty. Timing budgets are built using this signal swing.
4. Small-signal resistance is defined, for measured input current IIN as a function of applied voltage VIN, as the first derivative of the V-I plot:

$$R_{ODTss} = \frac{dV_{IN}}{dI_{IN}}$$

5. VDQSavg is defined as the average of 0.5*(DQS_t + DQS_c).
6. Low-speed refers to data rates less than or equal to 1600 Mbps.
7. High-speed refers to data rates greater than 1600 Mbps.
8. IO operation is supported only with ODT enabled.

9. The Vref value is dependent on pull-up/VOH and pull-down/ODT. PHY Vref is internally generated and programmed through local Vref generation at each receiver.

Table 8-17 LPDDR4 Input Slew Rates Versus Data Rate (in MT/s)

			2400		2667		3200		3733		4267		
Parameter	**Symbol**	**Units**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
Input slew rate: Single-ended signals	Sin	V/ns	1.25	9	1.4	9	1.67	9	1.67	9	1.67	9	1
Input slew rate: Differential signals	Sin	V/ns	2.5	18	2.8	18	3.3	18	3.3	18	3.3	18	2
Input slew rate mismatch between related BP_DAT pins	Smismatch	V/ns		0.8		0.6		0.6		0.6		0.6	1, 3

Table Notes:

1. This parameter applies to all single-ended memory input signals to the processor. The input slew rate is measured at the CPU pin between minimum VIH-AC – Vref for rising edge and Vref – maximum VIL-AC for the falling edge, where Vref is the programmed level for the internal reference voltage.
2. This parameter applies to all differential input signals to the processor. The differential input slew rate is measured differentially at the CPU pin between ±90mV for rising and falling edges.
3. These are the BP_DAT* pins associated with the same timing group, corresponding to all pins in a byte.

8.2.2 Common Output Conditions

The following tables list the parameters that are common across all memory interface standards. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins. Subsequent sections list parameters for specific memory interface standards. For the common parameters, please note that not all specifications are relevant for every interface standard.

Table 8-18 Common DC Output Parameters

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Output driver pull-down impedance: SE, DIFF	ROnPd	ohm		120, 60, 40, 30		1
Output driver pull-up impedance: SEC	ROnSECPu	ohm		400, 100, 66.6, 50		2
Output driver pull-down impedance: SEC	ROnSECPd	ohm		400, 100, 66.6, 50		2
Large-signal SEC pull-up driver variation at 0.5*VDD2H	ROnSECPu05 / ROn		0.5	1.0	1.8	3
Large-signal SEC pull-down driver variation at 0.5*VDD2	ROnSECPd05 / ROn		0.5	1.0	1.8	4

Table Notes:

1. Calibrated at VOH. The drive strength options are detailed in Table 9-10 on page 275 and Table 9-11 on page 276.
2. SEC output driver is uncalibrated and minimum/maximum impedance value is process, voltage, and temperature dependent.
3. Large-signal output resistance is defined for an applied voltage VOUT and a measured current of IOUT as:

$$R_{OUT} = \frac{V_{DD2} - V_{OUT}}{I_{OUT}}$$

4. Large-signal pull-down output resistance is defined for an applied voltage VOUT and a measured current of IOUT as

$$R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

Table 8-19 Common AC Output Parameters

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Small-signal SEC pull-up driver variation at 0.5*VDD2	ROnssDQPu25 / ROn		0.5		3	1
Small-signal SEC pull-down driver variation at 0.5*VDD2	ROnssDQPd25 / ROn		0.5		3	1

Table Notes:

1. Small-signal resistance is defined, for measured input current IIN as a function of applied voltage VIN, as the first derivative of the V-I plot:

$$R_{ODTss} = \frac{dV_{IN}}{dI_{IN}}$$

Table 8-20 Output Timing Characteristics

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
M_DQS high pulse width	tDQSH	ps	0.46*tck		0.54*tck	1
M_DQS low pulse width	tDQSL	ps	0.46*tck		0.54*tck	1

Table Notes:

1. This timing parameter applies to all address, bank address, command, and control signals.

Table 8-21 Common DC Output Conditions for Flyover Bypass

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Output high voltage	VOH_DC	V	0.8 * VDDQ			1, 2, 3, 4
Output low voltage	VOL_DC	V			0.2 * VDDQ	1, 2, 3, 4

Table Notes:

1. VOH_DC and VOL_DC for Flyover Bypass mode limit is without termination
2. For VOH / VOL DC testing with current load, use the following formula: maximum loading < (0.2*VDDQ / Ron)*0.9, Ron can be found in the "Common DC Output Parameters" table where Ron = RonPu or RonPd depending on signal direction.
3. When atpg_mode = 1, all output drivers are forced to maximum drive strength.
4. BP_MEMRESET_L and BP_ZN do not support Flyover Bypass mode

Table 8-22 Common DC Output Conditions for SEC

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
Output high voltage	VOH_DC	V	0.8 * VDD2H		VDD2H	1, 2, 3, 4
Output low voltage	VOL_DC	V	VSS		0.2* VDD2H	1, 2, 3, 4

Table Notes:

1. SEC drives full CMOS level without termination
2. For VOH / VOL DC testing with current load, use the following formula: maximum loading < (0.2*VDD2H / Ron)*0.9, Ron can be found in the "Common DC Output Parameters" table where Ron = RonPu or RonPd depending on signal direction.
3. For BP_MEMRESET_L, all IO drivers are forced to maximum drive strength for all protocols.
4. SEC is used for BP_MEMRESET_L, BP_DTO, LPDDR5-CS, and LPDDR4-CKE interfaces

8.2.2.1 LPDDR5 Output Parameters

Table 8-23 LPDDR5 DC Output Parameters

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
SEO, DIFF pull-up output driver characteristics, with ZQ calibration: VOHPU,nom = VDDQ*0.5	VOH,nom	mV		250		1, 2
	VOHPU,nom	VOH,nom	0.9	1.0	1.1	1, 2

Table Notes:

1. All values are after ZQ Calibration. Without ZQ Calibration VOH,nom values are ± 30%
2. VOH,nom (mV) values are based on a nominal VDDQ = 0.5V

Table 8-24 LPDDR5 Output Slew Rates Versus Data Rate (in MT/s)

			2400		2667		3200		4267		
Parameter	**Symbol**	**Units**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
Output slew rate: Single-ended signals	Sout-DQ	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	1,2,6,8
Output slew rate: Differential signals	Sout-DQ S	V/ns	6	16	6	16	6	16	6	16	1,3,6
Output slew rate: command and address	Sout-CA	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	4,5,7
			4800		**5333**		**5818**		**6400**		
Parameter	**Symbol**	**Units**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
Output slew rate: Single-ended signals	Sout-DQ	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	1,2,6,8
Output slew rate: Differential signals	Sout-DQ S	V/ns	6	16	6	16	6	16	6	16	1,3,6
Output slew rate: command and address	Sout-CA	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	4,5,7

Table Notes:

1. Slew rate for DQ and DQS signals are measured with the output driven into a 50ohm load. For LPDDR5, termination is to VSS.
2. For LPDDR5, measured between 0.2*VOH and 0.8*VOH.
3. The differential slew rate is measured at the CPU pin between DQS_H – DQS_L ±10%*VDDQ for rising and falling edges.
4. Slew rate for command and address signals are measured with the output driven into a 50ohm load. For LPDDR5, termination is to VSS.
5. For LPDDR5, measured between 0.2*VOH and 0.8*VOH.
6. Measured with driver output resistance Rout=40 ohms for DQ/DQS.
7. Measured with driver output resistance Rout=40 ohms for command and address.
8. For BP_MEMREST_L, SEC driver is set to maximum strength and slew rate will depends on board level loading. Some overshoot is possible. If customer configuration is lightly loaded on BP_MEMRESET_L, customer needs to put loading cap to avoid overshoot and meets < 1usec slew rate spec

8.2.2.2 LPDDR4X Output Parameters

Table 8-25 LPDDR4X DC Output Parameters

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
SE, DIFF pull-up output driver characteristics, with ZQ calibration: VOHPU,nom = VDDQ*0.5	VOH,nom	mV		300		1, 2
	VOHPU,nom	VOH,nom	0.9	1.0	1.1	1, 2
SE, DIFF pull-up output driver characteristics, with ZQ calibration: VOHPU,nom = VDDQ*0.6	VOH,nom	mV		360		1, 2
	VOHPU,nom	VOH,nom	0.9	1.0	1.1	1, 2

Table Notes:

1. All values are after ZQ Calibration. Without ZQ Calibration VOH,nom values are ± 30%
2. VOH,nom (mV) values are based on a nominal VDDQ = 0.6V

Table 8-26 LPDDR4X Output Slew Rates Versus Data Rate (in MT/s)

			2400		2667		3200		4267		
Parameter	Symbol	Units	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Output slew rate: Single-ended signals	Sout-DQ	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	1,2,6,8
Output slew rate: Differential signals	Sout-DQ S	V/ns	6	16	6	16	6	16	6	16	1,3,6
Output slew rate: command and address	Sout-CA	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	2,4,5,7

Table Notes:

1. Slew rate for DQ and DQS signals are measured with the output driven into a 50ohm load. For LPDDR4X, termination is to VSS.
2. For LPDDR4X, measured between 0.2*VOH and 0.8*VOH
3. The differential slew rate is measured at the CPU pin between DQS_H – DQS_L ±10%*VDDQ for rising and falling edges.
4. Slew rate for command and address signals are measured with the output driven into a 50 ohm load. For LPDDR4X, termination is to VSS.
5. For LPDDR4X, measured between 0.2*VOH and 0.8*VOH
6. Measured with driver output resistance Rout=40 ohms for DQ/DQS.
7. Measured with driver output resistance Rout=40 ohms for command and address.
8. For BP_MEMRESET_L, SEC driver is set to maximum strength and slew rate will depends on board level loading. Some overshoot is possible. If customer configuration is lightly loaded on BP_MEMRESET_L, customer needs to put loading cap to avoid overshoot and meets < 1usec slew rate spec.

8.2.2.3 LPDDR4 Output Parameters

Table 8-27 LPDDR4 DC Output Parameters

Parameter	Symbol	Unit	Minimum	Typical	Maximum	Notes
SE, DIFF pull-up output driver characteristics, with ZQ calibration: VOHPU,nom = VDDQ_DRAM/2.5	VOH,nom	mV		440		1
	VOHPU,nom	VOH,nom	0.9	1.0	1.1	
SE, DIFF pull-up output driver characteristics, with ZQ calibration: VOHPU,nom = VDDQ_DRAM/3	VOH,nom	mV		367		
	VOHPU,nom	VOH,nom	0.9	1.0	1.1	

Table Notes:

1. All values are after ZQ Calibration. Without ZQ Calibration VOH,nom values are ± 30%
2. VOH,nom (mV) values are based on a nominal VDDQ_DRAM = 1.1V

Table 8-28 LPDDR4 Output Slew Rates Versus Data Rate (in MT/s)

			2400		2667		3200		4267		
Parameter	Symbol	Units	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Output slew rate: Single-ended signals	Sout-DQ	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	1,2,6,8
Output slew rate: Differential signals	Sout-DQS	V/ns	6	16	6	16	6	16	6	16	1,3,6
Output slew rate: command and address	Sout-CA	V/ns	3.5	8	3.5	8	3.5	8	3.5	8	2,4,5,7

Table Notes:

1. Slew rate for DQ and DQS signals are measured with the output driven into a 50ohm load. For LPDDR4, termination is to VSS.
2. For LPDDR4, measured between 0.2*VOH and 0.8*VOH
3. The differential slew rate is measured at the CPU pin between DQS_H – DQS_L ±10%*VDDQ for rising and falling edges.
4. Slew rate for command and address signals are measured with the output driven into a 50 ohm load. for LPDDR4, termination is to VSS.
5. For LPDDR4, measured between 0.2*VOH and 0.8*VOH
6. Measured with driver output resistance Rout=40 ohms for DQ/DQS.
7. Measured with driver output resistance Rout=40 ohms for command and address.

8. For BP_MEMRESET_L, SEC driver is set to maximum strength and slew rate will depends on board level loading. Some overshoot is possible. If customer configuration is lightly loaded on BP_MEMRESET_L, customer needs to put loading cap to avoid overshoot and meets < 1usec slew rate spec.

8.2.3 PHY DQS2DQ Delay Drift

Table 8-29 LPDDR5 DQS2DQ Delay Drift

Parameter	Symbol	Maximum	Units
PHY DQ to DQS delay offset temperature variation	tPHY_DQS2DQ_temp	0.184	ps/°C
PHY DQ to DQS delay offset VDD variation	tPHY_DQS2DQ_VDD	0.590	ps/mV

Table 8-30 LPDDR4X DQS2DQ Delay Drift

Parameter	Symbol	Maximum	Units
PHY DQ to DQS delay offset temperature variation	tPHY_DQS2DQ_temp	0.179	ps/°C
PHY DQ to DQS delay offset VDD variation	tPHY_DQS2DQ_VDD	0.593	ps/mV

Table 8-31 LPDDR4 DQS2DQ Delay Drift

Parameter	Symbol	Maximum	Units
PHY DQ to DQS delay offset temperature variation	tPHY_DQS2DQ_temp	0.167	ps/°C
PHY DQ to DQS delay offset VDD variation	tPHY_DQS2DQ_VDD	0.604	ps/mV

8.3 Input Reference Clock Specification

8.3.1 PLL Locked Mode

Table 8-32 PLL Locked Mode

Parameter	Minimum	Maximum	Units
DFI Input Frequency (PLL Locked)	167.67	1066.75	MHz
DFIclk Duty Cycle	40	60	%

8.3.2 PLL Bypass Mode

Table 8-33 PLL Bypass Mode

Parameter	Minimum	Maximum	Units
DFI Input Frequency	12.50	166.67	MHz
PCLK input	50	667	MHz
DFIclk Duty Cycle	40	60	%

8.3.3 Spread Spectrum Clock Modulation

The PLL, internal to the MASTER, supports spread spectrum clock generation (SSCG) using a down spreading profiles. The frequency deviation or modulation factor, δ, is defined to be:

$$\delta = -\Delta f/F_{DFIclk} \text{ x } 100\%$$

For down spreading, the minimum DFIclk frequency is defined to be:

$$F_{DFIclk}\,(min) = (1-\delta) \text{ x } F_{DFIclk}$$

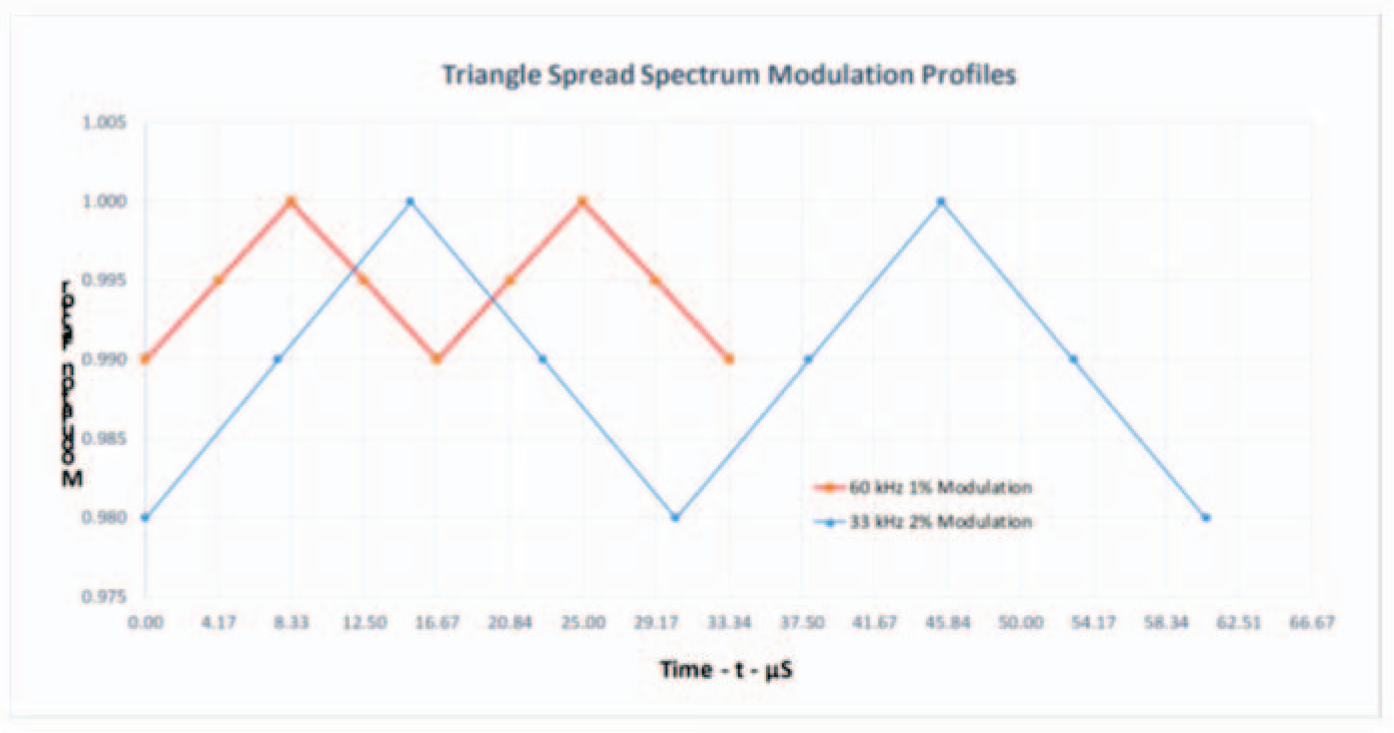
The following table provides the allowed input reference clock modulation that the PLL can support on DFIclk. If SSCG is used the user should make sure timing closure of the PUB accounts for this variation.

Table 8-34 Spread Spectrum Clock Modulation

Parameter	Value	Description
Spreading Type	Down Spreading	
Spreading Profiles	Triangle Hershey Kiss	
Percentage Spread and Rate of Change	-2% to 0% @ 33 kHz	0.98 x FDFIclk to 1.00 x FDFIck, Equivalent to 7.58 µS/%?DFIclk Frequency
	-1% to 0% @ 60 kHz	0.99 x FDFIclk to 1.00 x FDFIck, Equivalent to 8.33 µS/%?DFIclk Frequency

The Example of Triangular Modulation Profiles is an example of two different triangular spread-spectrum clock modulation that could be used.

Figure 8-3 Example of Triangular Modulation Profiles



8.3.4 Input Clock Jitter

The input reference clock to the PLL is driven by the DfiClk input clock to the PHY. The input reference clock (DfiClk) is specified through its impact on N-cycle jitter (timing error accumulated over N cycles) of the PLL's output clock Pclk.

The PHY PLL multiplies DfiClk by 4 to generate Pclk at the desired DDR rate (for example, for DDR 3200 DfiClk is 800MHz and Pclk is 3200MHz). Pclk is then used to generate the PHY MEMCLK output to the DRAM. The quality of the MEMCLK output depends on the DfiClk noise (Rj), SOC clock tree noise (Dj), PHY PLL noise (Rj), PHY clock tree noise (Dj) and IO noise (SSO).

In order to meet N-cycle jitter requirements at the MEMCLK output, the random jitter (Rj) at the PHY PLL DfiClk input, after being filtered by the 2nd order PHY PLL transfer function with a 3MHz bandwidth, must be such that the N-cycle jitter on the PLL output is limited by:

- JN(Pclk) = Pclk N-Cycle Jitter <= 0.06bits/DDRATE*(N/50), for any N between 2 and 50

Units of Pclk N-cycle jitter are in seconds with a DATARATE in bits/second. To be technically precise, the units of the pre-factor are therefore bits.

The Pclk N-cycle jitter derives from the PLL input DfiClk phase noise QRefClk(s) filtered by two transfer functions, HPLL(s), the PLL transfer function, and HN(s), the N-cycle jitter transfer function. Mathematically:

$$\Theta_N(s) = H_{PLL}(s)H_N(s)\Theta_{RefClk}(s)$$

Note The DfiClk is used for most of the logic in the PUB in addition to the PLL Input Reference Clock. The requirement outlined in this section is related to the DfiClk input path to the MASTER HardIP and the internal PLL. The other logic in the PUB, also driven by the DfiClk, may be subject to separate margining requirements as determined by the overall SoC requirements.

8.3.4.1 PHY PLL Transfer Function

The PHY PLL transfer function HPLL(s) shapes the RefClk phase noise and jitter and has a significant impact on the quality of the MEMCLK output. The PHY PLL is a type II second order system with a 3MHz loop filter bandwidth. The classic transfer function is given by:

$$H_{PLL}(s) = \frac{2z\omega_n s + \omega_n^2}{s^2 + 2z\omega_n s + \omega_n^2}$$

where z is the damping factor and ωn is the natural angular frequency related to the 3dB bandwidth by the following equation

$$\omega = \frac{2\pi f_{3dB}}{\sqrt{a + \sqrt{(a^2 + 1)}}}$$

and

$$a - 2z^2 + 1$$

8.3.4.2 N-Cycle Jitter Transfer Function

The low-pass nature of the PHY PLL cleans up the reference clock and minimizes its impact to MEMCLK jitter for low values of N. For high values of N, the attenuation from the PHY PLL will be smaller and the RefClk contributions will be a larger fraction of the N-cycle jitter.

The reference clock specification for N-cycle jitter must take into account the filtering of the PHY PLL and allocate to the reference clock a portion of the budget that increases with N (accumulated cycles).

The math for filtering jitter in order to find its contribution to the MEMCLK N-cycle jitter is given by

$$H(s) = (1 - e^{-2sNT_{CK}})$$

where TCK is the MEMCLK period (2UI, e.g. DDR3200 => 2/3200e6).

After filtering the peak to peak value of the MEMCLK accumulated jitter JCK(N) can be calculated by integrating the Rj terms over all noise frequencies s to achieve the RMS value and multiplying it by the desired BER scale factor.

8.3.4.3 Power Supply Injected Jitter (PSIJ)

In DDR systems deterministic jitter (Dj) is introduced through the power supply. It appears as an unwanted variation in delay as a function of power supply voltage variation. It is usually evaluated as a power supply sensitivity and quoted in ps/mV. By developing the sensitivity model for a given circuit configuration, knowing the power supply ripple on-chip allows the evaluation of the jitter contribution. PSIJ is almost always dominated by a single frequency, such as an SOC processor frequency. The peak to peak ripple of the power supply noise will result in peak to peak jitter contributions from components of the clock path. A pessimistic estimate of cascaded clock path sections would be to add the peak numbers directly by assuming the peak voltages are correlated at all locations across the power distribution network. Once the deterministic jitter components have been determined, they can be added as an RMS contribution to the other N-cycle jitter numbers since these contributions are not correlated.

8.4 EM Conditions

Table 8-35 EM Conditions

Parameter	Value	Value	Value
Lifetime (Operating Hours)	87,600	87,600	87,600
Process Corner	FF	FF	FF
Extraction Corner	typical	typical	typical
Temperature (base in °C)	105	105	105
Temperature (self-heating in °C)	<=5 [*]	<= 5 [*]	<= 5 [*]
Protocol	LPDDR5	LPDDR4x	LPDDR4
Operating Frequency (Mbps)	6400	4267	4267
Operating Voltage, VDD (V)	0.8925	0.8925	0.8925
Operating Voltage, VDDQ (V)	0.57	0.65	VDD
Operating Profile	50% read, 30% write, 20% idle	50% read, 30% write, 20% idle	50% read, 30% write, 20% idle
DRM Specification	TN07CLDR001_1_3.pdf	TN07CLDR001_1_3.pdf	TN07CLDR001_1_3.pdf

Table Notes:

1. Excursions allowed if wires at base and local self-heating temperature meet EM limits.

8.5 Build-It-Yourself ESD Protection

The PHY hard-macros contain no ESD protection clamp on any of the power supplies. The ESD protection clamps are required to be added and placed by customers. Detailed information regarding ESD clamp placement is available in the *LPDDR5/4/4x PHY Implementation Guide, Chapter Floorplanning, section IP Components, subsection ESD*. The following ESD clamps for VDDQ, VDD2H, and VAA_VDD2H supply are provided:

- dwc_ddrphy_clamp_dbyte10_<orientation>
- dwc_ddrphy_clamp_dbyte11_<orientation>
- dwc_ddrphy_clamp_dbyte12_<orientation>
- dwc_ddrphy_clamp_dbyte13_<orientation>
- dwc_ddrphy_clamp_ac2r_<orientation>
- dwc_ddrphy_clamp_ac1r_<orientation>
- dwc_ddrphy_clamp_master_<orientation>
- dwc_ddrphy_vaaclamp_master_<orientation>

These cells can be found inside the utility_blocks library provide with the PHY.

Note The PHY contains no ESD protection clamp on VDD supply. Customers are responsible for the proper amount of ESD protection on the VDD supply.

8.5.1 Human Body Model

The following table lists the expected human body model (HBM) performance. This model is the most common mechanism for characterizing an ESD event: The charged human body is modeled by a 100pF capacitor and a 1,500 ohms discharging resistance (MIL-STD-883G). The discharge itself is a double exponential waveform with a rise time of 2-10ns and a pulse duration of approximately 150ns (JESD625-A).

Table 8-36 Human Body Model (HBM)

Voltage Level	Category	Standard
+/-2kV	Class 2	JS-001-2017

8.5.2 Machine Model

Machine model qualification is not supported, as per recommendations in standard JEP155A.01.

8.5.3 Charged Device Model

The following table lists the expected charged device model (CDM) performance. This model is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

Note The CDM withstand voltage is highly dependent on the device package, whereas CDM withstand current is a more constant parameter. Therefore, we specify the CDM protection level as a current. The CDM protection voltage will vary by SOC package design.

Table 8-37 Charged Device Model (CDM)

Minimum Protection Level	JEDEC Class	Standard
±6A	Class C1	JS-002-2018

8.5.4 Latch-up

The following table lists the expected latch-up performance. This model attempts to induce a state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.

Table 8-38 Latch-up

Current Stress	Temperature	JEDEC Class	Standard
±100mA	125 deg C	Class II	JESD78E

8.6 Power Supply Capacitance

The following tables provide the effective series resistance / effective series capacitance (ESR / ESC) for:

- The UTILITY CELL library decoupling capacitance (DECAP) cells (also known as SNAPCAPS) and
- The hard IP blocks

Depending on the construction of the PHY, the SOC, the package, and the power delivery system, customers will need to provide enough capacitance to keep supply ringing below the PHY specification requirements. Customers can place as many instances of these cells, following the requirements of the Implementation Guide, to meet their supply decoupling requirements.The PHY contains no substantial decoupling on the VDD supply. Customers are responsible for adding their own VDD decap of sufficient quantity to meet noise limits.

Table 8-39 VDDQ-VSS Effective Capacitance and Series Resistance for Utility and Hard IP Blocks

	VDDQ-VSS DECAP (VDDQ=0.5V)						
	SS 125		TT 25		FF -40		
Cells	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Notes
dwc_ddrphyse_top_ns	7.024	1.695	6.366	1.505	4.055	1.383	
dwc_ddrphydiff_top_ns	3.818	3.296	3.558	2.930	4.394	2.689	
dwc_ddrphymaster_top_ns	1.562	23.804	1.191	25.626	0.913	27.703	
dwc_ddrphy_decapvddq_4x1_ns	0.026	52.600	0.026	58.600	0.026	64.900	2
dwc_ddrphy_decapvddq_1x1_ns	0.110	12.200	0.110	13.600	0.110	15.000	2
dwc_ddrphy_decapvddq_1by4x1_ns	0.600	2.100	0.600	2.400	0.600	2.600	2
dwc_ddrphy_decapvddqhd_4x1_ns	0.030	127.000	0.030	140.000	0.030	153.700	1
dwc_ddrphy_decapvddqhd_1x1_ns	0.140	29.600	0.140	32.700	0.140	35.800	1
dwc_ddrphy_decapvddqhd_1by4x1_ns	0.910	4.600	0.880	5.000	0.850	5.500	1
dwc_ddrphyse_top_ew	8.01	1.67	7.38	1.47	4.78	1.34	
dwc_ddrphydiff_top_ew	3.86	3.25	3.52	2.88	4.38	2.64	
dwc_ddrphymaster_top_ew	0.78	25.34	0.60	27.25	0.48	29.51	
dwc_ddrphy_decapvddq_4x1_ew	0.03	52.06	0.02	57.78	0.02	63.89	2
dwc_ddrphy_decapvddq_1x1_ew	0.11	12.59	0.11	13.96	0.11	15.44	2
dwc_ddrphy_decapvddq_1by4x1_ew	0.32	3.71	0.33	4.11	0.34	4.55	2
dwc_ddrphy_decapvddqhd_4x1_ew	0.03	123.84	0.03	136.38	0.03	149.12	1
dwc_ddrphy_decapvddqhd_1x1_ew	0.13	29.39	0.13	32.39	0.13	35.43	1
dwc_ddrphy_decapvddqhd_1by4x1_ew	0.43	8.69	0.43	9.57	0.44	10.47	1

	VDDQ-VSS DECAP (VDDQ=0.5V)						
	SS 125		TT 25		FF -40		
Cells	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Notes
dwc_ddrphy_clamp_dbyte10_ns	0.06	275.51	0.05	300.84	0.05	327.02	
dwc_ddrphy_clamp_dbyte11_ns	0.05	311.69	0.04	340.76	0.04	370.72	
dwc_ddrphy_clamp_dbyte12_ns	0.04	400.57	0.03	438.92	0.03	478.31	
dwc_ddrphy_clamp_dbyte13_ns	0.03	436.75	0.03	478.83	0.03	522.00	
dwc_ddrphy_clamp_ac1r_ns	0.15	150.22	0.12	162.55	0.11	175.53	
dwc_ddrphy_clamp_ac2r_ns	0.06	266.63	0.05	291.22	0.05	316.44	
dwc_ddrphy_clamp_master_ns	0.08	141.50	0.06	154.08	0.05	167.15	
dwc_ddrphy_endcell_ns	0.38	13.35	0.37	14.75	0.37	16.20	
dwc_ddrphy_clamp_dbyte10_ew	0.06	268.00	0.05	293.00	0.05	318.00	
dwc_ddrphy_clamp_dbyte11_ew	0.04	320.00	0.04	349.00	0.04	380.00	
dwc_ddrphy_clamp_dbyte12_ew	0.04	390.00	0.03	427.00	0.03	465.00	
dwc_ddrphy_clamp_dbyte13_ew	0.03	441.00	0.02	483.00	0.02	527.00	
dwc_ddrphy_clamp_ac1r_ew	0.14	146.09	0.12	157.93	0.11	170.41	
dwc_ddrphy_clamp_ac2r_ew	0.06	261.60	0.05	285.43	0.05	310.06	
dwc_ddrphy_clamp_master_ew	0.13	137.58	0.11	149.66	0.10	162.23	
dwc_ddrphy_endcell_ew	0.15	29.57	0.15	32.76	0.15	36.07	

Table Notes

1. Core devices are used in this DECAP cell to increase capacitance per unit area at low supply voltage levels. These DECAP cells enable users to make right trade-off area/capacitance versus leakage for the LPDDR54 PHY. Refer to Table 8-40 for HD DECAP leakage currents.
2. All non-HD DECAP cells use IO devices and will leak < 1nA across corners.

Table 8-40 VDDQ Leakage Current for HD DECAP Cells

	VDDQ Leakage (uA)					
	LPDDR5 mode		LPDDR4X mode		LPDDR4 mode	
Cells	TT 0.5V 25C	FF 0.57V 125C	TT 0.6V 25C	FF 0.65V 125C	TT 0.75V 25C	FF 0.7875V 125C
dwc_ddrphy_decapvddqhd_4x1_ns	1.371	8.357	3.21	15.57	9.349	39.27
dwc_ddrphy_decapvddqhd_1x1_ns	0.3201	1.951	0.7495	3.634	2.182	9.168

Cells	VDDQ Leakage (uA)					
	LPDDR5 mode		LPDDR4X mode		LPDDR4 mode	
	TT 0.5V 25C	FF 0.57V 125C	TT 0.6V 25C	FF 0.65V 125C	TT 0.75V 25C	FF 0.7875V 125C
dwc_ddrphy_decapvddqhd_1by4x1_ns	0.05494	0.3349	0.1286	0.6238	0.3746	1.574
dwc_ddrphy_decapvddqhd_4x1_ew	1.324	8.068	3.099	15.03	9.025	37.91
dwc_ddrphy_decapvddqhd_1x1_ew	0.3157	1.924	0.7392	3.584	2.152	9.042
dwc_ddrphy_decapvddqhd_1by4x1_ew	0.09354	0.5701	0.219	1.062	0.6378	2.679

Table 8-41 VDD-VSS Effective Capacitance and Series Resistance for Utility and Hard IP Blocks

Cells	VDD-VSS DECAP (VDD = 0.75V)						Notes
	SS 125		TT 25		FF -40		
	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	
dwc_ddrphyse_top_ns	0.105	38.684	0.088	36.250	0.082	34.558	
dwc_ddrphysec_top_ns	0.052	53.120	0.045	49.970	0.042	47.969	
dwc_ddrphydiff_top_ns	0.072	84.510	0.090	79.541	0.133	76.409	
dwc_ddrphymaster_top_ns	0.008	428.724	0.007	407.803	0.006	396.301	
dwc_ddrphy_decapvdd_4x1_ns	0.030	54.000	0.030	60.000	0.030	66.500	2
dwc_ddrphy_decapvdd_1x1_ns	0.110	12.600	0.110	14.000	0.110	15.500	2
dwc_ddrphy_decapvdd_1by4x1_ns	0.600	2.200	0.600	2.400	0.600	2.700	2
dwc_ddrphy_decapvddhd_4x1_ns	0.040	137.000	0.040	149.600	0.040	162.400	1
dwc_ddrphy_decapvddhd_1x1_ns	0.160	32.000	0.170	35.000	0.180	38.000	1
dwc_ddrphy_decapvddhd_1by4x1_ns	0.940	5.500	0.950	6.000	1.000	6.500	1
dwc_ddrphyse_top_ew	0.114	38.946	0.097	36.478	0.091	34.759	
dwc_ddrphysec_top_ew	0.051	53.317	0.045	50.165	0.042	48.163	
dwc_ddrphydiff_top_ew	0.065	84.890	0.077	79.889	0.112	76.731	
dwc_ddrphymaster_top_ew	0.008	433.682	0.007	413.078	0.006	402.267	
dwc_ddrphy_decapvdd_4x1_ew	0.030	53.250	0.030	58.890	0.030	65.050	2
dwc_ddrphy_decapvdd_1x1_ew	0.110	12.930	0.110	14.290	0.110	15.770	2
dwc_ddrphy_decapvdd_1by4x1_ew	0.320	3.810	0.330	4.210	0.340	4.650	2
dwc_ddrphy_decapvddhd_4x1_ew	0.030	132.960	0.040	144.840	0.041	157.120	1

Cells	VDD-VSS DECAP (VDD = 0.75V)						Notes
	SS 125		TT 25		FF -40		
	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	
dwc_ddrphy_decapvddhd_1x1_ew	0.130	31.720	0.140	34.550	0.140	37.480	1
dwc_ddrphy_decapvddhd_1by4x1_ew	0.450	9.370	0.450	10.220	0.470	11.080	1
dwc_ddrphy_decap_ac1r_ns	0.04	167	0.04	183	0.04	198	
dwc_ddrphy_decap_ac2r_ns	0.05	136	0.05	148	0.05	161	
dwc_ddrphy_endcell_ns	0.13	11.4	0.13	12.6	0.12	13.9	
dwc_ddrphy_decap_ac1r_ew	0.04	163	0.04	177	0.04	193	
dwc_ddrphy_decap_ac2r_ew	0.05	131	0.05	143	0.05	156	
dwc_ddrphy_endcell_ew	0.09	13.24	0.1	14.63	0.1	16.16	

Table Notes

1. Core devices are used in this DECAP cell to increase capacitance per unit area at low supply voltage levels. These DECAP cells enable users to make right trade-off area/capacitance versus leakage for the LPDDR54 PHY. Refer to Table 8-42 for HD DECAP leakage currents.
2. All non-HD DECAP cells use IO devices and will leak < 1nA across corners.

Table 8-42 VDD Leakage Current for cells using HD DECAP

Cells	VDD Leakage (uA)	
	TT 0.75V 25C	FF 0.7875V 125C
dwc_ddrphy_decapvddhd_4x1_ns	9.349	39.27
dwc_ddrphy_decapvddhd_1x1_ns	2.182	9.168
dwc_ddrphy_decapvddhd_1by4x1_ns	0.3746	1.574
dwc_ddrphy_decapvddhd_4x1_ew	9.025	37.91
dwc_ddrphy_decapvddhd_1x1_ew	2.152	9.042
dwc_ddrphy_decapvddhd_1by4x1_ew	0.6378	2.679

Table 8-43 VDD2H-VSS Effective Capacitance and Series Resistance for Utility and Hard IP Blocks

	VDD2H-VSS DECAP (VDD2H = 1.05V)					
	SS 125		TT 25		FF -40	
Cells	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)
dwc_ddrphysec_top_ns	0.53	8.65	0.33	9.28	0.24	10.03
dwc_ddrphymaster_top_ns	1.28	36.72	1.03	39.70	0.83	43.01
dwc_ddrphy_decapvdd2_4x1_ns	0.03	55.50	0.03	61.40	0.03	67.80
dwc_ddrphy_decapvdd2_1x1_ns	0.12	12.90	0.11	14.20	0.11	15.70
dwc_ddrphy_decapvdd2_1by4x1_ns	0.65	2.20	0.63	2.50	0.63	2.70
dwc_ddrphysec_top_ew	0.40	10.90	0.25	11.71	0.17	12.68
dwc_ddrphymaster_top_ew	0.83	41.04	0.67	44.32	0.56	48.05
dwc_ddrphy_decapvdd2_4x1_ew	0.03	54.19	0.03	59.89	0.03	66.17
dwc_ddrphy_decapvdd2_1x1_ew	0.11	13.15	0.11	14.53	0.11	16.04
dwc_ddrphy_decapvdd2_1by4x1_ew	0.33	3.87	0.34	4.28	0.35	4.72
dwc_ddrphy_clamp_ac1r_ns	6.78	8.44	7.70	8.50	8.36	8.62
dwc_ddrphy_clamp_ac2r_ns	6.51	8.58	7.41	8.64	8.06	8.75
dwc_ddrphy_clamp_master_ns	6.42	8.73	7.30	8.80	7.90	8.93
dwc_ddrphy_decap_ac1r_ns	0.03	67.00	0.03	75.00	0.04	83.00
dwc_ddrphy_decap_ac2r_ns	0.03	109.00	0.02	121.00	0.02	134.00
dwc_ddrphy_decap_master_ns	0.01	113.00	0.01	125.00	0.01	138.00
dwc_ddrphy_clamp_ac1r_ew	8.18	7.89	9.32	7.96	10.12	8.08
dwc_ddrphy_clamp_ac2r_ew	7.73	8.09	8.84	8.15	9.62	8.28
dwc_ddrphy_clamp_master_ew	7.60	8.18	8.67	8.25	9.43	8.37
dwc_ddrphy_decap_ac1r_ew	0.04	65.00	0.04	72.00	0.04	80.28
dwc_ddrphy_decap_ac2r_ew	0.02	105.30	0.02	116.70	0.02	129.26
dwc_ddrphy_decap_master_ew	0.02	105.27	0.02	116.67	0.02	129.23

Table 8-44 VAA_VDD2H-VSS Effective Capacitance and Series Resistance for Utility and Hard IP Blocks

	VAA_VDD2H-VSS DECAP (VAA_VDD2H=1.05V - 1.8V)					
	SS 125		TT 25		FF -40	
Cells[1]	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)	Rdie (Ohm)	Cdie (pF)
dwc_ddrphy_vaaclamp_master_ns	8.510	7.620	7.760	7.700	7.580	7.790
dwc_ddrphymaster_top_ns	9.887	7.115	8.950	7.214	8.600	7.314
dwc_ddrphy_vaaclamp_master_ew	11.910	6.800	11.410	6.880	11.440	6.990
dwc_ddrphymaster_top_ew	11.225	6.316	13.118	6.389	14.113	6.538

[1] VAA_VDD2H decoupling exists only in dwc_ddrphymaster_top

8.7 Power Consumption: PHY Compiler

The power consumption of a DDR PHY is a complex function of numerous parameters: supply voltage, process corner, temperature, data rate, hard IP instance count, DDR mode, DRAM loading, signal loading, data activity, among others. As such, power cannot be summarized in a simple set of tables.

Instead, Synopsys provides an online tool called PHY Compiler for power analysis. PHY Compiler contains a set of check boxes and drop-down menus to configure the PHY for the SOC use condition. PHY Compiler then calls a script that combines the power for each PHY sub-component based on the configuration. The script uses underlying data created through SPICE simulations and digital power analysis tools for the particular condition.

Note PHY Compiler is available on the Synopsys website: https://www.synopsys.com/dw/ddrphy.php

Because of the extensive data set required to predict power, PHY Compiler limits the process, voltage, temperature conditions.

- Typical process, nominal or boost voltage per databook specifications, 25C
- Fast process, max nominal or max boost voltage per databook specifications, 125C

Future enhancements may extend these conditions.

8.7.1 PHY Compiler Output

PHY Compiler will produce a set of tables listing average power consumed during different modes of operation or power states.

- Continuous read bursts
- Continuous write bursts
- Idle, where the PHY is fully active, waiting for the next command
- DFI_LP_DATA
- DFI_LP = DFI_LPDATA + DFI_LPCTRL + DRAMCLKSTOP (as described in the PUB databook)
- LP2 (described in the PUB databook)
- LP3 (described in the PUB databook)

In addition, power is broken out per supply. PHY Compiler also contains an option enabling it to break out power for each hard IP unit in a given configuration.

An example is shown in the following table. This table does not necessarily provide an accurate representation for this product. Please consult PHY Compiler to obtain more accurate power values.

Table 8-45 LPDDR5, 6400Mbps, 32 bit PHY, 2 channel, 1 Ranks, TT Transistors, 25C, with DMI

Rail	Voltage (V)	Read Power (mW)	Write Power (mW)	Idle Power (mW)	DFI_LP_DATA Power (mW)	DFI_LP Power (mW)	LP2 Power (mW)	LP3 Power (mW)
VDD	0.75	258.79	303.79	119.11	62.65	6.52	0.65	0

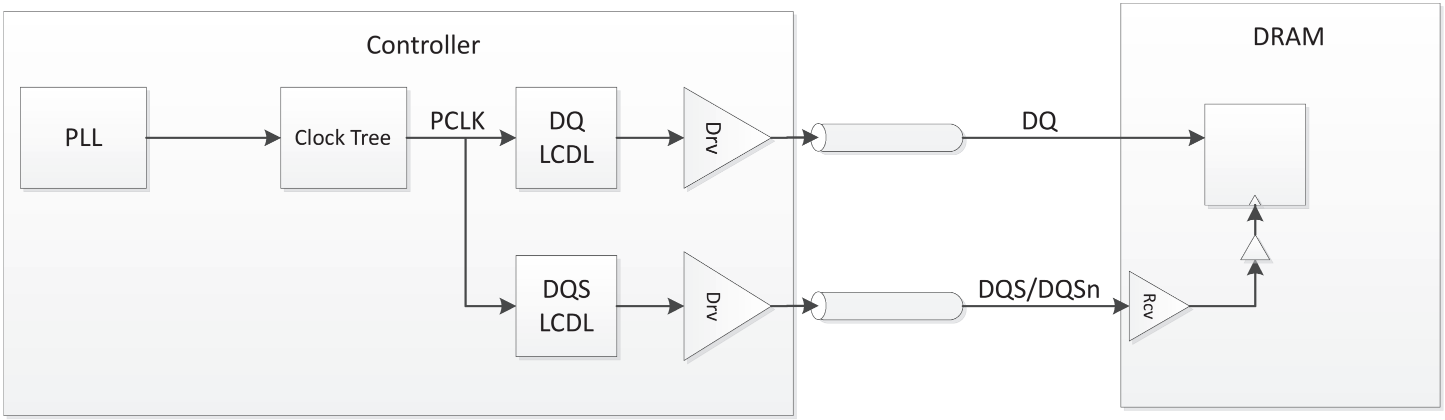
Rail	Voltage (V)	Read Power (mW)	Write Power (mW)	Idle Power (mW)	DFI_LP_DATA Power (mW)	DFI_LP Power (mW)	LP2 Power (mW)	LP3 Power (mW)
VDDQ	0.5	23.61	92.95	3.84	3.84	0.46	0.03	0
VDD2H	1.05	14.95	14.95	7.55	7.55	7.55	0	0
Total Power		297.35	411.69	130.5	74.04	14.53	0.68	0
Exit Latency		N/A	N/A	None	2 DFICLK	4 DFICLK	3µs + Retraining time	LP2 exit + 10µS (PLL pwron)

8.7.2 How Power is Calculated

For a fully contained system, power is calculated through the standard equation P = I * V. For a system with interconnected components, such as the DDR PHY plus DRAMs, power for off-chip signaling can be included in numerous ways.

Synopsys has chosen to calculate power as voltage multiplied by the current consumed for each input supply to the PHY. For a given VDDx, this can be thought of as VDDx multiplied by the current sourced by VDDx into the PHY. This enables power to the PHY to be measured through a test system and directly compared to our reported power.

Figure 8-4 Example for the VDDQ Supply



The figure shows an example for the VDDQ supply, which sources current through the current meter I(VDDQ) to the PHY output driver, termination, and internal circuits. Even though some part of the current may ultimately be dissipated outside of the PHY, we still calculate power as:

P = VDDQ * I(VDDQ)

Note that power calculated in this way is distinctly different from power for other purposes.

- It is not power dissipated in the PHY and is therefore not appropriate for thermal calculations.
- It may or may not match the power methodology for other system components. Calculating the power of the full PHY plus DRAM system will require computing power for other components in a similar manner as for the PHY.

9 Integrated I/O Functionality

This chapter discusses the following topics concerning the Synopsys LPDDR5/4/4x PHY Integrated I/O functionality:

9.1 Integrated I/O Functionality Overview

Based on the JEDEC specifications for LPDDR4/LPDDR4X/LPDDR5 SDRAMs, the DWC LPDDR5/4/4x PHY's I/O elements include PVT compensated on-die termination (ODT) and output impedance.

Note The I/O cells are integrated in the DWC LPDDR5/4/4X PHY hard macros.

9.1.1 Key Features

The DWC LPDDR5/4/4X PHY's SSTL I/O includes the following features:

- LPDDR4, LPDDR4X and LPDDR5 operation
- Compatible with JEDEC standard LPDDR4/LPDDR4X/LPDDR5 SDRAMs
- Programmable input termination (ODT)
- Programmable output impedance
- Slew rate control
- PVT-compensated ODT and output impedance
- Receiver power-down control
- Embedded boundary scan support logic
- PAD and internal loopback modes
- Supports flip chip packaging

9.1.2 Cell List

The following Table shows the cell list for the I/Os

Table 9-1 I/O Cell List

Cell Name	Cell Function	Cell Location
dwc_ddrphy_pclk_master	CLK Distribution and CLK Macros PwrOkVDD Distribution	MASTER Hard-macro
dwc_ddrphy_pclk_rpt1ch		CLK Distribution
dwc_ddrphy_pclk_rpt2ch		
dwc_ddrphy_pclk_rx		SE/SEC/DIFF Hard-macro
dwc_ddrphy_zcalana	MASTER Macros	MASTER Hard-macro
dwc_ddrphy_por		
dwc_ddrphy_vrefdacref		
dwc_ddrphy_lcdl	Bit Slice Components	SE/SEC/DIFF Hard-macro
dwc_ddrphy_rxreplica		DIFF Hard-macro

Cell Name	Cell Function	Cell Location
dwc_ddrphy_se_io	DBYTE, AC	SE Hard-macro MASTER Hard-macro (Impedance Calibration)
dwc_ddrphy_diff_io		DIFF Hard-macro
dwc_ddrphy_sec_io		SEC Hard-macro

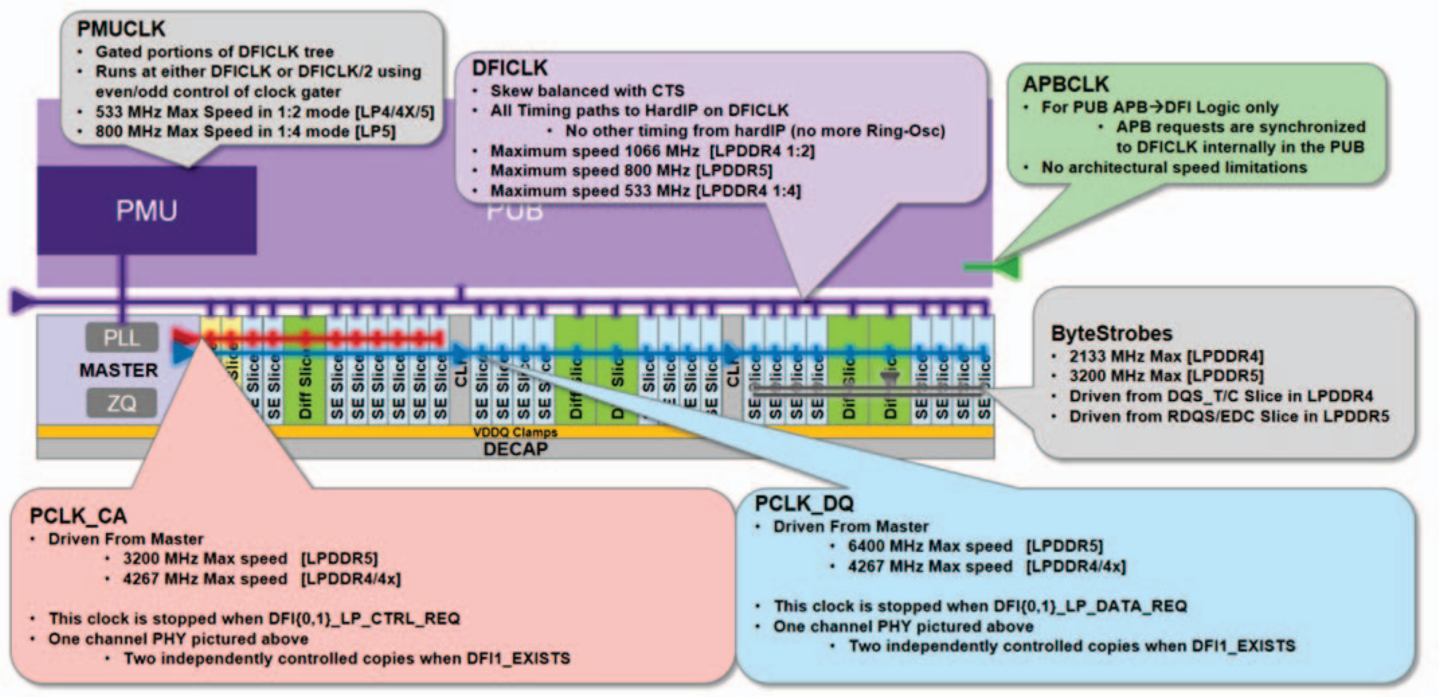
9.2 CLK Distribution and CLK Macros

The clock distribution macros span the entire DWC LPDDR5/4/4X PHY. The cells serve three main purposes:

1. Distribute the master PLL clock (Pclk) to all macros within the PHY
2. Ability to gate the clock from MASTER and SE/DIFF/SEC slices
3. Divide the clock to produce output clock of half frequency

An example recommended floorplan of the DWC LPDDR5/4/4X PHY clock distribution with the conceptual view of top-level Pclk distribution and clock signal names (see Figure 9-1).

Figure 9-1 PHY clock Distribution



PMUCLK
- Gated portions of DFICLK tree
- Runs at either DFICLK or DFICLK/2 using even/odd control of clock gater
- 533 MHz Max Speed in 1:2 mode [LP4/4X/5]
- 800 MHz Max Speed in 1:4 mode [LP5]

DFICLK
- Skew balanced with CTS
- All Timing paths to HardIP on DFICLK
  - No other timing from hardIP (no more Ring-Osc)
- Maximum speed 1066 MHz [LPDDR4 1:2]
- Maximum speed 800 MHz [LPDDR5]
- Maximum speed 533 MHz [LPDDR4 1:4]

APBCLK
- For PUB APB→DFI Logic only
  - APB requests are synchronized to DFICLK internally in the PUB
- No architectural speed limitations

ByteStrobes
- 2133 MHz Max [LPDDR4]
- 3200 MHz Max [LPDDR5]
- Driven from DQS_T/C Slice in LPDDR4
- Driven from RDQS/EDC Slice in LPDDR5

PCLK_CA
- Driven From Master
  - 3200 MHz Max speed [LPDDR5]
  - 4267 MHz Max speed [LPDDR4/4x]
- This clock is stopped when DFI{0,1}_LP_CTRL_REQ
- One channel PHY pictured above
  - Two independently controlled copies when DFI1_EXISTS

PCLK_DQ
- Driven From Master
  - 6400 MHz Max speed [LPDDR5]
  - 4267 MHz Max speed [LPDDR4/4x]
- This clock is stopped when DFI{0,1}_LP_DATA_REQ
- One channel PHY pictured above
  - Two independently controlled copies when DFI1_EXISTS

The clock tree distribution contains three cells which are stamped out through all macros in the PHY. The cells are: dwc_ddrphy_pclk_master, dwc_ddrphy_pclk_rx, and dwc_ddrphy_rpt[1/2]ch.

9.2.1 Logical Functionality

The clock signals are distributed by RDL driven from the master and received in each bit slice with the help of following macros:

- PCLK_MASTER: contains sync clock gater, clock divider and final driver (in MASTER)
- Repeater Blocks: contains clock buffer cells and PwrOkVDD buffer.
- PCLK_RX: contains async clock gater and atpg clock mux (in SE/SEC/DIFF slices)

9.2.1.1 PCLK_MASTER (dwc_ddrphy_pclk_master)

9.2.1.1.1 General Description

PCLK_MASTER cell receives Pclk signal from PLL and distributes to all macros in the PHY. The PCLK_MASTER macro has one input clock Pclk and 2 sets of 2 output clocks (2 channels). Suffix number 0/1 in the pin names in PCLK_MASTER represents channel 0/1.

- Pclk_Ca0/1 is used to clock Command-Address SE/SEC/DIFF slices
- Pclk_Dq0/1 is used to clock DQ/DQS SE/DIFF slices

There are two paths in the PCLK_MASTER to generate each output clock: one for clock gating and other for clock division.

The clock gater path:

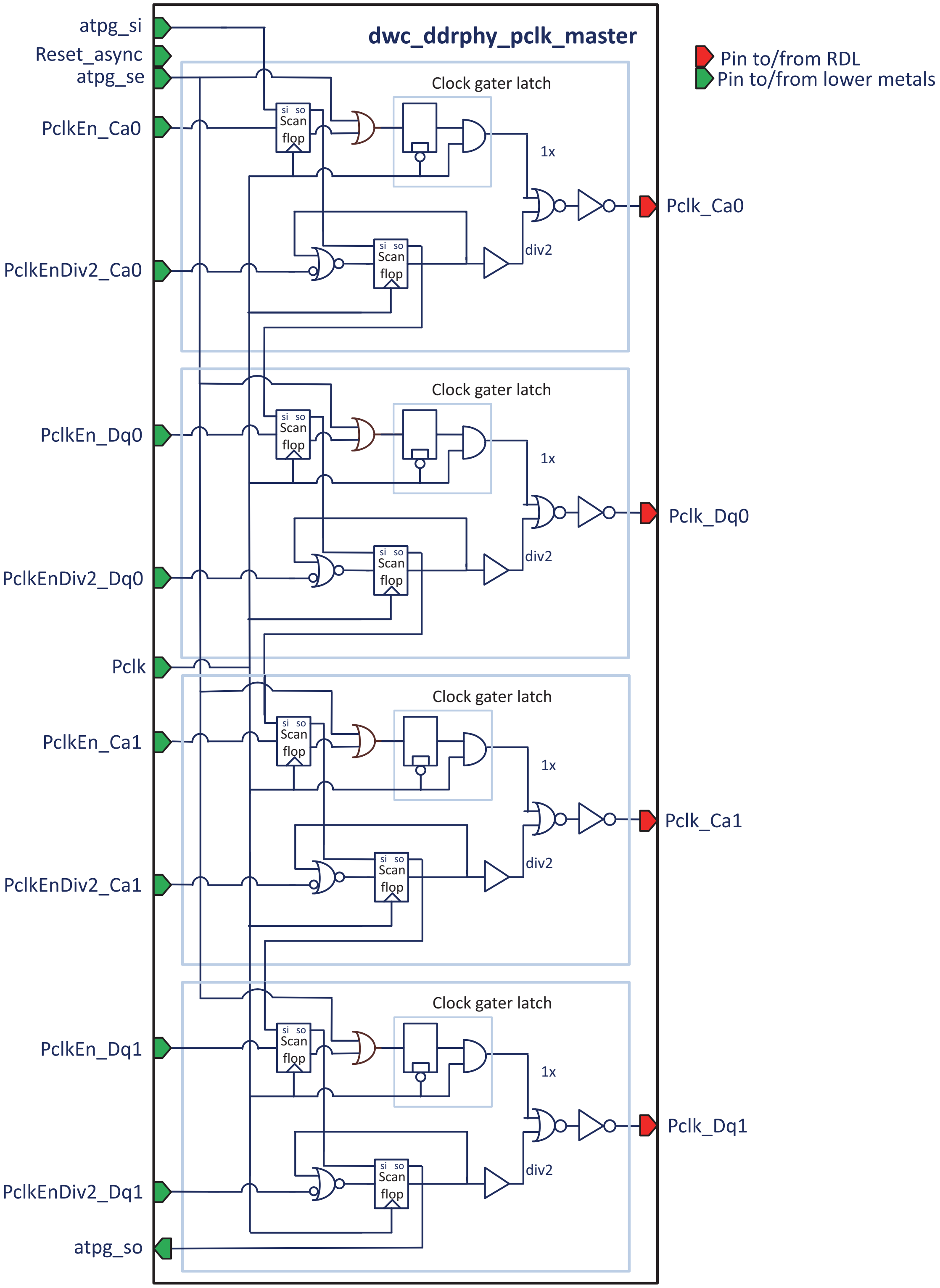
- 1x clock output (No clock division) when enabled
- A flop is added on the PclkEn to improve the IMPL timing
- The flop is atpg scan enabled
- An OR gate is added in the master for atpg mode control

The clock divider path:

- Generates a divide by 2 clock when enabled (div2 clock)
- The flop used is atpg scan enabled

The final stage in PCLK_MASTER combines the 1x and div2 clock with an OR gate (NOR + Inverter). The final inverter drives the clock into bit slices and clock repeater.

Figure 9-2 PCLK_MASTER Block Diagram



9.2.1.1.2 Pin List

The following table shows the pin list for the PCLK_MASTER cell.

Table 9-2 PCLK_Master Pin List

dwc_ddrphy_pclk_master				
Pin name	**Direction**	**Power Domain**	**Clock domain**	**Function**
VDD	Input	VDD	Async	Digital Logic Power Supply
VSS	Input	0	Async	Ground
Reset_async	Input	VDD	Async	Asynchronous reset input
Pclk	Input	VDD	Pclk	Pclk input
PclkEnDiv2_Ca0	Input	VDD	Pclk	CA/CK Pclk enable for divided clock (channel 0)
PclkEn_Ca0	Input	VDD	Pclk	CA/CK Pclk enable (channel 0)
Pclk_Ca0	Output	VDD	Pclk	Output Clk to CA/CK Slices (channel 0)
PclkEnDiv2_Dq0	Input	VDD	Pclk	Data Pclk enable for divided clock (channel 0)
PclkEn_Dq0	Input	VDD	Pclk	Data Pclk enable (channel 0)
Pclk_Dq0	Output	VDD	Pclk	Output Clk to DQ Slices (channel 0)
PclkEnDiv2_Ca1	Input	VDD	Pclk	CA/CK Pclk enable for divided clock (channel 1)
PclkEn_Ca1	Input	VDD	Pclk	CA/CK Pclk enable (channel 1)
Pclk_Ca1	Output	VDD	Pclk	Output Clk to CA/CK Slices (channel 1)
PclkEnDiv2_Dq1	Input	VDD	Pclk	Data Pclk enable for divided clock (channel 1)
PclkEn_Dq1	Input	VDD	Pclk	Data Pclk enable (channel 1)
Pclk_Dq1	Output	VDD	Pclk	Output Clk to DQ Slices (channel 1)
atpg_se	Input	VDD	atpg_DfiClk	Atpg mode/scan enable pin
atpg_si	Input	VDD	atpg_DfiClk	Atpg mode input
atpg_so	Output	VDD	atpg_DfiClk	Atpg mode output

9.2.1.2 Repeater Blocks

Clock repeater hard-macros are used to distribute high-speed clocks (PclkCa, PclkDq) across PHY. Two variants of repeater hard-macros are built to optimize power consumption and performance of clktree implementation:

- RPT1CH (dwc_ddrphy_rpt1ch)
- RPT2CH (dwc_ddrphy_rpt2ch)

The following table shows the pin list for Repeater Channel cells.

Table 9-3 Repeater Blocks

Pin name	Direction	Power Domain	Clock domain	Function
dwc_ddrphy_rpt1ch				
VDD	Input	VDD	Async	Digital Logic Power Supply
VDDQ	Input	VDDQ	Async	IO Power Supply
VSS	Input	0	Async	Ground
PclkIn0	Input	VDD	Pclk	Input0 of the rpt channel
PclkOut0	Output	VDD	Pclk	Buffered Pclk output0 of thr rpt channel
PwrOkVDDin	Input	VDD	Pclk	PwrOkVDD input of the rpt channel
PwrOkVDDout	Output	VDD	Pclk	Buffered PwrOkVDD output of the rpt channel
TieHigh	Output	VDD	Async	VDD tie high
Tielow	Output	VDD	Async	VDD tie low
dwc_ddrphy_rpt2ch				
VDD	Input	VDD	Async	Digital Logic Power Supply
VDDQ	Input	VDDQ	Async	IO Power Supply
VSS	Input	0	Async	Ground
PclkIn0	Input	VDD	Pclk	Input0 of the rpt channel
PclkOut0	Output	VDD	Pclk	Buffered Pclk output0 of thr rpt channel
PclkIn1	Input	VDD	Pclk	Input1 of the rpt channel
PclkOut1	Output	VDD	Pclk	Buffered Pclk output1 of thr rpt channel
PwrOkVDDin	Input	VDD	Pclk	PwrOkVDD input of the rpt channel
PwrOkVDDout	Output	VDD	Pclk	Buffered PwrOkVDD output of the rpt channel
TieHigh	Output	VDD	Async	VDD tie high
Tielow	Output	VDD	Async	VDD tie low

Figure 9-3 RPT1CH Block Diagram

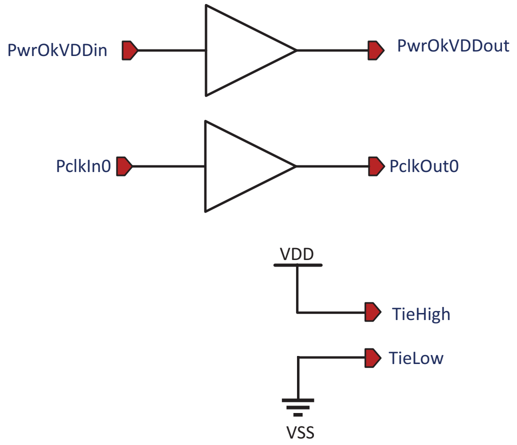
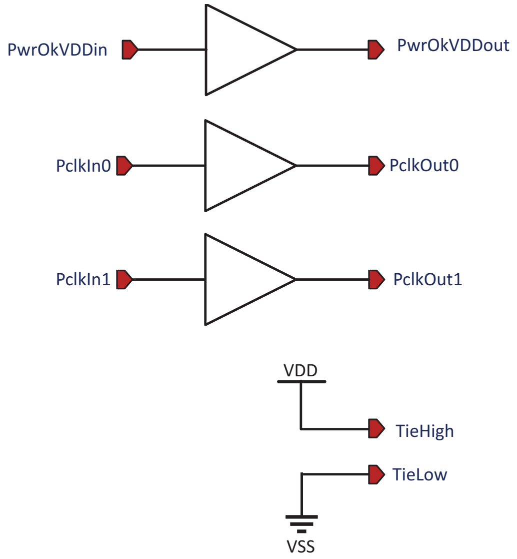


Figure 9-4 RPT2CH Block Diagram



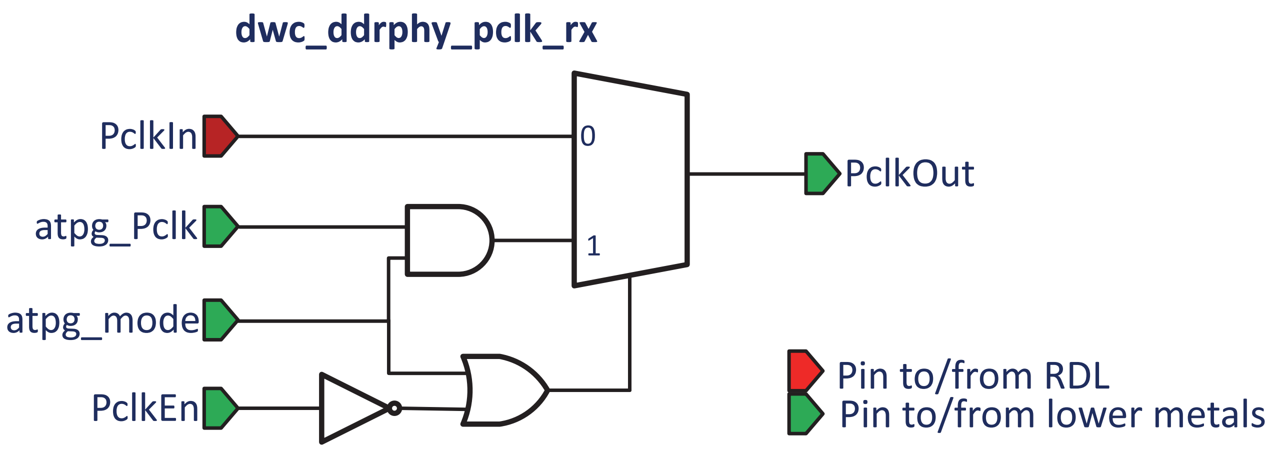
9.2.1.3 PCLK_RX (dwc_ddrphy_pclk_rx)

9.2.1.3.1 General Description

The Pclk signal is received by PCLK_RX clock receivers in SE/SEC/DIFF hard-macros. The PCLK_RX circuit-macro has:

- Option to asynchronously gate the Pclk signals for power saving
- ATPG clock mux included

Figure 9-5 dwc_ddrphy_pclk_rx Block Diagram



9.2.1.3.2 Pin List

The following table shows the pin list for PCLK_RX cell.

Table 9-4 PCLK_RX Pin List

dwc_ddrphy_pclk_rx				
Pin name	**Direction**	**Power Domain**	**Clock domain**	**Function**
VDD	Input	VDD	Async	Digital Logic Power Supply
VSS	Input	0	Async	Ground
PclkIn	Input	VDD	Pclk	Input Pclk from Master/Repeater
PclkEn	Input	VDD	Async	Pclk enable
PclkOut	Output	VDD	Pclk	Clock receiver output
atpg_mode	Input	VDD	atpg_DfiClk	Atpg mode enable
atpg_Pclk	Input	VDD	Pclk	Atpg mode clock

9.3 MASTER Macros

9.3.1 Analog Impedance Calibration Cell: ZCALANA (dwc_ddrphy_zcalana)

9.3.1.1 General Description

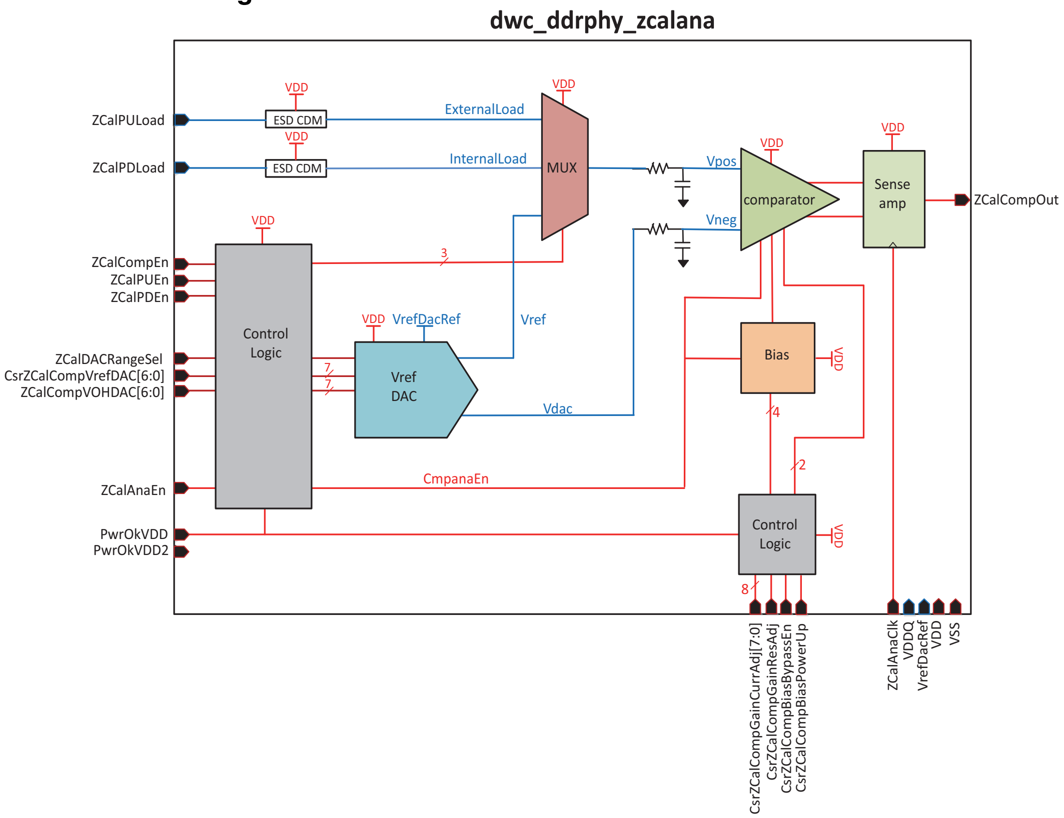
ZCALANA is an analog impedance calibration macro which has the analog circuits required to support pull-up and pull-down calibration. The macro generates a programmable voltage reference, multiplexes calibration nodes, provides analog filtering and contains a clocked comparator. The macro supports the calibration requirements of LPDDR4, LPDDR4X and LPDDR5 specs.

ZCALANA performs the following functions in the overall compensation scheme:

- Provides a precision voltage reference programmable to over the range 0.23*VrefDacRef to 0.55*VrefDacRef for LPDDR4 mode and 0.43*VrefDacRef to 0.67*VrefDacRef for LPDDR4X andLPDDR5 modes
- Provides a fine resolution DAC to generate an offset over a small correction voltage range around these Vref set-points. This DAC is used to null out the comparator’s inherent DC offset at the above set-points
- Houses a decoder for Vref generation and a decoder for the Offset Correction DAC
- Provides a very low-leakage analog mux to feed appropriate comparison voltages into the comparator’s inputs during each of the calibration steps
- Provides Analog RC filters (poly resistor, metal cap) to provide noise immunity on the sensitive comparator input nodes and reduce “LSB chatter” on the converged codes
- Consists of clocked comparator which provides digital output to make calibration decisions
- CDM diode cells to protect the comparator input gates exposed to bump connections

Offset compensation is achieved by comparing the DAC output against the precision Vref for each test code of the SAR algorithm. The algorithm naturally searches for the zero crossing of the comparator and hence forces the DAC code to converge to the “offset-compensated Vref”. This setting is then used as the reference for all the subsequent driver calibration steps.

Figure 9-6 ZCALANA Block Diagram



9.3.1.2 Pin List

The following Table shows the pin list for the ZCALANA cell.

Table 9-5 ZCALANA Pin List

Pin Name	Power Domain	Clock Domain	Direction	Description
ZCalPULoad	VDDQ	Async	Analog Input	Active node for Driver Pull-up Calibration. Connects to BP_ZN pin in RDL. BP_ZN pin connects SEPU IOPAD to external precision resistor for pull-up driver impedance calibration.
ZCalPDLoad	VDDQ	Async	Analog Input	Active node for Driver Pull-down Calibration. Connects to ZCAL_INT pin in lower metals. ZCAL_INT pin is SEPD IOPAD for pull-down driver impedance calibration against the calibrated pull-up driver.
PwrOkVDD	VDD	Async	Input	PwrOk on VDD power supply, Generated from POR circuit macro in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down

Pin Name	Power Domain	Clock Domain	Direction	Description
ZCalAnaEn	VDD	RefClk	Input	ZCALANA Enable Signal: Enables Comparator, Ibias, and Sense Amplifier ■ 0 = Disable ■ 1 = Enable
ZCalCompEn	VDD	RefClk	Input	MUX select for comparator offset calibration ■ 0 = Disable ■ 1 = Enable – Selects internal DAC output for comparator offset calibration
ZCalPUEn	VDD	RefClk	Input	MUX select for pull-up driver impedance calibration ■ 0 = Disable ■ 1 = Enable – Selects “ZCalPULoad” for pull-up driver impedance calibration against external precision resistor
ZCalPDEn	VDD	RefClk	Input	MUX select for pull-down driver impedance calibration ■ 0 = Disable ■ 1 = Enable - Selects “ZCalPDLoad” for pull-down driver impedance calibration against the calibrated pull-up driver
ZCalDACRangeSel	VDD	Async	Input	DAC Range Selection ■ 0: LPDDR5/LPDDR4X Mode ■ 1: LPDDR4 Mode
CsrZCalCompVrefDAC[6:0]	VDD	RefClk	Input	VREF code for Comparator offset compensation
ZCalCompVOHDAC[6:0]	VDD	RefClk	Input	DAC code for Comparator Offset-compensated reference
ZCalAnaClk	VDD	RefClk	Input	Sampling clock for comparator Senseamp
CsrZCalCompGainCurrAdj[7:0]	VDD	CsrClk	Input	Bias Current Trim and Comparator gain control ■ [7:6]= Reserved ■ [5:4]=Comparator Gain Control ■ [3:0]=Bias Current Trim ■ Default setting 8'b00000000
CsrZCalCompGainResAdj	VDD	CsrClk	Input	Comparator Gain Programmability with Resistor [Reserved]
CsrZCalCompBiasBypassEn	VDD	CsrClk	Input	[Reserved]
CsrZCalCompBiasPowerUp	VDD	Async	Input	[Reserved]
ZCalCompOut	VDD	RefClk	Output	Comparator output pin - provides comparator decision output

Pin Name	Power Domain	Clock Domain	Direction	Description
PwrOkVDD2	VDD2H	Async	Input	PwrOk on VDD2H power supply, Generated from POR circuit macro in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down
VrefDacRef	VDDQ	Async	Input	Supply (0.27V-1.21V)
VDD	VDD	Async	Input	Digital Logic Power Supply
VSS	0	Async	Input	Ground

9.3.2 Power On Reset: POR (dwc_ddrphy_por)

9.3.2.1 General Description

POR macro is responsible for:

- Generating and distributing PwrOK* signals to all slices in PHY
- Ensuring BP_MEMRESET_L pin is in a known valid state during power-up and retention

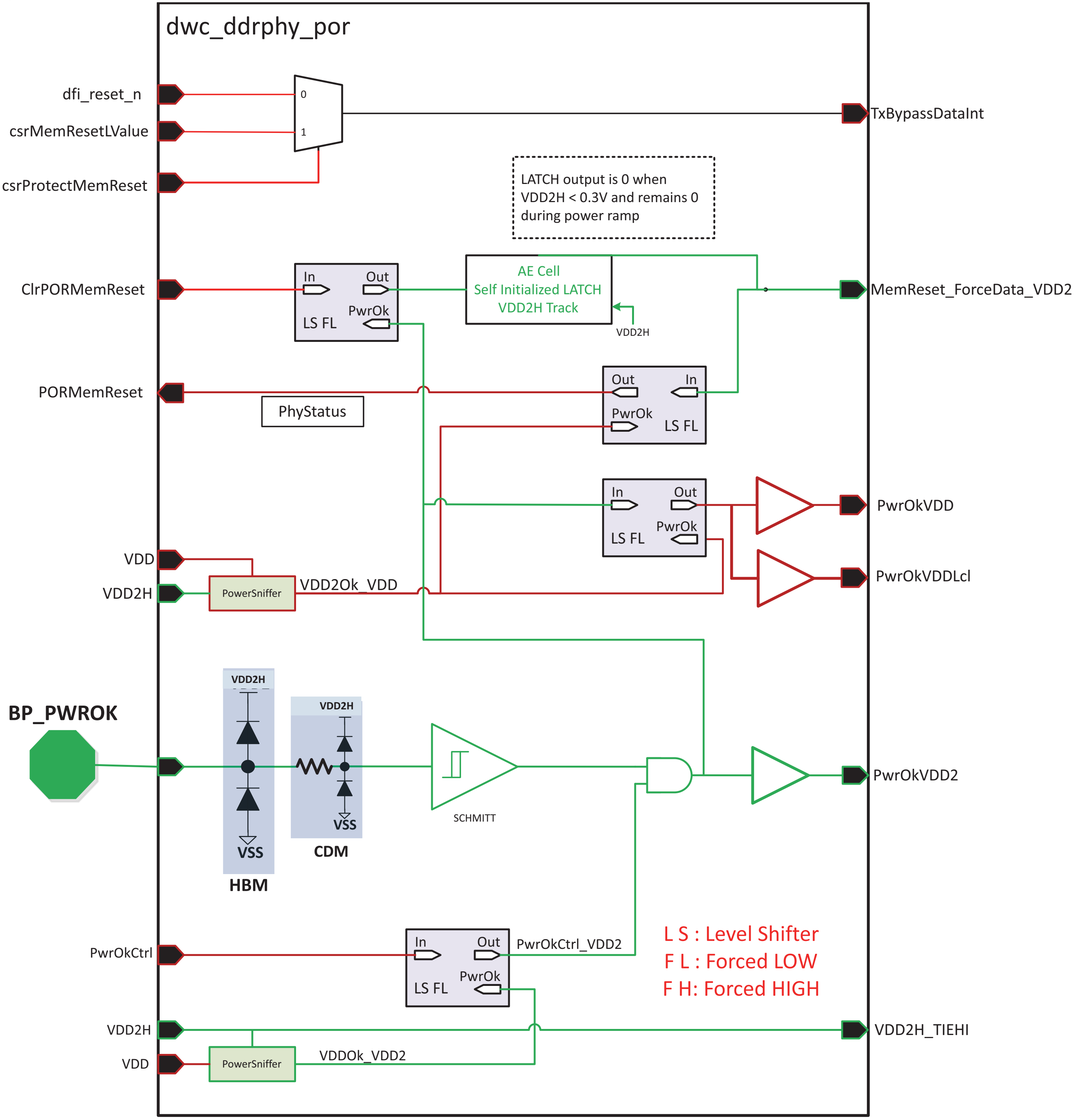
The POR detects initial VDD2H ramp up, followed or preceded by VDD ramp up. After both supplies are ramped up PwrOk* inputs rise followed by reset and control input sequencing during PHY initialization and LP3/IO retention.

POR macro is logically placed in the Master block. The output MemReset_ForceData_VDD2 is input to BP_MemReset_L output driver. A block diagram of POR cell is shown in Figure 9-7 on page 253.

POR macro block diagram illustrates functional elements and signal flow. The boxes labeled LS are special purpose level shifters used to level shift signals from VDD domain into VDD2H domain or vice versa. The PwrOkCtrl input and Power Sniffers force the level shifter outputs to levels indicated by the FL (Forced Low) and FH (Forced High) labels, low and high respectively. Both VDD2H and VDD must be "up" before PwrOkCtrl input to dwc_ddrphy_por is asserted. VDD2H name suffix indicates VDD2H power domain signaling. There are two VDD to VDD2H domain input level shifters and two VDD2H to VDD domain output level shifters.

POR does not have any clock input, PClk or RefClk. The POR macro state bits are dependent upon VDD2H and VDD up/down status and macro inputs sequencing. Any external logic observing macro outputs must synchronize to local clock domain.

Figure 9-7 POR Block Diagram



9.3.2.2 Pin List

The following table shows the pin list for the POR cell.

Table 9-6 POR Pin List

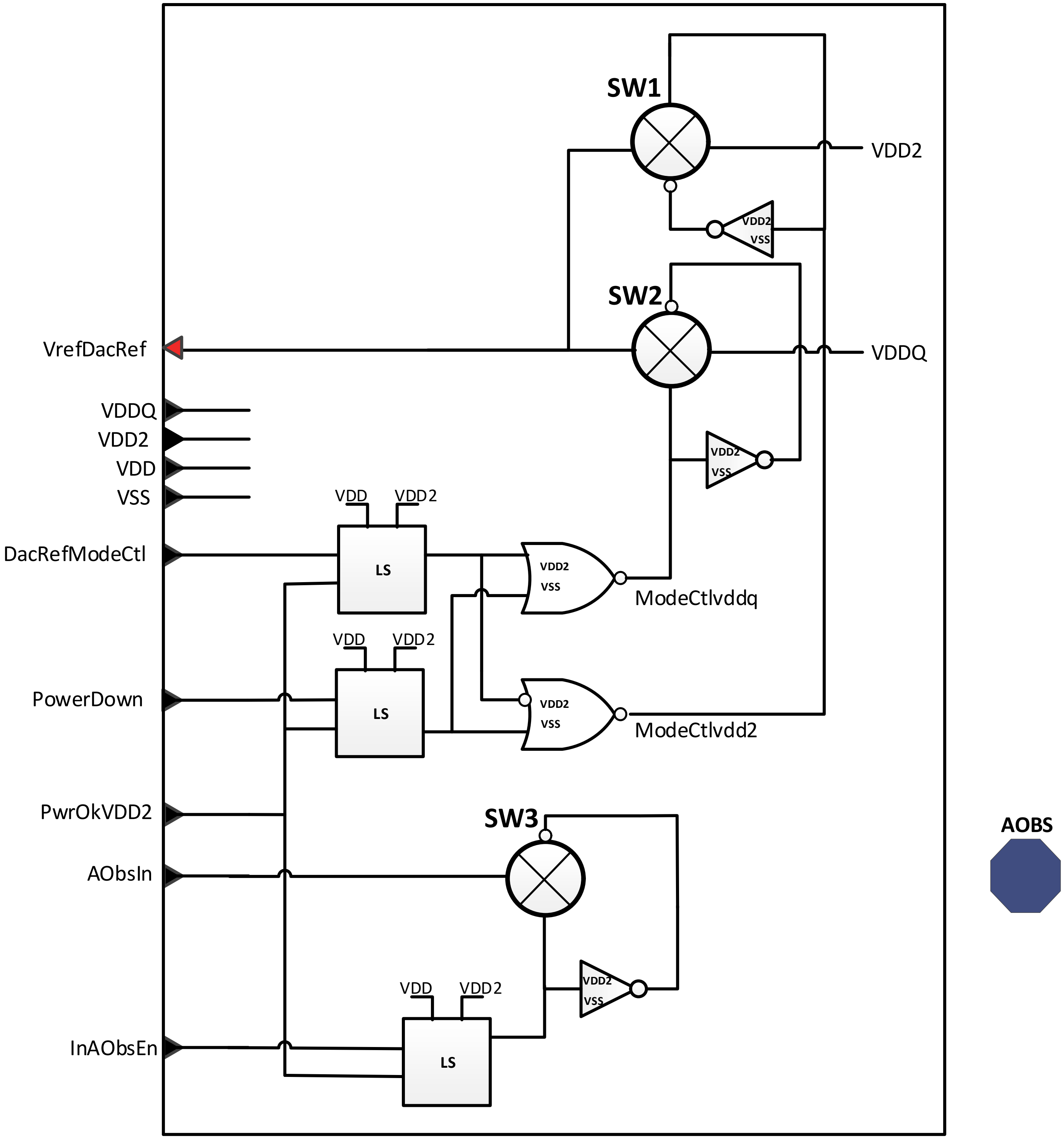
Pin Name	Direction	Power Domain	Clock Domain	Description
VDD2H	Input	VDD2H	Async	VDD2H Power Supply
VDD	Input	VDD	Async	Digital Logic Power Supply
VSS	Input	0	Async	Ground
VDD2H_TIEHI	Output	VVD2H	Async	Copy of VDD2H Power Supply. Provision to short BP_PWROK to VDD2H at user level.
ClrPORMemReset	Input	VDD	Async	When HIGH, sets dwc_ddrphy_por's VDD2H-based POR latch
BP_PWROK	Input	VDD2H	Async	Retention mode control. When de-asserted forces PwrOkVDD/VDD2 outputs to LOW.
PwrOkCtrl	Input	VDD	Async	Power Ok Control Input. When de-asserted forces PwrOkVDD/VDD2 outputs to LOW.
PwrOkVDD	Output	VDD	Async	Sniffs VDD2H supply and gives a 'High' signal in VDD domain if both VDD and VDD2H are 'Ok'
PwrOkVDD2	Output	VDD2H	Async	VDD2H version of PwrOkVDD.
MemReset_ForceData_VDD2	Output	VDD2H	Async	Remanis LOW during initialization and acts as data for BP_MEMRESET_L bump till PwrOkVDD2 is LOW. Set by ClrPORMemReset pulse.
PORMemReset	Output	VDD	Async	POR state: Reset by VDD2H LOW, Set by ClrPORMemReset pulse.
dfi_reset_n	Input	VDD	Async	Dfi Reset input directly from controller
csrMemResetLValue	Input	VDD	Async	BP_MEMRESET_L pad value when csrProtectMemReset=1.
csrProtectMemReset	Input	VDD	Async	When asserted, BP_MEMRESET_L pad gets the value from csrMemResetLValue input.
TxBypassDataInt	Output	VDD	Async	Bypass mode Int data input for SEC (MemReset) IO
PwrOkVDDLcl	Output	VDD	Async	Buffered copy of PwrOkVDD in M5 for internal requirement in Master

9.3.3 VREFDACREF (dwc_ddrphy_vrefdacref)

9.3.3.1 General Description

VREFDACREF is the VrefDacRef supply distribution macro implemented for LPDDR5/4/4x PHY. It supplies the power for all SE_IO and zcalana DAC resistor ladders. This macro is part of MASTER hard IP and VrefDacRef supply gets distributed to zcalana in MASTER and all SE_IOs in SE slices across the PHY in thick coper metal layers MTOP*.

Figure 9-8 VREFDACREF Block Diagram



9.3.3.2 Pin List

The following Table shows the pin list for the VREFDACREF cell.

Table 9-7 VREFDACREF Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
VDD	Input	VDD	Async	Digital Logic Power Supply
VDD2H	Input	VDD2H	Async	VDD2H Power Supply
VDDQ	Input	VDDQ	Async	IO Power Supply
VSS	Input	0	Async	Ground
VrefDacRef	Output	VDD2H	Async	Supply for SE_IO and ZCALANA DAC resistor ladders (0.27V – 1.17V)
DacRefModeCtl	Input	VDD	Async	VrefDacRef Mode Control ■ 0: LPDDR5/LPDDR4X Mode, VrefDacRef=VDDQ ■ 1: LPDDR4 Mode, VrefDacRef=VDD2H [a]
PwrOkVDD2	Input	VDD2H	Async	PwrOk on VDD2H Power Supply generated from POR macro in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down
PowerDown	Input	VDD	Async	Power down input ■ 1: Power Down VrefDacRef ■ 0: VrefDacRef = VDDQ or VDD2H depending on DacRefModeCtl
AObsIn	Input	VDD2H	Async	Analog Observability Input from PLL
InAObsEn	Input	VDD	Async	Enable for Analog Observability Input ■ 1: Pass AObsIn onto AOBS output PAD ■ 0: Tristate AOBS output PAD
AOBS	Output	VDD2H	Async	Analog Observability Output

[a] In LPDDR4 Mode, VDD2H is connected to VDDQ supply at the user level, i.e VDD2H=VDDQ

9.4 DDR IO TX/RX Cells

There are three main DDR IO TX/RX cells built for LPDDR5/4/4x PHY to interface with DRAM. These cells are SE_IO, DIFF_IO and SEC_IO.

9.4.1 IO Overview

SE_IO (dwc_ddrphy_se_io): The SE_IO is a fully custom macro used to implement a single-ended IO on the interface to DRAM. SE_IO is comprised of Transmitter with PVT compensated output driver and Single-ended Receiver with 1-tap DFE.

DIFF_IO (dwc_ddrphy_diff_io): The DIFF_IO is a fully custom macro used to implement differential IOs on the interface to DRAM. There is also an option to use it as two single-ended outputs. The DIFF_IO is comprised of two independently controlled Transmitters with PVT compensated output drivers and Differential Receiver.

SEC_IO (dwc_ddrphy_sec_io): The SEC_IO is a fully custom macro used to implement a single-ended CMOS output on the DRAM interface. The SEC_IO comprises of Transmitter and CMOS Receiver.

9.4.2 SE_IO (dwc_ddrphy_se_io)

This section includes the following topics:

- General Descriptions
- Pin List

9.4.2.1 General Description

The top level functional block diagram of SE_IO is shown in . The SE_IO comprises of Transmitter Front-End (TXFE), Transmitter Back-End (TXBE) and Single Ended Receiver (SE_RX).

TXFE represents the driver front end logic block that receives full rate data bit on TxClk and drives the data into TXBE.

TXBE is a back-end driver capable of driving with the 30Ω impedance at its strongest setting. It is built out of four 120Ω segments [pull-up (PU) and pull-down (PD)]. TXBE supports Transmit and ODT mode. The ODT mode is accomplished via actual drive segments. For LPDDR4, LPDDR4X and LPDDR5 read operation, a Thevenin ODT is not required. Instead, termination consists of a pull-down to VSS. However, SE_IO supports Thevenin ODT in calibration mode for calibrating the driver segment over process and temperature.

The SE_IO receiver is denoted in Figure 5-8 below as SE_RX, it contains:

- Four sense amp positive edge samplers at IOPAD
- Four channel DAC for VREF generation
- Flyover path
- Core loopback path

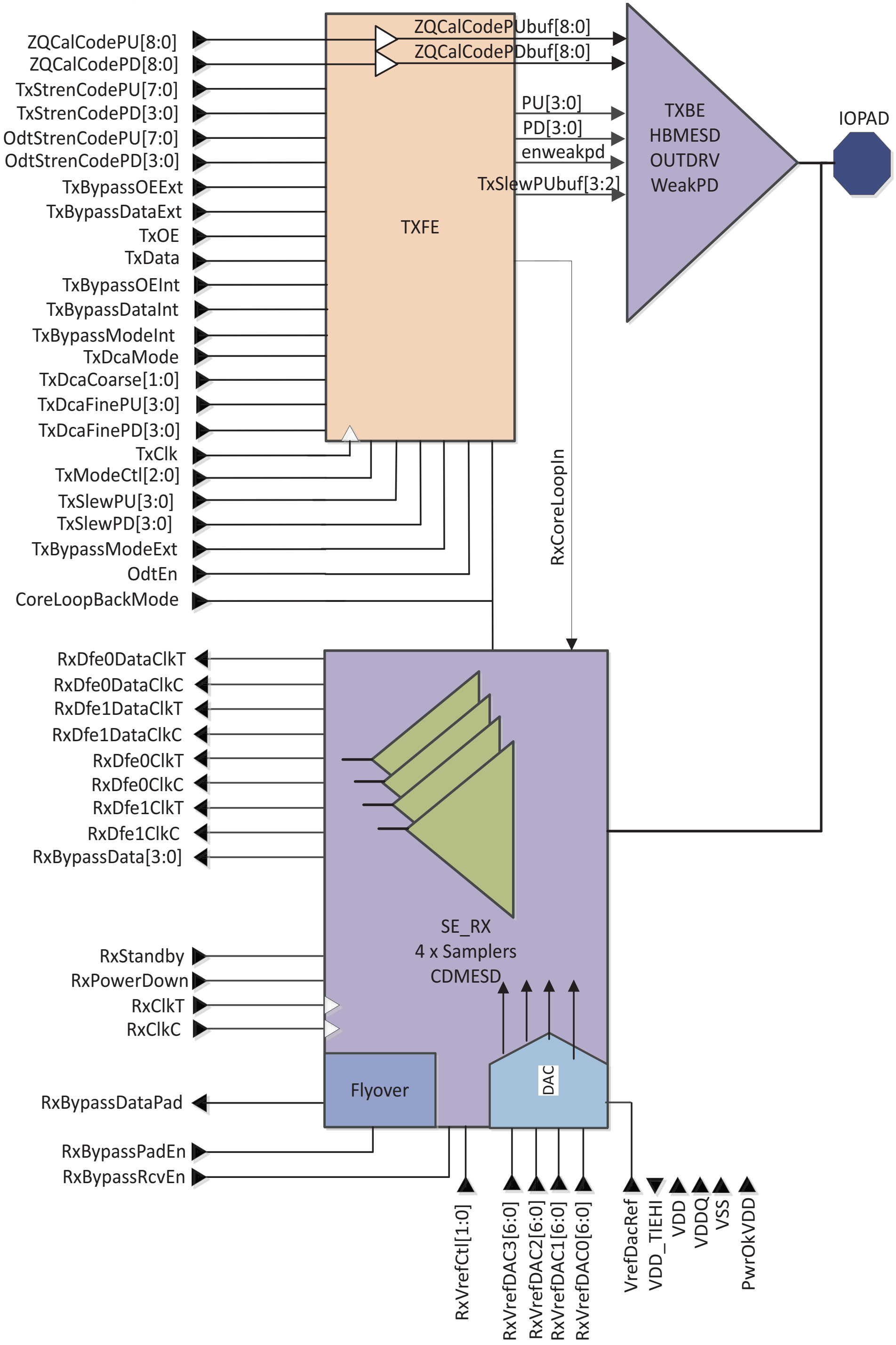
Receiver 1 Tap DFE is implemented outside of SE_IO, post FIFO.

- The entire SE_IO is built with thin gate devices, powered mostly by VDD power supply. The exceptions are:
- Final driver stage on PAD inside TXBE is on VDDQ supply

- VREF-DAC inside SE_RX is powered by a separate input pin, VrefDacRef. The VrefDacRef is a Reference Voltage generated from
- DRAM VDDQ supply by dwc_ddrphy_vrefdacref macro placed inside MASTER hard IP.

Note that the entire SE IO operates on VDD supply in LPDDR4 mode. The SE_IO/SLICE perspective VDDQ and VDD are always separate, the shorting of power rails is done at customer level.

Figure 9-9 SE_IO Block Diagram



9.4.2.2 Pin List

The following Table shows the pin list for the SE_IO cell.

Table 9-8 SE_IO Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
RxVrefCtrl[1:0]	Input	VDD	Async	RX DFE controls ■ 00: No DFE Function, ch0 is ON, ch1 is OFF ■ 01: DFE on, both channels are on ■ 10: Reserved ■ 11: Reserved
RxModeCtl[3:0]	Input	VDD	Async	■ RxModeCtl[3:2]: Reserved ■ RxModeCtl[1]: ❑ TieHi in DQ/DBI outside of SE SLICE; Hard tie in PUB RTL* ❑ Enable Vref DAC in CA/CS SE IO; CSR controlled from PUB** ■ RxModeCtl[0]: Enable vref kick back noise cancellation ❑ 0: Disable ❑ 1: Enable * Caution: Potential reliability issue if not implemented correctly ** Caution: Always connect the AC SE SLICE VrefDacRef pin to VDD. Potential reliability issue if VrefDacRef pin connected to dwc_ddrphy_vrefdacref output.
RxVrefDAC0[6:0]	Input	VDD	Async	Rx DAC control bits for internal VREF0. This is for even clock (RxClkT) ch0 corresponding to output RxDfe0DataClkT.
RxVrefDAC1[6:0]	Input	VDD	Async	Rx DAC control bits for internal VREF1. This is for odd clock (RxClkC) ch0 corresponding to output RxDfe0DataClkC.
RxVrefDAC2[6:0]	Input	VDD	Async	Rx DAC control bits for internal VREF2. This is for even clock (RxClkT) ch1 corresponding to output RxDfe1DataClkT.
RxVrefDAC3[6:0]	Input	VDD	Async	Rx DAC control bits for internal VREF3. This is for odd clock (RxClkC) ch1 corresponding to output RxDfe1DataClkC.
RxBypassPadEn	Input	VDD	Async	Enable RX bypass mode using flyover receiver
RxBypassRcvEn	Input	VDD	Async	Enable RX bypass mode using mission mode receiver
CoreLoopBackMode	Input	VDD	Async	Enables Tx-to-Rx loopback at a point inside the IO; before the PAD node

Pin Name	Direction	Power Domain	Clock Domain	Function
RxPowerDown	Input	VDD	Async	Rx PowerDown ■ 0: Rx Active ■ 1: Rx PowerDown
RxStandby	Input	VDD	Async	Rx Standby ■ 0: Rx Active ■ 1: Rx Standby
RxClkT	Input	VDD	RxClkT	True sampling clock from DQS
RxClkC	Input	VDD	RxClkC	Complement sampling clock from DQS
VrefDacRef	Input	VDDQ	Async	Reference Voltage for the VrefDAC in SE_IO/ZCALANA
VDD_TIEHI	Output	VDDQ	Async	Copy of VDD power supply. Provision to short VrefDacRef to VDD at user level for CA/CS SE_IO
RxBypassData[3:0]	Output	VDD	RxClkT/ RxClkC	Muxed DLL clocked output from mission mode sampler (both ch0 and ch1) on pad when RxBypassRcvEn is high. Otherwise forced to low. RxBypassData[3:0] = RxBypassRcvEn &{out_even1, out_odd1, out_even0, out_odd0}
RxBypassDataPad	Output	VDD	Async	Rx Flyover data output
RxDfe0DataClkT	Output	VDD	RxClkT	Rx mission mode Data even ch0 output
RxDfe0DataClkC	Output	VDD	RxClkC	Rx mission mode Data odd ch0 output
RxDfe1DataClkT	Output	VDD	RxClkT	Rx mission mode Data even ch1 output
RxDfe1DataClkC	Output	VDD	RxClkC	Rx mission mode Data odd ch1 output
RxDfe0ClkT	Output	VDD	RxClkT	Forwarded clk T ch0
RxDfe0ClkC	Output	VDD	RxClkC	Forwarded clk C ch0
RxDfe1ClkT	Output	VDD	RxClkT	Forwarded clk T ch1
RxDfe1ClkC	Output	VDD	RxClkC	Forwarded clk C ch1
TxBypassModeExt	Input	VDD	Async	Tx External Bypass Mode Enable TxBypassModeExt allows the TxBypassDataExt and TxBypassOEExt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.

Pin Name	Direction	Power Domain	Clock Domain	Function
TxBypassModeInt	Input	VDD	Async	Tx Internal Bypass Mode Enable TxBypassModeInt allows the TxBypassDataInt and TxBypassOEInt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. Internal bypass mode is used by PHY to control the IOs through hardware or CSR. During power-up initialization, PHY forces these IOs in known states (driving for RESET/CKE and tri-state for others).
TxBypassDataExt	Input	VDD	Async	Data input for External Bypass mode This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassDataInt	Input	VDD	Async	Data input for Internal Bypass mode
TxBypassOEExt	Input	VDD	Async	Tx External Bypass Output Enable When TxBypassModeExt = 1: ■ TxBypassOEExt =1: Pass the TxBypassDataExt to the output driver without clocks based on TxStrenCode* settings. ■ TxBypassOEExt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings. This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassOEInt	Input	VDD	Async	Tx Internal Bypass Output Enable When TxBypassModeInt = 1 and TxBypassModeExt = 0: ■ TxBypassOEInt =1: Pass the TxBypassDataInt to the output driver without clocks based on TxStrenCode* settings. ■ TxBypassOEInt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings.
TxClk	Input	VDD	TxClk	Full rate clock for data capture
TxData	Input	VDD	TxClk	When TxOE is active data will be delivered to the back end for a “1” or “0”
TxOE	Input	VDD	TxClk	When enabled data is delivered to the back end depending on the state of TxData

Pin Name	Direction	Power Domain	Clock Domain	Function
OdtEn	Input	VDD	Async	ODT Enable: When asserted, output driver is forced in tri-state and receiver ODT enabled. Leakage power saving feature to tri-state the IOPAD without turning on ODT. ■ 0: Tri-state IOPAD if TxOE=0 ■ 1: Enable receiver ODT based on OdtStrenCode* settings if TxOE=0 When TxOE=1, OdtEn is don't care.
ZQCalCodePD[8:0]	Input	VDD	Async	Pull-down ZQ Calibration Code ■ ZQCalCodePD[8]: Base leg control ■ ZQCalCodePD[7:0]: 8-bit binary calibration code ■ ZQCalCodePD[8:0] = 9'b000000000: High impedance ■ ZQCalCodePD[8:0] = 9'b111111111: Maximum drive strength or Lowest impedance
ZQCalCodePU[8:0]	Input	VDD	Async	Pull-up ZQ Calibration Code ■ ZQCalCodePU[8]: Base leg control ■ ZQCalCodePU[7:0]: 8-bit binary calibration code ■ ZQCalCodePU[8:0] = 9'b000000000: High impedance ■ ZQCalCodePU[8:0] = 9'b111111111: Maximum drive strength or Lowest impedance
TxModeCtl[2:0]	Input	VDD	Async	■ Tx Mode Control ■ TxModeCtl[2:1]: Reserved ■ TxModeCtl[0]: Programmable Weak Pull-down ❑ 0: Low Leakage Current * ❑ 1: High Leakage Current * Transmitter performance is optimized with TxModeCtl[0]=0
TxSlewPD[3:0]	Input	VDD	Async	TxSlewPD[3:1]: Slew Rate Control ■ TxSlewPD[0]: Reserved ■ TxSlewPD[3:1] should follow same setting as TxSlewPU[3:1] for optimized performance ■ Default setting TxSlewPD[3:0] = 110x
TxSlewPU[3:0]	Input	VDD	Async	TxSlewPU[3:1]: Slew Rate Control ■ TxSlewPU[0]: Reserved ■ TxSlewPU[3:1] should follow same setting as TxSlewPD[3:1] for optimized performance ■ Default setting TxSlewPU[3:0] = 110x
IOPAD	InOut	VDDQ	Async	PAD

Pin Name	Direction	Power Domain	Clock Domain	Function
PwrOkVDD	Input	VDD	Async	PwrOk on VDD Power Supply Generated from POR cell in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down
TxStrenCodePD[3:0]	Input	VDD	Async	Pull-down drive strength code ■ Active high control bits to enable pull-down output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
TxStrenCodePU[7:0]	Input	VDD	Async	Pull-up drive strength code ■ TxStrenCodePU[7:4]: Reserved ■ TxStrenCodePU[3:0]: Active high control bits to enable pull-up output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
OdtStrenCodePD[3:0]	Input	VDD	Async	Pull-down ODT impedance code ■ Active high control bits to enable pull-down output driver segments in ODT mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
OdtStrenCodePU[7:0]	Input	VDD	Async	Pull-up ODT impedance code ■ OdtStrenCodePU[7:4]: Reserved ■ OdtStrenCodePU[3:0]: Active high control bits to enable pull-up output driver segments in ODT mode * ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273 * Note that these control bits will be set to '1' ONLY in calibration mode.
TxDcaMode	Input	VDD	Async	Enable Tx DCA Mode ■ 0: Disable, DCA Bypass Mode ■ 1: Enable ■ For DBYTEs, SE_IO TxDcaMode value should match with TxDcaMode of DIFF_IO used for WCK (write) ■ For ACs, DCA should be disabled
TxDcaCoarse[1:0]	Input	VDD	Async	DCA Coarse Tune Bits ■ For all DBYTEs, SE_IO TxDcaCoarse[1:0] value should match with TxDcaCoarse of DIFF_IO used for WCK (write)
TxDcaFinePU[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Up path ■ Set to 4'b0110 by IMPL in SE hard-macro

Pin Name	Direction	Power Domain	Clock Domain	Function
TxDcaFinePD[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Down path ■ Set to 4’b0110 by IMPL in SE hard-macro
TxDcaMode	Input	VDD	Async	Enable Tx DCA mode
TxDcaCoarse[1:0]	Input	VDD	Async	Coarse tune bits
TxDcaFinePU[3:0]	Input	VDD	Async	Fine tune bits for pull-up path
TxDcaFinePD[3:0]	Input	VDD	Async	Fine tune bits for pull-down path
VDD	Input	VDD	Async	Digital Logic Power Supply
VDDQ	Input	VDDQ	Async	IO Power Supply
VSS	Input	0	Async	Ground

9.4.3 DIFF_IO (dwc_ddrphy_diff_io)

This section includes the following topics:

- General Descriptions
- Pin List

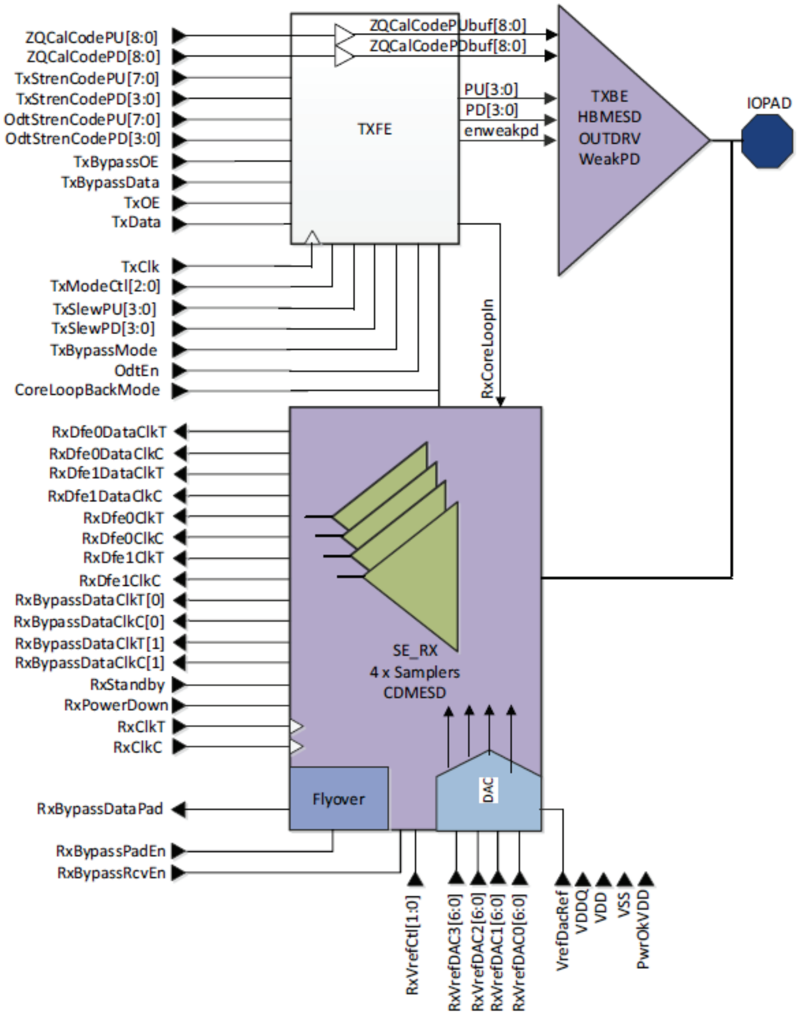
9.4.3.1 General Description

The block diagram of DIFF_IO is shown in Figure 9-10 on page 265. The IO is configured to contain two TX back ends, each capable to drive the pad with the impedance down to 30 Ohms. Each TXBE is built out of four-120 Ohms segments [pull up (PU) and pull down (PD)].

TXFE represents the driver front logic block that receives full rate data bit on TxClk and drives the data into TXBE. But more importantly for the strobe DQS mode it can drive the outputs differentially to two driver back ends.

DIFF_IO also contains a DIFF differential clock receiver. It receives DIFF strobe clocks from VDDQ domain and amplifies them, level shifts them to the CMOS VDD levels and differentially delivers them to the read DLL at the PHYDAT level.

Figure 9-10 DIFF_IO Block Diagram



9.4.3.2 Pin List

The following Table shows the pin list for the DIFF_IO cell.

Table 9-9 DIFF_IO Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
RxGainCurrAdj[3:0]	Input	VDD	Async	Bias current control Default setting RxGainCurrAdj [3:0] = 0101

Pin Name	Direction	Power Domain	Clock Domain	Function
RxDiffModeCtl[3:0]	Input	VDD	Async	RxDiffModeCtl [1:0] is used to control current according to boost/non-boost VDD. ■ 11: non-boost VDD ■ 00: boost VDD RxDiffModeCtl [3:2] is reserved.
CoreLoopBackMode	Input	VDD	Async	Enable core loopback function (allows to feed loopback signal from Tx FE into the receiver)
RxPowerDown	Input	VDD	Async	Active high signal which places the receiver in power-down mode (Power-down amplifier as well as bias)
RxStandby	Input	VDD	Async	Active high signal which places the receiver in standby mode (Power-down amplifier, but keeps bias on)
RxBypassPadEn	Input	VDD	Async	Enable bypass mode using flyover receiver.
RxBypassRcvEn	Input	VDD	Async	Enable bypass mode using mission mode receiver.
RxBypassDataRcvT	Output	VDD	IOPADT	CMOS level data strobe output, when RxBypassEn is high. Otherwise force to low
RxBypassDataRcvC	Output	VDD	IOPADC	
RxBypassDataPadT	Output	VDD	-	Flyover path buffered version of incoming DQ data. Enabled when RxBypassEn is high, force low when RxBypassEn is low
RxBypassDataPadC	Output	VDD	-	
RxDataCoreT	Output	VDD	-	Core loopback output. Enabled when CoreLoopBackMode is high, force low when low
RxDataCoreC	Output	VDD	-	
RxDataRcvT	Output	VDD	IOPADT	Mission mode RX output (CMOS level data strobe output)
RxDataRcvC	Output	VDD	IOPADC	
TxBypassModeExt	Input	VDD	Async	Tx External Bypass Mode Enable TxBypassModeExt allows the TxBypassDataExt and TxBypassOEExt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassDataTExt	input	VDD	Async	Data input for External Bypass mode – True This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.

Pin Name	Direction	Power Domain	Clock Domain	Function
TxBypassDataCExt	input	VDD	Async	Data input for External Bypass mode – Complement This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassOETExt	input	VDD	Async	■ Tx External Bypass Output Enable – True ■ When TxBypassModeExt = 1: ❑ TxBypassOETExt =1: Pass the TxBypassDataTExt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOETExt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings ❑ This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassOECExt	input	VDD	Async	■ Tx External Bypass Output Enable – Complement ■ When TxBypassModeExt = 1: ❑ TxBypassOECExt =1: Pass the TxBypassDataCExt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOECExt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings. ❑ This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassModeInt	input	VDD	Async	■ Tx Internal Bypass Mode Enable ■ TxBypassModeInt allows the TxBypassDataInt and TxBypassOEInt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. ■ Internal bypass mode is used by PHY to control the IOs through hardware or CSR. During power-up initialization, PHY forces these IOs in known states (driving for RESET/CKE and tri-state for others).
TxBypassDataTInt	input	VDD	Async	Data input for Internal Bypass mode – True
TxBypassDataCInt	input	VDD	Async	Data input for Internal Bypass mode – Complement

Pin Name	Direction	Power Domain	Clock Domain	Function
TxBypassOETInt	input	VDD	Async	■ Tx Internal Bypass Output Enable - True ■ When TxBypassModeInt = 1 and TxBypassModeExt = 0: ❑ TxBypassOETInt =1: Pass the TxBypassDataTInt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOETInt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings. ❑ This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassOECInt	input	VDD	Async	■ Tx Internal Bypass Output Enable – Complement ■ When TxBypassModeInt = 1 and TxBypassModeExt = 0: ❑ TxBypassOECInt =1: Pass the TxBypassDataCInt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOECInt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings.
OdtEn	input	VDD	Async	ODT Enable: When asserted, output driver is forced in tri-state and receiver ODT enabled. Leakage power saving feature to tri-state IOPADT/IOPADC without turning on ODT. ■ 0: Tri-state IOPADT/IOPADC if TxOET/TxOEC=0 ■ 1: Enable receiver ODT based on OdtStrenCode* settings if TxOET/TxOEC=0 ■ When TxOET/TxOEC=1, OdtEn is don’t care
TxClk	Input	VDD	TxClk	Full rate clock for data capture
TxDataT	Input	VDD	TxClk	When TxOET is active data will be delivered to the back end for a “1” or “0”
TxDataC	Input	VDD	TxClk	
TxOET	Input	VDD	TxClk	When enabled data is delivered to the back end depending in the state of TxDataT.
TxOEC	Input	VDD	TxClk	When enabled data is delivered to the back end depending in the state of TxDataC.
ZQCalCodePDT[8:0]	Input	VDD	Async	Pull-down ZQ Calibration Code - True ■ ZQCalCodePDT[8]: Base leg control ■ ZQCalCodePDT[7:0]: 8-bit binary calibration code. ■ ZQCalCodePDT[8:0] = 9’b000000000: High impedance ■ ZQCalCodePDT[8:0] = 9’b111111111: Maximum drive strength or Lowest impedance

Pin Name	Direction	Power Domain	Clock Domain	Function
ZQCalCodePUT[8:0]	Input	VDD	Async	Pull-up ZQ Calibration Code - True ■ ZQCalCodePUT[8]: Base leg control ■ ZQCalCodePUT[7:0]: 8-bit binary calibration code. ■ ZQCalCodePUT[8:0] = 9'b000000000: High impedance ■ ZQCalCodePUT[8:0] = 9'b111111111: Maximum drive strength or Lowest impedance
ZQCalCodePDC[8:0]	Input	VDD	Async	Pull-down ZQ Calibration Code - Complement ■ ZQCalCodePDC[8]: Base leg control ■ ZQCalCodePDC[7:0]: 8-bit binary calibration code. ■ ZQCalCodePDC[8:0] = 9'b000000000: High impedance ■ ZQCalCodePDC[8:0] = 9'b111111111: Maximum drive strength or Lowest impedance
ZQCalCodePUC[8:0]	Input	VDD	Async	Pull-up ZQ Calibration Code - Complement ■ ZQCalCodePUC[8]: Base leg control ■ ZQCalCodePUC[7:0]: 8-bit binary calibration code. ■ ZQCalCodePUC[8:0] = 9'b000000000: High impedance ■ ZQCalCodePUC[8:0] = 9'b111111111: Maximum drive strength or Lowest impedance
TxModeCtl[2:0]	Input	VDD	Async	Tx Mode Control TxModeCtl[2:1]: Reserved TxModeCtl[0]: Programmable Weak Pull-down ■ 0: Low Leakage Current * ■ 1: High Leakage Current * Transmitter performance is optimized with TxModeCtl[0]=0
TxSlewPD[3:0]	Input	VDD	Async	TxSlewPD[3:1]: Slew Rate Control ■ TxSlewPD[0]: Reserved ■ TxSlewPD[3:1] should follow same setting as TxSlewPU[3:1] for optimized performance ■ Default setting TxSlewPD[3:0] = 110x
TxSlewPU[3:0]	Input	VDD	Async	TxSlewPU[3:1]: Slew Rate Control ■ TxSlewPU[0]: Reserved ■ TxSlewPU[3:1] should follow same setting as TxSlewPD[3:1] for optimized performance ■ Default setting TxSlewPU[3:0] = 110x

Pin Name	Direction	Power Domain	Clock Domain	Function
IOPADT	InOut	VDDQ	Async	Output PADT
IOPADC	InOut	VDDQ	Async	Output PADC
PwrOkVDD	Input	VDD	Async	PwrOk on VDD Power Supply Generated from POR cell in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Any or All power rails are down
PwrOkVDDLcl	Output	VDD	Async	Buffered copy of PwrOkVDD in lower metals (example: M5) for internal requirement in MASTER
PwrOkVDDLcl	Output	VDD	Async	Buffered copy of PwrOkVDD in M5 for internal requirement in Master
TxStrenCodePDT[3:0]	Input	VDD	Async	Pull-down drive strength code – True ■ TxStrenCodePDT[3:0]: Active high control bits to enable pull-down output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
TxStrenCodePUT[7:0]	Input	VDD	Async	Pull-up drive strength code – True ■ TxStrenCodePUT[7:4]: Reserved ■ TxStrenCodePUT[3:0]: Active high control bits to enable pull-up output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
TxStrenCodePDC[3:0]	Input	VDD	Async	Pull-down drive strength code – Complement ■ TxStrenCodePDC[3:0]: Active high control bits to enable pull-down output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
TxStrenCodePUC[7:0]	Input	VDD	Async	Pull-up drive strength code – Complement ■ TxStrenCodePUC[7:4]: Reserved ■ TxStrenCodePUC[3:0]: Active high control bits to enable pull-up output driver segments in Transmit mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273
OdtStrenCodePDT[3:0]	Input	VDD	Async	Pull-down ODT impedance code – True ■ Active high control bits to enable pull-down output driver segments in ODT mode ■ Refer to "SE_IO/DIFF_IO Output Drive Strength Option" on page 273

Pin Name	Direction	Power Domain	Clock Domain	Function
OdtStrenCodePUT[7:0]	Input	VDD	Async	Pull-up ODT impedance code – True ■ OdtStrenCodePUT [7:4]: Reserved ■ OdtStrenCodePUT [3:0]: Active high control bits to enable pull-up output driver segments in ODT mode Note: Do Not Use – LPDDR54 DIFF hard-macro never configured in pull-up ODT mode
OdtStrenCodePDC[3:0]	Input	VDD	Async	Pull-down ODT impedance code – Complement ■ Active high control bits to enable pull-down output driver segments in ODT mode
OdtStrenCodePUC[7:0]	Input	VDD	Async	Pull-up ODT impedance code – Complement Path ■ OdtStrenCodePUC [7:4]: Reserved ■ OdtStrenCodePUC [3:0]: Active high control bits to enable pull-up output driver segments in ODT mode Note: Do Not Use – LPDDR54 DIFF hard-macro never configured in pull-up ODT mode
TxDcaMode	Input	VDD	Async	Enable Tx DCA Mode ■ 0: Disable, DCA Bypass Mode ■ 1: Enable ■ For DBYTEs, SE_IO TxDcaMode value should match with TxDcaMode of DIFF_IO used for WCK (write) ■ For ACs, DCA should be disabled
TxDcaCoarseT[1:0]	Input	VDD	Async	DCA Coarse Tune Bits – True ■ 10: WCK Frequency = 2.5 GHz ■ 11: WCK Frequency = 3.2 GHz ■ Default setting: 11
TxDcaCoarseC[1:0]	Input	VDD	Async	DCA Coarse Tune Bits – Complement ■ 10: WCK Frequency = 2.5 GHz ■ 11: WCK Frequency = 3.2 GHz ■ Default setting: 11
TxDcaFinePUT[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Up path – True ■ 0000: Target 45% duty cycle output ■ 0110: Target 50% duty cycle output ■ 1100: Target 55% duty cycle output ■ Default setting: 0110

Pin Name	Direction	Power Domain	Clock Domain	Function
TxDcaFinePDT[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Down path – True ■ 0000: Target 45% duty cycle output ■ 0110: Target 50% duty cycle output ■ 1100: Target 55% duty cycle output ■ Default setting: 0110
TxDcaFinePUC[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Up path – Complement ■ 0000: Target 45% duty cycle output ■ 0110: Target 50% duty cycle output ■ 1100: Target 55% duty cycle output ■ Default setting: 0110
TxDcaFinePDC[3:0]	Input	VDD	Async	DCA Fine Tune Bits for Pull-Down path – Complement ■ 0000: Target 45% duty cycle output ■ 0110: Target 50% duty cycle output ■ 1100: Target 55% duty cycle output ■ Default setting: 0110
TxDcaMode	Input	VDD	Async	Enable Tx DCA mode
TxDcaCoarseT[1:0]	Input	VDD	Async	Coarse tune bits – True
TxDcaCoarseC[1:0]	Input	VDD	Async	Coarse tune bits – Complement
TxDcaFinePUT[3:0]	Input	VDD	Async	Fine tune bits for pull-up path – True
TxDcaFinePDT[3:0]	Input	VDD	Async	Fine tune bits for pull-down path – True
TxDcaFinePUC[3:0]	Input	VDD	Async	Fine tune bits for pull-up path – Complement
TxDcaFinePDC[3:0]	Input	VDD	Async	Fine tune bits for pull-down path – Complement
dqsEn_arm	Input	VDD	Async	RXEN LCDL output, Enable the set of the rsm flop
train	Input	VDD	Async	Training mode for the phase detector and disable of the set of the rsm flop
track	Input	VDD	Async	Tracking mode of the phase detector
rsm_reset	Input	VDD	Async	RSM flop reset
dqsEnSync	Input	VDD		Input to the rsm flop from the fifo
clk_rsmX	Output	VDD	IOPADT/C	Clock for the read state machine used to read data out of the fifo
dqsSamp_train	Output	VDD	dqsEn_arm	Training flop output
dqsSamp_track	Output	VDD	dqsEn_arm	Tracking flop output

Pin Name	Direction	Power Domain	Clock Domain	Function
RxDiffSeCtl[1:0]	input	VDD	Async	Differential Rx SE Mode Control ■ 00: IOPADT/C are differential inputs ■ 01: Single ended input on IOPADT, VREF is connected with IOPADC ■ 10: Single ended input on IOPADC , VREF is connected with IOPADT ■ 11: Illegal. Model outputs as “x”
RxDiffSeVrefDACEn	input	VDD	Async	Differential Rx SE Mode DAC Enable ■ 0: disable internal VREFDAC ■ 1: enable internal VREFDAC Tie to VDD if VrefDacRef is connected to VrefDacRef distribution
RxDiffSeVrefDAC[6:0]	input	VDD	Async	DAC control for internal VREF. All four Vrefs share the same DAC code.
VrefDacRef	input	VDDQ	Async	Reference Voltage for the VrefDAC in SE_IO/DIFF_IO/ZCALANA. This special power supply helps VrefDAC to track VDDQ if connected to VrefDacRef distribution. User has the option to connect VrefDacRef to either VDD or VrefDacRef distribution. * Note that if VrefDacRef is connected to VrefDacRef distribution, pin RxDiffSeVrefDACEn needs to be tie high to avoid reliability issue.
VDD_TIEHI	Output	VDD	Async	Copy of VDD power supply. Provision to short VrefDacRef to VDD at user level for DIFF_IO
VDD	Input	VDD	Async	Digital Logic Power Supply
VDDQ	Input	VDDQ	Async	VDDQ power supply
VSS	Input	0	Async	Ground

9.4.4 SE_IO/DIFF_IO Output Drive Strength Option

This section covers the details of calibration points, output driver strength control, preserving pull-up VOH levels, and strength settings used for impedance calibration.

- SE_IO and DIFF_IO circuit-macros use the same transmitter backend (TXBE)
- TXBE consists of 4 x 120Ω pull-up driver segments and 4 x 120Ω pull-down driver segments
- Each output driver segment is controlled by 9-bit ZQ Calibration Codes
    - ZQCalCode*[7:0]: Each driver segment uses 8-bit binary calibration codes which are PVT calibrated
    - ZQCalCode*[8]: Each driver segment uses 1-bit base leg control which is not part of impedance calibration

- LPDDR54 PHY supports impedance calibration with external resistor RZN = 120Ω ± 1% tolerance

9.4.4.1 LPDDR5 VOH=0.5*VDDQ

- VOH calibration point = 0.5*VDDQ
- Pull-up (PU) calibration: 1-segment of PU against external 120Ω resistor (RZN)
- In order to preserve calibrated VOH level customer can use mission mode drivers with following DRAM ODT:
  - 2-segments of TX PU driving DRAM's 60Ω ODT
- Pull-down (PD) calibration: 2-segment of PD against 1-segment of calibrated PU
- In this configuration a single segment of NMOS PD would be always calibrated to 120Ω

9.4.4.2 LPDDR4X VOH=0.5*VDDQ, 0.6*VDDQ

- VOH calibration point = 0.5*VDDQ or 0.6*VDDQ
- Pull-up (PU) calibration: 1-segment of PU against external 120Ω resistor (RZN)
- In order to preserve calibrated VOH level customer can use mission mode drivers with following DRAM ODT:
  - 1-segment of TX PU driving DRAM's 120Ω ODT
  - 2-segments of TX PU driving DRAM's 60Ω ODT
  - 3-segments of TX PU driving DRAM's 40Ω ODT
  - 4-segments of TX PU driving DRAM’s 30Ω ODT
- Pull-down (PD) calibration: 1-segment of PD against 1-segment of calibrated PU
- In this configuration a single segment of NMOS PD would be always calibrated to 120Ω

9.4.4.3 LPDDR4 VOH=VDDQ_DRAM/3

- VOH calibration point = VDDQ_DRAM/3
- Pull-up (PU) calibration: 1-segment of PU against external 120Ω resistor (RZN)
- In order to preserve calibrated VOH level customer can use mission mode drivers with following DRAM ODT:
  - 1-segment of TX PU driving DRAM's 120Ω ODT
  - 2-segments of TX PU driving DRAM's 60Ω ODT
  - 3-segments of TX PU driving DRAM's 40Ω ODT
  - 4-segments of TX PU driving DRAM’s 30Ω ODT
- Pull-down (PD) calibration: 1-segment of PD against 1-segment of calibrated PU
- In this configuration a single segment of NMOS PD would be always calibrated to 120Ω

9.4.4.4 LPDDR4 VOH=VDDQ_DRAM/2.5

- VOH calibration point = VDDQ_DRAM/2.5
- Pull-up (PU) calibration: 2-segment of PU against external 120Ω resistor (RZN)
- In order to preserve calibrated VOH level customer can use mission mode drivers with following DRAM ODT:
  - 1-segment of TX PU driving DRAM's 240Ω ODT
  - 2-segments of TX PU driving DRAM's 120Ω ODT
  - 3-segments of TX PU driving DRAM's 80Ω ODT
- Pull-down (PD) calibration: 2-segment of PD against 2-segment of calibrated PU
- In this configuration a single segment of NMOS PD would be always calibrated to 240Ω

9.4.4.5 Pull-up drive strength control

Table 9-10 Pull-up drive strength control

TxStrenCode PU[7:0] TxStrenCode PUT[7:0] TxStrenCode PUC[7:0]	No of pull-up driver segments enabled	LPDDR5/4X Rdrv (Ohm) @ VOH=0.5*VDDQ	LPDDR4X Rdrv (Ohm) @ VOH=0.6*VDDQ	LPDDR4 Rdrv (Ohm) @ VOH=VDDQ_DRAM/3	LPDDR4 Rdrv (Ohm) @ VOH=VDDQ_DRAM/2.5
xxxx0000	0	High impedance	High impedance	High impedance impedance	High impedance
xxxx0001	1	120	80	240	360
xxxx0011	2	60	40	120	180
xxxx0111	3	40	Do Not Use	80	120
xxxx1111	4	30	Do Not Use	60	

1. Specified impedance values can only be achieved with valid PVT calibrated binary impedance codes ZQCalCode*[7:0].
2. Independent of TxStrenCode* setting if ZQCalCode*[8:0] is forced to 9’b000000000 then output driver will be set to high impedance.
3. Setting maximum output drive strength: Setting both TxStrenCode* and ZQCalCode* to all ones will configure the output driver in maximum possible output drive strength.

9.4.4.6 Pull-down drive strength control

Table 9-11 Pull-down drive strength control

TxStrenCode PD[3:0] TxStrenCode PDT[3:0] TxStrenCode PDC[3:0]	No of pull-down driver segments enabled	LPDDR5/4X Rdrv (Ohm) @ VOH=0.5*VDDQ	LPDDR4X Rdrv (Ohm) @ VOH=0.6*VDDQ	LPDDR4 Rdrv (Ohm) @ VOH=VDDQ_DRAM/3	LPDDR4 Rdrv (Ohm) @ VOH=VDDQ_DRAM/2.5
0000	0	High impedance	High impedance	High impedance	High impedance
0001	1	120	120	120	240
0011	2	60	60	60	120
0111	3	40	Do Not Use	40	80
1111	4	30	Do Not Use	30	

1. Specified impedance values can only be achieved with valid PVT calibrated binary impedance codes ZQCalCode*[7:0].
2. Independent of TxStrenCode* setting if ZQCalCode*[8:0] is forced to 9’b000000000 then output driver will be set to high impedance.
3. Setting maximum output drive strength: Setting both TxStrenCode* and ZQCalCode* to all ones will configure the output driver in maximum possible output drive strength.

9.4.4.7 Pull-down ODT strength control

Table 9-12 Pull-down ODT strength control

OdtStrenCode PD[3:0] OdtStrenCode PDT[3:0] OdtStrenCode PDC[3:0]	No of pull-down driver segments enabled	LPDDR5/4X Rodt (Ohm) @ VOH=0.5*VDDQ	LPDDR4X Rodt (Ohm) @ VOH=0.6*VDDQ	LPDDR4 Rodt (Ohm) @ VOH=VDDQ_DRAM/3	LPDDR4 Rodt (Ohm) @ VOH=VDDQ_DRAM/2.5
0000	0	High impedance	High impedance	High impedance	High impedance
0001	1	120	120	120	
0011	2	60	60	60	120
0111	3	40	40	40	
1111	4	30	30	30	

1. Specified impedance values can only be achieved with valid PVT calibrated binary impedance codes ZQCalCode*[7:0].
2. Independent of OdtStrenCode* setting if ZQCalCode*[8:0] is forced to 9′b000000000 then output driver will be set to high impedance.
3. Setting max ODT strength: Setting both OdtStrenCode* and ZQCalCode* to all ones will configure the output driver in maximum possible ODT strength.

9.4.4.8 SE_IO driver strength settings for impedance calibration

Table 9-13 SE_IO driver strength settings for impedance calibration

DDR Mode	Calibration VOH	OdtStrenCode PU[7:0]	OdtStrenCode PD[3:0]	No of driver segments enabled	
				Pull-up	Pull-down
LPDDR5	0.5*VDDQ	xxxx1000	1000	1	1
LPDD4X	0.5*VDDQ	xxxx1000	1000	1	1
	0.6*VDDQ	xxxx1000	1000	1	1
LPDDR4	VDDQ_DRAM/3	xxxx1000	1000	1	1
	VDDQ_DRAM/2.5	xxxx1100	1100	2	2

9.4.5 SEC_IO (dwc_ddrphy_sec_io)

This section includes the following topics:

- General Descriptions
- Pin List

9.4.5.1 General Description

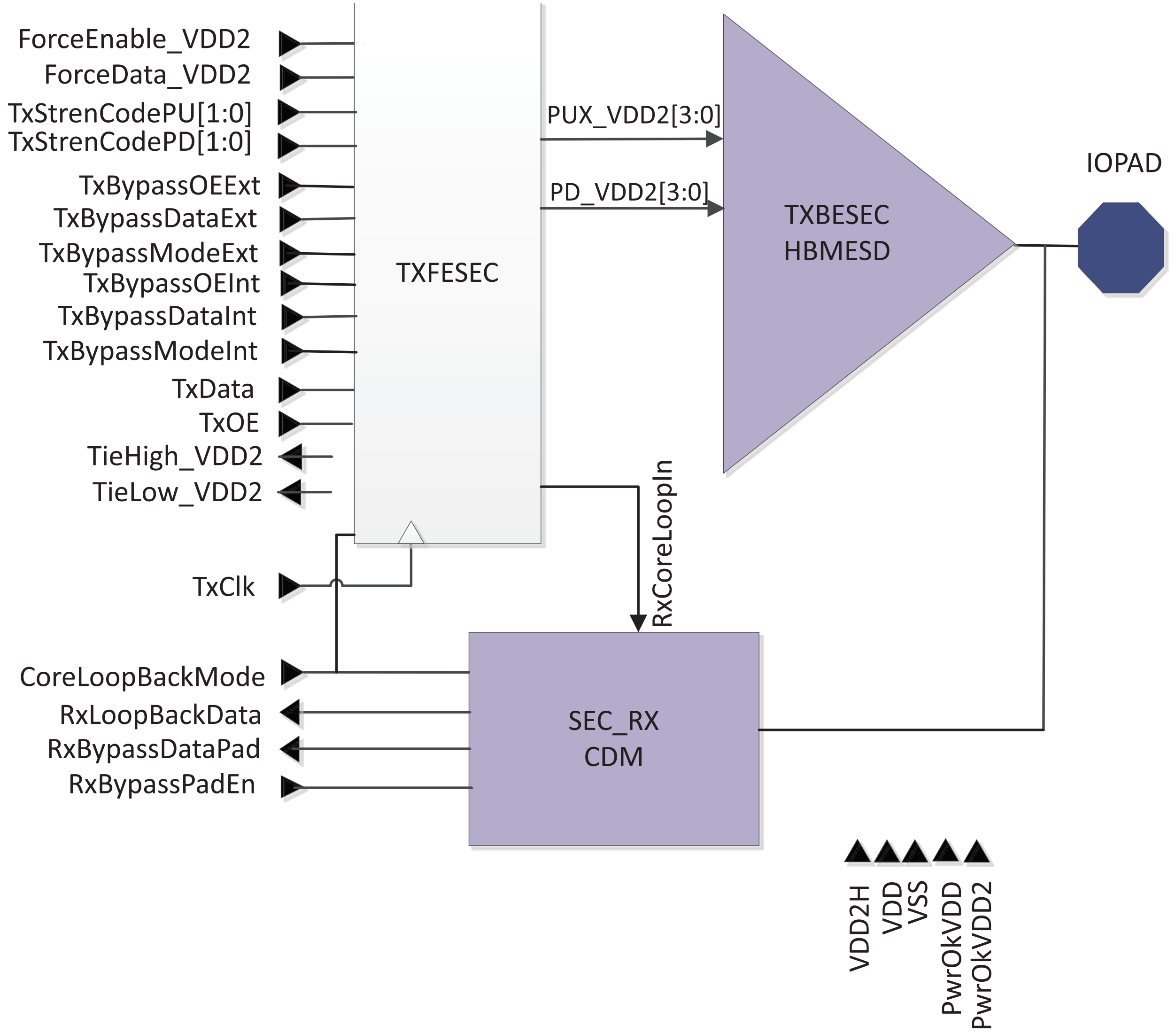
The SEC_IO is used to implement a single-ended CMOS output on the DRAM interface. The SEC_IO comprises of Transmitter and CMOS Receiver.

The top level functional block diagram of SEC_IO is shown in the following Figure. TXFESEC represents the driver front logic block that receives data bits, drives data to the TXBESEC. The data inputs TxData, and TxOE get captured on the positive edge of full rate clock TxClk. The data output bit rate at IOPAD is the same as the input clock frequency.

TXBESEC is a back-end driver capable of driving with the 50 Ohms impedance at its strongest setting in support of POP. It is built out of eight 400Ω segments [pull up (PU) and pull down (PD)] and supports programmable driving strength of 50Ω, 66Ω, 100Ω and 400Ω at typical corner. Driver back-end TXBESEC is uncalibrated and unterminated.

The IO receiver is denoted in figure below as SECRX, it contains two paths, one from the IOPAD controlled by RxBypassEn signal and the other is loopback path coming from the TXFESEC controlled by CoreLoopBackMode.

Figure 9-11 SEC_IO Block Diagram



9.4.5.2 Pin List

The following Table shows the pin list for the SEC_IO cell.

Table 9-14 SEC_IO Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
CoreLoopBackMode	Input	VDD	Async	Enables Tx-to-Rx loopback at a point inside the IO; before the PAD node
RxBypassPadEn	Input	VDD	Async	Enable bypass mode using flyover receiver. Flyover receiver is the only receiver in SEC IO.

Pin Name	Direction	Power Domain	Clock Domain	Function
RxBypassDataPad	Output	VDD	Aync	Flyover path buffered version of incoming DQ data. Enabled when RxBypassEn is high, force low when RxBypassEn is low.
RxLoopBackData	Output	VDD	Async	Core loopback output when CoreloopMode is high, otherwise outputs flyover receiver output.
TxBypassModeExt	Input	VDD	Async	■ Tx External Bypass Mode Enable ■ TxBypassModeExt allows the TxBypassDataExt and TxBypassOEExt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. ■ This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassModeInt	Input	VDD	Async	■ Tx Internal Bypass Mode Enable ■ TxBypassModeInt allows the TxBypassDataInt and TxBypassOEInt inputs to asynchronously control the output driver without clocks. Bypass mode supports IOPAD states of Pull up, Pull down, ODT and tri-state. ■ Internal bypass mode is used by PHY to control the IOs through hardware or CSR. During power-up initialization, PHY forces these IOs in known states (driving for RESET/CKE and tri-state for others).
TxBypassDataExt	Input	VDD	Async	Data input for External Bypass mode This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.
TxBypassDataInt	Input	VDD	Async	Data input for Internal Bypass mode
TxBypassOEExt	Input	VDD	Async	Tx External Bypass Output Enable ■ When TxBypassModeExt = 1: ❑ TxBypassOEExt =1: Pass the TxBypassDataExt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOEExt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings. ■ This is connected to PHY_TOP directly so that SOC/Customer can controls the IOs during different type of testing modes.

Pin Name	Direction	Power Domain	Clock Domain	Function
TxBypassOEInt	Input	VDD	Async	Tx Internal Bypass Output Enable ■ When TxBypassModeInt = 1 and TxBypassModeExt = 0: ❑ TxBypassOEInt =1: Pass the TxBypassDataInt to the output driver without clocks based on TxStrenCode* settings. ❑ TxBypassOEInt =0: ODT or Tri-state IOPAD based on OdtStrenCode* settings.
TxClk	Input	VDD	TxClk	Full rate clock for data capture
TxData	Input	VDD	TxClk	When TxOE is active data will be delivered to the back end for a “1” or “0”
TxOE	Input	VDD	TxClk	When enabled data is delivered to the back end depending in the state of TxData.
TxStrenCodePD[1:0]	Input	VDD	Async	Enables the pull-down segments ■ 00: 400 Ohms ■ 01: 100 Ohms ■ 10: 66.6 Ohms ■ 11: 50 Ohms
TxStrenCodePU[1:0]	Input	VDD	Async	Enables the pull-up segments ■ 00: 400 Ohms ■ 01: 100 Ohms ■ 10: 66.6 Ohms ■ 11: 50 Ohms
ForceData_VDD2	Input	VDD2H	Async	■ Force Data – VDD2H supply level ■ When ForceEnable_VDD2 is asserted, ForceData_VDD2 value is passed to IOPAD
ForceEnable_VDD2	Input	VDD2H	Async	Force Enable – VDD2H supply level When PwrOkVDD2=0: ■ ForceEnable_VDD2=1 forces IOPAD to ForceData_VDD2 ■ ForceEnable_VDD2=0, IOPAD is tri-stated
IOPAD	InOut	VDD2H	Async	PAD
PwrOkVDD	Input	VDD	Async	PwrOk on VDD Power Supply Generated from POR cell in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down

Pin Name	Direction	Power Domain	Clock Domain	Function
PwrOkVDD2	Input	VDD2H	Async	PwrOk on VDD2H Power Supply Generated from POR cell in MASTER ■ 1: All power rails are up (VDD/VDDQ/VDD2H) ■ 0: Anyone or All power rails are down
TieHigh_VDD2	Output	VDD2H	Async	VDD2H Tie High for IMPL usage
TieLow_VDD2	Output	VDD2H	Async	VDD2H Tie Low for IMPL usage
VDD	Input	VDD	Async	Digital Logic Power Supply
VDD2H	Input	VDD2H	Async	VDD2H Power Supply
VSS	Input	0	Async	Ground

9.5 Bit Slice Components: LCDL and RXREPLICA

LCDL and RXREPLICA are full custom macros used in SE/DIFF/SEC slices.

9.5.1 LCDL (dwc_ddrphy_lcdl)

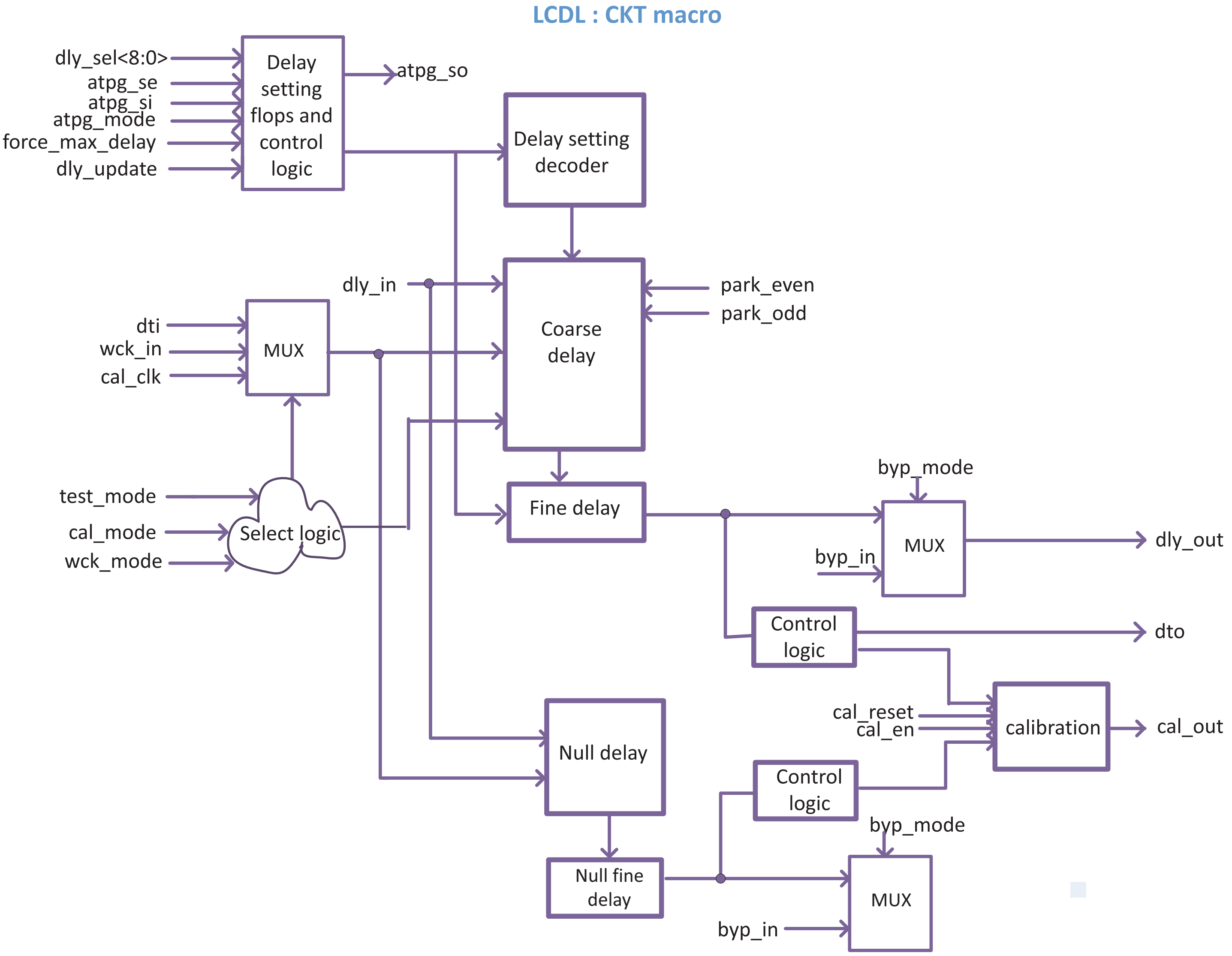
This section includes the following topics:

9.5.1.1 General Description

LCDL ("local calibrated delay line") delay cells are used in the DIFF/SE/SEC slices to achieve fractional UI timing of the DRAM interface signals and doubles the purpose in measuring the steps required for 1UI shift.

The DIFF Slice has 2 LCDL for Transmit DQS and Timing the gate for read DQS. SE Slice has 3 LCDL for Read DQSt, Read DQSc and Transmit Single ended DQ/DM or CA signal. SEC Slice has 1 LCDL for transmit Single ended signal.

Figure 9-12 LCDL : CKT macro



9.5.1.2 Pin List

The following Table shows the pin list for the LCDL macro.

Table 9-15 LCDL Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
VDD	Input	VDD	Async	Digital Logic Power Supply
VSS	Input	0	Async	Ground

dly_in	Input	VDD	Self	Delay Line Input: Input signal to be delayed
				dly_in = PClk for TX LCDLs
				dly_in = DQS_T/C for RX LCDLs
				dly_in = RxStrobeEn for RXEN LCDL

wck_in	Input	VDD	Self	Write Clock input

wck_mode	Input	VDD	-	WCK mode select for wck_in input
				wck_mode = 1'b0 => dly_out = dly_in | dti | cal_clk
				wck_mode = 1'b1 => dly_out = wck_in

dly_sel[8:0]	Input	VDD	dly_update	Delay Line Select. Sets the delay based on the bit setting.
dly_update	Input	VDD	Self	Clock for the delay line delay select (dly_sel) flops
park_even	Input	VDD	-	Input that controls parking direction for glitch-less phase update, works differentially with park_odd.
park_odd	Input	VDD	-	Input that controls parking direction for glitch-less phase update, works differentially with park_even.
dly_out	Output	VDD	dly_in/cal_clk/dti/wck_in	Delay Line Output: Output delayed by the delay selected by dly_sel. Refer to truth table Table 3
cal_mode	Input	VDD	Async	Calibration Mode: Indicates (if cal_mode is set) that the delay line is in calibration. In this mode the delay line calibrates to 1UI over VT drifts.

Pin Name	Direction	Power Domain	Clock Domain	Function
cal_clk	Input	VDD	Self	Calibration Clock: Clock whose period is measured when the delay line is in calibration mode. This clock is used to sample the calibration measure mode enable input, cal_en.
cal_en	Input	VDD	Async	Calibration Enable: Enables measurement phase for calibration. This signal is sampled by the calibration clock .
cal_reset	Input	VDD	Async	Asynchronous reset pin to reset the calibration logic

cal_out	Output	VDD	-	Calibration Output: Indicates the status of the delayed clock relative to the reference (null delay) clock.
				cal_out = 1 for delay > 1UI
				cal_out = 0 for delay < 1UI
				cal_out gets sampled by a flop clocked by DFI clock outside LCDL.

test_mode	Input	VDD	Async	Test Mode: Selects the test modes of the delay line. 0 = Mission mode or WCK or calibration mode 1 = Test mode
dti	Input	VDD	-	Test Input: Delay line input during test mode
dto	Output	VDD	dti	Test Output: Delay line output during test mode
byp_in	Input	VDD	-	Bypass mux input for bypass mode
byp_mode	Input	VDD	-	Bypass mode enable. When asserted, the input byp_in is chosen to be output at dly_out
atpg_mode	Input	VDD	-	Scan mode: when asserted, the dly_sel flops are in scan mode
atpg_se	Input	VDD	-	dly_sel flops scan chain enable
atpg_si	Input	VDD	-	dly_sel flops scan chain input
atpg_so	Output	VDD	-	dly_sel flops scan chain output
force_max_delay	Input	VDD	Async	Force dly_sel bits to high for burn-in

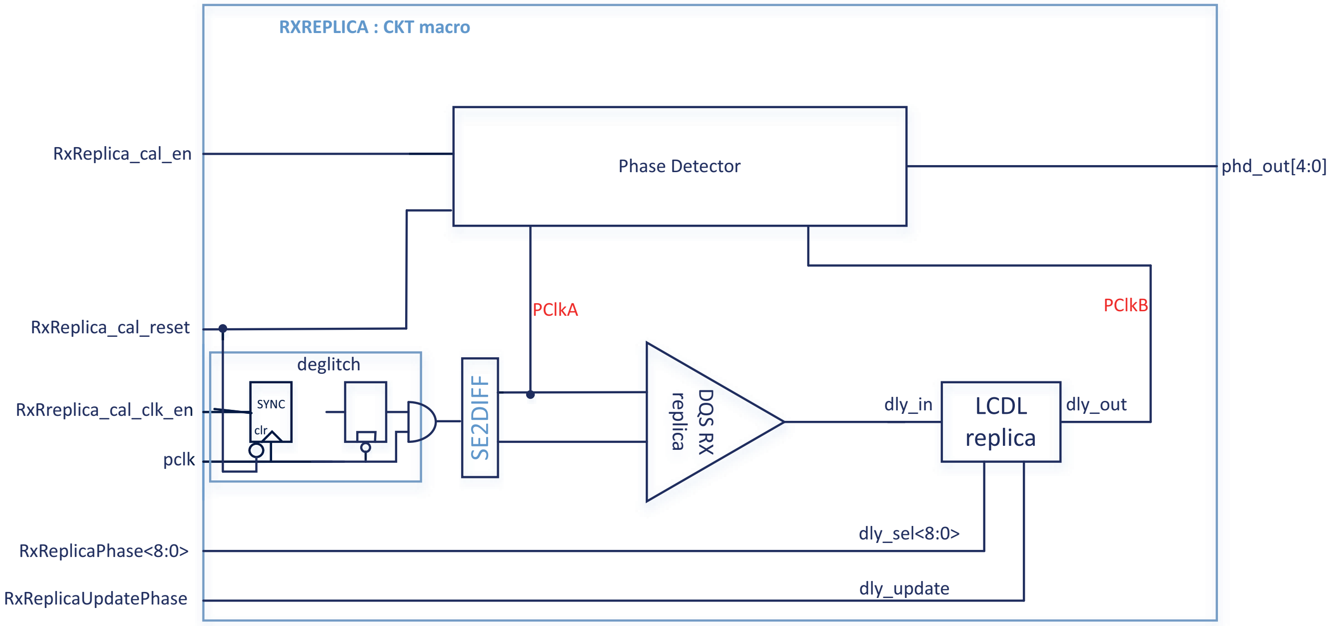
9.5.2 RXREPLICA (dwc_ddrphy_rxreplica)

This section includes the following topics:

9.5.2.1 General Description

RXREPLICA circuit macro replicates all logic elements (including IO RX and LCDL) on RDQS path from DIFF slice IO PAD pin to Rx Sampler CK pin which are susceptible to VT changes. This macro takes pclk input and passes it through a replica DQS path. The phase detectors compare the DQS+LCDL replica path delay with 1UI to 5UI and indicates which UI the path delay falls. This information is used by the PUB FSM to caliberate the DQS replica path LCDL to caliberate the path delay to the required value.

Figure 9-13 RXREPLICA Block Diagram



9.5.2.2 Pin List

The following Table shows the pin list for the RXREPLICA macro.

Table 9-16 RXREPLICA Pin List

Pin Name	Direction	Power Domain	Clock Domain	Function
VDD	Input	VDD	Async	Digital Logic Power Supply
VSS	Input	0	Async	Ground
RxReplica_cal_en	Input	VDD	DFI clk	RxReplica caliberation enable signal. Data input to phase detector flops.
RxReplica_cal_reset	Input	VDD	DFI clk	RxReplica caliberation reset for phase detector flops.

Pin Name	Direction	Power Domain	Clock Domain	Function
RxReplica_cal_clk_en	Input	VDD	DFI clk	RxReplica caliberation clock enable for pclk gating.
pclk	Input	VDD	Pclk	Input clock.
RxReplicaPhase[8:0]	Input	VDD	DFI clk	Delay select signals for replica LCDL
RxReplicaUpdatePhase	Input	VDD	DFI clk	Delay phase update signal for replica LCDL
phd_out[0:4]	Output	VDD	pclk	Phase detector outputs for 1UI to 5UI. phd_out<*> depends on the delay difference between DQS Rx + LCDL path delay compared to * UI delay. 0 – Early (DqsRx + LCDL delay < * UI)Late (DqsRx + LCDL delay > * UI)
RxReplica_RxGainCurrAdj [3:0]	Input	VDD	Async	Bias current control
RxReplica_RxDiffModeCtl[3:0]	Input	VDD	Async	Bits [1:0] are used to control current according to boost/non-boost VDD. 11 – non-boost VDD 00 – boost VDD Bits [3:2] are chicken bits for now.
RxReplica_RxBypassRcvEn	Input	VDD	Async	Enable bypass mode using mission mode receiver.
PwrOkVDD	Input	VDD	Async	This is a VDD domain signal. When this signal is high it indicates all power rails are stable. To be ORed with RxPowerDown.
RxReplica_RxPowerDown	Input	VDD	Async	Active high signal which places the receiver in powerdown mode (bias is off),

Pin Name	Direction	Power Domain	Clock Domain	Function
RxReplica_RxStandby	Input	VDD	Async	Active high signal which places the receiver in standby mode (bias is on),
RxReplica_rsm_reset	Input	VDD	Async	RSM flop reset.
RxReplica_dqsEn_arm	Input	VDD	Async	Enable the set of the rsm flop.
RxReplica_dqsEnSync	Input	VDD	clk_rsmX	Input to the rsm flop, from CMD FIFO. Controls the falling edge of readgate.
RxReplica_RxBypassDataRcvT	Output	VDD	RxClk	CMOS level data strobe output, when RxBypassEn is high. Otherwise force to low.
RxReplica_RxBypassDataRcvC	Output	VDD	RxClk	CMOS level data strobe output, when RxBypassEn is high. Otherwise force to low.
RxReplica_lcdl_park_even	Input	VDD	-	Input that controls parking direction for glitch-less phase update, works differentially with park_odd.
RxReplica_lcdl_park_odd	Input	VDD	-	Input that controls parking direction for glitch-less phase update, works differentially with park_even.
RxReplica_lcdl_cal_mode	Input	VDD	Async	Calibration Mode: Indicates (if cal_mode is set) that the delay line is in calibration. In this mode the delay line calibrates to 1UI over VT drifts.
RxReplica_lcdl_cal_clk	Input	VDD	Self	Calibration Clock: Clock whose period is measured when the delay line is in calibration mode. This clock is used to sample the calibration measure mode enable input, cal_en.
RxReplica_lcdl_cal_en	Input	VDD	Async	Calibration Enable: Enables measurement phase for calibration. This signal is sampled by the calibration clock .
RxReplica_lcdl_cal_reset	Input	VDD	Async	Asynchronous reset pin to reset the calibration logic

Pin Name	Direction	Power Domain	Clock Domain	Function

RxReplica_lcdl_cal_out	Output	VDD	-	Calibration Output: Indicates the status of the delayed clock relative to the reference (null delay) clock.
				cal_out = 1 for delay > 1UI
				cal_out = 0 for delay < 1UI
				cal_out gets sampled by a flop clocked by DFI clock outside LCDL.

RxReplica_lcdl_test_mode	Input	VDD	Async	Test Mode: Selects the test modes of the delay line. 0 = Mission mode or WCK or calibration mode 1 = Test mode
RxReplica_lcdl_dti	Input	VDD	-	Test Input: Delay line input during test mode
RxReplica_lcdl_dto	Output	VDD	dti	Test Output: Delay line output during test mode
RxReplica_lcdl_byp_in	Input	VDD	-	Bypass mux input for bypass mode
RxReplica_lcdl_byp_mode	Input	VDD	-	Bypass mode enable. When asserted, the input byp_in is chosen to be output at dly_out
RxReplica_lcdl_atpg_mode	Input	VDD	-	Scan mode: when asserted, the dly_sel flops are in scan mode
RxReplica_lcdl_atpg_se	Input	VDD	-	dly_sel flops scan chain enable
RxReplica_lcdl_atpg_si	Input	VDD	-	dly_sel flops scan chain input
RxReplica_lcdl_atpg_so	Output	VDD	-	dly_sel flops scan chain output
RxReplica_lcdl_force_max_delay	Input	VDD	Async	Force dly_sel bits to high for burn-in

10

Layout Design Guidelines

This chapter discusses the following topics concerning the Synopsys DWC AP LPDDR5/4/4x PHY and its foundry dependent layout constraints:

- "Overview" on page 292
- "PCLK Construction" on page 293
- "Hard Macro Abutment and Spacing Requirements" on page 296
- "RxStrobeT/C Construction" on page 303
- "VrefDacRef Construction" on page 304
- "PwrOkVDD/PwrOkVDD2 Construction" on page 305
- "Layout Exceptions" on page 306
- "MIMCAP Support" on page 308
- "Required Bump Connection Resistance and Capacitance Limits" on page 309

10.1 Overview

This guideline chapter describes the placement of the hard macros and the connection of their top-level routing.

10.2 PCLK Construction

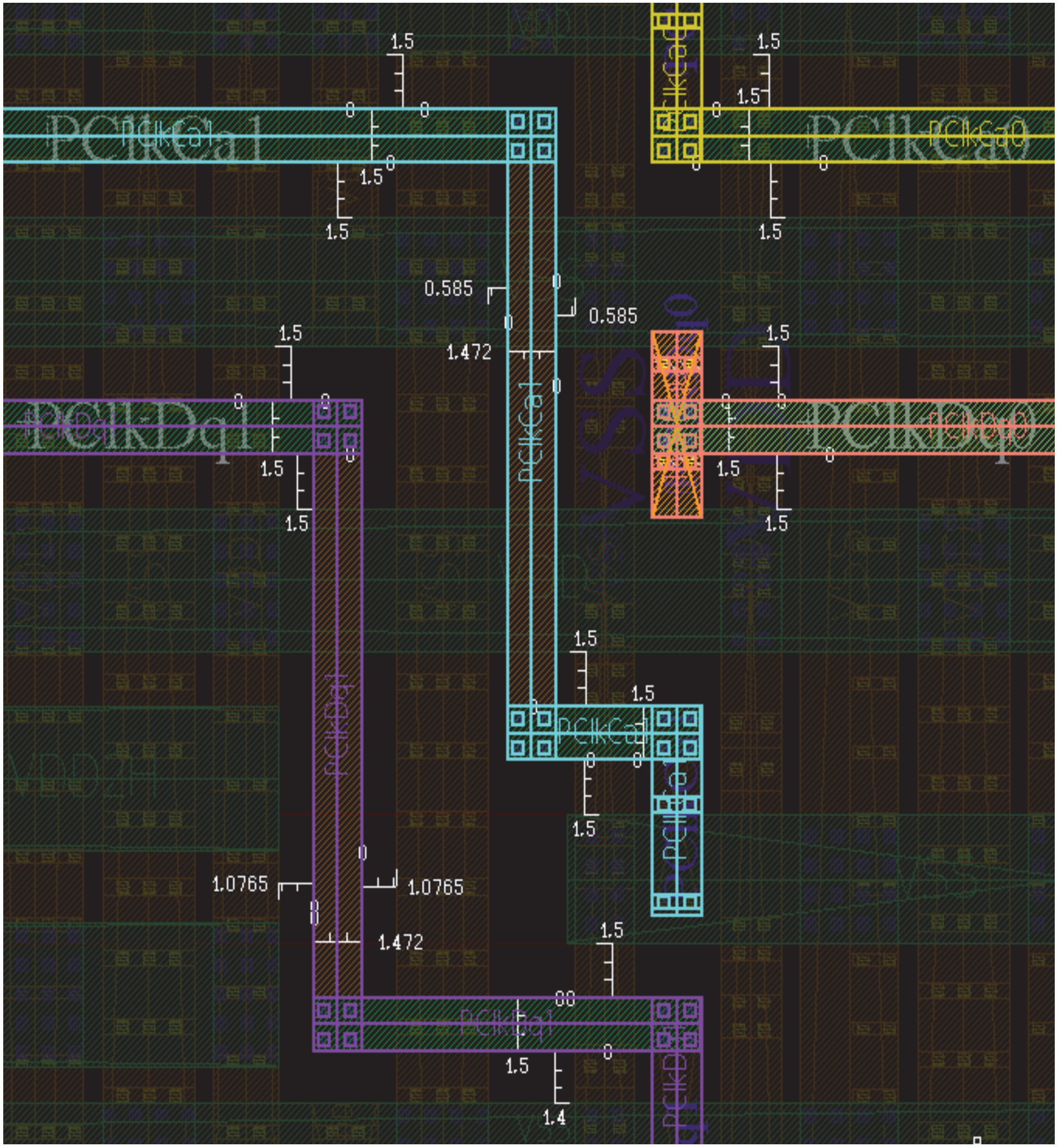
The PCLK performance varies by process and metal stack. The following table outlines the constraints for PCLK and its shielding. Detailed information regarding PCLK Construction is available in the LPDDR5/4/4x PHY Implementation Guide, section PCLK Network Construction Parameters.

The following table is applicable to both NS and EW orientations.

Table 10-1 PCLK Parameters

Parameter	PclkCa0/PclkCa1	PclkDq0/PclkDq1	Unit
Route Width	1.5	1.5	um
Shield Width	1.5	1.5	um
Route to Shield Spacing	1.5	1.5	um
Maximum Length: master to repeater	850	850	um
Maximum Length: repeater to farthest DBYTE	1030	1030	um
Maximum MTOP to MTOP-1 transitions	2	2	

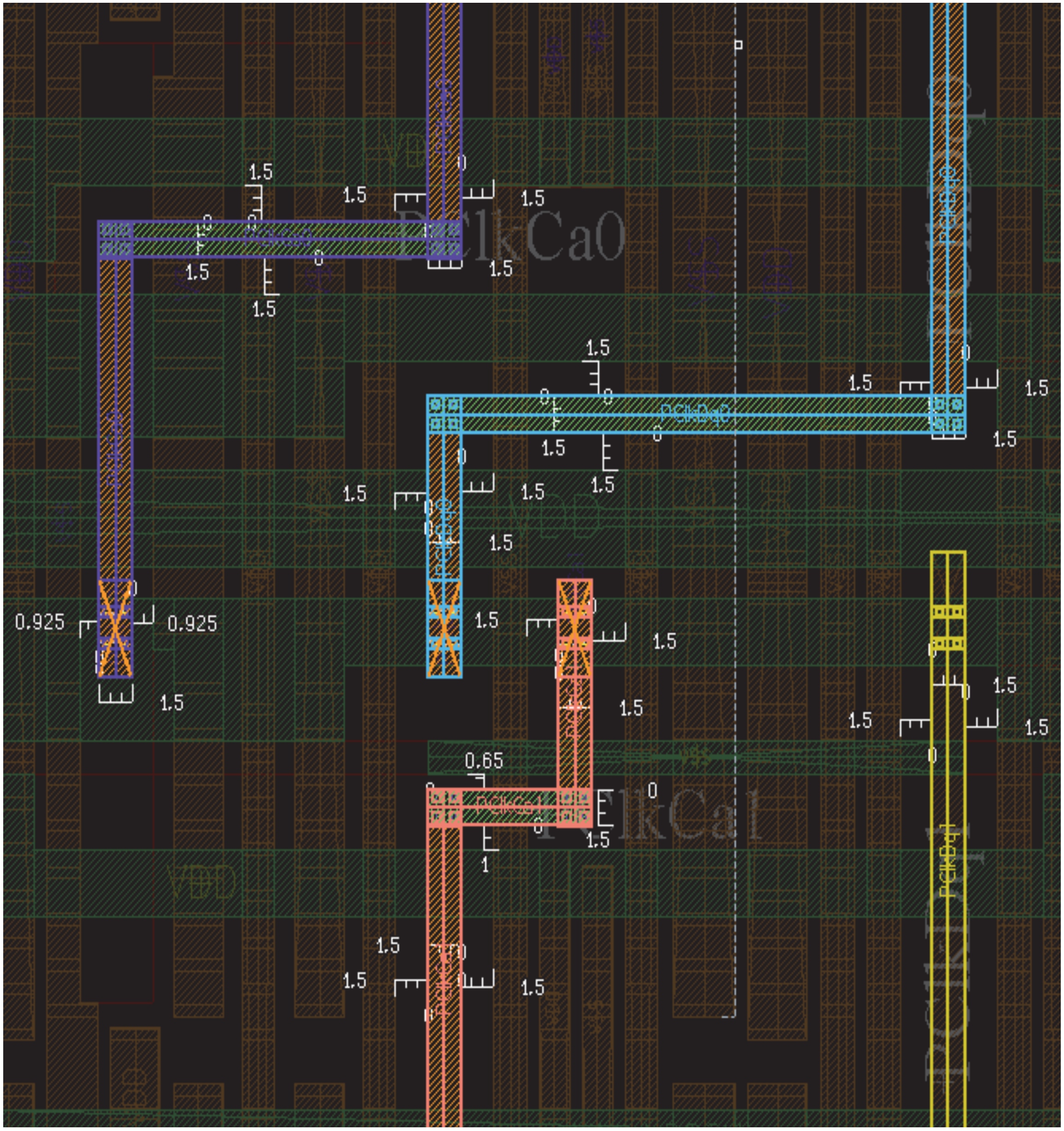
Figure 10-1 PCLK Exceptions NS Orientation



Pclk Exception in master NS

- Pclk* horizontal MTOP routing to shield spacing is 1.4
- Pclk* vertical MTOP-1 routing to shield spacing is 0.585
- Pclk* vertical MTOP-2 width is 1.472

Figure 10-2 PCLK Exceptions EW Orientation



Pclk Exception in master EW

- Pclk* horizontal MTOP routing to shield spacing is 0.65
- Pclk* vertical MTOP-1 routing to shield spacing is 0.925

Note Breaking a PCLK route to switch from MTOP to MTOP-1 or MTOP-1 to MTOP is considered a transition

10.3 Hard Macro Abutment and Spacing Requirements

This section documents the supported abutments for the DBYTE and AC which are constructed using hard-macros and utility blocks.

It describes the following:

- Allowed orientations and abutments each hard macro orientation can support.
- Spacing required from the hard macros to adjacent IP or standard cell regions to ensure a latch-up free implementation

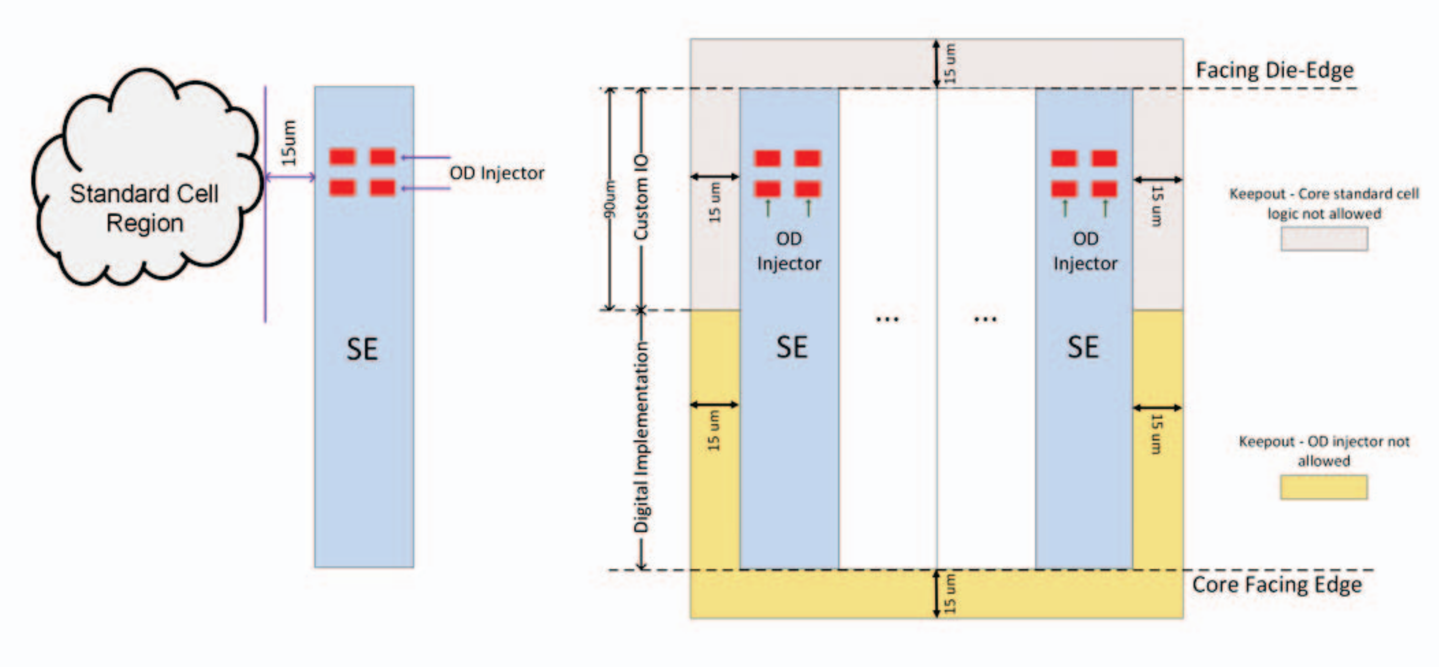
10.3.1 Legal Hard Macro Abutments

Detailed information regarding legal hard-macro abutments is available in the LPDDR5/4/4x PHY Implementation Guide, section Hard-Macro Abutments

10.3.2 Spacing Requirements NS Orientation

There is no macro to macro spacing requirement. The only spacing requirement is the SE to standard cell region to ensure a latch-up free implementation. This is illustrated in the Figure 10-3.

Figure 10-3 SE to standard cell region spacing requirement



A spacing of 15 um between the SE and the standard cell region is necessary to meet the following rule:

- LUP.2.4 : OD injector {INTERACT {HIADMY OR SR_ESD}} to the IP boundary distance is required to be larger than or equal to 15 um (LUP.2.4 would be checked by turning on 'ESDLU_IP_TIGHT-EN_DENSITY') Exception: a. If OD injector is covered by LUPIEDMY, LUP.2.4 can be excluded. (It is not recommended to use this layer before silicon proven) >= 15

Placement of multiple ENDCELLs abutting to the SE will ensure that 15um spacing is met from OD injector to the standard cell region as shown in Figure 10-3.

Figure 10-4 Placement of ENDCELL

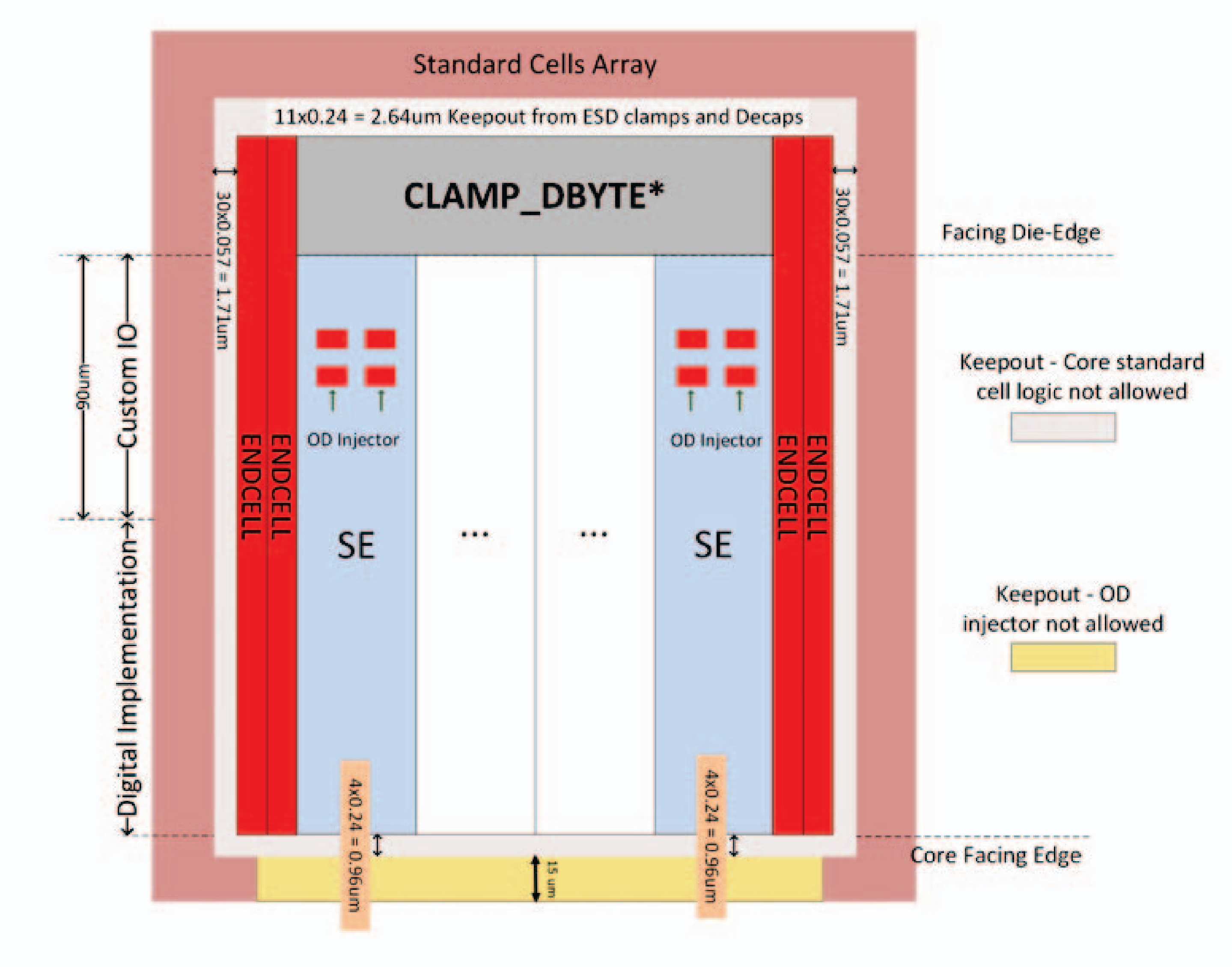


Figure 10-5 MASTER hard-macro to standard cell region spacing requirement

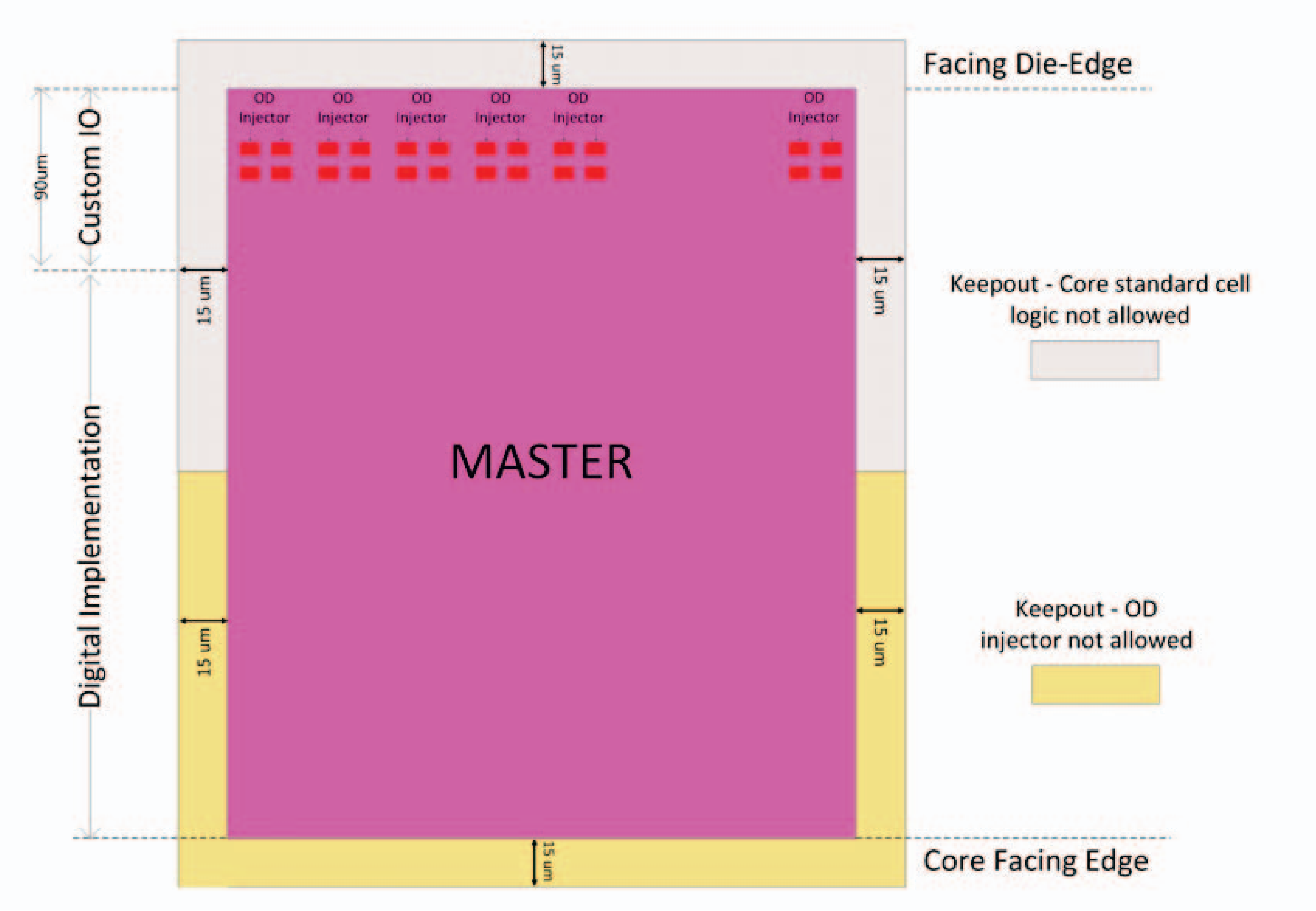
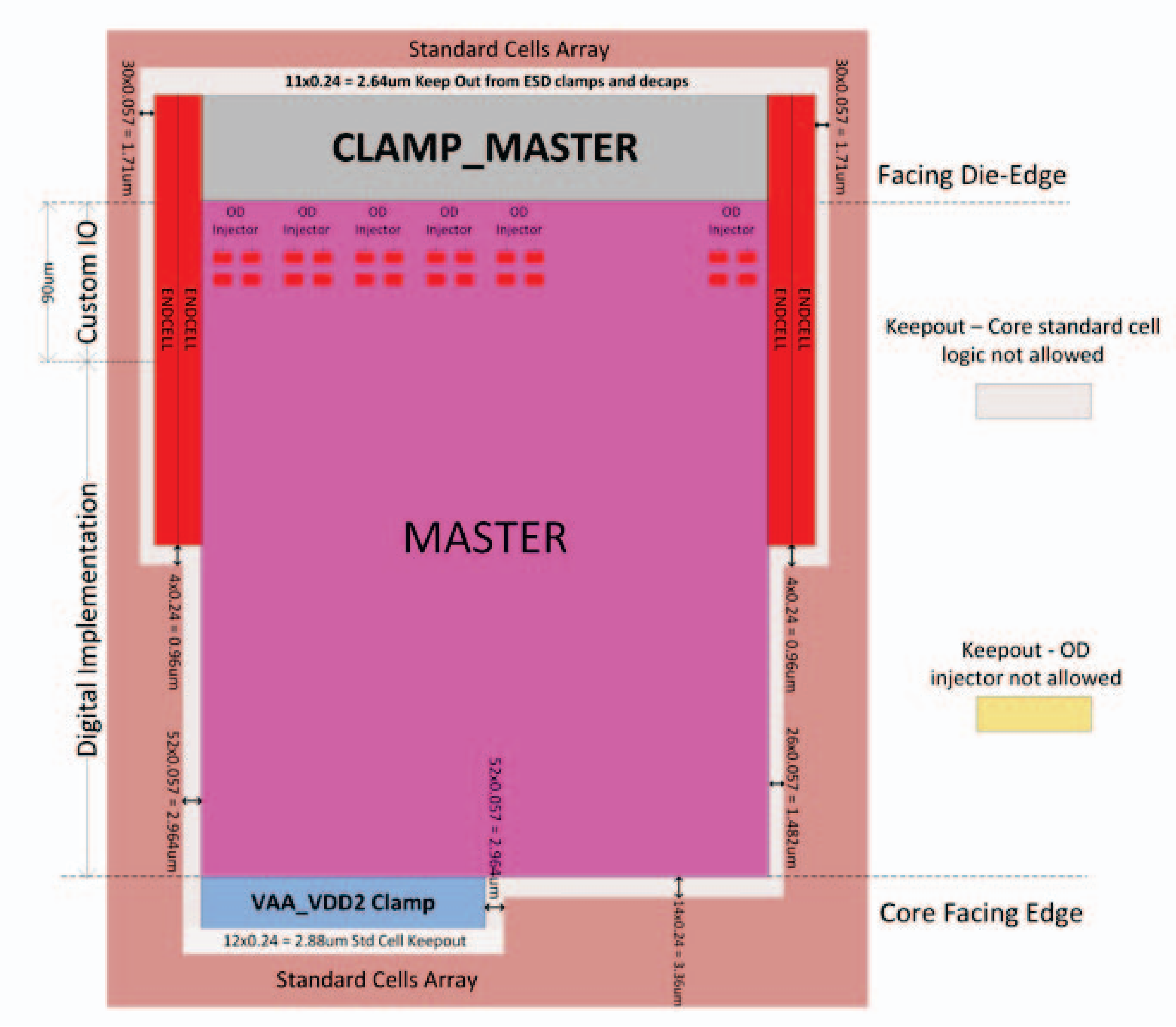


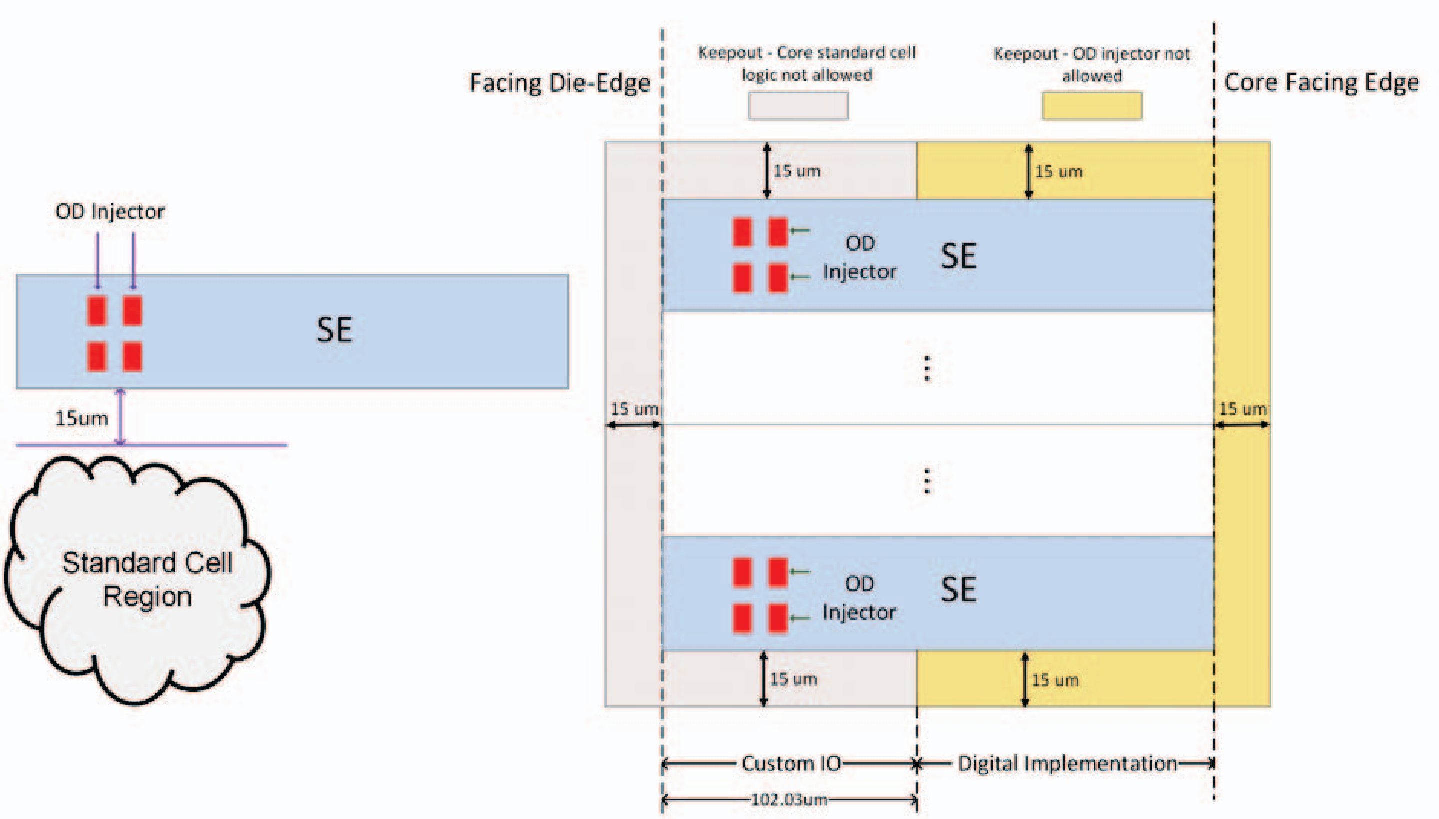
Figure 10-6 Placement of ENDCELL abutted to MASTER hard-macro



10.3.3 Spacing Requirements EW Orientation

There is no macro to macro spacing requirement. The only spacing requirement is the SE to standard cell region to ensure a latch-up free implementation. This is illustrated in the Figure 10-3 on page 296.

Figure 10-7 SE to standard cell region spacing requirement



A spacing of 15 um between the SE and the standard cell region is necessary to meet the following rule:

- LUP.2.4 : OD injector {INTERACT {HIADMY OR SR_ESD}} to the IP boundary distance is required to be larger than or equal to 15 um (LUP.2.4 would be checked by turning on 'ESDLU_IP_TIGHT-EN_DENSITY') Exception: a. If OD injector is covered by LUPIEDMY, LUP.2.4 can be excluded. (It is not recommended to use this layer before silicon proven) >= 15

Placement of multiple ENDCELLs abutting to the SE will ensure that 15um spacing is met from OD injector to the standard cell region as shown in Figure 10-7.

Figure 10-8 Placement of ENDCELL

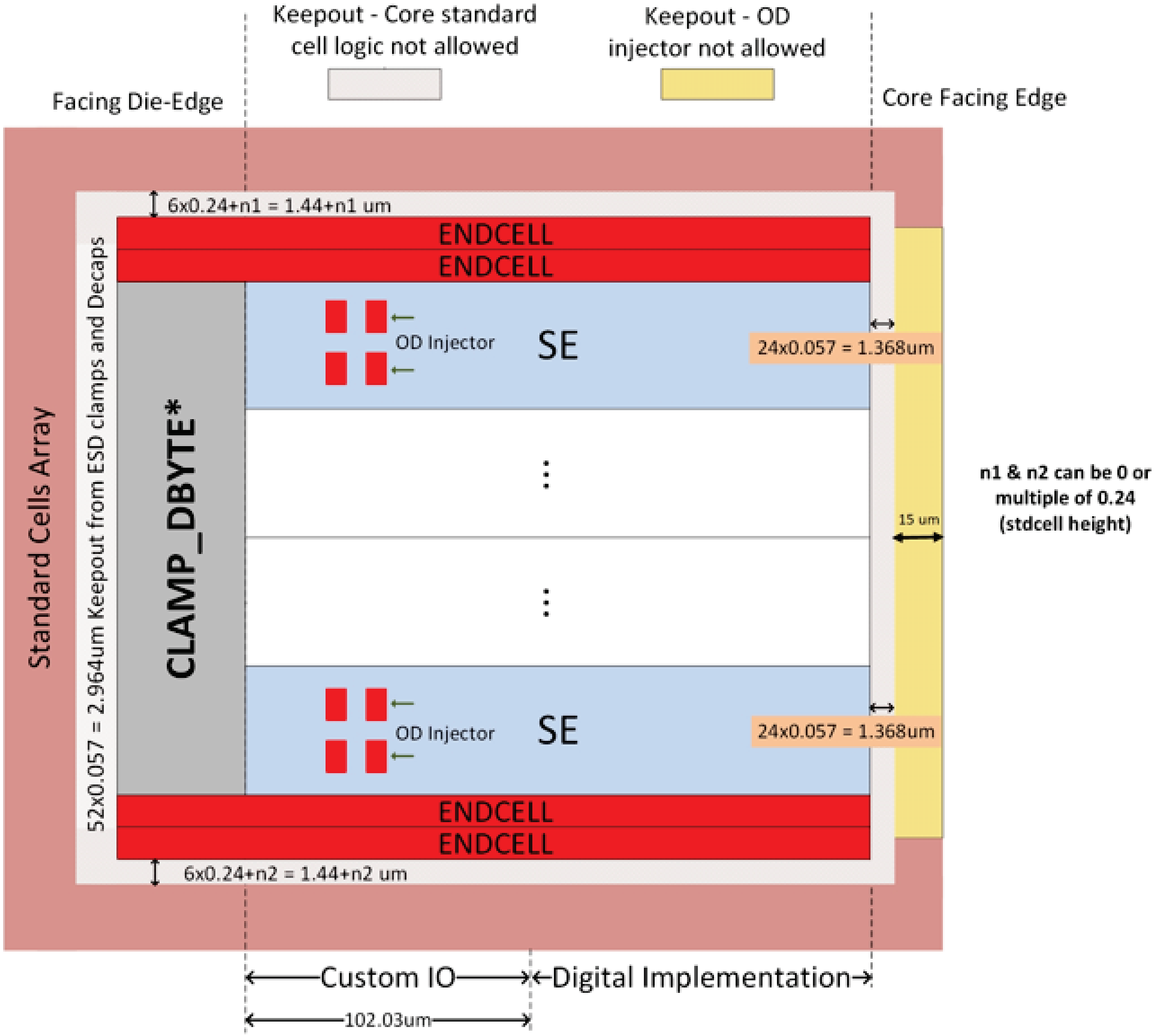
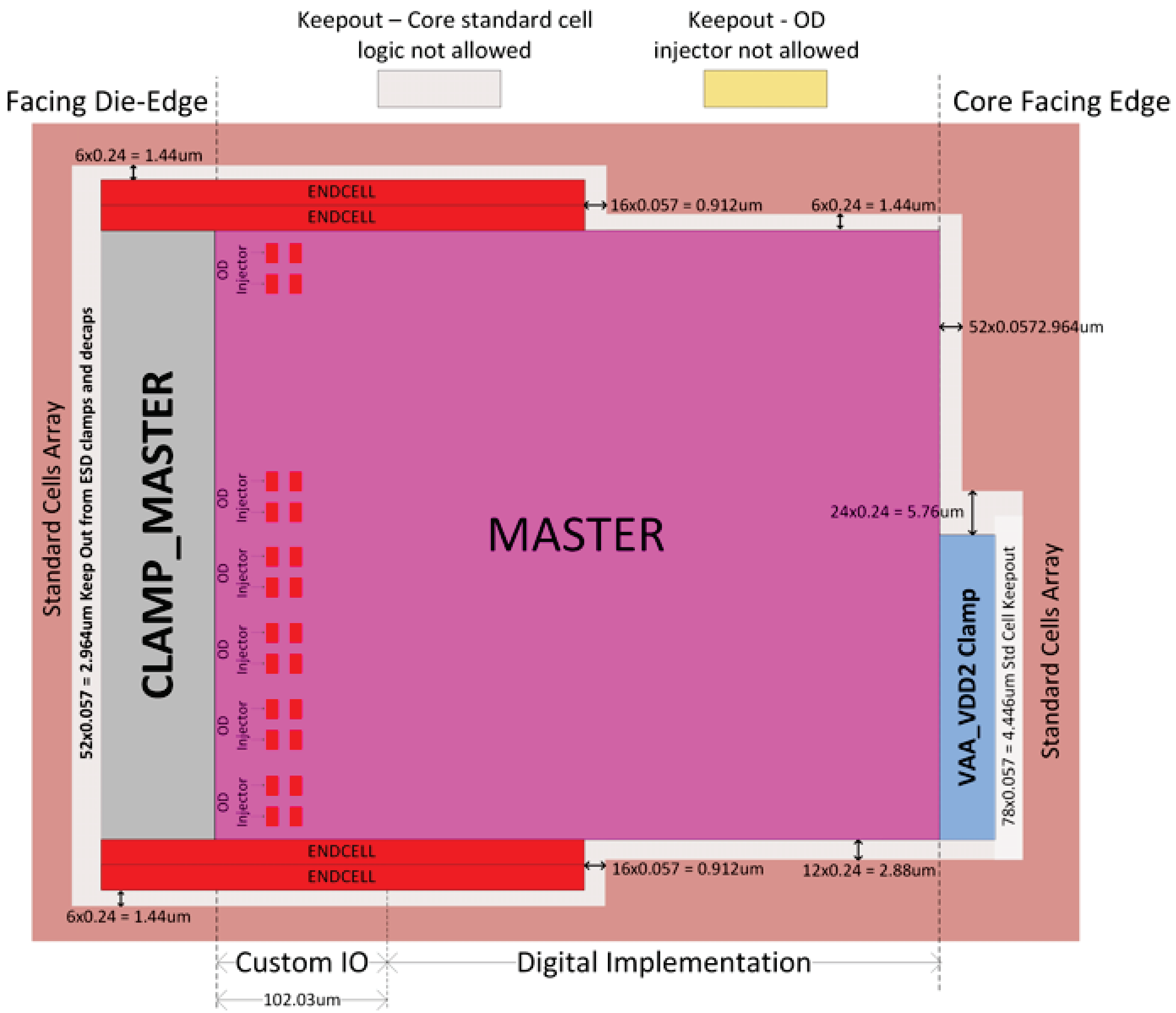


Figure 10-9 Placement of ENDCELL abutted to MASTER hard-macro



10.4 RxStrobeT/C Construction

The RxStrobeT/C performance varies by process and metal stack. The following table outlines the constraints for RxStrobeT/C and its shielding. Detailed information regarding RxStrobeT/C Construction is available in the LPDDR5/4/4x PHY Implementation Guide, section RxStrobeT/C Network Construction Parameters.

Table 10-2 RxStrobeT/C Parameters NS Orientation

Parameter	RxStrobeT	RxStrobeC	Unit
Route Width	1.5	1.5	µm
Shield Width	1.5	1.5	µm
Route to Shield Spacing	1.5	1.5	µm
RxStrobeT to RxStrobeC Spacing	1.5	1.5	µm
Maximum Length*	510	510	µm
Maximum MTOP to MTOP-1 transitions	2	2	

Table 10-3 RxStrobeT/C Parameters EW Orientation

Parameter	RxStrobeT	RxStrobeC	Unit
Route Width	1.5	1.5	µm
Shield Width	2.1	2.1	µm
Route to Shield Spacing	1.5	1.5	µm
RxStrobeT to RxStrobeC Spacing	1.5	1.5	µm
Maximum Length*	470	470	µm
Maximum MTOP to MTOP-1 transitions	2	2	

10.5 VrefDacRef Construction

The VrefDacRef performance varies by process and metal stack. The following table outlines the constraints for VrefDacRef and its shielding. Detailed information regarding VrefDacRef Construction is available in the LPDDR5/4/4x PHY Implementation Guide, section VrefDacRef Network Construction Parameters.

The following table is applicable to both NS and EW orientations.

Table 10-4 VrefDacRef Parameters

Parameter	VrefDacRef	Unit
Route Width	3.0	µm
Shield Width	0.5	µm
Route to Shield Spacing	0.75	µm
Maximum Length	3640	µm
Maximum MTOP to MTOP-1 transitions	1	

10.6 PwrOkVDD/PwrOkVDD2 Construction

The PwrOkVDD/PwrOkVDD2 performance varies by process and metal stack. The following table outlines the constraints for PwrOkVDD/PwrOkVDD2 and its shielding. Detailed information regarding PwrOkVDD/PwrOkVDD2 Construction is available in the LPDDR5/4/4x PHY Implementation Guide, section PwrOkVDD/PwrOkVDD2 Network Construction Parameters.

Table 10-5 PwrOkVDD/PwrOkVDD2 Parameters NS Orientation

Parameter	PwrOkVDD	PwrOkVDD2	Unit
Route Width	0.5	0.5	µm
Shield Width	0.5	0.5	µm
Route to Shield Spacing	0.5	0.5	µm
Maximum Length	1410	2420	µm
Maximum MTOP to MTOP-1 transitions	2	2	

Table 10-6 PwrOkVDD/PwrOkVDD2 Parameters EW Orientation

Parameter	PwrOkVDD	PwrOkVDD2	Unit
Route Width	0.6	0.6	µm
Shield Width	0.6	0.6	µm
Route to Shield Spacing	0.6	0.6	µm
Maximum Length	1565	2575	µm
Maximum MTOP to MTOP-1 transitions	2	2	

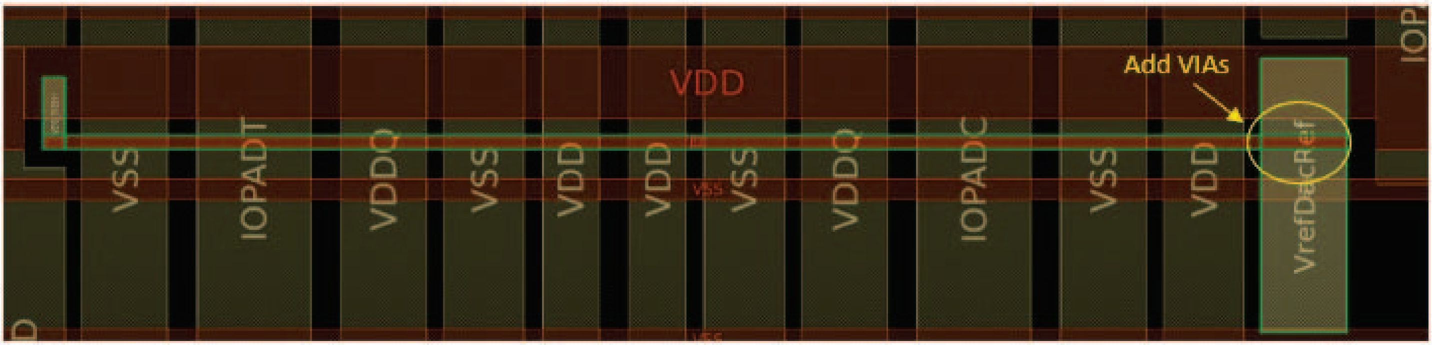
10.7 Layout Exceptions

This section documents areas of the PHY that may deviate from instructions provided by the Implementation Guide.

10.7.1 VrefDacRef pins in DIFF/SE hard-macro

The following figures are exceptions for this technology node to the “lp54cs2dq18ch2 build – VrefDacRef Implementation” section within the Implementation Guide.

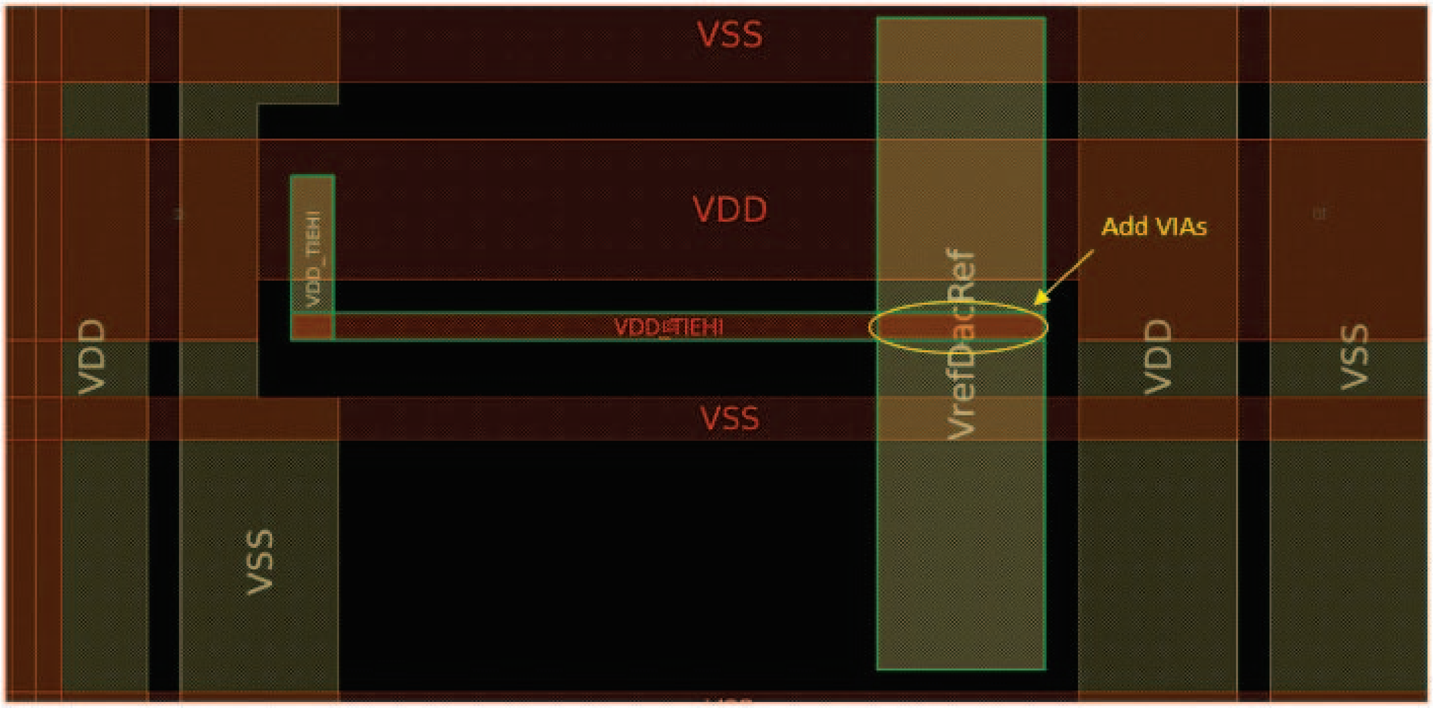
Figure 10-10 DIFF NS exception to Figure 11-48 Example snapshot of SE/DIFF EW hard-macro illustrating VrefDacRef pins



Additional VIAs (as opposed to jumpers) are required to connect VDD_TIEHI and VrefDacRef:

- The VDD_TIEHI port has 2 terminals on MTOP-1 and MTOP.
- The VrefDacRef port has 1 terminal on MTOP-1.

Figure 10-11 SE NS exception to Figure 11-48 Example snapshot of SE/DIFF EW hard-macro illustrating VrefDacRef pins



Additional VIAs (as opposed to jumpers) are required to connect VDD_TIEHI and VrefDacRef:

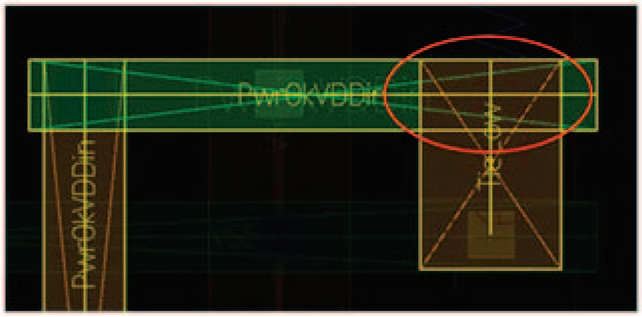
- The VDD_TIEHI port has two terminals on MTOP-1 and MTOP
- The VrefDacRef port has one terminal on MTOP-1

10.7.2 RPT*CH Pclk Repeater TieLow/TieHigh Connection in NS orientation

For the NS Repeaters, the connections available for the PwrOkVDDin and PclkIn* can be done to only TieLow by dropping VIATOPs as shown in Figure 10-12, Figure 10-13, and Figure 10-14.

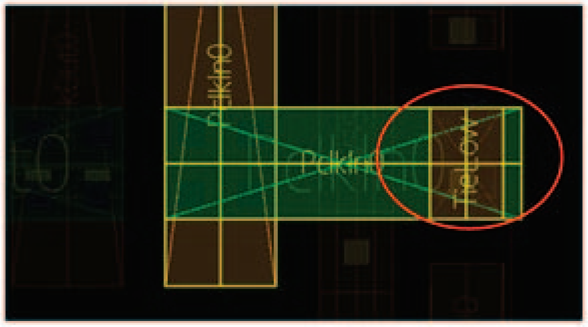
TieLow on MTOP-1 can be connected to PwrOkVDDin on MTOP by just adding VIATOP on their intersection as shown in Figure 10-12.

Figure 10-12 PwrOkVDDin Connection



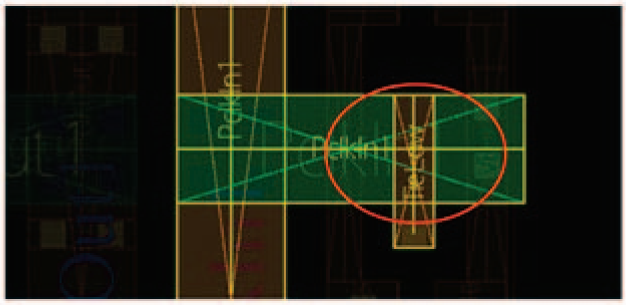
TieLow on MTOP-1 can be connected to Pclkin0 on MTOP by just adding VIATOP on their intersection as shown in Figure 10-13.

Figure 10-13 Pclkin0 Connection



TieLow on MTOP-1 can be connected to Pclkin1 on MTOP by just adding VIATOP on their intersection as shown in Figure 10-14.

Figure 10-14 Pclkin1 Connection



10.8 MIMCAP Support

The LPDDR5/4x/4 PHY in TSMC7FF does not support MIMCAP. Please contact Synopsys for questions about MIMCAP support.

10.9 Required Bump Connection Resistance and Capacitance Limits

The following table provide resistance and capacitance limits for bump connections per metal stacks listed in the “Process Information” on page 43.

The following table is applicable to both NS and EW orientations.

Table 10-7 Required bump connection resistance and capacitance limits

Pin Name	Maximum Resistance	Recommended Maximum Capacitance	Notes
BP_DFI	1.5 Ohms	210 fF (target)	
	1.5 Ohms	210 fF (spec)	1

1. The BP_DFI* capacitive load recommendation is to achieve optimal performance. Excessive capactive loading will erode performance.

11

Automotive Grade 2 Support

This chapter discusses the following topics concerning the Synopsys DWC AP LPDDR5/4/4x PHY Automotive Support:

11.1 Automotive Grade 2 Compliance

Synopsys' Automotive Grade 2 IP is designed to support applications requiring ISO 26262 ASIL B and AEC Q100 Grade 2. This assumes that the integrity of the IP is maintained during implementation of the host SoC, Package, and PCB/System.

11.2 PHY Features

- AEC Q100 qualified Automotive Grade 2 (AP)

11.3 Automotive Support

11.3.1 ISO 26262

In order to make an IP product better suited for applications in the automotive space, functional safety needs to be considered throughout the IP development process. ISO 26262 addresses functional safety, and requires the HW components to be analyzed with respect to their ability to detect and/or control the effects of random hardware faults. Random hardware faults can occur at any point in time during the life-cycle of the HW component. They can take the form of permanent faults, or transient faults, and require safety mechanisms to be in place to ensure that severe consequences do not occur as a result of those faults.

11.3.2 ASIL B Ready Certification

The DDR PHY IP has been analyzed in the scope of ISO 26262 targeting ASIL B.Users of the PHY should understand that the ASIL B Ready status is dependent on external safety features (i.e. External Measures) supplied by the controller or the SoC. These External Measures are described in the accompanying Safety Manual.

11.3.3 FMEDA

As part of the ASIL B Ready analysis, a Failure Mode, Effects, and Diagnostic Analysis (FMEDA) analysis has been performed for the DDR PHY IP. The analysis utilizes a per-transistor failure rate derived in accordance to IEC TR -62380. This, in conjunction with transistor count information allows one to determine the failure rate for the IP which can then be distributed between the modules of the design according to their relative area.

Safety Goals are defined for the IP. A list of failure modes and their effects is derived for each module and each of the failure modes is assigned a portion of the failure rate of the module they belong to. Failure modes are reviewed in the context of which Safety Goals they may cause to be violated, and if the violation is of type single-point or multi-point. If there is a diagnostic capability for each failure mode a Diagnostic Coverage number is assigned. The process is repeated for all failure modes and finally results are accumulated and IP safety metrics are collected in the FMEDA.

11.3.4 Implementation Requirements

This IP supports AEC Q100 CDM Class C4A and supports an SoC being tested to CDM Class C4B—assuming the signals of this IP are not assigned to corner pins/balls of the package. The AEC Q100 rating of CDM Class C4B is applicable to the SoC and is related specifically to 750V support at the corner pins/balls.

This IP is not intended to support 750V CDM. You should not assign signals of this IP to corner pins/balls of the SoC package. However, the corner pins/balls of the SoC package can be unconnected, unpopulated, or assign them to another function of the SoC or supply of the SoC, such as a ground plane.

11.4 EM Conditions for Automotive

11.4.1 Electromigration

Electromigration for Automotive Grade 2 IP in TSMC7FF process is evaluated at a base Junction Temperature of 105 °C utilizing TSMC's Automotive EM rules as applicable to Synopsys' Grade 2 Automotive Mission Profile.

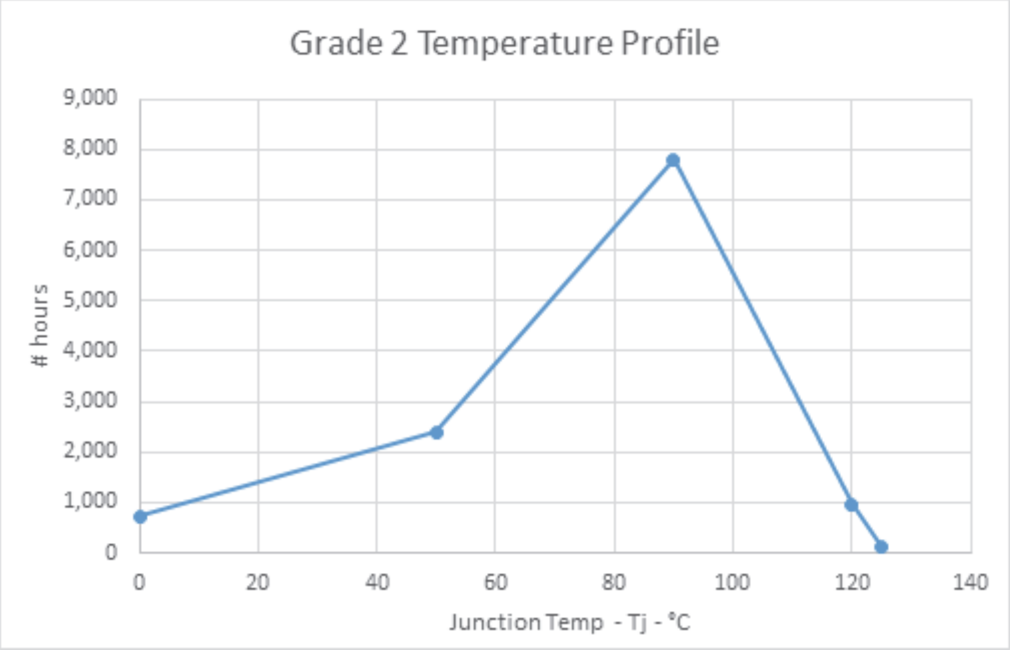
11.4.2 Synopsys' Automotive Mission Profile: Grade 2 (AP)

The following table show the Junction Temperature, TJ, vs Operating Hours profile used as the Mission Profile for the Grade 2 IP product. The junction temperature includes the effects of package thermal resistance.

Table 11-1 Synopsys' Grade 2 Mission Profile

Synopsys Grade 2 Profile	
Junction Temperature (°C)	**Operating Hours (hrs)**
0	720
50	2,400
90	7,800
120	960
125	120
Total	12,000

Figure 11-1 Synopsys' Grade 2 Temperature Profile


Grade 2 Temperature Profile
# hours
Junction Temp - Tj - °C