Micron 140s migration quick note

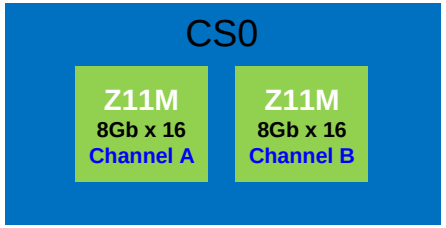
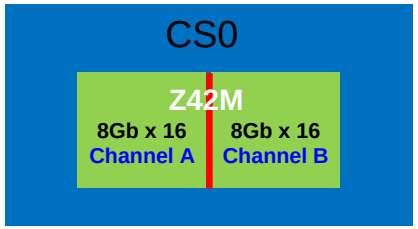
- Refresh Related

Don’t use in 1-alpha or beyond	140s Supported
“4x refresh” even if temperature is low	2x refresh lowest
Postpone or pull-in 8 refresh commands	Postpone or pull-in 4 refresh commands
Max refresh interval 9 x 2 x tREFI	Max refresh interval 5 x 2 x tREFI
	MR0[0] read out value = 1
	MR4[2:0] read out value remove 001
Recommend to set refresh rate depends on MR4 read out value, and then the refresh will be no risk.	

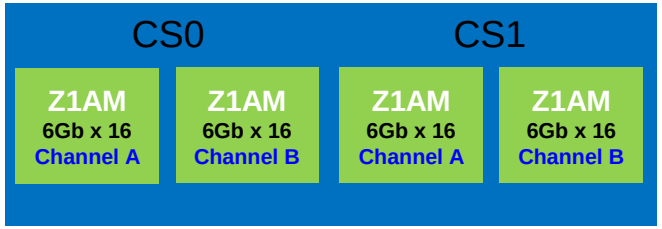
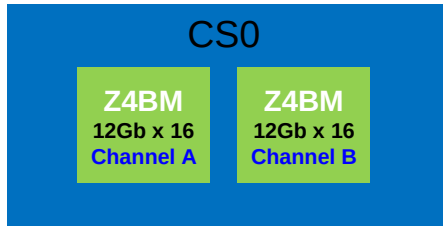
- Other check points (For Z1AM QDP to Z4BM DDP, Z32M DDP to Z42M DDP)
  - How Soc supports Channels and Ranks
  - How Soc supports 16-bit or 17-bit row addressing

Details

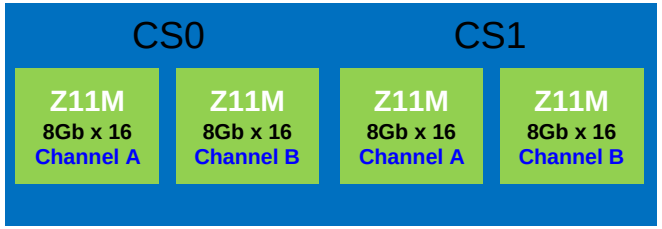
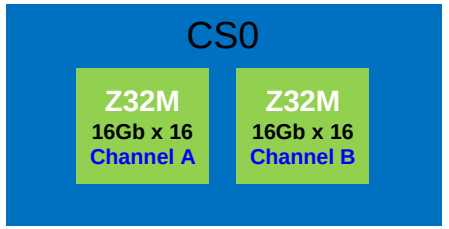
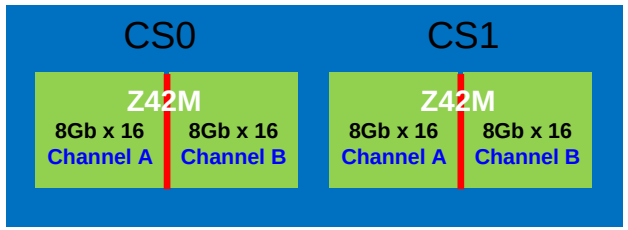
16Gb 200b x32

	Z11M DDP	Z42M SDP
Configuration		
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	1	1
Num Active Die Per x32 Access	2	1
Die Architecture	x16 8Gb single-channel die	x32 16Gb dual-channel die
Row Addressing	R[15:0]	R[15:0]
MR0 OP[2,0]	00b	01b
MR6 OP[7:0]	0000 0000b	0000 0111b
MR8 OP[5:2]	0100b	0100b
Num RZQ	1	1
Package Options	DS, DT, (Existing pkg) FW (Improved pkg)	FW (Improved pkg)
tRFC	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns
Refresh Rates	See Table 1 & Table 2	
MR4 Code	See Table 3	

24Gb 200b x32

	Z1AM QDP	Z4BM DDP
Configuration		
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	2	1
Num Active Die Per x32 Access	2	2
Die Architecture	x16 6Gb single-channel die	x16 12Gb single-channel die
Row Addressing	R[15:0]	R[16:0]
MR0 OP[2,0]	00b	01b
MR6 OP[7:0]	0000 0100b	TBD
MR8 OP[5:2]	0011b	0101b
Num RZQ	2	1
Package Options	DT (Existing pkg), DE (Improved pkg)	DE (Improved pkg)
tRFC	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns
Refresh Rates	See Table 1 & Table 2	
MR4 Code	See Table 3	

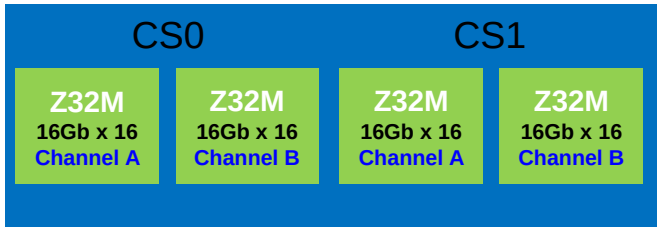
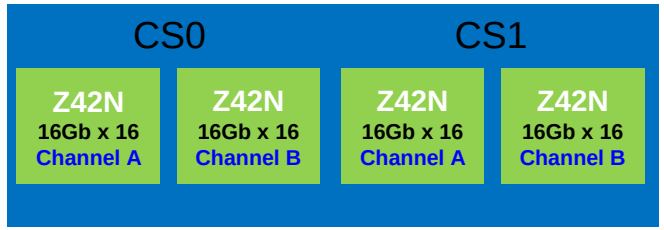
32Gb 200b x32

	Z11M QDP	Z32M DDP	Z42M DDP
Package Configuration			
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	2	1	2
Num Active Die Per x32 Access	2	2	1
Die Architecture	x16 8Gb single-channel die	x16 16Gb single-channel die	x32 16Gb dual-channel die
Row Addressing	R[15:0]	R[16:0]	R[15:0]
MR0 OP[2,0]	00b	00b	01b
MR6 OP[7:0]	0000 0000b	0000 0110b	0000 0111b
MR8 OP[5:2]	0100b	0110b	0100b
Num RZQ	2	1	2
Package Options	DT (Existing pkg)	FW (Improved pkg)	FW (Improved pkg)
tRFC	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns
Refresh Rates	See Table 1 & Table 2		
MR4 Code	See Table 3		

48Gb 200b x32

	Z2BM QDP	Z3BM QDP	Z4BM QDP
Package Configuration	CS0: Z2BM 12Gb x 16 Channel A; Z2BM 12Gb x 16 Channel B — CS1: Z2BM 12Gb x 16 Channel A; Z2BM 12Gb x 16 Channel B	CS0: Z3BM 12Gb x 16 Channel A; Z3BM 12Gb x 16 Channel B — CS1: Z3BM 12Gb x 16 Channel A; Z3BM 12Gb x 16 Channel B	CS0: Z4BM 12Gb x 16 Channel A; Z4BM 12Gb x 16 Channel B — CS1: Z4BM 12Gb x 16 Channel A; Z4BM 12Gb x 16 Channel B
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	2	2	2
Num Active Die Per x32 Access	2	2	2
Die Architecture	x16 12Gb single-channel die	x16 12Gb single-channel die	x16 12Gb single-channel die
Row Addressing	R[16:0]	R[16:0]	R[16:0]
MR0 OP[2,0]	00b	00b	01b
MR6 OP[7:0]	0000 0101b	0000 0110b	TBD
MR8 OP[5:2]	0101b	0101b	0101b
Num RZQ	2	2	2
Package Options	DT (Existing pkg)	DE (Improved pkg)	DE (Improved pkg)
tRFC	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns
Refresh Rates	See Table 1 & Table 2		
MR4 Code	See Table 3		

64Gb 200b x32

	Z32M QDP	Z42N QDP
Configuration		
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	2	2
Num Active Die Per x32 Access	2	2
Die Architecture	x16 16Gb single-channel die	x16 16Gb single-channel die
Row Addressing	R[16:0]	R[16:0]
MR0 OP[2,0]	00b	01b
MR6 OP[7:0]	0000 0110b	TBD
MR8 OP[5:2]	0110b	0110b
Num RZQ	2	2
Package Options	DT (Existing pkg) DE (Improved pkg)	DE (Improved package)
tRFC	tRFCab/pb = 280ns/140ns	tRFCab/pb = 280ns/140ns
Refresh Rates	See Table 1 & Table 2	
MR4 Code	See Table 3	

8Gb 200b x32

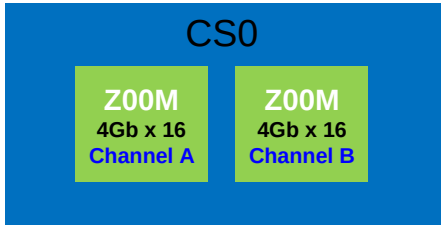
	Z00M DDP	Z41M SDP
Configuration		
I/O Interface	x32 (Two x16 channels)	x32 (Two x16 channels)
Num Rank	1	1
Num Active Die Per x32 Access	2	1
Die Architecture	x16 4Gb single-channel die	x32 8Gb dual-channel die
Row Addressing	R[14:0]	R[14:0]
MR0 OP[2,0]	00b	01b
MR6 OP[7:0]	0000 0011b	TBD
MR8 OP[5:2]	0010b	0010b
Num RZQ	1	1
Package Options	DS(Existing pkg), FW (Improved pkg)	FW (Improved pkg)
tRFC	tRFCab/pb = 180ns/90ns	TBD
Refresh Rates	See Table 1 & Table 2	
MR4 Code	See Table 3	

Table 1: Refresh Rates & Modes Across 100s-140s

MR4 OP[2:0]	Refresh Rate	100s/110s/120s			130s			140s		
		Distributed Refresh	Burst Refresh		Distributed Refresh	Burst Refresh		Distributed Refresh	Burst Refresh	
			Legacy Mode	Modified Mode		Legacy Mode	Modified Mode		Legacy Mode	Modified Mode
000b	Low temp limit	N/A			N/A			N/A		
001b	4x refresh rate	O	O	O	O	O	O	X[1]		
010b	2x refresh rate	O	O	O	O	O	O	O	X[2]	O[2]
011b	1x refresh rate	O	O	O	O	O	O	O	O	O
100b	0.5x refresh rate	O	O	O	O	O	O	O	O	O
101b	0.25x refresh rate	O	O	O	O	O	O	O	O	O
110b	0.25x refresh rate	O	O	O	O	O	O	O	O	O
111b	High temp limit	N/A			N/A			N/A		

Note:

1. 4x refresh rate is no longer supported on 140s LP4.
2. Only modified refresh mode is supported at 2x refresh rate on 140s LP4.

O - Supported
X - Not supported

Table 2: Max Refresh Interval Across 100s-140s

MR4 OP[2:0]	Refresh Rate	100s/110s/120s		130s		140s	
		Distributed Refresh	Burst Refresh	Distributed Refresh	Burst Refresh	Distributed Refresh	Burst Refresh
000b	Low temp limit	N/A		N/A		N/A	
001b	4x refresh rate	4 x tREFI	9 x 4 x tREFI	4 x tREFI	9 x 4 x tREFI	Not Supported[1]	
010b	2x refresh rate	2 x tREFI	9 x 2 x tREFI	2 x tREFI	9 x 2 x tREFI	2 x tREFI	5 x 2 x tREFI[2]
011b	1x refresh rate	1 x tREFI	9 x tREFI	1 x tREFI	9 x tREFI	1 x tREFI	9 x tREFI
100b	0.5x refresh rate	0.5 x tREFI	9 x 0.5 x tREFI	0.5 x tREFI	9 x 0.5 x tREFI	0.5 x tREFI	9 x 0.5 x tREFI
101b	0.25x refresh rate	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI
110b	0.25x refresh rate	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI
111b	High temp limit	N/A		N/A		N/A	

Note:

1. 4x refresh rate is no longer supported on 140s LP4.
2. Only modified refresh mode is supported at 2x refresh rate on 140s LP4.

Table 3: MR4 OP[2:0] Across 100s-140s

Temperature (Tj)	100s/110s/120s		130s		140s	
	MR4 OP[2:0]	Refresh Rate	MR4 OP[2:0]	Refresh Rate	MR4 OP[2:0]	Refresh Rate
T < -38C	000b	Low temp limit	001b	4x	010b	2x
-38C <= T < 36C	001b	4x	001b	4x	010b	2x
36C <= T < 61C	010b	2x	010b	2x	010b	2x
61C <= T < 75C	011b	1x	010b	2x	010b	2x
75C <= T < 85C	011b	1x	010b	2x	010b	2x
85C <= T < 95C	100b	0.5x	011b	1x	011b	1x
95C <= T < 105C	101b	0.25x	100b	0.5x	100b	0.5x
105C <= T < 115C	110b	0.25x w/ derating	101b	0.25x	101b	0.25x
115C <= T < 125C	110b	0.25x w/ derating	110b	0.25x w/ derating	110b	0.25x w/ derating
125C<=T	111b	High temp limit	110b	0.25x w/ derating	110b	0.25x w/ derating

Micron EBU 140s Refresh Support Change Summary

- 4x refresh rate is removed altogether, 2x refresh rate will be the lowest refresh rate (longest refresh interval) on 140s
- Distributed refresh supports 0.25x to 2x refresh rates
- Burst refresh only supports modified refresh mode at 2x refresh rate (max 4 postponed or pulled-in REF commands, 5 x 2 x tREFI max refresh interval)
- Both legacy and modified refresh modes are supported at 0.25x to 1x refresh rates
- MR0 OP[0] will output 1b to signify only modified mode is supported at 2x refresh rate
- MR4 OP[2:0] removes 001b as 4x refresh rate is no longer supported
- Date retention and Row Hammer reliability at the supported refresh rates and modes are guaranteed by the DRAM device itself and does not require RFM support from the host

Distributed and Burst Refresh

MR4 OP[2:0]	Refresh Rate	Previous Series			130s			140s		
		Distributed Refresh	Burst Refresh		Distributed Refresh	Burst Refresh		Distributed Refresh	Burst Refresh	
			Legacy Mode	Modified Mode		Legacy Mode	Modified Mode		Legacy Mode	Modified Mode
000b	Low temp limit	N/A[1]			N/A[1]			N/A[1]		
001b	4x refresh rate	O	O	O	O	O	O	X[2]		
010b	2x refresh rate	O	O	O	O	O	O	O	X[3]	O[3]
011b	1x refresh rate	O	O	O	O	O	O	O	O	O
100b	0.5x refresh rate	O	O	O	O	O	O	O	O	O
101b	0.25x refresh rate	O	O	O	O	O	O	O	O	O
110b	0.25x refresh rate	O	O	O	O	O	O	O	O	O
111b	High temp limit	N/A[1]			N/A[1]			N/A[1]		

Note:

1. MR4 OP[2:0] = 000b and 111b (high and low temp limits) have been removed since 130s. Products of previous series will output MR4 OP[2:0] = 000b and 111b for temperatures beyond the high and low limits.
2. 140s products removes MR4 OP[2:0] = 001b as 4x refresh rate is no longer supported.
3. 140s products only support modified mode for burst refresh at 2x refresh rate.

Max Interval Between Two REFab

MR4 OP[2:0]	Refresh Rate	Previous Series		130s		140s	
		Distributed Refresh	Burst Refresh	Distributed Refresh	Burst Refresh	Distributed Refresh	Burst Refresh
000b	Low temp limit	N/A[1]		N/A[1]		N/A[1]	
001b	4x refresh rate	4 x tREFI	9 x 4 x tREFI	4 x tREFI	9 x 4 x tREFI	Not Supported[2]	
010b	2x refresh rate	2 x tREFI	9 x 2 x tREFI	2 x tREFI	9 x 2 x tREFI	2 x tREFI	5 x 2 x tREFI[3]
011b	1x refresh rate	1 x tREFI	9 x tREFI	1 x tREFI	9 x tREFI	1 x tREFI	9 x tREFI
100b	0.5x refresh rate	0.5 x tREFI	9 x 0.5 x tREFI	0.5 x tREFI	9 x 0.5 x tREFI	0.5 x tREFI	9 x 0.5 x tREFI
101b	0.25x refresh rate	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI
110b	0.25x refresh rate	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI	0.25 x tREFI	9 x 0.25 x tREFI
111b	High temp limit	N/A[1]		N/A[1]		N/A[1]	

Note:

1. MR4 OP[2:0] = 000b and 111b (high and low temp limits) have been removed since 130s. Products of previous series will output MR4 OP[2:0] = 000b and 111b for temperatures beyond the high and low limits.
2. 140s products removes MR4 OP[2:0] = 001b as 4x refresh rate is no longer supported.
3. 140s products only support modified mode for burst refresh at 2x refresh rate.

Refresh Rate Requirement Across Temperatures

Temperature	Previous Series		130s		140s	
	MR4 OP[2:0]	Refresh Rate	MR4 OP[2:0]	Refresh Rate	MR4 OP[2:0]	Refresh Rate
T < -38C	000b	Low temp limit	001b	4x	010b	2x[1]
-38C <= T < 36C	001b	4x	001b	4x	010b	2x[1]
36C <= T < 61C	010b	2x	010b	2x	010b	2x
61C <= T < 75C	011b	1x	010b	2x	010b	2x
75C <= T < 85C	011b	1x	010b	2x	010b	2x
85C <= T < 95C	100b	0.5x	011b	1x	011b	1x
95C <= T < 105C	101b	0.25x	100b	0.5x	100b	0.5x
105C <= T < 115C	110b	0.25x w/ derating	101b	0.25x	101b	0.25x
115C <= T < 125C	110b	0.25x w/ derating	110b	0.25x w/ derating	110b	0.25x w/ derating
125C<=T	111b	High temp limit	110b	0.25x w/ derating	110b	0.25x w/ derating

Note:

1. 2x refresh rate is required for temperatures below 36C. Refresh rate requirement for other temperatures remain the same with 130s.

140s Datasheet Changes

- MR4 OP[2:0] - Remove 000b, 001b and 111b

Table 32: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh rate	Read-only	OP[2:0]	~~000b: SDRAM low temperature operating limit exceeded~~ ~~001b: 4x refresh~~ 010b: 2x refresh 011b: 1x refresh (default) 100b: 0.5x refresh 101b: 0.25x refresh, no derating 110b: 0.25x refresh, with derating ~~111b: SDRAM high temperature operating limit exceeded~~	1–4, 7–9

- MR0 OP[0] = 1b – Only modified mode supported at 2x refresh rate (even though both legacy and modified mode are supported at 0.25x to 1x refresh rate)

Table 20: MR0 Device Feature 0 (MA[5:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		RFU	Latency mode	REF

Table 21: MR0 Op-Code Bit Definitions

Register Information	Type	OP	Definition	Notes
Refresh mode	Read-only	OP[0]	0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported	

Reference – Legacy and Modified Refresh Mode

Table 109: Legacy REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh rate	Max. No. of pulled-in or postponed REFab	Max. Interval between two REFab	Max. No. of REFab[1]	Per-bank REFRESH
000b	Low temp. limit	N/A	N/A	N/A	N/A
001b	4 × ^{t}REFI	8	9 × 4 × ^{t}REFI	16	1/8 of REFab
010b	2 × ^{t}REFI	8	9 × 2 × ^{t}REFI	16	1/8 of REFab
011b	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100b	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab
101b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111b	High temp. limit	N/A	N/A	N/A	N/A

Note: 1. Maximum number of REFab within MAX(2 × ^{t}REFI × refresh rate multiplier, 16 × ^{t}RFC).

Table 110: Modified REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh Rate	Max. No. of Pulled-in or Postponed REFab	Max. Interval between Two REFab	Max. No. of REFab[1]	Per-bank REFRESH
000B	Low temp. limit	N/A	N/A	N/A	N/A
001B	4 × ^{t}REFI	2	3 × 4 × ^{t}REFI	4	1/8 of REFab
010B	2 × ^{t}REFI	4	5 × 2 × ^{t}REFI	8	1/8 of REFab
011B	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100B	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab
101B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111B	High temp. limit	N/A	N/A	N/A	N/A

Notes:
1. For any thermal transition phase where refresh mode is transitioned to either 2 × ^{t}REFI or 4 × ^{t}REFI, LPDDR4 devices will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in REFRESH commands in the previous thermal phase are not applied in the new thermal phase. Entering a new thermal phase, the controller must count the number of pulled-in REFRESH commands as zero, regardless of the number of remaining pulled-in REFRESH commands in the previous thermal phase.
2. LPDDR4 devices are refreshed properly if the memory controller issues REFRESH commands with same or shorter refresh period than reported by MR4 OP[2:0]. If a shorter refresh period is applied, the corresponding requirements from this table apply. For example, when MR4 OP[2:0] = 001b, the controller can be in any refresh rate from 4 × ^{t}REFI to 0.25 × ^{t}REFI. When MR4 OP[2:0] = 010b, the only prohibited refresh rate is 4 × ^{t}REFI.