Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

HyperFlash
Palladium Memory Model
User Guide

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

HyperFlash Memory Model

1. Introduction

The Cadence Palladium HyperFlash Palladium memory model is based upon the *SPANSION HyperFlash specification (S26KL_KS-S, Revision 02, June 12, 2015) and CYPRESS HyperFlash specification (S26K-T, Rev. *D, June 13, 2017).*

The model is initially only available in a few configurations based on the SPANSION and CYPRESS HyperFlash specification. Currently, only a few different sizes are available, please consult the memory model catalog for the current available list.

HyperFlash Memory models available in protected RTL (*.vp) formats:

- s26ks128s : SPANSION 128 Mbit (16 Mbyte) HyperFlash
- s26ks256s : SPANSION 256 Mbit (32 Mbyte) HyperFlash
- s26ks512s : SPANSION 512 Mbit (64 Mbyte) HyperFlash

- s26ks512t (Beta) : CYPRESS 512 Mbit (64 Mbyte) 1.8V HyperFlash
- s26kl512t (Beta) : CYPRESS 512 Mbit (64 Mbyte) 3.0V HyperFlash
- s26ks01gt (Beta) : CYPRESS 1 Gbit (128 Mbyte) 1.8V HyperFlash
- s26kl01gt (Beta) : CYPRESS 1 Gbit (128 Mbyte) 3.0V HyperFlash

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Acronyms

Table 1: HyperFlash Model Acronyms

NAME	Descriptions
ASO	Address Space Overlay
ASP	Advanced Sector Protection
ASPR	ASP Configuration Register
ATBR	AutoBoot Register
CFI	Common Flash Interface
DED	Dual Error Detect
DYB	Dynamic Protection Bits
DCRC	Data Integrity Check (Memory Array) Cyclic Redundancy Check
EA	Embedded Algorithm
EAC	Embedded Algorithm Controller
ECC	Error Correction Code
ID	Device Identification
INT	Interrupt
ICRC	Interface Cyclic Redundancy Check
NVCR	Non-Volatile Configuration Register
POR	Power-On-Reset
PPB	Persistent Protection Bits
RWDS	Read Write Data Strobe
SA	Sector Address
SR	Status Register
SSR	Secure Silicon Region
SEC	Sector Erase Count
SFDP	Serial Flash Discoverable Parameters
VCR	Volatile Configuration Register

4. Features

The HyperFlash Palladium memory model is based upon the *SPANSION and CYPRESS HyperFlash spec*ification. Below tables list which features are supported and which are unsupported. Please refer to the *HyperFlash spec* for detailed information.

NOTE: The CYPRESS part models are currently available in Initial Release (IR) BETA program only. These models are not in the official MMP release. Please request access to these model via an FAE, the emulation support team, or the MMP support team.

Table 2: Features List of SPANSION HyperFlash Model

FEATURE	SUPPORT	NOTE
Memory Array Read (Wrapped Burst)	Yes	
Memory Array Read (Continuous Burst)	Yes	
Memory Array Write (Word Program)	Yes	
Memory Array Write (Buffer Program)	Yes	
Program Suspend/ Resume	Yes	
Chip erase/ Sector erase	Yes	
Erase Suspend/ Resume	Yes	
Blank Check	Yes	
Evaluate Erase Status	Yes	
Non-Volatile Configuration Register (NVCR) and Volatile Configuration Register (VCR)	Yes	
Status Register	Yes	
ID-CFI	Yes	
Secure Silicon Region (SSR)	Yes	
Advanced Sector Protection (ASP)	Yes	
Persistent Protection Bits (PPB)	Yes	
PPB Lock	Yes	
Dynamic Protection Bits (DYB)	Yes	
Persistent Protection Mode	Yes	
Password Protection Mode	Yes	
Read Password Protection Mode	Yes	
Hybrid Burst	Yes	
Interrupt (INT)	Yes	
Power-On-Reset	No	

Table 3: Features List of CYPRESS HyperFlash Model

FEATURE	SUPPORT	NOTE
Memory Array Read (Wrapped Burst)	Yes	
Memory Array Read (Linear Burst)	Yes	
Memory Array Write (Word Program)	Yes	
Memory Array Write (Buffer Program)	Yes	
Program Suspend/ Resume	Yes	
Chip erase/ Sector erase	Yes	
Erase Suspend/ Resume	Yes	
Blank Check	Yes	
Evaluate Erase Status	Yes	
Power-On Reset Timer Register	Yes	
Interrupt Configuration Register	Partial	Only Busy to Ready interrupt is supported
Interrupt Status Register	Partial	
Non-Volatile Configuration Register 1(NVCR1) and Volatile Configuration Register 1 (VCR1)	Yes	
Non-Volatile Configuration Register 2(NVCR1) and Volatile Configuration Register 2 (VCR1)	Yes	
Status Register	Yes	
ID-CFI-SFDP	Yes	
Secure Silicon Region (SSR)	Yes	
Advanced Sector Protection (ASP)	Yes	
Persistent Protection Bits (PPB)	Yes	
PPB Lock	Yes	
Dynamic Protection Bits (DYB)	Yes	
Persistent Protection Mode	Yes	
Password Protection Mode	Yes	
Read Password Protection Mode	Yes	
ECC Status ASO	Partial	ECC Status ASO Command is supported, but ECC Function is not supported, Read Command will return All 0
Data Integrity CRC ASO	Yes	
Interface CRC ASO	Partial	ICRC ASO Command is supported, but ICRC Function is not supported, Read Command will return all 1
AutoBoot ASO	Yes	
Sector Erase Count ASO	Yes	
EnduraFlex Pointer ASO	Yes	
Hybrid Burst	Yes	
Interrupt (INT)	Partial	Only Busy to Ready interrupt is supported
Legacy SPI Boot Mode	Yes	
Power-On-Reset	No	
Deep Power-Down	No	

5. Configurations

Below tables list the possible configurations. Not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Table 4: SPANSION HyperFlash Model Configurations

Memory Size	Sector Count	Sector Size (Kbyte)
64 Mbyte	256	256
32 Mbyte	128	256
16 Mbyte	64	256

Table 5: CYPRESS HyperFlash Model Configurations

Memory Size	Sector Count	Sector Size (Kbyte)
128 Mbyte	*512*	*256*
64 Mbyte	*256*	*256*

NOTE: The CYPRESS part models are currently available in Initial Release (IR) BETA program only. These models are not in the official MMP release. Please request access to these model via an FAE, the emulation support team, or the MMP support team.

6. Model Block Diagram

The following figures show the HyperFlash model block diagram, which has a low pin count bus interface. The VCC power pin is not supported.

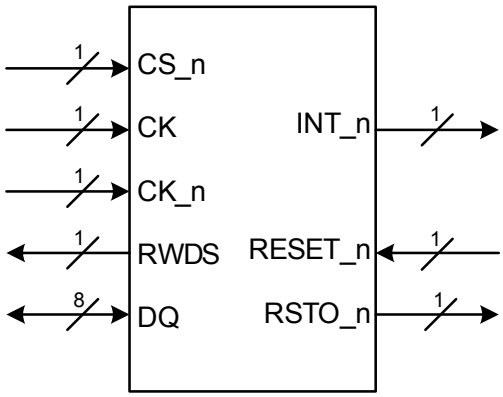


Figure 1: SPANSION HyperFlash Model Block Diagram

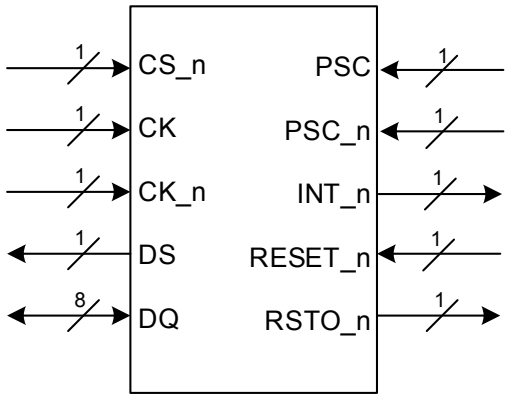


Figure 2: CYPRESS HyperFlash Model Block Diagram

7. I/O Signal Description

The tables below list and describe the model I/O signals.

Table 6: SPANSION HyperFlash Model I/O Signals

NAME	TYPE	DESCRIPTION
CS_n	Input	**Chip Select**: Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition.
CK, CK_n	Input	**Differential Clock:** Command/ Address/ Data information is input or output with respect to the crossing of the CK and CK_n signals.
RWDS	Output	**Read Write Data Strobe:** Output data during read transactions are edge aligned with RWDS.
DQ[7:0]	I/O	**Data Input/ Output:** Command/ Address/ Data information is transferred on these DQs during Read and Write transactions.

NAME	TYPE	DESCRIPTION
RESET_n	Input	**Hardware Reset:** When Low the device will self-initialize and return to the array read state. RWDS and DQ are placed into the High-Z state when RESET_n is Low.
RSTO_n	Output	**RESET Output:** Power On Reset is not supported, so the RSTO_n will be always High.
INT_n	Output	**INT Output:** When Low the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred.

Table 7: CYPRESS HyperFlash Model I/O Signals

NAME	TYPE	DESCRIPTION
CS_n	Input	**Chip Select**: Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition.
CK, CK_n	Input	**Differential Clock:** Command/ Address/ Data information is input or output with respect to the crossing of the CK and CK_n signals. **Single Ended:** CK is used (CK_n is not used and can be left floating). Command / Address / Data information is input or output with respect to the edges of CK signal. **Note:** The clock is not required to be free running.
DS	Output	**Read Data Strobe:** Output data during read transactions are edge aligned with DS.
DQ[7:0]	I/O	**Data Input/ Output:** Command/ Address/ Data information is transferred on these DQs during Read and Write transactions.
PSC,PSC_n	Input	**Phase Shifted Clock.** PSC/PSC# allows independent skewing of the DS signal with respect to CK/CK_n inputs. PSC and PSC_n may be driven High and Low respectively or both may be driven Low during write transactions. **Note:** PSC/PSC_n follows CK/CK_n configuration. If clock is differential, Phase Shifted Clock must also be differential as well and vice versa.
RESET_n	Input	**Hardware Reset:** When Low, the device will self initialize and return to the array read state. DS and DQ[7:0] are placed into the High-Z state when RESET_n is Low. RESET_n includes a weak pull-up, if RESET_n is left unconnected it will be pulled up to the High state..
RSTO_n	Output	**RESET Output:** Power On Reset is not supported, so the RSTO_n will be always High.
INT_n	Output	**INT Output:** When Low the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred.

8. Model Parameter Descriptions

The following table provides details on the user adjustable parameters for the Palladium HyperFlash memory model. These parameters may be modified when instantiating a HyperFlash wrapper or, if necessary, by modifying the HDL parameter declarations and default values which are exposed for access and debug visibility.

Table 8: User Adjustable Parameters (SPANSION Models)

User Adjustable Parameter	Default Value	Description
addr_bits	25	The address width of HyperFlash

Table 9: User Adjustable Parameters (CYPRESS Models)

User Adjustable Parameter	Default Value	Description
addr_bits	25	The address width of HyperFlash

The following table provides some information about exposed parameters and localparams that are NOT user adjustable. On rare occasion the user may find one of these parameters or localparam needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

Table 10: Visible Non-User-Adjustable Parameters & Localparams (SPANSION Models)

Parameter / Localparam	Default Value	Description
data_bits	8	The data bus width of HyperFlash

Table 11: Visible Non-User-Adjustable Parameters & Localparams (CYPRESS Models)

Parameter / Localparam	Default Value	Description
data_bits	8	The data bus width of HyperFlash
device_id	0x3032_8303_4D20_0201	Device Identification is not defined in datasheet. The user can modify it if needed
device_uid	0x3032_8303_4D20_0201	Device Unique Identification is not defined in datasheet. The user can modify it if needed.

Note that there are additional exposed localparams in the model HDL that are not described here nor intended to be described here. These additional localparams are exposed for debugging purposes only and will not be described herein.

9. Address mapping

The array of the HyperFlash model is mapped into the internal memory of the Palladium system. This array is a signal two dimensional array. The array width is 16bit and the address of the memory array is word address.

The array name in the model is: memcore

NOTE: For CYPRESS HyperFlash model, when it is in SPI Mode, all addresses of SPI command are byte addresses.

10. Commands

The HyperFlash memory model supports the commands listed in below tables. Please refer to the *SPANSION and CYPRESS HyperFlash* specifications for details about the timing and bus cycles for each command.

Table 12: Command List of SPANSION HyperFlash Model

Command Sequence		SUPPORT
Read		Yes
Reset / ASO Exit		Yes
Status Register Read		Yes
Status Register Clear		Yes
Enter Deep Power-Down		Yes
Program Power-On Reset Timer Register		Yes
Read Power-On Reset Timer Register		Yes
Load Interrupt Configuration Register		Yes
Read Interrupt Configuration Register		Yes
Load Interrupt Status Register		Yes
Read Interrupt Status Register		Yes
Load Volatile Configuration Register		Yes
Read Volatile Configuration Register		Yes
Program Non-Volatile Configuration Register		Yes
Erase Non-Volatile Configuration Register		Yes
Read Non-Volatile Configuration Register		Yes
Word Program		Yes
Write to Buffer		Yes
Program Buffer to Flash (Confirm)		Yes
Write-to-Buffer-Abort Reset		Yes
Chip Erase		Yes
Sector Erase		Yes
Blank Check		Yes
Evaluate Erase Status		Yes
Erase Suspend		Yes
Erase Resume		Yes
Program Suspend		Yes
Program Suspend		Yes
ID-CFI ASO	ID (Autoselect) Entry	Yes
	CFI Enter	Yes
	ID-CFI Read	Yes
	Reset/ ASO Exit	Yes
SSR ASO	SSR Entry	Yes
	Read	Yes
	Word Program	Yes
	Write to Buffer	Yes
	Program Buffer to Flash (confirm)	Yes
	Write-to-Buffer-Abort Reset	Yes
	SSR Exit	Yes
	Reset/ ASO Exit	Yes
ASP R	ASP Register Entry	Yes
	Program	Yes
	ASPR Read	Yes

Command Sequence		SUPPORT
	ASPR ASO Exit	Yes
	Reset/ ASO Exit	Yes
Password ASO	Password ASO Entry	Yes
	Program	Yes
	Read	Yes
	Unlock	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
PPB ASO	PPB Entry	Yes
	PPB Program	Yes
	All PPB Erase	Yes
	PPB Read	Yes
	SA Protection Status	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
PPB Lock Bit	PPB Lock Entry	Yes
	PPB Lock Bit Clear	Yes
	PPB Lock Status Read	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
DYB ASO	DYB ASO Entry	Yes
	DYB Set	Yes
	DYB Clear	Yes
	DYB Status Read	Yes
	SA Protection Status	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes

Table 13: HyperBus Command List of CYPRESS HyperFlash Model

Command Sequence	SUPPORT
Read	Yes
Reset / ASO Exit	Yes
Enter SPI Mode	Yes
Status Register Read	Yes
Status Register Clear	Yes
Enter Deep Power-Down	Yes
Program Power-On Reset Timer Register	Yes
Read Power-On Reset Timer Register	Yes
Load Interrupt Configuration Register	Yes
Read Interrupt Configuration Register	Yes
Load Interrupt Status Register	Yes
Read Interrupt Status Register	Yes
Load Volatile Configuration Register(VCR1)	Yes
Load Volatile Configuration Register(VCR2)	Yes
Read Volatile Configuration Register(VCR1)	Yes
Read Volatile Configuration Register(VCR2)	Yes
Program Non-Volatile Configuration Register(NVCR1)	Yes
Program Non-Volatile Configuration Register(NVCR2)	Yes
Erase Non-Volatile Configuration Registers	Yes

Read Non-Volatile Configuration Register(NVCR1)		Yes
Read Non-Volatile Configuration Register(NVCR2)		Yes
Word Program		Yes
Write to Buffer		Yes
Program Buffer to Flash(confirm)		Yes
Write-to-Buffer-Abort Reset		Yes
Chip Erase		Yes
Sector Erase		Yes
Blank Check		Yes
Evaluate Erase Status		Yes
Erase Suspend		Yes
Erase Resume		Yes
Program Suspend		Yes
Program Resume		Yes
ID-CFI-SFDP ASO	ID-CFI-SFDP Entry	Yes
	ID-CFI-SFDP Enter	Yes
	ID-CFI-SFDP Read	Yes
	Reset / ASO Exit	Yes
SSR ASO	SSR Entry	Yes
	Read	Yes
	Word Program	Yes
	Write to Buffer	Yes
	Program Buffer to Flash (confirm)	Yes
	Write-to-Buffer-Abort Reset	Yes
	SSR Exit	Yes
	Reset/ ASO Exit	Yes
ASPR ASO	ASP Register Entry	Yes
	Program	Yes
	ASPR Read	Yes
	ASPR ASO Exit	Yes
	Reset/ ASO Exit	Yes
Password ASO	Password ASO Entry	Yes
	Program	Yes
	Read	Yes
	Unlock	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
PPB ASO	PPB Entry	Yes
	PPB Program	Yes
	All PPB Erase	Yes
	PPB Read	Yes
	SA Protection Status	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
PPB Lock Bit	PPB Lock Entry	Yes
	PPB Lock Bit Clear	Yes
	PPB Lock Status Read	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
D Y	DYB ASO Entry	Yes
	DYB Set	Yes

	DYB Clear	Yes
	DYB Status Read	Yes
	SA Protection Status	Yes
	Command Set Exit	Yes
	Reset/ ASO Exit	Yes
ECC Status ASO	ECC Status Enter	Yes
	ECC Status Read	Yes
	Error Lower Address Register	Yes
	Error Upper Address Register	Yes
	Read Error Detection Counter	Yes
	Clear ECC Errors	Yes
	Reset/ASO Exit	Yes
Data Integrity CRC ASO	CRC ASO Entry	Yes
	Load CRC Start Address	Yes
	Load CRC End Address (start calculation)	Yes
	CRC Suspend	Yes
	Array Read (during suspend)	Yes
	CRC Resume	Yes
	Read Check-value Low Result Register	Yes
	Read Check-value High Result Register	Yes
	Reset / ASO Exit	Yes
Interface CRC ASO	CRC ASO Entry	Yes
	Read Check-value Low Result Register	Yes
	Read Check-value High Result Register	Yes
	Reset / ASO Exit	Yes
AutoBoot ASO	AutoBoot Register Entry	Yes
	AutoBoot Register Write	Yes
	AutoBoot Register Read	Yes
	Command Set Exit	Yes
	Reset / ASO Exit	Yes
SEC ASO	SEC Register Entry	Yes
	SEC Command	Yes
	SEC Register Read	Yes
	Command Set Exit	Yes
	Reset / ASO Exit	Yes
EFP ASO	EFP ASO Entry	Yes
	EFP Program	Yes
	EFP Read	Yes
	Command Set Exit	Yes
	Reset / ASO Exit	Yes

Table 14: SPI Command List of CYPRESS HyperFlash Model

Function	Command Name	Instruction Value(Hex)	SUPPORT
Read Device ID	RDID	9F	Yes
	RSFDP	5A	Yes
	RUID	4C	Yes
Register Access	RDAR	65	Yes
	RDSR1	05	Yes
	RDSR2	07	Yes
	WRDI	04	Yes
	WREN	06	Yes
	WRENV	50	Yes
	WRAR	71	Yes
	CLSR	30 / 82	Yes
	SWL	C0	Yes
ECC	ECCRD	19	Yes
	CLECC	1B	Yes
CRC	RICRC	64	Yes
	DICR	5B	Yes
Read Flash Array	4READ	13	Yes
	4FAST_READ	0C	Yes
Program Flash Array	4PP	12	Yes
Erase Flash Array	4P4E	21	Yes
	4SE	DC	Yes
	BE	60 / C7	Yes
	EES	D0	Yes
Suspend / Resume	EPCS	75 / 85	Yes
	EPCR	30 / 7A / 8A	Yes
One Time Program Array	OTPP	42	Yes
	OTPR	4B	Yes
Advanced Sector Protection	4DYBRD	E0	Yes
	4DYBWR	E1	Yes
	4PPBRD	E2	Yes
	4PPBP	E3	Yes
	PPBE	E4	Yes
	PPBEA	EA	Yes
	PLBRD	A7	Yes
	PLBWR	A6	Yes
	PASSU	E9	Yes
Reset	RSTEN	66	Yes
	RST	99	Yes
DPD	DPD	B9	Yes
NOP	NOP	00	Yes

Note: Program and Erase - Flash data bits may be individually programmed from the erased 1 state to the programmed logical 0 (low) state. A data bit of 0 cannot be programmed back to a 1. A succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1. Programming the same word location more than once with different 0 bits will result in the logical AND of the previous data and the new data being programmed.

11. Initialization Sequence

The HyperFlash memory model requires that the memory controller first issue a hardware reset before issuing any commands.

12. ID-CFI Address Map

The follow table shows the ID-CFI Address Map definition and default values.

NOTE: The ID-CFI Table is only used for SPANSION HyperFlash models.

Table 15: ID-CFI Address Map

Word Address	Default Value	Description
(SA) + 0000h	0001h	Manufacture ID
(SA) + 0001h	007Eh	Device ID
(SA) + 0002h - 000Bh	0000h	RFU
(SA) + 000Ch	0005h	Lower Software Bits
(SA) + 000Dh	0000h	Upper Software Bits
(SA) + 000Eh	0070h = 512 Mb 0072h = 256 Mb 0074h = 128 Mb	Device ID
(SA) + 000Fh	0000h	Device ID
(SA) + 0010h (SA) + 0011h (SA) + 0012h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
(SA) + 0013h (SA) + 0014h	0002h 0000h	Primary OEM Command Set
(SA) + 0015h (SA) + 0016h	0040h 0000h	Address for Primary Extended Table
(SA) + 0017h (SA) + 0018h	0000h 0000h	Alternate OEM Command Set
(SA) + 0019h (SA) + 001Ah	0000h 0000h	Address for Alternate OEM Extended Table
(SA) + 001Bh	0017h	Vcc Min. (erase/ program)
(SA) + 001Ch	0019h	Vcc Max. (erase/ program)
(SA) + 001Dh	0000h	Vpp Min. voltage
(SA) + 001Eh	0000h	Vpp Max. voltage
(SA) + 001Fh	0009h	Typical timeout per single word write 2^N us
(SA) + 0020h	0009h	Typical timeout for max multi-byte program 2^N us
(SA) + 0021h	000Ah	Typical timeout per individual block erase 2^N us
(SA) + 0022h	0012h (512 Mb) 0011h (256 Mb) 0010h (128 Mb)	Typical timeout for full chip erase 2^N timers typical
(SA) + 0023h	0002h	Max. timeout for single word write 2^N times typical
(SA) + 0024h	0002h	Max. timeout for buffer write 2^N timers typical

Word Address	Default Value	Description
(SA) + 0025h	0002h	Max. timeout per individual block erase 2^N times typical
(SA) + 0026h	0002h	Max. timeout for full chip erase 2^N times typical
(SA) + 0027h	001Ah (512 Mb) 0019h (256 Mb) 0018h (128 Mb)	Device Size = 2^N byte
(SA) + 0028h (SA) + 0029h	0000h 0000h	Flash Device Interface Description 0= x8-only
(SA) + 002Ah (SA) + 002Bh	0009h 0000h	Max. number of byte in multi-byte write = 2^N
(SA) + 002Ch	0001h	Number of Erase Block Regions within device
(SA) + 002Dh	00FFh (512 Mb) 007Fh (256 Mb) 003Fh (128 Mb)	Erase Block Region 1 Information
(SA) + 002Eh (SA) + 002Fh (SA) + 0030h	0000h 0000h 0004h	Erase Block Region 1 Information
(SA) + 0031h (SA) + 0032h (SA) + 0033h (SA) + 0034h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information
(SA) + 0035h (SA) + 0036h (SA) + 0037h (SA) + 0038h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
(SA) + 0039h (SA) + 003Ah (SA) + 003Bh (SA) + 003Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information
(SA) + 0040h (SA) + 0041h (SA) + 0042h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
(SA) + 0043h	0031h	Major version number, ASCII
(SA) + 0044h	0035h	Minor version number, ASCII
(SA) + 0045h	001Ch	Address Sensitive Unlock and process technology
(SA) + 0046h	0002h	Erase suspend
(SA) + 0047h	0001h	Sector Protect
(SA) + 0048h	0000h	Temporary Sector Unprotect
(SA) + 0049h	0008h	Sector Protect/ Unprotect Scheme
(SA) + 004Ah	0000h	Simultaneous Operation
(SA) + 004Bh	0001h	Burst Mode Type
(SA) + 004Ch	0000h	Page Read Mode Type
(SA) + 004Dh	0000h	ACC Supply Minimum
(SA) + 004Eh	0000h	ACC Supply Maximum
(SA) + 004Fh	0006h	WP# Protection=06h WP protect for all sectors
(SA) + 0050h	0001h	Program Suspend
(SA) + 0051h	0000h	Unlock Bypass
(SA) + 0052h	000Ah	Secure Silicon Sector Size 2^N bytes
(SA) + 0053h	008Dh	Software Feature
(SA) + 0054h	0005h	Page Size = 2^N bytes
(SA) + 0055h	0006h	Erase Suspend Timeout Maximum
(SA) + 0056h	0006h	Program Suspend Timeout Maximum
(SA) + 0057h - 0077h	FFFFh	Reserved

Word Address	Default Value	Description
(SA) + 0078h	0006h	Embedded Hardware Reset Timeout Maximum
(SA) + 0079h	0009h	Non-embedded Hardware Reset Timeout Maximum
(SA) + 007Ah - 007Fh	0000h	Reserved for factory data
(SA) + 0080h - 008Ch	0000h	Reserved for factory programmed data
(SA) + 008Dh - 00FFh	0000h	Reserved for factory data

13. ID-CFI-SFDP Address Map

The following table shows the ID-CFI-SFDP Address Map.

NOTE: The ID-CFI-SFDP table below is only used for CYPRESS HyperFlash models. The detailed address map definition is not defined in the datasheet.

Table 16: ID-CFI-SFDP Address Map Overview

Word Address	Description	Read/Write
(SA) + 0000h to 03FFh	SFDP	Read Only
(SA) + 0400h to 0407h	Unique ID	Read Only
(SA) + 1000h to 13FFh	ID-CFI	Read Only

14. SSR Address Map

The follow table shows the SSR Address Map definition and default values, the SSR region is 16bit in width and uses word address.

Table 17: SSR Address Map

Word Address	Default Value	Description
0000h 0001h 0002h 0003h 0004h 0005h 0006h 0007h	1234h 5678h 9ABCh DEF0h 1234h 5678h 9ABCh DEF0h	Spansion Programed Random Number
0008h 0009h	FFFFh FFFFh	Region Locking Bits
000Ah - 000Fh	FFFFh	RFU
0010h - 001Fh	FFFFh	Region 1, Available for User Programming
0020h - 002Fh	FFFFh	Region 2, Available for User Programming
……	……	……
01F0h - 01FFh	FFFFh	Region 31, Available for User Programming

15. Configuration Registers

The following table shows the configuration registers of the HyperFlash model.

Table 18: Configuration Registers of SPANSION HyperFlash Model

Name	Width (bits)	Default Value	Description
NVCR	16	8EBBh	Non-Volatile Configuration Register
PWD	64	FFFF FFFF FFFF FFFFh	Password Protection Register Hardware reset will NOT reset the value of PWD
PPB	1-bit per sector	1 when ASPR[2:1] = 10 or 11 0 when ASPR[2:1] = 01	Persistent Protection Bits
ASPR	16	FEFFh	ASP Configuration Register Hardware reset will NOT reset the value of ASPR
PORTime	16	FFFFh	Power-on Reset Time
VCR	16	NVCR	Volatile Configuration Register
DYB	1-bit per sector	1	Dynamic Protection Bits
PPB Lock Bit	1	ASPR[2]	
ICR	16	FFFFh	Interrupt Configuration Register

Table 19: HyperBus Configuration Registers of Cypress HyperFlash Model

Name	Width (bits)	Default Value	Description
NVCR1	16	0ECBh	Non-Volatile Configuration Register 1
NVCR2	16	FFFFh	Non-Volatile Configuration Register 2
PWD	64	FFFF FFFF FFFF FFFFh	Password Protection Register Hardware reset will NOT reset the value of PWD
PPB	1-bit per sector	1 when ASPR[2:1] = 10 or 11 0 when ASPR[2:1] = 01	Persistent Protection Bits
ASPR	16	FEFFh	ASP Configuration Register Hardware reset will NOT reset the value of ASPR
PORTime	16	FFFFh	Power-on Reset Time
AutoBoot	32	FFFF_FFFFh	AutoBoot Register
VCR1	16	NVCR1	Volatile Configuration Register 1
VCR2	16	NVCR2	Volatile Configuration Register 2
DYB	1-bit per sector	1	Dynamic Protection Bits
PPB Lock Bit	1	ASPR[2]	
ICR	16	FFFFh	Interrupt Configuration Register

Table 20: SPI Configuration Registers of Cypress HyperFlash Model

Name	Width (bits)	Default Value	Description
NVCR1	8	00h	Non-Volatile Configuration Register 1
NVCR2	8	88h	Non-Volatile Configuration Register 2
NVCR3	8	00h	Non-Volatile Configuration Register 3
NVCR4	8	18h	Non-Volatile Configuration Register 4
VCR1	8	NVCR1	Volatile Configuration Register 1
VCR2	8	NVCR2	Volatile Configuration Register 2
VCR3	8	NVCR3	Volatile Configuration Register 3
VCR4	8	NVCR4	Volatile Configuration Register 4

16. Limitations

1. Unsupported features are listed in the relevant model features lists. See Table 2 and Table 3.

2. SSR: After an SSR region is programed, the controller should program the related protection bit in the SSR Lock Bytes to prevent further programming.

17. Compile and Emulation

The model is provided as protected RTL files (*.vp). The files need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64bit -ua +sv +dut+s26ks512s \
    ./s26ks512s.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile s26ks512s.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog s26ks512s.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
s26ks512s
……

2)
vavlog s26ks512s.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog s26ks512s.vg
s26ks512s
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

There are two data files that need to be preloaded for information initialization.

Table 21: SPANSION HyperFlash Model Preload Data File List

DATA FILE NAME	DESCRIPTIONS
xxx_id_cfi.dat	For ID_CFI information 'xxx' is the model part number name for different size: s26ks512s/ s26ks256s/s26ks128s
ssr.dat	For SSR initialization

Table 22: CYPRESS HyperFlash Model Preload Data File List

DATA FILE NAME	DESCRIPTIONS
xxx_id_cfi_sfdp.dat	For ID_CFI_SFDP information 'xxx' is the model part number name for different size: s26ks512t/ s26kl512t/s26ks01gt/s26kl01gt The content of the ID-CFI-SFDP is not defined in the datasheet, user can modify it if needed.
ssr.dat	For SSR initialization

For the SPANSION HyperFlash model, the user should preload all the initial dat files for the ID_CFI and SSR initialization as listed in Table 21. The user also needs to set the main array 'memcore' and the buffer array 'membuf' to all '1'.

For the CYPRESS HyperFlash model, the user should preload all the initial dat files for the ID_CFI_SFDP and SSR initialization as listed in Table 22. The user also needs to set the main array 'memcore' and the buffer array 'membuf_hb' and 'membuf_spi' to all '1'. If the Sector Erase Count ASO is used, the user also needs to reset the SEC array 'mem_sec' to all '0'.

Below is a scripting example snippet showing the preloading of the dat files into the HyperFlash model. The user can change the HyperFlash model instance name "hyperflash_inst" as needed.

Example for SPANSION HyperFlash models

```
……
xc xt0 zt0 run
xc memory -load %readmemh hyperflash_inst.mem_id_cfi -file s26ks512s_id_cfi.dat
xc memory -load %readmemh hyperflash_inst.mem_ssr -file ssr.dat
xc memory -set hyperflash_inst.memcore
xc memory -set hyperflash_inst.membuf
……
```

Example for CYPRESS HyperFlash models

```
……
xc xt0 zt0 run
xc memory -load %readmemh hyperflash_inst.mem_id_cfi -file s26ks512t_id_cfi_sfdp.dat
xc memory -load %readmemh hyperflash_inst.mem_ssr -file ssr.dat
xc memory -set hyperflash_inst.memcore
xc memory -set hyperflash_inst.membuf_hb
xc memory -set hyperflash_inst.membuf_spi
xc memory -set hyperflash_inst.mem_sec
……
```

18. Debugging

The HyperFlash model has several debugging options techniques and tips that may assist the user may use in isolating a problem.

- For issues that are may not be HyperFlash specific please review the *Memory Model Portfolio FAQ for All Models User Guide.*

- **Debug Signal**:

  The following signals can be monitored to examine SPANSION HyperFlash command sequence:
  - cmd_seq_state : State machine of HyperBus Command Sequence
  - addr_space_map : Address space map
  - BL : Burst Length
  - RL : Read Latency
  - word_prog_flag : Word program flag
  - wr_to_buf_flag : Write to program buffer flag
  - prog_buf_to_flash_flag : Program data in buffer to flash memory flag
  - rd_mem_array_flag : Read memory array flag
  - sec_erase_flag : Sector erase flag

  The following signals can be monitored to examine Cypress HyperFlash command sequence:
  - hb_seq_state : State machine of HyperBus Command Sequence
  - addr_space_map : Address space map
  - ca_cycle_cnt : CA cycle counter for HyperBus interface.
  - word_prog_flag : Word Program flag
  - buf_prog_flag : Program data in buffer to flash memory flag
  - sec_erase_flag : Sector erase flag
  - spi_seq_state : State machine of SPI Command Sequence
  - page_prog_flag : Page program flag
  - atb_flag : AutoBoot flag
  - atb_rd_addr : AutoBoot address

- **Golden waveform:** A package with a reference waveform is available which shows the following command sequence:

  Command sequence for SPANSION HyperFlash models:

  (1) Hardware reset
  (2) Word Program
  Wrapped burst Read
  Continuous burst Read
  (3) Load VCR, set BL=64 RL=12
  Write to Buffer
  Program Buffer to Flash
  Wait ready [Read Status Register]
  Wrapped burst Read

Continuous burst Read
(4) Sector Erase
Wait ready [Read Status Register]
Blank Check
Wait ready [Read Status Register]
Evaluate Erase Status
Wait ready [Read Status Register]
(5) ASPR Entry
ASPR Program [Enable Hybrid burst]
ASPR Exit
Loac VCR, set BL=32 RL=16
Word Program
Wrapped burst Read
ASPR Entry
ASPR Program [Disable Hybrid burst]
ASPR Exit
(6) ID_CFI Entry
ID_CFI Read
ID_CFI Exit
(7) SSR Entry
SSR Word Program
SSR Read [Wrapped burst]
SSR Write to Buffer
SSR Program Buffer to Flash
Wait ready [Read Status Register]
SSR Read [Continuous burst]
SSR Exit
(8) Password Entry
Password Program
Password Read
Password Exit
ASPR Entry
ASPR Program [Enable Password Protection mode]
ASPR Exit
Hardware Reset
Password Entry
Password Unlock
Password Exit
(9) PPB Entry
PPB Erase
PPB Program
PPB Exit
(10)PPB Lock Bit Entry
PPB Lock Bit Read
PPB Lock Bit Clear
PPB Lock Bit Exit
(11)DYB Entry
DYB Set
DYB Status Read
DYB SA Protect Status
DYB Clear
DYB Exit

Command sequence for CYPRESS HyperFlash models:

(1) Hardware reset

(2) SPI - Read ID
SPI - Read SFDP
SPI - Read Unique ID

(3) SPI - Read Status Register-1
SPI - Read Status Register-2
SPI - Read AutoBoot Register[7: 0]
SPI - Read AutoBoot Register[15: 8]
SPI - Read AutoBoot Register[23:16]
SPI - Read AutoBoot Register[31:24]

(4) SPI - Write Enable
SPI - Page Program
SPI - Wait ready [Read Status Register-1]
SPI - Fast Read

(5) SPI - Write Enable
SPI - Sector Erase
SPI - Wait ready [Read Status Register-1]
SPI - Fast Read

(6) SPI - Evaluate Erase Status
SPI - Wait ready [Read Status Register-1]

(7) SPI - Write Enable
SPI - OTP Program
SPI - OTP Read

(8) SPI - Write Enable
SPI - DYB Write
SPI - DYB Read
SPI - Write Enable
SPI - DYB Write
SPI - DYB Read

(9) SPI - Write Enable
SPI - PPB Program
SPI - PPB Read
SPI - Write Enable
SPI - PPB Program
SPI - PPB Read

(10) SPI - Write Enable
SPI - PPB Erase Addressed
SPI - PPB Read
SPI - Write Enable
SPI - PPB Erase
SPI - PPB Read

(11) SPI - Write Enable
SPI - PLB Write
SPI - PLB Read

(12) SPI - Password Unlock

(13) SPI - Write Enable
SPI - Page Program
SPI - Write Enable
SPI - Write AutoBoot Register[7: 0]
SPI - Write Enable
SPI - Write AutoBoot Register[15: 8]
SPI - Write Enable
SPI - Write AutoBoot Register[23:16]
SPI - Write Enable
SPI - Write AutoBoot Register[31:24]
Hardware reset

SPI - AutoBoot

(14) SPI - Write Enable
SPI - Write Configuration Register-3[SPI to HyperBus Interface]
Hardware reset

(15) HyperBus - Word Program
HyperBus - Wrapped burst Read
HyperBus - Linear burst Read

(16) HyperBus - Load VCR1, set BL=64,RL=12
HyperBus - Write to Buffer
HyperBus - Program Buffer to Flash
HyperBus - Wait ready [Read Status Register]
HyperBus - Wrapped burst Read
HyperBus - Linear burst Read

(17) HyperBus - Sector Erase
HyperBus - Wait ready [Read Status Register]
HyperBus - Blank Check
HyperBus - Wait ready [Read Status Register]
HyperBus - Evaluate Erase Status
HyperBus - Wait ready [Read Status Register]

(18) HyperBus - Load VCR1, set BL=32,RL=16
HyperBus - Load VCR2, Enable Hybrid burst
HyperBus - Word Program
HyperBus - Wrapped burst Read[Hybrid Burst]
HyperBus - Load VCR2, Disable Hybrid burst

(19) HyperBus - ID-CFI-SFDP Entry
HyperBus - ID-CFI-SFDP Read
HyperBus - ID-CFI-SFDP Exit

(20) HyperBus - SSR Entry
HyperBus - SSR Word Program
HyperBus - SSR Read [Wrapped burst]
HyperBus - SSR Write to Buffer
HyperBus - SSR Program Buffer to Flash
HyperBus - Wait ready [Read Status Register]
HyperBus - SSR Read [Continuous burst]
HyperBus - SSR Exit

(21) HyperBus - Password Entry
HyperBus - Password Program
HyperBus - Password Read
HyperBus - Password Exit
HyperBus - ASPR Entry
HyperBus - ASPR Program [Enable Password Protection mode]
HyperBus - ASPR Exit
HyperBus - Hardware Reset
HyperBus - Password Entry
HyperBus - Password Unlock
HyperBus - Password Exit

(22) HyperBus - PPB Entry
HyperBus - PPB Erase
HyperBus - PPB Program
HyperBus - PPB Exit

(23) HyperBus - PPB Lock Bit Entry
HyperBus - PPB Lock Bit Read

HyperBus - PPB Lock Bit Clear
HyperBus - PPB Lock Bit Exit

(24) HyperBus - DYB Entry
HyperBus - DYB Set
HyperBus - DYB Status Read
HyperBus - DYB SA Protect Status
HyperBus - DYB Clear
HyperBus - DYB Exit

(25) HyperBus - ECC Status Enter
HyperBus - ECC Status Read
HyperBus - Error Lower Address Register Read
HyperBus - Error Upper Address Register Read
HyperBus - Error Detection Counter Read
HyperBus - Clear ECC Errors
HyperBus - ECC Status Exit

(26) HyperBus - DCRC ASO Entry
HyperBus - Load CRC Start Address
HyperBus - Load CRC End Address
HyperBus - Wait ready [Read Status Register]
HyperBus - Read Check-value Low Result Register
HyperBus - Read Check-value High Result Register
HyperBus - DCRC ASO Exit

(27) HyperBus - ICRC ASO Entry
HyperBus - Read Check-value Low Result Register
HyperBus - Read Check-value High Result Register
HyperBus - ICRC ASO Exit

(28) HyperBus - AutoBoot ASO Entry
HyperBus - AutoBoot Write[Low Word]
HyperBus - AutoBoot Write[High Word]
HyperBus - AutoBoot Read Low Word
HyperBus - AutoBoot Read High Word
HyperBus - AutoBoot ASO Exit

(29) HyperBus - SEC ASO Entry
HyperBus - SEC Command
HyperBus - SEC Read Low Word
HyperBus - SEC Read High Word
HyperBus - SEC ASO Exit

(30) HyperBus - EFP ASO Entry
HyperBus - EFP Program[Pointer Address 0]
HyperBus - EFP Program[Pointer Address 1]
HyperBus - EFP Program[Pointer Address 2]
HyperBus - EFP Program[Pointer Address 3]
HyperBus - EFP Program[Pointer Address 4]
HyperBus - EFP Read[Pointer Address 0]
HyperBus - EFP Read[Pointer Address 1]
HyperBus - EFP Read[Pointer Address 2]
HyperBus - EFP Read[Pointer Address 3]
HyperBus - EFP Read[Pointer Address 4]
HyperBus - EFP ASO Exit

- **Debug Display:** The Palladium HyperFlash memory model has available a built-in debug methodology called MMP Debug Display that is based on the Verilog system task

$display. Please see the *Palladium Memory Model Debug Display User Guide* in the release docs directory for additional information.

- **Manual Configuring of this MMP Model Family**

This MMP model supports manual configuration by accompanying the model mode register or configuration register declarations with synthesis directives, such as keep_net directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing. For a general description of this support please see the user guide in the MMP release with path and filename *docs/MMP_FAQ_for_All_Models.pdf*.

While MMP strongly recommends following protocol-based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments.

The following table lists the internal register path and naming along with the specification or datasheet naming for model mode registers or configuration registers that are accompanied by keep_net synthesis directives in support of such manual configuration. ONLY writeable configuration registers or fields are supported thusly. Please read the relevant datasheet for details about individual register behavior and mapping to fields.

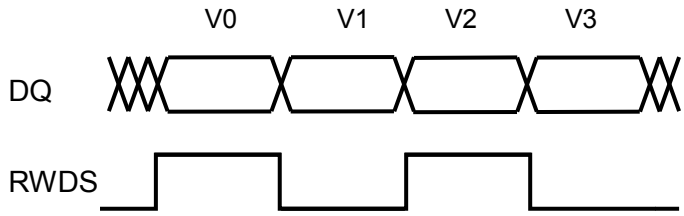
Table 23: Writeable Mode Register / Configuration Register Info

Hierarchical RTL Naming for Writeable Configuration Related Registers & Signals	Specification or Vendor Datasheet Naming for Configuration Related Registers	Access
For Spansion models		
<model_name>.nvcr	Non-Volatile Configuration Register	R/W
<model_name>.vcr	Volatile Configuration Register	R/W
<model_name>.aspr	ASP Configuration Register	R/W
For Cypress models		
<model_name>.hb_vcr1	Volatile Configuration Register 1	R/W
<model_name>.hb_vcr2	Volatile Configuration Register 2	R/W
<model_name>.spi_vcr1	Legacy SPI mode Configuration Register 1	R/W
<model_name>.spi_vcr2	Legacy SPI mode Configuration Register 2	R/W
<model_name>.spi_vcr3	Legacy SPI mode Configuration Register 3	R/W
<model_name>.spi_vcr4	Legacy SPI mode Configuration Register 4	R/W

19. Handling RWDS in Palladium HyperFlash Memory Model

For reads from the HyperFlash model, the HyperFlash model will drive DQ and RWDS with the first RWDS edge at the *beginning* of the first valid data, not at the end:

NOTE: For the CYPRESS HyperFlash model, the DS Signal is the same to RWDS.



The HyperFlash model behaves this way to conform to HyperFlash spec. The design reading the data from the HyperFlash model must delay the RWDS signal, and use the delayed-RWDS signal to sample the DQ. A delay of one Q_FDP0B should work fine, even in CAKE 1X mode. If you are using CAKE 1X mode and the HyperFlash clock is the fastest design clock, the DQ signal will change twice per FCLK, and the Q_FDP0B delaying RWDS will provide one-half FCLK delay, so that each delayed-RWDS edge is at the end of the corresponding data valid period.

To delay the RWDS signal, a commonly used approach is to create a special pad cell for RWDS that has a Q_FDP0B delay cell inserted on the path that leads from the HyperFlash memory into the design.

The user may insert delays into pad cells (or elsewhere in the design) using the below code example which leverages ixc_pulse, an internal primitive that can be used to access FCLK and to create controlled delay, for IXCOM flow and leverages the Q_FDP0B primitive for delay generation in the Classic ICE flow. For more detailed information about ixc_pulse please reference the *UXE User Guide* section called *Generating Pulses*. There is no need for the user to define IXCOM_UXE for the Verilog macro; it is predefined for the user in IXCOM flow. Note that in UXE 13.1.0 and prior the equivalent pulse generating function was named axis_pulse.

```
// Flow independent delay cell
module pxp_fclk_delay (in, out_delay);
input in;
output out_delay;

reg out_delay;

`ifdef IXCOM_UXE
  wire VCC=1'b1;
```

```
  ixc_pulse #(1)(Fclk,VCC);
  always @(posedge Fclk)
    out_delay <= in;
`else
  Q_FDP0B fclk_dly (.D(in), .Q(out_delay));
`endif

endmodule
```

Revision History

The following table shows the revision history for this document

Date	Version	Revision
March 2015	1.0	Initial release
March 2015	1.1	Update script example for IXCOM and ICE compile
June 2015	1.2	Remove limitation description about NOT check and prevent programing bit ‘0’ back to ‘1’
July 2015	1.3	Update Cadence naming on front page
Aug 2015	1.4	Update based on JUN 2015 spec, remove WP_n and ECC/CRC, remove 4MB/8MB configuration
September 2015	1.5	Added note about synthesis options. Remove watermark. Release model at MR level.
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming
October 2016	1.8	Rename port name RDS to RWDS
March 2017	1.9	Change model name to use lower case
September 2017	1.10	Add Cypress HyperFlash model support Add debug Signals for Cypress and Spansion HyperFlash model.
January 2018	2.0	Modify header and footer
June 2018	2.1	Add section for Manual configuration
July 2018	2.2	Update for new utility library