

Virtual TSA Intro Simplified

EBU APAC Application Engineering

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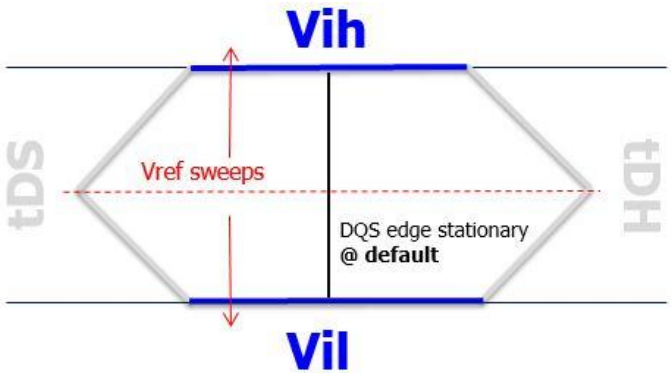


Virtual TSA – Sample Parameter Sweep...

- Using the memory controller interface to sweep each channel from $-n$ to $+m$ of the nominal set points of voltages, timing alignments, etc... provides a detailed matrix of the range of settings that result in a “pass” functionally.

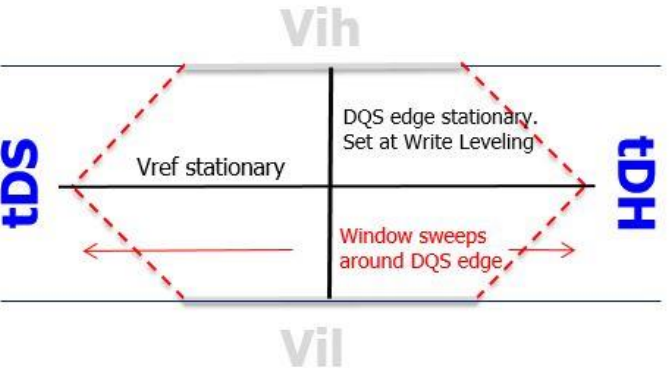
Vih/Vil → TxVHigh/TxVLow

- DQS placement set to 'default', obtained from training at nom conditions.
- System sweeps DRAM's VREF input, to find upper/lower edges write window.



tDS/tDH → TxLeft/TxRight

- System place's DRAM's Vref at nominal ($1/2V_{dd}$).
- DQS edge placement will sweep relative to data window to find pass/fail



Sample Memory Controls Needed for V-TSA

Parameters For LPDDR4
DRAM Vref_CA
DRAM Vref_DQ
DRAM DQ Voh
DRAM Drive Strength
DRAM CA ODT
DRAM DQ ODT
Controller CA Voh
Controller DQ Voh
Controller CA Drive Strength
Controller CK Drive Strength
Controller DQ Drive Strength
Controller DQS Drive Strength
Controller DQ ODT
Controller’s trained value for the centered tDQS2DQ per byte lane for writes... along with the right & left boundaries.
Controller’s trained value for the edge aligned tDQS2DQ per byte lane for reads... along with the right & left boundaries.



