Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

QDR/QDRII/QDRII+
Palladium Memory Model
User Guide

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

DDR2 Memory Model

1. Introduction

The Cadence Palladium QDR Model is available in several configurations with model sizes to match real devices manufactured by Samsung. Different sizes from 18Mb up to 72Mb are available, please consult the memory model catalog for the current available list.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations

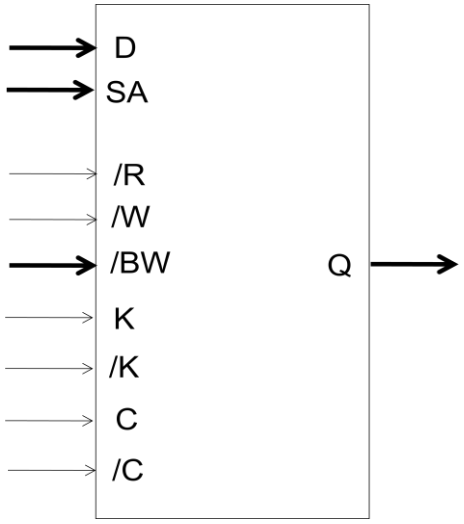
The following table lists the possible configurations. Not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Part Number	Density	Organization
K7S3236U4C	36M bit	1Mx36
K7S3218U4C	36M bit	2Mx18
K7S3236T4C	36M bit	1Mx36
K7S3218T4C	36M bit	2Mx18
K7S1636U4C	18M bit	512Kx36
K7S1618U4C	18M bit	1Mx18
K7S1618T4C	18M bit	1Mx18
K7R643682M	72M bit	2Mx36
K7R641882M	72M bit	4Mx18
K7R640982M	72M bit	8Mx9
K7R643684M	72M bit	2Mx36
K7R641884M	72M bit	4Mx18
K7R323682C	36M bit	1Mx36
K7R321882C	36M bit	2Mx18
K7R320982C	36M bit	4Mx9
K7R323684C	36M bit	1Mx36
K7R321884C	36M bit	2Mx18
K7R320984C	36M bit	4Mx9
K7R163682B	18M bit	512Kx36
K7R161882B	18M bit	1Mx18
K7R160982B	18M bit	2Mx9
K7R163684B	18M bit	512Kx36
K7R161884B	18M bit	1Mx18
K7Q163662B	18M bit	512Kx36
K7Q161862B	18M bit	1Mx18
K7Q163664B	18M bit	512Kx36
K7Q161864B	18M bit	1Mx18

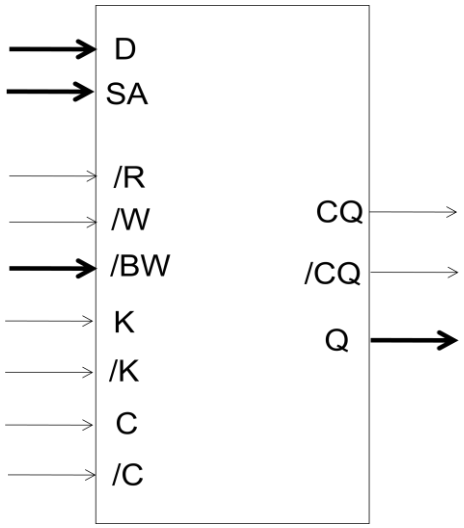
4. Model Block Diagram

The widths of the SA, D, BW, and Q buses are dependent on the density of the part being used.

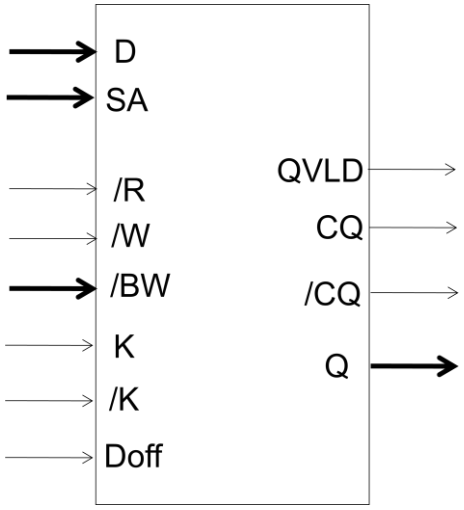
QDR SRAM:



QDRII SRAM:



QDRII+ SRAM:



5. Pin names

SYMBOL	DESCRIPTION
K, /K	Input Clock
C, /C	Input Clock for Output Data
CQ, /CQ	Output Echo Clock
/Doff	DLL Disable when low
QVLD	Q valid Output
SA	Address Inputs
D	Data Inputs
Q	Data Outputs
/W	Write Control Pin, active when low
/R	Read Control Pin, active when low
/BWx	Block Write Control Pin, active when low

6. Truth Table and Waveforms for Read/Write

6.1. QDR SRAM (burst length = 2)

K	/R	/W	D		Q		OPERATION
			D(A0)	D(A1)	Q(A0)	Q(A1)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	H-Z	H-Z	No Operation
↑	L	X	X	X	Dout at C(T+1)	Dout at /C(T+1)	Read
↑	X	L	Din at K(t)	Din at /K(t)	X	X	Write

The QDR operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maxmized as data can be transfered into sram on every rising edge of K and /K, and transfered out of sram on every rising edge of C and /C. And totally independent read and write ports eliminate the need for high speed bus turn around.

Address, data inputs, and all control signals are synchronized to the input clock (K or /K).Normally data outputs are synchronized to output clocks (C and /C), but when C and /C are tied high, the data outputs are synchronized to the input clocks (K and /K).
Read address is registered on rising edges of the input K clocks, and write address is registered on rising edges of the input /K clocks.

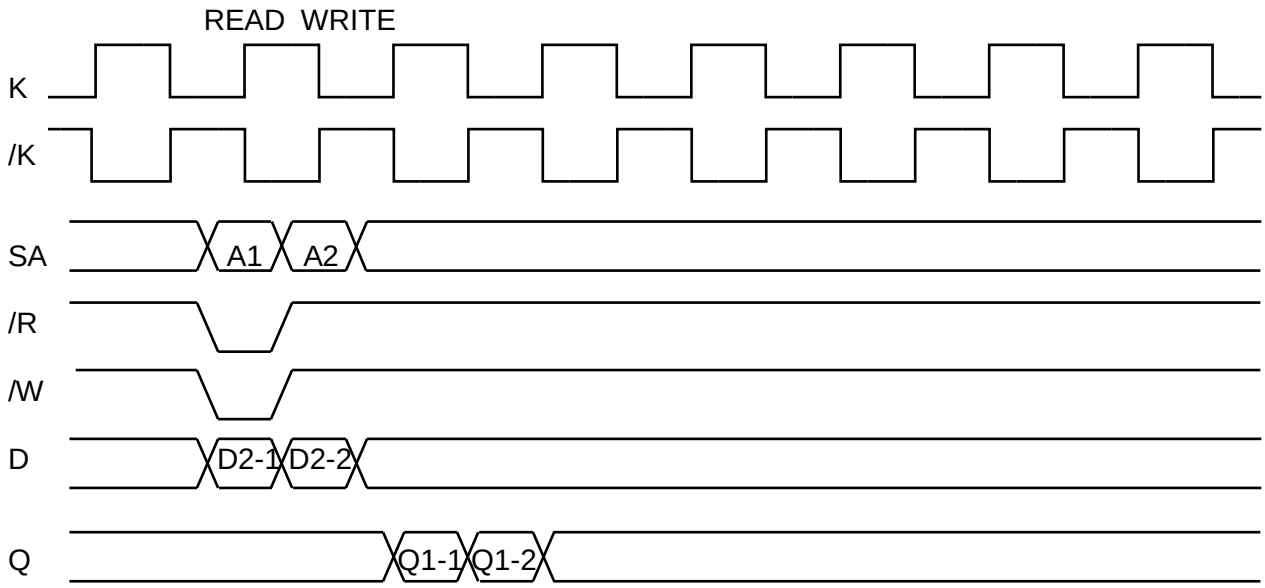
Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 2-bit sequential for both read and write operations.

Synchronous pipeline read and early write enable high speed operations.

Byte write operation is supported with BW0 and BW1 (BW2 and BW3) pins.

QDR Timing Waveforms (Burst Length =2)



6.2. QDR SRAM (burst length = 4)

K	/R	/W	D				Q				operation
			D(A1)	D(A2)	D(A3)	D(A4)	D(A1)	D(A2)	D(A3)	D(A4)	
Stopped	X	X	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Clock Stop
↑	H	H	X	X	X	X	H-Z	H-Z	H-Z	H-Z	No operation
↑	L	X	X	X	X	X	Dout at C (t+1)	Dout at /C (t+1)	Dout at C (t+2)	Dout at /C (t+2)	Read
↑	H	L	Din at K (t+1)	Din at /K (t+1)	Din at K (t+2)	Din at /K (t+2)	X	X	X	X	Write

QDR supports DDR (Dual Data Rate) read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of K and /K, and transferred out of SRAM on every rising edge of C and /C.
Address for read and write are latched on alternate rising edges of the input clock K.
Data inputs, and all control signals are synchronized to the input clock (K or /K).
Normally data outputs are synchronized to output clocks (C and /C), but when C and /C are tied high, the data outputs are synchronized to the input clocks (K and /K).

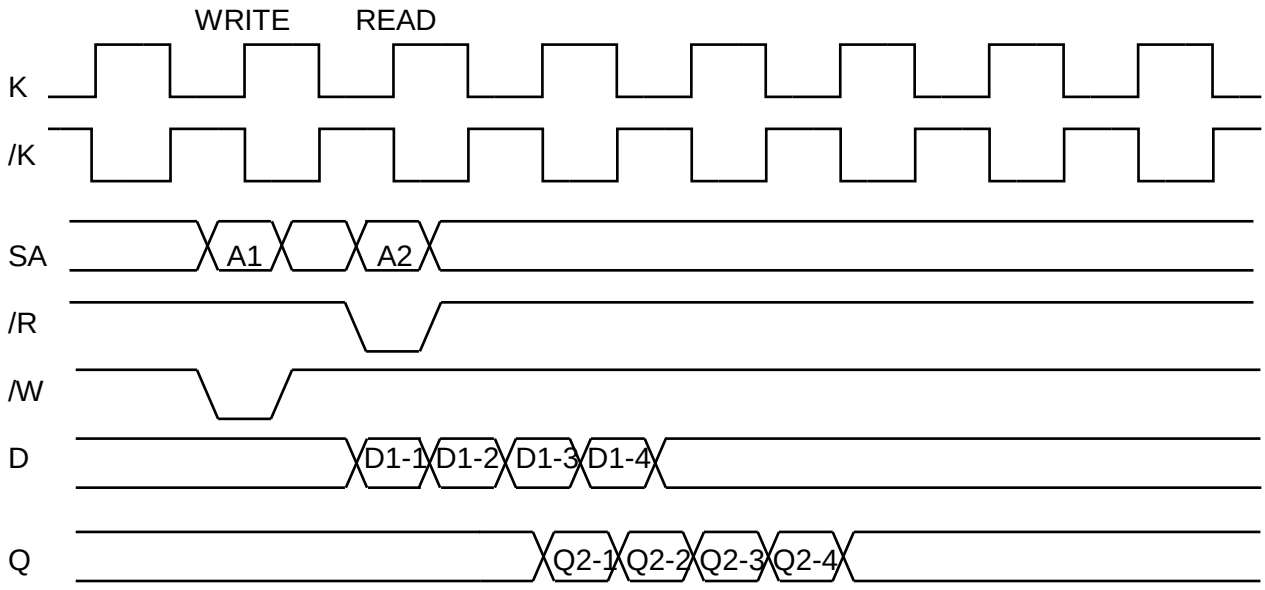
Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 4-bit sequential for both read and write operations, requiring tow full clock bus cycles.

Any request that attempts to interrupt a burst operation in progress is ignored.

Byte write operation is supported with BW0 and BW1 (BW2 and BW3) pins.

QDR Timing Waveforms(Burst length =4)



6.3. QDRII SRAM (burst length = 2)

K	/R	/W	D		Q		OPERATION
			D(A0)	D(A1)	Q(A0)	Q(A1)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	H-Z	H-Z	No Operation
↑	L	X	X	X	Dout at /C(T+1)	Dout at C(T+2)	Read
↑	X	L	Din at K(t)	Din at /K(t)	X	X	Write

QDR supports DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of K and /K, and transferred out of SRAM on every rising edge of C and /C.

Address, data inputs, and all control signals are synchronized to the input clock (K or /K).Normally data outputs are synchronized to output clocks (C and /C), but when C and /C are tied high, the data outputs are synchronized to the input clocks (K and /K).

Read data are referenced to echo clock (CQ or /CQ) outputs.

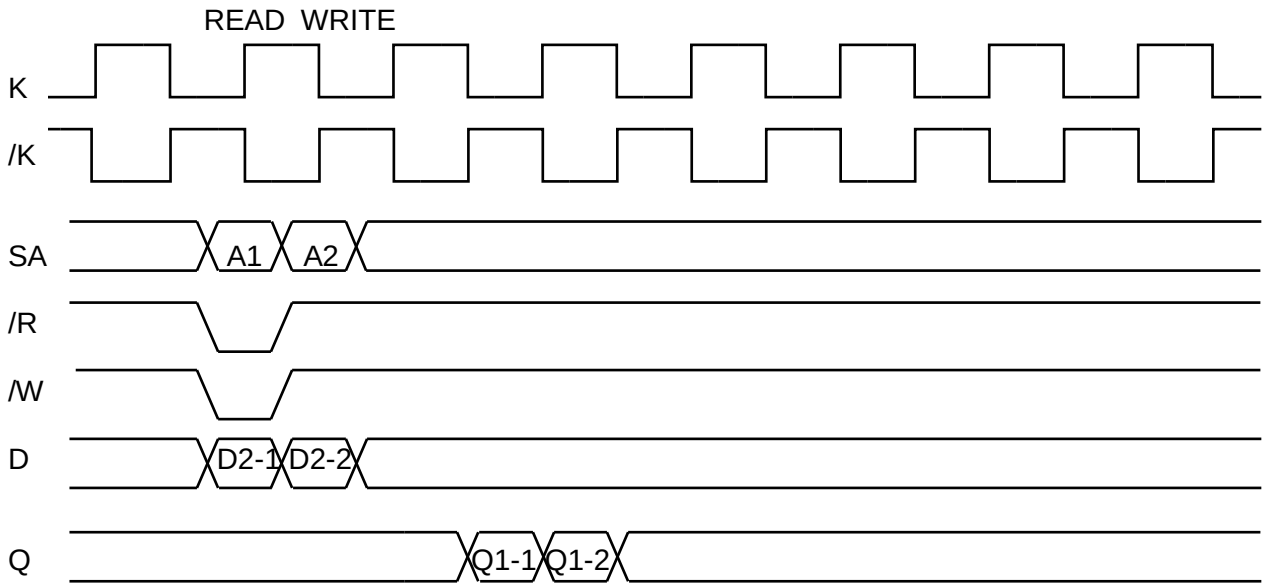
Read address is registered on rising edges of the input K clocks, and write address is registered on rising edges of the input /K clocks.

Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 2-bit sequential for both read and write operations.

Byte write operation is supported with BW0 and BW1(BW2 and BW3) pins for x18 (x36) device and only BW pin for x9 device.

QDRII Timing Waveforms (Burst Length=2)



6.4. QDRII SRAM (burst length = 4)

K	/R	/W	D				Q				operation
			D(A1)	D(A2)	D(A3)	D(A4)	D(A1)	D(A2)	D(A3)	D(A4)	
Stopped	X	X	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Clock Stop
↑	H	H	X	X	X	X	H-Z	H-Z	H-Z	H-Z	No operation
↑	L	X	X	X	X	X	Dout at /C (t+1)	Dout at C (t+2)	Dout at /C (t+2)	Dout at C (t+3)	Read
↑	H	L	Din at K (t+1)	Din at /K (t+1)	Din at K (t+2)	Din at /K (t+2)	X	X	X	X	Write

The QDR operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of K and /K, and transferred out of SRAM on every rising edge of C and /C. And totally independent read and write ports eliminate the need for high speed bus turn around.

Address for read and write are latched on alternate rising edges of the input clock K. Data inputs, and all control signals are synchronized to the input clock (K or /K). Normally data outputs are synchronized to output clocks (C and /C), but when C and /C are tied high, the data outputs are synchronized to the input clocks (K and /K). Read data are referenced to echo clock (CQ or /CQ) outputs.

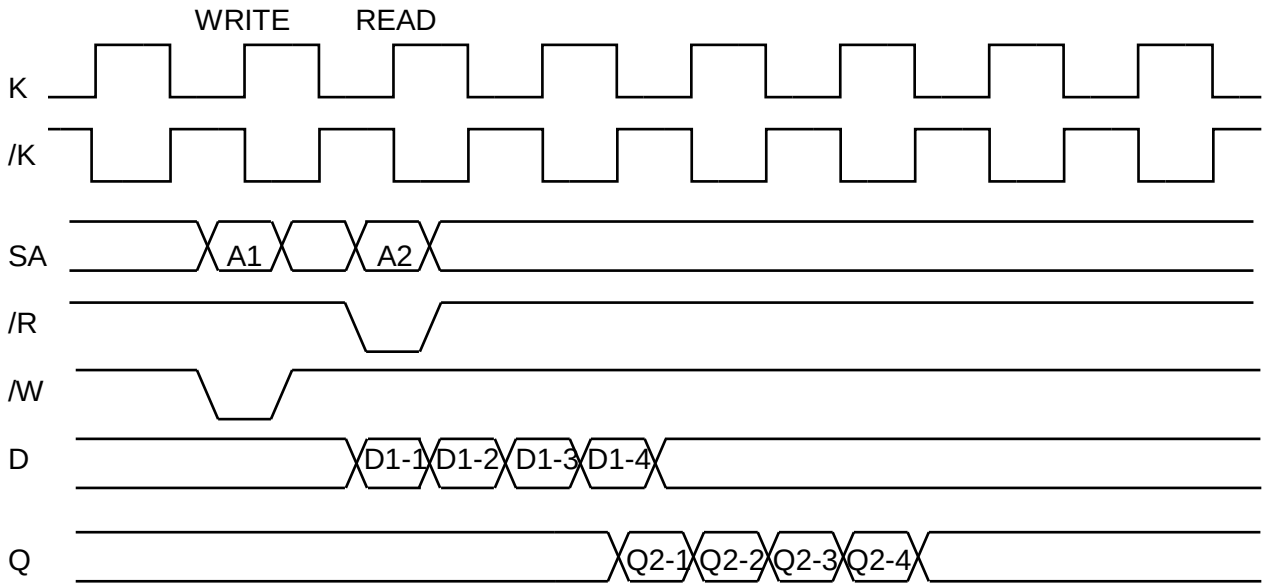
Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 4-bit sequential for both read and write operations, requiring tow full clock bus cycles.

Any request that attempts to interrupt a burst operation in progress is ignored.

Byte write operation is supported with BW0 and BW1 (BW2 and BW3) pins.

QDR II Timing Waveforms (Burst length=4)



6.5. QDRII+ SRAM (burst length = 4)

K	/R	/W	D				Q				operation
			D(A1)	D(A2)	D(A3)	D(A4)	D(A1)	D(A2)	D(A3)	D(A4)	
Stopped	X	X	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Clock Stop
↑	H	H	X	X	X	X	H-Z	H-Z	H-Z	H-Z	No operation
↑	L	X	X	X	X	X	Dout at C (t+2)	Dout at /C (t+2)	Dout at C (t+3)	Dout at /C (t+3)	Read
↑	H	L	Din at K (t+1)	Din at /K (t+1)	Din at K (t+2)	Din at /K (t+2)	X	X	X	X	Write

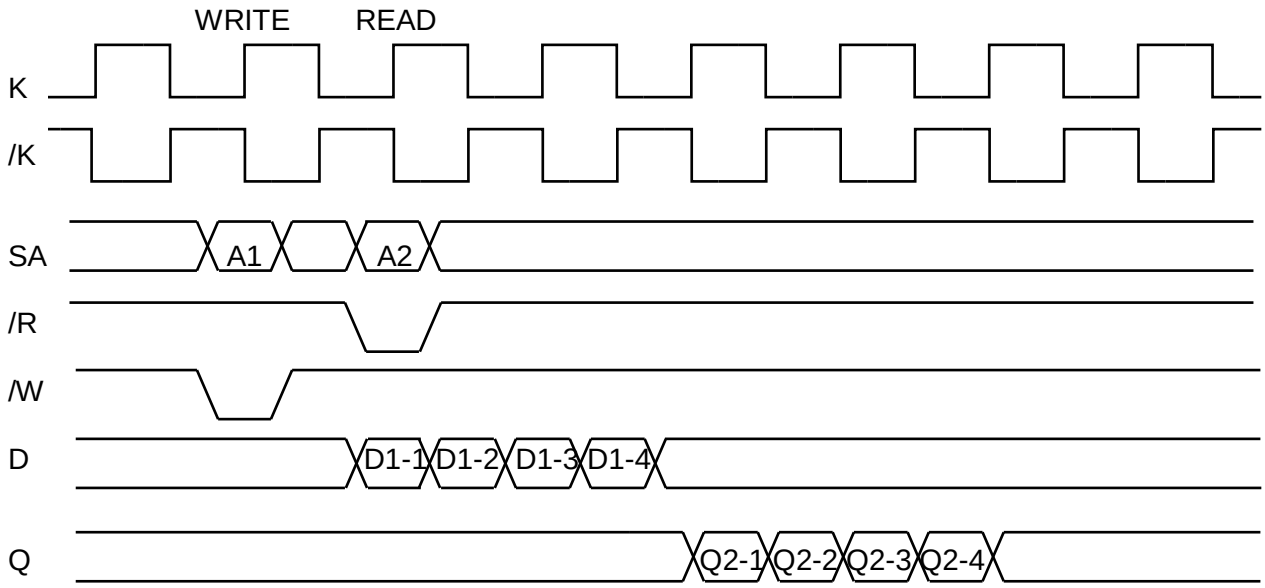
QDR supports DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into and out of SRAM on every rising edge of K and /K. And totally independent read and write ports eliminate the need for high speed bus turn around.

Address for read and write are latched on alternate rising edges of the input clock K. Data inputs, data output, and all control signals are synchronized to the input clock (K or /K). Read data are referenced to echo clock (CQ or /CQ) outputs. Common address bus is used to access address both for read and write operations. The internal burst counter is fixed to 4-bit sequential for both read and write operations, requiring two full clock bus cycles. Any request that attempts to interrupt a burst operation in progress is ignored.

Synchronous pipeline read and late write enable high speed operations. Simple depth expansion is accomplished by using R and W for port selection.

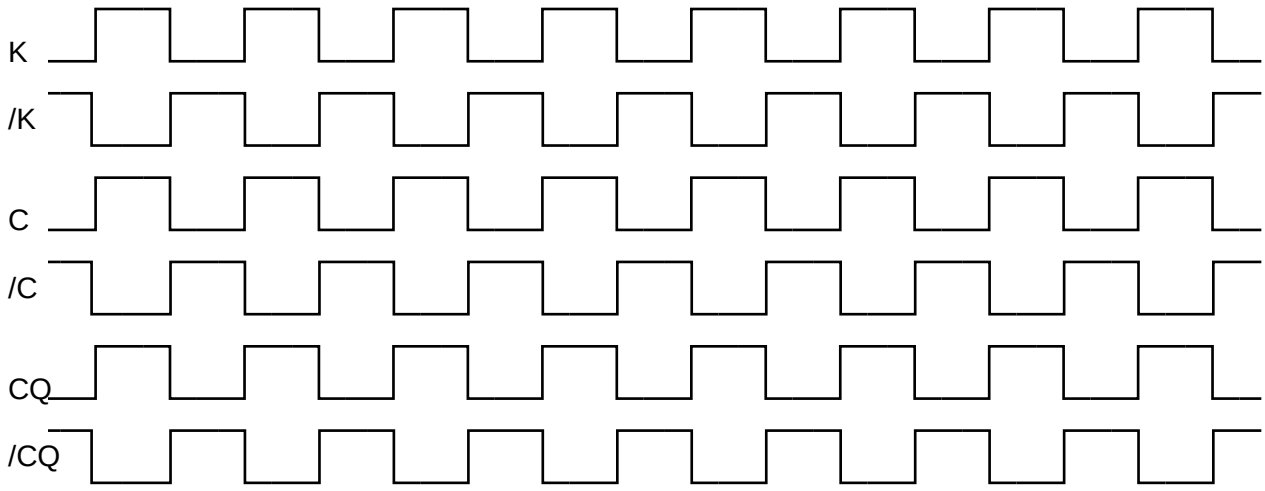
Byte write operation is supported with BW0 and BW1 (BW2 and BW3) pins

QDRII+ Timing Waveforms (Burst Length =4)



7. Clocks

For QDR/QDRII/QDRII+ models provided by Cadence for Palladium, We usually don't care about the time delay and the internal DLL for phase adjustment, so the K, C and CQ signals are exactly the same, so do the /K , /C and /CQ.



8. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) of this model in the IXCOM flow is shown below.

```
ixcom -ua +dut+k7q161862b \
    ./ k7q161862b.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile k7q161862b.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog k7q161862b.vg
```

```
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
k7q161862b
……

2)
vavlog jedec_wideio_1gb_128bit_4ch_1rank.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog k7q161862b.vg
k7q161862b
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

Revision History

The following table shows the revision history for this document

Date	Version	Revision
July 2010	1.0	Initial version
June 2011	1.1	Updated with “Related Documents” information
July 2014	1.2	Repaired doc title property. Added revision history. Updated legal.
September 2014	1.3	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.4	Remove emulation capacity info. Update related publications list.
July 2015	1.5	Update Cadence naming on front page
September 2015	1.6	Add compile and emulation section
January 2016	1.7	Update for Palladium-Z1 and VXE
July 2016	1.8	Remove hyphen in Palladium naming
January 2018	1.9	Modify header and footer
July 2018	2.0	Update for new utility library