Horizon Package Review: X2A

dwc_ap_lpddr4x_mphy_tsmc16ffc18: LPDDR4/4x,DDR4 at 4266MT/s

Synopsys SIPI Team

31/03/2020

CONFIDENTIAL INFORMATION

The information contained in this presentation is the confidential and proprietary information of Synopsys. You are not permitted to disseminate or use any of the information provided to you in this presentation outside of Synopsys without prior written authorization.

IMPORTANT NOTICE

In the event information in this presentation reflects Synopsys' future plans, such plans are as of the date of this presentation and are subject to change. Synopsys is not obligated to update this presentation or develop the products with the features and functionality discussed in this presentation. Additionally, Synopsys' services and products may only be offered and purchased pursuant to an authorized quote and purchase order or a mutually agreed upon written contract with Synopsys.

WARRANTY DISCLAIMER

THIS REPORT AND ALL INFORMATION CONTAINED IN THIS REPORT ARE PROVIDED “AS IS” WITHOUT WARRANTY, INDEMNIFICATION OR SUPPORT OF ANY KIND, AND SYNOPSYS MAKES NO OTHER WARRANTIES EXPRESS, IMPLIED, STATUTORY OR OTHERWISE REGARDING SUCH INFORMATION. SYNOPSYS SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT, OR ARISING FROM A COURSE OF DEALING OR USAGE OF TRADE.

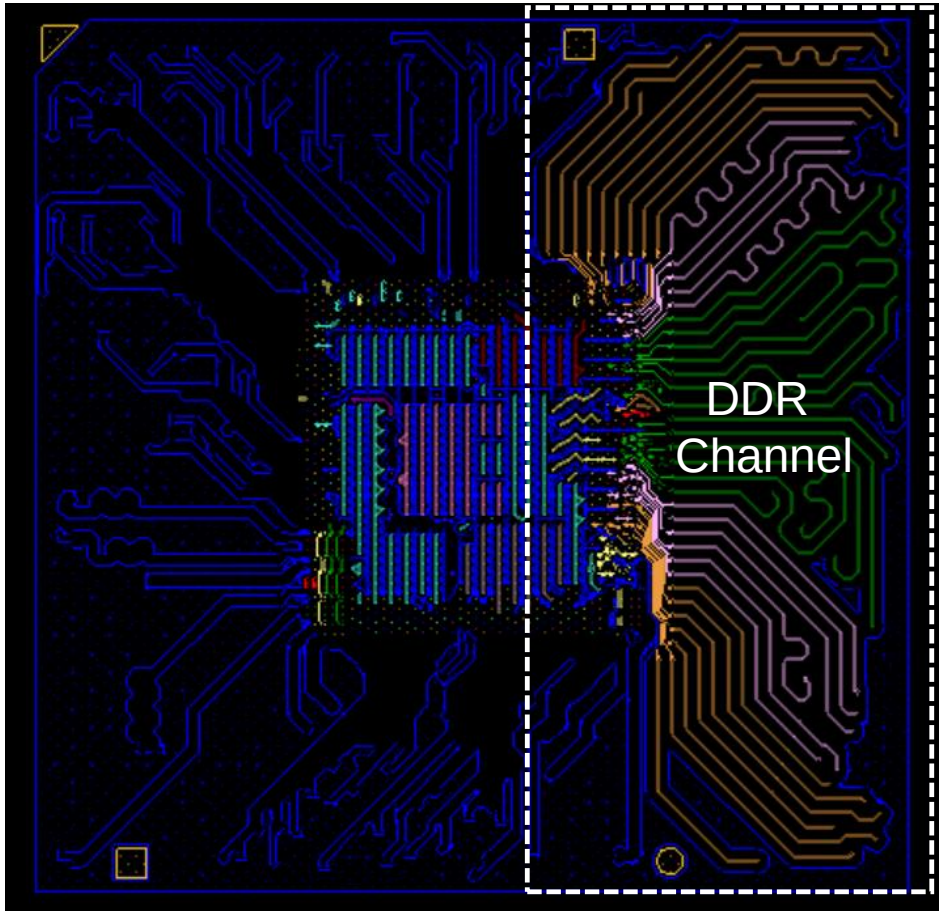
Reference documentation

- Documents used in the review:
  - dwc_lpddr4x_multiphy_signal_integrity_application_note.pdf
  - dwc_ap_lpddr4x_multiphy_tsmc16ffc18_databook.pdf

- Data provided by customer
  - SIPI_review_request_form_from_Horizon_20200320.xlsx
  - Horizon_X2aJ2a_Trace Length Report_20190815_(Security C).xlsx
  - A27611-A_20200317.sip
  - Substrate material data.xlsx
  - Substrate-X-Section.pptx

Interface Overview

- Signal routing: L1,L3 & L6.
- Protocols used: LPDDR4/4X, DDR4
- Bus Width: 32b
- Rank: 2
- Data rate : 4266Mbps
- Interface details :
  1. Discrete LPDDR4/LPDDR4x x32 on board or
  2. Discrete DDR4 x16 on board
- List of signals:
  - BP_A[0-38]
  - BP_D[0-46]
  - BP_ZN , BP_ALERT_N, BP_MEMRESET_L
- List of Supply nets
  - VDD_DDR, VDDQ_DDR, VDDQLP,BP_VREF,VAA, VSS



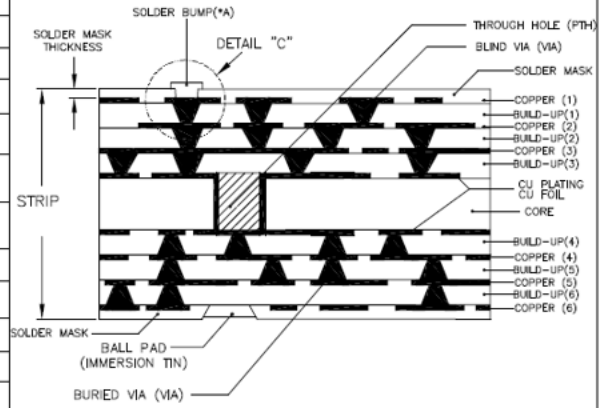
Package Review

- Stack-up
- Impedance matching
- Spacing guidelines
- Signal spacing
- Signal routing
- Power distribution
- Conclusion

Stack-up

Subclass Name	Type	Material	Thickness (UM)	Tol +	Tol -	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent
	SURFACE	AIR				0	3.8	0
UBM_Z1-DIE1	DIESTACK							
	DIELECTRIC	FR-4	1.000000	0	0	0	5.2	0.004
TOP-PRESOLDER	DIELECTRIC	FR-4	1.000000	0	0	0	5.2	0.004
SM-TOP	DIELECTRIC	FR-4	25.000000	0	0	0	5.2	0.004
CU-1	CONDUCTOR	COPPER	15.000000	0	0	580000	5.2	0.004
DRILL12	DIELECTRIC	FR-4	30.000000	0	0	0	4.5	0.035
CU-2	CONDUCTOR	COPPER	15.000000	0	0	595900	4.5	0
DRILL23	DIELECTRIC	FR-4	30.000000	0	0	0	4.5	0.035
CU-3	CONDUCTOR	COPPER	15.000000	0	0	595900	5.2	0.004
DRILL34	DIELECTRIC	FR-4	30.000000	0	0	0	4.5	0.035
CU-4	CONDUCTOR	COPPER	18.000000	0	0	595900	4.5	0.035
DRILL45	DIELECTRIC	FR-4	800.000000	0	0	0	4.5	0.035
CU-5	CONDUCTOR	COPPER	18.000000	0	0	595900	5.2	0.004
DRILL56	DIELECTRIC	FR-4	30.000000	0	0	0	4.5	0.035
CU-6	CONDUCTOR	COPPER	15.000000	0	0	595900	4.5	0
DRILL67	DIELECTRIC	FR-4	30.000000	0	0	0	4.5	0.035
CU-7	CONDUCTOR	COPPER	15.000000	0	0	595900	4.5	0.035
DRILL78	DIELECTRIC	FR-4	30.000000	0	0	0	5.2	0.004
CU-8	CONDUCTOR	COPPER	15.000000	0	0	580000	1	0
SM-BTM	DIELECTRIC	FR-4	25.000000	0	0	0	4.5	0.035
	SURFACE	AIR				0	1	0

DESCRIPTION		MATERIAL	THICKNESS	FIGURE
FINISHED THICKNESS			1156+/-100	
PRE-SOLDER		SAC305 Ultra low alpha: ≤ 0.002 cph/cm²	(*A)	
METAL FINISH	BUMP PAD		SDP	
	BALL PAD	IMMERSION TIN	1MIN.	
	OTHER (*B)	IMMERSION TIN	1MIN.	
SOLDER MASK		SR7300GR	25+/-10 (ON CU)	
COPPER THICKNESS (1X2X3X4X5X6)			15+/-5	
BUILD-UP THICKNESS (1X2X3X4X5X6)		ABF-GX92	30+/-6	
CU PLATING + CU FOIL			18+/-8	
CORE		E-700GR	800+/-60	
COPPER THICKNESS IN PTH HOLE		MECHANICAL	10MIN	
COPPER THICKNESS IN BLIND VIA		LASER	FILLED	
Core Plugging Material		----		
DIMPLE			15 MAX.	



- Suggest to reduce the Core layer thickness from 800u to 400-600u to keep core via length short and reduce inductance of power/VSS vias loop.
- Longer vias can contribute to higher power net loop inductance (need to make sure return vias are close to power vias) and may result in higher supply noise

- For operation above 3200Mbps, microstrip routing should be avoided. Since the signals routed in microstrip are exposed to a mixed dielectric environment, crosstalk will create timing differences among the different coupling modes. This will result in far end cross-talk that will erode the timing margins. Strip-line configuration is recommended for routing the channels.

Impedance matching

- Signals should have a proper reference plane to define a controlled characteristic impedance and the line impedance should be according to standard requirements
  - For signals within the same group, differential impedance should be twice the impedance of the single-ended ones.
- Signals should have a proper reference plane: routing over plane gaps and/or plane splits should be avoided
  - Impedance mismatches will lead to unwanted reflections.

Spacing guidelines

- Synopsys recommendation for trace spacing is:
  - 2 times the distance to the reference plane, for signals within the same group
  - 3 times the distance to the reference plane, for signals of different groups

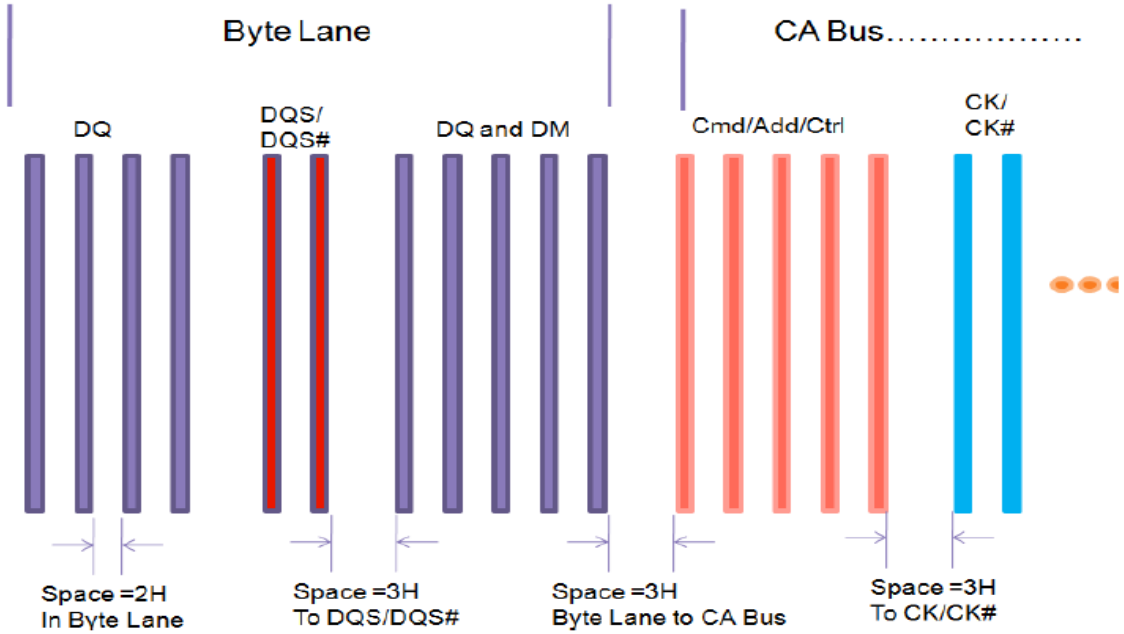


Figure 18: Spacing between Different Signal Groups (Relative to height from reference plane)

Note *If possible, spacing greater that 2H between signals should be used. This will further reduce the impact of crosstalk on timing in microstrip structures. In stripline, however, narrower spacing than 2H may be acceptable as the impact on timing is much reduced since mode velocities are equal.*

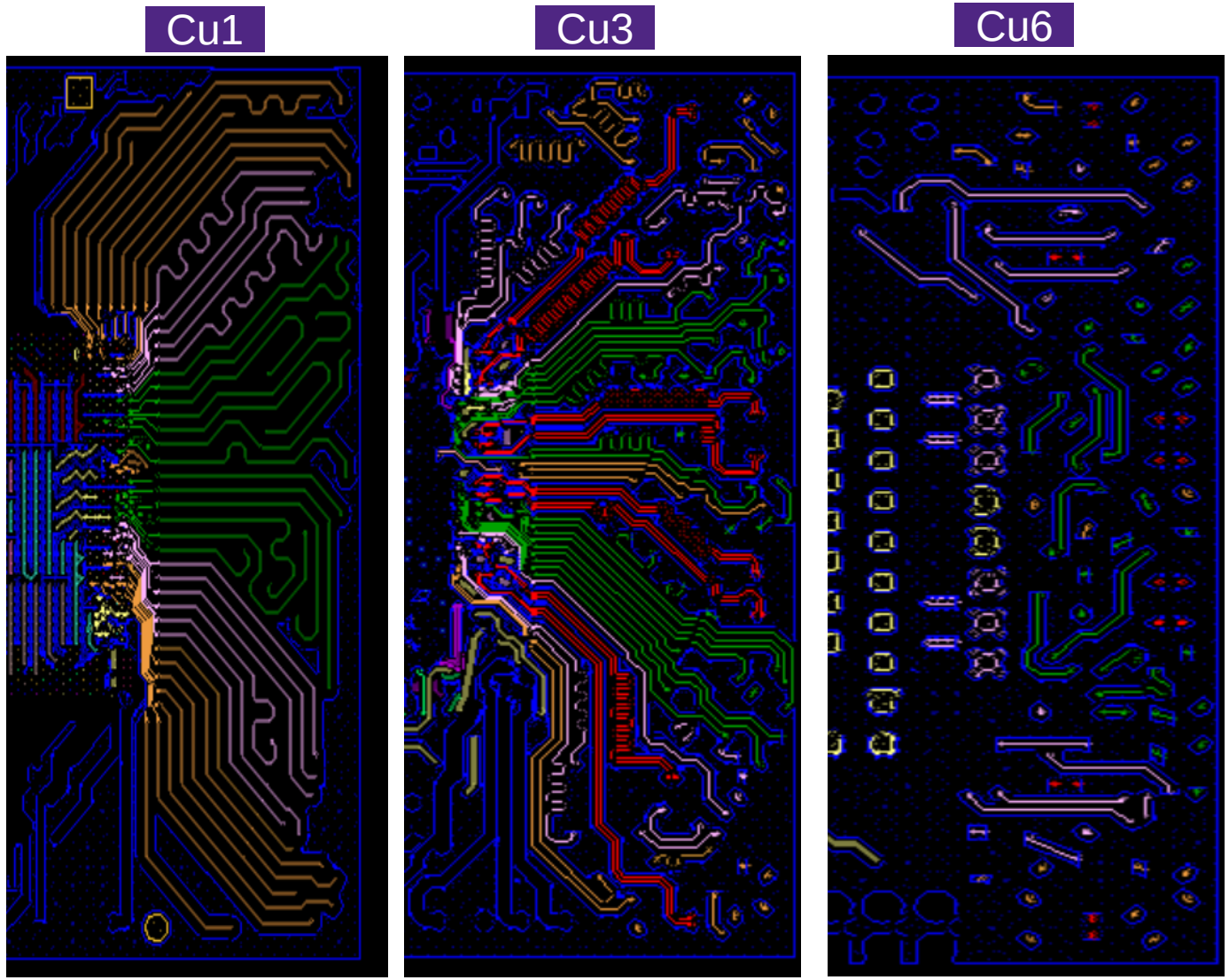
Signal spacing

- Guidelines for separation of signals within same group (≥2H) and from different group (≥3H) should be followed
- The signal spacing between DQ and DQS within a byte should also be >=3H
  - Signal Integrity of the signals will be affected due to crosstalk
- H is the distance to closest reference plane
- Based on measured spacing between signals within same group and different groups, Signal Integrity will be affected due to small spacing between traces
- Impact of the crosstalk on the performance of the interface should be confirmed by simulations with extracted model

Signal routing

- Microstrip layer routing is not recommended for the signals beyond 3200MT/s!
- Signals of a group-DQ-DQS in a byte lane/CA-CLK are synchronous and recommended to route in same layer.
- Signals in a byte should have same no.of vias & layer changes
- Die break out region also concerns as spacing very tight.

Routing is not as per the recommendation



Signal spacing

- ≥3H spacing should be followed between the signals of different group. (H-Height from the reference plane)
- The impact of spacing must be assessed by running crosstalk simulations

Net name	Closest Ref plane Height (H) in um	Provided Spacing (as per PCB)	Synopsys Recommendation
			3* Height (H)
BP_A3 to BP_D16	30	75	90

Spacing is not as per the recommendation

Signal routing

- Signals should have a proper reference plane: routing over plane gaps and/or plane splits should be avoided. Routing over splits can lead to,
  - Reflections due to impedance mismatches over the splits.
  - Excessive crosstalk due to absence of proper reference.
  - DQ/DQS are double data rate signals and usually have smaller timing margins and it’s preferable to route them over the VSS planes where there are no splits.
  - ADD/CMD/CTRL are single rate signals and can have a combination of both VDDQ and VSS layers as reference. Clock also has to be routed on the same layer since it’s synchronous with ADD/CMD/CTRL group. However a sign off on this should be done only after simulation run and quantifying whether the impact of the split/noise is acceptable on the eye margins.

Skew control overview

- Intra-pair skew
  - Differential signals (CK/CK# and DQS/DQS#) routing length should be skew matched
- Total delay should be accounted for and matched, considering complete interface
  - RDL + Package + PCB
- LPDDR4/4x Skew Requirements:

System Routing requirements for LPDDR4/4X 4267 operation			
Constraints	**Available Deskew Range**	**Recommended Routed Skew Limits**	**Notes**
DQ to DQ arrival time mismatch within a byte or nibble	<200 ps	<20 ps	It is highly recommended that flight times across the data lanes be tightly matched in order to preserve operating margin and reduce vertical eye collapse that can occur from crosstalk between unaligned DQ signals.
DQ to DQS domain	DQS position +/-100 ps	DQS position +/-10 ps	
CS, ODT, CKE, Cmd, Add to CK/CK#	Not applicable	CK position +/-25 ps	PHY can be programmed to add delay to 4 bit groups of AC signals to address potential skew violations.
DQS to CK domain	-0.5 to +5.47 Clock Cycles	CK edge position +/-60 ps (without Write Leveling)	Write Leveling training can compensate for delay differences that extend over multiple clock cycles.

Table 4: Summary of Outing Skew Requirements for LPDDR4

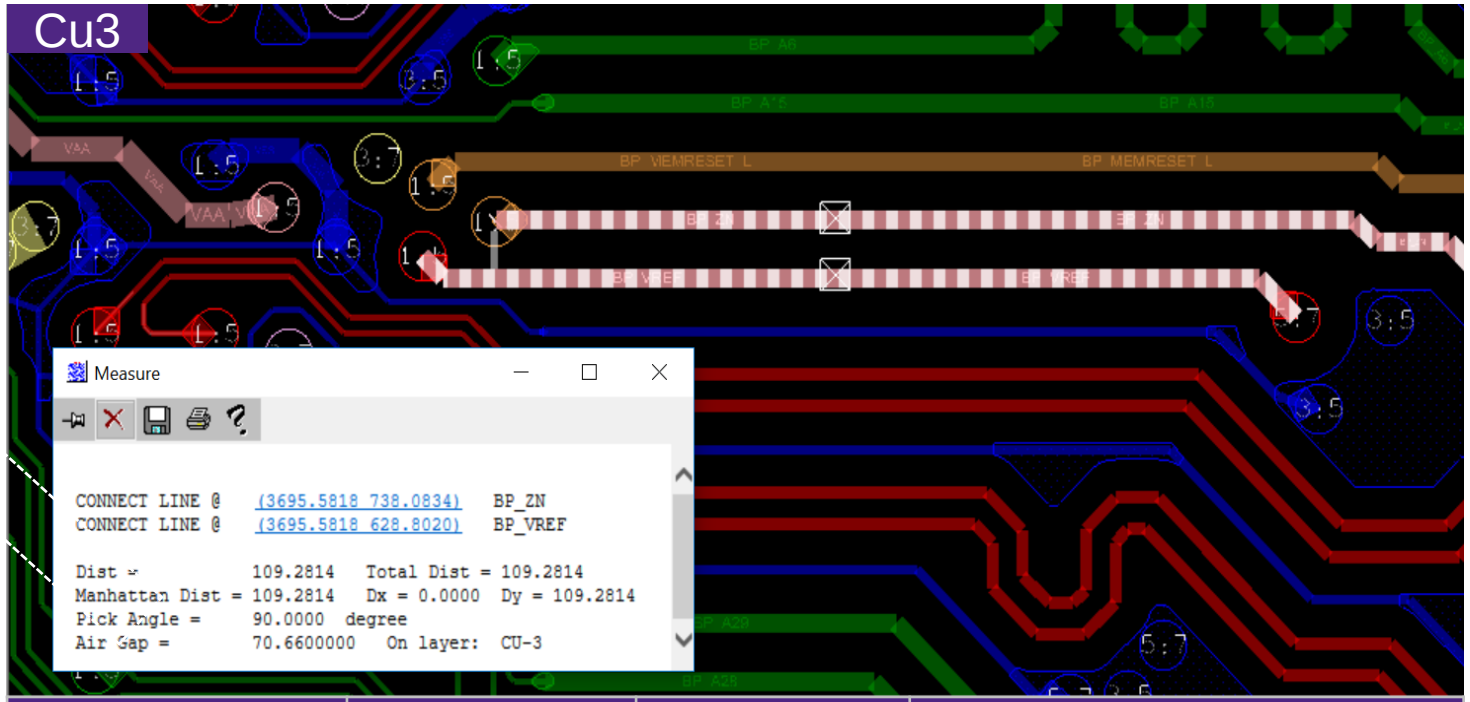
Propagation Delay Difference (Calculated)

- The provided trace length data is not clear about the byte lane groups (DQ/DQS), differential clock & CAA Signals to calculate the propogation delay difference.
- The total skew must be calculated taking into account the RDL,Package & PCB skews.

Simulation results and calculation of timing budget tables considering all the contributions [RDL + Package + PCB] will allow us to understand the impact on the margins and on the performance of the interface.

Vref spacing

- Requirement is ≥ 3H to adjacent traces. H is the distance to the nearest reference plane.

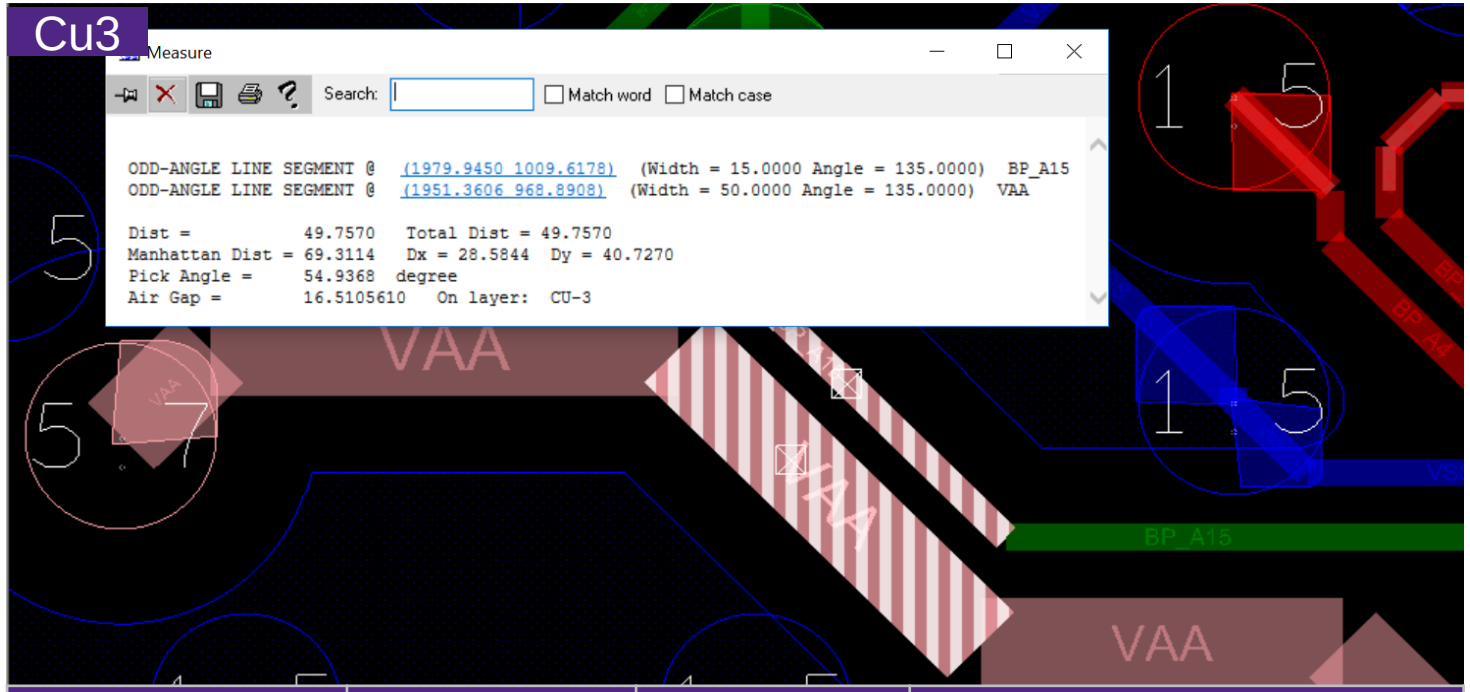


Net name	Closest Ref plane Height (H) in um	Provided Spacing (as per PCB)	Synopsys Recommendation	
			3* Height (H)	4* Height (H)
BP_ZN to BP_VREF	30	70.6	90	120

Spacing is not as per the recommendation

PLL spacing

- Requirement is ≥ 3H to adjacent traces. H is the distance to the nearest reference plane.



Net name	Closest Ref plane Height (H) in um	Provided Spacing (as per PCB)	Synopsys Recommendation	
			3* Height (H)	4* Height (H)
VAA to BP_A15	30	16.5	90	120

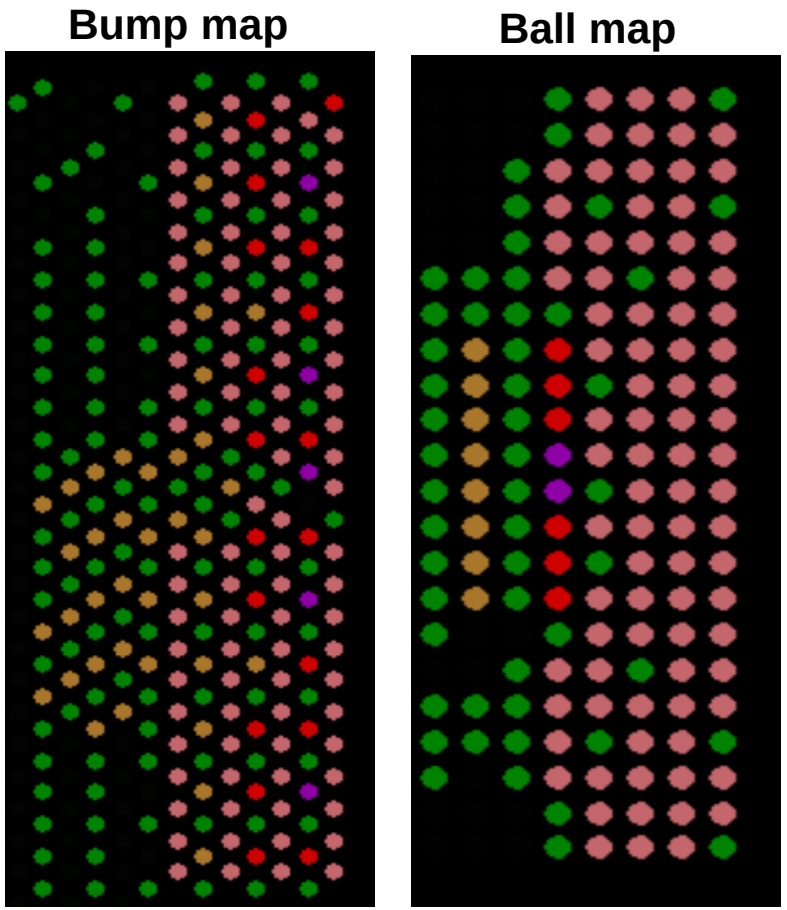
Spacing is not as per the recommendation

Power Distribution Considerations

- The power bumps should well distributed around the interface
- The number of vias through a layer and balls are at least half of the number of bump connections
- The number of ball are at least half of the number of bumps
- There should not be excessive slotting in the power planes

Power Distribution

	Provided		
Net Name	BGA Balls	Bumps	~Vias
VDDQ_DDR	6	18	32
VDDQLP	2	5	8
VDD_DDR	8	36	53
VSS	52	101	436



With 68 Highspeed Signals:
6 VDDQ BGAs. That calculates to 68/8 = 8.5 signals per VDDQ_DDR BGA.
2 VDDQLP BGAs which calculates to 68/2 = 34 signals per VDDQLP BGA

By comparison the 200ball lpddr4x DRAM used on the board has..
68 signals
24 VDD2 BGAs (VDDQ). This calculates to 68/24 = 2.8 signals per VDDQ BGA
20 VDDQ BGAs (VDDQLP). This calculates to 68/20 = 3.4 signals per VDDQLP BGA.

Recommended to approach these ratios for VDDQ (3:1:1). There is more margin for VDDQLP since the ripple spec is higher (+/-5%)

Power Distribution (Contd..)

- 70-100pH target for the package + PCB VDDQ inductance. It‘s contribution to PSIJ is more important than that of VDDQLP. it will depend on CDie used and it is also recommended for placing low inductance package cap footprints onto the package.
- Customer must account for all current contributions for any circuit powered by VDD_Core and analyze the Power Delivery Network
- There is no de-coupling capacitor place holders found in the package for the VDDQ & VDD rails.
- PDN analysis including transient simulations must be performed to validate Vripple specs are met.
- Risk is high to fail ripple spec if no on package cap properly implemented!

Summary

- PI analysis is advised on all supply nets and it should meet the Synopsys Guideline.
  - De-coupling capacitor place holders are not found for VDDQ/VDD, Highly recommended to analyze the Voltage ripple performance of the PDN.
- Guidelines for separation between signals of different groups are not being followed
  - High crosstalk will affect the overall performance of the interface
  - Routing distance between traces should be increased as much as possible
  - Design should be extracted and simulated to validate current implementation
- The total skew must be calculated taking into account the RDL,Package & PCB skews and it should meet the synopsys guidelines.
- SNPS has identified potential improvements on the PCB design. However, by visual inspection alone, it is not possible to determine whether the design is robust enough to meet all system specifications

<u>The design must be signed off based on design extraction, modeling and system level SI/PI simulation</u>

SYNOPSYS®
Silicon to Software™

Thank You


SYNOPSYS®
Silicon to Software™