DFI

DDR PHY Interface

DFI 3.1 Specification

MARCH 21, 2014

Release Information

Rev #	Date	Change
1.0	30 Jan 2007	Initial Release
2.0	17 Jul 2007	Modifications/Additions for DDR3 Support
2.0	21 Nov 2007	Additional modifications/additions for DDR3 support. Added read and write leveling. Changes approved by the Technical Committee for DDR3 support.
2.0	21 Dec 2007	Removed references to data eye training for PHY Evaluation mode, added a gate training-specific mode signal, corrected references and clarified read training.
2.0	11 Jan 2008	Modified wording; standardized notations in figures, clarified terminology for read and write leveling.
2.0	26 Mar 2008	Added timing parameter t_{rdlvl_en} and t_{wrlvl_en}, signal dfi_rdlvl_edge.
2.1	2 Oct 2008	Added initial LPDDR2 support and corrected minor errors from 2.0 release.
2.1	24 Nov 2008	Added frequency change protocol, signal timing definitions, t_{rdlvl_load} and t_{wrlvl_load} timing parameters and adjusted diagrams accordingly.
2.1	30 Jan 2009	Added DFI logo.
2.1	31 Mar 2009	Updated width of dfi_rdlvl_edge, corrected erroneous figures, updated t_{rdlvl_en} and t_{wrlvl_en} definitions.
2.1	20 May 2009	Added low power control interface, modified leveling request signal description to include frequency change, added dfi_data_byte_disable signal and t_{phy_wrdata} timing parameters. Added DIMM support to the status interface and updated frequency ratios from an example to a defined method. Updated frequency ratios information for new proposals, modified default values and requirements for some training interface signals, incorporated LPDDR2 training operations changes
2.1	22 Jun 2009	Expanded frequency ratio information to include vectored read data, expanded use of dfi_init_start, added timing diagrams for 1:4 frequency ratio systems
2.1.1	23 Mar 2010	Added reference to the parity interface to the Overview. Changed dfi_parity_in signal to have a phase index. Modified description of dfi_freq_ratio signal to make it optional except for MCs/PHYs that support multiple frequency ratios. Expanded figure 32 into two figures to represent odd and even timing parameters.
2.1.1	01 Apr 2010	Changed minimum value for t_{lp_wakeup}.
2.1.1	20 Apr 2010	Corrected figure 3 timing violation. Corrected erroneous sentence for 2T timing. Corrected figure 35 t_{phy_wrlat} timing. Correct incorrect references to t_{phy_wrlat} in frequency ratio read examples.
2.1.1	27 May 2010	Added Figure 4 and text to explain differences between Figure 3 and 4.
2.1.1	09 Jun 2010	Modified text in dfi_init_start and surrounding figures 3 and 4 for more clarity.
3.0	21 May 2012	Added DDR4 DRAM support for: CRC, CA parity timing, CRC and CA parity errors, DBI, leveling support, and CA modifications. Added DFI read data rotation clarification, read data pointer resynchronization, independent timing of DFI read data valid per data slice, data path chip select, error interface, and programmable parameters. Renamed PHY evaluation mode. Removed MC evaluation mode and $\mathbf{t_{phy\_wrdelay}}$ timing parameter. Added support for refresh during training, multiple CS training, enhancements to the update interface and the idle bus definition
3.1	19 May 2012	Added support for LPDDR3. Enhanced the Low Power Control Interface to have separate control and data requests. Added the PHY-Requested Training Interface to enable PHY-independent training in non-DFI training mode.
--	14 Nov 2013	Synchronized book files to 3.1 in advance of upcoming changes from JM.

--	21 Nov 2013	Incorporated review corrections.
--	21 Mar 2014	Incorporated committee comments, corrected erroneous cross references, fine-tuned formatting, fine-tuned typographical items.

Proprietary Notice

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Cadence.

Cadence makes no warranties with respect to this documentation and disclaims any implied warranties of merchantability or fitness for a particular purpose. Information in this document is subject to change without notice. Cadence assumes no responsibility for any errors that may appear in this document.

Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy, or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

RESTRICTED RIGHTS LEGEND

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraphs (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013.

Destination Control Statement

All technical data contained in this product is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Trademarks

Cadence and the Cadence logo are registered trademarks of Cadence Design Systems, Inc.

All other products or brand names mentioned are trademarks or registered trademarks of their respective holders.

End User License Agreement2

1.Subject to the provisions of Clauses 2, 3, 4, 5 and 6, Cadence hereby grants to licensee ("Licensee") a perpetual, nonexclusive, nontransferable, royalty free, worldwide copyright license to use and copy the DFI (DDR PHY Interface) specification (the "DFI Specification") for the purpose of developing, having developed, manufacturing, having manufactured, offering to sell, selling, supplying or otherwise distributing products which comply with the DFI Specification.

2.THE DFI SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES EXPRESS, IMPLIED OR STATUTORY, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF SATISFACTORY QUALITY, MERCHANTABILITY, NONINFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE.

3.No license, express, implied or otherwise, is granted to Licensee, under the provisions of Clause 1, to use Cadence's or any other person or entity participating in the development of the DFI Specification listed herein (individually "Participant," collectively "Participants") trade name, or trademarks in connection with the DFI Specification or any products based thereon. Nothing in Clause 1 shall be construed as authority for Licensee to make any representations on behalf of Cadence or the other Participants in respect of the DFI Specification.

4.NOTWITHSTANDING ANYTHING ELSE WILL CADENCE'S TOTAL AGGREGATE LIABILITY FOR ANY CLAIM, SUIT, PROCEEDING OR OTHERWISE, RELATING IN ANYWAY TO THE DFI SPECIFICATION EXCEED $1.00USD.

5.NOTWITHSTANDING ANYTHING ELSE WILL ANY PARTICIPANT'S TOTAL AGGREGATE LIABILITY FOR

ANY CLAIM, SUIT, PROCEEDING OR OTHERWISE, RELATING IN ANYWAY TO THE DFI SPECIFICATION EXCEED $1.00USD.

6.Licensee agrees that Cadence and the Participants may use, copy, modify, reproduce and distribute any written comments or suggestions ("Communications") provided regarding the DFI Specification by Licensee and that Licensee will not claim any proprietary rights in the DFI Specification, or implementations thereof by any Participant or third party, as a result of the use of the Communications in developing or changing the DFI Specification. Cadence and the participants will have no confidentiality obligations with respect to the Communications and Licensee will not include any confidential information of Licensee or any third party in any Communications.

Participants

ARM Cadence Intel LSI Samsung ST Synopsys

CONTENTS

LIST OF TABLES

LIST OF FIGURES

1.0 Overview

The DDR PHY Interface (DFI) is an interface protocol that defines the signals, timing parameters, and programmable parameters required to transfer control information and data across the DFI, and between the MC and the PHY. The programmable parameters are options defined by the MC, PHY, or system and programmed into the MC and/or the PHY. DFI applies to: DDR4, DDR3, DDR2, DDR1, LPDDR3, LPDDR2 and LPDDR1 DRAMs.

The DFI protocol does not encompass all of the features of the MC or the PHY, nor does the protocol put any restrictions on how the MC or the PHY interface to other aspects of the system.

This specification is organized by the interface groups listed in Table 1.

TABLE 1. *Interface Groups*

Interface Group	Description
Control	Required to drive the address, command, and control signals to the DRAM devices.
Write Data	Used to send write and receive valid read data across the DFI.
Read Data	
Update	Provides an ability for the MC or the PHY to initiate idling the DFI bus.
Status	Used for system initialization, feature support, and to control the presence of valid clocks to the DRAM interface.
Training	Used to execute gate training, read data eye training, write leveling and CA training operations.
Low Power Control	Allows the PHY to enter power-saving modes.
Error	Used to communicate error information from the PHY to the MC.

Within each interface group are signals and parameters. Some signals are applicable only to certain DRAM types. All of the DFI signals must use the corresponding parameters.

The DFI signals associated with each interface group, and the device originating the signal, are shown in Figure 1, “Block Diagram of Interface Signals: Control, Write, Read, Update and Status,” on page 16, and Figure 2, “Block Diagram of Interface Signals: Training, Low Power Control and Error,” on page 17. The signal requirements and parameters associated with each signal are listed in Table 2, “DFI Signal Requirements,” on page 18. Other signals may exist between the MC and the PHY for a particular implementation.

Changes in the DFI protocol between versions may result in incompatibilities between MCs and PHYs which were designed to adhere to different versions of the DFI specification. If using devices designed for different versions of the DFI specification, review the changes associated with the corresponding versions and ensure changes will not interfere with interoperability in a specific configuration.

All figures are provided for illustrative purposes only. Timing diagrams may illustrate condensed or otherwise unrealistic signal timing.

A glossary of terminology used in this specification can be found in Table 29, “Glossary of Terms,” on page 138.

2.0 Architecture

The DFI specification requires a DFI clock and DFI-defined signals that must be driven directly by registers referenced to a rising edge of the DFI clock. There are no rules dictating the source of the DFI clock, nor are there restrictions on how the DFI-defined signals are received. For DFI interoperability between the MC and the PHY, ensure compatibility in:

- Signal widths
- Interconnect timing
- Timing parameters
- Frequency ratio
- Function

Interconnect timing compatibility between the MC and the PHY at target frequencies is determined by the specification of the output timing for signals driven and the setup and hold requirements to receive these signals on the DFI per device, as defined by the device.

The DFI specification does not dictate absolute latencies or a fixed range of values that must be supported by each device. Certain DFI timing parameters can be specified as fixed values, maximum values, or as constants based on other values in the system.

DFI timing parameters must be held constant while commands are being executed on the DFI bus; however, if necessary, DFI timing parameters may be changed during a frequency change or while the bus is in the idle state. For more information on timing, refer to Section 5.0, “Signal Timing,” on page 134.

The DFI specification identifies the DFI signals relevant to a specific implementation based upon support for specific DRAM device(s), optional features, and frequency ratio. For more information on which signals are relevant to a specific implementation, refer to Table 2, “DFI Signal Requirements,” on page 18.

The MC and the PHY must operate at a common frequency ratio. For matched frequency systems, the DFI write data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, the DFI write data bus width will be multiplied proportional to the frequency ratio to allow the MC to send all of the DRAM-required write data to the PHY in a single DFI clock cycle. The write data must be delivered with the DFI data words aligned in ascending order.

- In a matched frequency system, the MC and the PHY operate with a 1:1 ratio.
- In a frequency ratio system, the MC and the PHY operate with a common frequency ratio of 1:2 or 1:4; the PHY must be able to accept a command on any and all phases. The frequency ratio depends on the relationship of the reference clocks for the MC and the PHY.

  Phase-specific signals with a suffix of “_pN”, with the phase number N (e.g., **dfi_wrdata_pN**), replace the matched frequency signals for the control, write data, read data, and status interface signals. Phase-specific signals allow the MC to drive multiple commands in a single clock cycle.

  Data word-specific signals with a suffix of “_wN”, with the DFI data word number N (e.g., **dfi_rddata_wN**), replace the matched frequency signals for the read interface to distinguish how DRAM words are transferred across the DFI bus.

  Variable pulse width-specific signals with a suffix of “aN”, with the PHY clock cycle N (e.g., **dfi_alert_n_aN)**, replace the matched frequency signals for the status interface to maintain the pulse width during transmission of error signals from the memory system to the PHY.

For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional.

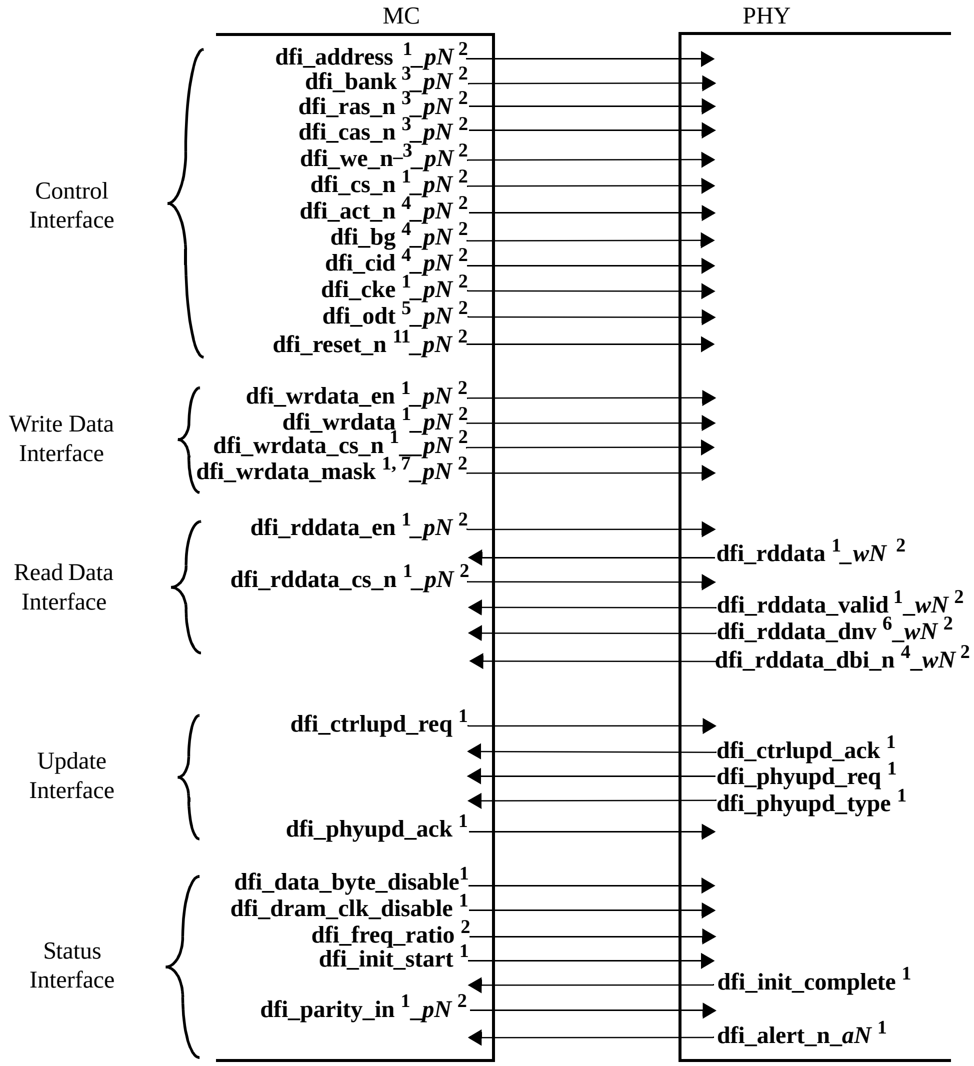
For more information on frequency ratios, refer to Section 4.8, “Frequency Ratios Across the DFI,” on page 93.

Optional protocols handle data bus inversion (DBI), cyclic redundancy check (CRC), system frequency change, command/address (CA) parity, low power, and the error interface. For more information on optional protocols, refer to Section 4.3, “Data Bus Inversion,” on page 66, Section 4.4.3, “Cyclic Redundancy Check,” on page 75, Section 4.9, “Frequency Change,” on page 110, Section 4.10, “CA Parity Signaling and CA Parity, CRC Errors,” on page 112, Section 4.11.7, “PHY-Requested Training Sequence,” on page 127, and Section 4.13, “Error Signaling,” on page 132.

The DRAM type and system configuration determine the types of training available to a system; a system may or may not utilize each type of training. If training is supported, the system may utilize DFI training or support a different training method.

The DFI signals associated with control/write data/read data/update/status interface groups, and the device originating the signals, are shown in Figure 1, “Block Diagram of Interface Signals: Control, Write, Read, Update and Status,” on page 16. The DFI signals associated with the training/low power/error interface groups, and the device originating the signals, are shown in Figure 2, “Block Diagram of Interface Signals: Training, Low Power Control and Error,” on page 17. The signals are listed functionally within each interface group.

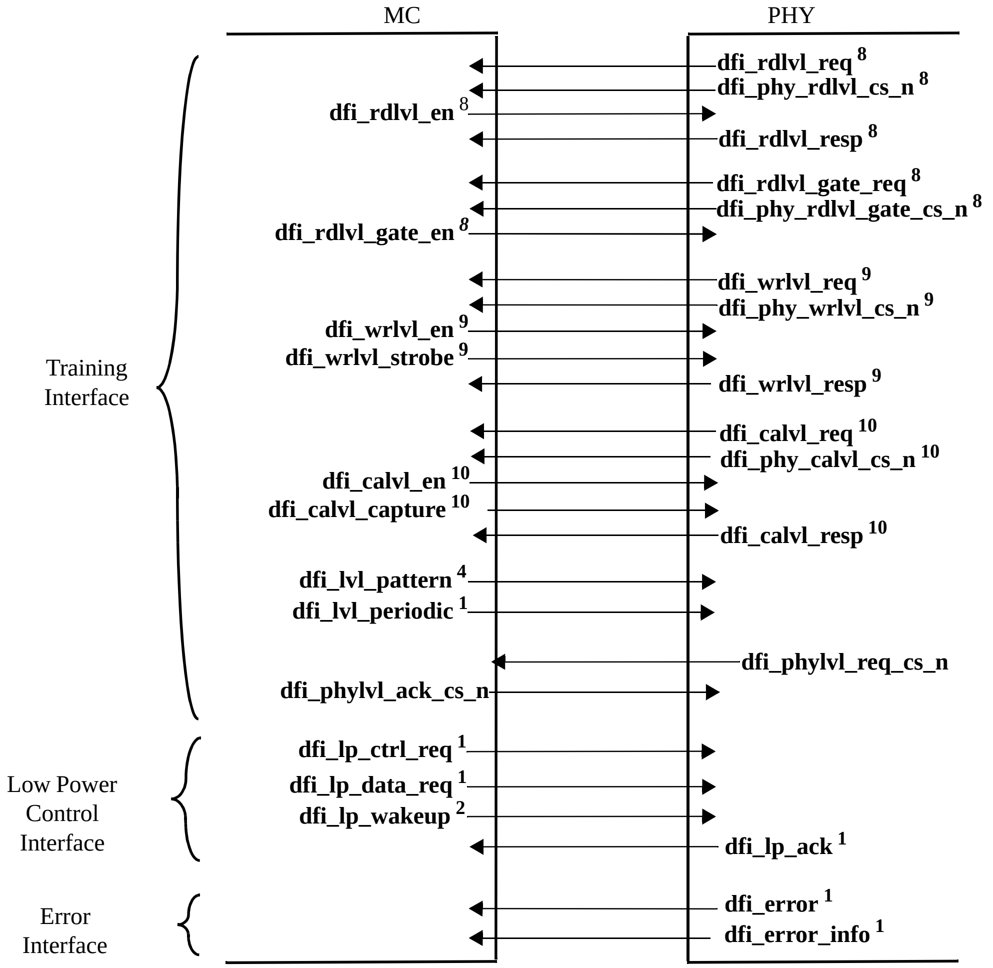
FIGURE 1. *Block Diagram of Interface Signals: Control, Write, Read, Update and Status*



1. Used by all DRAMs.
2. Optional suffix for frequency ratio systems.
3. Used with DDR4, DDR3, DDR2, DDR1 and LPDDR1 DRAMs.
4. Used with DDR4 DRAM only.
5. Used with DDR4, DDR3, DDR2 and LPDDR3 DRAMs.
6. Used with LPDDR2 DRAM only.
7. Dual-function signal. In DDR4 systems with write DBI enabled, the signal transforms from a mask to a write DBI signal.
8. Used with DDR4, DDR3, LPDDR3 and LPDDR2 DRAMs.
9. Used with DDR4, DDR3 and LPDDR3 DRAMs.
10. Used with LPDDR3 DRAMs only.
11. Used with DDR4 and DDR3 DRAMs.

Italicized text indicates that the phase/word/cycle is optional.

FIGURE 2. *Block Diagram of Interface Signals: Training, Low Power Control and Error*



1. Used with all DRAMs.
2. Optional suffix for frequency ratio systems.
3. Used with DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs.
4. Used with DDR4 DRAM only.
5. Used with DDR4, DDR3, DDR2 and LPDDR3 DRAMs.
6. Used with LPDDR2 DRAM only.
7. Dual-function signal. In DDR4 systems with write DBI enabled, the signal transforms from a mask to a write DBI signal.
8. Used with DDR4, DDR3, LPDDR3 and LPDDR2 DRAMs.
9. Used with DDR4, DDR3 and LPDDR3 DRAMs.
10. Used with LPDDR3 DRAMs only.

Italicized text indicates that the phase/word/cycle is optional.

To determine which signals are required for a specific configuration, review Table 2, “DFI Signal Requirements”. This table identifies the signals associated with each interface group, the parameters associated with each signal, and whether the signal is applicable, required, or optional for each device.

Each signal is device-specific and has corresponding parameters which must be used. Multiple parameter types may apply to a signal. Timing parameters are indicated with the prefix **t** (e.g., $\mathbf{t_{xxxxx\_xxxxx}}$). Programmable parameters are indicated with a prefix to indicate the defining device and a suffix (e.g., $\mathbf{phy_{xxxx\_en}}$). The signals are listed functionally within each interface group.

TABLE 2. *DFI Signal Requirements*

Control Interface Group			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_address_*pN*	$\mathbf{t_{ctrl\_delay}}$	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_bank _*pN*	$\mathbf{t_{ctrl\_delay}}$	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_ras_n _*pN*	$\mathbf{t_{ctrl\_delay}}$	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_cas_n_*pN*	$\mathbf{t_{ctrl\_delay}}$	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_we_n_*pN*	$\mathbf{t_{ctrl\_delay}}$	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4, DDR3, DDR2, DDR1, and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]

TABLE 2. *DFI Signal Requirements (Continued)*

dfi_cs_n_ *pN*	t_{cmd_lat} t_{ctrl_delay}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_act_n_*pN*	t_{ctrl_delay}	Required for DDR4. [b]	Required for DDR4. [b]
dfi_bg_*pN*	t_{ctrl_delay}	Required for DDR4. [b]	Required for DDR4. [b]
dfi_cid_*pN*	t_{ctrl_delay}	Required for DDR4. [b]	Required for DDR4 3D stack devices. [b]
dfi_cke_*pN*	t_{ctrl_delay}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_odt_*pN*	phy_{crc_mode} t_{ctrl_delay}	Required for DDR4, DDR3, DDR2, and LPDDR3 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4, DDR3, DDR2, and LPDDR3 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_reset_n_*pN*	t_{ctrl_delay}	Required for DDR4 and DDR3 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR4 and DDR3 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
Write Interface Group			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_wrdata_en_*pN*	phy_{crc_mode} t_{cmd_lat} $t_{phy\_crcmax\_lat}$ $t_{phy\_crcmin\_lat}$ t_{phy_wrdata} t_{wrdata_delay} t_{phy_wrlat} dfi_{rw_length}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_wrdata_*pN*	phy_{crc_mode} t_{phy_wrdata} t_{phy_wrlat}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]

TABLE 2. *DFI Signal Requirements (Continued)*

dfi_wrdata_cs_n_*pN*	$t_{phy\_wrcsgap}$ $t_{phy\_wrcslat}$	Required for all DRAMs if any of the training features are supported, otherwise, optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_wrdata_mask_*pN*	phy_{crc_mode} t_{phy_wrdata} t_{phy_wrlat}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
Read Interface Group			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_rddata_en_*pN*	t_{phy_rdlat} t_{rddata_en} dfi_{rw_length}	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_rddata_*wN*	t_{phy_rdlat} t_{rddata_en}	Required for all DRAMs. Suffix (_wN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]
dfi_rddata_cs_n_*pN*	$t_{phy\_rdcsgap}$ $t_{phy\_rdcslat}$	Required for all DRAMs if read training is supported, otherwise, optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_rddata_valid_*wN*	t_{phy_rdlat} t_{rddata_en}	Required for all DRAMs. Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]	Required for all DRAMs. Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]
dfi_rddata_dnv_*wN*	t_{phy_rdlat} t_{rddata_en}	Required for LPDDR2 DRAM. [b] Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]	Required for LPDDR2 DRAM. [b] Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]
dfi_rddata_dbi_n_*wN*	phy_{dbi_mode} t_{phy_rdlat} t_{rddata_en}	Applicable for DDR4 only. Required when MC DBI support is enabled and $\mathbf{phy_{dbi\_mode}=0}$. Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]	Applicable for DDR4 only. Required when MC DBI support is enabled and $\mathbf{phy_{dbi\_mode}=0}$. Suffix (_wN) required for frequency ratio systems to replicate information across the word. [a]
Update Interface Group			

TABLE 2. *DFI Signal Requirements (Continued)*

Signal	Associated Parameters	MC	PHY
dfi_ctrlupd_req	$t_{ctrlupd\_interval}$ $t_{ctrlupd\_max}$ $t_{ctrlupd\_min}$ t_{phyupd_type0} t_{phyupd_type1} t_{phyupd_type2} t_{phyupd_type3} t_{phyupd_resp}	Required for all DRAMs.	Optional.
dfi_ctrlupd_ack	$t_{ctrlupd\_min}$ $t_{ctrlupd\_max}$	Required for all DRAMs.	Optional.
dfi_phyupd_req	t_{phyupd_type0} t_{phyupd_type1} t_{phyupd_type2} t_{phyupd_type3} t_{phyupd_resp}	Required for all DRAMs.	Optional.
dfi_phyupd_type	t_{phyupd_type0} t_{phyupd_type1} t_{phyupd_type2} t_{phyupd_type3}	Required for all DRAMs.	Optional.
dfi_phyupd_ack	t_{phyupd_type0} t_{phyupd_type1} t_{phyupd_type2} t_{phyupd_type3} t_{phyupd_resp}	Required for all DRAMs.	Optional.
Status Interface Group			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_data_byte_disable		Optional.	Optional.
dfi_dram_clk_disable	$t_{dram\_clk\_disable}$ $t_{dram\_clk\_enable}$	Required for all DRAMs.	Required for all DRAMs.
dfi_freq_ratio		Required if the system supports multiple frequency ratios. [b] Not applicable if the system supports a single ratio.	Required if the system supports multiple frequency ratios. Not applicable if the system supports a single ratio.

TABLE 2. *DFI Signal Requirements (Continued)*

dfi_init_start	$\mathbf{t_{init\_start}}$ $\mathbf{t_{init\_complete}}$	Applicable if device supports data byte disabling, multiple frequency ratios, or the frequency change protocol. Required for systems supporting frequency change.	Applicable if device supports data byte disabling, multiple frequency ratios, or the frequency change protocol. Required for systems supporting frequency change.
dfi_init_complete	$\mathbf{t_{init\_start}}$ $\mathbf{t_{init\_complete}}$	Required for all DRAMs.	Required for all DRAMs.
dfi_parity_in_*pN*	$\mathbf{t_{parin\_lat}}$	Required for the following systems: • DDR3 RDIMM systems • DDR4 systems that support CA parity In all other cases, this signal is not required, but can optionally be included. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Optional. Only relevant for the following systems when the PHY requires the MC to generate the parity information: • DDR3 RDIMM systems • DDR4 systems that support CA parity. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_alert_n_*aN*	$\mathbf{phy_{crc\_mode}}$ $\mathbf{t_{parin\_lat}}$ $\mathbf{t_{phy\_crcmax\_lat}}$ $\mathbf{t_{phy\_crcmin\_lat}}$	Required for the following systems: • DDR3 RDIMM systems • DDR4 systems that support CRC, CA parity, or both. In all other cases, this signal is not required, but can optionally be included. NOTE: Requirement because of CRC is unrelated to $\mathbf{phy_{crc\_mode}}$ value. NOTE: Requirement because of CA parity is unrelated to location (MC, PHY) that the parity is generated. Suffix (_aN) required for frequency ratio systems to replicate information across the word. [a]	Required for the following systems: • DDR3 RDIMM systems • DDR4 systems that support CRC, CA parity, or both. In all other cases, this signal is not required, but can optionally be included. NOTE: Requirement because of CRC is unrelated to $\mathbf{phy_{crc\_mode}}$ value. NOTE: Requirement because of CA parity is unrelated to location (MC, PHY) that the parity is generated. Suffix (_aN) required for frequency ratio systems to replicate information across the word. [a]
Training Interface Group - Read Training			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_rdlvl_req	$\mathbf{t_{rdlvl\_resp}}$	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Optional. Only applicable when read training is supported.

TABLE 2. *DFI Signal Requirements (Continued)*

dfi_phy_rdlvl_cs_n	t_{rdlvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Optional. Only applicable when read training is supported.
dfi_rdlvl_en	t_{rdlvl_en} t_{rdlvl_max} t_{rdlvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs when read training is supported.[b]
dfi_rdlvl_resp	t_{rdlvl_max}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs when read training is supported.[b]
dfi_rdlvl_gate_req	t_{rdlvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Optional. Only applicable when read training is supported.
dfi_phy_rdlvl_gate_cs_n	t_{rdlvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Optional. Only applicable when read training is supported.
dfi_rdlvl_gate_en	t_{rdlvl_en} t_{rdlvl_max} t_{rdlvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs when read training is supported. [b]
(not associated with a signal)	phy_{rdlvl_en}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs when read training is supported.[b]
(not associated with a signal)	$phy_{rdlvl\_gate\_en}$	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs when read training is supported.[b]
Training Interface Group - Write Leveling			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_wrlvl_req	t_{wrlvl_resp}	Required for DDR4, DDR3, and LPDDR3 DRAMs. [b]	Optional when write leveling is supported.
dfi_phy_wrlvl_cs_n	t_{wrlvl_resp}	Required for DDR4, DDR3, and LPDDR3 DRAMs. [b]	Optional when write leveling is supported.
dfi_wrlvl_en	t_{wrlvl_en} t_{wrlvl_max} t_{wrlvl_resp}	Required for DDR4, DDR3, and LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when write leveling is supported. [b]
dfi_wrlvl_strobe	t_{wrlvl_en} t_{wrlvl_ww}	Required for DDR4, aDDR3, and LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when write leveling is supported. [b]
dfi_wrlvl_resp	t_{wrlvl_max}	Required for DDR4, DDR3, and LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when write leveling is supported.[b]

TABLE 2. *DFI Signal Requirements (Continued)*

(not associated with a signal)	**phy_{wwlvl_en}**	Required for DDR4, DDR3, and LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when write leveling is supported.[b]
Training Interface Group - CA Training			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_calvl_req	**t_{calvl_resp}**	Required for LPDDR3 DRAMs. [b]	Optional when CA training is supported.
dfi_phy_calvl_cs_n	**t_{calvl_resp}**	Required for LPDDR3 DRAMs. [b]	Optional when CA training is supported.
dfi_calvl_en	**t_{calvl_en}** **t_{calvl_max}** **t_{calvl_resp}**	Required for LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when CA training is supported. [b]
dfi_calvl_capture	**t_{calvl_en}** **$t_{calvl\_capture}$** **t_{calvl_cc}**	Required for LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when CA training is supported. [b]
dfi_calvl_resp	**t_{calvl_max}**	Required for LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when CA training is supported. [b]
(not associated with a signal)	**phy_{calvl_en}**	Required for LPDDR3 DRAMs. [b]	Required for DDR4, DDR3, and LPDDR3 DRAMs when CA training is supported. [b]
Training Interface Group - Leveling			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_lvl_pattern	**t_{rdlvl_en}** **t_{rdlvl_max}** **t_{rdlvl_resp}**	Required for DDR4, LPDDR3, and LPDDR2 DRAMs. [b]	Required for DDR4, LPDDR3, and LPDDR2 DRAMs. [b]
dfi_lvl_periodic	**t_{rdlvl_en}** **t_{rdlvl_max}** **t_{rdlvl_resp}** **t_{wrlvl_en}** **t_{wrlvl_max}** **t_{wrlvl_resp}**	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs.	Optional.
Training Interface Group - PHY-Requested Training			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_phylvl_req_cs_n	**t_{phylvl}** **t_{phylvl_resp}**	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs.	Optional.

TABLE 2. *DFI Signal Requirements (Continued)*

dfi_phylvl_ack_cs_n	t_{phylvl} t_{phylvl_resp}	Required for DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs.	Optional.
Low Power Control Interface Group (optional)			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_lp_ctrl_req	t_{lp_resp}	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
dfi_lp_data_req	t_{lp_resp}	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
dfi_lp_wakeup	t_{lp_wakeup}	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
dfi_lp_ack	t_{lp_resp} t_{lp_wakeup}	Supported for all DRAM types. Required when low power is supported.	Supported for all DRAM types. Required when low power is supported.
Error Interface Group (optional)			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_error	t_{error_resp}	Supported for all DRAM types. Required when error interface is supported.	Supported for all DRAM types. Required when error interface is supported.
dfi_error_info	t_{error_resp}	Optional.	Optional.

[a] For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N *(pN)*/data word N*(wN)*/clock cycle N*(aN)*, as applicable. The phase 0 suffixes are not required.

[b] Other DRAMs must hold this signal in the idle state.

3.0 Interface Signal Groups

3.1 Control Interface

The control interface handles the transmission of signals required to drive the address, command, and control signals to the DRAM devices; the interface includes signals and timing parameters. The signals are intended to be passed to the DRAM devices in a manner that maintains the timing relationship among the signals on the DFI; the $\mathbf{t_{ctrl\_delay}}$ timing parameter defines the delay introduced between the DFI interface and the DRAM interface.

Some of the control interface signals are DRAM technology-specific and are only required if the associated technology is used. Examples of DRAM technology-specific control interface signals are:

- **dfi_reset_n** is specific to DDR4 and DDR3 DRAMs
- **dfi_odt** is specific to DDR4, DDR3, DDR2, and LPDDR3 DRAMs

For LPDDR3 and LPDDR2 DRAMs, the CA bus is mapped onto to the **dfi_address** bus. The following signals must be held at constant values when present in an LPDDR3 or LPDDR2 implementation: **dfi_cid**, **dfi_bank**, **dfi_bg**, **dfi_act_n**, **dfi_ras_n**, **dfi_cas_n**, and **dfi_we_n**. The **dfi_address** bus must have a minimum of 20 bits to hold the LPDDR3 or LPDDR2 rising and falling DDR CA bus for the entire clock period. The PHY is responsible for transmitting the 20-bit **dfi_address** bus as a double data rate 10-bit output, transmitting to the LPDDR3 or LPDDR2 DRAM on the rising and falling CA phases. The LPDDR3/LPDDR2 interface mapping is detailed in Table 3, “Bit Definitions of the dfi_address bus for LPDDR3 and LPDDR2”.

During CA training, the **dfi_address**, **dfi_cke**, and **dfi_cs_n** signals have additional functionality. For details on the signal functionality, refer to Table 4, “Control Signals,” on page 27.

For frequency ratio systems, the buses/signals of the control interface are replicated into phase-specific signals with a suffix of “_pN” that defines the signal value for each phase N of the DFI PHY clock. Phase 0 may exclude the suffix if desired. The MC may issue commands on any phase to communicate with the PHY. For example, the MC may issue commands only on a single phase, such as phase 0, or may issue commands on any combination of phases; the PHY must be able to accept a command on any and all phases.

TABLE 3. *Bit Definitions of the **dfi_address** bus for LPDDR3 and LPDDR2*

dfi_address	⎍	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CA Bus	↑											LPDDR3/LPDDR2 1									
												9	8	7	6	5	4	3	2	1	0
	↓	LPDDR3/LPDDR2 2																			
		9	8	7	6	5	4	3	2	1	0										

For more information on the control interface, refer to Section 4.2, “Control Signals,” on page 64. The signals and parameters in the control interface are listed in Table 4 and Table 5.

For more information on the control interface, refer to Section 4.2, “Control Signals,” on page 64. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the control interface are listed in Table 4.

TABLE 4. *Control Signals*

Signal	From	Width	Default	Description
dfi_act_n or **dfi_act_n_pN** [a]	MC	1 bit	- [b]	DFI activate signal. This signal is used for encoding DRAM commands. The following signals define all or a subset of the command encoding: **dfi_act_n**, **dfi_cas_n**, **dfi_ras_n**, **dfi_we_n**.
dfi_address or **dfi_address_pN** [a]	MC	DFI Address Width	- [b], [c]	DFI address bus. These signals define the address information. The PHY must preserve the bit ordering of the **dfi_address** signals when it sends this data to the DRAM devices. For DDR4 DRAMs, the **dfi_address** bus defines the column address and a portion of the row address. DDR4 devices do not use the **dfi_address** bits [16:14] since DDR4 devices transmit the row address bits [16:14] on **dfi_ras_n, dfi_cas_n,** and **dfi_we_n**. For larger density devices, **dfi_address** bits A17 and above are utilized. Consequently, when a larger density device interfaces with a DDR4 system, there can be gaps in the address bus. For systems that support multiple DRAM classes, all or a subset of the **dfi_address** bits [16:14] can be used to address a non-DDR4 DRAM. For LPDDR3 memory systems, during a CA training routine, the **dfi_address** bus should drive a defined background pattern when the command bus is idle, and drive a defined pattern with the calibration command. Both the background and command patterns driven on the **dfi_address** bus must be able to be uniquely defined by the MC for each assertion of the **dfi_calvl_en** signal and cannot be changed while the **dfi_calvl_en** signal remains asserted. For LPDDR3 and LPDDR2 DRAMs, the **dfi_address** bus maps to the CA bus as described in Section 3.1, “Control Interface,” on page 26.
dfi_bank or **dfi_bank_pN** [a]	MC	DFI Bank Width	- [b]	DFI bank bus. These signals define the bank information. The PHY must preserve the bit ordering of the **dfi_bank** signals when it sends the DFI bank data to the DRAM devices.
dfi_bg or **dfi_bg_pN** [a]	MC	DFI Bank Group Width	- [b]	DFI bank group. This signal defines the bank group of a command. The PHY must preserve the bit ordering of the **dfi_bg** signals when it sends the DFI bank group data to the DRAM devices.

TABLE 4. *Control Signals (Continued)*

Signal	From	Width	Default	Description
dfi_cas_n or **dfi_cas_n_pN** [a]	MC	DFI Control Width	0x1 [d]	DFI column address strobe. This signal is used for encoding DRAM commands. The following signals define all or a subset of the command encoding: **dfi_act_n**, **dfi_cas_n**, **dfi_ras_n**, **dfi_we_n**.
dfi_cid or **dfi_cid_pN** [a]	MC	DFI Chip ID Width	- [b]	DFI Chip ID. This signal defines the chip ID. The PHY must preserve the bit ordering of the **dfi_cid** signals when it sends the DFI chip ID data to the DRAM devices.
dfi_cke or **dfi_cke_pN** [a]	MC	DFI Chip Select Width	0x0 [e] 0x1 [e]	DFI clock enable.This signal defines the clock enable. The MC must drive CKE signals in all phases. The PHY must be able to accept a command on any and all phases for DFI frequency ratio compliance. For LPDDR3 memory, during CA training, the **dfi_cke** signal is used in training sequence to enable the output drivers on the DRAM.
dfi_cs_n or **dfi_cs_n_pN** [a]	MC	DFI Chip Select Width	0x1	DFI chip select. This signal defines the chip select. For LPDDR3 memory, during CA training, the **dfi_cs_n** signal is used as the calibration command which is transmitted on the bit corresponding to the chip select currently being trained. For frequency ratio systems, the calibration command must be asserted on a single phase to create a single cycle DRAM pulse.
dfi_odt or **dfi_odt_pN** [a]	MC	DFI Chip Select Width	0x0	DFI on-die termination control bus. These signals define the ODT. The MC must drive ODT signals in all phases. The PHY must be able to accept a command on any and all phases for DFI frequency ratio compliance.
dfi_ras_n or **dfi_ras_n_pN** [a]	MC	DFI Control Width	0x1 [d]	DFI row address strobe. This signal is used for encoding DRAM commands. The following signals define all or a subset of the command encoding: **dfi_act_n**, **dfi_cas_n**, **dfi_ras_n**, **dfi_we_n**.
dfi_reset_n or **dfi_reset_n_pN** [a]	MC	DFI Chip Select Width	0x0 0x1[f]	DFI reset bus. These signals define the RESET. The PHY must preserve the bit ordering of the **dfi_reset_n** signals when it sends the DFI chip ID data to the DRAM devices.
dfi_we_n or **dfi_we_n_pN** [a]	MC	DFI Control Width	0x1 [d]	DFI write enable signal. This signal is used for encoding DRAM commands. The following signals define all or a subset of the command encoding: **dfi_act_n**, **dfi_cas_n**, **dfi_ras_n**, **dfi_we_n**.

a. For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N(aN), as applicable. The phase 0 suffixes are not required.

b. This signal is not meaningful during initialization; no default value is required.

c. For LPDDR3 and LPDDR2 memory systems, the **dfi_address** bus must be driven with an NOP until **dfi_init_complete** is asserted.

d. This signal has multiple purposes with DDR4 devices. For all commands that have **dfi_act_n** de-asserted, this signal communicates command encoding similar to the functionality defined for other DRAM devices. When **dfi_act_n** is asserted, the signal transmits upper row address bits with the following address mapping: **dfi_cas_n** → A15, **dfi_ras_n** → A16, **dfi_we_n** → A14.

e. Most DRAMs define CKE as low at reset; some devices, such as Mobile DDR, define CKE as high at reset. The default value should adhere to the DRAM definition.

f. In general, the **dfi_reset_n** signal is defined as low at reset; however, in some cases it may be necessary to hold **dfi_reset_n** high during initialization.

The timing parameters associated with the control interface are listed in Table 5.

TABLE 5. *Control Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{cmd\_lat}}$	MC	0	- [a]	DFI PHY clock cycles [b]	Specifies the number of DFI clocks after the **dfi_cs_n** signal is asserted until the associated CA signals are driven.
$\mathbf{t_{ctrl\_delay}}$	PHY	0	[a]	DFI clock cycles	Specifies the number of DFI clock cycles from the time that any control signal changes and when the change reaches the DRAM interface. If the DFI clock and the DRAM clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.

[a] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

[b] For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

3.2 Write Data Interface

The write data interface handles the transmission of write data across the DFI; the interface includes signals, timing parameters, and programmable parameters.

Table 6, “Write Data Signals,” on page 31 describes the signals **dfi_wrdata** (write data bus), **dfi_wrdata_cs_n** (write data chip select), **dfi_wrdata_en** (write data and data mask enable), and **dfi_wrdata_mask** (write data byte mask).

The **dfi_wrdata** bus transfers write data from the MC to the PHY. The **dfi_wrdata_en** signal indicates to the PHY that valid **dfi_wrdata** and **dfi_wrdata_mask** will be transmitted in $\mathbf{t_{phy\_wrdata}}$ cycles.

3.2.1 Write Data Mask/Write DBI

The **dfi_wrdata_mask** signal has two mutually exclusive functions. If the DBI feature (described in Section 4.3, “Data Bus Inversion,” on page 66) is not enabled, **dfi_wrdata_mask** defines the bytes within the **dfi_wrdata** signals that will be written to DRAM. Alternately, if the DBI feature is enabled and $\mathbf{phy_{dbi\_mode}}$=0, the **dfi_wrdata_mask** signal is no longer a mask, instead it becomes a write DBI signal and indicates whether the write data is inverted

3.2.2 Write Data Chip Select

If data chip select is enabled, the **dfi_wrdata_cs_n** signal indicates which chip select is accessed for the associated write data to independently compensate for timing differences on the data interface accessing different chip selects.

3.2.3 Write Data CRC

If the MC generates the CRC, the MC sends the appropriate CRC data word across the DFI bus using the existing **dfi_wrdata** signals, and adjusts control signal timing to handle the additional data word.

Table 7, “Write Data Timing Parameters,” on page 32 describes the write timing parameters $\mathbf{t_{phy\_wrcsgap}}$, $\mathbf{t_{phy\_wrcslat}}$, $\mathbf{t_{phy\_wrdata}}$, $\mathbf{t_{phy\_wrlat}}$, $\mathbf{t_{wrdata\_delay}}$, $\mathbf{t_{phy\_crcmax\_lat}}$, and $\mathbf{t_{phy\_crcmin\_lat}}$.

The $\mathbf{t_{phy\_wrcsgap}}$ timing parameter specifies the minimum number of additional DFI PHY clocks required between commands when changing the target chip select driven on the **dfi_wrdata_cs_n** signal, and defines a minimum additional delay between commands when changing the target chip select as required by the PHY. The $\mathbf{t_{phy\_wrcslat}}$ parameter specifies the number of DFI PHY clocks between when a write command is sent on the DFI control interface and when the associated **dfi_wrdata_cs_n** signal is asserted, and has a delay defined relative to the command to maximize timing flexibility.

The $\mathbf{t_{phy\_wrdata}}$ parameter specifies the number of DFI PHY clock cycles between when the **dfi_wrdata_en** signal is asserted to when the associated write data is driven on the **dfi_wrdata** bus. The $\mathbf{t_{phy\_wrlat}}$ parameter specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the **dfi_wrdata_en** signal is asserted. The $\mathbf{t_{wrdata\_delay}}$ parameter specifies the number of DFI clocks from the time that the **dfi_wrdata_en** signal is asserted and when the corresponding write data transfer completes on the DRAM bus.The PHY-defined $\mathbf{t_{phy\_crcmax\_lat}}$ and $\mathbf{t_{phy\_crcmin\_lat}}$ timing parameters create a time window around an error occurrence on the DFI bus. The sequence of events occurs as follows:

1. The PHY sends a write command, followed by associated data and CRC values to the DRAM. A problem could arise during transmission of the values.
2. When the DRAM logic compares the data and CRC values to each other, if it detects mismatch(es), it asserts the ALERT_N signal on the memory bus.
3. The PHY propagates the ALERT_N value to the MC through the **dfi_alert_n** signal.

The MC can use these timing parameters to pinpoint the command or set of commands associated with the error condition and reissue commands after the CRC error is addressed. The CRC error timing parameters define the relationship between **dfi_wrdata_en** and **dfi_alert_n_aN** signals.

Table 8, “Write Data Programmable Parameters,” on page 33 describes the programmable parameters applicable when CRC and DBI features are enabled. When the optional CRC feature is enabled in DFI, the parameter determines whether the MC or the PHY performs CRC generation and validation. When the optional DBI feature is enabled in DFI, the PHY-defined $\mathbf{phy_{dbi\_mode}}$ parameter determines whether DBI generation and data inversion is performed by the MC or the PHY.

3.2.4 Frequency Ratio

For frequency ratio systems, the signals are replicated into phase-specific signals with a suffix of “_pN” that defines the signal value for each phase N of the PHY clock. Phase 0 may exclude the suffix if desired.

3.2.5 *Write Data Signals and Parameters*

The signals and parameters in the write data interface are listed in Table 6, “Write Data Signals”, Table 7, “Write Data Timing Parameters,” on page 32, and Table 8, “Write Data Programmable Parameters,” on page 33.

For more information on the write data interface, refer to Section 4.4, “Write Transactions,” on page 67. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the write data interface are listed in Table 6.

TABLE 6. *Write Data Signals*

Signal	From	Width	Default	Description
dfi_wrdata or **dfi_wrdata_pN** [a]	MC	DFI Data Width	- [b]	Write data. These signals transfer write data from the MC to the PHY $\mathbf{t}_{\mathbf{phy\_wrdata}}$ cycles after the **dfi_wrdata_en** signal is asserted and continues transferring data for the number of cycles that the **dfi_wrdata_en** signal is asserted.
dfi_wrdata_cs_n or **dfi_wrdata_cs_n_pN** [a]	MC	DFI Chip Select Width x DFI Data Enable Width [c]	- [b]	DFI Write Data Chip Select. This signal serves two functions as follows: • During write leveling, **dfi_wrdata_cs_n** indicates the chip select that is currently active. • During non-leveling operation, **dfi_wrdata_cs_n** is an optional signal for the MC that indicates the chip select that is accessed or targeted for associated write data.
dfi_wrdata_en or **dfi_wrdata_en_pN** [a]	MC	DFI Data Enable Width [d]	0x0	Write data and data mask enable. This signal indicates to the PHY that valid **dfi_wrdata** will be transmitted in $\mathbf{t}_{\mathbf{phy\_wrdata}}$ cycles. Both $\mathbf{t}_{\mathbf{phy\_wrlat}}$ and $\mathbf{t}_{\mathbf{phy\_wrdata}}$ may be defined as zero. Ideally, there is a one-to-one correspondence between **dfi_wrdata_en** bits and PHY data slices. The **dfi_wrdata_en** [0] signal corresponds to the lowest segment of **dfi_wrdata** signals.
dfi_wrdata_mask or **dfi_wrdata_mask_pN** [a]	MC	DFI Data Width/8	[b]	Write data byte mask. This bus is used for transferring either the write data mask or the write DBI information, depending on system/DRAM settings. It uses the same timing as the **dfi_wrdata** signal. • **dfi_wrdata_mask** [0] = Masking or DBI for the **dfi_wrdata** [7:0] signals • **dfi_wrdata_mask** [1] = Masking or DBI for the **dfi_wrdata** [15:8] signals, etc. If the **dfi_wrdata** bus is not a multiple of 8, the upperrmost bit of the **dfi_wrdata_mask** signal corresponds to the most significant partial byte of data.

[a] For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N (aN), as applicable. The phase 0 suffixes are not required.

[b] This signal is not meaningful during initialization; no default value is required.

[c] The width is defined to be replicated and multiply driven to each of the PHY data slices for interconnect simplicity.

[d] Since all bits of the **dfi_wrdata_en** signal are identical, the width of the signal on the MC side and the PHY side may be different; the PHY is not required to use all of the bits.

Table 7 lists the timing parameters that are associated with the write data interface.

TABLE 7. *Write Data Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{phy\_crcmax\_lat}}$	System	1	-[a]	DFI PHY clock cycles[b]	This parameter specifies the maximum number of DFI PHY cycle clocks between **dfi_wrdata_en** (the DFI cycle that is associated with CRC code being transmitted) and the associated CRC error that is transmitted on **dfi_alert_n_aN**. The PHY samples the CRC code on the DFI interface. The MC samples the associated CRC error on **dfi_alert_n_aN**. Use this parameter with $\mathbf{t_{phy\_crcmin\_lat}}$ to determine a window of time that the erroneous data transmits across the DFI bus.
$\mathbf{t_{phy\_crcmin\_lat}}$	System	0	-[a]	DFI PHY clock cycles[b]	This parameter specifies the minimum number of DFI PHY cycle clocks between **dfi_wrdata_en** (the DFI cycle that is associated with CRC code being transmitted) and the associated CRC error that is transmitted on **dfi_alert_n_aN**. The PHY samples the CRC code on the DFI interface. The MC samples the associated CRC error on **dfi_alert_n_aN**. Use this parameter with $\mathbf{t_{phy\_crcmax\_lat}}$ to determine a window of time that the erroneous data transmits across the DFI bus.
$\mathbf{t_{phy\_wrcsgap}}$	PHY	0	-[a]	DFI PHY clock cycles[b]	This parameter specifies the minimum number of additional DFI PHY clocks (or DFI PHY clock) cycles that are required between commands when changing the target chip select that is driven on the **dfi_wrdata_cs_n** signal. This parameter must be supported in the MC transaction-to-transaction timing. The minimum assertion duration of **dfi_wrdata_cs_n** is determined by $\mathbf{t_{phy\_wrcsgap} + dfi_{rw\_length}}$[c].
$\mathbf{t_{phy\_wrcslat}}$	PHY	0	-[a]	DFI PHY clock cycles[b]	This parameter specifies the number of DFI PHY clock cycles from the time that a write command is sent on the DFI control interface and when the associated **dfi_wrdata_cs_n** signal is asserted.
$\mathbf{t_{phy\_wrdata}}$	PHY	0[d]	-[d]	DFI PHY clock cycles[b]	This parameter specifies the number of DFI PHY clock cycles from the time that the **dfi_wrdata_en** signal is asserted and when the associated write data is driven on the **dfi_wrdata** signal. The parameter adjusts the relative time between enable and data transfer with no effect on performance. DFI 1.0 and DFI 2.0 MCs support a $\mathbf{t_{phy\_wrdata}}$ value of only 1. The MC should support a range of $\mathbf{t_{phy\_wrdata}}$ values. A PHY is designed to operate at a single $\mathbf{t_{phy\_wrdata}}$ value.

TABLE 7. *Write Data Timing Parameters (Continued)*

Parameter	Defined By	Min	Max	Unit	Description
t_{phy_wrlat}	PHY	0 [d]	- [d]	DFI PHY clock cycles [b]	This parameter specifies the number of DFI PHY clock cycles from the time that a write command is sent on the DFI control interface and when the **dfi_wrdata_en** signal is asserted. NOTE: This parameter may be specified as a fixed value, or as a constant that is based on other fixed values in the system.
t_{wrdata_delay}	System	0	-	DFI clock cycles	This parameter specifies the number of DFI clocks from the time that the **dfi_wrdata_en** signal is asserted and when the corresponding write data transfer completes on the DRAM bus.

[a] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

[b] This timing parameter is defined in terms of DFI PHY clock cycles for frequency ratio systems. For matched frequency systems, a DFI PHY clock is identical to the DFI clock.

[c] The $\mathbf{dfi}_{\mathbf{rw\_length}}$ value is the total number of DFI clocks required to transfer one DFI read or write command worth of data. For a matched frequency system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ would typically equal (burst length/2). For a frequency ratio system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ is defined in terms of DFI PHY clocks and would typically equal (burst length/2). Additional DFI clock (or DFI PHY clock) cycles must be added for the CRC data transfer.

[d] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

The programmable parameters associated with the write data interface are listed in Table 8.

TABLE 8. *Write Data Programmable Parameters*

Parameter	Defined By	Description
$\mathbf{phy}_{\mathbf{crc\_mode}}$	PHY	Sends CRC data as part of the data burst. • ‘b0 = CRC code generation and validation performed in the MC. • ‘b1 = CRC code generation and validation performed in the PHY.
$\mathbf{phy}_{\mathbf{dbi\_mode}}$	PHY	Determines which device generates DBI and inverts the data. • ‘b0 = DBI generation and data inversion performed in the MC. • ‘b1 = DBI generation and data inversion performed in the PHY.

3.3 Read Data Interface

The read data transaction handles the capture and return of data across the DFI; the interface includes signals, timing parameters, and a programmable parameter.

The width is defined to be replicated and multiply driven to each of the PHY data slices for interconnect simplicity.

Table 9, “Read Data Signals,” on page 35 describes the signals **dfi_rddata** (read data bus), **dfi_rddata_cs_n** (data path chip select), **dfi_rddata_en** (read data enable), **dfi_rddata_valid** (read data valid indicator), the DRAM-specific

LPDDR2 signal **dfi_rddata_dnv** (dfi data not valid), and the DDR4 signal **dfi_rddata_dbi_n**. When the **dfi_rddata_dbi_n** signal is used, it is sent with the **dfi_rddata** signal.

3.3.1 Read DBI

If the DBI feature is enabled and $\mathbf{phy}_{\mathbf{dbi\_mode}}$=0, the MC captures read DBI data transmitted from the PHY and selectively inverts the read data based on DBI as required.

3.3.2 Read Data Chip Select

When accessing different chip-selects, it may be desirable to independently compensate for timing differences on the data interface. In this case, the PHY may require knowledge of the target chip select for each read transaction. The optional **dfi_rddata_cs_n** signal provides the target data path chip select value to each of the PHY data slices.

The data path chip select signal **dfi_rddata_cs_n** is defined similar to the **dfi_cs_n** signal, and has a separate timing parameter, $\mathbf{t}_{\mathbf{phy\_rdcslat}}$. The delay is defined relative to the command to maximize timing flexibility. Additionally, the $\mathbf{t}_{\mathbf{phy\_rdcsgap}}$, timing parameter defines a minimum additional delay between commands when changing the target chip select as required by the PHY.

3.3.3 Read Data Valid

The **dfi_rddata_valid** signal allows each PHY data slice to return **dfi_rddata** independently. The **dfi_rddata_valid** signal width is equivalent to the number of PHY data slices.

When valid data is being transferred, the **dfi_rddata_valid** signal must be asserted. This signal is a response from the PHY to **dfi_rddata_en** assertion by the MC. Additionally, there is a one-to-one correspondence between **dfi_rddata_en** assertion clocks and **dfi_rddata_valid** assertion clocks.

DFI dictates a timing relationship **from dfi_rddata_en** to dfi_rddata_valid, specified by $\mathbf{t}_{\mathbf{phy\_rdlat}}$; DFI does not dictate an exact number of cycles. The **dfi_rddata_valid** signal can assert earlier than the maximum delay, and does not need to be held for consecutive cycles if the $\mathbf{t}_{\mathbf{phy\_rdlat}}$ value is met for every transfer.

Table 10, “Read Data Timing Parameters,” on page 36 describes the timing parameters $\mathbf{t}_{\mathbf{phy\_rdcsgap,}}$ $\mathbf{t}_{\mathbf{phy\_rdcslat,}}$ $\mathbf{t}_{\mathbf{rddata\_en}}$, and $\mathbf{t}_{\mathbf{phy\_rdlat}}$.

The $\mathbf{t}_{\mathbf{phy\_rdlat}}$ parameter defines the maximum number of cycles allowed from the assertion of the **dfi_rddata_en** signal to the assertion of the **dfi_rddata_valid** signal for all data slices. This parameter is specified by the system, but the exact value of this parameter is not determined by the DFI specification.

The $\mathbf{t}_{\mathbf{rddata\_en}}$ and $\mathbf{t}_{\mathbf{phy\_rdlat}}$ timing parameters must be held constant while commands are being executed on the DFI bus; however, if necessary, the timing parameters may be changed when the bus is in the idle state. These parameters work together to define a maximum number of cycles from the assertion of a read command on the DFI control interface to the assertion of the **dfi_rddata_valid** signal, indicating the first cycle of the read data. Read data may be returned earlier by asserting the **dfi_rddata_valid** signal before $\mathbf{t}_{\mathbf{phy\_rdlat}}$ cycles have expired. When the signal **dfi_rddata_valid** is asserted, the entire DFI read data word from the associated data slice must be valid. For the LPDDR2 DFI, the signal **dfi_rddata_dnv** must also be sent with the read data signal **dfi_rddata** when the **dfi_rddata_valid** signal is asserted.

3.3.4 Frequency Ratio

For frequency ratio systems, the read data enable signal is replicated into phase-specific signals with a suffix of “_pN” that defines the signal value for each phase N of the DFI PHY clock relative to the DFI clock. The read data, read data valid and read data not valid signals are replaced with DFI data word-specific signals with a suffix of “_wN” to specify the DFI data word N. For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional.

Table 11, “Read Data Programmable Parameter,” on page 37 describes the programmable parameter $\mathbf{phy_{dbi\_mode}}$ which applies to both write and read signals.

For more information on the read data interface, refer to Section 4.5, “Read Transactions,” on page 81. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the read data interface are listed in Table 9.

TABLE 9. *Read Data Signals*

Signal	From	Width	Default	Description
dfi_rddata or **dfi_rddata_wN** [a]	PHY	DFI Data Width	- [b]	Read data bus. This bus transfers read data from the PHY to the MC. Read data is expected to be received at the MC within $\mathbf{t_{phy\_rdlat}}$ cycles after the **dfi_rddata_en** signal is asserted.
dfi_rddata_cs_n or **dfi_rddata_cs_n_pN** [a]	MC	DFI Chip Select Width x DFI Data Enable Width		DFI Read Data Chip Select. This signal has two functions. During read training, **dfi_rddata_cs_n** indicates which chip select is currently active. During non-leveling operation, **dfi_rddata_cs_n** is an optional signal for the MC to indicate which chip select is accessed or targeted for associated read data.
dfi_rddata_dbi_n or **dfi_rddata_dbi_n_wN** [a]	PHY	DFI DBI Width		Read Data DBI. This signal is sent with **dfi_rddata** bus indicating DBI functionality. This signal is used only when $\mathbf{phy_{dbi\_mode}=0}$.
dfi_rddata_en or **dfi_rddata_en_pN** [a]	MC	DFI Data Enable Width [c]	0x0	Read data enable. This signal indicates to the PHY that a read operation to memory is underway and identifies the number of data words to be read. The **dfi_rddata_en** signal must be asserted $\mathbf{t_{rddata\_en}}$ cycles after the assertion of a read command on the DFI control interface and remains valid for the duration of contiguous read data expected on the **dfi_rddata** bus. Ideally, there is a single **dfi_rddata_en** bit for each PHY data slice. The **dfi_rddata_en** [0] signal corresponds to the lowest segment of **dfi_rddata** signals.

TABLE 9. *Read Data Signals (Continued)*

Signal	From	Width	Default	Description
dfi_rddata_valid or **dfi_rddata_valid_wN** [a]	PHY	DFI Read Data Valid Width	0x0	Read data valid indicator. Each bit of the **dfi_rddata_valid** signal is asserted with the corresponding **dfi_rddata** for the number of cycles that data is being sent. The timing is the same as for the **dfi_rddata** bus. The width of the **dfi_rddata_valid** signal is equivalent to the number of PHY data slices. Ideally, there is a one-to-one correspondence between a **dfi_rddata_valid** signal bit and each PHY data slice.The **dfi__rddata_valid**[0] signal corresponds to the lowest segment of the **dfi_rddata** signals.
dfi_rddata_dnv or **dfi_rddata_dnv_wN** [a]	PHY	DFI Data Width/8	0x0	DFI data not valid. The timing is the same as for the **dfi_rddata_valid** signal. The **dfi_rddata_dnv** [0] signal correlates to the **dfi_rddata** [7:0] signals, the **dfi_rddata_dnv** [1] signal correlates to the **dfi_rddata** [15:8] signals, etc. If the **dfi_rddata** bus is not a multiple of 8, the uppermost bit of the **dfi_rddata_dnv** signal corresponds to the most significant partial byte of data.

a. For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N(aN), as applicable. The phase 0 suffixes are not required.

b. This signal is not meaningful during initialization; no default value is required.

c. Since all bits of the **dfi_rddata_en** signal are identical, the width of the signal on the MC side and the PHY side may be different; the PHY is not required to use all of the bits.

The timing parameters associated with the read data interface are listed in Table 10.

TABLE 10. *Read Data Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{phy\_rdcsgap}}$	PHY	0	-[a]	DFI PHY clock cycles [b]	Specifies the minimum number of additional DFI PHY clocks required between commands when changing the target chip select driven on the **dfi_rddata_cs_n** signal. This parameter needs to be supported in the MC transaction-to-transaction timing. The minimum assertion duration of **dfi_rddata_cs_n** is determined by $\mathbf{t_{phy\_rdcsgap}}$ **+** $\mathbf{dfi_{rw\_length}}$[c].
$\mathbf{t_{phy\_rdcslat}}$	PHY	0	-[a]	DFI PHY clock cycles [b]	Specifies the number of DFI PHY clocks between when a read command is sent on the DFI control interface and when the associated **dfi_rddata_cs_n** signal is asserted.
$\mathbf{t_{phy\_rdlat}}$	PHY	0	-[a]	DFI PHY clock cycles [b]	Specifies the maximum number of DFI PHY clock cycles allowed from the assertion of the **dfi_rddata_en** signal to the assertion of each of the corresponding bits of the **dfi_rddata_valid** signal.
$\mathbf{t_{rddata\_en}}$	System	0	- [a]	DFI PHY clock cycles [b]	Specifies the number of DFI PHY clock cycles from the assertion of a read command on the DFI to the assertion of the **dfi_rddata_en** signal. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.

[a] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

[b] For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

[c] The $\mathbf{dfi}_{\mathbf{rw\_length}}$ value is the total number of DFI clocks required to transfer one DFI read or write command worth of data. For a matched frequency system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ would typically equal (burst length/2). For a frequency ratio system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ is defined in terms of DFI PHY clocks and would typically equal (burst length/2). Additional DFI clock (or DFI PHY clock) cycles must be added for the CRC data transfer.

The programmable parameter associated with the read data interface is listed in Table 11.

TABLE 11. *Read Data Programmable Parameter*

Parameter	Defined By	Min	Max	Description
$\mathbf{phy}_{\mathbf{dbi\_mode}}$	PHY	0	1	Determines which device generates DBI and inverts the data. • ‘b0 = DBI generation and data inversion performed in the MC. • ‘b1 = DBI generation and data inversion performed in the PHY.

3.4 Update Interface

The update interface facilitates various commands that might require interruption of their transmission on the DFI. These commands include timing adjustments, calibration, training, etc. This interface defines signals and timing parameters.To ensure that updates do not interfere with signals on the DRAM interface, the DFI supports update modes when the DFI bus is placed in an idle state.

When the DFI bus is in an idle state, the control interface is not sending any commands and all read and write data has transferred on the DFI bus. The data has reached its destination (DRAM or MC), and the write data transfer has completed on the DRAM bus; The state of the DRAM bus is unchanged. The DFI specification supports both MC-initiated and PHY-initiated updates. For more information on the update interface, refer to Section 4.6, “Update,” on page 89.

The MC initiates an update request by asserting the **dfi_ctrlupd_req** signal, following initialization, and training if required. The PHY can acknowledge or ignore the request. If the PHY acknowledges the request, by asserting the **dfi_ctrlupd_ack** signal, the protocol described in Section 4.6.1, “MC-Initiated Update,” on page 89 must be followed.

The $\mathbf{t}_{\mathbf{ctrlupd\_interval}}$ parameter defines the maximum interval at which the MC can assert **dfi_ctrlupd_req** signals. Following a self-refresh exit, the **dfi_ctrlupd_req** signal must be asserted prior to allowing read/write traffic to begin.

If a PHY initiates an update request by asserting the **dfi_phyupd_req** signal, the MC must acknowledge the request by asserting the **dfi_phyupd_ack** signal. The DFI specifies up to 4 different update PHY-initiated request modes. Each mode differs only in the number of cycles that the DFI interface must be suspended while the update occurs. During this time, the MC is responsible for placing the system in a state where the DFI bus is suspended from all activity other than activity specifically related to the update process being executed. For more details, refer to Section 4.6.2, “PHY-Initiated Update,” on page 90.

The DFI specification does not require the PHY to issue update requests nor does the specification specify an interval in which requests must be offered. If the PHY offers update requests, it must follow the specified protocol.

It is possible that both update request signals (**dfi_ctrlupd_req** and **dfi_phyupd_req**) could be asserted at the same time. When both request signals are driven, the MC and the PHY could violate the protocol by simultaneously acknowledging the other's request. To prevent this situation, the MC is not permitted to assert both **dfi_ctrlupd_req** and **dfi_phyupd_ack** at the same time. If **dfi_ctrlupd_req** is asserted at the same time as **dfi_phyupd_req**, the PHY is permitted to de-assert **dfi_phyupd_req**, though it is not required to be de-asserted. This is the only situation in which the PHY is permitted to de-assert the **dfi_phyupd_req** signal without an acknowledge from the MC. Since it is the PHY (not the MC) that uses the Update interface to request the DFI bus to be IDLE, the PHY should not

de-assert **dfi_phyupd_req** unless the signal is no longer required due to the assertion of **dfi_ctrlupd_req.** The acknowledged request must follow the appropriate protocol.

The signals and timing parameters in the update interface are listed in Table 12 and Table 13.

For more information on the update interface, refer to Section 4.6, "Update," on page 89. For more information on which signals are required and which signals are optional, refer to Table 2, "DFI Signal Requirements," on page 18.

The signals associated with the update interface are listed in Table 12.

TABLE 12. *Update Interface Signals*

Signal	From	Width	Default	Description
dfi_ctrlupd_ack	PHY	1 bit	0x0	MC-initiated update acknowledge. The **dfi_ctrlupd_ack** signal is asserted to acknowledge an MC-initiated update request. The PHY is not required to acknowledge this request. While this signal is asserted, the DFI bus must remain in the idle state except for transactions specifically associated with the update process. If the PHY acknowledges the request, the **dfi_ctrlupd_ack** signal must be asserted before $\mathbf{t_{ctrlupd\_min}}$ occurs and the **dfi_ctrlupd_req** signal de-asserts. If the PHY ignores the request, the **dfi_ctrlupd_ack** signal must remain de-asserted until the **dfi_ctrlupd_req** signal is de-asserted. The **dfi_ctrlupd_req** signal is guaranteed to be asserted for at least $\mathbf{t_{ctrlupd\_min}}$ cycles. The **dfi_ctrlupd_ack** signal cannot be asserted after $\mathbf{t_{ctrlupd\_min}}$, occurs, even if **dfi_ctrlupd_req** is still asserted.

TABLE 12. *Update Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_ctrlupd_req	MC	1 bit	0x0	MC-initiated update request. The **dfi_ctrlupd_req** signal is used with an MC-initiated update to indicate that the DFI will be in the idle state for some time, in which case the PHY may perform an update. The **dfi_ctrlupd_req** signal must be asserted for a minimum of $\mathbf{t_{ctrlupd\_min}}$ cycles and a maximum of $\mathbf{t_{ctrlupd\_max}}$ cycles. A **dfi_ctrlupd_req** signal assertion is an invitation for the PHY to update and does not require a response. The behavior of the **dfi_ctrlupd_req** signal is dependent on the **dfi_ctrlupd_ack** signal: • If the update is acknowledged by the PHY, the **dfi_ctrlupd_req** signal remains asserted as long as the **dfi_ctrlupd_ack** signal is asserted, but **dfi_ctrlupd_ack** must de-assert before $\mathbf{t_{ctrlupd\_max}}$ expires. While **dfi_ctrlupd_req** is asserted, the DFI bus remains in the idle state except for transactions specifically associated with the update process. • If the update is not acknowledged, the **dfi_ctrlupd_req** signal may de-assert at any time after $\mathbf{t_{ctrlupd\_min}}$ occurs**,** and before $\mathbf{t_{ctrlupd\_max}}$.expires.
dfi_phyupd_ack	MC	1 bit	0x0	PHY-initiated update acknowledge. The **dfi_phyupd_ack** signal is used for a PHY-initiated update to indicate that the DFI is idle and remains in the idle state until the **dfi_phyupd_req** signal de-asserts. The MC must assert the **dfi_phyupd_ack** signal within $\mathbf{t_{phyupd\_resp}}$ cycles of the **dfi_phyupd_req** signal, and must remain asserted as long as the **dfi_phyupd_req** signal remains asserted. The **dfi_phyupd_ack** signal must de-assert upon the detection of **dfi_phyupd_req** signal de-assertion. The **dfi_phyupd_req** cannot be re-asserted prior to the de-assertion of **dfi_phyupd_ack** for the previous transaction. NOTE: If a **dfi_ctrlupd_req** occurs at the same time as a **dfi_phyupd_req**, the $\mathbf{t_{phyupd\_resp}}$ requirement is allowed to not be met since **dfi_phyupd_ack** and **dfi_ctrlupd_req** cannot be asserted simultaneously. While **dfi_phyupd_ack** is asserted, the DFI bus must remain in the idle state except for transactions specifically associated with the update process. The time period from when the **dfi_phyupd_ack** signal is asserted to when the **dfi_phyupd_req** signal is de-asserted is a maximum of $\mathbf{t_{phyupd\_typeX}}$ cycles, based on the **dfi_phyupd_type** signal.

TABLE 12. *Update Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_phyupd_req	PHY	1 bit	0x0	PHY-initiated update request. The **dfi_phyupd_req** signal is used for a PHY-initiated update to indicate that the PHY requires the DFI bus to be placed in an idle state and not send control, read or write commands or data for a specified period of time. The maximum time required is specified by the $\mathbf{t_{phyupd\_typeX}}$ parameter associated with the **dfi_phyupd_type** signal. Once asserted, the **dfi_phyupd_req** signal must remain asserted until the request is acknowledged by the assertion of the **dfi_phyupd_ack** signal and the update has been completed. The MC must acknowledge this request. While this signal is asserted, the DFI bus must remain in the idle state other than any transactions specifically associated with the update process. The de-assertion of the **dfi_phyupd_req** signal triggers the de-assertion of the **dfi_phyupd_ack** signal.
dfi_phyupd_type	PHY	2 bits	- [a]	PHY-initiated update select. The **dfi_phyupd_type** signal indicates which one of the 4 types of PHY update times is being requested by the **dfi_phyupd_req** signal. The value of the **dfi_phyupd_type** signal determines which of the timing parameters ($\mathbf{t_{phyupd\_type0}}$, $\mathbf{t_{phyupd\_type1}}$, $\mathbf{t_{phyupd\_type2}}$, $\mathbf{t_{phyupd\_type3}}$) is relevant. The **dfi_phyupd_type** signal must remain constant during the entire time the **dfi_phyupd_req** signal is asserted.

[a] This signal is not meaningful during initialization; no default value is required.

The timing parameters associated with the update interface are listed in Table 13.

TABLE 13. *Update Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{ctrlupd\_interval}}$	MC	- [a]	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the MC may wait between assertions of the **dfi_ctrlupd_req** signal.
$\mathbf{t_{ctrlupd\_min}}$	MC	1	- [a]	DFI clock cycles	Specifies the minimum number of DFI clock cycles that the **dfi_ctrlupd_req** signal must be asserted.
$\mathbf{t_{ctrlupd\_max}}$	MC	- [a]	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_ctrlupd_req** signal can assert.

TABLE 13. *Update Timing Parameters (Continued)*

Parameter	Defined By	Min	Max	Unit	Description
t_{phyupd_type0}	PHY	1	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_phyupd_req** signal may remain asserted after the assertion of the **dfi_phyupd_ack** signal for **dfi_phyupd_type** = 0x0. The **dfi_phyupd_req** signal may de-assert at any cycle after the assertion of the **dfi_phyupd_ack** signal.
t_{phyupd_type1}	PHY	1	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_phyupd_req** signal may remain asserted after the assertion of the **dfi_phyupd_ack** signal for **dfi_phyupd_type** = 0x1. The **dfi_phyupd_req** signal may de-assert at any cycle after the assertion of the **dfi_phyupd_ack** signal.
t_{phyupd_type2}	PHY	1	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_phyupd_req** signal may remain asserted after the assertion of the **dfi_phyupd_ack** signal for **dfi_phyupd_type** = 0x2. The **dfi_phyupd_req** signal may de-assert at any cycle after the assertion of the **dfi_phyupd_ack** signal.
t_{phyupd_type3}	PHY	1	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_phyupd_req** signal may remain asserted after the assertion of the **dfi_phyupd_ack** signal for **dfi_phyupd_type** = 0x3. The **dfi_phyupd_req** signal may de-assert at any cycle after the assertion of the **dfi_phyupd_ack** signal.
t_{phyupd_resp}	PHY	1	- [a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles after the assertion of the **dfi_phyupd_req** signal to the assertion of the **dfi_phyupd_ack** signal.

[a] The minimum supportable value is 1; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

3.5 Status Interface

The status interface signal conveys status information between the MC and the PHY for initialization and clock control to the DRAM devices.

3.5.1 Initialization

Initialization uses the **dfi_init_start** and **dfi_init_complete** signals. These signals are also used during a frequency change request, which Section 3.5.3, “Frequency Ratio,” on page 42 describes in detail. At initialization, the **dfi_init_start** signal indicates to the PHY that the frequency ratio, data byte lane use, or both have been defined. The PHY can use this signal to detect when these settings from the MC are valid.

At initialization, the **dfi_init_complete** signal indicates that the PHY is ready to accept DFI transactions. The optional **dfi_data_byte_disable** signal is used for informing the PHY the data slices that will be unused. The value of the **dfi_data_byte_disable** signal, which is not expected to change, must be defined at initialization.

The byte lanes correspond to the byte order defined for the **dfi_wrdata** and **dfi_rddata** signals. The MC and the PHY must both support the same partial use of data signals in order to use byte disabling. For example, if the MC disables the upper bits (most significant bits) of the data bus, the PHY must be able to operate accurately with the remaining byte lanes. The DFI specification does not define supported active/inactive patterns, and therefore care must be taken to insure the interoperability of the MC and the PHY.

For more information on initialization, refer to Section 4.1, “Initialization,” on page 62.

3.5.2 Clock Disabling

The **dfi_dram_clk_disable** signal is used by the MC to inform the PHY when to enable/disable the clock to the DRAMs. The timing parameters $\mathbf{t_{dram\_clk\_disable}}$ and $\mathbf{t_{dram\_clk\_enable}}$ define the timing of the DRAM clock enable/disable relative to the **dfi_dram_clk_disable** signal.

For more information on the DFI clock interface, refer to Section 4.7, “DFI Clock Disabling,” on page 92.

3.5.3 Frequency Ratio

The optional **dfi_freq_ratio** signal is used for conveying frequency ratio information to the PHY. This static signal indicates the ratio expected by the MC, and dictates how control, read and write information is passed across the DFI.

For more information on the frequency ratio protocol, refer to Section 4.8, “Frequency Ratios Across the DFI,” on page 93.

3.5.4 Frequency Change

The DFI specification defines a frequency change protocol between the MC and the PHY to allow the devices to change the clock frequency of the MC and the PHY without completely resetting the system.

The signals used in the frequency change protocol are **dfi_init_start** and **dfi_init_complete** during normal operation. The behavior of the **dfi_init start** signal depends on the **dfi_init_complete** signal. A frequency change request is triggered when the MC asserts **dfi_init_start**. The PHY indicates the acceptance of the frequency change by asserting **dfi_init_complete**. The associated timing parameters are $\mathbf{t_{init\_start}}$ and $\mathbf{t_{init\_complete}}$.

For more information on the frequency change protocol, refer to Section 4.9, “Frequency Change,” on page 110.

3.5.5 CRC and CA Parity

The CRC and CA parity support signals are provided specifically for DDR4 and DDR3 DRAMs. The DDR4 and DDR3 systems include additional IO pins to receive command parity, communicate command parity, and write CRC error status. In systems that require command parity support, the MC communicates its command parity setting on the **dfi_parity_in** signal. In systems that require either command parity or CRC support, the PHY reports command parity errors on the **dfi_alert_n_aN** signal.

For more information on CRC and CA parity support signals, refer to Section 3.6, “DFI Training Interface,” on page 47 and Section 3.6, “DFI Training Interface,” on page 47.

The **dfi_init_start** signal and the **dfi_init_complete** signal are used at initialization and as part of the frequency change protocol.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the status interface are listed in Table 14.

TABLE 14. *Status Interface Signals*

Signal	From	Width	Default	Description
dfi_alert_n_aN [a]	PHY	DFI Alert Width	1	CRC or parity error indicator. This signal is driven when a CRC or command parity error is detected in the memory system. The PHY is not required to distinguish between a CRC and command parity error. The PHY holds the current state until the PHY error input transitions to a new value; the pulse width of the **dfi_alert_n_aN** signal matches the pulse width of the DRAM subsystem error signal, plus or minus synchronization cycles.
dfi_data_byte_disable	MC	DFI Data Width/8	- [b]	Data byte disable. When set, this signal indicates that the associated data byte is not being used. In this state, the PHY is permitted to place the associated bytes in a low power state. When the bit is clear, the byte operates normally. The byte lanes correspond to the byte order defined for the **dfi_wrdata** and **dfi_rddata** signals. This signal may be defined only during initialization, and is expected to remain constant. When defined, the MC drives the **dfi_init_start** signal to the PHY.
dfi_dram_clk_disable	MC	DFI Chip Select Width	0x0 [c]	DRAM clock disable. When active, this indicates to the PHY that the clocks to the DRAM devices must be disabled such that the clock signals hold a constant value. When the **dfi_dram_clk_disable** signal is inactive, the DRAMs should be clocked normally.

TABLE 14. *Status Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_freq_ratio	MC	2 bits	- [b]	DFI frequency ratio indicator. This signal defines the frequency ratio for this system. This signal is required for MCs and PHYs that support multiple frequency ratios and the DFI frequency ratio protocol. This signal is optional for MCs and PHYs that support only a single frequency ratio or do not support the DFI frequency ratio protocol. This signal may only be defined during initialization, and is expected to remain constant. Once defined, the MC drives the **dfi_init_start** signal to the PHY. • ‘b00 = 1:1 MC:PHY frequency ratio (matched frequency) • ‘b01 = 1:2 MC:PHY frequency ratio • ‘b10 = 1:4 MC:PHY frequency ratio • ‘b11 = Reserved
dfi_init_complete	PHY	1 bit	0x0	PHY initialization complete. The **dfi_init_complete** signal indicates that the PHY is able to respond to any proper stimulus on the DFI. All DFI signals that communicate commands or status must be held at their default values until the **dfi_init_complete** signal asserts. During a PHY re-initialization request (such as a frequency change), this signal is de-asserted. For a frequency change request, the de-assertion of the **dfi_init_complete** signal acknowledges the frequency change protocol. Once de-asserted, the signal should only be re-asserted within $\mathbf{t_{init\_complete}}$ cycles after the **dfi_init_start** signal has de-asserted, and once the PHY has completed re-initialization.

TABLE 14. *Status Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_init_start	MC	1 bit	0x0 [d] 0x1	DFI setup stabilization or frequency change initiation. This optional signal can perform two functions. When **dfi_init_start** is asserted during initialization, the MC is indicating that the **dfi_data_byte_disable** or **dfi_freq_ratio** signals or both (if present) have been defined. When **dfi_init_start** is asserted during normal operation, the MC is requesting a frequency change. During initialization, when both **dfi_init_start** and **dfi_init_complete** are asserted for at least one DFI clock cycle, the MC can either hold or de-assert the **dfi_init_start** signal. For frequency change, the **dfi_init_start** signal must assert to trigger the event. After the rising edge of **dfi_init_start** occurs, the behavior of the **dfi_init_start** signal depends on the **dfi_init_complete** signal as follows: • If the PHY accepts the frequency change request, it must de-assert the **dfi_init_complete** signal within $\mathbf{t}_{\mathbf{init\_start}}$ cycles of the **dfi_init_start** assertion. The MC continues to hold the **dfi_init_start** signal asserted until the clock frequency change has been completed. The de-assertion should be used by the PHY to reiinitialize on the new clock frequency. • If the frequency change is not acknowledged (the **dfi_init_complete** signal remains asserted), the **dfi_init_start** signal must de-assert after $\mathbf{t}_{\mathbf{init\_start}}$ cycles. • The frequency must assert **dfi_init_start** until **dfi_init_complete** is asserted at least one DFI clock. Initialization is complete when both the **dfi_init_start** and the **dfi_init_complete** signals are asserted simultaneously for at least one DFI clock.
dfi_parity_in or **dfi_parity_in_pN** [a]	MC	1 bit	0x0 [e] 0x1[e]	Parity value. This signal has a one-to-one correspondence with each DFI command and is valid for 1 cycle. This value applies to the **dfi_address**, **dfi_bank**, **dfi_bg, dfi_act_n, dfi_cas_n**, **dfi_ras_n** and **dfi_we_n** signals. This signal is relevant for only systems that support command parity. • ‘b0 = An even number of the parity value signals are electrically high. • ‘b1 = An odd number of the parity value signals are electrically high.

[a] For frequency ratio systems, replicates signals into phase/data word/clock cycle-specific buses that define the validity of the data for each phase N (pN)/data word N (wN)/clock cycle N (aN), as applicable. The phase 0 suffixes are not required.

[b] At initialization, this signal must be driven with the valid settings for the system to convey information to the PHY. Refer to this table.

[c] When **dfi_init_start** is asserted during initialization, **dfi_dram_clk_disable** must indicate the clocks that are being used. In normal operation, this signal can dynamically change.

[d] The PHY may optionally wait for the **dfi_init_start** signal assertion before asserting the **dfi_init_complete** signal.

e. The value of this signal must be driven with the correct parity for the selected control interface signals.

The timing parameters associated with the status interface are listed in Table 15.

TABLE 15. *Status Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$t_{dram\_clk\_disable}$ [a]	PHY	0	- [b]	DFI clock cycles [c]	Specifies the number of DFI clock cycles from the assertion of the **dfi_dram_clk_disable** signal on the DFI until the clock to the DRAMs at the PHY-DRAM boundary maintains a low value. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.
$t_{dram\_clk\_enable}$ [a]	PHY	0	- [b]	DFI clock cycles [c]	Specifies the number of DFI clock cycles from the de-assertion of the **dfi_dram_clk_disable** signal on the DFI until the first valid rising edge of the clock to the DRAMs at the PHY-DRAM boundary. NOTE: This parameter may be specified as a fixed value, or as a constant based on other fixed values in the system.
$t_{init\_complete}$	PHY	0	- [b]	DFI clock cycles [c]	Specifies the maximum number of DFI clock cycles after the de-assertion of the **dfi_init_start** signal to the re-assertion of the **dfi_init_complete** signal during a frequency change operation.
t_{init_start}	MC	0	- [b]	DFI clock cycles [c]	During a frequency change operation, this parameter specifies the number of DFI clock cycles from the assertion of the **dfi_init_start** signal on the DFI until the PHY must respond by de-asserting the **dfi_init_complete** signal. If the **dfi_init_complete** signal is not de-asserted within this time period, the PHY indicates that it can not support the frequency change at this time. In this case, the MC must abort the request and release the **dfi_init_start** signal. When t_{init_start} expires, the PHY must not de-assert the **dfi_init_complete** signal. The MC can re-assert **dfi_init_start** at a later point.
t_{parin_lat}	MC	0	- [b]	DFI PHY clock cycles [c]	Specifies the number of DFI PHY clocks between when the dfi command is asserted and when the associated **dfi_parity_in** signal is driven.
$t_{phy\_paritylat}$	PHY	4	- [b]	DFI clock cycles [c]	Specifies the maximum number of DFI clock cycles between when the **dfi_parity_in** signal is driven and when the associated **dfi_alert_n_aN** signal is returned.

a. If the DFI clock and the DRAM clock are not phase-aligned, this timing parameter should be rounded up to the next integer value.

b. The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

c. For matched frequency systems, a DFI PHY clock is identical to the DFI clock. For frequency ratio systems, this timing parameter is defined in terms of DFI PHY clock cycles.

3.6 DFI Training Interface

The DFI training interface enables increased accuracy at higher speeds in the alignment of critical timing signals on DDR4, DDR3, LPDDR3 and LPDDR2 DRAMs; the interface includes signals, timing parameters, and programmable parameters.

The DRAM type and system configuration determine the types of training available to a system; a system may or may not utilize each type of training. If training is supported, the system may utilize DFI training or support a different training method. There are four training operations; the first two operations (gate training, and read data eye training) are collectively referred to as "read training".

4. Gate training, used by DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs.
5. Read data eye training, used by DDR4, DDR3, LPDDR3, and LPDDR2 DRAMs.
6. Write leveling, used by DDR4, DDR3, and LPDDR3 DRAMs.
7. CA training, only applicable to the MCs and PHYs that support LPDDR3 DRAMs.

To be DFI-compliant, the MC is required to support read training, write leveling, and CA training operations whereas the PHY optionally supports each of the operations.

Support for each training operation is enabled or disabled through the corresponding programmable parameter and the enable may be implemented as programmable registers within the device.

The read training, write leveling, and CA training signals that communicate from the MC to the PHY are multiply driven inside the MC to allow a direct connection from the MC to each PHY data slice and the signals must be driven with the same value.

The read training, write leveling, and CA training signals that communicate from the PHY to the MC may be individually driven by each PHY data slice or collectively driven as a single signal.

More information on the training interface is provided in Section 4.10.1, "CA Parity Timing," on page 113. The signals, timing parameters, and programmable parameters for the training interface are listed in Table 16, "Training Interface Signals," on page 49. The timing parameters associated with the training interface are listed in Table 17, "Training Interface Timing Parameters," on page 53. The programmable parameters associated with the training interface are listed in Table 18, "DFI Training Programmable Parameters," on page 55.

The MC and the PHY can be synchronized with the defined training sequences, and the sequence required for each training operation, with **dfi_lvl_pattern** encoding. For information on **dfi_lvl_pattern** encoding, refer to Section 3.6.4, "dfi_lvl_pattern Encoding," on page 55. For information on multiple training patterns used with LPDDR3 and LPDDR2, refer to Table 26, "Data Calibration Pattern," on page 126.

Long or short training sequences can be defined with the **dfi_lvl_periodic** signal. For information on the **dfi_lvl_periodic** signal, refer to Section 3.6.5, "Periodic Training Flag," on page 56.

Training sequences can be initiated in non-DFI mode after initialization has completed. For information on initiating training sequences, refer to Section 3.6.7, "PHY-Requested Training in Non-DFI Training Mode," on page 56.

3.6.1 Read Training Operation

In DFI read training mode, the MC sets up the DRAM for gate training or read data eye training and periodically issues read commands. The PHY evaluates the data returned from the commands and adjusts the gate training and read data eye training capture timing accordingly.

Multiple training sequences can be defined, with either the MC or the PHY supplying the sequence information. In DFI training mode, the PHY is responsible for adjusting the delays and evaluating the responses from the DRAM. Therefore, it is the PHY, not the MC, which determines the sequences necessary to accomplish training. The MC must provide flexibility to run sequences required by the PHY and should not dictate a set of sequences.

A read training sequence can be initiated from the MC or the PHY. In both cases, the MC asserts the **dfi_rdlvl_en** signal to initiate or accept the training sequence, and the MC holds the enable signal asserted until the current training operation completes. During read training, **dfi_rddata_cs_n** indicates the chip select that is currently being trained.

For more information on **dfi_rddata_cs_n**, refer to Section 3.3, “Read Data Interface,” on page 33, and Table 9, “Read Data Signals,” on page 35.

In DDR4, LPDDR3, and LPDDR2 systems, the MC drives the **dfi_lvl_pattern** signal to define the required training sequence. The **dfi_lvl_pattern** signal must be valid when either **dfi_rdlvl_gate_en** (for read gate training) or **dfi_rdlvl_en** (for read data eye training) is asserted. Similar to **dfi_rdlvl_en**, the **dfi_lvl_pattern** signal may transition after training completes. Due to a difference in the training patterns, the **dfi_lvl_pattern** signal definition is different for DDR4 than for LPDDR3 and LPDDR2.

For more information on read training, refer to Section 4.11, “DFI Training Operations,” on page 115, Table 25, “DDR4 Encoding of dfi_lvl_pattern,” on page 125, and Table 26, “Data Calibration Pattern,” on page 126.

3.6.2 Write Leveling Operation

The goal of write leveling is to locate the delay at which the write DQS rising edge aligns with the rising edge of the DRAM clock. By identifying this delay, the system can accurately align the write DQS within the DRAM clock.

A write leveling sequence can be initiated from the MC or the PHY. In both cases, the MC asserts the **dfi_wrlvl_en** signal to initiate or accept the leveling sequence, and the MC holds the enable signal asserted until the current training operation completes. During write leveling, **dfi_wrdata_cs_n** indicates the chip select that is currently being trained.

The signals used in write leveling are: **dfi_wrlvl_en**, **dfi_wrlvl_req**, and **dfi_wrlvl_strobe**. The programmable parameter is **$\mathbf{phy_{wrlvl\_en}}$**. The write leveling chip select signal is **dfi_phy_wrlvl_cs_n**.

For more information on **dfi_phy_wrlvl_cs_n, refer to** Section 3.2, “Write Data Interface,” on page 29 and Table 6, “Write Data Signals,” on page 31.

For more information on write leveling signals, refer to Section 58, “Read Training in DFI Training Mode for LPDDR3 and LPDDR2 Memory Systems,” on page 119.

3.6.3 CA Training Operation

CA training supports increased frequency and the double-data rate address and command interface.

During CA training, the PHY may selectively not utilize any of the MC signals defined in the protocol, however the PHY must drive all signals to the MC, as defined. Some of the CA training signals from the MC to the PHY are multiply driven by the MC to allow a direct connection from the MC to the PHY memory command logic and/or each of the PHY memory data slices. All multiply driven signals originating from the MC to the PHY are driven with identical values.

The signals specific to CA training are: **dfi_calvl_capture** (CA training capture), **dfi_phy_calvl_cs_n** (CA training chip select), **dfi_calvl_en** (PHY CA training logic enable), **dfi_calvl_req (**PHY-initiated CA training request), and **dfi_calvl_resp** (CA training response) described in Table 16, “Training Interface Signals”.

Signals modified to support CA training are: **dfi_address** (DFI address bus), **dfi_cke** (DFI clock enable), and **dfi_cs_n** (DFI chip select) described in Table 4, “Control Signals,” on page 27.

CA training parameters $\mathbf{phy_{calvl\_en}}$ (PHY CA training mode), $\mathbf{t_{calvl\_capture}}$ (CA training capture delay from command), $\mathbf{t_{calvl\_en}}$ (CA training enable time), $\mathbf{t_{calvl\_max}}$ (CA training maximum time), $\mathbf{t_{calvl\_resp}}$ (CA training response), and $\mathbf{t_{calvl\_cc}}$ (CA training chip select to chip select delay) are described in Table 18, “DFI Training Programmable Parameters,” on page 55.

The $\mathbf{phy_{calvl\_en}}$ programmable parameter specifies the PHY operating mode. When the parameter is asserted, DFI CA training is enabled in the PHY. When the parameter is de-asserted, DFI CA training is disabled in the PHY. The MC must support the $\mathbf{phy_{calvl\_en}}$ parameter in both asserted and de-asserted modes; the PHY may support the $\mathbf{phy_{calvl\_en}}$ parameter in one or both modes.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the training interface are listed in Table 16.

TABLE 16. *Training Interface Signals*

Signal	From	Width	Default	Description
dfi_calvl_capture	MC	DFI CA Training MC I/F Width		CA training capture. This signal is asserted for one DFI clock pulse; initiates the capture of the CA bus value from the DQ bus within the PHY. The capture pulse is asserted $\mathbf{t_{calvl\_capture}}$ cycles after the calibration command is driven on **dfi_cs_n**.
dfi_phy_calvl_cs_n	PHY	DFI Chip Select Width		CA training chip select. Indicates the target chip select associated with the current **dfi_calvl_req**. This signal is only valid when **dfi_calvl_req** is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
dfi_calvl_en	MC	DFI CA Training MC I/F Width		PHY CA training logic enable. This signal is asserted during CA training and can be used by the PHY to enable the associated logic to execute training. If the PHY initiated the CA training request (**dfi_calvl_req**), this serves as acknowledgement of the request. • ’b0 = Normal operation • ’b1 = CA training enabled. The assertion of this signal immediately initiates the CA training process.

TABLE 16. *Training Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_calvl_req	PHY	DFI CA Training PHY I/F Width		PHY-initiated CA training request. This is an optional signal for the PHY; other sources may be used to initiate CA training or the MC may initiate CA training independently. If the PHY asserts the **dfi_calvl_req** signal, the MC must acknowledge this request by asserting the **dfi_calvl_en** signal within $\mathbf{t_{calvl\_resp}}$ cycles, after which the PHY should de-assert the **dfi_calvl_req** signal. The PHY is not required to assert this signal during initialization or a frequency change operation. However, if the PHY does assert the request during a frequency change, the **dfi_calvl_req** signal must be asserted before or coincident with the assertion of the **dfi_init_complete** signal.
dfi_calvl_resp	PHY	DFI CA Training Response Width		CA training response. This signal indicates that the PHY has completed the current CA training routine. The training sequence may consist of one or more training routines to each of the two CA segments. The response is defined as follows: • ’b00 = Not done • ’b01 = Done with pattern, do not change CA segment • ‘b10 = Done with pattern, change CA segment • ‘b11 = Complete The **dfi_calvl_resp** signal is asserted during both phase 1 CA training (enabled with MR41) and phase 2 CA training (enabled with MR48). The width of the **dfi_calvl_resp** signal is generally defined as two bits.
dfi_lvl_pattern	MC	4-bits x DFI Read Training PHY I/F Width [a], 1 [b]	0x0 [a], 0x1[b]	Training pattern. Used to determine which training pattern should be run with the current read training operation. This is used with both gate training and read data eye training. For LPDDR3 and LPDDR2 DRAMs, **dfi_lvl_pattern** also defines the pattern used for read training. • ‘b0 = Issue 1 MRR command to MR32. • ‘b1 = Issue 1 MRR command to MR40.
dfi_lvl_periodic	MC	DFI Leveling PHY I/F Width	0	Training length indicator (full or periodic). Global signal used for all training interfaces, which dictates the type of training required. • ‘b0 = Full training required; long sequence used during initialization and for larger variations. • ‘b1 = Periodic training required; shorter sequence used for small variations.
dfi_phylvl_ack_cs_n	MC	DFI Chip Select Width		DFI PHY training chip select acknowledge. MC acknowledgement of PHY request to train a chip select, which is granted only when the DRAM bus is idle and available for the PHY to use for training.

TABLE 16. *Training Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_phylvl_req_cs_n	PHY	DFI Rank Width		DFI PHY training chip select request. This signal enables the PHY to request to train each chip select individually.
dfi_phy_rdlvl_cs_n	PHY	DFI Chip Select Width x DFI Read Training PHY I/F Width	0x1	Read training chip select for read data eye training. Indicates the target chip select associated with the current **dfi_rdlvl_req**. This signal is only valid when **dfi_rdlvl_req** is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
dfi_phy_rdlvl_gate_cs_n	PHY	DFI Chip Select Width x DFI Read Training PHY I/F Width	0x1	Read training chip select for gate training. Indicates the target chip select associated with the current **dfi_rdlvl_gate_req**. This signal is only valid when **dfi_rdlvl_gate_req** is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
dfi_phy_wrlvl_cs_n	PHY	DFI Chip Select Width x DFI Write Leveling PHY I/F Width	0x1	Write leveling chip select. Indicates the target chip select associated with the current **dfi_wrlvl_req**. This signal is only valid when **dfi_wrlvl_req** is asserted. Only a single bit can be asserted during the request. If no bits are asserted, the MC determines which chip select(s) to target for the training request.
dfi_rdlvl_en	MC	DFI Read Leveling MC I/F Width	0x0	PHY read data eye training logic enable. This signal is asserted during read data eye training. If the PHY initiated the read data eye training request (**dfi_rdlvl_req**), this serves as an acknowledge of that request. • ‘b0 = Normal operation • ‘b1 = Read Data eye training logic enabled. The assertion of this signal immediately initiates read data eye training. This signal may enable specific training logic within the PHY. If the **dfi_rdlvl_en** signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0 on de-assertion of this signal. For more information, refer to Section 4.8.4, “Read Data Interface in Frequency Ratio Systems”.

TABLE 16. *Training Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_rdlvl_gate_en	MC	DFI Read Leveling MC I/F Width	0x0	PHY gate training logic enable. This signal is asserted during gate training. If the PHY initiated the gate training request (**dfi_rdlvl_gate_req**), this serves as an acknowledge of that request. • 'b0 = Normal operation • 'b1 = Gate training logic enabled. The assertion of this signal immediately triggers gate training. If the **dfi_rdlvl_gate_en** signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0 on de-assertion of this signal. For more information, refer to Section 4.8.4, "Read Data Interface in Frequency Ratio Systems".
dfi_rdlvl_gate_req	PHY	DFI Read Leveling PHY I/F Width	0x0	PHY-initiated gate training request. The PHY initiates gate training, other sources may be used to initiate gate training, or the MC may initiate gate training independently. The PHY may drive independent gate training requests from each data slice; however the MC must gate train all data slices based on a single assertion of the **dfi_rdlvl_gate_req** signal. If the PHY asserts the **dfi_rdlvl_gate_req** signal, the MC must acknowledge the request by asserting the **dfi_rdlvl_gate_en** signal within $\mathbf{t_{rdlvl\_resp}}$ cycles, after which the PHY should de-assert the **dfi_rdlvl_gate_req** signal. The PHY should not assert **dfi_rdlvl_gate_req** during initialization and frequency change operations because the MC is responsible for gate training during these operations.
dfi_rdlvl_req [a]	PHY	DFI Read Leveling PHY I/F Width	0x0	PHY-initiated read data eye training request. The PHY initiates read data eye training, other sources may be used to initiate read data eye training, or the MC may initiate read data eye training independently. The PHY may drive independent read data eye training requests from each data slice; however the MC must read level all data slices based on a single assertion of the **dfi_rdlvl_req** signal. If the PHY asserts the **dfi_rdlvl_req** signal, the MC must acknowledge the request by asserting the **dfi_rdlvl_en** signal within $\mathbf{t_{rdlvl\_resp}}$ cycles, after which the PHY should de-assert the **dfi_rdlvl_req** signal.
dfi_rdlvl_resp	PHY	DFI Read Leveling Response Width		Read training response. Indicates that the PHY has completed read data eye training or gate training. The width of the **dfi_rdlvl_resp** signal is generally defined as a bit-per-PHY data slice.

TABLE 16. *Training Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_wrlvl_en	MC	DFI Write Leveling MC I/F Width	0x0	PHY write leveling logic enable. This signal is asserted during write leveling. If the PHY initiated the write leveling request (**dfi_wrlvl_req**), this serves as an acknowledge of that request. • ‘b0 = Normal operation • ‘b1 = Write leveling enabled. The assertion of this signal initiates write leveling.
dfi_wrlvl_req [a]	PHY	DFI Write Leveling PHY I/F Width	0x0	PHY write leveling request. This is an optional signal for the PHY; other sources may be used to initiate write leveling, or the MC may initiate write leveling independently. The PHY may drive independent write leveling requests from each data slice; however the MC must write level all data slices based on a single assertion of the **dfi_wrlvl_req** signal. If the PHY asserts the **dfi_wrlvl_req** signal, the MC must acknowledge the request by asserting the **dfi_wrlvl_en** signal within $\mathbf{t_{wrlvl\_resp}}$ cycles, after which the PHY should de-assert the **dfi_wrlvl_req** signal.
dfi_wrlvl_resp	PHY	DFI Write Leveling Response Width		Write leveling response. Indicates that the PHY has completed write leveling. The width is generally defined as a bit-per-PHY data slice.
dfi_wrlvl_strobe	MC	DFI Write Leveling MC I/F Width	0x0	Write leveling strobe. Asserts for one DFI clock pulse; initiates the capture of the write level response from the DQ bus within the PHY.

a. Applies to DDR4 DRAMs.

b. Applies to LPDDR2 and LPDDR3 DRAMs.

Table 16, “Training Interface Signals,” on page 49 identifies timing parameters that are relevant for certain read training and write leveling operations. Table 17, “Training Interface Timing Parameters” lists the timing parameters that are associated with the training interface. All timing parameters are defined only once for the interface and must apply to all PHY data slices.

TABLE 17. *Training Interface Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{calvl\_capture}}$	PHY	1	-[a]	DFI clock cycles	CA training capture delay from command. Specifies the number of DFI clock cycles after the controller transmits the calibration command on **dfi_cs_n** before the **dfi_ca_capture** pulse is driven.
$\mathbf{t_{calvl\_en}}$	PHY	1	-[a]	DFI clock cycles	CA training enable time. Specifies the minimum number of DFI clock cycles from the assertion of the **dfi_calvl_en** signal to the de-assertion of the **dfi_cke** signal.

TABLE 17. *Training Interface Timing Parameters (Continued)*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{calvl\_max}}$	MC	1	-[a]	DFI clock cycles	CA training maximum time. Specifies the maximum number of DFI clock cycles that the MC will wait for a response (**dfi_calvl_resp**) to a CA training enable signal (**dfi_calvl_en)**.
$\mathbf{t_{calvl\_resp}}$	MC	1	-[a]	DFI clock cycles	CA training response. Specifies the maximum number of DFI clock cycles after a CA training request is asserted (**dfi_calvl_req**) to when the MC will respond with a CA training enable signal (**dfi_calvl_en**).
$\mathbf{t_{calvl\_cc}}$	PHY	1	-[a]	DFI clock cycles	CA training chip select to chip select delay. Specifies the minimum number of DFI clock cycles from one calibration command to the next calibration command.
$\mathbf{t_{phylvl}}$	PHY	1	-[a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that the **dfi_phylvl_req_cs_n(x)** signal may remain asserted after the assertion of the **dfi phylvl_ack_cs_n(x)** signal. The **dfi_phylvl_req_cs_n(x)** signal may de-assert at any cycle after the assertion of the **dfi_phylvl_ack_cs_n(x)** signal.
$\mathbf{t_{phylvl\_resp}}$	PHY	1	-[a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles after the assertion of the **dfi phylvl_req_cs_n(x)** signal to the assertion of the **dfi_phylvl_ack_cs_n(x)** signal.
$\mathbf{t_{rdlvl\_en}}$	PHY	1	- [a]	DFI clock cycles	Read training enable time. Specifies the minimum number of DFI clock cycles from the assertion of the **dfi_rdlvl_en** or **dfi_rdlvl_gate_en** signal to the first read (DDR4 or DDR3) or mode register read (LPDDR3 or LPDDR2) command.
$\mathbf{t_{rdlvl\_max}}$	MC	1	- [a]	DFI clock cycles	Read training maximum time. Specifies the maximum number of DFI clock cycles that the MC waits for a response (**dfi_rdlvl_resp**) to a read training enable signal (**dfi_rdlvl_en** or **dfi_rdlvl_gate_en**).
$\mathbf{t_{rdlvl\_resp}}$	MC	1	- [a]	DFI clock cycles	Read training response. Specifies the maximum number of DFI clock cycles after a read training request is asserted (**dfi_rdlvl_req** or **dfi_rdlvl_gate_req**) to when the MC responds with a read training enable signal (**dfi_rdlvl_en** or **dfi_rdlvl_gate_en**). If there are no read or write transactions occurring on the interface, exceeding the response time is not an error condition. However, the MC must execute the requested training operation prior to restarting traffic.
$\mathbf{t_{rdlvl\_rr}}$	PHY	1	- [a]	DFI clock cycles	Read training command-to-command delay. Specifies the minimum number of DFI clock cycles after the assertion of a read command to the next read command. For DDR4 and DDR3 DRAMs, references a read data command. For LPDDR3 and LPDDR2 DRAMs, references a mode register read command.
$\mathbf{t_{wrlvl\_en}}$	PHY	1	- [a]	DFI clock cycles	Write leveling enable time. Specifies the minimum number of DFI clock cycles from the assertion of the **dfi_wrlvl_en** signal to the first assertion of the **dfi_wrlvl_strobe** signal.
$\mathbf{t_{wrlvl\_max}}$	MC	1	- [a]	DFI clock cycles	Write leveling maximum time. Specifies the maximum number of DFI clock cycles that the MC waits for a response (**dfi_wrlvl_resp**) to a write leveling enable signal (**dfi_wrlvl_en**).

TABLE 17. *Training Interface Timing Parameters (Continued)*

Parameter	Defined By	Min	Max	Unit	Description
t_{wrlvl_resp}	MC	1	-[a]	DFI clock cycles	Write leveling response. Specifies the maximum number of DFI clock cycles after a write leveling request is asserted (**dfi_wrlvl_req**) to when the MC responds with a write leveling enable signal (**dfi_wrlvl_en**). If there are no read or write transactions occurring on the interface, exceeding the response time is not an error condition. However, the MC must execute the requested training operation prior to restarting traffic.
t_{wrlvl_ww}	PHY	1	-[a]	DFI clock cycles	Write leveling write-to-write delay. Specifies the minimum number of DFI clock cycles after the assertion of the **dfi_wrlvl_strobe** signal to the next assertion of the **dfi_wrlvl_strobe** signal.

[a] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

TABLE 18. *DFI Training Programmable Parameters*

Parameter	Defined by	Description
phy_{calvl_en}	PHY	PHY CA Leveling Mode. Defines the CA training operating mode of the PHY. • 0: DFI CA Training disabled • 1: DFI CA Training enabled
phy_{rdlvl_en}	PHY	Specifies whether the PHY is supporting read data eye training on the DFI bus. • ‘b0 = Disabled • ‘b1 = Enabled
$phy_{rdlvl\_gate\_en}$	PHY	Specifies whether the PHY is supporting gate training on the DFI bus. • ‘b0 = Disabled • ‘b1 = Enabled
phy_{wrlvl_en}	PHY	Specifies whether the PHY is supporting write leveling on the DFI bus. • ‘b0 = Disabled • ‘b1 = Enabled

3.6.4 dfi_lvl_pattern Encoding

To synchronize the MC and the PHY with the defined training sequences, and the specific sequence required for each training operation, the MC transmits the **dfi_lvl_pattern** signal across the DFI bus to the PHY.

The **dfi_lvl_pattern** signal must be valid when the enable signal is asserted for gate training or read data eye training. Similar to the enable signal, the **dfi_lvl_pattern** signal may transition when training completes.

For more information on **dfi_lvl_pattern** signal encoding, refer to Table 25, “DDR4 Encoding of dfi_lvl_pattern,” on page 125.

3.6.5 Periodic Training Flag

The **dfi_lvl_periodic** control signal is a general purpose training signal that is relevant when the PHY can execute a long or short training sequence as needed.

The **dfi_lvl_periodic** signal defines the type of training required and determines if a full training sequence is required. The MC sets a single bit on the **dfi_lvl_periodic** signal to indicate to the PHY whether the system may require a longer training sequence (when initializing or re-starting from the self refresh state), or whether the system only needs a short training (when in an operating state and simply tuning the delays).

The **dfi_lvl_periodic** signal is utilized with all training interfaces and all DRAM types that utilize training. The encoding of the **dfi_lvl_periodic** signal is defined in Table 16, “Training Interface Signals,” on page 49.

3.6.6 PHY-Initiated Training in DFI Training Mode

The DFI Specification mandates a response within the period of time defined by $\mathbf{t_{rdlvl\_resp}}$ and $\mathbf{t_{wrlvl\_resp}}$. When the MC is not driving data traffic and training is undesirable (e.g., DRAM is in the self refresh state), the training request should remain asserted without MC acknowledgement until the MC response time has been reached. Once the timer has timed out, the PHY has the option to de-assert **dfi_rdlvl_req/dfi_rdlvl_gate_req/dfi_wrlvl_req** or leave the request asserted; the MC must initiate the requested training prior to restarting data traffic.

3.6.7 PHY-Requested Training in Non-DFI Training Mode

In non-DFI training mode, the PHY performs PHY-requested training by taking control of the DRAM bus with the DRAM in the idle state. The PHY requests the bus, and the MC puts the DRAM into the idle state with all pages closed and grants the PHY control of the bus. The DFI bus must remain in the idle state while the PHY has control.

PHY-requested training in non-DFI training mode makes per-chip-select training requests utilizing the **dfi_phylvl_req_cs_n** and **dfi_phylvl_ack_cs_n** signals and the $\mathbf{t_{phylvl}}$ and $\mathbf{t_{phylvl\_resp}}$ timing parameters.

The timing parameters associated with the training interface are listed in Table 17, “Training Interface Timing Parameters,” on page 53.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

3.7 Low Power Control Interface

The Low Power Control interface handles transmission of signals to enter and exit an idle state; the interface includes signals and timing parameters. Low Power Control is an optional feature for both the MC and the PHY unless the system requires a low power interface. It may be advantageous to place the PHY in a low power state when the MC has knowledge that the memory subsystem will remain in the idle state for a period of time. Depending on the state of the system, the MC communicates state information to the PHY allowing the PHY to enter the appropriate power saving state.

The Low Power Control interface consists of signals that inform the PHY of a low power mode opportunity, as well as how quickly the MC will require the PHY to resume normal operation, and timing parameters. Table 19, “Low Power

Control Interface Signals” describes the signals used in the low power control interface: **dfi_lp_ctrl_req** (low power opportunity control request), **dfi_lp_data_req** (low power opportunity data request), **dfi_lp_ack** (low power acknowledge) and **dfi_lp_wakeup** (low power wakeup time).

Once a low power request is asserted, the other low power request cannot be asserted until either the **dfi_lp_ack** signal is asserted or the low power request is aborted and a new low power request is generated. Once asserted, a low power request cannot be de-asserted unless the **dfi_lp_ack** is not asserted within t_{lp_resp} or when exiting the low power handshake; when exiting, if both low power requests are asserted, both requests must be de-asserted simultaneously.

Table 20, “Low Power Control Timing Parameters,” on page 59 describes the timing parameters: t_{lp_resp} and t_{lp_wakeup}.

More information on the low power control interface is provided in Section 4.11.7, “PHY-Requested Training Sequence,” on page 127. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18

The signals associated with the low power interface are listed in Table 19

TABLE 19. *Low Power Control Interface Signals*

Signal	From	Width	Default	Description
dfi_lp_ack	PHY	1 bit	0x0	Low power acknowledge. The **dfi_lp_ack** signal is asserted to acknowledge the MC low power opportunity request. The PHY is not required to acknowledge this request. If the PHY acknowledges the request, the **dfi_lp_ack** signal must be asserted within t_{lp_resp} cycles after the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal assertion. Once asserted, this signal remains asserted until the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal de-asserts. The signal de-asserts within t_{lp_wakeup} cycles after the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal de-asserts, indicating that the PHY is able to resume normal operation. If the PHY ignores the request, the **dfi_lp_ack** signal must remain de-asserted for the remainder of the low power mode opportunity. The **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is asserted for at least t_{lp_resp} cycles.
dfi_lp_ctrl_req	MC	1 bit	0x0	Low power opportunity control request. The **dfi_lp_ctrl_req** signal is used by the MC to inform the PHY of an opportunity to switch to a low power mode. When asserted, the MC indicates that no more commands will be sent on the Control Interface. The MC must assert a constant value on the **dfi_lp_wakeup** signal while this signal is asserted before the request is acknowledged by the PHY through the assertion of the **dfi_lp_ack** signal or until t_{lp_resp} cycles have elapsed. The MC may increase the value of the **dfi_lp_wakeup** signal if both the **dfi_lp_ctrl_req** and **dfi_lp_ack** signals are asserted. Following the de-assertion of the **dfi_lp_ctrl_req** signal, the PHY has t_{lp_wakeup} cycles to resume normal operation and de-assert the **dfi_lp_ack** signal.

TABLE 19. *Low Power Control Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_lp_data_req	MC	1 bit	0x0	Low power opportunity data request. The **dfi_lp_data_req** signal is used by the MC to inform the PHY of an opportunity to switch to a low power mode. When asserted, the MC indicates that no more commands will be sent on the Data Interface. The MC must assert a constant value on the **dfi_lp_wakeup** signal while this signal is asserted before the request is acknowledged by the PHY through the assertion of the **dfi_lp_ack** signal or until $\mathbf{t_{lp\_resp}}$ cycles have elapsed. The MC may increase the value of the **dfi_lp_wakeup** signal if both the **dfi_lp_data_req** and **dfi_lp_ack** signals are asserted. Following the de-assertion of the **dfi_lp_data_req** signal, the PHY has $\mathbf{t_{lp\_wakeup}}$ cycles to resume normal operation and de-assert the **dfi_lp_ack** signal.

TABLE 19. *Low Power Control Interface Signals (Continued)*

Signal	From	Width	Default	Description
dfi_lp_wakeup	MC	4 bits	-[a]	Low power wakeup time. The **dfi_lp_wakeup** signal indicates which one of the 16 wakeup times the MC is requesting for the PHY. The signal is only valid when the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is asserted. The **dfi_lp_wakeup** signal must remain constant until the **dfi_lp_ack** signal is asserted. Once the request has been acknowledged, the MC may increase the **dfi_lp_wakeup** signal, permitting the PHY to enter a lower power state. The PHY is not required to change power states in response to the wakeup time change. The MC may not decrease this value once the request has been acknowledged. The value of the **dfi_lp_wakeup** signal at the time that the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is de-asserted sets the $\mathbf{t_{lp\_wakeup}}$ time. • ‘b0000 = $\mathbf{t_{lp\_wakeup}}$ is 16 cycles • ‘b0001 = $\mathbf{t_{lp\_wakeup}}$ is 32 cycles • ‘b0010 = $\mathbf{t_{lp\_wakeup}}$ is 64 cycles • ‘b0011 = $\mathbf{t_{lp\_wakeup}}$ is 128 cycles • ‘b0100 = $\mathbf{t_{lp\_wakeup}}$ is 256 cycles • ‘b0101 = $\mathbf{t_{lp\_wakeup}}$ is 512 cycles • ‘b0110 = $\mathbf{t_{lp\_wakeup}}$ is 1024 cycles • ‘b0111 = $\mathbf{t_{lp\_wakeup}}$ is 2048 cycles • ‘b1000 = $\mathbf{t_{lp\_wakeup}}$ is 4096 cycles • ‘b1001 = $\mathbf{t_{lp\_wakeup}}$ is 8192 cycles • ‘b1010 = $\mathbf{t_{lp\_wakeup}}$ is 16384 cycles • ‘b1011 = $\mathbf{t_{lp\_wakeup}}$ is 32768 cycles • ‘b1100 = $\mathbf{t_{lp\_wakeup}}$ is 65536 cycles • ‘b1101 = $\mathbf{t_{lp\_wakeup}}$ is 131072 cycles • ‘b1110 = $\mathbf{t_{lp\_wakeup}}$ is 262144 cycles • ‘b1111 = $\mathbf{t_{lp\_wakeup}}$ is unlimited

[a] This signal is not meaningful during initialization; no default value is required.

The timing parameters associated with the low power interface are listed in Table 20.

TABLE 20. *Low Power Control Timing Parameters*

Parameter	Defined By	Min	Max	Unit	Description
$\mathbf{t_{lp\_resp}}$	MC	1[a]	7	DFI clock cycles	Specifies the maximum number of DFI clock cycles after the assertion of the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal to the assertion of the **dfi_lp_ack** signal.

TABLE 20. *Low Power Control Timing Parameters (Continued)*

Parameter	Defined By	Min	Max	Unit	Description
t_{lp_wakeup}	MC	16	- [b]	DFI clock cycles	Specifies the target maximum number of DFI clock cycles that the **dfi_lp_ack** signal may remain asserted after the de-assertion of the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal. The **dfi_lp_ack** signal may de-assert at any cycle after the de-assertion of the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal. Exceeding the maximum is not considered an error condition.

[a] It is recommended to fix this timing parameter at 7 cycles.

[b] The minimum supportable value is 0; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

3.8 Error Interface

The error interface handles the transmission of error information; the interface includes signals and timing parameters. The error interface is an optional feature for both the MC and the PHY.

In a DDR memory sub-system, the PHY may detect various error conditions including DRAM errors (e.g., ECC errors) or PHY-specific errors (e.g., loss of DLL lock or a read DQS error). In error-condition scenarios, it may be desirable to communicate the error information from the PHY to the MC for error reporting and other possible error responses. The MC is not required to take any action other than reporting errors.

The error interface defines two signals and a timing parameter. The PHY may support the **dfi_error** signal with or without **dfi_error_info**. The PHY may use a subset of the **dfi_error_info** signal; un-driven signals must be tied LOW at the MC.

The error signals are not phased for Frequency Ratio. For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

The signals associated with the error interface are listed in Table 21.

TABLE 21. *Error Signals*

Signal	From	Width	Default	Description
dfi_error	PHY	DFI Error Width	0	DFI Error. Indicates that the PHY has detected an error condition.
dfi_error_info	PHY	DFI Error Width * x 4	0	DFI Error Info. Provides additional information about the source of the error detected. Only considered valid when **dfi_error** is asserted.

Typically, the width of the **dfi_error** signal would be equal to 1-bit per data slice plus 1 bit for control. The PHY may implement **dfi_error** as a single bit or any other width not exceeding the sum of the data slices + 1 bit for control. The MC should accept 1 bit per instance as defined by the sum of data slices plus 1 bit for control.

The **dfi_error_info** signal is 4-bits per instance. The number of instances should be the same for the **dfi_error** and **dfi_error_info** signals. The **dfi_error_info** signal is defined for some error types in this specification and may be further defined as design-specific errors by the PHY.

The error interface defines a maximum timing parameter, **t_{error_resp}**. The timing parameter defines the maximum delay between receiving a command or data, and detection of an error associated with that command or data.

The timing parameter associated with the error interface is listed in Table 22.

TABLE 22. *Error Timing Parameter*

Parameter	Defined By	Min	Max	Unit	Description
t_{error_resp}	PHY	1	[a]	DFI clock cycles	Specifies the maximum number of DFI clock cycles that may occur from the DFI bus transaction(s) which are known to be affected by the error condition and the assertion of the **dfi_error** signal.

[a] The minimum supportable value is 1; the DFI does not specify a maximum value. The range of values supported is implementation-specific.

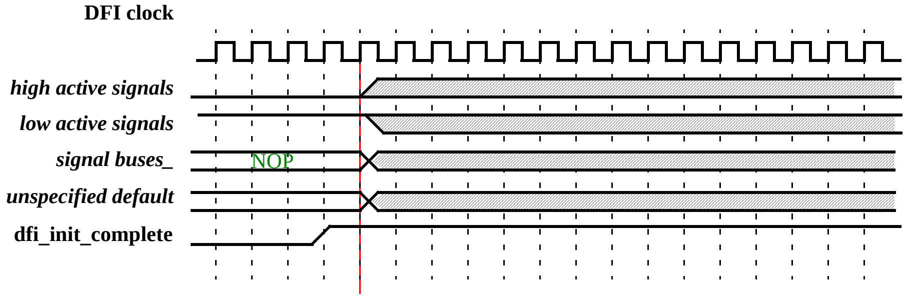
4.0 Functional Use

While some of the diagrams illustrate DFI PHY signals, these signals are only an interpretive example of internal PHY signals, they are not signals on the DFI.

4.1 Initialization

The DFI signals that communicate commands or status, shown in Figure 3, “Dependency on dfi_init_complete”, must maintain their default value until the **dfi_init_complete** signal is asserted.

FIGURE 3. *Dependency on dfi_init_complete*



The default value for each signal is listed in the corresponding interface table. For example, the default for control signals are listed in the default column of Table 4, “Control Signals,” on page 27.

1. High active signals have a default value of 0 (e.g., **dfi_odt, dfi_wrdata_en**).
2. Low active signals have a default value of 1 (e.g., **dfi_cs_n, dfi_we_n**).
3. Signal buses have an unspecified default value (e.g., **dfi_address**[1], **dfi_cid)**.
4. State-specific signals have state-specific values (e.g., **dfi_dram_clk_disable, dfi_parity_in**).

[1] The **dfi_address** signal does not have a default value in most cases. However, for LPDDR3 and LPDDR2 DRAMs, the **dfi_address** bus must drive a NOP command until the **dfi_init_complete** signal is asserted.

The **dfi_init_start** signal is used for indicating that the MC is driving valid values on the DFI signals and that two optional signals of the status interface (**dfi_data_byte_disable** and **dfi_freq_ratio**) are valid. The **dfi_data_byte_disable** signal informs the PHY if the MC is disabling certain byte lanes from use during data transfers, and the **dfi_freq_ratio** signal identifies the MC:PHY frequency ratio. The PHY may use the **dfi_init_start** signal assertion to know that these status signals are valid.

Figure 4, “System Setting Signals - dfi_init_start Asserts Before dfi_init_complete,” on page 63 shows that during initialization, if data byte disabling or the frequency ratio protocol are implemented, the **dfi_init_start** signal should only be asserted after the **dfi_data_byte_disable** and/or the **dfi_freq_ratio** signals have been defined. If the PHY requires this information for proper initialization, the PHY should wait for the **dfi_init_start** assertion before asserting the

dfi_init_complete signal. When both **dfi_init_start** and **dfi_init_complete** signals are asserted for at least one DFI clock cycle, the MC can de-assert the **dfi_init_start** signal or continue to hold it asserted.

FIGURE 4. *System Setting Signals - **dfi_init_start** Asserts Before **dfi_init_complete***

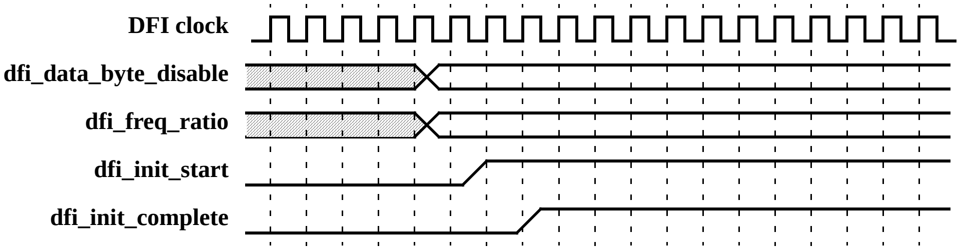
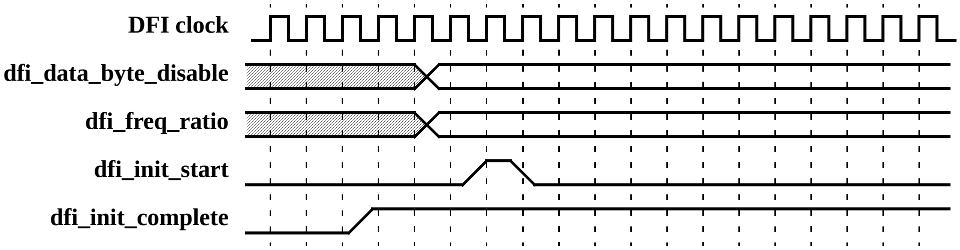


Figure 5, “System Setting Signals - dfi_init_start Asserts After dfi_init_complete” shows that the **dfi_init_complete** signal may be asserted before the assertion of the **dfi_init_start** signal If neither the data byte disabling nor the frequency ratio protocol are implemented, or the PHY does not require this information for proper initialization, the PHY may assert the **dfi_init_complete** signal without regard to the assertion of the **dfi_init_start** signal. Note that the **dfi_init_start** signal must be asserted during initialization, even if the PHY is not requiring this information. When both **dfi_init_start** and **dfi_init_complete** signals are asserted for at least one DFI clock cycle, the MC can de-assert the **dfi_init_start** signal or continue to hold it asserted.

FIGURE 5. *System Setting Signals - **dfi_init_start** Asserts After **dfi_init_complete***



The DFI specification does not impose or dictate a reset sequence or any type of signal training for either the PHY or the MC prior to DFI signal assertion. However, the assertion of the **dfi_init_complete** signal signifies that the PHY is ready to respond to any assertions on the DFI by the MC and ensures appropriate responses on the DFI. The PHY must guarantee the integrity of the address and control interface to the DRAMs prior to asserting the **dfi_init_complete** signal.

For LPDDR3 and LPDDR2 DRAMs, the **dfi_address** bus must drive a NOP command until the **dfi_init_complete** signal is asserted and the signals **dfi_act_n, dfi_bank**, **dfi_bg, dfi_cid, dfi_cas_n**, **dfi_ras_n** and **dfi_we_n** are unused and must remain at a constant value when the DFI bus is being used.

Some of the training interface signals must remain at default until after the assertion of the **dfi_init_complete** signal. No default value must be maintained for the following signals:**dfi_act_n, dfi_bank**, **dfi_bg, dfi_wrdata**, **dfi_wrdata_mask**,

dfi_rddata, **dfi_phyupd_type**, **dfi_rdlvl_resp**, **dfi_wrlvl_resp**, and **dfi_lp_wakeup**. The **dfi_address** signal also has no default value except for LPDDR3 and LPDDR2 DRAMs.

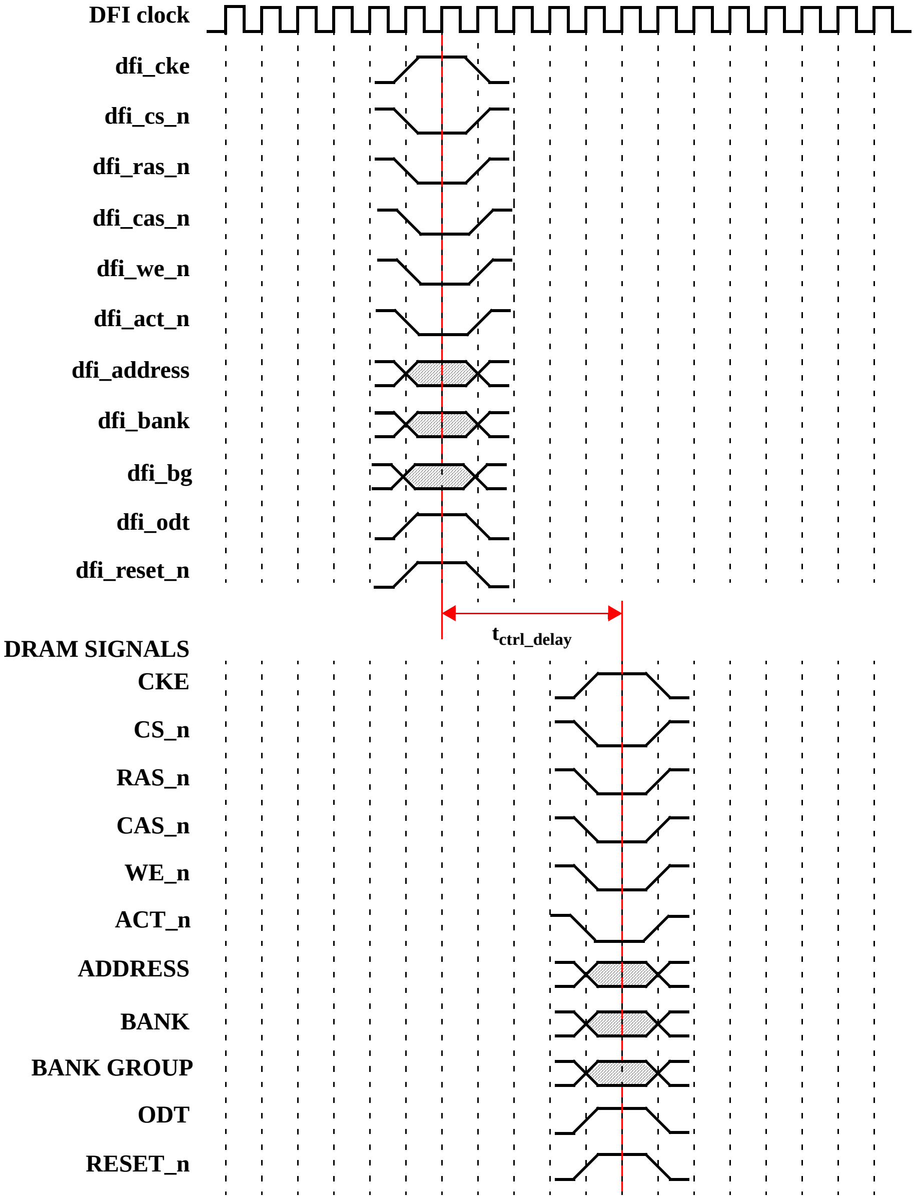
4.2 Control Signals

The DFI control signals consist of the Command Address (CA) signals **dfi_act_n, dfi_address**, **dfi_bank**, **dfi_bg, dfi_cas_n**, **dfi_ras_n** and **dfi_we_n,** and **dfi_cid, dfi_cke**, **dfi_cs_n**, **dfi_odt, and dfi_reset_n.** The DFI control signals correlate to the DRAM control signals, and are driven according to the timing parameters $\mathbf{t_{ctrl\_delay}}$ and $\mathbf{t_{cmd\_lat.}}$

For more information on control signals and parameters, refer to Section 3.1, “Control Interface”.

Figure 6, “DFI Control Interface Signal Relationships,” on page 65 shows that the control signals are driven to the DRAMs and the DFI relationship of the control signals is expected to be maintained at the PHY-DRAM boundary so any delays should be consistent across all signals and defined through the timing parameter $\mathbf{t_{ctrl\_delay}}$. All control signals are illustrated but might not all be required, depending on system requirements. Refer to Table 2, “DFI Signal Requirements,” on page 18 to determine the signals that are relevant for a specific system.

FIGURE 6. *DFI Control Interface Signal Relationships*



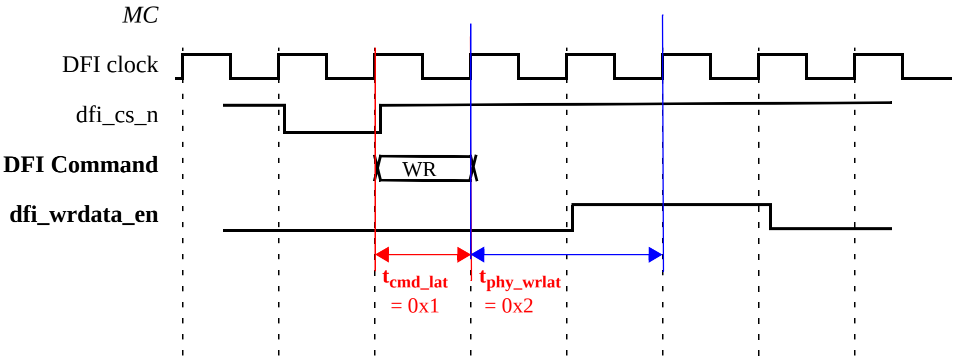
NOTE: The system might not use all of the pins on the DRAM interface, such as additional bank and chip selects. If these signals are never used in a system, they are not required on the DFI. However, if multiple memory sub-systems are supported, the union of the required signals must exist on DFI. In this case, signals unused for a specific topology must be driven through the DFI and must not be left floating.

Based on current DRAM settings, the MC defines $\mathbf{t_{cmd\_lat}}$ with the parameter value defining when the CA bus is driven for each command. The timing of the CA bus assertion is relative to the assertion of **dfi_cs_n.**

Figure 7, "Example of tcmd_lat (tcmd_lat=1, tphy_wrlat=2)" illustrates how the $\mathbf{t_{cmd\_lat}}$ parameter relates the DFI command to the DFI chip select. Furthermore, Figure 7 shows how DFI timing parameters, such as $\mathbf{t_{phy\_wrlat,}}$ relate to the DFI command when $\mathbf{t_{cmd\_lat}}$ is defined as a non-zero value.

For more information on $\mathbf{t_{cmd\_lat}}$, refer to Table 5, "Control Timing Parameters," on page 29.

FIGURE 7. *Example of t_{cmd_lat} (t_{cmd_lat}=1, t_{phy_wrlat}=2)*



4.3 Data Bus Inversion

DBI is an optional DFI feature used with write and read data transmissions to generate write DBI data and invert both write and read data for DBI as required. When DBI is enabled, the $\mathbf{phy_{dbi\_mode}}$ parameter is applicable.

If $\mathbf{phy_{dbi\_mode}}$ = 0, the MC controls the DBI functionality and the **dfi_rddata_dbi_n** signal is required.
If $\mathbf{phy_{dbi\_mode}}$ = 1, the PHY performs DBI generation and data inversion. If DBI is required in a system, either the MC or the PHY can generate the DBI output to DRAM and the output must be used to selectively invert data for write commands.

The PHY defines the $\mathbf{phy_{dbi\_mode}}$ parameter value to determine how DBI is handled, as defined in Table 8, "Write Data Programmable Parameters," on page 33.

If the MC supports DBI on DFI, the MC must support both settings of the $\mathbf{phy_{dbi\_mode}}$ parameter; the MC must be able to generate DBI and invert the write data and read data as needed for DBI, and interface with a PHY that generates and handles the data inversion for DBI. The PHY can optionally support either setting of the $\mathbf{phy_{dbi\_mode}}$ parameter; the PHY can optionally generate DBI and invert the write data and read data as required. If the PHY does not generate DBI and invert the corresponding write/read data, the PHY must be able to interface to an MC that has DBI support. When both CRC and DBI are enabled in a system, special care needs to be taken regarding where CRC and DBI are performed in order to operate correctly.

When **phy**$_{\textbf{dbi\_mode}}$ = 0, the PHY transfers the read DBI data on **dfi_rddata_dbi** coincident with **dfi_rddata**. The MC transfers the write DBI data on **dfi_wrdata_mask** coincident with **dfi_wrdata**.

4.4 Write Transactions

The write data transaction handles the transmission of write data across the DFI bus.

The DFI write transaction includes the signals for write data (**dfi_wrdata**), write data mask (**dfi_wrdata_mask**), write data enable (**dfi_wrdata_en**), and the optional write data chip select (**dfi_wrdata_cs_n)**, and the associated timing parameters **t**$_{\textbf{phy\_wrlat}}$ and **t**$_{\textbf{phy\_wrdata}}$, and programmable parameters **phy**$_{\textbf{crc\_mode}}$ and **phy**$_{\textbf{dbi\_mode}}$.

The **dfi_wrdata_en** signal must correlate with the number of data transfers executed on the DRAM bus; one continuous assertion of the **dfi_wrdata_en** signal may encompass data for multiple write commands.

If write data chip select is enable, the **dfi_wrdata_cs_n** signal provides the target data path chip select value to each of the PHY data slices. For more information on these signals, refer to Section 3.2, “Write Data Interface,” on page 29.

4.4.1 Write Transaction Sequence

The sequence for DFI write transactions is listed below; the effect of using the optional write data chip select, CRC, or DBI is shown within brackets.

1. The write command is issued.
2. **t**$_{\textbf{phy\_wrlat}}$ cycles elapse (**t**$_{\textbf{phy\_wrlat}}$ can be zero).

   [If write data chip select is enabled, **t**$_{\textbf{phy\_wrcslat}}$ cycles elapse.]

   The **t**$_{\textbf{phy\_wrlat}}$ parameter defines the number of cycles between when the write command is driven on the DFI to assertion of the **dfi_wrdata_en** signal. The **t**$_{\textbf{phy\_wrlat}}$ parameter is PHY-defined but may be specified in terms of other fixed system values.

   The write timing parameters (**t**$_{\textbf{phy\_wrdata}}$ and **t**$_{\textbf{phy\_wrlat}}$) must be held constant while commands are being executed on the DFI bus; however, if necessary, the write timing parameter values may be changed when the bus is in the idle state. The **t**$_{\textbf{phy\_wrdata}}$ and **t**$_{\textbf{phy\_wrlat}}$ timing parameters work together to define the number of cycles from the assertion of a write command on the DFI control interface to when write data is driven on the DFI bus and must be consistent with the write latency timing that correlates to the DRAM timing.

   [If chip select is enabled, the PHY defines the **t**$_{\textbf{phy\_wrcslat}}$ timing parameter to specify the desired alignment of the command to the **dfi_wrdata_cs_n** signal; the PHY defines the **t**$_{\textbf{phy\_wrcsgap}}$ timing parameter to specify the additional delay it requires between two consecutive commands that are targeting different chip selects. The **t**$_{\textbf{phy\_wrcslat}}$ timing parameter must be held constant while commands are being executed on the DFI bus; however, if necessary, the **t**$_{\textbf{phy\_wrcslat}}$ parameter value may be changed when the bus is in the idle state. The PHY may require the MC to add delay beyond other system timing requirements to account for PHY-specific adjustments transitioning between data path chip selects.]

   [The gap timing requirement may only be applicable to certain chip-select-to-chip-select transitions and not be applicable to other data path chip select transitions where the PHY is not required to make an internal adjustment on the transition; this gap timing requirement is system-specific. For example, a system may not require additional delay on transitions between chip select 0 and chip select 1, but may require additional delay when transitioning from chip select 0 to chip select 2. Accordingly, the interface does not require the gap timing to be applied to every chip select transition.]

3. [If chip select is enabled and the MC supports chip select, the MC drives **dfi_wrdata_cs_n** a minimum of the DFI data transfer width ($\mathbf{dfi}_{\mathbf{rw\_length}}$) plus the gap timing ($\mathbf{t}_{\mathbf{phy\_wrcsgap}}$). The minimum time the chip select is guaranteed to remain driven to the PHY relative to the write command is defined by $\mathbf{t}_{\mathbf{phy\_wrcslat}} + \mathbf{dfi}_{\mathbf{rw\_length}} + \mathbf{t}_{\mathbf{phy\_wrcsgap}}$.]

   The maximum delay that can be achieved between the assertion of a new chip select value on **dfi_wrdata_cs_n** and the corresponding **dfi_wrdata_en** is limited to the maximum time the PHY has from changing the target chip select to receiving the write data transfer ($\mathbf{t}_{\mathbf{phy\_wrlat}} - \mathbf{t}_{\mathbf{phy\_wrcslat}}$).

   The PHY must define the $\mathbf{t}_{\mathbf{phy\_wrcslat}}$ and $\mathbf{t}_{\mathbf{phy\_wrcsgap}}$ timing parameters to allocate the time between transactions to different chip selects necessary for PHY-specific adjustments.

   If the MC does not support chip select but the PHY does support it, the PHY inputs should be tied-off disabled.]

4. For non-contiguous write commands, the **dfi_wrdata_en** signal is asserted on the DFI after $\mathbf{t}_{\mathbf{phy\_wrlat}}$ is met and remains asserted for the number of cycles required to complete the write data transfer sent on the DFI control interface; $\mathbf{t}_{\mathbf{phy\_wrlat}}$ can be zero.

   [If CRC is enabled, the MC extends the **dfi_wrdata_en** signal to accommodate the extended DRAM burst length and the signal is asserted for an odd number of cycles per burst.]

5. For contiguous write commands, the **dfi_wrdata_en** signal is asserted after $\mathbf{t}_{\mathbf{phy\_wrlat}}$ is met and remains asserted for the entire length of the data stream; $\mathbf{t}_{\mathbf{phy\_wrlat}}$ can be zero. [If CRC is enabled, the MC extends the **dfi_wrdata_en** signal to accommodate the extended DRAM burst length and the signal may be asserted for an odd number of cycles per burst.]

6. $\mathbf{t}_{\mathbf{phy\_wrdata}}$ cycles elapse.

7. The associated write data (**dfi_wrdata**) and masking (**dfi_wrdata_mask**) signals are sent.

   [If CRC is enabled, the MC utilizes the **dfi_wrdata** bus to send CRC data to the PHY; the MC utilizes the **dfi_wrdata_pN** outputs for frequency ratio systems.]

   [If DBI is enabled, **dfi_wrdata_mask** transfers the write data inversion information instead of the write data mask.]

The MC must always drive **dfi_wrdata** and associated signals with the correct timing relative to the write command as defined by the timing parameters $\mathbf{t}_{\mathbf{phy\_wrdata}}$ and $\mathbf{t}_{\mathbf{phy\_wrlat}}$.

The $\mathbf{t}_{\mathbf{phy\_wrdata}}$ parameter defines the timing requirements between the assertion of the **dfi_wrdata_en** signal assumed and when the write data is driven on the **dfi_wrdata** signal. The exact value of the $\mathbf{t}_{\mathbf{phy\_wrdata}}$ parameter for a particular application is determined by how many cycles the PHY must receive the **dfi_wrdata_en** signal prior to receiving the **dfi_wrdata** signal.

If the PHY requires notification of pending write data sooner than 1 cycle, the $\mathbf{t}_{\mathbf{phy\_wrdata}}$ parameter may be increased. However, setting $\mathbf{t}_{\mathbf{phy\_wrdata}}$ to a value greater than 1 may restrict the minimum write latency supported by the interface. The DFI specification does not dictate a value for the $\mathbf{t}_{\mathbf{phy\_wrdata}}$ parameter.

8. The **dfi_wrdata_en** signal de-asserts t_{phy_wrdata} cycles before the last valid data is transferred on the **dfi_wrdata** bus.
9. $t_{phy\_wrdata\_delay}$ cycles elapse.The DFI bus enters the idle state.

   The idle state timing parameter defines the number of DFI clocks from **dfi_wrdata_en** to the completion of the write data transfer on the DRAM bus. The MC drives the next value (any valid chip select or inactive).

Seven situations showing system behavior with two write transactions are presented in Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, and Figure 14. System behavior with three write transactions using dfi_wrdata_cs_n is shown in Figure 15, “Write Commands Utilizing dfi_wrdata_cs_n (DRAM Burst of 4: tphy_wrlat=3, tphy_wrdata=4, tphy_wrcslata=2, tphy_wrcsgap=1),” on page 74.

Figure 8 shows back-to-back writes for a system with a t_{phy_wrlat} of zero and a t_{phy_wrdata} of one. The **dfi_wrdata_en** signal is asserted with the write command for this situation, and is asserted for two cycles per command to inform the DFI that two cycles of DFI data are sent for each write command. The timing parameters and the timing of the write commands allow the **dfi_wrdata_en** signal and the **dfi_wrdata** stream to be sent contiguously.

FIGURE 8. *Back-to-Back Writes (DRAM Burst of 4:* t_{phy_wrlat}=0, t_{phy_wrdata}=1*)*

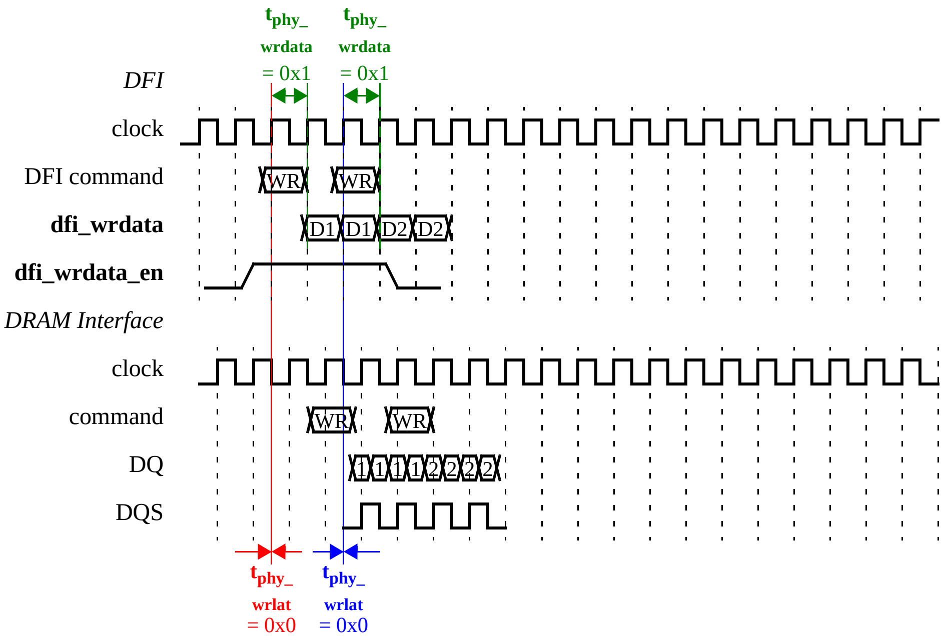


Figure 9, “Back-to-Back Interrupted Contiguous Writes (DRAM Burst of 8: tphy_wrlat=3, tphy_wrdata=2),” on page 70 shows an interrupted write command. The **dfi_wrdata_en** signal should be asserted for 4 cycles for each of these write transactions. However, since the first write is interrupted, the **dfi_wrdata_en** signal is asserted for a portion of the first transaction and the complete second transaction. The **dfi_wrdata_en** signal will not de-assert between write commands, and the **dfi_wrdata** stream will be sent contiguously for a portion of the first command and the complete second command.

FIGURE 9. *Back-to-Back Interrupted Contiguous Writes (DRAM Burst of 8:* $\mathbf{t_{phy\_wrlat}}$=3, $\mathbf{t_{phy\_wrdata}}$=2*)*

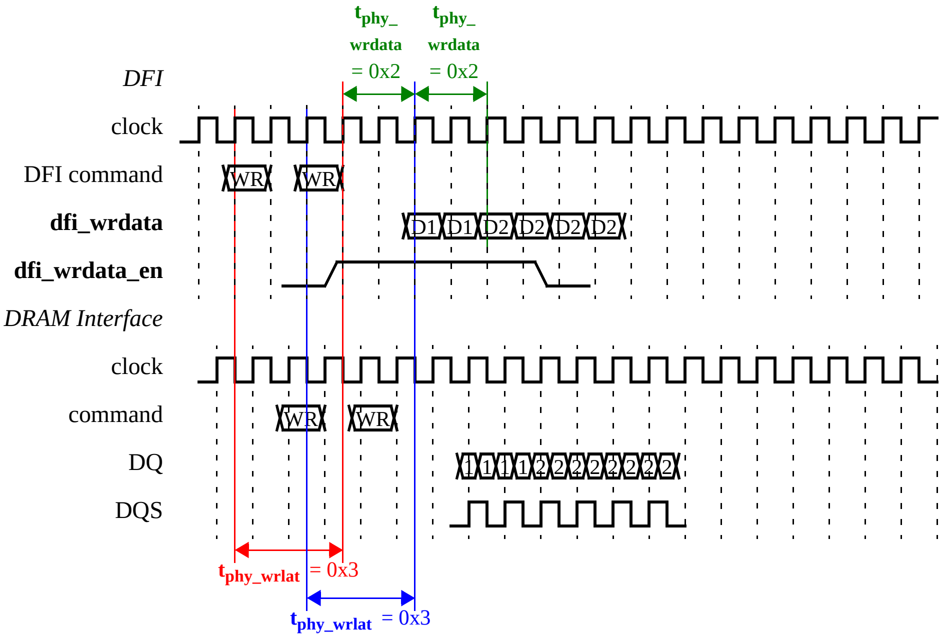


Figure 10 shows back-to-back burst-of-8 writes. The **dfi_wrdata_en** signal must be asserted for 4 cycles for each of these write transactions.

FIGURE 10. *Back-to-Back Writes (DRAM Burst of 8:* $\mathbf{t}_{\mathbf{phy\_wrlat}}$*=4,* $\mathbf{t}_{\mathbf{phy\_wrdata}}$*=4)*

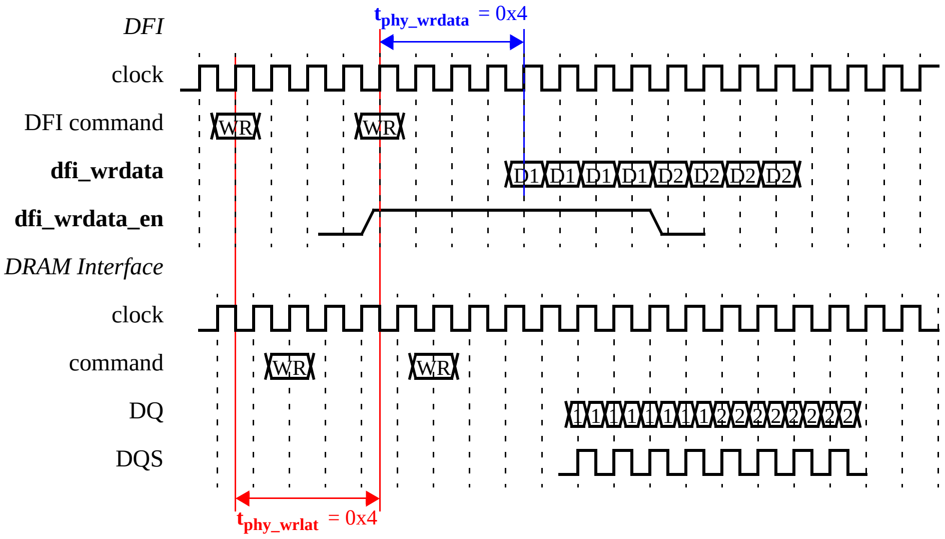


Figure 11, Figure 12, Figure 13, and Figure 14 also show two complete write commands, with different $\mathbf{t}_{\mathbf{phy\_wrlat}}$ and $\mathbf{t}_{\mathbf{phy\_wrdata}}$ timing parameters and for different DRAM types. The **dfi_wrdata_en** signal is asserted for two cycles for each write transaction. The $\mathbf{t_{phy\_wrlat}}$ timing and the timing between the write commands causes the **dfi_wrdata_en** signal to be de-asserted between commands. As a result, the **dfi_wrdata** stream is non-contiguous.

FIGURE 11. *Two Independent Writes (DRAM Burst of 4:* $\mathbf{t_{phy\_wrlat}}$=0, $\mathbf{t_{phy\_wrdata}}$=1*)*

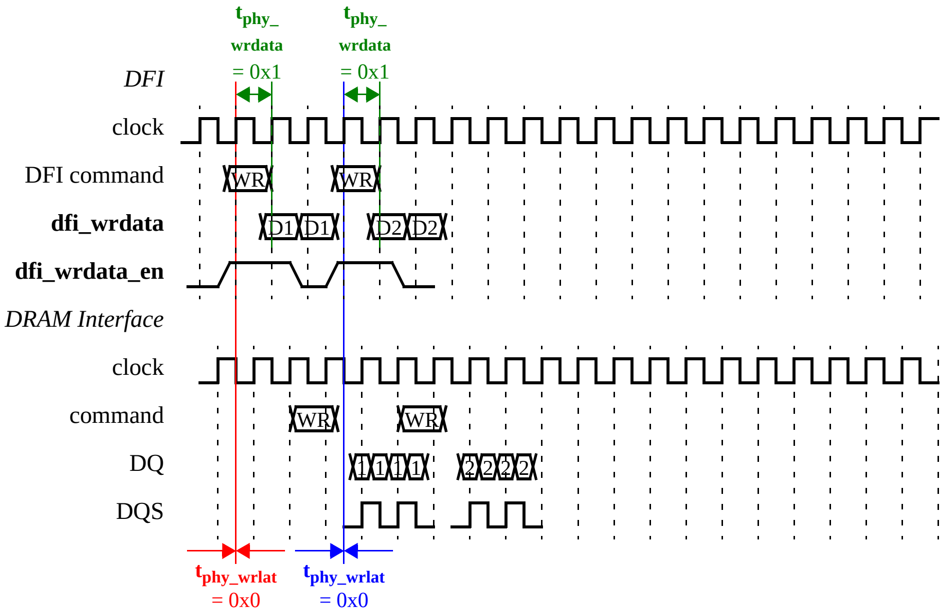


FIGURE 12. *Two Independent Writes (DRAM Burst of 4:* $\mathbf{t_{phy\_wrlat}}=3$, $\mathbf{t_{phy\_wrdata}}=1$*)*

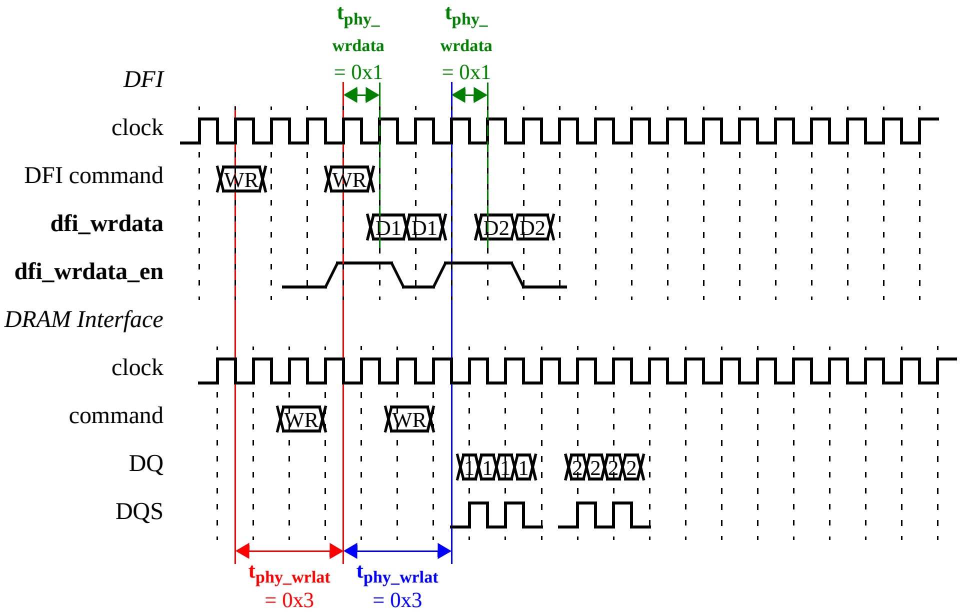


FIGURE 13. *Two Independent Writes (DRAM Burst of 8:* $\mathbf{t_{phy\_wrlat}}=3$, $\mathbf{t_{phy\_wrdata}}=3$*)*

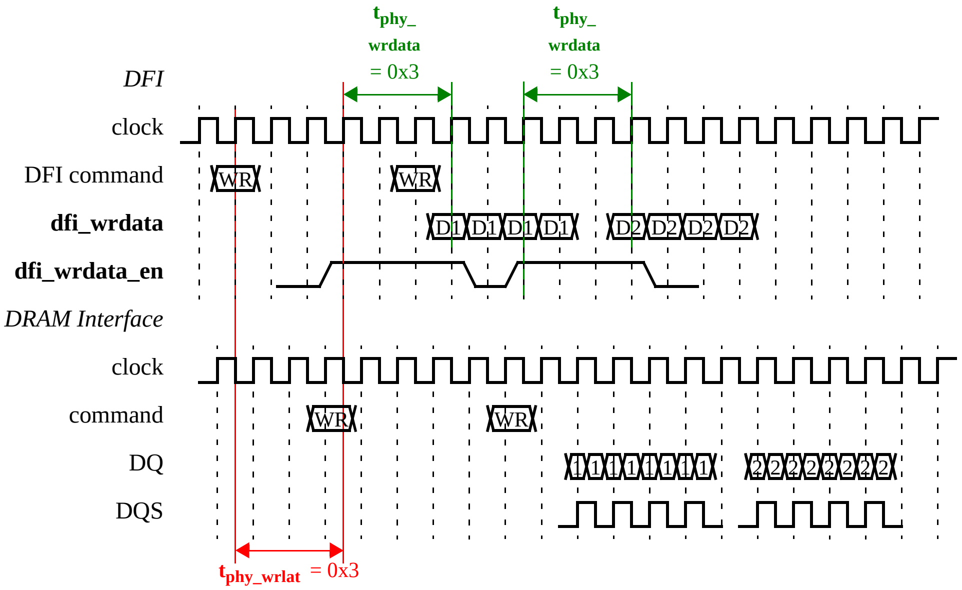


FIGURE 14. *Two Independent Writes (DRAM Burst of 4:* $\mathbf{t_{phy\_wrlat}}$=3, $\mathbf{t_{phy\_wrdata}}$=4*)*

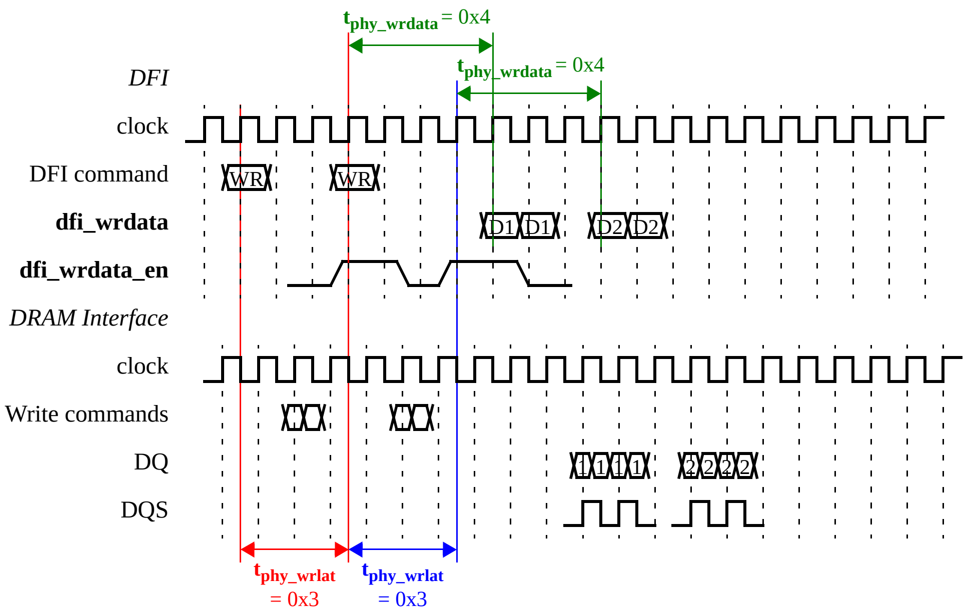
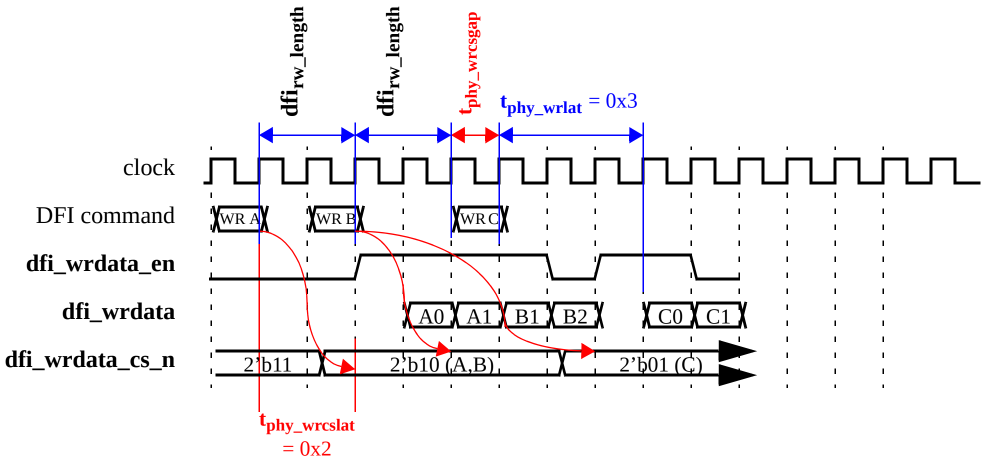


Figure 15, “Write Commands Utilizing dfi_wrdata_cs_n (DRAM Burst of 4: tphy_wrlat=3, tphy_wrdata=4, tphy_wrcslata=2, tphy_wrcsgap=1)” shows three write commands, with a gap between the second and third commands. The first two commands (WR A and WR B) address CS0 while the third one (WR C) addresses CS1. The two first write commands are back to back, that is, spaced by $\mathbf{dfi_{rw\_length}}$. The third command is also back to back, but with the required extra spacing, $\mathbf{t_{phy\_wrcsgap}}$.

FIGURE 15. *Write Commands Utilizing **dfi_wrdata_cs_n** (DRAM Burst of 4:* $\mathbf{t_{phy\_wrlat}}$=3, $\mathbf{t_{phy\_wrdata}}$=4, $\mathbf{t_{phy\_wrcslata}}$=2, $\mathbf{t_{phy\_wrcsgap}}$=1*)*



4.4.2 DBI - Write

DBI is an optional DFI feature used with write data transmissions. The **phy**$_{\textbf{dbi\_mode}}$ parameter is only needed when DBI is supported in DFI.

For more information on the **phy**$_{\textbf{dbi\_mode}}$ parameter, refer to Table 7, “Write Data Timing Parameters,” on page 32.

When the MC generates the write DBI data, the MC also inverts write data for DBI as required. The MC transmits the write DBI data across the DFI bus on **dfi_wrdata_mask_pN.** In DBI mode, the PHY is only required to transfer the write DBI data through the PHY. While write data is transmitting, the DBI data transmits simultaneously on the **dfi_wrdata_mask** signal. The **dfi_wrdata_mask** signal is sent coincident with the corresponding **dfi_wrdata** bus.

For frequency ratio systems, the **dfi_wrdata_mask** signal is extended, with a signal defined per phase.

When both DBI and CRC are enabled in a system, special care needs to be taken regarding where DBI and CRC are performed in order to operate correctly.

4.4.3 Cyclic Redundancy Check

CRC is an optional DFI feature used with write data transmissions to send CRC data as part of the write data burst. CRC extends a burst of 8 unit intervals (UI) to 10 UIs. When CRC is used, either the MC or the PHY can generate the CRC data; however, the MC must generate the CRC data if the PHY does not generate it. The CRC data is made of the CRC code that is expanded by the needed padding values to reach a full DFI PHY clock cycle data transfer (An example is padding with 1's for DDR4 x8 and x16 devices.)

While either the MC or the PHY can generate the CRC data, the PHY defines the value of the **phy**$_{\textbf{crc\_mode}}$ programmable parameter. The **phy**$_{\textbf{crc\_mode}}$ parameter is only needed when CRC is supported in DFI and uses the following definition to determine how CRC is handled:

- **phy**$_{\textbf{crc\_mode}}$ == 0 → CRC generation is handled in the MC
- **phy**$_{\textbf{crc\_mode}}$ == 1 → CRC generation is handled in the PHY

When CRC is supported in DFI, the system must be capable of the conditions listed in Table 23, “Systems Requiring CRC Support”.

TABLE 23. *Systems Requiring CRC Support*

Description	MC	PHY
Generates CRC Data	Yes	Optional
Interfaces with CRC Data	Yes	Yes [a]

[a] Required if the PHY does not generate the CRC data.

Regardless of which device generates the CRC, the MC asserts ODT such that it applies to all data sent + CRC data words.

4.4.3.1 MC CRC Support (phy_{crc_mode} ==0)

When the MC generates the CRC data, the $\mathbf{phy_{crc\_mode}}$ == 0 and the MC has the following requirements.

- The MC must assert the **dfi_wrdata_en** signal for the data transmitted across the DFI bus, including CRC data.
- The MC spaces commands to handle an extended burst with CRC.
- The MC generates **dfi_odt** (**dfi_odt_pN** in frequency ratio systems) based on the DRAM burst length including CRC data. With CRC enabled, the MC may need to extend ODT.
- The MC needs to receive and capture error information from the PHY. These CRC write data errors are transmitted on the **dfi_alert_n_aN** signal. In systems that support either command parity or CRC, the MC must support a **dfi_alert_n_aN** input and the PHY must support the **dfi_alert_n_aN** output.

With CRC, the **dfi_wrdata_en** signal could be asserted for an odd number of cycles per burst. Without exception, the PHY must support the odd CRC burst timing.

DFI dictates that when CRC is used, the CRC data word must be incorporated in the burst of write data, but DFI does not dictate placement within the burst. The specific ODT timing requirements are dependent on the chip selects accessed and system architecture. The **dfi_odt** assertion and de-assertion are identical in the MC CRC and PHY CRC support modes. The ODT signal timing shown is only an example of one potential solution.

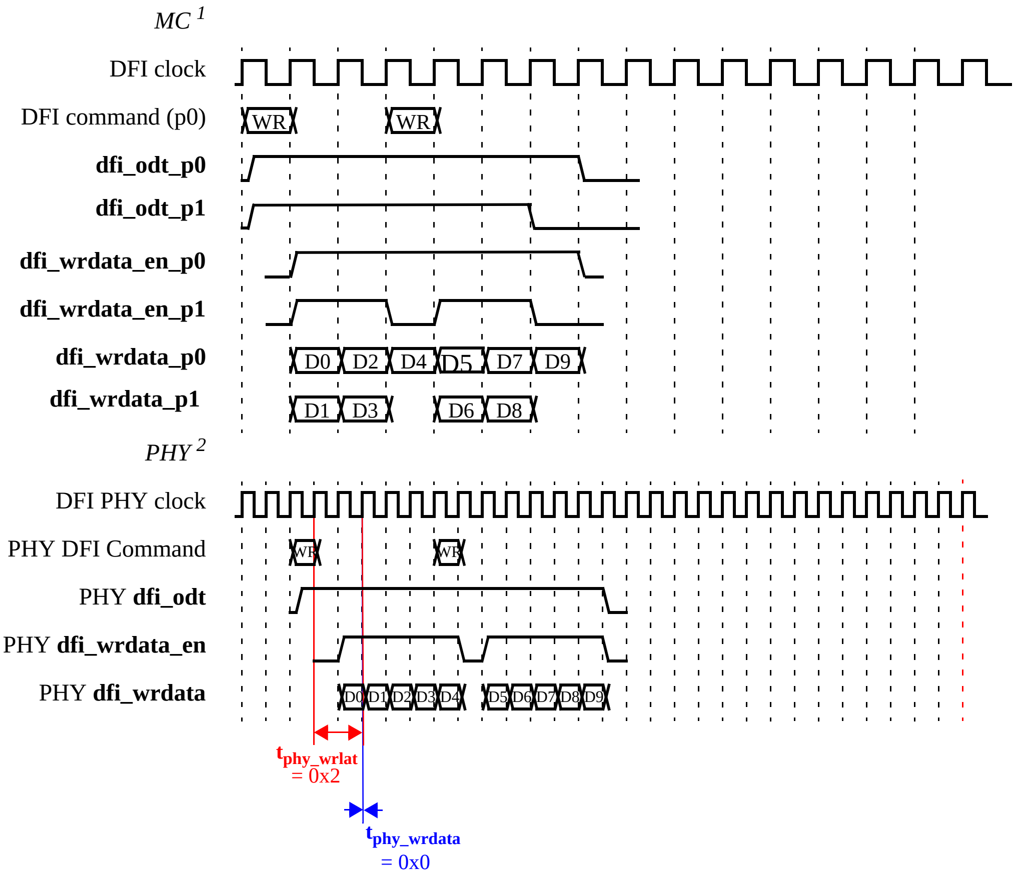
To further compare MC CRC support mode and PHY CRC support mode, DFI ODT signals are included in the following figures:

- Figure 16, “DFI Write Data Bus for MC CRC Support Mode (Two Bursts starting in Phase 0),” on page 77
- Figure 17, “DFI Write Data Bus for MC CRC Support Mode (Two Back-to-Back Bursts),” on page 78
- Figure 18, “DFI Write Data Bus for PHY CRC Support Mode,” on page 80
- Figure 19, “DFI Write Data Bus for PHY CRC Support Mode with Burst Chop,” on page 81.

Figure 16 and Figure 17 illustrate the DFI write data bus for a 2:1 frequency ratio system with CRC extending a burst of 8 by1 additional clock DRAM cycle.

The **dfi_wrdata_en** signal is only asserted for the data transmitted across the DFI, and consequently is not extended to include CRC data words.

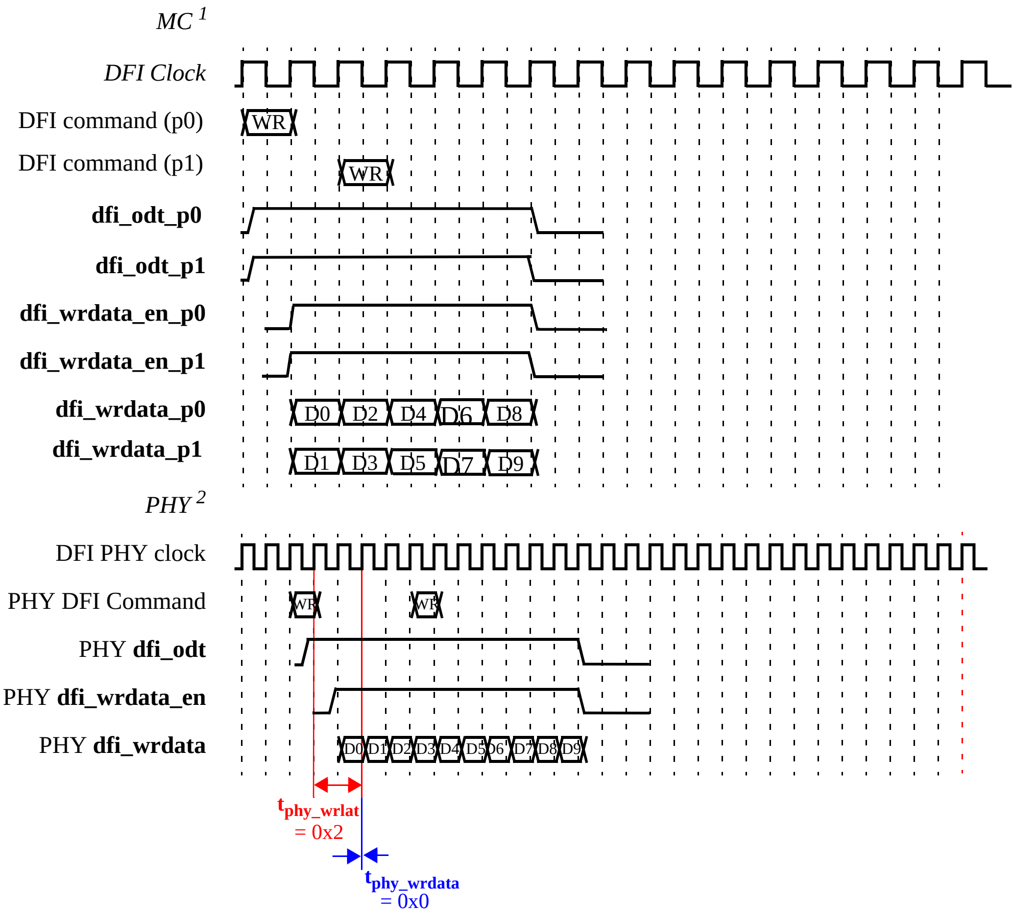
FIGURE 16. *DFI Write Data Bus for MC CRC Support Mode (Two Bursts starting in Phase 0)*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

FIGURE 17. *DFI Write Data Bus for MC CRC Support Mode (Two Back-to-Back Bursts)*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.4.3.2 PHY CRC Support (phy$_{\text{crc\_mode}}$ ==1)

If a PHY is capable of generating CRC data, the **phy**$_{\textbf{crc\_mode}}$ == 1 and the MC has the following requirements.

- The MC must disable its CRC generation logic so that CRC data is not transmitted across the DFI bus for write commands.
- The MC must assert the **dfi_wrdata_en** signal only for the data transmitted across the DFI bus, NOT for CRC.
- The MC spaces commands to handle an extended burst with CRC.
- The MC generates **dfi_odt** (**dfi_odt_pN** in frequency ratio systems) based on the DRAM burst length including CRC data. With CRC enabled, the MC may need to extend ODT.

- The MC needs to receive and capture error information from the PHY. These CRC write data errors are transmitted on the **dfi_alert_n_aN** signal. In systems that support command parity or CRC, the MC must support a **dfi_alert_n_aN** input and the PHY must support a **dfi_alert_n_aN** output.

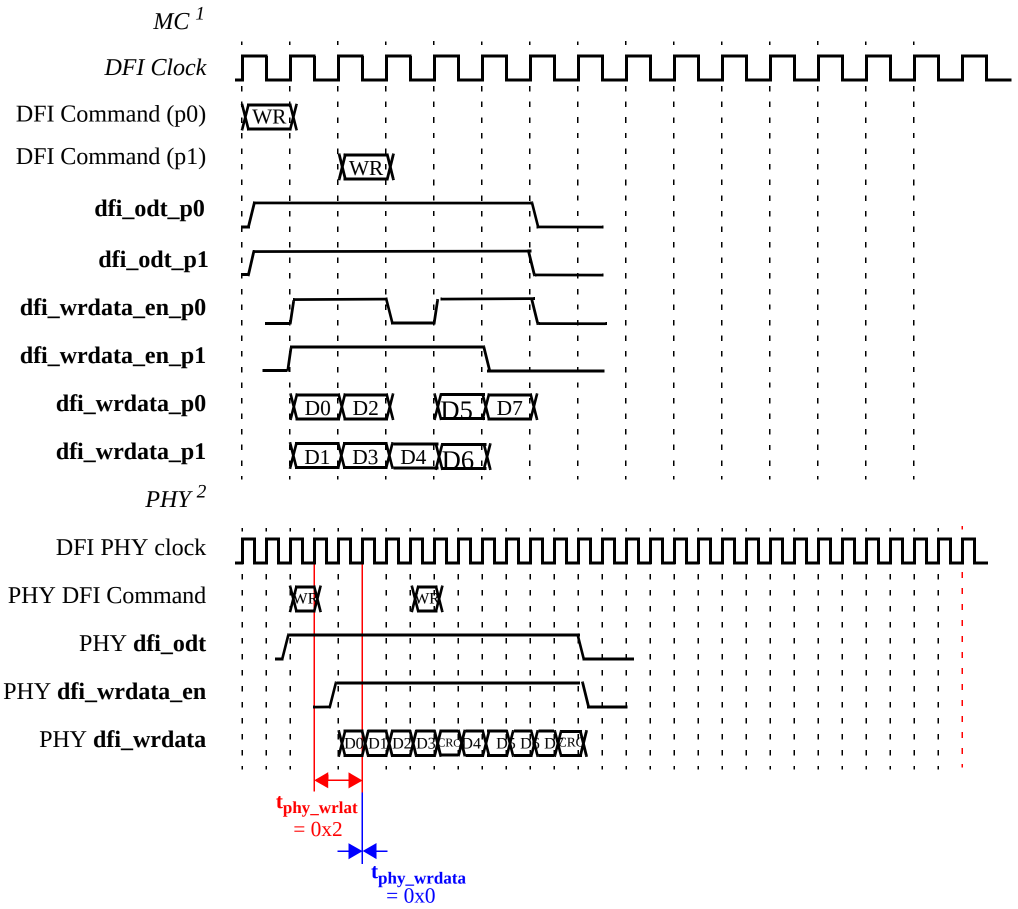
4.4.3.3 Burst Chop 4 with PHY CRC Support

In Burst Chop4 (BC4) mode, the memory burst is extended for CRC, similar to a burst of 8 requiring a 10 UI transfer. When the PHY generates the CRC data, the controller does not adjust **dfi_wrdata_en_pN** to account for the transfer of CRC data words.In a system supporting dynamic burst lengths and BC4, the PHY can use the width of the **dfi_wrdata_en_pN** signal to determine whether a transfer is a burst of 8 or whether the transfer is a BC4 data transmission. The PHY can utilize this information to determine how to generate CRC and when to send the CRC data.

Figure 18 and Figure 19 show PHY outputs that include a single extra CRC data word, shown at the end of the burst (the location of the CRC data word is DRAM-dependent). The figures also show that **dfi_odt** assertion and de-assertion for PHY CRC support are identical to the MC CRC Support mode in which the **dfi_odt** signals are extended to cover both CRC and write data. The specific ODT timing requirements are dependent on the chip selects accessed and the system topology. The ODT signal timing shown is only an example of one potential solution.

Figure 19, “DFI Write Data Bus for PHY CRC Support Mode with Burst Chop” illustrates a write BC4 case. This example shows a BC4 write followed by a burst of 8 write. With BC4, the MC only transmits 2 data words across the DFI bus. For both BC4 and burst of 8 commands, the CRC data is transmitted at the end of the burst, in UI9 and UI10.

FIGURE 18. *DFI Write Data Bus for PHY CRC Support Mode*

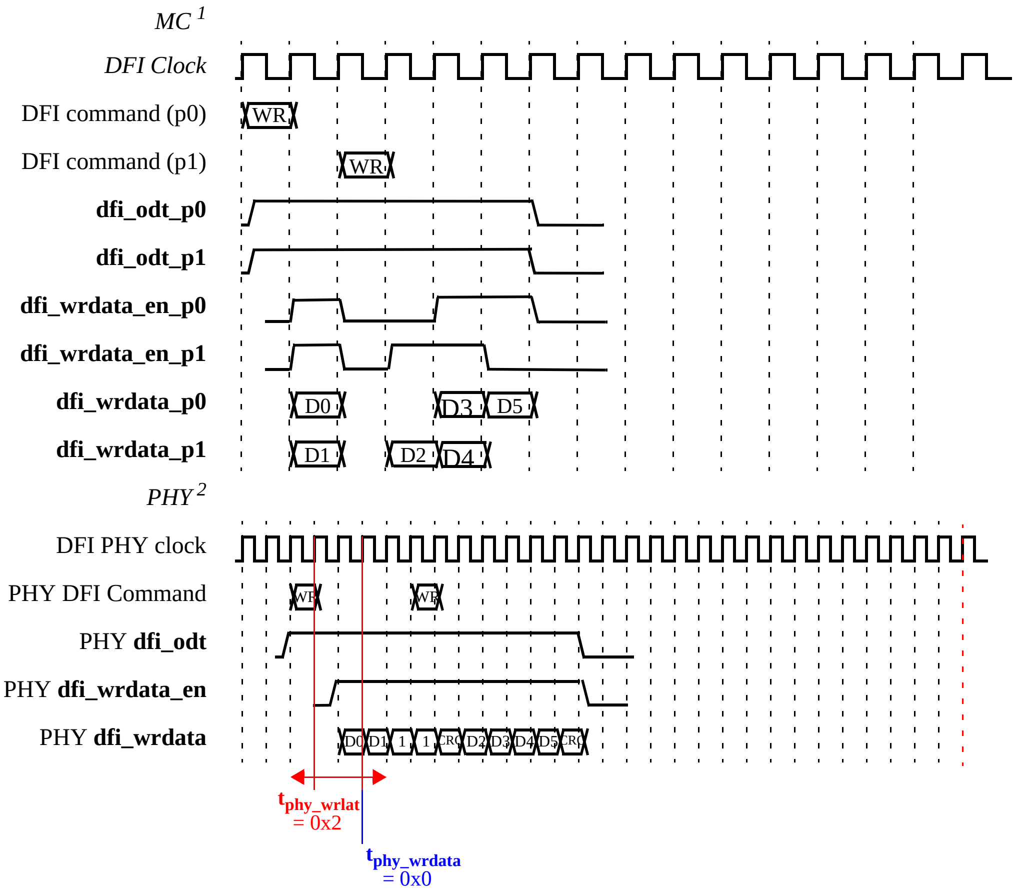


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

FIGURE 19. *DFI Write Data Bus for PHY CRC Support Mode with Burst Chop*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock diagram.

1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.5 Read Transactions

The read data transaction handles the capture and return of data across the DFI bus.

The DFI read transaction includes the signals for read data enable (**dfi_rddata_en**), read data (**dfi_rddata**), the read data valid (**dfi_rddata_valid**), read data not valid (**dfi_rddata_dnv**) for LPDDR2 DRAMs, read data inversion (**dfi_rddata_dbi**) for DDR4 systems, an optional target data chip select (**dfi_rddata_cs_n)**, and the timing parameters $\mathbf{t_{rddata\_en}}$ and $\mathbf{t_{phy\_rdlat}}$.

The number of clocks of **dfi_rddata_en** assertion must correlate with the number of data transfers executed on the DRAM bus.

If used, the **dfi_rddata_cs_n** signal provides the target data path chip select value to each of the PHY data slices. For more information on these signals, refer to Section 3.3, “Read Data Interface,” on page 33.

DFI read data must be returned from the PHY within a maximum delay defined by the sum of the $\mathbf{t_{rddata\_en}}$ and $\mathbf{t_{phy\_rdlat}}$ timing parameters. The $\mathbf{t_{rddata\_en}}$ is a fixed delay, but the $\mathbf{t_{phy\_rdlat}}$ is defined as a maximum value. The delay can be adjusted as long as both the MC and the PHY coordinate the change such that the DFI specification is maintained. Both parameters may be expressed as equations based on other fixed system parameters.

4.5.1 Read Transaction Sequence

The sequence for DFI read transactions is listed below; the effect of using the optional read data chip select or DBI is shown within brackets.

1. The read command is issued.
2. $\mathbf{t_{rddata_en}}$cycles elapse.

   [If using read data chip select, $\mathbf{t_{phy\_rdcslat}}$ cycles elapse.]

   [The PHY defines the $\mathbf{t_{phy\_rdcslat}}$ timing parameter to specify the desired alignment of the command to the **dfi_rddata_cs_n** signal; the PHY defines the $\mathbf{t_{phy\_rdcsgap}}$ timing parameter to specify the additional delay it requires between two consecutive commands that are targeting different chip selects. The PHY may require the MC to add additional delay beyond other system timing requirements to account for PHY-specific adjustments transitioning between chip selects.]

   [The gap timing requirement is system-specific and may only be applicable to certain chip-select-to-chip-select. It may not be applicable to other chip select transitions where the PHY is not required to make an internal adjustment on the chip select change. For example, a system may not require additional delay on transitions between chip select 0 and chip select 1, but may require additional delay when transitioning from chip select 0 to chip select 2. Accordingly, the interface does not require the gap timing to be applied on every chip select transition.]
3. The $\mathbf{t_{rddata\_en}}$ parameter defines the timing requirements between the read command on the DFI interface and the assertion of the **dfi_rddata_en** signal to maintain synchronicity between the MC and the PHY for the start of contiguous read data expected on the DFI interface. The exact value of this parameter for a particular application is determined by memory system components. For non-contiguous read commands, $\mathbf{t_{rddata\_en}}$ cycles elapse, and the **dfi_rddata_en** signal is asserted on the DFI and remains asserted for the number of contiguous cycles that read data is expected.
4. For contiguous read commands, $\mathbf{t_{rddata\_en}}$ cycles after the first read command of the stream, the **dfi_rddata_en** signal is asserted and remains asserted for the entire length of the data stream.
5. One continuous assertion of the **dfi_rddata_en** signal may encompass data for multiple read commands. The **dfi_rddata_en** signal de-asserts to signify there is no more contiguous data expected from the DFI read command(s). Note that the **dfi_rddata_en** signal is not required to be asserted for any fixed number of cycles. The MC continues to drive **dfi_rddata_cs_n** a minimum of the data transfer width (**dfi_ rw_length**) plus the gap timing ($\mathbf{t_{phy\_rdcsgap}}$); the MC may then drive the next chip select or a valid value (any valid chip select or inactive).

   The minimum time the chip select is guaranteed to remain driven to the PHY relative to the read command is defined by $\mathbf{t_{phy\_rdcslat}}$ **+ dfi_ wr_length +** $\mathbf{t_{phy\_rdcsgap}}$.

The maximum delay that can be achieved from the assertion of a new chip on **dfi_rddata_cs_n** and the corresponding **dfi_rddata_en** is limited to the maximum time the PHY has to make internal adjustments associated with changing the target chip select relative to the read data transfer ($\mathbf{t_{rddata\_en}}$ **-** $\mathbf{t_{phy\_rdcslat}}$),.

The PHY must define the $\mathbf{t_{phy\_rdcslat}}$ and $\mathbf{t_{phy_rdcsgap}}$timing parameters to allocate the time between transactions to different chip selects necessary for internal adjustments.

6. The data is returned with the **dfi_rddata_valid** signal asserted.

[For LPDDR2 memory systems, the **dfi_rddata_dnv** signal has the same timing as the **dfi_rddata** signal.]

7. The associated read data signal (**dfi_rddata**) is sent.

[If DBI is enabled, the read data dbi signal (**dfi_rddata_dbi)** is sent coincident with the read data signal.]

Ten situations are presented in Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, Figure 27, Figure 28, and Figure 29.

Figure 20 shows a single read transaction. In this case, the **dfi_rddata_en** signal is asserted for two cycles to inform the DFI that two cycles of DFI data are expected and data is returned $\mathbf{t_{phy\_rdlat}}$ cycles after the **dfi_rddata_en** signal assertion.

FIGURE 20. *Single Read Transaction of 2 Data Words*

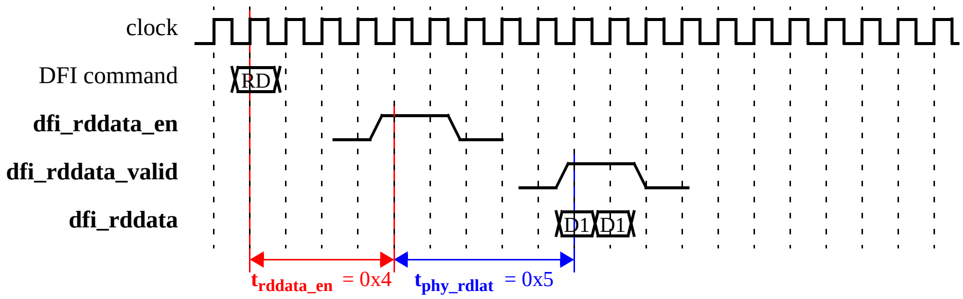


Figure 21 shows a single read transaction where the data is returned in less than the maximum delay. The data returns one cycle less than the maximum PHY read latency.

FIGURE 21. *Single Read Transaction of 4 Data Words*

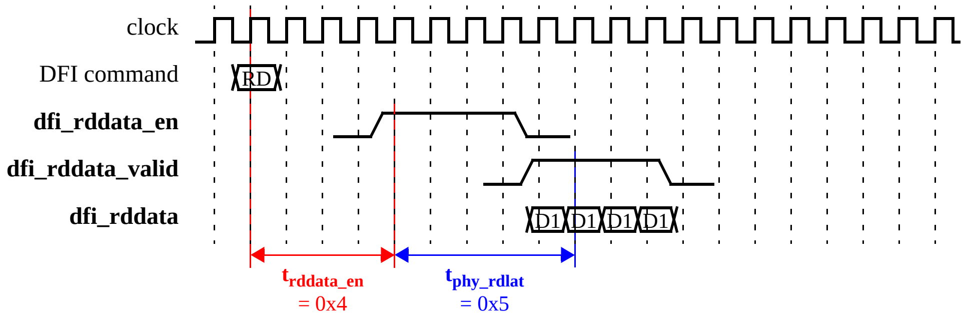


Figure 22 shows an interrupted read command. The **dfi_rddata_en** signal must be asserted for 4 cycles for each of these read transactions. However, since the first read is interrupted, the **dfi_rddata_en** signal is asserted for a portion of the first transaction and the complete second transaction. In this case, the **dfi_rddata_en** signal will not de-assert between read commands.

FIGURE 22. *Back-to-Back Read Transactions with First Read Burst Interrupted (DDR1 Example BL=8)*

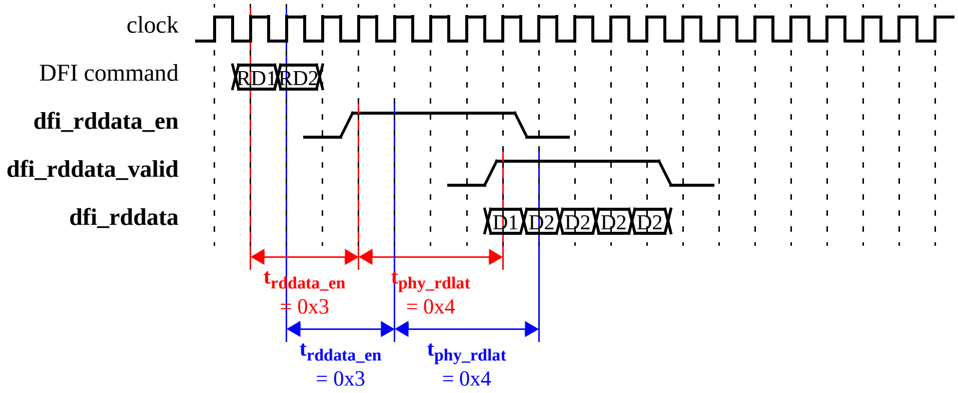
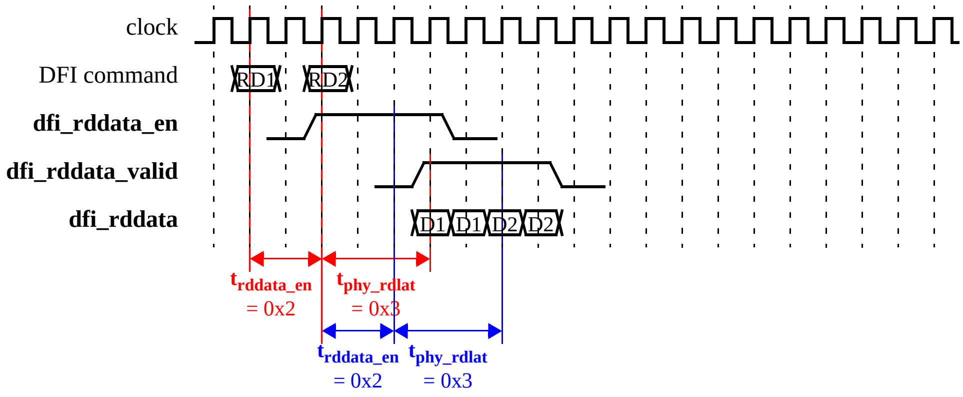


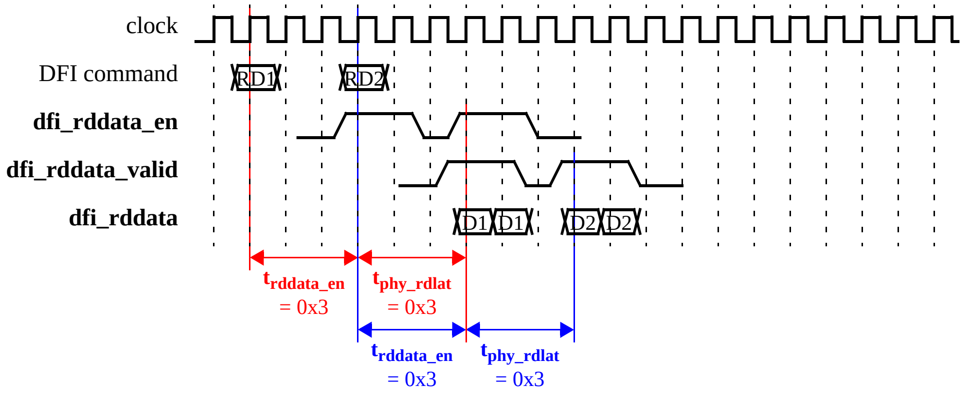
Figure 23 and Figure 24 also show two complete read transactions. The **dfi_rddata_en** signal is asserted for two cycles for each read transaction. In Figure 23, “Two Independent Read Transactions (DDR1 Example)”, the values for the timing parameters are such that the read data is returned in a contiguous data stream for both transactions. Therefore, the **dfi_rddata_en** signal and the **dfi_rddata_valid** signal are each asserted for the complete read data stream.

FIGURE 23. *Two Independent Read Transactions (DDR1 Example)*



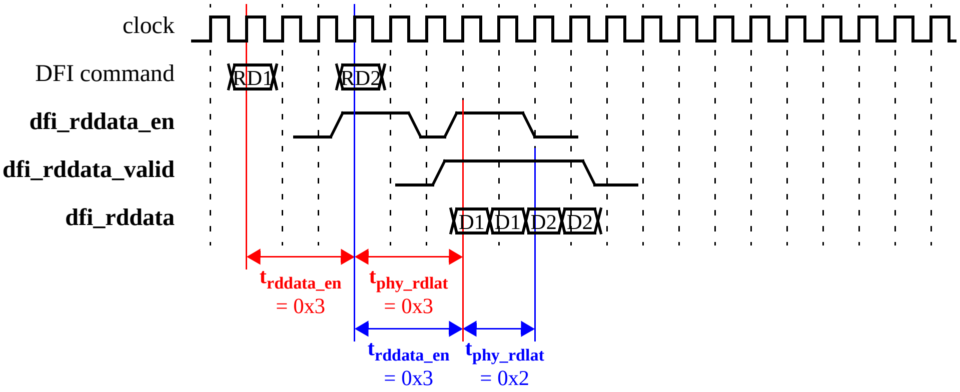
In Figure 24, "Two Independent Read Transactions (DDR2 Example)", the $\mathbf{t_{rddata\_en}}$ timing and the timing between the read commands causes the **dfi_rddata_en** signal to be de-asserted between commands. As a result, the **dfi_rddata_valid** signal is de-asserted between commands and the **dfi_rddata** stream is non-contiguous.

FIGURE 24. *Two Independent Read Transactions (DDR2 Example)*



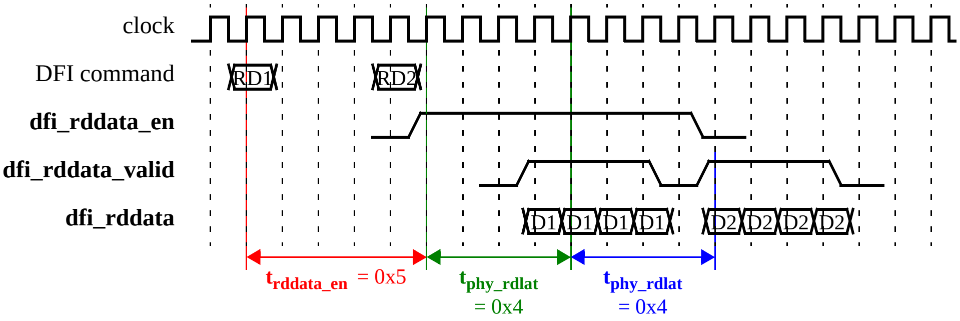
In Figure 25, “Two Independent Read Transactions (DDR2 Example)”, the effective **t_{phy_rdlat}** for the two transactions is different. This results in a situation in which the **dfi_rddata_valid** signal remains asserted across commands and the **dfi_rddata** stream is contiguous.

FIGURE 25. *Two Independent Read Transactions (DDR2 Example)*



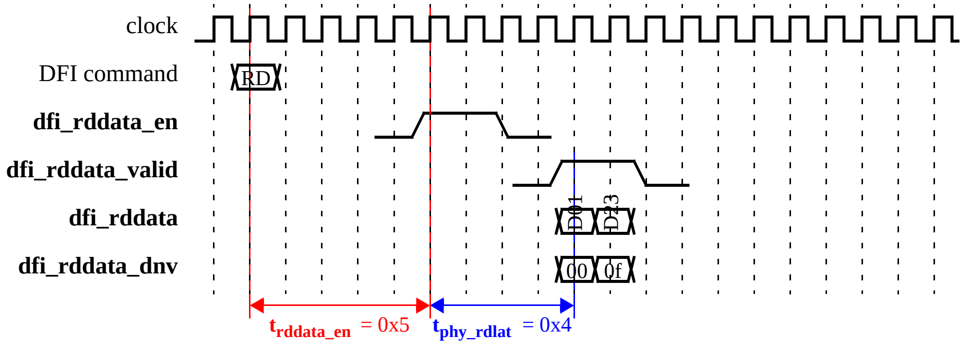
The data may return to the DFI in fewer cycles than maximum delay. In Figure 26, “Two Independent Read Transactions (DDR3 Example)”, the first read data transfer is returned in three cycles, even though the **t_{phy_rdlat}** timing parameter is set to four cycles. The second read data transfer is returned in the maximum of four cycles.

FIGURE 26. *Two Independent Read Transactions (DDR3 Example)*



LPDDR3 and LPDDR2 DRAMs define a new transaction type of mode register read (MRR). From the DFI perspective, a mode register read is handled like any other read command and utilizes the same signals. Figure 27, “Example MRR Transactions with LPDDR2” shows an MRR transaction for a LPDDR3 or LPDDR2 memory device.

FIGURE 27. *Example MRR Transactions with LPDDR2*



In Figure 28, “DFI Read Data Transfer Illustrating dfi_rddata_valid Definition”, the **dfi_rddata_valid** signals are transferred independently. This figure shows a one-to-one correspondence between the data words for **dfi_rddata_en** and **dfi_rddata_valid;** the **dfi_rddata_valid** words do not need to be contiguous.

FIGURE 28. *DFI Read Data Transfer Illustrating **dfi_rddata_valid** Definition*

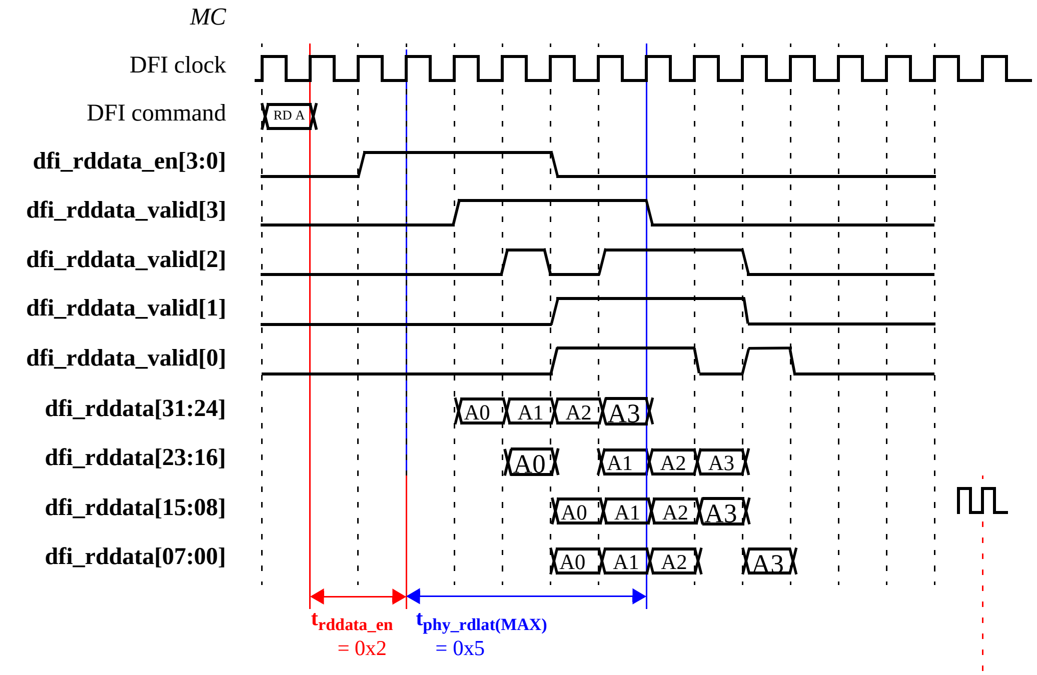
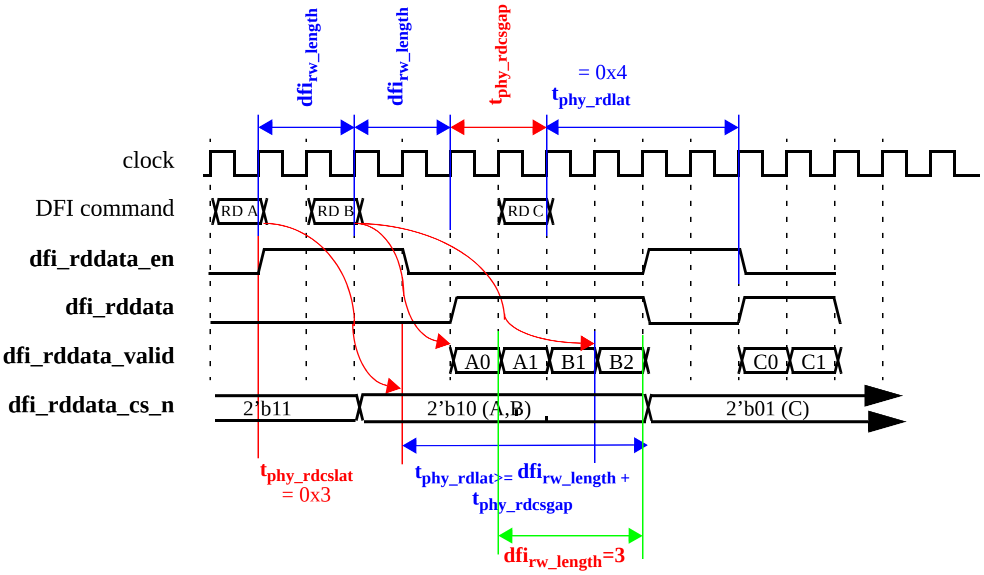


Figure 29, “Read Commands Utilizing dfi_rddata_cs_n” shows three read commands, with a gap between the second and third commands.

FIGURE 29. *Read Commands Utilizing* ***dfi_rddata_cs_n***



4.5.2 DBI - Read

DBI is an optional DFI feature used with read data transmissions. The **phy**$_{\textbf{dbi\_mode}}$ parameter is only needed when DBI is supported in DFI. If DBI is required in a system, DRAM DBI input must be received and used to selectively invert data for read commands.

For more information on the **phy**$_{\textbf{dbi\_mode}}$ parameter, refer to Table 8, “Write Data Programmable Parameters,” on page 33.

4.5.2.1 MC DBI Support (phy$_{dbi\_mode}$==0)

The PHY captures the DRAM read DBI data and transmits the data over the DFI to the MC using the **dfi_rddata_dbi** signals. For more information on the DBI signals, refer to Table 6, “Write Data Signals,” on page 31 and Table 9, “Read Data Signals,” on page 35. The timing of the **dfi_rddata_dbi** signal is identical to the timing of the **dfi_rddata** signal, and the DBI data is sent coincident with the corresponding **dfi_rddata** bus.

For frequency ratio systems, the **dfi_rddata_dbi** signal is extended, similar to **dfi_rddata**, with a signal defined per phase. For example, with a 4:1 frequency system, the DBI information is transmitted across the **dfi_rddata_dbi_w0**, **dfi_rddata_dbi_w1**, **dfi_rddata_dbi_w2**, and **dfi_rddata_dbi_w3** signals.

The timing of the phase outputs for DBI is identical to the **dfi_rddata_wN** outputs, with the data returned in a rolling order.

4.5.2.2 PHY DBI Support (phy$_{dbi\_mode}$==1)

When the PHY generates the write DBI data, the **dfi_rddata_dbi** signal is not needed.

4.6 Update

The DFI contains signals to support MC-initiated and PHY-initiated update processes. The signals used in the update interface are: **dfi_ctrlupd_req**, **dfi_ctrlupd_ack**, **dfi_phyupd_req**, **dfi_phyupd_type** and **dfi_phyupd_ack**. The idle state timing parameters used in the update interface are: t_{ctrl_delay} and t_{wrdata_delay}.

For more information on the signals, refer to Section 3.4, “Update Interface,” on page 37. For more information on the idle state timing parameters, refer to Table 5, “Control Timing Parameters,” on page 29 and Table 7, “Write Data Timing Parameters,” on page 32.

4.6.1 MC-Initiated Update

During normal operation, the MC may encounter idle time during which no commands are issued to the DRAMs and all outstanding read and write data have been transferred on the DFI bus and the write data transfer has completed on the memory bus. Assertion of the **dfi_ctrlupd_req** signal indicates the control, read and write interfaces on the DFI are idle. While the **dfi_ctrlupd_ack** signal is asserted, the DFI bus may only be used for commands related to the update process.

The MC guarantees that **dfi_ctrlupd_req** signal is asserted for at least $t_{ctrlupd\_min}$ cycles, allowing the PHY time to respond. The PHY may respond to or ignore the update request. To acknowledge the request, the **dfi_ctrlupd_ack** signal must be asserted before $t_{ctrlupd\_max}$ expires and while the **dfi_ctrlupd_req** signal is asserted. The **dfi_ctrlupd_ack** signal must de-assert at least one cycle before $t_{ctrlupd\_max}$ expires.

The MC must hold the **dfi_ctrlupd_req** signal as long as the **dfi_ctrlupd_ack** signal is asserted. The PHY must de-assert the **dfi_ctrlupd_ack** signal before $t_{ctrlupd\_max}$ expires.

Figure 30, “MC-Initiated Update Timing Diagram” shows that the DFI does not specify the number of cycles after the **dfi_ctrlupd_ack** signal de-asserts before the **dfi_ctrlupd_req** signal de-asserts.

FIGURE 30. *MC-Initiated Update Timing Diagram*

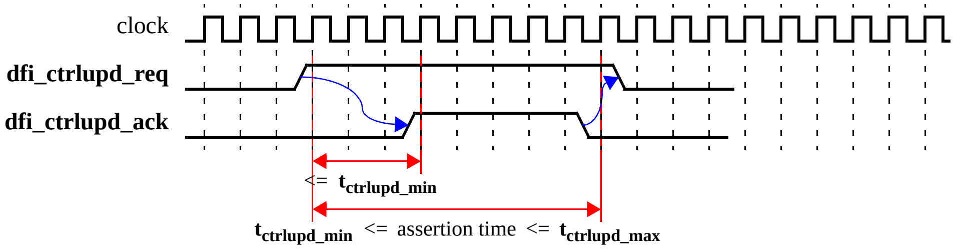
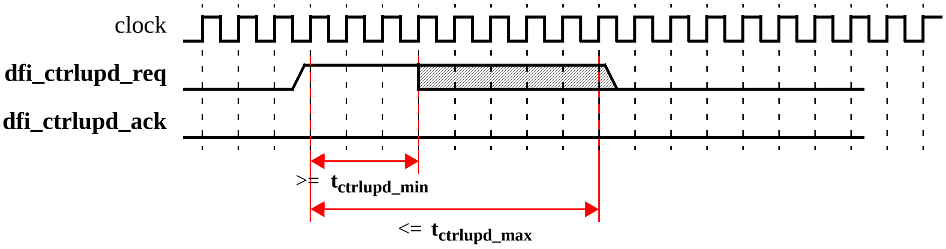


Figure 31, “MC-Initiated Update with No Response” shows the important point that the **dfi_ctrlupd_ack** signal is not required to assert when the **dfi_ctrlupd_req** signal is asserted. The MC must assert the **dfi_ctrlupd_req** signal for at least $\mathbf{t_{ctrlupd\_min}}$ within every $\mathbf{t_{ctrlupd\_interval}}$ cycle, but the total number of cycles that the **dfi_ctrlupd_req** signal is asserted must not exceed $\mathbf{t_{ctrlupd\_max}}$.

FIGURE 31. *MC-Initiated Update with No Response*



4.6.2 PHY-Initiated Update

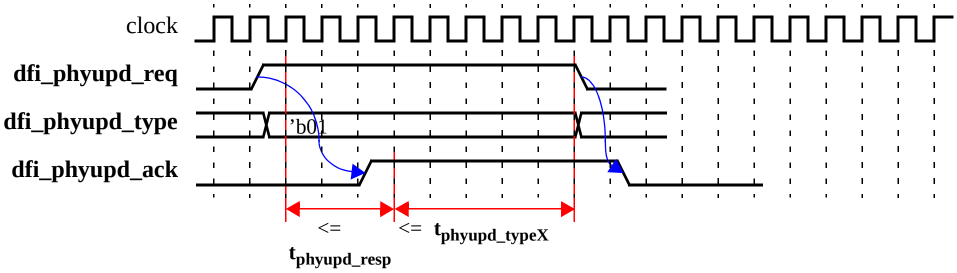
The PHY may also trigger the DFI to enter an idle state. This update process utilizes three signals: **dfi_phyupd_req**, **dfi_phyupd_type** and **dfi_phyupd_ack**. The **dfi_phyupd_req** signal indicates the need for idle time on the DFI, the **dfi_phyupd_type** signal defines the type of update required, and the **dfi_phyupd_ack** signal is the MC’s response signal. Four update types are specified by the DFI.

To request an update, the **dfi_phyupd_type** signal must be valid when the **dfi_phyupd_req** signal is asserted. The $\mathbf{t_{phyupd\_typeX}}$ parameters indicate the maximum number of cycles of idle time on the DFI control, read and write data interfaces being requested. The **dfi_phyupd_ack** signal must assert within $\mathbf{t_{phyupd\_resp}}$ cycles after the assertion of the **dfi_phyupd_req** signal.

When the **dfi_phyupd_ack** signal is asserted, it must remain asserted until the **dfi_phyupd_req** signal de-asserts; the **dfi_phyupd_req** signal must de-assert before $\mathbf{t_{phyupd\_typeX}}$ cycles have expired. The **dfi_phyupd_ack** signal must de-assert following the detection of the **dfi_phyupd_req** signal de-assertion. The **dfi_phyupd_ack** signal for the previous transaction must be de-asserted before the **dfi_phyupd_req** signal can re-assert. While the **dfi_phyupd_ack** signal is asserted, the DFI bus may only be used for commands related to the update process.

Figure 32, “PHY-Initiated Update Timing Diagram” shows that the MC must respond to a PHY update request, unlike MC-initiated updates shown in Figure 30, “MC-Initiated Update Timing Diagram” and Figure 31, “MC-Initiated Update with No Response”.

FIGURE 32. *PHY-Initiated Update Timing Diagram*



4.6.3 DFI Idle

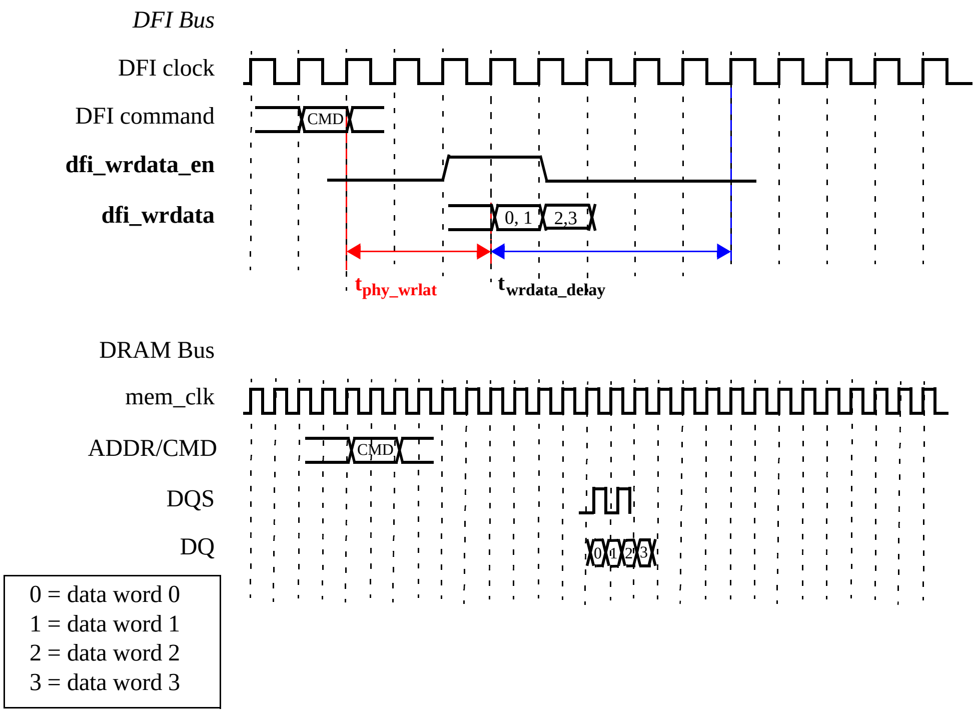
To prevent the condition where a PHY may disrupt the write data transfer on the memory bus, the write data transfer on the memory bus must complete before the DFI idle state is reached.

The $\mathbf{t_{wrdata\_delay}}$ idle state timing parameter defines the number of DFI clocks from **dfi_wrdata_en** to the completion of the write data transfer on the memory bus. Since the requirement for an idle bus state following a write is generally an infrequent event relative to the overall traffic pattern, the accuracy of the setting should not be a performance issue, so it may be set to a larger value.

If a PHY has no dependency between completing a write data transfer on the DFI bus and the idle state, the $\mathbf{t_{wrdata\_delay}}$ parameter can be set to zero.

When a PHY does have a dependency between completing a write data transfer on the DFI bus and the idle state, the $\mathbf{t_{wrdata\_delay}}$ parameter should be set to a sufficiently large value to accommodate the write data width, flight time through the PHY, and worst-case timing on the memory bus.

FIGURE 33. *Bus Idle State Timing Parameter - t_{wrdata_delay}*

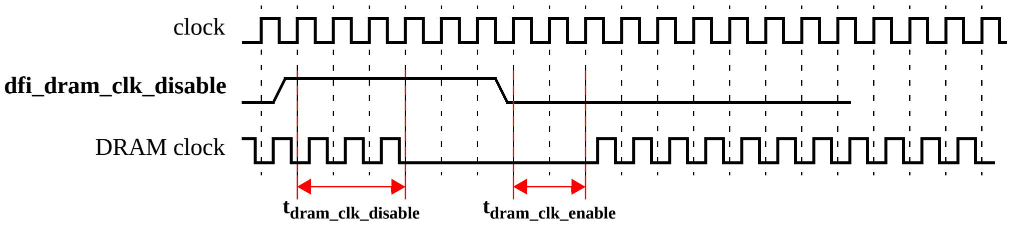


4.7 DFI Clock Disabling

The DFI contains a **dfi_dram_clk_disable** signal which controls the DRAM clock signal to the DRAM device(s). In the default state, the DRAM clock functions normally and the **dfi_dram_clk_disable** bits are all de-asserted. If the system requires the clocks of the memory device(s) to be disabled, the **dfi_dram_clk_disable** signal is asserted. For more information on the **dfi_dram_clk_disable** signal, refer to Section 3.5, “Status Interface,” on page 41.

Figure 34, “DRAM Clock Disable Behavior” shows that two timing parameters $t_{dram\_clk\_disable}$ and $t_{dram\_clk\_enable}$ indicate the number of DFI cycles that the PHY requires to respond to the assertion and de-assertion of the **dfi_dram_clk_disable** signal. The $t_{dram\_clk\_disable}$ value determines the number of DFI cycles in which a rising edge of the **dfi_dram_clk_disable** signal affects the DRAM clock and $\mathbf{t_{dram\_clk\_enable}}$ sets the number of cycles required for the DRAM clock to be active again.

FIGURE 34. *DRAM Clock Disable Behavior*



4.8 Frequency Ratios Across the DFI

In a DDR memory subsystem, it may be advantageous to operate the PHY at a higher frequency than the MC. If the PHY operates at a multiple of the MC frequency, the PHY transfers data at a higher data rate relative to the DFI clock and the MC has the option to execute multiple commands in a single DFI clock cycle. The DFI is defined at the MC to PHY boundary and therefore operates in the clock frequency domain of the MC.

The MC clock is always the DFI clock and all DFI signals are referenced from the MC clock.

The DFI specification supports a 1:1, 1:2 or 1:4 MC to PHY frequency ratio, defining the relationship of the reference clocks for the MC and the PHY. The DFI DDR PHY clock is always the same frequency as the DRAM clock, which is 1/2 the data rate for the memory.

DFI signals may be sent or received on the DFI PHY clock, provided the signals reference the rising edge of the DFI clock and the clock is phase aligned. The MC communicates frequency ratio settings to the PHY on the **dfi_freq_ratio** signal. This signal is only required for devices using this frequency ratio protocol.

For more information on the frequency ratio clock, refer to Section 4.8.1, “Frequency Ratio Clock Definition,” on page 94.

The frequency ratio protocol affects the write data and read data interfaces, including read data rotation and resynchronization.

For information on how the write data and read data interfaces are affected, refer to Section 4.8.2, “Interface Signals with Frequency Ratio Systems,” on page 94, Section 4.8.3, “Write Data Interface in Frequency Ratio Systems,” on page 98, Section 4.8.4, “Read Data Interface in Frequency Ratio Systems,” on page 100, Section 4.8.4.1, “DFI Read Data Rotation,” on page 107, and Section 4.8.4.1.1, “Read Data Resynchronization,” on page 110.

Frequency ratio also affects CA and CRC parity errors.

For information on how frequency ratio affects CA and CRC parity errors, refer to Section 4.10.2.1, “CA Parity and CRC Errors in Frequency Ratio Systems,” on page 114.

4.8.1 Frequency Ratio Clock Definition

The DFI clock and the DFI PHY clock must be phase-aligned and at a 1:2 or 1:4 frequency ratio relative to one another. Some DFI signals from the MC to the PHY must communicate information about the signal in reference to the DFI PHY clock to maintain the correct timing information. Therefore, the DFI PHY clock is described in terms of phases, where the number of clock phases for a system is the ratio of the DFI PHY clock to the DFI clock.

Figure 35, “Frequency Ratio 1:2 Phase Definition” and Figure 36, “Frequency Ratio 1:4 Phase Definition” show the clock phase definitions for 1:2 and 1:4 frequency ratio systems.

FIGURE 35. *Frequency Ratio 1:2 Phase Definition*

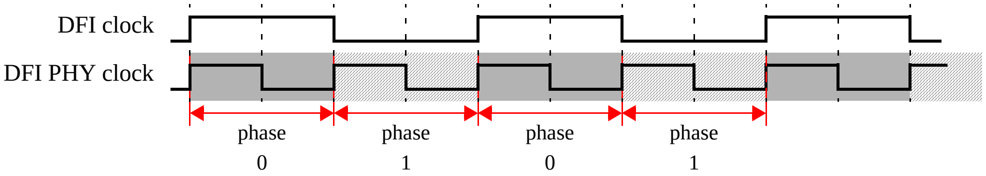
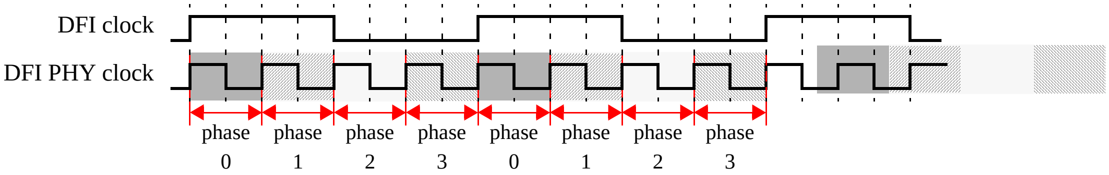


FIGURE 36. *Frequency Ratio 1:4 Phase Definition*



4.8.2 Interface Signals with Frequency Ratio Systems

Write data and read data signals are defined on a per-phase basis and all signal timing is in reference to the DFI clock. The PHY must account for any assertions based on the DFI clock. Any signals driven by the PHY must only change during phase 0 of the DFI PHY clock to allow the MC the full DFI clock to capture the signal change.

The DFI specification supports the ability to send a unique command on each phase of the DFI PHY clock. To communicate this information to the PHY, the DFI specification defines commands for a frequency ratio system in a vectored format. The PHY must maintain this information to preserve the timing relationships between commands and data. Therefore, for frequency ratio systems, the control signal interface, the write data interface and the read data enable signal are all suffixed with a “_pN” where N is the phase number. As an example, for a 1:2 frequency ratio system, instead of a single **dfi_address** signal, there are 2 signals: **dfi_address_p0** and **dfi_address_p1**. The read data signal, read data valid and read data not valid signals are suffixed with a “_wN” where N is the DFI data word. More information on the read data interface for frequency ratio systems is provided in Section 4.8.4, “Read Data Interface in Frequency Ratio Systems”. The phase 0 or DFI data word 0 suffixes are not required.

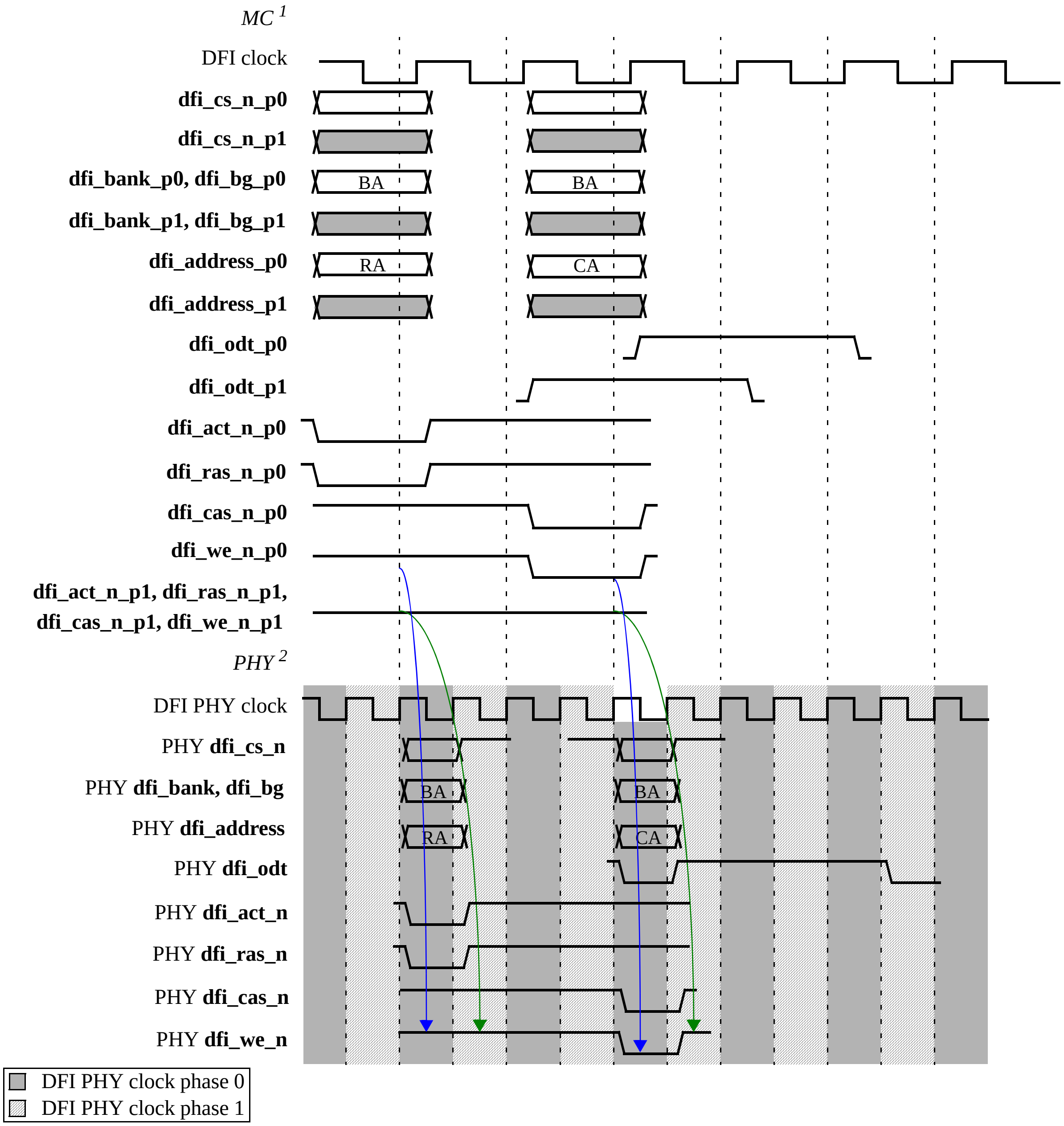
There is flexibility in system setup for frequency ratio systems. The MC may be implemented to support command output on a single phase or on multiple phases. Even if multiple phases are supported, the MC is not required to implement or drive every phase of a signal. Only phases where a command is sent must be implemented and driven. The exceptions to the rule are the **dfi_cke_pN** and **dfi_odt_pN** signals. These two signals are not necessarily driven in the same phase as the rest of the command. Therefore, these signals must be implemented for all phases of the clock to allow flexibility in timing.

The PHY must be able to accept a command on all phases to be DFI compliant. If the MC is only using certain phases, the PHY must be appropriately connected to properly interpret the command stream.

There is no requirement that signals must be implemented in the same way across the interfaces. For example, in a 2T implementation, the **dfi_ras_n_pN**, **dfi_cas_n_pN** and **dfi_we_n_pN** signals may be driven by the MC on all clock phases, but the **dfi_cs_n_pN** signal may only be driven by the MC on half of the phases.

Figure 37, “Example 1:2 Frequency Ratio Command Stream” illustrates an example command stream for a 1:2 frequency ratio system and how the PHY in this system would interpret the DFI signals. In this example, a command is only sent on phase 0; the values of phase 0 and phase 1 commands will be different. ODT information is provided on both phases. The command bus signals are not always the same value and are not always equal to one.

FIGURE 37. *Example 1:2 Frequency Ratio Command Stream*



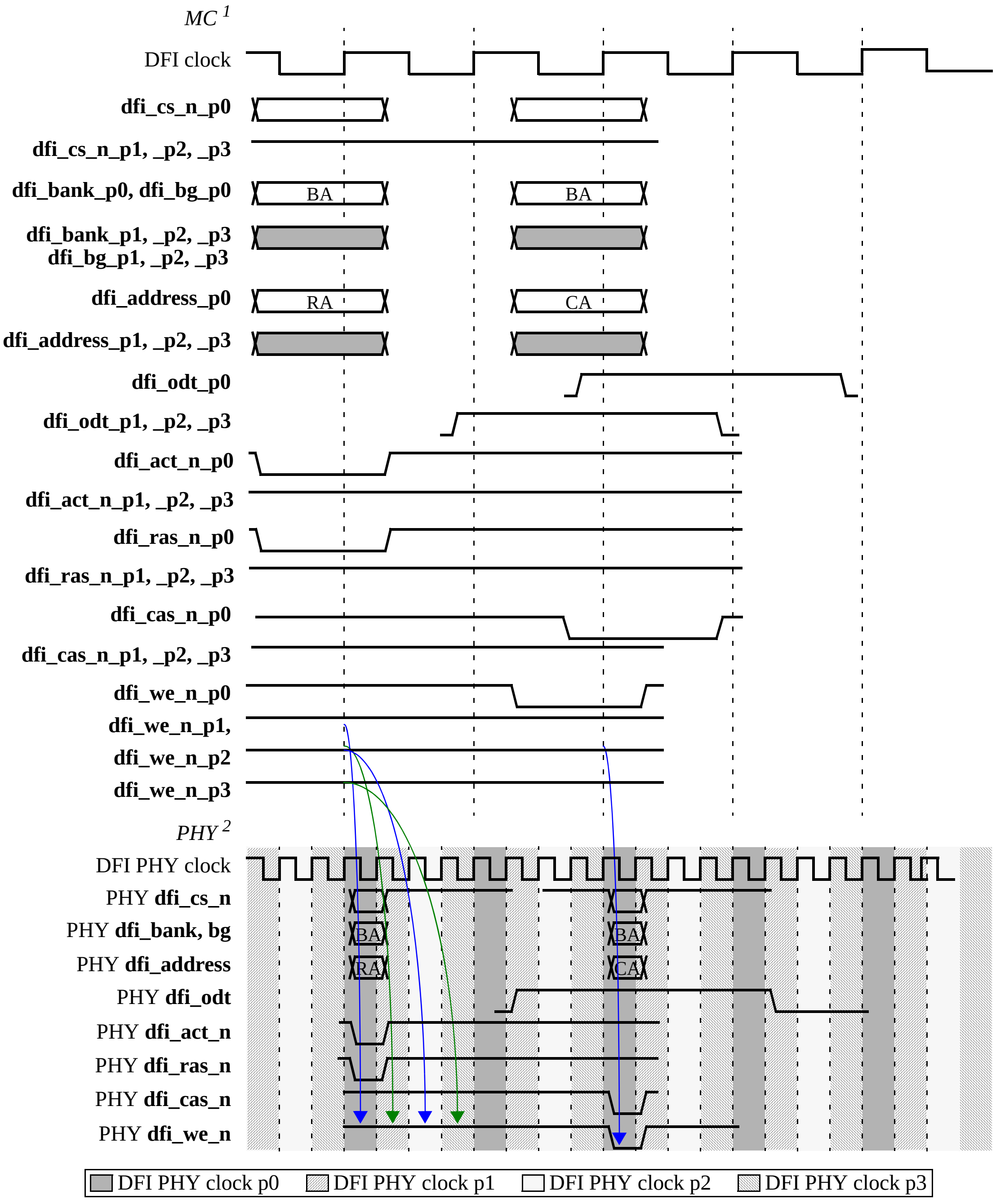
NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

Figure 38, “Example 1:4 Frequency Ratio Command Stream” represents the same example, in a 1:4 frequency ratio system. The command is only sent on phase 0 and ODT information is provided on all phases.

FIGURE 38. *Example 1:4 Frequency Ratio Command Stream*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

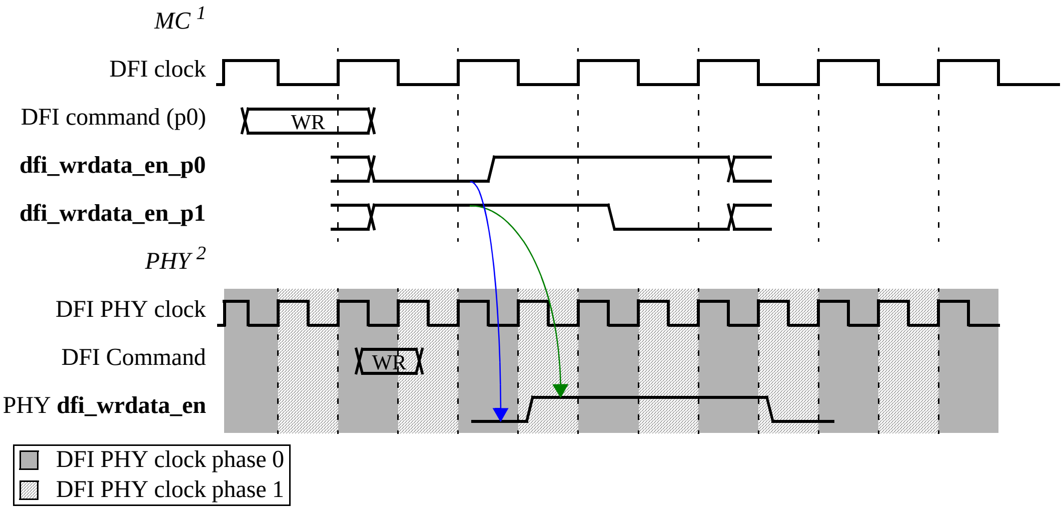
1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.8.3 Write Data Interface in Frequency Ratio Systems

The write data enable signal (**dfi_wrdata_en_pN**) indicates to the PHY that valid **dfi_wrdata** will be transmitted in $\mathbf{t_{phy\_wrdata}}$ DFI PHY clock cycles and its width defines the number of data phases of the write. In order to communicate this information to the PHY, the phase information must be encoded within the signal. Therefore, this signal is also vectored into multiple signals based on the frequency ratio. Similar to the DFI command, each signal is associated with a phase of the DFI PHY clock.

Figure 39 demonstrates how a vectored **dfi_wrdata_en_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system.

FIGURE 39. *1:2 Frequency Ratio Write Data Example*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

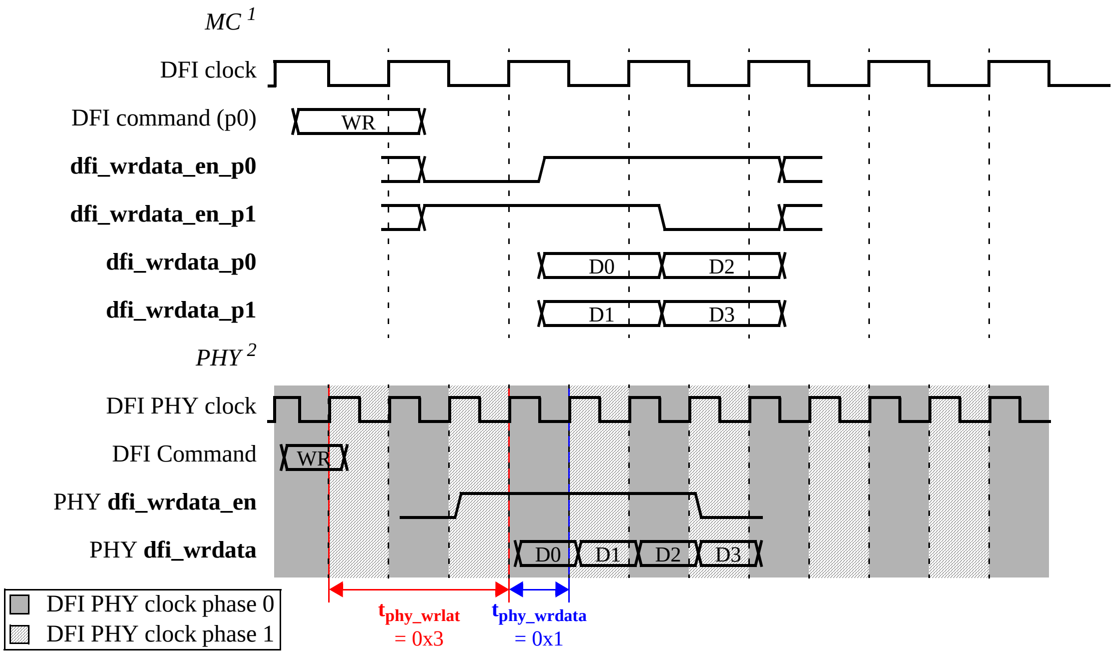
1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

For matched frequency systems, the DFI write data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, this DFI write data bus width is proportional to the frequency ratio to allow all of the write data that the memory requires to be sent in a single DFI clock cycle. The write data must be delivered with the DFI data words aligned in ascending order.

The timing parameters $\mathbf{t_{phy\_wrlat}}$ and $\mathbf{t_{phy\_wrdata}}$ apply in frequency ratio systems in the same way as in matched frequency systems. The $\mathbf{t_{phy\_wrlat}}$ parameter defines the delay from the write command to the **dfi_wrdata_en_pN** signal. The $\mathbf{t_{phy\_wrdata}}$ parameter defines the delay from the **dfi_wrdata_en_pN** signal to when data is driven on the **dfi_wrdata_pN** signal. These timing parameters are defined in terms of DFI PHY clocks and are measured relative to how the PHY interprets the data.

Figure 40 shows how data is received by the PHY in a situation where the data is sent aligned, but the enable signals are not aligned.

FIGURE 40. *1:2 Frequency Ratio Aligned Write Data Example*

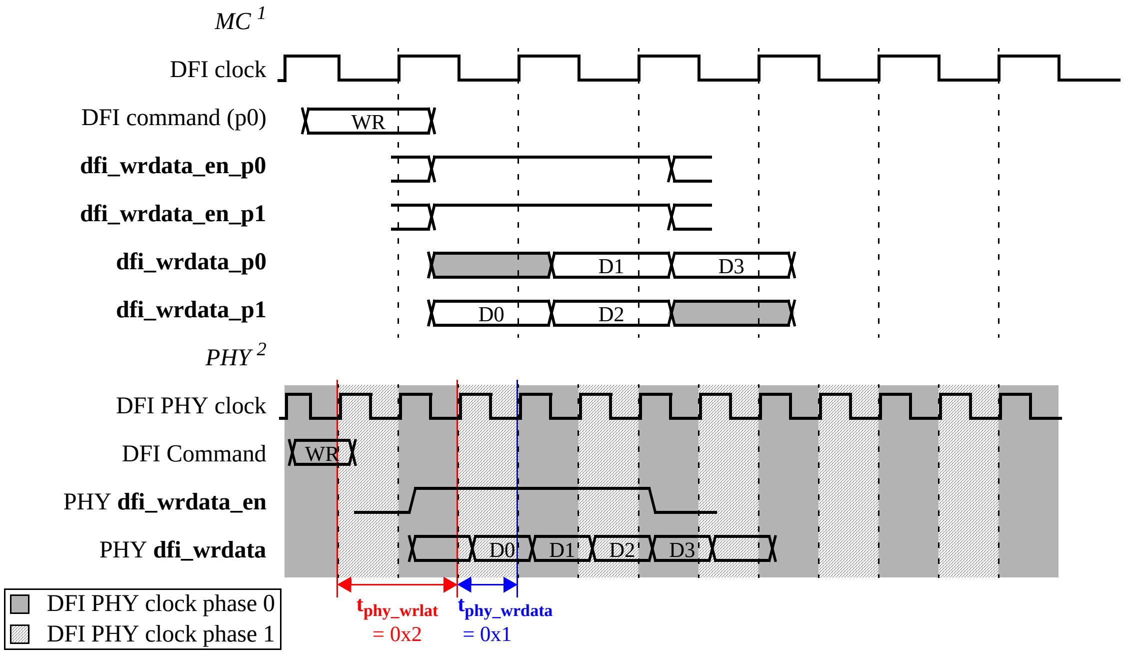


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

In Figure 41, the enable signals are sent aligned, but the data is not aligned. The MC sends the first beat of data on the phase 1 data signal. The write data must be sent un-aligned to achieve the proper relationship between the command and data.

FIGURE 41. *1:2 Frequency Ratio Aligned Write Enable Example*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock diagram.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.8.4 Read Data Interface in Frequency Ratio Systems

Similar to the write data enable signal, the read data enable signal (**dfi_rddata_en_pN**) defines the number of clocks between the read command and the read data, and its width defines the number of data phases of the read. The PHY sends read data to the MC on the **dfi_rddata_wN** buses whenever read data is available, asserting the associated **dfi_rddata_valid_wN** signals to inform the MC which buses contain valid data. Unlike the read data enable signal which correlates to the phase of the DFI PHY clock, the read data, read data valid and read data not valid signals are all vectored with the DFI data word suffix.

For matched frequency systems, the DFI read data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, this DFI read data bus width is proportional to the frequency ratio to allow all of the read data that the memory returns to be sent in a single DFI clock cycle. The read data must be delivered with the DFI data words aligned in ascending order.

For a 1:2 frequency ratio system, the read data bus is divided into 2 DFI read data words. For a 1:4 frequency ratio system, the read data bus is divided into 4 DFI read data words. Each DFI data word transfers a memory data word, the data associated with one rising and falling DQS. For example, in a 1:4 system with a memory data width of 32 bits, the DFI read data bus would consist of 4 64-bit DFI data words.

On a DFI clock, the PHY is permitted to assert any number of consecutive **dfi_rddata_valid_wN** signals that correspond to valid read data. However, the read data must be returned in a rolling order of DFI data words. For a 1:4 frequency ratio system, if read data is returned on the **dfi_rddata_w0** and **dfi_rddata_w1** buses on one DFI clock cycle, the next transaction must return data starting on the **dfi_rddata_w2** bus, regardless of the number of DFI data words being returned. If that next transaction returned 2 DFI data words, data must be returned on the **dfi_rddata_w2** and **dfi_rddata_w3** buses. If that next transaction returned 4 DFI data words, data must be returned on the **dfi_rddata_w2**, **dfi_rddata_w3**, **dfi_rddata_w0** and **dfi_rddata_w1** buses - in that order.

For a 1:2 frequency ratio system, read data must be returned in the same manner, in a rolling order of DFI data words. In this case, there are only 2 DFI data words in the DFI read data bus - **dfi_rddata_w0** and **dfi_rddata_w1**.

The rolling order rule must be followed regardless of whether the subsequent data transfer occurs on the next DFI clock or several clocks later. For LPDDR3 and LPDDR2 memory systems, the rolling order rule applies to both reads and mode register reads. The order is critical for the PHY and MC to correctly communicate read data. Each DFI data word must be used prior to sending data on the subsequent DFI data word, requiring data to be sent contiguously. The subsequent read data must be returned on the next DFI data word relative to the previous transaction. If the last transaction ended on **dfi_rddata_w2**, for example, the next transfer must begin on **dfi_rddata_w3**. Similarly, it is not legal to return read data on only the **dfi_rddata_w0** and **dfi_rddata_w2** buses.

Both the MC and the PHY must track which signals were used in the last transfer in order to interpret the data accurately. At initialization, the DFI data word pointer is set to 0, and the first read data returned is expected on the **dfi_rddata_w0** bus. During normal operation, certain procedures may affect the read data rotation, such as frequency changing, data training or gate training. Therefore, any assertion of the **dfi_init_start** signal, or a de-assertion of the **dfi_rdlvl_en** or **dfi_rdlvl_gate_en** signals must trigger a re-initialization of the DFI data word pointer to 0.

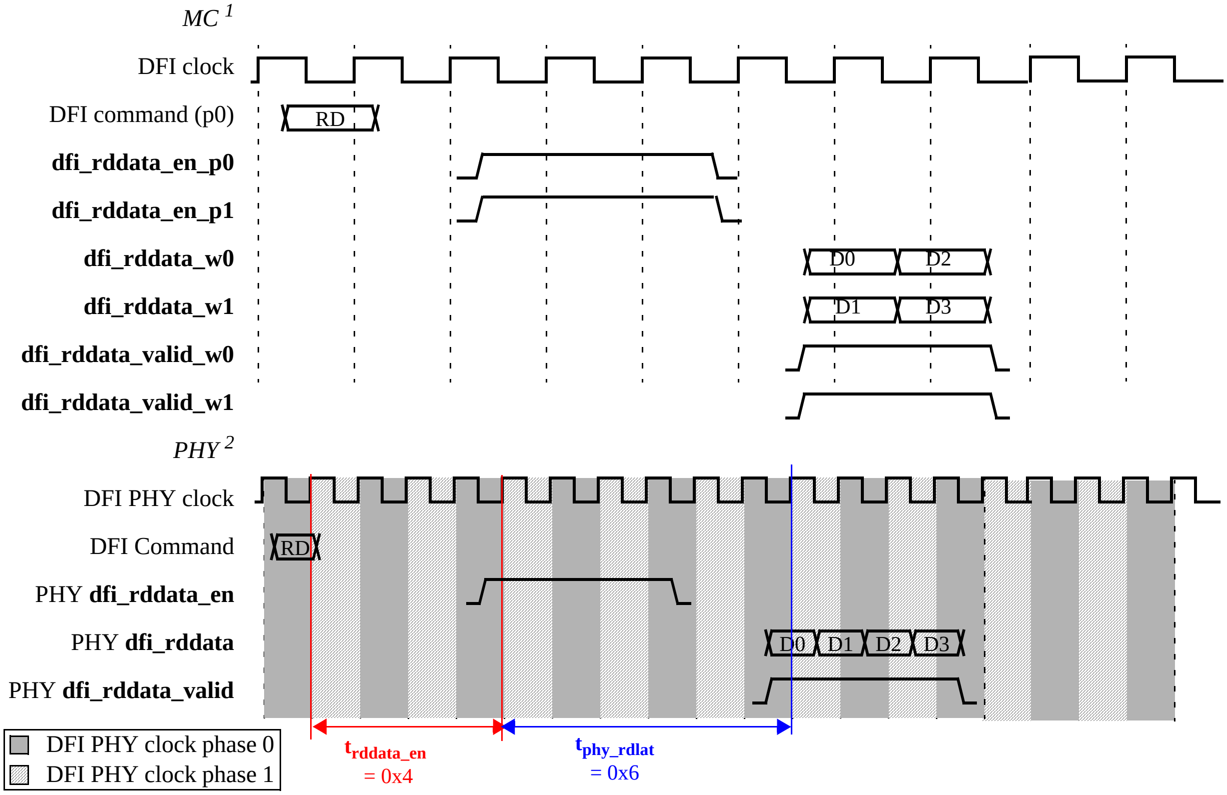
The rotational use of the **dfi_rddata_valid_wN** signals is only required in situations where the system may return less data than the DFI read data bus. If the minimum transfer size is a multiple of the DFI read data bus width, data can always be returned on all DFI data words and the **dfi_rddata_valid_wN** signals are all driven identically. Otherwise, only certain DFI data words of the DFI read data bus are used. In either case, the MC must be able to receive data in a rotating order based on the last transfer to be DFI compliant for frequency ratio. A PHY may optionally be implemented such that it always returns read data on the entire DFI read data bus per transaction.

Regardless of how the signals are vectored, the PHY may only change read data, read data valid and read data not valid signals during phase 0 of the DFI PHY clock to allow the MC the entire DFI clock period to capture the signal and read data.

The timing parameters $\mathbf{t_{rddata\_en}}$ and $\mathbf{t_{phy\_rdlat}}$ apply in frequency ratio systems in the same way as in matched frequency systems. These timing parameters define the delay from the read command to the **dfi_rddata_en_pN** signal, and from the **dfi_rddata_en_pN** signal to when data is returned on the **dfi_rddata_wN** bus, respectively. These timing parameters are defined in terms of DFI PHY clocks and are measured relative to how the PHY interprets the data.

Figure 42 demonstrates how a vectored **dfi_rddata_en_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system with an even value for the $\mathbf{t_{rddata\_en}}$ timing parameter, and where all DFI data words are returned on a DFI clock cycle.

FIGURE 42. *1:2 Frequency Ratio Single Read Data Example with Even Read Data to Enable Timing*



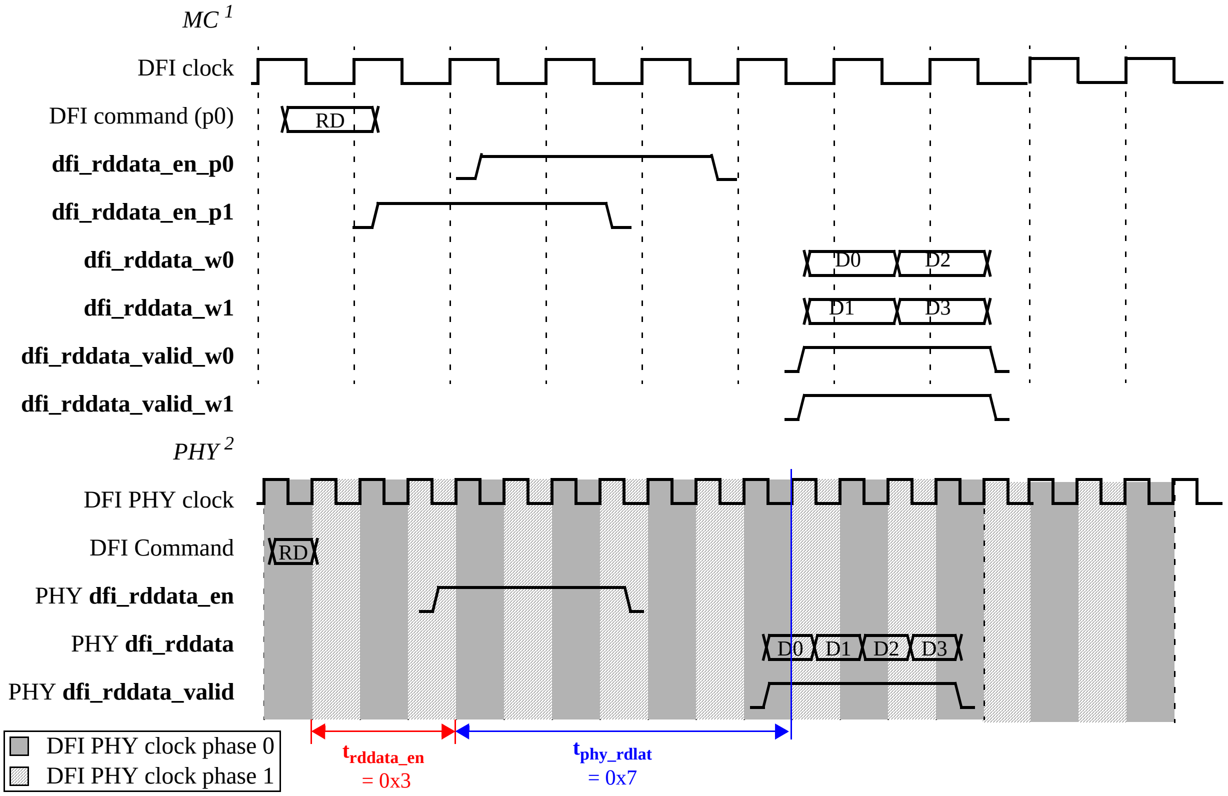
NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

Figure 43 demonstrates how a vectored **dfi_rddata_en_pN** signal is interpreted by the PHY in a 1:2 frequency ratio system with an odd value for the $\mathbf{t}_{\mathbf{rddata\_en}}$ timing parameter, and where all DFI data words are returned on a DFI clock cycle.

FIGURE 43. *1:2 Frequency Ratio Single Read Data Example with Odd Read Data to Enable Timing*



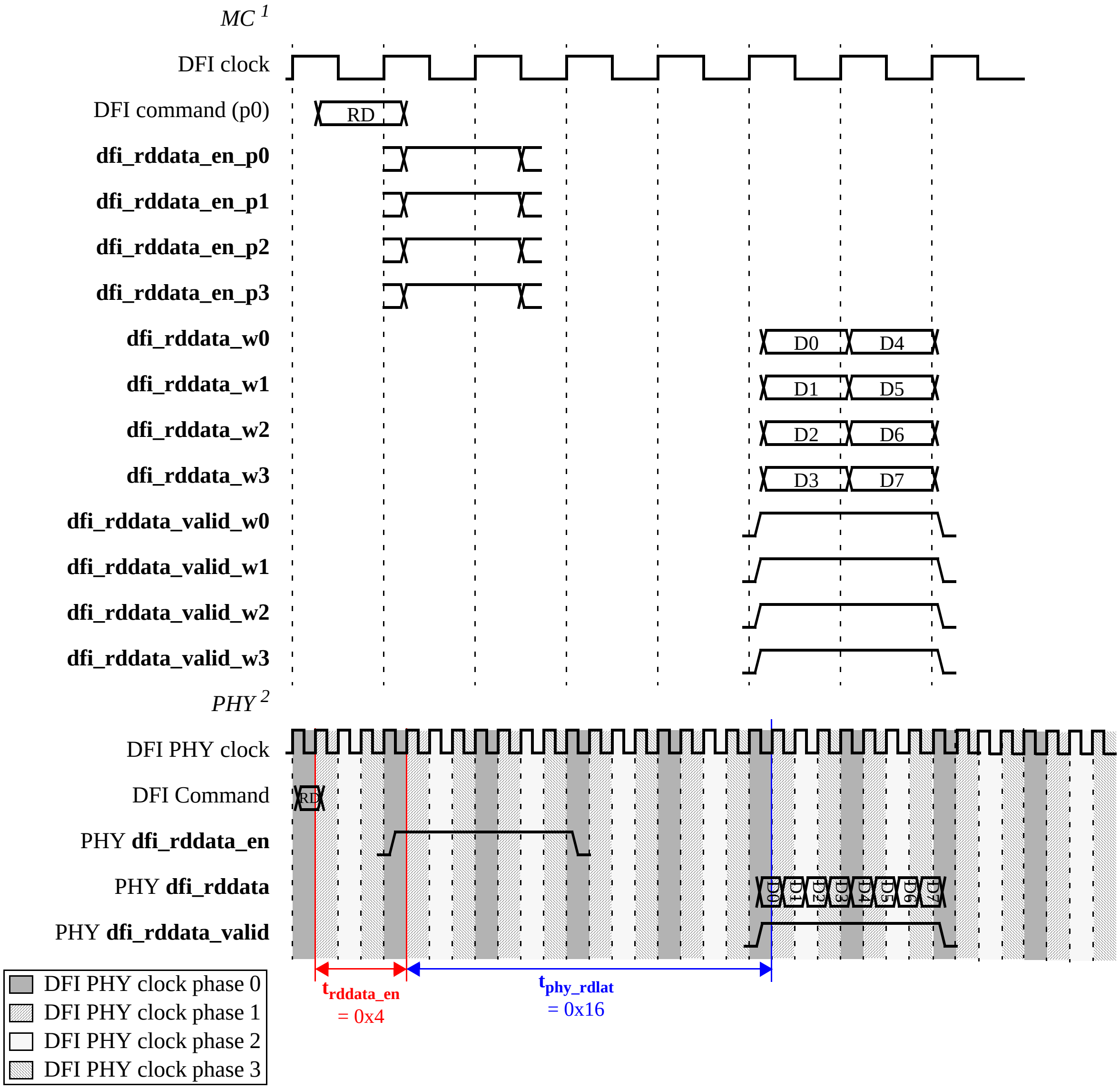
NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

Figure 44 demonstrates how a vectored **dfi_rddata_en_pN** signal is interpreted by the PHY in a 1:4 frequency ratio system where all DFI data words are being returned on a DFI clock cycle.

FIGURE 44. *1:4 Frequency Ratio Single Read Data Example*



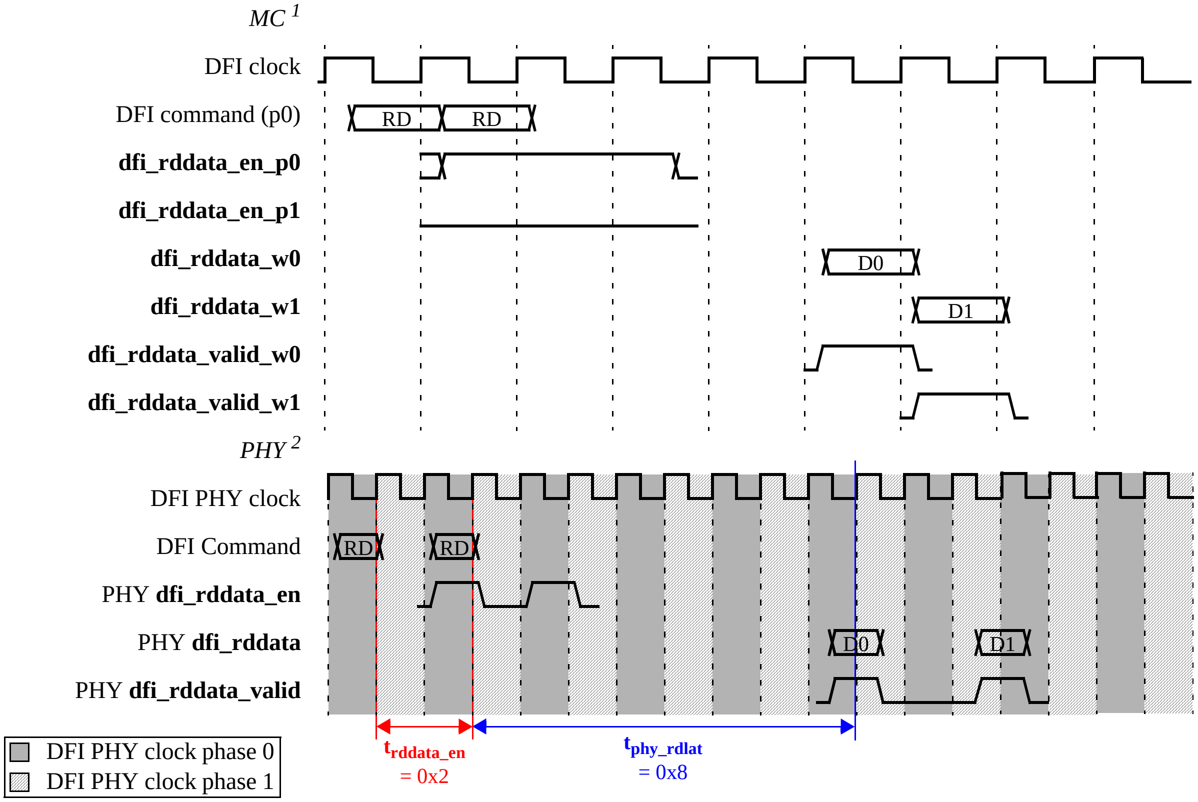
NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

Figure 45 returns a single DFI data word with each command. The data for the second read command is returned on the **dfi_rddata_w1** bus following the rotational order rule.

FIGURE 45. *1:2 Frequency Ratio Multiple Read Data Example*

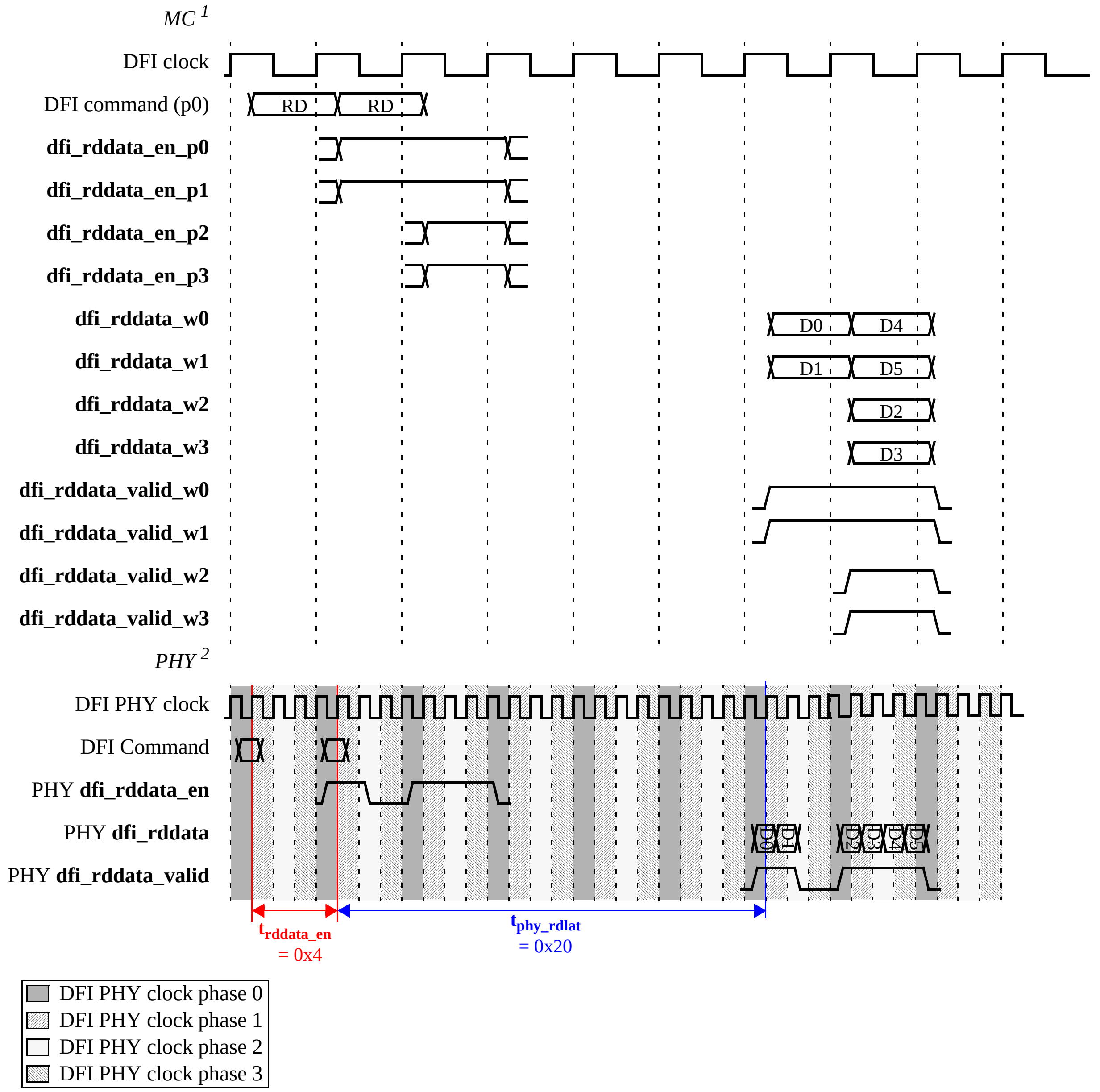


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

Similar to Figure 45, “1:2 Frequency Ratio Multiple Read Data Example”, Figure 46 shows a burst length 4 followed by a burst length 8 read. The data for the burst length 8 read command is returned starting on the **dfi_rddata_w2** bus following the rotational order rule.

FIGURE 46. *1:4 Frequency Ratio Multiple Read Data Example*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.8.4.1 DFI Read Data Rotation

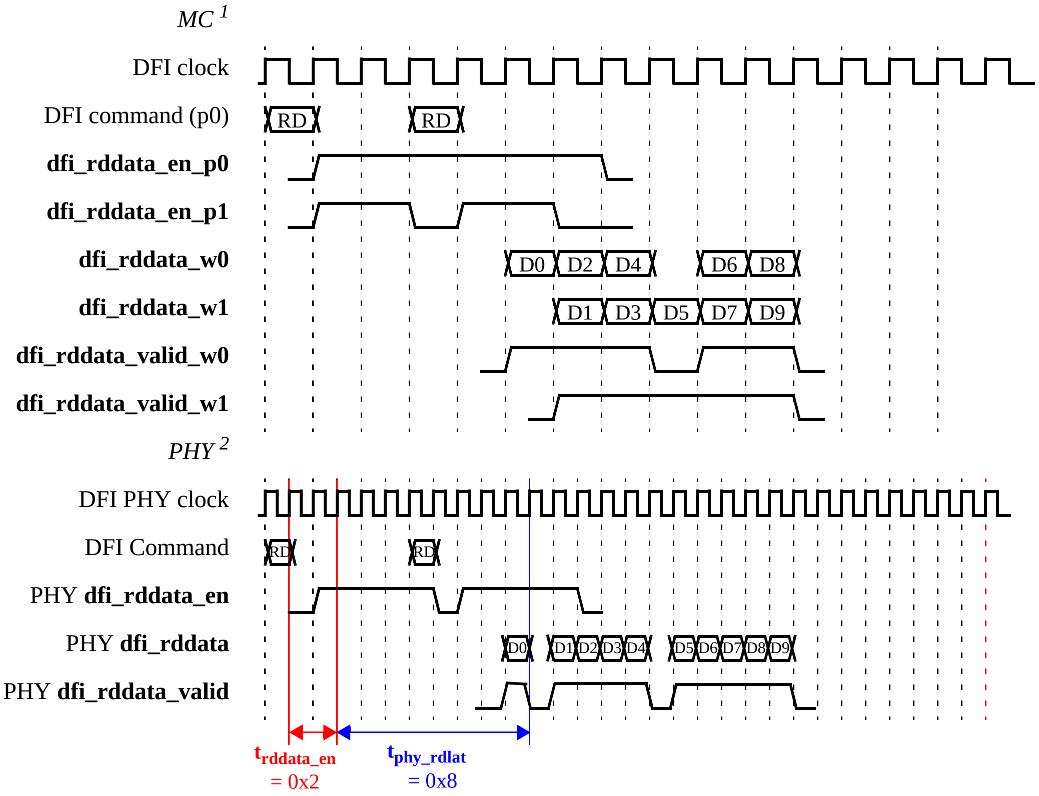
For simplicity, the following four diagrams illustrate different potential timing scenarios with a 1:2 frequency ratio system, transmitting 2 bursts of data, with each burst extended by one DRAM clock cycle.

Many DFI systems do not require support for burst transfers that are not a multiple of the frequency ratio. However, if a system does support these burst transfers, the PHY must transfer the read data in a rotating order as follows:

1. Figure 47, “DFI Read Data Bus for Two 10UI Bursts, each starting in Phase 0”
2. Figure 48, “DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 (trddata_en=2, tphy_rdlat=8)”
3. Figure 49, “DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 1”
4. Figure 50, “DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 (trddata_en=2, tphy_rdlat=10)”

Additionally, the MC must be able to capture this data correctly and correlate it to the proper read command.

FIGURE 47. *DFI Read Data Bus for Two 10UI Bursts, each starting in Phase 0*

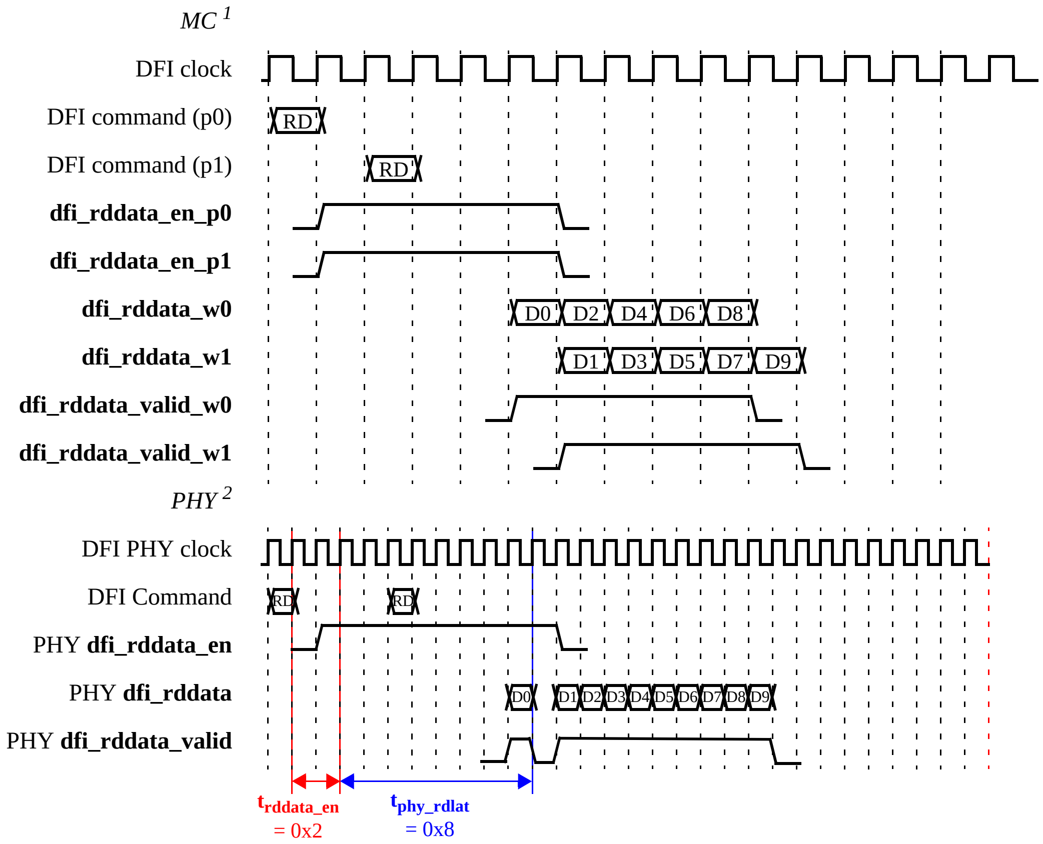


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain. In this figure, the signals are shown changing on the positive clock edge.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

FIGURE 48. *DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 (t_{rddata_en}=2, t_{phy_rdlat}=8)*

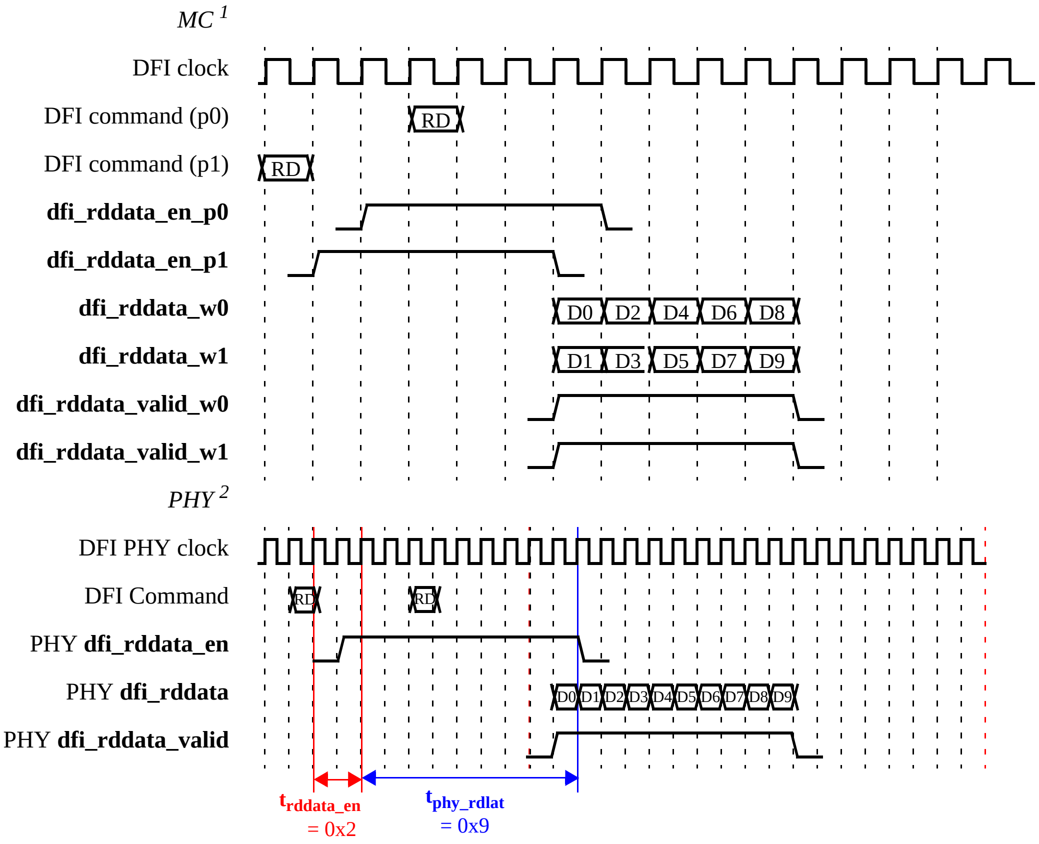


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain. In this figure, the signals are shown changing on the positive clock edge.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

FIGURE 49. *DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 1*

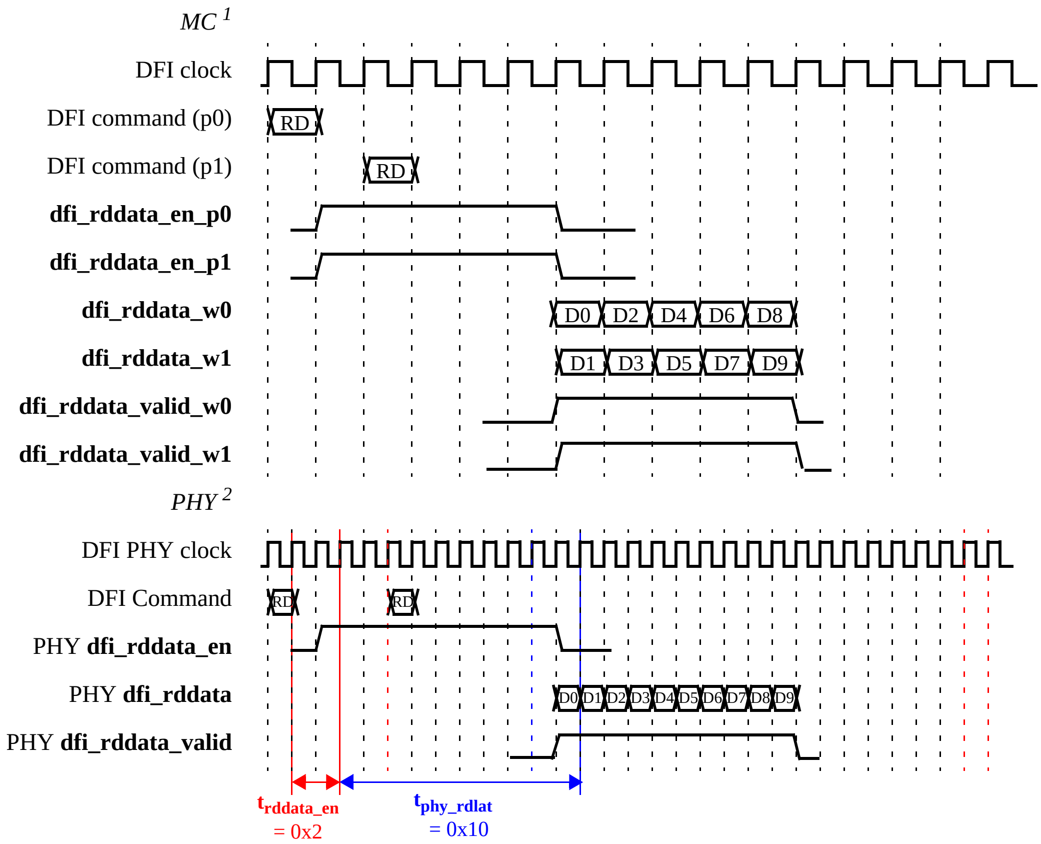


NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain. In this figure, the signals are shown changing on the positive clock edge.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

FIGURE 50. *DFI Read Data Bus for 10UI Back-to-Back Bursts Starting in Phase 0 (t_{rddata_en}=2, t_{phy_rdlat}=10)*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain. In this figure, the signals are shown changing on the positive clock edge.

1. In the MC clock diagram, the timing shows the DFI bus signalling.

2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.8.4.1.1 Read Data Resynchronization

When the read data rotation order is applicable, the MC and the PHY must maintain read data synchronization to properly interpret the read data order. If a condition occurs where the read data synchronization may be lost, a mechanism is necessary to resynchronize the devices. Conditions may include training or reporting an error. In order to be able to resynchronize when either the **dfi_ctrlupd_req** or **dfi_phyupd_ack** signals are asserted, reset the read data in a Frequency Ratio implementation in both the MC and PHY. Following the assertion of either the **dfi_ctrlupd_req** or **dfi_phyupd_ack** signal, the next read data word is always sent on **dfi_rddata_w0** regardless of the location of the previous data word.

4.9 Frequency Change

The DFI specification defines a frequency change protocol between the MC and the PHY to allow the devices to change the clock frequency of the memory controller and PHY without completely re-setting the system. The memory specifications define various memory states in which the clock frequency can be changed safely. The general procedure is to put the memory in one of these states, modify the clock frequency and re-synchronize the system. When the new clock frequency has been established, the PHY may need to re-initialize various circuits to the new clock frequency prior to resuming normal memory operation. Once complete, the memory system is ready to resume normal operation.

Frequency Change is an optional feature. The system may use a non-DFI frequency change method, or may choose to not support frequency change. However, if both the MC and the PHY intend to use the frequency change protocol, the MC and PHY must comply with the handshake defined by the DFI specification. The handshaking protocol defines the signals through which the MC and the PHY allow a frequency change to occur and also provides a means to abort the process if the PHY does not respond to a frequency change request. When a frequency change occurs, some of the DFI timing parameters may need to be changed.

NOTE: During the frequency change, the DFI clock must remain valid - either operating at a valid frequency or gated high or low.

The signals used in the frequency change protocol are **dfi_init_start,** asserted during initialization and in normal operation, and **dfi_init_complete**. For more information on these signals, refer to Section 3.5, “Status Interface”.

4.9.1 Frequency Change Protocol - Acknowledged

During normal operation, once the **dfi_init_start** and **dfi_init_complete** signal have been asserted, the system may change the DFI clock frequency. The MC asserts the **dfi_init_start** signal to indicate that a clock frequency change is being requested. The PHY should not interpret the initial **dfi_init_start** assertion as a frequency change request. When the **dfi_init_start** signal is asserted, the MC and the PHY must reset their DFI read data word pointers to 0.

The MC guarantees that the **dfi_init_start** signal remains asserted for at least $\mathbf{t_{init\_start}}$ cycles, allowing the PHY time to respond. The PHY may respond or ignore the frequency change request. To acknowledge the request, the **dfi_init_complete** signal must be de-asserted within $\mathbf{t_{init\_start}}$ cycles of the assertion of the **dfi_init_start** signal, or the opportunity for frequency change is withdrawn until the MC re-asserts this signal. The **dfi_init_complete** signal must de-assert at least one cycle before $\mathbf{t_{init\_start}}$ expires.

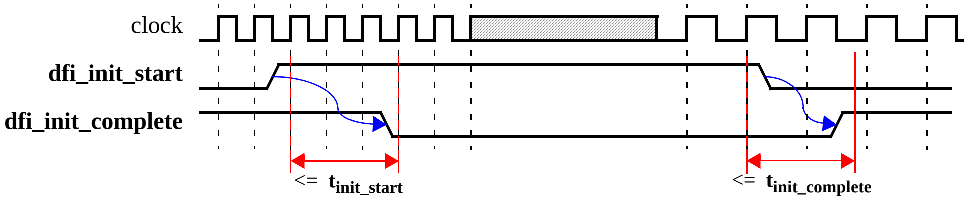
If the frequency change is acknowledged, the MC must hold the **dfi_init_start** signal asserted as long as the frequency change continues. Once the frequency change has completed, the MC de-asserts the **dfi_init_start** signal. The PHY must then complete any re-initialization required for the new clock frequency and re-assert **dfi_init_complete** within $\mathbf{t_{init\_complete}}$ cycles.

During a frequency change operation, the PHY must ensure that the memory interface is maintained at valid and stable levels throughout the operation to ensure that memory protocol is being observed. The MC must also insure that it maintains valid and stable levels on the DFI while **dfi_init_start** is asserted or **dfi_init_complete** is de-asserted.

Note that no maximum number of cycles for the entire cycle to complete is specified by the DFI.

Figure 51, “Frequency Change Acknowledge Timing Diagram” shows the MC holding the **dfi_init_start** signal asserted as long as the frequency change continues and the PHY re-asserting **dfi_init_complete** within $\mathbf{t_{init\_complete}}$ cycles.

FIGURE 51. *Frequency Change Acknowledge Timing Diagram*

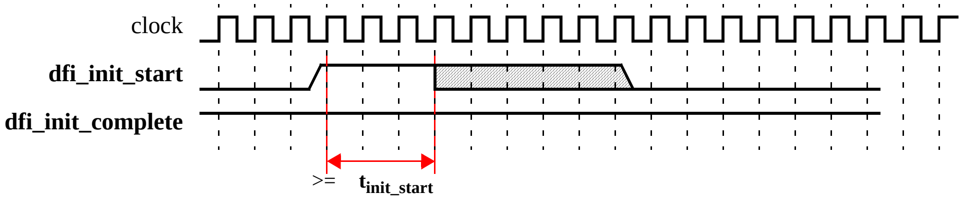


4.9.2 Frequency Change Protocol - Not Acknowledged

The MC must assert the **dfi_init_start** signal for at least $\mathbf{t_{init\_start}}$ cycles. It is important to note that the PHY is not required to respond to a frequency change request.

Figure 52, “Frequency Change Request Ignored Timing Diagram” shows the MC asserting the **dfi_init_start** signal for $\mathbf{t_{init\_start}}$ cycles.

FIGURE 52. *Frequency Change Request Ignored Timing Diagram*



4.10 CA Parity Signaling and CA Parity, CRC Errors

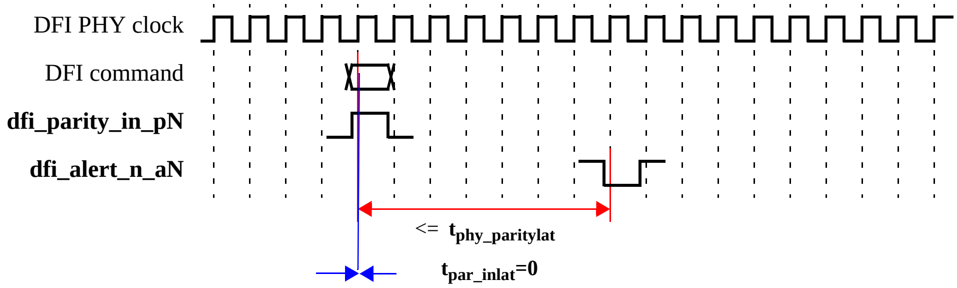
Parity bits are used in command transmission for verifying that the command has been transmitted correctly between master and slave. A single parity bit is sent with each command and identifies if the number of bits set high in the **dfi_address**, **dfi_act_n**, **dfi_bg**, **dfi_bank**, **dfi_cas_n**, **dfi_ras_n** and **dfi_we_n** signals is an even or an odd number. If the DRAM receives a command that the number of bits of these signals that is set to ‘b1 does not match the even/odd setting of the **dfi_parity_in** signal, an error occurred during transmission.

The MC sends the **dfi_parity_in signal**, which is valid for one cycle per command. The PHY must delay the **dfi_parity_in signal** identically to the command bus. Consequently, the PHY sends the **dfi_parity_in signal**, along with the command and other DFI signals, to the DRAM interface $\mathbf{t_{ctrl\_delay}}$ cycles after it receives the MC **dfi_parity_in** signal.

The **dfi_parity_in** signal is sent $\mathbf{t_{par\_inlat}}$ cycles after the DFI command; if $\mathbf{t_{par\_inlat}}$=0, **dfi_parity_in** and the DFI command are sent in the same cycle. The memory systems compute parity on the incoming command and compare the computed value with the value driven on the DFI parity signal. If these values do no match, the memory systems assert a parity error output, which is sent back to the PHY. The **dfi_alert_n** signal is asserted within $\mathbf{t_{phy\_paritylat}}$ cycles of the associated **dfi_parity_in** signal. Since $\mathbf{t_{phy\_paritylat}}$ is a maximum value, the **dfi_alert_n** signal can not be correlated to one specific command, but to any command sent within the last $\mathbf{t_{phy\_paritylat}}$ cycles.

Figure 53, "Odd Command Parity Error Example Timing Diagram" shows the timing between the command and error with an odd command parity example.

FIGURE 53. *Odd Command Parity Error Example Timing Diagram*



4.10.1 CA Parity Timing

The DFI protocol supports CA parity utilizing the **dfi_parity_in** signal to transmit the parity data across the DFI. The MC generates the **dfi_parity_in** signal and sends it across the DFI., The PHY transmits the signal to the memory subsystem, incorporating the same $\mathbf{t_{ctrl\_delay}}$ as the command bus.

In frequency ratio systems, the **dfi_parity_in** signal is defined per phase, similar to the CA bus. For example, in a 1:2 frequency ratio system, the parity data is sent on **dfi_parity_in_p0** and **dfi_parity_in_p1**.

To generalize the parity support for current and future parity implementations, the $\mathbf{t_{parin\_lat}}$ parameter, defined in Table 14, "Status Interface Signals," on page 43, specifies the timing of the **dfi_parity_in_pN** signal relative to the dfi command. The $\mathbf{t_{parin\_lat}}$ parameter, allows the parity data to be sent coincident with the command or on a subsequent cycle.

4.10.2 CA Parity and CRC Errors

The DRAM generates both CA parity and CRC errors. The error signals are transferred across the DFI bus to the MC. In systems that require CA parity or CRC support, the MC and PHY must both support the **dfi_alert_n_aN** error signal.

The active low **dfi_alert_n_aN** signal transmits both CA parity and write CRC errors. The PHY is not required to distinguish between a CA parity and a CRC error, instead, the PHY transmits the error to the MC for evaluation. The PHY holds the current state of the **dfi_alert_n_aN** signal until the PHY error input transitions to a new value. Consequently, the pulse width of **dfi_alert_n_aN** matches the pulse width of the DRAM subsystem error signal, plus or minus any synchronization cycles.

4.10.2.1 CA Parity and CRC Errors in Frequency Ratio Systems

With frequency ratio systems, multiple **dfi_alert_n_aN** outputs from the PHY are required to accurately transfer the error pulse width.

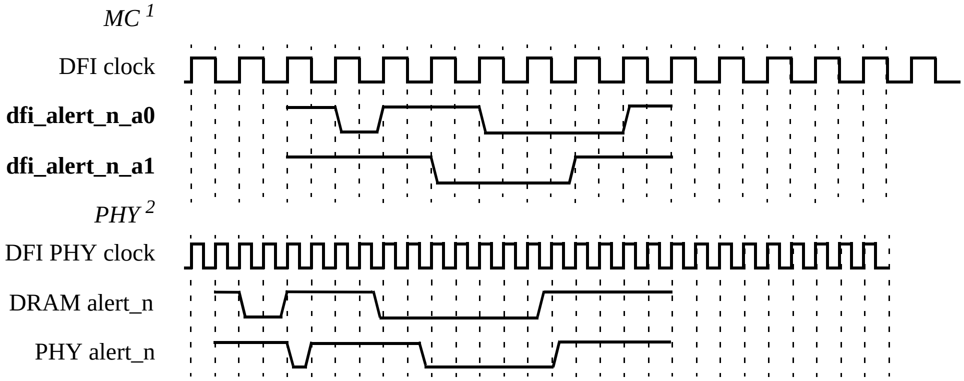
Table 24, “dfi_alert_n Signal With Matched and Frequency Ratio Systems,” on page 114 defines the outputs for matched frequency, 1:2 frequency, and 1:4 frequency systems. In all cases, the PHY must synchronize the **dfi_alert_n_aN** outputs to the DFI clock domain. During synchronization, the width of the DRAM error signal may change by a few cycles, and these small changes in the error pulse width are acceptable.

TABLE 24. ***dfi_alert_n*** *Signal With Matched and Frequency Ratio Systems*

System	Alert Outputs	Description
Matched Frequency	dfi_alert_n	Single Output Width of output indicates width of error pulse +/- synchronization errors.
1:2 Frequency	dfi_alert_n_a0 dfi_alert_n_a1	2 outputs, one for each phase of the DFI clock. Combination of signals is used for determining error pulse width. EXAMPLE: dfi_alert_n_a0 and dfi_alert_n_a1 are both asserted for one DFI clock period. The error signal width is 2 DRAM clocks +/- synchronization errors.
1:4 Frequency	dfi_alert_n_a0 dfi_alert_n_a1 dfi_alert_n_a2 dfi_alert_n_a3	4 outputs, one for each phase of the DFI clock. Combination of signals is used for determining error pulse width. EXAMPLE: **dfi_alert_n_a0, dfi_alert_n_a1, dfi_alert_n_a2,** and **dfi_alert_n_a3** are all asserted for one DFI clock period The error signal width is 4 DRAM clocks +/- synchronization errors. EXAMPLE: Only **dfi_alert_n_a1** and **dfi_alert_n_a2** are asserted for one DFI clock period The error signal width is 2 DRAM clocks +/- synchronization errors.

In Figure 54, “dfi_alert_n_aN with 1:2 Frequency Ratio”, the 1st assertion of the DRAM error signal (DRAM **alert_n**) is held for 2 DRAM clocks, but due to synchronization, only **dfi_alert_n_a0** is asserted on the DFI bus, indicating a single DRAM clock period pulse. The 2nd assertion of the DRAM error signal is held for multiple cycles, and the DFI output indicates this functionality by asserting both **dfi_alert_n_a0** and **dfi_alert_n_a1** as required. The **dfi_alert_n_a0** and **dfi_alert_n_a1 signals** correlate to the phase of the DFI clock. However, the assertion of **dfi_alert_n_a0** does not directly relate to the phase of assertion on the DRAM bus and therefore the assertion of **dfi_alert_n_a0** is not directly related to the phase of the write data.

FIGURE 54. ***dfi_alert_n_aN*** *with 1:2 Frequency Ratio*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signalling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.11 DFI Training Operations

DFI read and write training operations can increase accuracy of signal placement at higher speeds in DDR4, DDR3, LPDDR3, and LPDDR2 systems. CA training optimizes the CA bus setup and hold times relative to the memory clock.

The DFI has four training operations to support read training, write leveling, and CA training. “Read training” collectively refers to two operations, gate training and read data eye training. For more information on the training operations and to identify operations that correspond to specific devices, refer to Section 3.6, “DFI Training Interface,” on page 47.

For DFI compliance, the MC must support both “Non-DFI Mode” and “DFI Training Mode” for the applicable training operations; the PHY may support one mode for each applicable training operation and the mode is set per operation.

Support for the defined state of each programmable parameter must be defined by each device and may be implemented as programmable registers within the device. The parameter is defined as a single enable bit indicating whether or not the corresponding DFI training operation (gate training, read data eye training, write leveling, or CA training) is enabled.

In DFI training mode, the MC sets up the DRAM for gate training, read data eye training, write leveling, or CA training and periodically issues read commands, write strobes, or calibration commands as applicable. The PHY is responsible for determining the correct delay programming for each operation. The PHY evaluates the data returned from the commands, adjusts the delays and evaluates the results to locate the appropriate edges. The MC assists by enabling and disabling the leveling logic in the DRAMs and the PHY and by generating the necessary read commands, mode register reads or write strobes. The PHY informs the MC when it has completed training, which triggers the MC to stop generating commands and to return to normal operation.

The MC must complete all transactions in progress to memory prior to initiating any of the training operations. Once any of the enable signals are asserted, the PHY should immediately enable the associated logic. During training, the MC does not use the memory response from the PHY. Therefore the only relevant DFI timing parameters are $\mathbf{t_{rdlvl\_rr}}$ for read training, $\mathbf{t_{wrlvl\_ww}}$ for write leveling, and $\mathbf{t_{calvl\_cc}}$ for CA training. The timing parameter $\mathbf{t_{rdlvl\_rr}}$ defines the minimum number of cycles that the MC should wait between issuing reads for DDR4 and DDR3 memory systems or mode register reads for LPDDR3 and LPDDR2 memory systems. The timing parameter $\mathbf{t_{wrlvl\_ww}}$ dictates the minimum delay between write strobes. The timing parameter $\mathbf{t_{calvl\_cc}}$ dictates the minimum delay between calibration commands. The MC continues to drive subsequent commands every $\mathbf{t_{rdlvl\_rr}}$ cycles, or subsequent write strobes every $\mathbf{t_{wrlvl\_ww}}$ until the PHY drives all bits of the response signal (**dfi_rdlvl_resp** or **dfi_wrlvl_resp**) high.

Multiple training sequences can be defined, with the sequence information supplied by either the MC or the PHY. The MC must provide flexibility to run training sequences required by the PHY and should not dictate a set of sequences. The PHY determines the sequences necessary to accomplish training. Both the MC and the PHY need to be aware of the defined training sequences and the specific sequence required for each training operation.

Whether the MC or the PHY initiates the training sequence, the MC asserts the enable signal to initiate or accept the training sequence, and the MC holds the enable signal asserted until the current training operation completes. For information on how the MC defines the required training sequence, refer to Section 3.6.1, “Read Training Operation,” on page 48.

NOTE: The DFI training requires the MC to support the training sequences to the PHY by generating MRW commands, toggling the enable parameter, generating the appropriate strobe signals, and evaluating the response. The PHY is responsible for adjusting the DLL delays and evaluating the responses from memory. When the PHY is satisfied with the training sequence, a completion response is sent back to the MC. For more information on the operating modes, refer to Section 4.11.3, “Write Leveling,” on page 119.

For DDR4, training sequence accuracy is increased with a selection of encodings. The MC determines a sequence of up to four unique, non-default Multi-Purpose Register (MPR) values and formats and drives the **dfi_lvl_pattern** signal to communicate the sequence to the PHY to indicate the training pattern that is currently active.

In non-DFI mode, the PHY either does not support training or supports training independent of the DFI signaling. In non-DFI mode, the associated training interface is not used, and the MC should be capable of generating the required MRS commands to enter or exit the test modes of the DRAMs.

4.11.1 Initiating a Training Operation

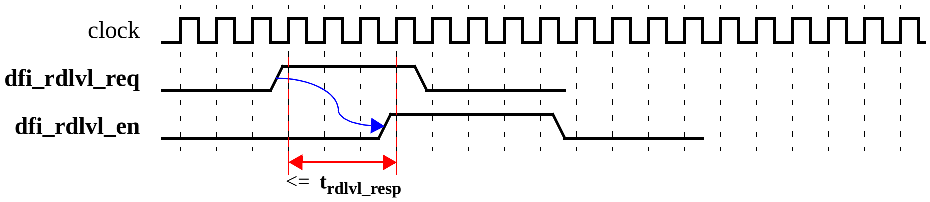
The MC or the PHY may initiate any training operation. Training may be executed during initialization, frequency change or during normal operation. The MC is responsible for initiating gate training, read data eye training, and/or write leveling required during initialization or frequency change. The PHY should not request training or leveling during initialization; if the PHY requests training during a frequency change, the PHY must assert it prior to asserting **dfi_init_complete**.

The PHY can request gate training by driving the **dfi_rdlvl_gate_req** signal. read data eye training by driving the **dfi_rdlvl_req** signal, or write leveling by driving the **dfi_wrlvl_req** signal.

The MC must respond to any of these requests by asserting the appropriate enable (**dfi_rdlvl_en**, **dfi_wrlvl_en** or **dfi_rdlvl_gate_en**) within the relevant $\mathbf{t_{rdlvl\_resp}}$ or $\mathbf{t_{wrlvl\_resp}}$ cycles.

Figure 55 shows this timing relationship for the data eye training process. The timing is similar for gate training and write leveling.

FIGURE 55. *Read Data Eye Training Request Timing*



The MC waits for the response signal to be asserted before disabling the active training logic. The response is always received on the **dfi_rdlvl_resp** or **dfi_wrlvl_resp** signals. The DFI specifies maximum times that the system waits for a response on the **dfi_rdlvl_resp** or **dfi_wrlvl_resp** signals as $\mathbf{t_{rdlvl\_max}}$ and $\mathbf{t_{wrlvl\_max}}$, respectively.

During read training, when **dfi_rdlvl_en** or **dfi_rdlvl_gate_en** is asserted, the MC will drive the target chip select on **dfi_rddata_cs_n**. During write leveling when **dfi_wrlvl_en** is asserted, the MC will drive the target chip select on **dfi_wrdata_cs_n.**

An MC supporting the DFI training mode in a system that supports independent training per chip select must support the data path chip selects **dfi_rddata_cs_n** and **dfi_wrdata_cs_n**, and the training chip select signals **dfi_phy_rdlvl_cs_n, dfi_phy_rdlvl_gate_cs_n,** and **dfi_phy_wrlvl_cs_n**. A PHY asserting the DFI training mode request optionally may support any combination of these signals. Any unused input signals should be tied inactive at the MC.

For more information on write leveling signals, refer to Figure 58, “Read Training in DFI Training Mode for LPDDR3 and LPDDR2 Memory Systems,” on page 119.

For more information on which signals are required and which signals are optional, refer to Table 2, “DFI Signal Requirements,” on page 18.

4.11.2 Read Training

“Read training” collectively refers to gate training and read data eye training.

The goal of gate training is to locate the setting at which the initial read DQS rising edge aligns with the rising edge of the read DQS gate. Once this setting is identified, the read DQS gate can be adjusted to the approximate midpoint of the read DQS preamble prior to the DQS.

To indicate proper alignment of the gate to the first read DQS, the gate training operation requires that the read DQS gate be placed within the bounds of the beginning of the read DQS preamble and the falling edge of the first read DQS. Placing the gate within the bounds of the timing window may require another alignment method or may require running gate training iteratively.

For an example of gate training, refer to Figure 56, “Gate Leading DQS Timing,” on page 118.

The gate training signals are: **dfi_rddata_en**, **dfi_rdlvl_gate_en**, **dfi_rdlvl_gate_req**, **dfi_rdlvl_resp** and the DFI command bus. The corresponding mode parameter is $\mathbf{phy}_{\mathbf{rdlvl\_gate\_en}}$. When the PHY initiates gate training, the PHY can optionally send the **dfi_phy_rdlvl_gate_cs_n** signal to indicate the targeted chip select. The MC transfers the **dfi_rddata_cs_n** signal to identify the chip select currently being trained.

The goal of data eye training is to identify the delay at which the read DQS rising edge aligns with the beginning and end transitions of the associated DQ data eye. By identifying these delays, the system can calculate the midpoint between the delays and accurately center the read DQS within the DQ data eye.

The read data eye training signals are: **dfi_rddata_en**, **dfi_rdlvl_en**, **dfi_rdlvl_req**, **dfi_rdlvl_resp** and the DFI command bus. The corresponding mode parameter is $\mathbf{PHY}_{\mathbf{rdlvl\_en}}$. When the PHY initiates data eye training, the PHY can optionally send the **phy_rdlvl_cs_n** signal to indicate the targeted chip select. The MC responds by executing training and transfers **dfi_rddata_cs_n** to indicate the chip select being trained.

From the MC perspective, the gate training and read data eye training operations are handled identically so both operations may be issued utilizing a single interface.For more information on the gate training and data eye training operations, refer to Section 3.3, “Read Data Interface,” on page 33 and Section 3.6, “DFI Training Interface,” on page 47.

Figure 56 is an example of gate training.

FIGURE 56. *Gate Leading DQS Timing*

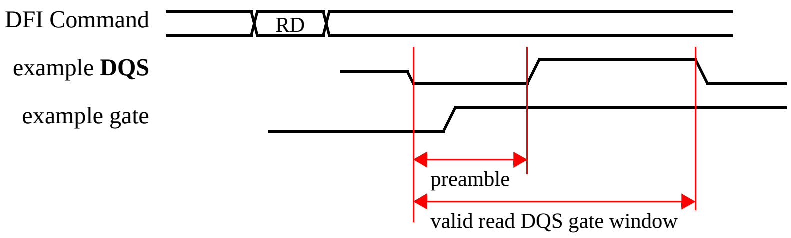
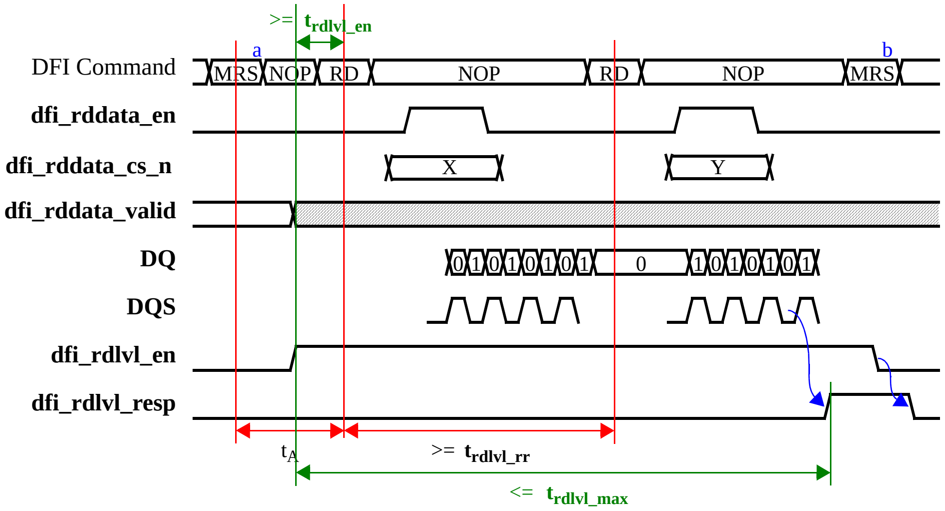


Figure 57 demonstrates read training in DDR4 and DDR3 memory systems. Figure 58 shows read training in LPDDR3 and LPDDR2 memory systems.

- DDR4, DDR3: MRS commands are used to enable and disable the read training logic in the DRAMs.
- LPDDR3, LPDDR2: No MRS commands are required to enable/disable the leveling mode in the DRAMs.

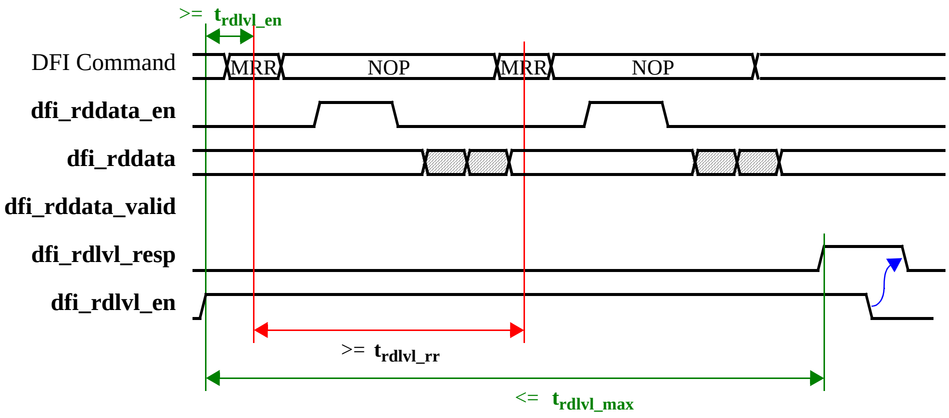
In both cases, the **dfi_rdlvl_en** signal is used for enabling or disabling the read training logic in the PHY. During read training, **dfi_rddata_valid** and **dfi_rddata** are ignored. All evaluations and delay changes are handled within the PHY. When the PHY has found the necessary edges and completed read training, the PHY drives the **dfi_rdlvl_resp** signal high, which informs the MC that the procedure is done. The MC then de-asserts the **dfi_rdlvl_en** signal. Once the **dfi_rdlvl_en** signal has de-asserted, the PHY may stop driving the **dfi_rdlvl_resp** signal.

FIGURE 57. *Read Training in DFI Training Mode for DDR4 and DDR3 Memory Systems*



a = Enables DRAM read training logic.
b = Disables DRAM read training logic.
t_A = Timing delays required by the DDR4 and DDR3 specifications.
X, Y = Target chip select.
NOTE: When **dfi_rddata_en** is asserted, **dfi_rddata_cs_n** must be set to the target chip select.

FIGURE 58. *Read Training in DFI Training Mode for LPDDR3 and LPDDR2 Memory Systems*



4.11.3 *Write Leveling*

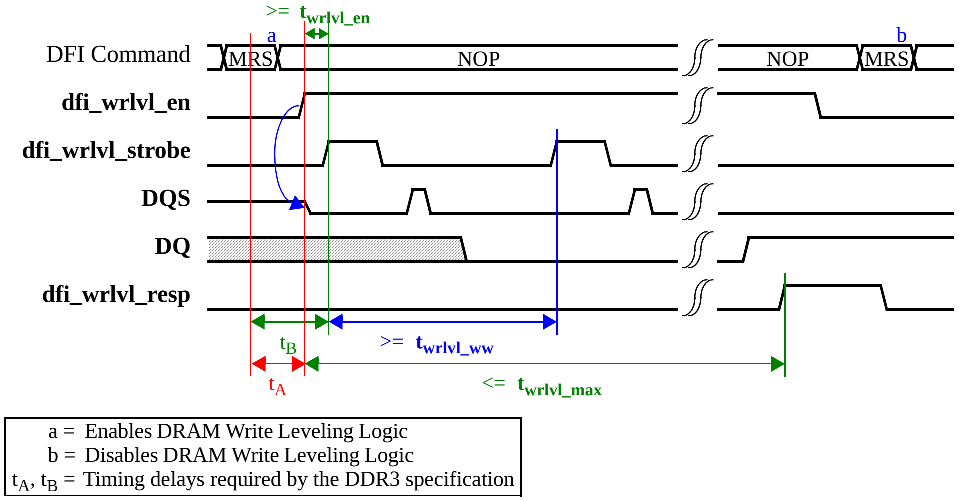
The goal of write leveling is to locate the delay at which the write DQS rising edge aligns with the rising edge of the memory clock. By identifying this delay, the system can accurately align the write DQS within the memory clock.

When the PHY initiates write leveling, the PHY can optionally send the **dfi_phy_wrlvl_cs_n** signal to indicate the targeted chip select. The MC transfers the signal to identify the chip select currently being trained. For more information on the write leveling parameter, refer to Section 3.6.2, “Write Leveling Operation,” on page 48.

The signals used in write leveling are: **dfi_wrlvl_en**, **dfi_wrlvl_req**, and **dfi_wrlvl_strobe**. The corresponding parameter is PHY_WRLVL_EN. The write leveling chip select signal is **dfi_phy_wrlvl_cs_n.** For more information on write leveling signals, refer to Section 3.2, “Write Data Interface,” on page 29.

Figure 59 demonstrates write leveling in DFI training mode. The MRS commands are used to enable and disable the write leveling logic in the DRAMs and the **dfi_wrlvl_en** signal is used for enabling or disabling the write leveling logic in the PHY.

FIGURE 59. *Write Leveling in DFI Training Mode*


>= t_{wrlvl_en}
a
b
DFI Command
MRS
NOP
NOP
MRS
dfi_wrlvl_en
dfi_wrlvl_strobe
DQS
DQ
dfi_wrlvl_resp
t_B
>= t_{wrlvl_ww}
t_A
<= t_{wrlvl_max}
a = Enables DRAM Write Leveling Logic
b = Disables DRAM Write Leveling Logic
t_A, t_B = Timing delays required by the DDR3 specification

4.11.4 CA Training

CA training optimizes the CA bus setup and hold times relative to the memory clock. A Mode Register Write (MRW) enables the CA training mode of operation in the memory. Two mode registers are defined to enter CA training to allow testing across the entire CA bus, and one mode register is defined to exit CA training. The DFI specification does not dictate the CA bus values driven during testing.

CA training expands the functionality of the **dfi_cke** signal (driven LOW to enable the memory to drive the CA value on the DQ bus) and the **dfi_cs_n** signal (used to generate a calibration command transferring the CA bus pattern to the memory). The CA pattern can be any value defined by the system for the purpose of training. The PHY can vary the delay settings of the command bus relative to the memory clock to determine the maximum setup and hold time settings.

The PHY may request CA training by asserting the **dfi_calvl_req** signal. The MC will respond to an assertion of the **dfi_calvl_req** signal by asserting the **dfi_calvl_en** signal within $t_{dfi\_calvl\_resp}$ cycles. The **dfi_calvl_en** signal enables the CA training logic in the PHY and begins the CA training sequence. During initialization or a frequency change operation, the MC should be configured to initiate CA training when necessary, but the PHY is not required to assert **dfi_calvl_req**.

If the PHY manages CA training during a frequency change, the **dfi_calvl_req** signal may be asserted while the **dfi_init_complete** signal is de-asserted, but must be asserted before or coincident with the assertion of the **dfi_init_complete** signal in order to guarantee that the training occurs prior to restarting normal command traffic.

4.11.4.1 CA Training Sequence

During CA training, the PHY is responsible for generating the CA patterns to be driven on the memory bus, adjusting the timing of the CA bus relative to the memory clock, and checking the CA pattern captured from the DQ bus against the expected CA pattern.

The CA training sequence can be initiated by either the PHY or the MC.

If the PHY requests CA training:

1. The PHY asserts the **dfi_calvl_req** signal.

   NOTE: This is an optional signal for the PHY since a PHY is not required to initiate CA training.
2. Within $\mathbf{t_{calvl\_resp}}$ DFI clock cycles, the MC is required to begin training.

CA training sequence:

1. The MC executes the MRW write commands to each memory to put the targeted chip select into the CA training state.
2. When the memory is in the CA training state, the MC asserts the **dfi_calvl_en** signal to indicate that the PHY should begin operating in the CA training mode.
3. The MC drives a background pattern on the **dfi_address** bus.
4. The $\mathbf{t_{calvl\_en}}$ timing parameter is met.
5. The MC must de-assert the **dfi_cke** signal for the target chip select.
6. The MC drives periodic CA training calibration commands, and the associated **dfi_address** bus command pattern, as defined by the $\mathbf{t_{calvl\_cc\_}}$ timing parameter.

   The background and command patterns must be configurable as required by the PHY and must be able to be changed for each separate assertion of the **dfi_calvl_en** signal. The patterns must remain unchanged as long as the **dfi_calvl_en** signal remains asserted.
7. The MC continues driving calibration commands until the **dfi_calvl_resp** signal indicates the training routine is complete.
8. The MC de-asserts the **dfi_calvl_en** signal and asserts the **dfi_cke** signal.
9. If additional training routines are required as part of the overall CA training sequence, the MC issues additional MRW commands as necessary for programming and re-asserts the **dfi_calvl_en** signal and associated commands for each training routine.
10. When the final routine of a sequence completes, the MC issues the MRW command to exit memory from the CA training state.

The PHY may either utilize the values being driven on the **dfi_address** bus or ignore these values and generate CA values by another method.

The PHY is responsible for specifying all of the patterns utilized on the CA bus during CA training. The DFI interface does not define the CA values to be driven during CA training or their means of communication.

Figure 60 illustrates the signal timing during a CA training routine including the calibration command timing, the background and command patterns driven on the **dfi_address** bus to produce the CA pattern desired on the memory interface, and the capture signal timing.

FIGURE 60. *CA Training Signaling*

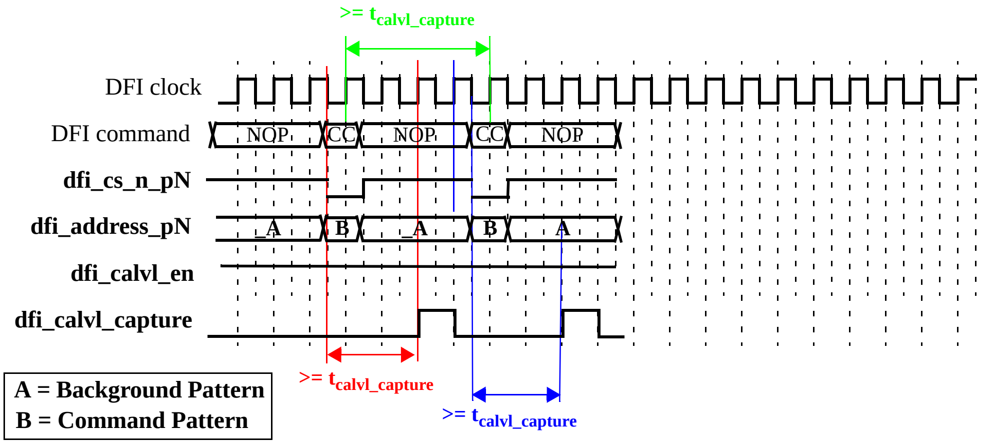


Figure 61 illustrates an MC-initiated CA training sequence. In this sequence, a single pattern is driven on the **dfi_address** bus during the entire sequence. After both segments of the CA bus are trained, the sequence is completed.

FIGURE 61. *MC-Initiated CA Training Sequence*

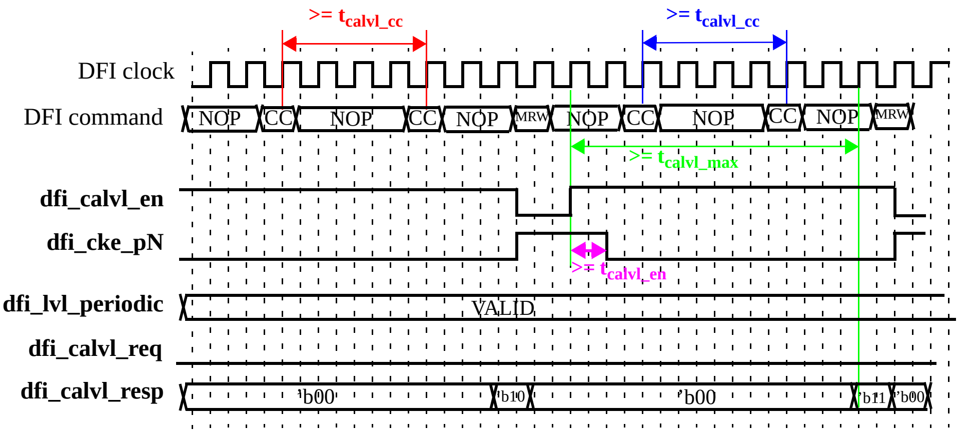


Figure 62 illustrates a PHY-initiated CA training sequence. The PHY requests the CA training and runs two separate routines to the same CA segment before transitioning to the next CA segment. The sequence continues beyond this diagram to train the upper CA segment.

FIGURE 62. *PHY-Initiated CA Training Sequence with Multiple Patterns per CA Segment*

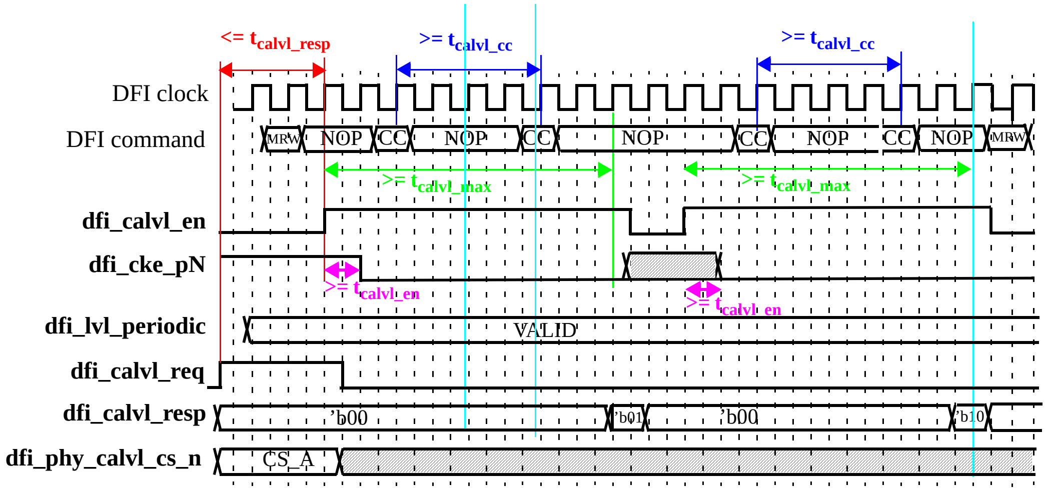
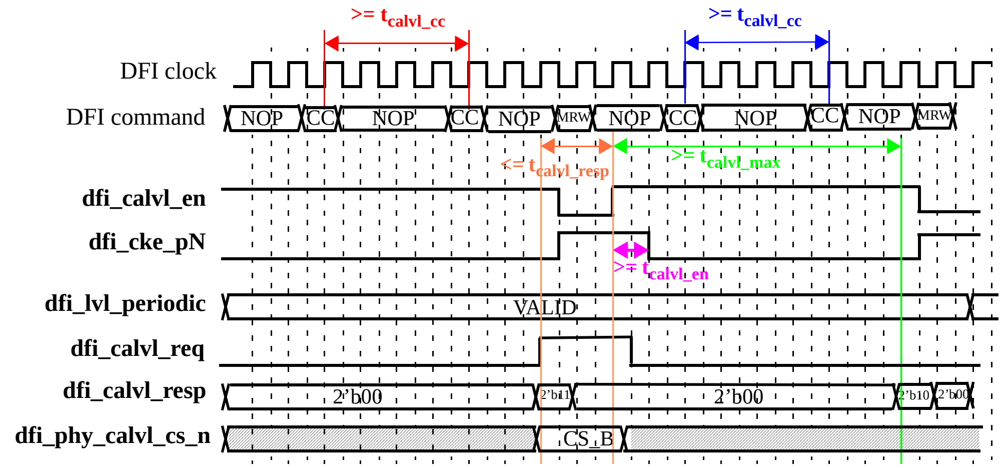


Figure 63 shows the training sequence continued to train another chip select.

FIGURE 63. *PHY-initiated CA Training Sequence - Completed*



4.11.5 dfi_lvl_pattern Encoding

In DDR4, LPDDR3, and LPDDR2 systems executing read training, the MC drives the **dfi_lvl_pattern** signal to define the required training sequence. The **dfi_lvl_pattern** signal must be valid when the enable signal is asserted for gate training and data eye training. Similar to the enable signal, the **dfi_lvl_pattern** signal may transition when training completes.

In DDR4 systems, the **dfi_lvl_pattern** signal encodes the required training sequences. The width of **dfi_lvl_pattern** is: (4 x DFI Read Leveling PHY I/F Width), with a 4-bit encoding defined per slice. The DDR4 encoding determines which MPR is accessed, which DRAM-defined MPR data format is used, and if a unique, non-default, pattern is utilized. The DFI bus does not define the unique patterns; the MPR signals contain a set of encodings which can be used to define unique patterns, with the MC and the PHY programming determining the specific patterns.

NOTE: The **dfi_lvl_pattern** signal must hold its value and not transition throughout the training sequence.

In Figure 64, “dfi_lvl_pattern Timing,” on page 125, ‘Sequence X’ can be any valid sequence defined by the valid **dfi_lvl_pattern** encodings. This value will indicate the pattern returned by the DRAM and evaluated by the PHY.

NOTE: If multiple sequences are required, the MC can assert **dfi_rdlvl_en** and/or **dfi_rdlvl_gate_en** multiple times with different values driven on **dfi_lvl_pattern**.

The **dfi_lvl_pattern** signal encoding supports both serial and staggered MPR formats without specific support for the parallel format. The non-default MPR value and format encodings can be used to select a parallel format if required. The **dfi_lvl_pattern** encodings support up to 4 unique, non-default, MPR values and formats for DDR4. These encodings, ‘b1000 to ‘b1011, can select an MPR number, value, and format to create a unique training sequence. For example, the ‘b1000 encoding, defined as Sequence 0, could select the following training sequence:

- MPR Number: MPR2
- MPR Value: 0x1111_1110
- MPR Format: Serial

A setting of 4’b0000 will select a DDR3-like MPR setting.

FIGURE 64. *dfi_lvl_pattern Timing*

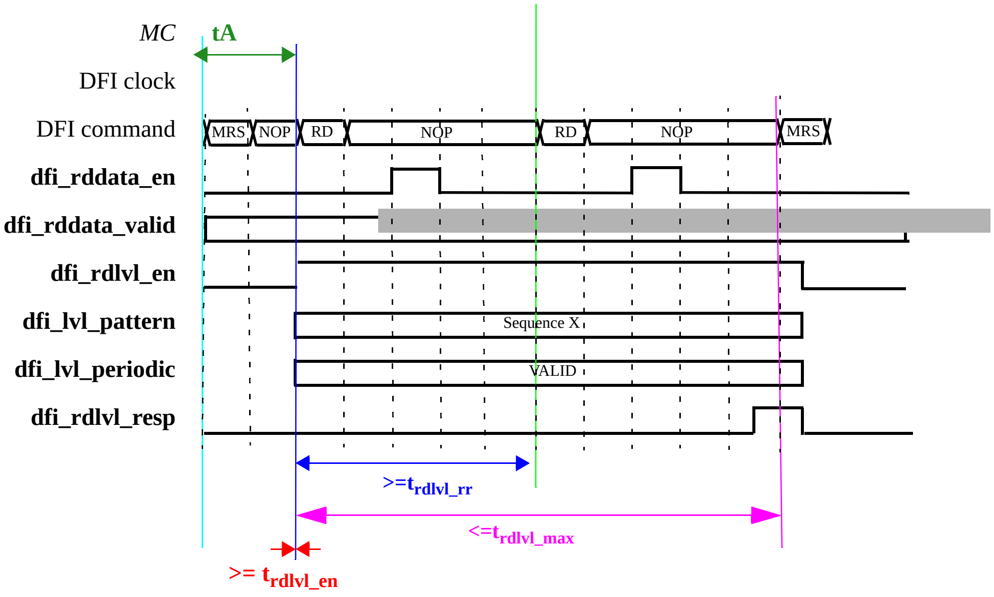


Table 25 is used for gate training and data eye training for DDR4 DRAMs.

TABLE 25. *DDR4 Encoding of dfi_lvl_pattern*

dfi_lvl_pattern					
Non-default	**Format**	**MPR**			
[3]	**[2]**	**[1]**	**[0]**	**Description**	
0	**0**	**0**	**0**	Serial format	Access MPR0
0	**0**	**0**	**1**	Default MPR Value	Access MPR1
0	**0**	**1**	**0**		Access MPR2
0	**0**	**1**	**1**		Access MPR3
0	**1**	**0**	**0**	Staggered format	Access starting with MPR0
0	**1**	**0**	**1**	Default MPR Value	Access starting with MPR1
0	**1**	**1**	**0**		Access starting with MPR2
0	**1**	**1**	**1**		Access starting with MPR3
1	**0**	**0**	**0**	Non-default MPR Value	Sequence 0
1	**0**	**0**	**1**	Any MPR	Sequence 1
1	**0**	**1**	**0**	Any format	Sequence 2
1	**0**	**1**	**1**	All defined programatically	Sequence 3

TABLE 25. *DDR4 Encoding of dfi_lvl_pattern (Continued)*

dfi_lvl_pattern				**Description**
Non-default	**Format**	**MPR**		
[3]	**[2]**	**[1]**	**[0]**	
1	**1**	**0**	**0**	Reserved for future use
1	**1**	**0**	**1**	
1	**1**	**1**	**0**	
1	**1**	**1**	**1**	

In LPDDR3 and LPDDR2 DRAMs, two DQ calibration mode registers are registered: MR32 and MR40. The mode registers produce two data calibration patterns defined in Figure 26, “Data Calibration Pattern,” on page 126.

TABLE 26. *Data Calibration Pattern*

Pattern	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
“A” (MR32)	**1**	**0**	**1**	**0**
“B” (MR40)	**0**	**0**	**1**	**1**

4.11.6 Support for Non-data Commands During Training

A PHY training sequence that exceeds the time the MC allows between refreshes or other required commands requires a method for executing these commands. This sequence must be supported by all MCs and PHYs supporting the DFI training interface for all supported DFI training sequences.

For DDR4 and DDR3, read training and write leveling require an MRW command to be issued to place memory in a data eye training (MPR) or write leveling operating mode. In either case, the memory specification does not permit any commands other than NOP and MRW while memory is in the special operating mode. Therefore, execution of a refresh will require issuance of an MRW to exit the special operating mode before executing the refresh command.

The sequence required to execute a refresh or other non-data command while running a read or write leveling sequence during training is:

1. Wait for the current command-to-command timing to complete ($\mathbf{t_{rdlvl\_rr}}$ or $\mathbf{t_{wrlvl\_ww}}$.
2. If required, execute an MRW to exit the training mode. In all cases, maintain the assertion of the training enable signal (**dfi_rdlvl_en**, **dfi_rdlvl_gate_en**, or **dfi_wrlvl_en**).
3. Execute a refresh or other non-data command.
4. If required, execute an MRW to re-enter the identical training state previously occupied.
5. Continue training sequence after meeting all timing requirements associated with MRW-to-command timing as defined at the beginning of the sequence.

Maintaining the assertion of the enable signal (**dfi_rdlvl_en**, **dfi_rdlvl_gate_en**, or **dfi_wrlvl_en**) allows the PHY to distinguish the exit portion of this command sequence from an aborted training sequence and the enter portion of this command sequence from the start of a new sequence.

Figure 65, “Refresh Execution During Read Training Operation” shows that the PHY should continue the training from the point where it was interrupted. Since the PHY did not assert the response signal (**dfi_rdlvl_resp** or **dfi_wrlvl_resp**), the sequence is not complete.

Figure 66, “Refresh Execution During Read Training Operation With Completion Response” shows that if the response is asserted any time during the refresh sequence, the training sequence should be completed as previously defined.

The training sequences may require the MC to maintain certain signal states while training is in progress. For example, during write leveling the MC may drive ODT. When exiting the training sequence to execute a non-data command such as a refresh, the MC may need to change the state of such signals as appropriate for the commands being executed.

FIGURE 65. *Refresh Execution During Read Training Operation*

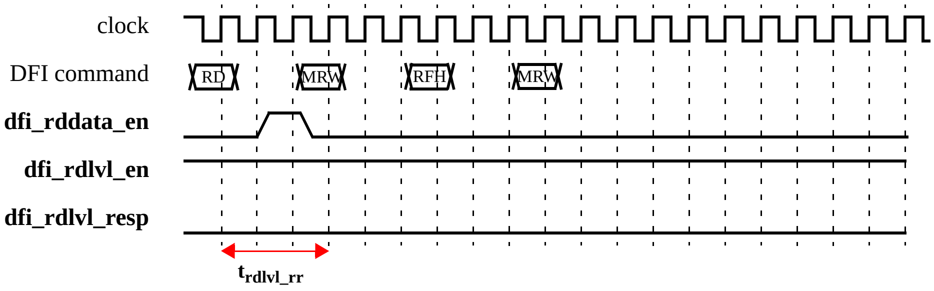
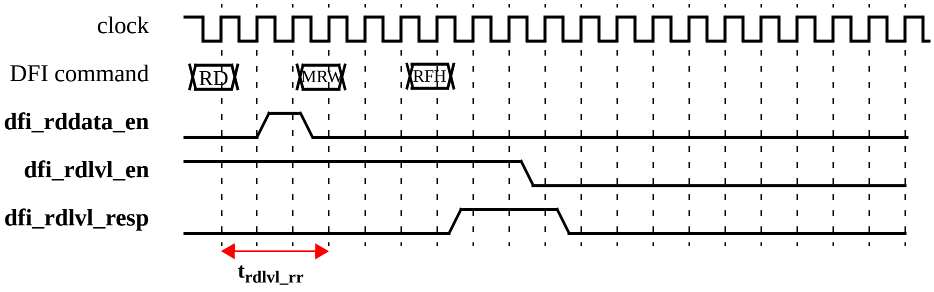


FIGURE 66. *Refresh Execution During Read Training Operation With Completion Response*



4.11.7 PHY-Requested Training Sequence

To execute PHY-requested training to a given chip select, the PHY asserts the **dfi_phylvl_req_cs_n[x]** associated with the chip select, and the MC grants the bus to the PHY for training using the following sequence:

1. The MC places the DRAM associated with the requested chip select in the IDLE state.
2. The MC idles the DFI bus.
3. The MC asserts **dfi_phylvl_ack_cs_n[x]**.
4. The PHY may assert multiple **dfi_phylvl_req_cs_n[x]** signals if there are multiple chip selects requiring training.

5. The MC may assert any number of **dfi_phylvl_ack_cs_n[x]** signals in response.

   An MC that does not support per-chip select logic for this interface may assert ALL **dfi_phlvl_ack_cs_n[x]** signals in unison in response to ANY **dfi_phylvl_req_cs_n[x]** signal (provided the MC follows the sequence of closing pages and waiting for commands to complete across all chip selects before asserting the **dfi_phlvl_ack_cs_n[x]** signal). The **dfi_phlvl_ack_cs_n[x]** signal must assert within $\mathbf{t_{phylvl\_resp}}$ clock cycles of the assertion of the associated **dfi_phylvl_req_cs_n[x]** signal.

   When one or more **dfi_phylvl_ack_cs_n** signals are asserted, the PHY is prohibited from asserting additional **dfi_phylvl_req_cs_n** signals.

When the PHY completes training for a given chip select, the PHY uses the following sequence:

1. The PHY de-asserts the **dfi_phylvl_req_cs_n[x]** signal associated with the specific chip select.
2. The MC de-asserts the **dfi_phylvl_ack_cs_n[x]** signals as soon as possible after all **dfi_phylvl_req_cs_n** signals are de-asserted.

If there are multiple **dfi_phylvl_req_cs_n[x]/dfi_phylvl_ack_cs_n[x]** pairs asserted simultaneously, the PHY may optionally de-assert **dfi_phylvl_req_cs_n** for each chip select as the training for each chip selects completes; if the PHY does de-assert one **dfi_phlvl_req_cs_n** out of multiple **dfi_phylvl_req_cs_n/dfi_phylvl_ack_cs_n** pairs asserted together, the MC has the option to de-assert the associated **dfi_phy_lvl_ack_cs_n** or to wait until all **dfi_phylvl_req_cs_n** signals are de-asserted. The MC must de-assert ALL **dfi_phylvl_ack_cs_n[x**] signals at least one cycle prior to sending any commands to DRAM.

The following rules must be followed to address the corner cases possible between **dfi_phylvl_req_cs_n[x]** and **dfi_phyupd_req:**

1. The PHY may assert **dfi_phylvl_req_cs_n[x]** and **dfi_phyupd_req** simultaneously.
2. The MC may assert any number of **dfi_phylvl_ack_cs_n[x]** or **dfi_phyupd_ack** signals, but it may not assert both signals simultaneously. If both **dfi_phylvl_req_cs_n[x]** and **dfi_phyupd_req** signals are asserted simultaneously, it might not be possible to satisfy both $\mathbf{t_{phylvl\_resp}}$ and $\mathbf{t_{phyupd\_resp}}$ timing parameters, so the MC is required to satisfy only one of them, depending on which request is acknowledged. After the MC has de-asserted one of the acknowledge signals, it must then assert the other acknowledge signal, if the corresponding request is still asserted.
3. During training, the PHY is responsible for issuing refreshes to satisfy all SDRAM refresh requirements for all supported chip selects in the system.

In Figure 67, “Training Chip Select #0, Controller gives 1 ACK,” on page 129 and Figure 68, “Training Chip Select #0, Controller Gives all ACKs,” on page 129, the PHY waits at time period “A” while the MC completes ongoing reads/ writes and closes open pages in chip select 0. The PHY owns the command bus to the DRAM and issues all commands required to train in time period “B”.

FIGURE 67. *Training Chip Select #0, Controller gives 1 ACK*

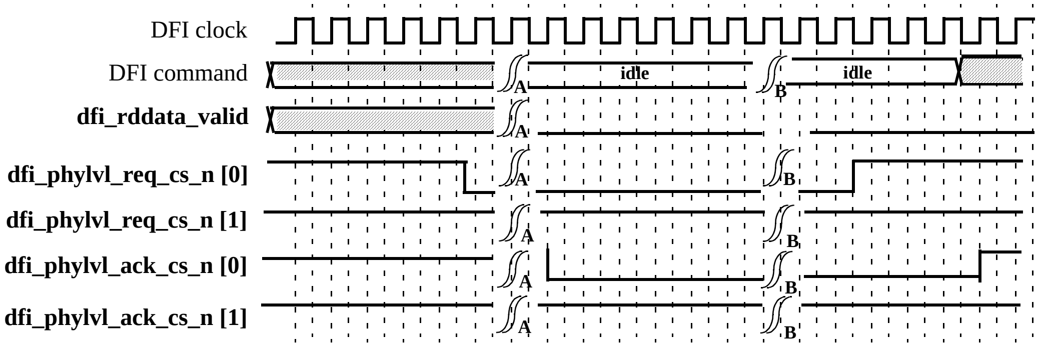
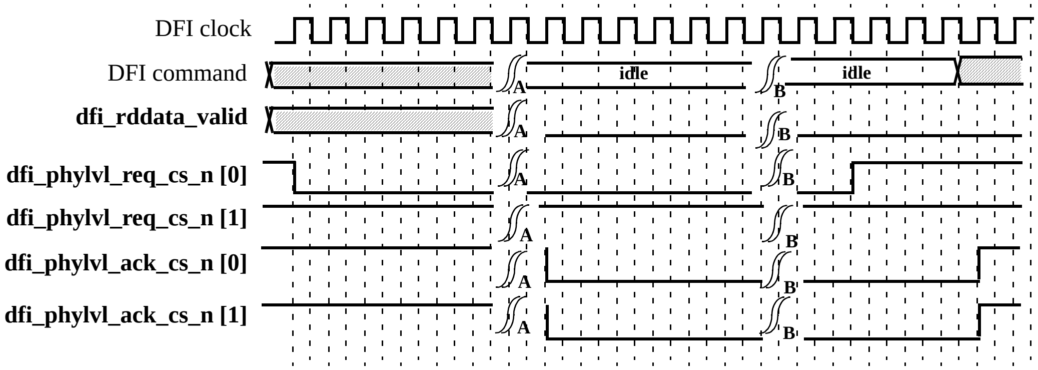


FIGURE 68. *Training Chip Select #0, Controller Gives all ACKs*



4.12 Low Power Control Handshaking

If the PHY has knowledge that the DFI will be idle for a period of time, the PHY may be able to enter an MC-initiated low power state. During low power handshaking, the DFI clock must maintain a valid and constant clock operating frequency until **dfi_lp_data_req**, **dfi_lp_ack**, and **dfi_lp_wakeup** have reached a constant state.

When the MC detects an idle time, the MC asserts the **dfi_lp_data_req** signal to the PHY and the **dfi_lp_wakeup** signal with the wakeup time required. The PHY can acknowledge the request and go into low power mode based on the wakeup time required and remain in low power mode as long as the request and acknowledge are both asserted, or the PHY can disregard the request and not change power states even if a low power opportunity request was acknowledged.

If the request is acknowledged through the assertion of the **dfi_lp_ack** signal, the PHY may enter a low power mode as long as the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal remains asserted. Once the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is de-asserted, the PHY must return to normal operating mode within the number of cycles indicated by the **dfi_lp_wakeup** signal.

When **dfi_lp_ctrl_req** or **dfi_lp_data_req** and **dfi_lp_ack** have asserted, the MC will not de-assert **dfi_lp_ctrl_req** or **dfi_lp_data_req** to increase the wakeup time. In order for the PHY to recognize that the MC has increased the wakeup time, the PHY must monitor the **dfi_lp_wakeup** signal.

Wakeup time is a specific number of cycles ($\mathbf{t_{lp\_wakeup}}$ cycles) in which the PHY is expected to respond to a signal change (the de-assertion of either the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal) on the DFI. If **dfi_lp_ctrl_req** and **dfi_lp_data_req** signals are both asserted, both must be de-asserted at the same time. The DFI specification defines up to 16 different wakeup times; neither the MC nor the PHY are required to support all of the defined wakeup times. Generally, the PHY should enter the lowest supported power state that allows low power exit within the required wakeup time. The wakeup time may be an average or estimated delay; therefore, exceeding the wakeup time should not be treated as an error condition.

The MC guarantees that **dfi_lp_ctrl_req** or **dfi_lp_data_req** will be asserted and the **dfi_lp_wakeup** signal will be constant for at least $\mathbf{t_{lp\_resp}}$ cycles, allowing the PHY time to respond. The PHY may respond or ignore the low power mode request. To acknowledge the request, the PHY must assert the **dfi_lp_ack** signal within $\mathbf{t_{lp\_resp}}$ clock cycles of the request signal assertion, during which time the MC must hold the **dfi_lp_wakeup** signal constant. Once the request has been acknowledged by the PHY, the MC may de-assert the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal. The PHY is expected to de-assert the **dfi_lp_ack** signal within $\mathbf{t_{lp\_wakeup}}$ clock cycles after the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is de-asserted and be ready for normal operation.

Figure 69, "Low Power Control Handshaking Timing Diagram" shows a sequence in which the request is acknowledged.

FIGURE 69. *Low Power Control Handshaking Timing Diagram*

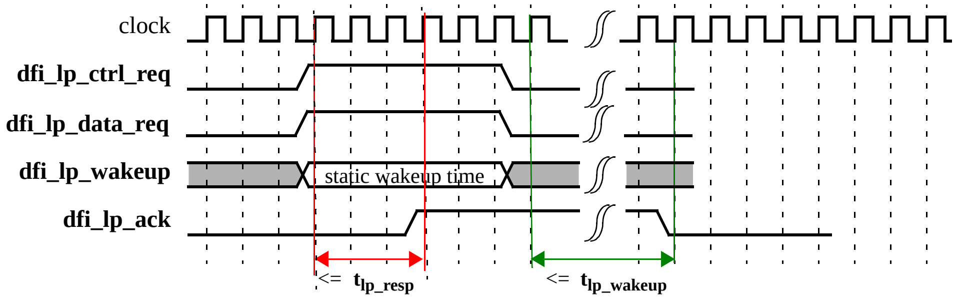
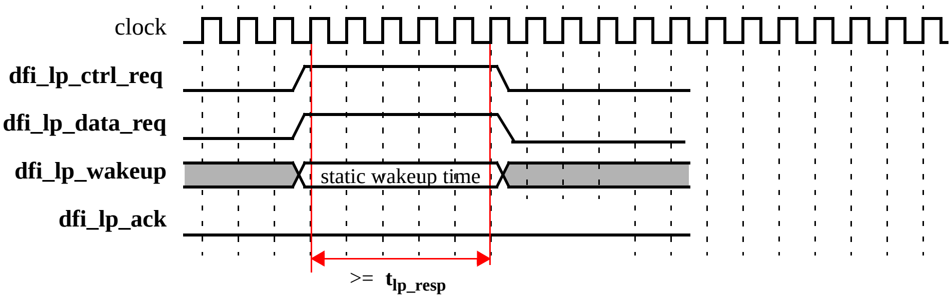


Figure 70, "Low Power Control Request with No Response" shows that the **dfi_lp_ack** signal is not required to assert when the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is asserted. The MC must assert the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal for at least $\mathbf{t_{lp\_resp}}$ cycles. If the **dfi_lp_ack** signal is not asserted within $\mathbf{t_{lp\_resp}}$ cycles, the PHY must not assert the acknowledge for the current request. The **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal should be de-asserted after $\mathbf{t_{lp\_resp}}$ cycles have elapsed without an acknowledge.

FIGURE 70. *Low Power Control Request with No Response*



After the request has been acknowledged, the MC may increase the time that the PHY has to respond beyond the time that was initially defined. The MC is allowed to change the **dfi_lp_wakeup** signal to a larger value as long as both the **dfi_lp_ack** and **dfi_lp_ctrl_req** or **dfi_lp_data_req** signals are asserted. This results in a longer $\mathbf{t_{lp\_wakeup}}$ time for the PHY. The value of the **dfi_lp_wakeup** signal when the **dfi_lp_ctrl_req** or **dfi_lp_data_req** signal is de-asserted will be used to define the $\mathbf{t_{lp\_wakeup}}$ time.

Figure 71, "Low Power Control Handshaking Timing Diagram with Multiple Wakeup Times" shows a scenario with the assumption that the wakeup time is increased with each change.

FIGURE 71. *Low Power Control Handshaking Timing Diagram with Multiple Wakeup Times*

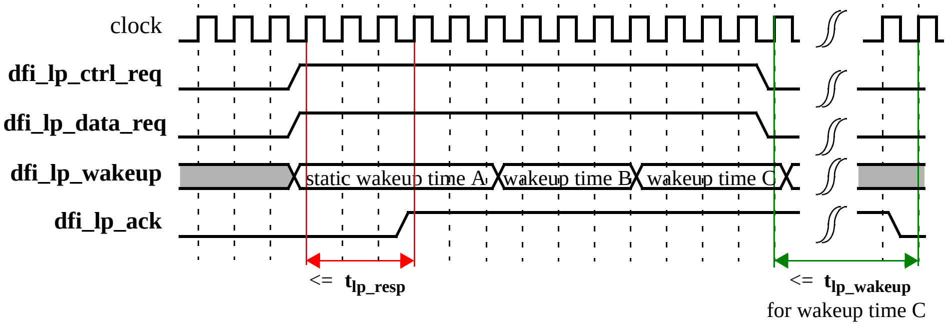


Figure 72, “Low Power State Progressing From an Active Control Interface to Inactive” illustrates **dfi_lp_ctrl_req** and **dfi_lp_data_req** when progressing from a low power state that requires use of the control interface into a low power state that can operate when the Control Interface is inactive.

FIGURE 72. *Low Power State Progressing From an Active Control Interface to Inactive*

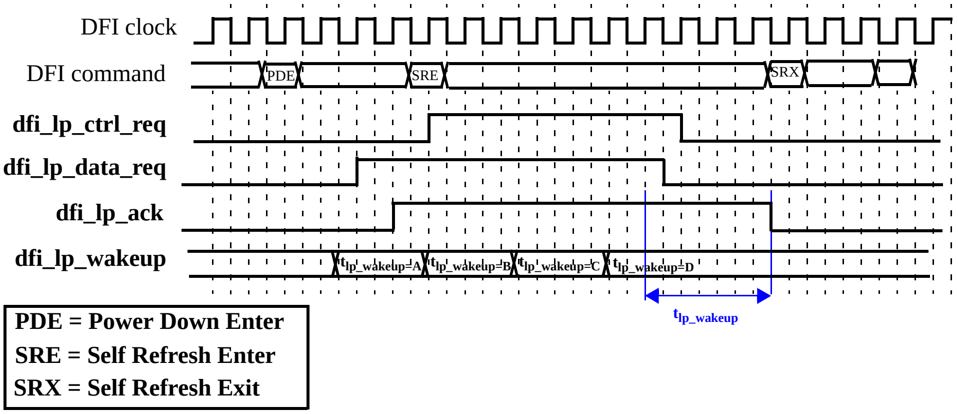
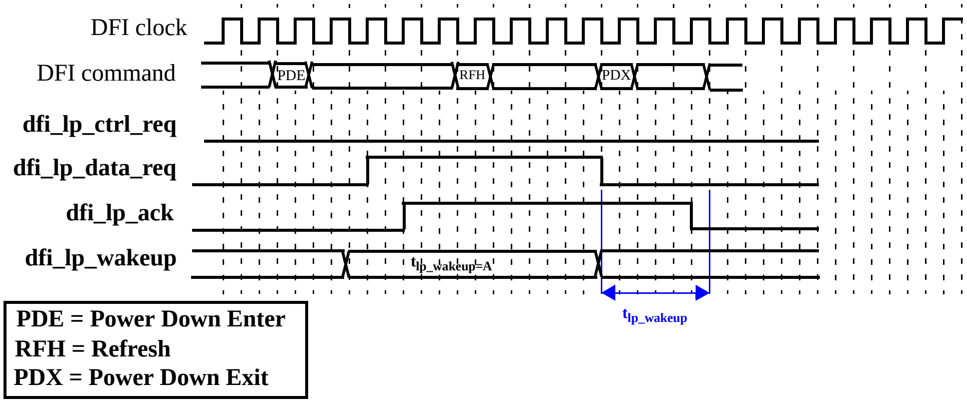


Figure 73, “Low Power State Requiring Ongoing Use of the Control Interface” illustrates **dfi_lp_data_req** when entering a low power state that must continue to execute memory commands.

FIGURE 73. *Low Power State Requiring Ongoing Use of the Control Interface*



4.13 Error Signaling

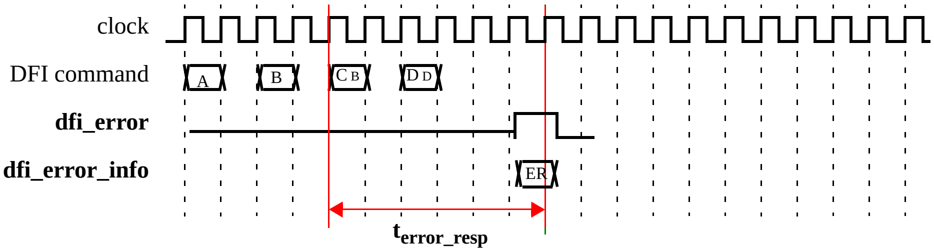
The optional DFI error interface enables the PHY to communicate error information from the PHY to the MC.

For data errors, the timing parameter is defined as the max delay from **dfi_wrdata_en** or **dfi_rddata_en** to the assertion of the **dfi_error** signal.

For command errors, the timing parameter is defined as the max delay from command to the assertion of the **dfi_error** signal. Since the timing parameter is a maximum delay, it is not always possible to correlate the error with a specific command.

Figure 74, “Example of Error Condition”, shows the error interface for the control signal interface of the PHY. The error condition does not affect RD A and RD B, the error condition may affect RD C and/or RD D.

FIGURE 74. *Example of Error Condition*



4.13.1 Error Code Definitions

Table 27, “Error Codes” defines specific error codes, error codes reserved for future use, and error codes available for design-specific definition. Not all defined error codes apply to all systems; all error types are optional unless required as part of another interface.

If multiple errors occur in a single clock cycle, the PHY is responsible for resolving communication through error prioritization, using multiple clocks, or other means.

TABLE 27. *Error Codes*

Error Response Code	Name	Description
0000	General purpose	The PHY indicates a general purpose error.
0001	Internal PHY	The PHY indicates some internal error condition.
0010-0111	Reserved	Reserved for a future definition.
1000 - 1111	User-defined	These error codes are available for user definition.

5.0 Signal Timing

The DFI specification does not specify timing values for signaling between the MC and the PHY. The only requirement is that a DFI clock must exist, and all DFI-related signals must be driven by registers referenced to the rising edge of this clock. There are no restrictions on how these signals are received, nor any rules on the source of the DFI clock. Compatibility between the MC and the PHY at given frequencies is dependent on the specification of both the output timing for signals driven and the setup and hold requirements for reception of these signals on the DFI.

However, the DFI signals are categorized into three signal groups that place restrictions on how signals may be driven and captured by DFI devices. All DFI signals may be driven from the DFI clock and captured on the following rising edge of the DFI clock. However, some signals may allow less restrictive timing which may alleviate timing restrictions within the design.

For frequency ratio systems, the PHY must send and receive DFI signals with respect to the rising edge of the DFI clock, even if the signals are driven and captured by registers clocked by the higher frequency DFI PHY clock.

There are three signal groups:

1. **Standard Signals**

   Standard signals contain timing critical information on a cycle-by-cycle basis and, therefore, must be sent and received on every DFI clock. The Control Interface signals fall into the standard signal category because the Control Interface signals must be cycle-accurate to properly communicate memory commands.

   Standard signals must be sent on the DFI clock and must be received on every DFI clock period for proper operation. All standard signals are required to meet setup and hold time to the DFI clock at the destination. Neither device should have a dependency on the source clock of the other device; the source and destination clock should always be assumed to be the DFI clock.

2. **State-Retaining Signals**

   State retaining signals contain information that is not single cycle-critical because state retaining signals retain a state change until either a signal acknowledge is received or a timing parameter has been satisfied. The Update Interface signals fall into the standard signal category because all signal state changes are defined in terms of signal responses and timing parameters.

   State-retaining signals may be sent and received in the same way on every DFI clock period. They may also be sent and/or received by a divided frequency clock; provided that the lower frequency clock is an even multiple (½, ¼, etc.) and is phase aligned to the DFI clock.

   All state-retaining signals are required to meet setup and hold time to the DFI clock at the destination regardless of whether the signal is generated from the DFI clock or from a lower frequency, phase-aligned clock source. Neither device should have a dependency on the source clock of the other device; the source and destination clock should always be assumed to be the DFI clock. If a lower frequency clock is used, the associated timing parameters must be set to appropriately account for the timing effects of using a lower frequency clock at either the source or destination. The timing parameters are always defined in terms of the DFI clock regardless of the source and destination clock frequency.

3. Timer-Based Signals

Training signals such as the **dfi_rdlvl_delay_x** and **dfi_rdlvl_resp** are classified as timer-based signals because the training signals are not valid until the $\mathbf{t_{rdlvl\_load}}$ and $\mathbf{t_{rdlvl\_resplat}}$ timing parameters are met.

Timer-based signals do not have a clock-edge dependency because timer-based signals are either not required to be valid until a timing parameter has been met, another signal has been asserted, or they are expected to be static during normal operation (static signals may be changed during idle times).

Timer-based signals do not have to meet setup and hold time to the DFI clock except on the cycle after meeting the associated timing parameter. Timer-based signals may also be changed during idle times in which case the setup and hold times are irrelevant. For the purpose of timing analysis, timer-based signals may be treated as multi-cycle paths.

Table 28, “Signal Group Divisions” shows that each DFI signal is categorized into a signal group.

TABLE 28. *Signal Group Divisions*

Signal	Signal Group
dfi_act_n **(or dfi_act_n_pN)**	Standard
dfi_alert_n_aN	Standard
dfi_address (or **dfi_address_pN**)	Standard
dfi_bank (or **dfi_bank_pN**)	Standard
dfi_bg **(or dfi_bg_pN)**	Standard
dfi_cas_n (or **dfi_cas_pN**)	Standard
dfi_cid **(or dfi_cid_pN)**	Standard
dfi_cke (or **dfi_cke_pN**)	Standard
dfi_cs_n (or **dfi_cs_pN**)	Standard
dfi_ctrlupd_ack	State-Retaining
dfi_ctrlupd_req	State-Retaining
dfi_data_byte_disable	Timer-Based
dfi_dram_clk_disable	Standard
dfi_error	Standard
dfi_error_info	Standard
dfi_freq_ratio	Timer-Based

TABLE 28. *Signal Group Divisions (Continued)*

Signal	Signal Group
dfi_init_complete	State-Retaining
dfi_init_start	State-Retaining
dfi_lp_ack	State-Retaining
dfi_lp_ctrl_req	State-Retaining
dfi_lp_data_req	State-Retaining
dfi_lp_wakeup	State-Retaining
dfi_lvl_pattern	State-Retaining
dfi_lvl_periodic	State-Retaining
dfi_odt (or **dfi_odt_pN**)	Standard
dfi_alert_n	Standard
dfi_parity_in (or **dfi_parity_in_pN**)	Standard
dfi_phy_rdlvl_cs_n	State-Retaining
dfi_phy_rdlvl_gate_cs_n	State-Retaining
dfi_phyupd_ack	State-Retaining
dfi_phyupd_req	State-Retaining
dfi_phyupd_type	State-Retaining
dfi_phy_wrlvl_cs_n	State-Retaining
dfi_ras_n (or **dfi_ras_pN**)	Standard
dfi_rddata (or **dfi_rddata_wN**)	Standard
dfi_rddata_cs_n_pN	State-Retaining
dfi_rddata_dbi_n_wN	Standard
dfi_rddata_dnv (or **dfi_rddata_dnv_wN**)	Standard
dfi_rddata_en (or **dfi_rddata_en_pN**)	Standard
dfi_rddata_valid (or **dfi_rddata_valid_wN**)	Standard
dfi_rdlvl_en	State-Retaining
dfi_rdlvl_gate_en	State-Retaining
dfi_rdlvl_gate_req	State-Retaining
dfi_rdlvl_req	State-Retaining
dfi_rdlvl_resp	Timer-Based

TABLE 28. *Signal Group Divisions (Continued)*

Signal	Signal Group
dfi_reset_n (or **dfi_reset_pN**)	Standard
dfi_we_n (or **dfi_we_pN**)	Standard
dfi_wrdata (or **dfi_wrdata_pN**)	Standard
dfi_wrdata_cs_n_pN	Standard
dfi_wrdata_en (or **dfi_wrdata_en_pN**)	Standard
dfi_wrdata_mask (or **dfi_wrdata_mask_pN**)	Standard
dfi_wrlvl_en	State-Retaining
dfi_wrlvl_req	State-Retaining
dfi_wrlvl_resp	Timer-Based
dfi_wrlvl_strobe	Standard

6.0 Glossary

TABLE 29. *Glossary of Terms*

Term	Definition
Command Address (CA) Signals	Includes the following control interface signals: **dfi_act_n, dfi_address**, **dfi_bank**, **dfi_bg, dfi_ras_n, dfi_cas_n**, and **dfi_we_n.** The DRAM class determines the signals applicable to a specific system.
CA Bus	JEDEC defines the CA bus as a double data rate bus containing command, address and bank/row buffer information. The CA bus is specific to LPDDR3 and LPDDR2 systems.
CA Training	A mechanism provided by the LPDDR3 DRAM, which utilizes a double data rate CA bus to optimize the CA timing relative to the memory clock. CA training is specific to LPDDR3 systems.
Command Bus	Includes the following control interface signals: **dfi_act_n, dfi_cas_n**, **dfi_ras_n** and **dfi_we_n.** The DRAM class determines the signals applicable to a specific system.
Column Selection (CAS)	Column address strobe.
Data Bus Inversion (DBI)	A feature of the DRAM that allows read and write data to be inverted selectively before the data is transferred across the DDR data bus.
DFI Alert Width	The width of the alert signal on the DFI interface. Typically the PHY would drive an alert signal per slice and the alert is typically 1-bit.
DFI Width	The width of the bus on the DFI interface. This is generally the same width as the DRAM bus.
DFI Bank Width	The number of bank bits on the DFI interface. This is generally the same number of bits as the number of bank pins on the DRAM device.
DFI Bank Group Width	The number of bank group bits on the DFI interface. This is generally the same number of bits as the number of BG bits on the DRAM device.
DFI Address Width	The number of address bits on the DFI interface. This is generally the same number of bits as the number of address bits on the DRAM device.
DFI Chip Select Width	The number of chip select bits on the DFI interface. This is generally the same number of bits as the number of chip select pins on the DRAM bus. Rank width and chip select width are equivalent.
DFI Chip ID Width	The CID signals are used with 3D stacks. For DDR4, the MAX width is 3-bits (stack of 8). There are also stacks with 1-bit for CID (stack of 2).
DFI clock cycle	The DFI clock has the same phase and frequency as the MC clock.
DFI clock frequency	Defines the clock frequency of the MC.
DFI CA Training MC I/F Width	The CA training MC interface width on the DFI interface. This is typically one bit per PHY command slice and typically one command slice.
DFI CA Training PHY I/F Width	The CA training PHY interface width on the DFI interface. This is typically one bit per PHY command slice and typically one command slice.
DFI CA Training Response Width	The CA training response width on the DFI interface. This is 2-bits per PHY command slice and typically one command slice.
DFI Control Width	The number of bits required to control the DRAMs, usually a single bit.
DFI DBI Width	The DBI width on the DFI interface. Typically DFI Data Width/8. See the description of dfi_wrdata_mask for more details.

TABLE 29. *Glossary of Terms (Continued)*

Term	Definition
DFI Data Enable Width	The width of the datapath enable signals on the DFI interface. For PHYs with an 8-bit slice, this is generally 1/16th of the DFI Data Width to provide a single enable bit per memory data slice, but may be 1/4, 1/8, 1/32, or any other ratio. Bit zero corresponds to the lowest segment.
DFI Data Width	The width of the datapath on the DFI interface. This is generally twice the DRAM data width.
DFI data word	One phase of read or write data passed between the MC and the PHY. A DFI data word is twice the width of the bus between the DRAM and the PHY and corresponds to a single memory word transfer across the DFI bus.
DFI Leveling PHY I/F Width	The leveling PHY interface width on the DFI interface. Typically one bit per PHY data and command slice that support training.
DFI PHY clock cycle	The DFI PHY clock cycle is the DFI clock cycle divided by the frequency ratio. For a 1:1 frequency ratio, the DFI clock cycle and the DFI PHY clock cycle are equivalent.
DFI Rank Width	Rank width and chip select width are equivalent. See “DFI Chip Select Width”.
$\mathrm{dfi}_{\mathrm{rw\_length}}$	The value of the total number of DFI clocks required to transfer one DFI read or write command worth of data. • For a matched frequency system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ would typically equal (burst length/2). • For a frequency ratio system: $\mathbf{dfi}_{\mathbf{rw\_length}}$ is defined in terms of DFI PHY clocks and would typically equal (burst length/2). Additional DFI clock (or DFI PHY clock) cycles must be added for the CRC data transfer.
DFI Read Data Valid Width	The width of the datapath valid signals on the DFI interface. Equivalent to the number of PHY data slices, the same width definition as the **dfi_rddata_en** signal. Bit zero corresponds to the lowest segment.
DFI Read Leveling MC I/F Width	The read leveling MC interface width on the DFI interface. Typically one bit per PHY data slice.
DFI Read Leveling PHY I/F Width	The read leveling PHY interface width on the DFI interface. Typically one bit per PHY data slice.
DFI Read Leveling Response Width	The read leveling response width on the DFI interface. Typically one bit per PHY data slice.
DFI Read Training Delay Width	The number of bits required to communicate read delay information to the PHY.
DFI Read Training Gate Delay Width	The number of bits required to communicate gate training delay information to the PHY.
DFI Read Training PHY I/F Width	The number of bits used to control the read training interface from the PHY perspective. The PHY may drive a signal from each memory data slice or combine the signals into a single signal.
DFI Read Training Response Width	The number of bits used to communicate read training status to the MC. The PHY Read Training response may be one bit per memory data slice or one bit per bit on the memory data bus. If this width is the same width as the memory data bus, gate training information should be returned on the lowest bit of each data slice.
DFI Training Interface	Utilized when the DFI training mode is enabled. The DFI training interface has three operations: gate training, read data eye training, and write leveling. Gate training and read data eye training are referred to collectively as “read training”. The training operation used is determined by the memory type and whether the system is using read signals or write signals.

TABLE 29. *Glossary of Terms (Continued)*

Term	Definition
DFI Write Leveling Delay Width	The number of bits required to communicate write delay information to the PHY.
DFI Write Leveling MC I/F Width	The number of bits used to control the write leveling interface from the MC perspective. The MC write leveling signals are generally fanned out such that a copy of the signal can be sent to each PHY memory data slice.
DFI Write Leveling PHY I/F Width	The number of bits used to control the write leveling interface from the PHY perspective. The PHY may drive a signal from each memory data slice or combine the signals into a single signal.
DFI Write Leveling Response Width	The number of bits used to communicate write leveling status to the MC. The PHY should drive a single bit per memory data slice.
DQ	The bi-directional bus that transfers read and write data to the DRAM.
DQS	The bi-directional data strobe bus transmitted to and from the DRAM.
Frequency Ratio	In a frequency ratio system, the MC and the PHY operate at a common frequency ratio of 1:2 or 1:4; the PHY must be able to accept a command on any and all phases. The frequency ratio depends on the relationship of the reference clocks for the MC and the PHY. Phase-specific signals with a suffix of "_pN" with the phase number N (e.g., **dfi_wrdata_pN**) replace the matched frequency control, write data, read data and status interface enable signals. Phase-specific signals allow the MC to drive multiple commands in a single clock cycle. Data word-specific signals with a suffix of "_wN" with the DFI data word number N (e.g., **dfi_rddata_wN**) replace the matched frequency read data interface signals to distinguish how memory words are transferred across the DFI bus. Variable pulse width-specific signals with a suffix of "aN", with the PHY clock cycle N (e.g., **dfi_alert_n_aN)**, replace the matched frequency status interface signals to maintain the pulse width during transmission of error signals from the memory system to the PHY. For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional. For more information on frequency ratios, refer to Section 4.8, "Frequency Ratios Across the DFI". For all signal types, the suffix for phase 0/word 0/clock cycle 0 is optional. For more information on frequency ratios, refer to Section 4.8, "Frequency Ratios Across the DFI".
Gate Training	An operation utilizing the MPR feature of the DRAM to center the DQS gate in the read data preamble.
Idle	The DFI bus is considered idle when the control interface is not sending any commands and all read and write data has transferred on the DFI bus, reached its destination (DRAM or MC), and the write data transfer has completed on the DRAM bus. No pages are open.
Matched Frequency	In a matched frequency system, the MC and the PHY operate at a common frequency ratio of 1:1.
MC	DDR Memory Controller logic
PHY	DDR Physical Interface logic
PHY Data Word	One phase of read or write data passed between the PHY and the DRAM. A PHY data word is the width of the bus between the PHY and the DRAM and corresponds to a single memory word transfer across the DFI bus. A PHY data word is half the width of a DFI data word.

TABLE 29. *Glossary of Terms (Continued)*

Term	Definition
DFI PHY clock frequency	Defines the period of the clock frequency of the PHY. For matched systems, this is the same as the period of the DFI clock frequency. For frequency ratio systems, the period of the PHY DFI clock frequency must be 1/2 or 1/4 the period of the DFI clock frequency. These clocks must be aligned in phase.
Read data eye training	An operation utilizing the MPR feature of the DRAM to center the DQS in the read data eye.
Read training	May refer to either gate training, data eye training, or both.
Row Selection (RAS)	Row address strobe.
Unit interval (UI)	Half of a data word; the number of DRAM data words in one DRAM burst. NOTE: With DDR DRAM devices, the number of DRAM data words is 2x the number of DFI data words.
Variable pulse width-specific signals	Differentiated with a suffix of “aN”, with the PHY clock cycle N (e.g., **dfi_alert_n_aN)**, variable pulse width-specific signals replace status interface matched frequency signals to maintain the pulse width during transmission of error signals from the memory system to the PHY.
Write leveling	A feature of the DRAM used to adjust the relationship between the DQS and the DRAM clock.