DesignWare® Cores LPDDR5/4/4X Memory Controller

Release Notes

DWC LPDDR5/4/4X Controller – Product Code: E092-0
DWC LPDDR5/4/4X Controller AFP – Product Code: E093-0
DWC AP LPDDR5/4/4X Controller – Product Code: E094-0

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LPDDR5/4/4X Memory Controller Release Notes

This release note describes the changes for release 1.10a-lca00 of the DesignWare Cores LPDDR5/4/4X.

The following topics are covered:

Note

This release supports a limited number of configurations.
Contact Synopsys to check whether your configuration is supported.
Contact Synopsys if you intend to tape-out your configuration with this release, for confirmation that the configuration is supported for tape-out.

1.1 STARs on the Web

You can view a complete list of problem reports for this product, including problems identified after product release, by accessing the STAR reports (STARs on the Web). You must have a SolvNet ID to view STAR reports.

DWC_ddrctl_lpddr54:

https://www.synopsys.com/dw/ipdir.php?c=dwc_lpddr54_controller

1.2 PHY Versions

This release contains the following DWC LPDDR5/4/4X PHY versions:

- PUB: 2.20a
- PHYINIT: C-2021.06
- FIRMWARE: C-2021.06

1.3 Fixed Defects and Enhancements

1.3.1 1.10a-lca00

1.3.1.1 Fixed Defects

- HWFFC flow is corrupted in certain conditions.
- DRAMSET1TMG2.rd2wr must be used in 16B mode.
- Automotive documentation must exist in workspace/automotive folder.
- Does not re-assert dfi_lp_data_req after ctrlupd/phyupd at low speed device.
- Documentation typo in Address Mapping for LPDDR5.
- SCHED0, SCHED3 and SCHED4 registers must be static.
- LPDDR5 Derate: Maximum interval between two refreshes limitation can be violated in 1.3x refresh rate.
- dfi_lp_data_req is not deasserted before assertion of dfi_init_start during HWFFC.
- Critical REFpb is blocked by ACTIVATE.
- Scrubber burst length is not equal to the programmed burst length register field.

1.3.1.2 Enhancements

- Enhanced incremental Periodic Phase Training (PPT2).
- Automatic switching from REFpb to REFab in case of derating for LPDDR5/4.
- [LPDDR5A] Support tCSLCK for WCK.
- Optimized PERFWR1.w_xact_run_length behavior for enhanced RDWR switch.
- Increased maximum width of MEMC_HIF_TAGBITS and MEMC_HIF_WDATA_PTR_BITS.
- Simplified TMGCFG.dfi_freq_fsp by removing replicated ones per frequency.
- Propagate Uncorrectable Read Link ECC Error to AXI-RRESP or HIF sideband signal.
- LPDDR5A: RTL update for timing gap between PDX and the next command.
- Removed unused ports from LPDDR DDRCTL interface post 1.01a-lca01 release.
- [JESD209-5A] 7.7.5 Refresh Management Command (RFM).
- Clarification of LPDDR5 WCK related parameters.
- Stop critical refresh burst when disabling automatic refresh.
- LPDDR5/4/4X Code cleanup post 1.01a-lca01 release.
- [JESD209-5A] Added 7.7.9.1 CAS-command-based Enhanced WCK Always On Mode.
- Support for parameter combinations of Link ECC and OCCAP.
- Hide hardware parameter MEMC_RDWR_SWITCH_POL_SEL and changed default value to 0.
- Minimized command gap between ACT and PRE to the same bank for performance improvement.
- Removed DRAMSET1TMG8 register (not used in LPDDR54).
- [LPDDR5A] Added a constraint from WRA to PDE.

- Enabled bypass path in XPI_RMW to be used when RMWs are not needed.

1.3.1.3 Hardware Parameter Changes

The following Hardware parameters have been added:

- DDRCTL_CHB_TSZ_REG_NUM
- DDRCTL_CHB_TZ_EN
- DDRCTL_PPT2
- DDRCTL_XPI_USE_RMWR

The following Hardware parameters have been deleted:

- MEMC_ENH_CAM_PTR
- MEMC_ENH_RDWR_SWITCH
- MEMC_FREQ_RATIO
- MEMC_OPT_WDATARAM
- MEMC_RDWR_SWITCH_POL_SEL

For details, refer to the “Parameter Descriptions” chapter of the databook.

1.3.1.4 Signal Changes

The following signals have been added:

- dfi0_ctrlupd_type
- dfi1_ctrlupd_type
- hif_rdata_eapar_err
- hif_rdata_eapar_err_dch1
- hif_rdata_uncorr_linkecc_err
- perf_op_is_cas_wck_sus
- perf_op_is_cas_wck_sus_dch1
- perf_op_is_cas_ws_off
- perf_op_is_cas_ws_off_dch1
- perf_op_is_rfm
- perf_op_is_rfm_dch1

The following signals have been deleted:

- perf_bypass_bank
- perf_bypass_bank_dch1
- perf_bypass_bg
- perf_bypass_bg_dch1
- perf_bypass_cid
- perf_bypass_cid_dch1

- perf_bypass_rank
- perf_bypass_rank_dch1

The following signals have been changed:

- PortWidth of signal dfi0_address_P0 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P0.
- PortWidth of signal dfi0_address_P1 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P1.
- PortWidth of signal dfi0_address_P2 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P2.
- PortWidth of signal dfi0_address_P3 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P3.
- PortWidth of signal dfi1_address_P0 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P0.
- PortWidth of signal dfi1_address_P1 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P1.
- PortWidth of signal dfi1_address_P2 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P2.
- PortWidth of signal dfi1_address_P3 changed from work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH to work.DWC_ddrctl_cc_constants.svh.MEMC_DFI_ADDR_WIDTH_P3.

For details, refer to the “Signal Descriptions” chapter of the databook.

1.3.1.5 Register Changes

The following registers have been added:

- REGB_ARB_PORT0.PCFGW.snf_mode
- REGB_ARB_PORT10.PCFGW.snf_mode
- REGB_ARB_PORT11.PCFGW.snf_mode
- REGB_ARB_PORT12.PCFGW.snf_mode
- REGB_ARB_PORT13.PCFGW.snf_mode
- REGB_ARB_PORT14.PCFGW.snf_mode
- REGB_ARB_PORT15.PCFGW.snf_mode
- REGB_ARB_PORT1.PCFGW.snf_mode
- REGB_ARB_PORT2.PCFGW.snf_mode
- REGB_ARB_PORT3.PCFGW.snf_mode

- REGB_ARB_PORT4.PCFGW.snf_mode
- REGB_ARB_PORT5.PCFGW.snf_mode
- REGB_ARB_PORT6.PCFGW.snf_mode
- REGB_ARB_PORT7.PCFGW.snf_mode
- REGB_ARB_PORT8.PCFGW.snf_mode
- REGB_ARB_PORT9.PCFGW.snf_mode
- REGB_DDRC_CH0.DFIMISC.dfi_freq_fsp
- REGB_DDRC_CH0.MSTR4.wck_suspend_en
- REGB_DDRC_CH0.MSTR4.ws_off_en
- REGB_DDRC_CH0.PPT2CTRL0.ppt2_burst
- REGB_DDRC_CH0.PPT2CTRL0.ppt2_burst_num
- REGB_DDRC_CH0.PPT2CTRL0.ppt2_ctrlupd_num_dfi0
- REGB_DDRC_CH0.PPT2CTRL0.ppt2_ctrlupd_num_dfi1
- REGB_DDRC_CH0.PPT2CTRL0.ppt2_wait_ref
- REGB_DDRC_CH0.PPT2STAT0.ppt2_burst_busy
- REGB_DDRC_CH0.PPT2STAT0.ppt2_state
- REGB_DDRC_CH0.RFMMOD0.raadec
- REGB_DDRC_CH0.RFMMOD0.raaimt
- REGB_DDRC_CH0.RFMMOD0.raamult
- REGB_DDRC_CH0.RFMMOD0.rfm_en
- REGB_DDRC_CH0.RFMMOD0.rfmsbc
- REGB_DDRC_CH0.RFMMOD0.rfmth_rm_thr
- REGB_DDRC_CH0.SCHED0.prefer_read
- REGB_DDRC_CH1.MSTR4.wck_suspend_en
- REGB_DDRC_CH1.MSTR4.ws_off_en
- REGB_FREQ0_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1
- REGB_FREQ0_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1_unit
- REGB_FREQ0_CH0.DFIUPDTMG2.ppt2_en
- REGB_FREQ0_CH0.DRAMSET1TMG32.t_wcksus
- REGB_FREQ0_CH0.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ0_CH0.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ0_CH0.RFMSET1TMG0.t_rfmpb
- REGB_FREQ0_CH0.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ0_CH0.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ0_CH1.DRAMSET1TMG32.t_wcksus
- REGB_FREQ0_CH1.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ0_CH1.DRAMSET1TMG32.ws_off2ws_fs

- REGB_FREQ0_CH1.RFMSET1TMG0.t_rfmpb
- REGB_FREQ0_CH1.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ0_CH1.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ1_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1
- REGB_FREQ1_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1_unit
- REGB_FREQ1_CH0.DFIUPDTMG2.ppt2_en
- REGB_FREQ1_CH0.DRAMSET1TMG32.t_wcksus
- REGB_FREQ1_CH0.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ1_CH0.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ1_CH0.RFMSET1TMG0.t_rfmpb
- REGB_FREQ1_CH0.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ1_CH0.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ1_CH1.DRAMSET1TMG32.t_wcksus
- REGB_FREQ1_CH1.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ1_CH1.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ1_CH1.RFMSET1TMG0.t_rfmpb
- REGB_FREQ1_CH1.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ1_CH1.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ2_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1
- REGB_FREQ2_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1_unit
- REGB_FREQ2_CH0.DFIUPDTMG2.ppt2_en
- REGB_FREQ2_CH0.DRAMSET1TMG32.t_wcksus
- REGB_FREQ2_CH0.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ2_CH0.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ2_CH0.RFMSET1TMG0.t_rfmpb
- REGB_FREQ2_CH0.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ2_CH0.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ2_CH1.DRAMSET1TMG32.t_wcksus
- REGB_FREQ2_CH1.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ2_CH1.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ2_CH1.RFMSET1TMG0.t_rfmpb
- REGB_FREQ2_CH1.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ2_CH1.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ3_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1
- REGB_FREQ3_CH0.DFIUPDTMG2.dfi_t_ctrlupd_interval_type1_unit
- REGB_FREQ3_CH0.DFIUPDTMG2.ppt2_en
- REGB_FREQ3_CH0.DRAMSET1TMG32.t_wcksus

- REGB_FREQ3_CH0.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ3_CH0.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ3_CH0.RFMSET1TMG0.t_rfmpb
- REGB_FREQ3_CH0.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ3_CH0.RFSHSET1TMG3.refresh_to_ab_x32
- REGB_FREQ3_CH1.DRAMSET1TMG32.t_wcksus
- REGB_FREQ3_CH1.DRAMSET1TMG32.ws_fs2wck_sus
- REGB_FREQ3_CH1.DRAMSET1TMG32.ws_off2ws_fs
- REGB_FREQ3_CH1.RFMSET1TMG0.t_rfmpb
- REGB_FREQ3_CH1.RFSHSET1TMG1.t_rfc_min_ab
- REGB_FREQ3_CH1.RFSHSET1TMG3.refresh_to_ab_x32

The following registers have been deleted:

- REGB_ARB_PORT0.SBRCTL.sbr_correction_mode
- REGB_ARB_PORT0.SBRSTAT.scrub_drop_cnt
- REGB_ARB_PORT0.SBRSTAT.scrub_drop_cnt_dch1
- REGB_DDRC_CH0.ECCCFG2.bypass_internal_ecc
- REGB_DDRC_CH0.ECCCFG2.flip_bit_pos0
- REGB_DDRC_CH0.ECCCFG2.flip_bit_pos1
- REGB_DDRC_CH0.HWFFCCTL.hwffc_odt_en
- REGB_DDRC_CH0.HWFFCCTL.hwffc_vref_en
- REGB_DDRC_CH0.OPCTRL0.dis_collision_page_opt
- REGB_FREQ0_CH0.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ0_CH0.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ0_CH0.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ0_CH0.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ0_CH0.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ0_CH0.TMGCFG.dfi_freq_fsp
- REGB_FREQ0_CH1.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ0_CH1.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ0_CH1.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ0_CH1.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ0_CH1.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ1_CH0.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ1_CH0.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ1_CH0.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ1_CH0.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ1_CH0.DRAMSET2TMG31.rfm_raa_thr_2

- REGB_FREQ1_CH0.TMGCFG.dfi_freq_fsp
- REGB_FREQ1_CH1.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ1_CH1.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ1_CH1.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ1_CH1.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ1_CH1.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ2_CH0.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ2_CH0.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ2_CH0.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ2_CH0.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ2_CH0.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ2_CH0.TMGCFG.dfi_freq_fsp
- REGB_FREQ2_CH1.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ2_CH1.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ2_CH1.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ2_CH1.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ2_CH1.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ3_CH0.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ3_CH0.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ3_CH0.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ3_CH0.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ3_CH0.DRAMSET2TMG31.rfm_raa_thr_2
- REGB_FREQ3_CH0.TMGCFG.dfi_freq_fsp
- REGB_FREQ3_CH1.DRAMSET1TMG8.t_xs_dll_x32
- REGB_FREQ3_CH1.DRAMSET1TMG8.t_xs_x32
- REGB_FREQ3_CH1.DRAMSET2TMG31.rfm_raaimt_2
- REGB_FREQ3_CH1.DRAMSET2TMG31.rfm_raa_ref_decr_2
- REGB_FREQ3_CH1.DRAMSET2TMG31.rfm_raa_thr_2

The following registers have been changed:

- RegisterResetValue of register REGB_DDRC_CH0.DDRCTL_VER_NUMBER.ver_number changed from 0x3130312a to 0x3131302a.
- RegisterResetValue of register REGB_DDRC_CH0.DDRCTL_VER_TYPE.ver_type changed from 0x6c633031 to 0x736f3031.
- Name of register REGB_DDRC_CH0.RFSHMOD0.mixed_refsb_hi_thr changed from REGB_DDRC_CH0.RFSHMOD0.mixed_refsb_hi_thr to REGB_DDRC_CH0.RFSHMOD0.auto_refab_en.
- RegisterResetValue of register REGB_DDRC_CH0.RFSHMOD0.mixed_refsb_hi_thr changed from 0xf to 0x0.

For details, refer to the “Register Descriptions” chapter of the Programming Guide.

1.3.2 1.01a-lca01

1.3.2.1 Fixed Defects

- Controller Assisted Drift Tracking is not initiated while DRAM is put into power down (STAR 3441761).
- perf_op_is_tcr_mrr is asserted even when an MRR command is issued other than to MR4 (STAR 3482346).
- Assert duration of perf_op_is_zqstart is not always one DFI clock cycle (STAR 3375678).
- In LPDDR4 mode, SRE/SRX/PDE/PDX is issued for both ranks irrespective of MSTR0.active_ranks (STAR 3395111).
- Scrubber sends less than expected number of transactions in the last scrub burst.
- HIF timing diagrams for DFI 1:2/1:1:2 frequency ratio mode are incorrect in "Channel Modes" chapter of DWC LPDDR5/4/4X Memory Controller Databook (STAR 3375680).
- The description of the w_max_starve feature is not correct in the Programming Guide (STAR 3440863).

1.3.2.2 Enhancements

- Changed bit width of dfi*_address_P<0-3> from 20 to 14 because higher 6 bits were unused/redundant
- Restrict reliability features with AP/AFP licenses
- Added support for HBW mode [only with MEMC_DRAM_DATA_WIDTH=32 and 16-bit PHY]
- dfi*_phymstr_ack and dfi*_phyupd_ack will now assert exclusively when both dfi*_phymstr_req and dfi*_phyupd_req assert (applicable when used with 3rd party PHYs)
- Added support for single rank LPDDR4/4X HWFFC
- Optimized XPI RRB for timing closure
- Improved clock gating in DWC_ddr_umctl2_datasync.v module
- Added support for Fusion Compiler
- Support for architectural clock gating of BSMs during low power states to reduce power consumption
- Improved CDC ack logic for registers containing R/W1S and R/W1C fields
- Improved control of starvation timer for WR CAM threshold when WR is issued
- Added register parity protection to LINKECCERRSTAT
- [LPDDR5A] 7.5.1 Refresh command - Update burst REFab constraints
- Added VC SpyGlass support

1.3.2.3 Hardware Parameter Changes

The following Hardware parameters have been added:

- `DDRCTL_CAPAR_CMDFIFO_DEPTH`
- `DDRCTL_CAPAR_RETRY`
- `DDRCTL_CHB_WRB_RAM_RD_ADDR_REG_OUT`

- DDRCTL_CHB_WRB_RAM_RD_DATA_REG_IN
- DDRCTL_CHB_WRB_RAM_WR_REG_OUT
- DDRCTL_CHB_WR_PROTQ_SIZE
- DDRCTL_ENH_ECC_REPORT_EN
- DDRCTL_HW_RFM_CTRL
- DDRCTL_NUM_BITS_PER_KBD
- DDRCTL_PBW_MODE_SUPPORT
- DDRCTL_RSD_PIPELINE
- DDRCTL_SW_RDWR_EN
- UMCTL2_OCCAP_PIPELINE

The following Hardware parameters have been deleted:

- UMCTL2_RETRY_CMD_FIFO_DEPTH
- UMCTL2_RETRY_MAX_ADD_RD_LAT
- UMCTL2_RETRY_WDATA_EXTERNAL_SRAM
- UMCTL2_RETRY_WDATA_EXTRAM_AW
- UMCTL2_RETRY_WDATA_EXTRAM_DEPTH
- UMCTL2_RETRY_WDATA_EXTRAM_DW

The following Hardware parameters have been changed:

- Default Value of HW parameter DDRCTL_RETRY_FIFO_DEPTH changed from 24 to 40.
- Value of HW parameter DDRCTL_RETRY_FIFO_DEPTH changed from 24 to 40.
- Default Value of HW parameter MEMC_NUM_TOTAL_BANKS changed from 16 to 0x10.
- Value of HW parameter MEMC_NUM_TOTAL_BANKS changed from 16 to 0x10.

For details, refer to the “Parameter Descriptions” chapter of the databook.

1.3.2.4 Signal Changes

The following signals have been added:

- bsm_clk
- hif_wdata_kbd
- hif_wdata_kbd_dch1
- bsm_clk_en
- hif_rdata_kbd
- hif_rdata_kbd_dch1

The following signals have been deleted:

- hif_wdata_ecc
- hif_wdata_ecc_dch1
- hif_wdata_mask_ecc

- hif_wdata_mask_ecc_dch1
- dbg_resp_ecc_data
- dbg_resp_ecc_data_dch1
- dbg_rxdata_ecc
- dbg_rxdata_ecc_dch1
- dbg_rxdata_mask_ecc
- dbg_rxdata_mask_ecc_dch1
- hif_rdata_ecc
- hif_rdata_ecc_dch1
- mpam_ns_err_intr
- mpam_s_err_intr

For details, refer to the “Signal Descriptions” chapter of the databook.

1.3.2.5 Register Changes

The following registers have been added:

- REGB_DDRC_CH0.ECCCSYN2.cb_corr_syndrome
- REGB_DDRC_CH0.ECCSTAT.sbr_read_ecc_ce
- REGB_DDRC_CH0.ECCSTAT.sbr_read_ecc_ue
- REGB_DDRC_CH0.ECCUSYN2.cb_uncorr_syndrome
- REGB_DDRC_CH0.HWFFCCTL.cke_power_down_mode
- REGB_DDRC_CH0.HWFFCCTL.ctrl_word_num
- REGB_DDRC_CH0.HWFFCCTL.hwffc_en
- REGB_DDRC_CH0.HWFFCCTL.init_fsp
- REGB_DDRC_CH0.HWFFCCTL.init_vrcg
- REGB_DDRC_CH0.HWFFCCTL.power_saving_ctrl_word
- REGB_DDRC_CH0.HWFFCCTL.skip_mrw_odtvref
- REGB_DDRC_CH0.HWFFCCTL.target_vrcg
- REGB_DDRC_CH0.HWFFCSTAT.current_frequency
- REGB_DDRC_CH0.HWFFCSTAT.current_fsp
- REGB_DDRC_CH0.HWFFCSTAT.current_vrcg
- REGB_DDRC_CH0.HWFFCSTAT.hwffc_in_progress
- REGB_DDRC_CH0.HWFFCSTAT.hwffc_operating_mode
- REGB_DDRC_CH0.RFSHMOD0.mixed_refsb_hi_thr
- REGB_DDRC_CH1.ECCCSYN2.cb_corr_syndrome
- REGB_DDRC_CH1.ECCSTAT.sbr_read_ecc_ce
- REGB_DDRC_CH1.ECCSTAT.sbr_read_ecc_ue
- REGB_DDRC_CH1.ECCUSYN2.cb_uncorr_syndrome

- REGB_DDRC_CH1.HWFFCSTAT.current_frequency
- REGB_DDRC_CH1.HWFFCSTAT.current_fsp
- REGB_DDRC_CH1.HWFFCSTAT.current_vrcg
- REGB_DDRC_CH1.HWFFCSTAT.hwffc_in_progress
- REGB_DDRC_CH1.HWFFCSTAT.hwffc_operating_mode
- REGB_FREQ0_CH0.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ0_CH0.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ0_CH1.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ0_CH1.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ1_CH0.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ1_CH0.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ1_CH1.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ1_CH1.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ2_CH0.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ2_CH0.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ2_CH1.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ2_CH1.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ3_CH0.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ3_CH0.DRAMSET1TMG17.t_vrcg_enable
- REGB_FREQ3_CH1.DRAMSET1TMG17.t_vrcg_disable
- REGB_FREQ3_CH1.DRAMSET1TMG17.t_vrcg_enable

The following registers have been deleted:

- REGB_ARB_PORT0.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT10.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT11.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT12.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT13.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT14.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT15.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT1.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT2.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT3.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT4.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT5.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT6.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT7.PCHBLCTRL.txsactive_en
- REGB_ARB_PORT8.PCHBLCTRL.txsactive_en

- REGB_ARB_PORT9.PCHBLCTRL.txsactive_en
- REGB_DDRC_CH0.ADVECCINDEX.ecc_err_symbol_sel
- REGB_DDRC_CH0.ADVECCINDEX.ecc_poison_beats_sel
- REGB_DDRC_CH0.ADVECCINDEX.ecc_syndrome_sel
- REGB_DDRC_CH0.ADVECCSTAT.advecc_corrected_err
- REGB_DDRC_CH0.ADVECCSTAT.advecc_err_symbol_bits
- REGB_DDRC_CH0.ADVECCSTAT.advecc_err_symbol_pos
- REGB_DDRC_CH0.ADVECCSTAT.advecc_num_err_symbol
- REGB_DDRC_CH0.ADVECCSTAT.advecc_uncorrected_err
- REGB_DDRC_CH0.ECCCFG0.ecc_type
- REGB_DDRC_CH0.ECCCFG1.poison_chip_en
- REGB_DDRC_CH1.ADVECCSTAT.advecc_corrected_err
- REGB_DDRC_CH1.ADVECCSTAT.advecc_err_symbol_bits
- REGB_DDRC_CH1.ADVECCSTAT.advecc_err_symbol_pos
- REGB_DDRC_CH1.ADVECCSTAT.advecc_num_err_symbol
- REGB_DDRC_CH1.ADVECCSTAT.advecc_uncorrected_err

The following registers have been changed:

- Name of register REGB_ADDR_MAP0.ADDRMAPLUTCFG.addrmap_lut_max_active_hif_addr_bit changed from REGB_ADDR_MAP0.ADDRMAPLUTCFG.addrmap_lut_max_active_hif_addr_bit to REGB_ADDR_MAP0.ADDRMAPLUTCFG.addrmap_lut_max_active_hif_addr_width.
- Name of register REGB_ARB_PORT0.SBRCTL.gen_rmw changed from REGB_ARB_PORT0.SBRCTL.gen_rmw to REGB_ARB_PORT0.SBRCTL.sbr_correction_mode.
- Name of register REGB_ARB_PORT0.SBRCTL.scrub_burst_length_normal changed from REGB_ARB_PORT0.SBRCTL.scrub_burst_length_normal to REGB_ARB_PORT0.SBRCTL.scrub_burst_length_nm.
- RegisterResetValue of register REGB_DDRC_CH0.DDRCTL_VER_NUMBER.ver_number changed from 0x3130302a to 0x3130312a.

For details, refer to the "Register Descriptions" chapter of the Programming Guide.

1.3.3 1.00a-lca01

1.3.3.1 Fixed Defects

- Both dfi_init_start and dfi_phyupd_ack can be asserted together (STAR 3213927).
- LPDDR5 ACT commands cannot be issued effectively when data rate is higher than 4800 (STAR 3158528)

- ACT is blocked by critical per-bank refresh for other bank (STAR 3101606)
- PHY master can cause Refresh interval violation (STAR 3109087)
- Incorrect behavior of VPR/W timeouts in dual channel configurations (STAR 9001485660)
- `DFIUPD0.dis_auto_ctrlupd` should be Quasi-dynamic Group 2 (STAR 9001509740)
- Issue with `DFITMG0.dfi_tphy_wrlat/dfi_tphy_wrdata` in frequency change procedure (STAR 9001511588)
- Scrubber's burst length is not equal to the programmed burst length register (STAR 3094530)

1.3.3.2 Enhancements

- Support for Dual RAQ with no AXI read data interleaving
- RRB Threshold Based VC Selection Feature for Read Data Interleaving Disabled Configuration
- Area efficient VTQ implementation in RRB
- Support Link ECC without enabling `MEMC_INLINE_ECC`
- Support for Single DDRC Single DFI configuration for LPDDR54
- Align LPDDR5 wck period after WCK Buffer timeout
- Support CAM and Read/Write Switching Enhancement in Dynamic BSM configuration
- Enhanced On-Chip Parity feature to corrupt ECC on write data when OCPAR write data parity error is detected in corresponding write data beat
- Improve management of ACT ordering for performance
- Minor timing closure improvement
- Add support `UMCTL2_PA_OPT_TYPE=2` for multiport AXI configurations.
  a. Default value of `UMCTL2_PA_OPT_TYPE` has changed. Up to 4 Internal ports default value of `UMCTL2_PA_OPT_TYPE` value is 2; for more than 4 internal ports it is 1.
- Add support MEMC_NO_OF_BLK_CHANNE=32 in inline ECC configurations
- Improve clock gating ratio
- Add feature to hide `ECCCSYN*` and `ECCUSYN*` register value by new input pin `dis_regs_ecc_syndrome` for security purpose. (ECC configurations only)
- Add support to generate multi-cycle path constraints when `DDRCTL_MCP_INCLUDE=1`

1.3.3.3 Hardware Parameter Changes

The following parameters have been added:

- `DDRCTL_SYS_INTF` parameter was added to select the System Interface for DDRC instead of `UMCTL2_INCL_ARB`
- `UMCTL2_RRB_THRESHOLD_EN_n`
- `UMCTL2_PA_OPT_TYPE`

1.3.3.4 Signal Changes

The following signals have been added:

- `dis_regs_ecc_syndrome`

1.4 Known Issues and Limitations

Table 1-1 lists unsupported features, as well as known issues and limitations in this version of the DDR Controller.

Table 1-1 Unsupported And Unverified Features in DWC LPDDR5/4/4X Controller

Category	Known Issues and Limitations	Notes
LPDDR5	8-bank mode is not supported.	
LPDDR5	BL32 is not supported.	
LPDDR5	Write X is not supported.	
LPDDR5	Data Copy is not supported.	
LPDDR5	CAS (B3) command (that is, Non-Zero Burst Start Address for RD) is not supported.	This limitation is only for HIF configuration (hif_address[3:0] must always be 0).
LPDDR5/4	Data rate less than 1066Mbps is not fully verified.	Contact Synopsys for more information.
LPDDR5/4	DFI Low-Power Control Handshaking for data is not fully verified.	
LPDDR5/4	Changing DFI frequency ratio dynamically is not supported.	
LPDDR5	DVFSC mode change is verified only during SR/SRPD.	Contact Synopsys for more information.
LPDDR4	HWFFC is supported only for LPDDR4/4X SDRAM with limited configuration.	Data rate has to be within the range between 1066Mbps and 4266Mbps. Contact Synopsys for more information.
LPDDR5	LPDDR5 HWFFC is not supported.	
DFI or PHY	Controller Assisted Drift Tracking for LPDDR4 (DQSOSC) is not recommended to be used.	Contact Synopsys for more information.
DFI or PHY	Changing DBI mode dynamically is not supported after initialization.	LPDDR54 PHY does not support it.
DFI or PHY	DBI mode in the PHY is not verified (only DFIMISC.phy_dbi_mode=0 is supported).	
Config/topology	Controller HW cannot be configured as dual channel configuration (Only single DDRC can exist in the controller).	Refer to the databook for more details.

Category	Known Issues and Limitations	Notes
Config/topology	Only 1:4 HW configuration is supported (DFI 1:2 mode or DFI 1:4 mode can be chosen by TMGCFG register during reset).	
Config/topology	Half Bus Width (HBW) is supported only with MEMC_DATA_WIDTH=32 and 16-bit PHY.	Refer to the databook for more details. For HBW mode, contact Synopsys for more information.
Config/topology	Quarter Bus Width (QBW) is not supported.	
Application Interface	CHI is not supported in LPDDR5/4/4X Controller.	
Automotive	ASIL- B Ready Certification packaged in this release is for Config1, Config2 and Config4. Config3 in FMEDA/Safety Manual is for reference only.	Contact Synopsys directly to agree usage of this Config3 in your application following future certification process.
TB	Warning-[FCPSBU] Invalid values in bin Warning-[FCIBR] Invalid bin range.	To avoid these warnings, if UMCTL2_A_IDW is set to a larger value than 23, the following command needs to be executed in the command line of coreConsultant GUI or included it in your configuration batch file: set_activity_parameter DWC_ddrctl_Simulate suppress_warning_noFCPSBU_plus_noFCIBR 1
TB	UVM_ERROR uvm_test_top [write_export_dfi] test_dwc_ddrctl_perf_vseq cast failed	If DDRCTL_HW_RFM_CTRL is set to 1, this UVM_ERROR is expected to be seen in the test test_dwc_ddrctl_default_settings_lpddr5.