Horizon X2A&J2A LPDDR4 & LPDDR4X System Simulation

Electrical Lab.

ASE Group Kaohsiung

Oct. 4, 2019

Outline
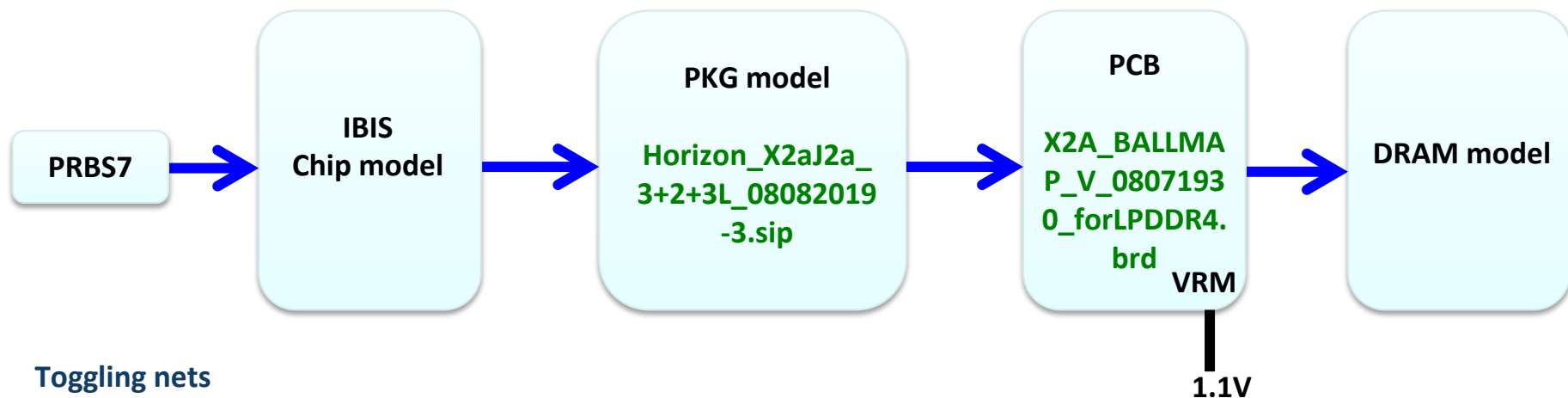
- **LPDDR4**
  - **SI Part**
  - **PI Part**
  - **AR**
- **LPDDR4X**
  - **SI Part**
  - **PI Part**

LPDDR4

ASE GROUP

Write mode Schematic

```
PRBS7 → IBIS Chip model → PKG model
                          Horizon_X2aJ2a_3+2+3L_08082019-3.sip → PCB
                                                                X2A_BALLMAP_V_08071930_forLPDDR4.brd
                                                                VRM
                                                                1.1V → DRAM model
```

- ➤ **Toggling nets**
  - ➤ **Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A**
  - ➤ **Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A**
  - ➤ **Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B**
  - ➤ **Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B**
  - ➤ **CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A**
  - ➤ **CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B**
- ➤ **Chip model : dwc_ddrphy_txrxdq_ns_clipped_lpd4.ibs, dwc_ddrphy_txrxdqs_ns_clipped_lpd4.ibs, dwc_ddrphy_txrxca_ns_clipped_lpd4.ibs**
  - ➤ DQ : mal4drv27_dl4_40
  - ➤ DQS: mal4drv27_dl4_40
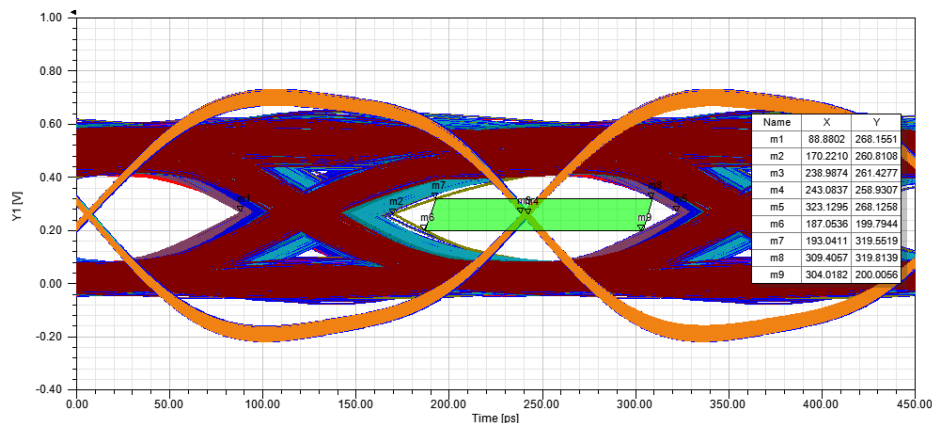 - ➤ CA: mal4drv27_dl4_40
  - ➤ CLK: mal4drv27_dl4_40
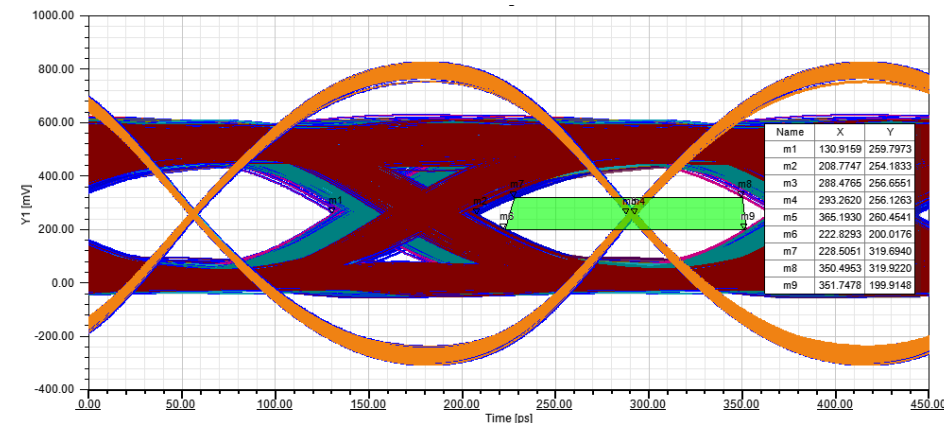- ➤ **On-die decap : 3.6nF & 4.4mohm**
- ➤ **DRAM model : z11m_1p1v_at.ibs**
  - ➤ DQ_IN_ODT40_VOH25_4266
  - ➤ DQS_IN_ODT40_VOH25_4266
  - ➤ CA_INPUT_ODT40_VOH25_4266
  - ➤ CLK_INPUT_ODT40_VOH25_4266

DQ Write Mode
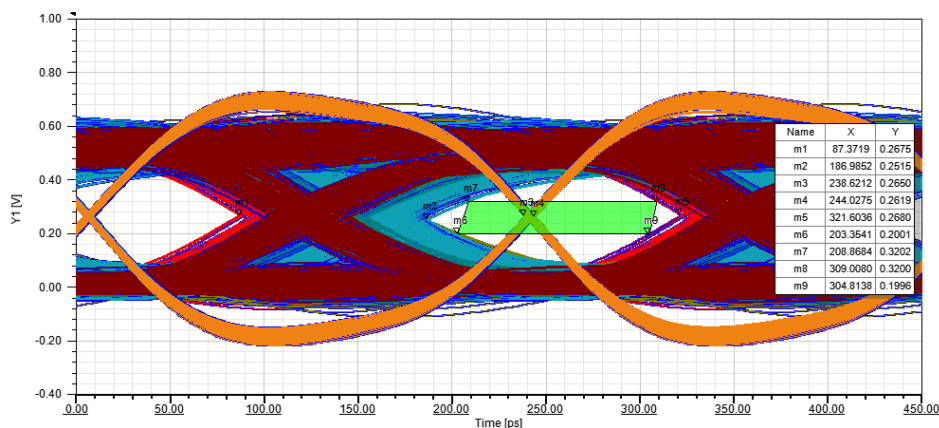
Vac & Vdc: 0.26 +/- 0.06V (320mv & 200mv)
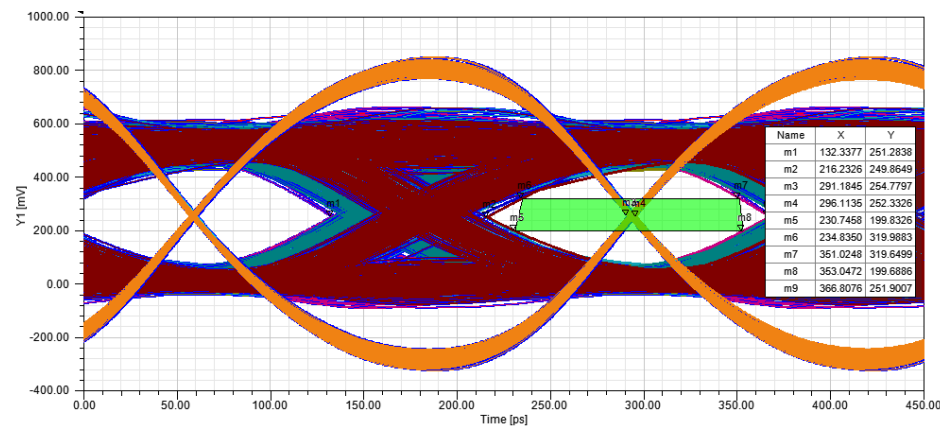

DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A

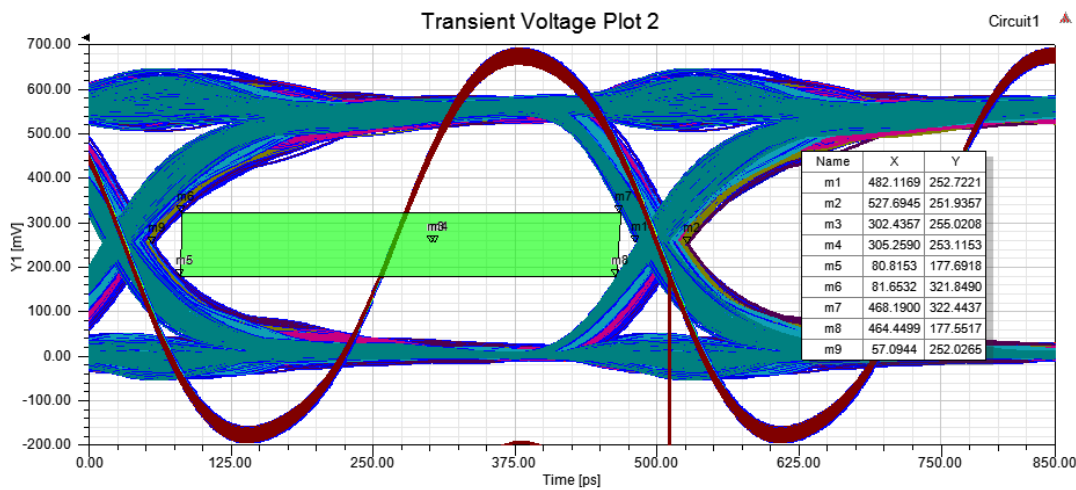DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A

DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B

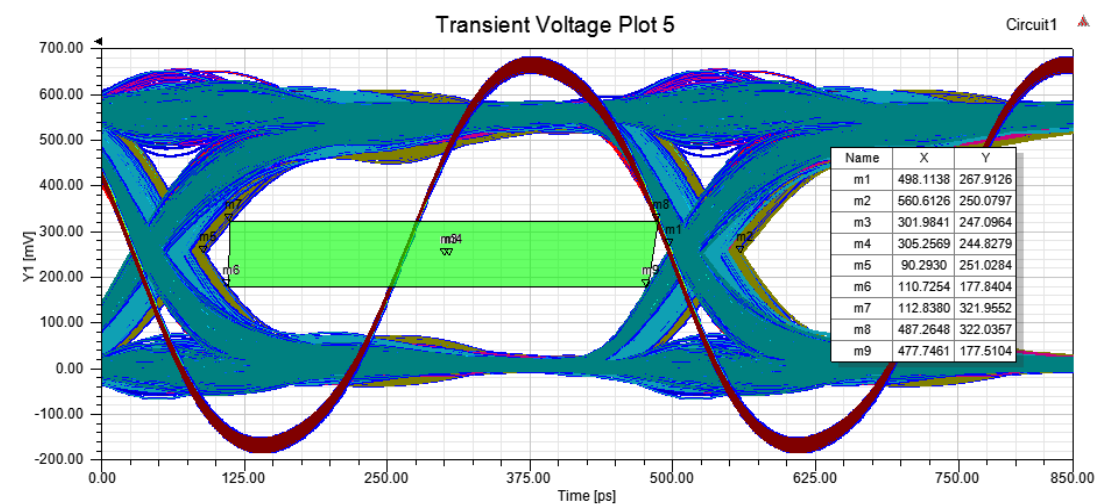DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

CA Write Mode

Vac & Vdc: 0.25 +/- 0.0725V (322.5mv & 177.5mv)

Transient Voltage Plot 2 — Circuit1

Name	X	Y
m1	482.1169	252.7221
m2	527.6945	251.9357
m3	302.4357	255.0208
m4	305.2590	253.1153
m5	80.8153	177.6918
m6	81.6532	321.8490
m7	468.1900	322.4437
m8	464.4499	177.5517
m9	57.0944	252.0265

Transient Voltage Plot 5 — Circuit1

Name	X	Y
m1	498.1138	267.9126
m2	560.6126	250.0797
m3	301.9841	247.0964
m4	305.2569	244.8279
m5	90.2930	251.0284
m6	110.7254	177.8404
m7	112.8380	321.9552
m8	487.2648	322.0357
m9	477.7461	177.5104

CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A

CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B

Write Mode Simulation Result

DQ Write Mode
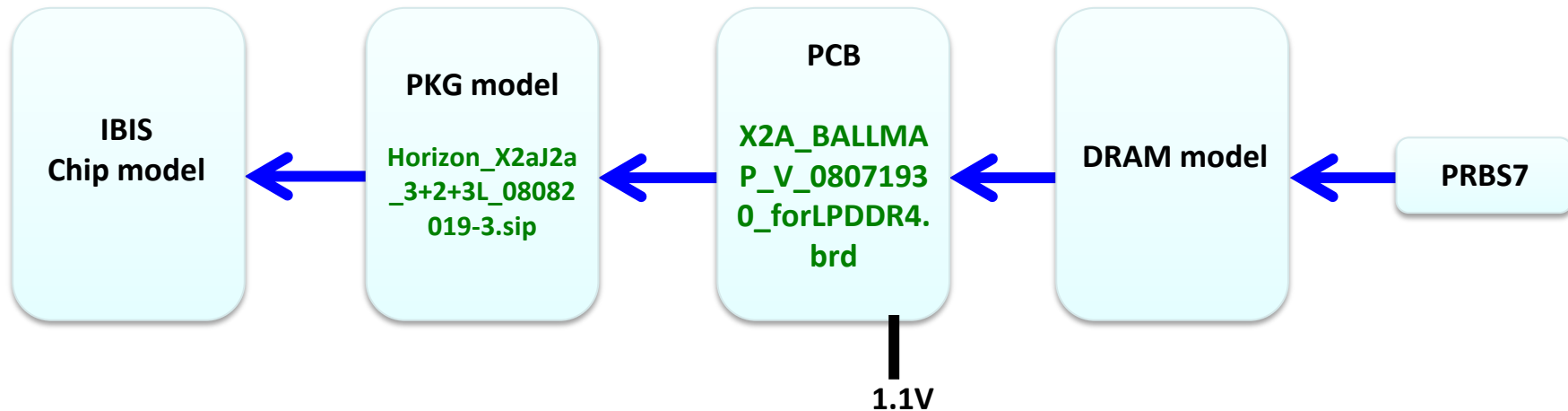
Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	81	78	100	84	-
DQS Jitter (ps)	4	5	5	5	-
TdIPW_total (UI)	0.65	0.67	0.58	0.64	0.45
TdIVW_total (UI)	0.47	0.52	0.41	0.49	0.25

CA Write Mode

Items	CA_1	CA_2	SPEC
CA Skew+Jitter (ps)	46	63	-
CLK Jitter (ps)	3	3	-
TcIPW_total (UI)	0.91	0.87	0.6
TcIVW_total (UI)	0.81	0.78	0.3

Read mode Schematic


```
IBIS              PKG model            PCB                DRAM model      PRBS7
Chip model    ←   Horizon_X2aJ2a   ←   X2A_BALLMA     ←   DRAM model   ←   PRBS7
                  _3+2+3L_08082        P_V_0807193
                  019-3.sip            0_forLPDDR4.
                                       brd
                                         |
                                       1.1V
```
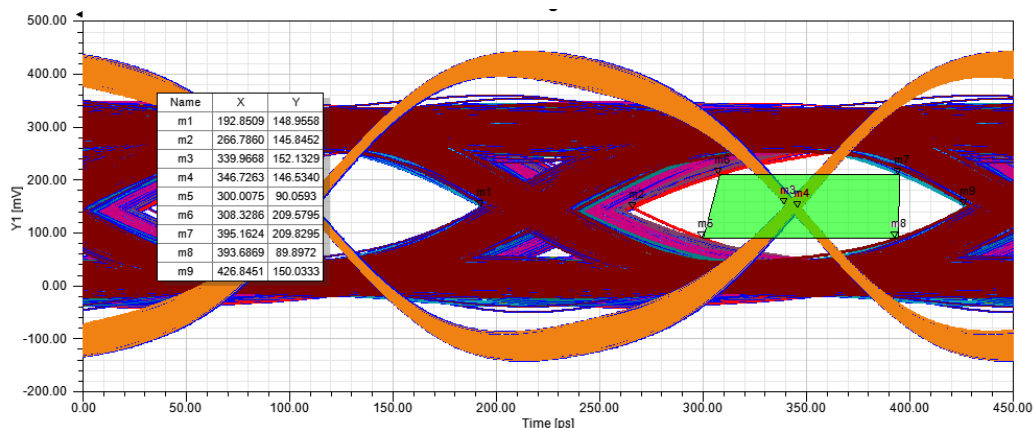
➢ **Toggling nets**
  ➢ **Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A**
  ➢ **Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A**
  ➢ **Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B**
  ➢ **Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B**
➢ **Chip model : dwc_ddrphy_txrxdq_ns_clipped_lpd4.ibs, dwc_ddrphy_txrxdqs_ns_clipped_lpd4.ibs**
  ➢ DQ : mal4drv27_dl4_odt40
  ➢ DQS: mal4drv27_dl4_odt40
➢ **On-die decap : 3.6nF & 4.4mohm**
➢ **DRAM model : z11m_1p1v_at.ibs**
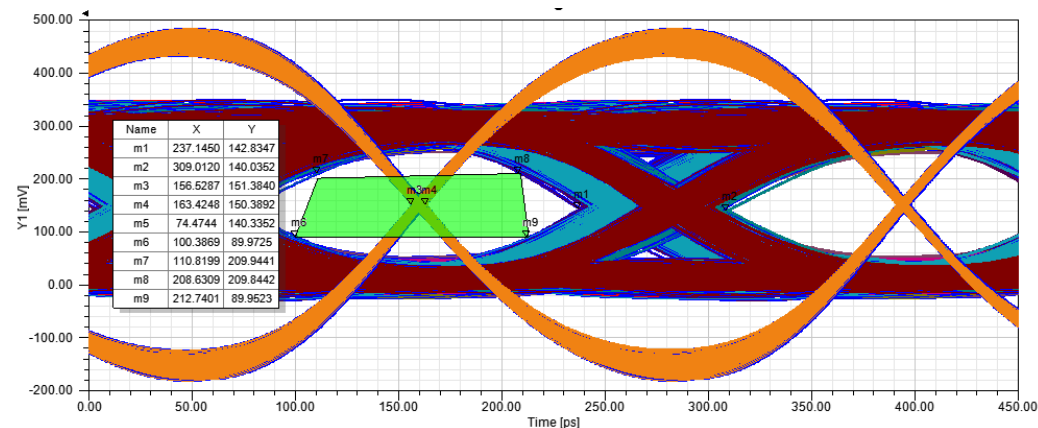 ➢ DQ_PD40_ODTDIS_VOH25_4266
  ➢ DQS_PD40_ODTDIS_VOH25_4266

DQ Read Mode

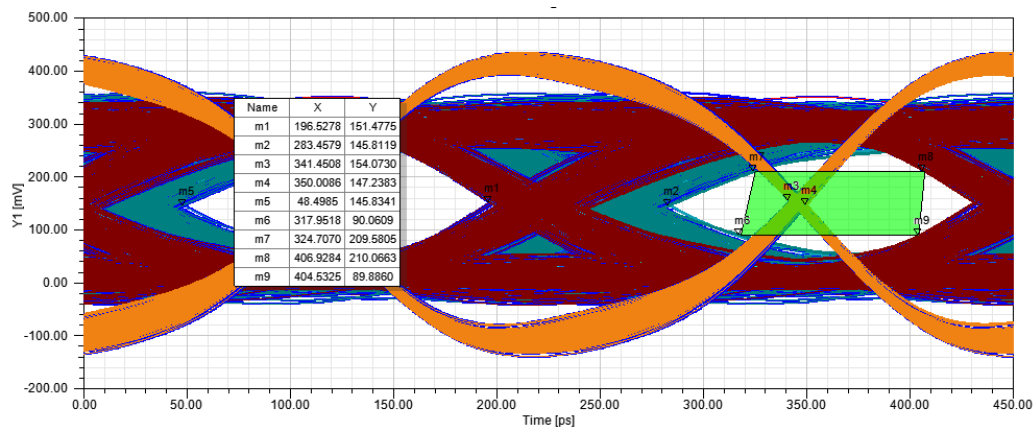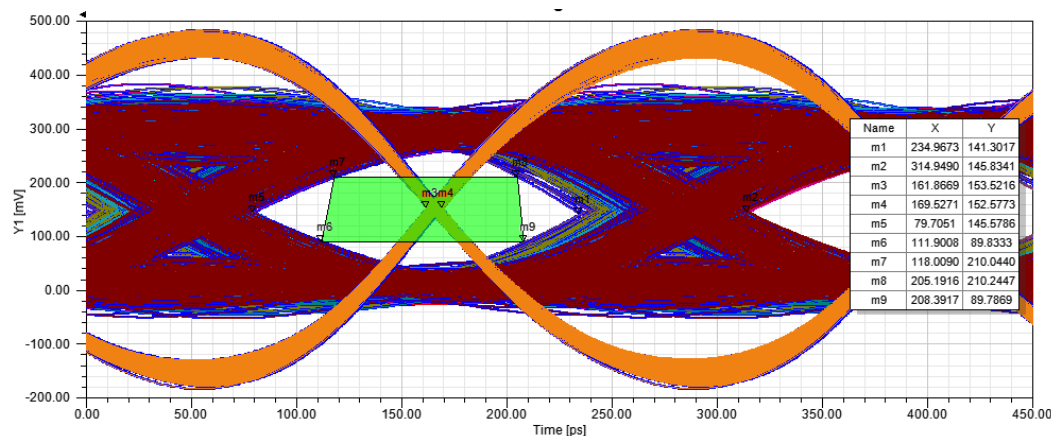Vac & Vdc: 0.15 +/- 0.06V (210mv & 90mv)

Name	X	Y
m1	192.8509	148.9558
m2	266.7860	145.8452
m3	339.9668	152.1329
m4	346.7263	146.5340
m5	300.0075	90.0593
m6	308.3286	209.5795
m7	395.1624	209.8295
m8	393.6869	89.8972
m9	426.8451	150.0333

DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A

Name	X	Y
m1	237.1450	142.8347
m2	309.0120	140.0352
m3	156.5287	151.3840
m4	163.4248	150.3892
m5	74.4744	140.3352
m6	100.3869	89.9725
m7	110.8199	209.9441
m8	208.6309	209.8442
m9	212.7401	89.9523

DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A

Name	X	Y
m1	196.5278	151.4775
m2	283.4579	145.8119
m3	341.4508	154.0730
m4	350.0086	147.2383
m5	48.4985	145.8341
m6	317.9518	90.0609
m7	324.7070	209.5805
m8	406.9284	210.0663
m9	404.5325	89.8860

DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B

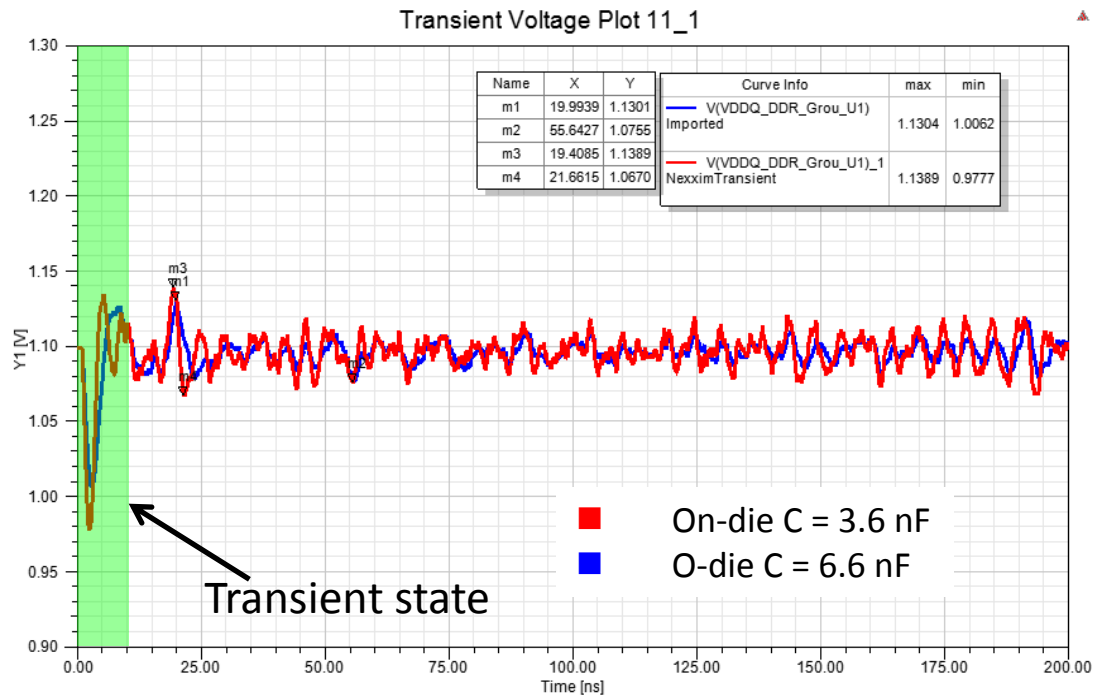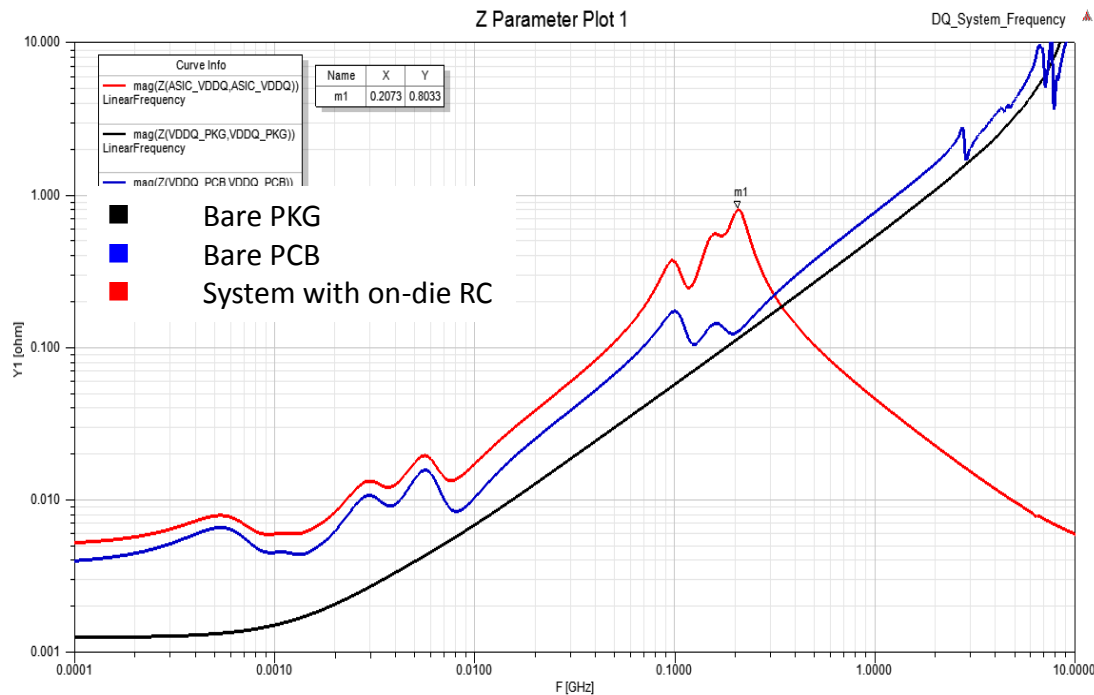| Name	X	Y
m1	234.9673	141.3017
m2	314.9490	145.8341
m3	161.8669	153.5216
m4	169.5271	152.5773
m5	79.7051	145.5786
m6	111.9008	89.8333
m7	118.0090	210.0440
m8	205.1916	210.2447
m9	208.3917	89.7869

DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

Read Mode Simulation Result

DQ Read Mode

Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	73	72	86	80	-
DQS Jitter (ps)	7	7	9	8	-
TdIPW_total (UI)	0.68	0.7	0.63	0.66	0.45
TdIVW_total (UI)	0.37	0.41	0.35	0.37	0.25

VDDQ_DDR

Z Parameter Plot 1 — DQ_System_Frequency

Curve Info
mag(Z(ASIC_VDDQ,ASIC_VDDQ)) LinearFrequency
mag(Z(VDDQ_PKG,VDDQ_PKG)) LinearFrequency
mag(Z(VDDQ_PCB,VDDQ_PCB))

m1 0.2073 0.8033

■ Bare PKG
■ Bare PCB
■ System with on-die RC

Transient Voltage Plot 11_1

Name	X	Y	Curve Info	max	min
m1	19.9939	1.1301	V(VDDQ_DDR_Grou_U1) Imported	1.1304	1.0062
m2	55.6427	1.0755			
m3	19.4085	1.1389	V(VDDQ_DDR_Grou_U1)_1 NexximTransient	1.1389	0.9777
m4	21.6615	1.0670			

■ On-die C = 3.6 nF
■ O-die C = 6.6 nF

Transient state

- Transient state (0 ~ 10ns):
  - On-die C => 3.6 nF: P2P Noise = 2.3% ~ -11%
  - On-die C => 6.6 nF: P2P Noise = 2.1% ~ -8.5%
- Steady state (10 ~ 200ns):
  - On-die C => 3.6nF: P2P Noise = 3% ~ -3%
  - On-die C => 6.6nF: P2P Noise = 2.7% ~ -2.3%
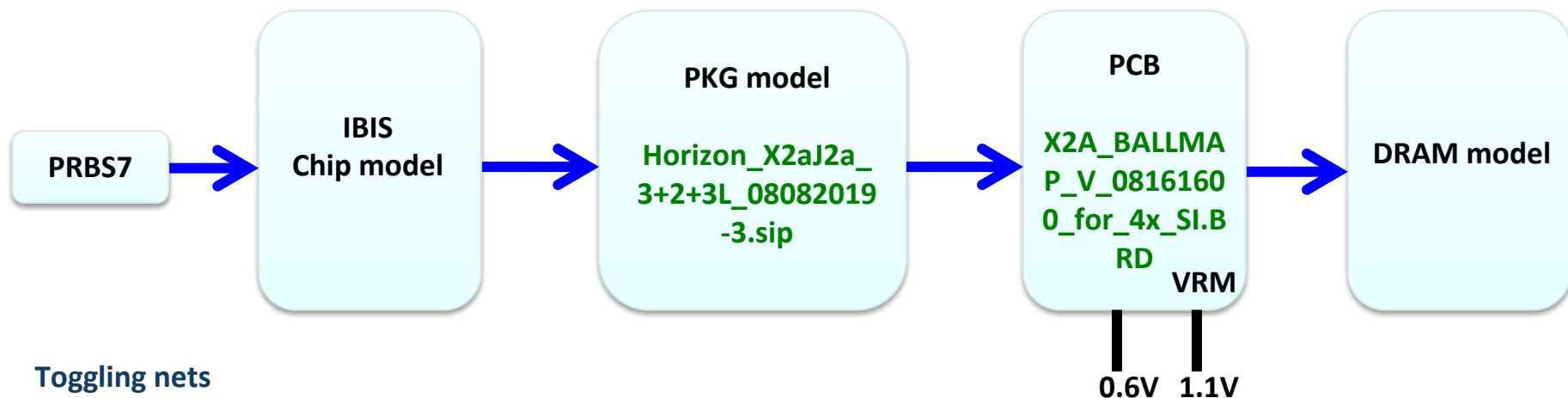
- SPEC: +/- 2.5% noise
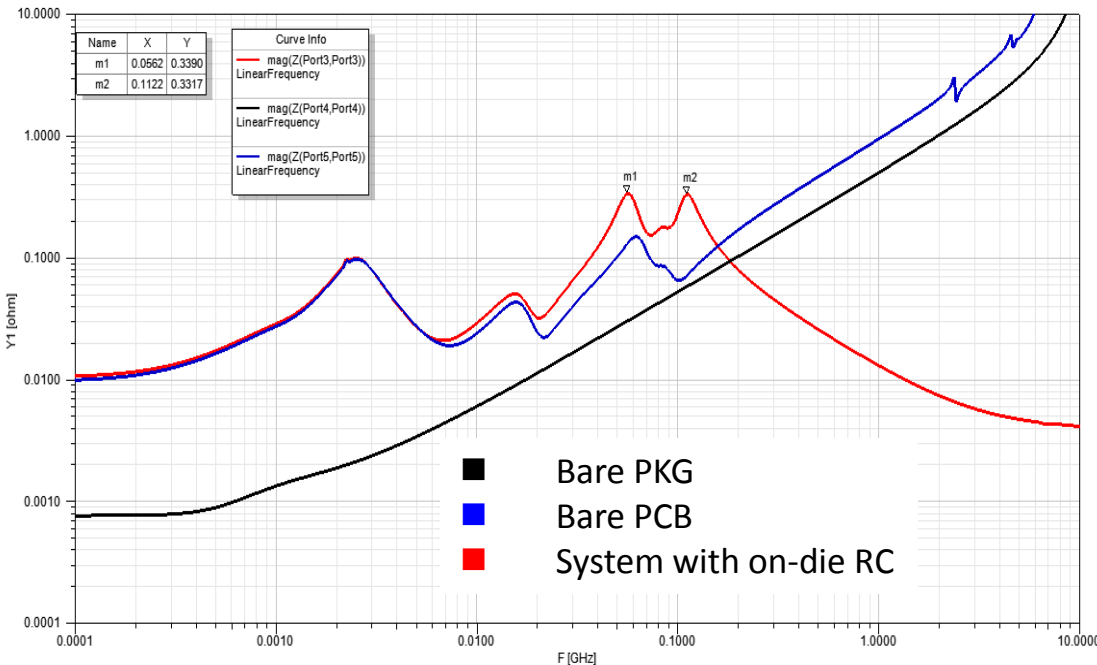
VDD_DDR
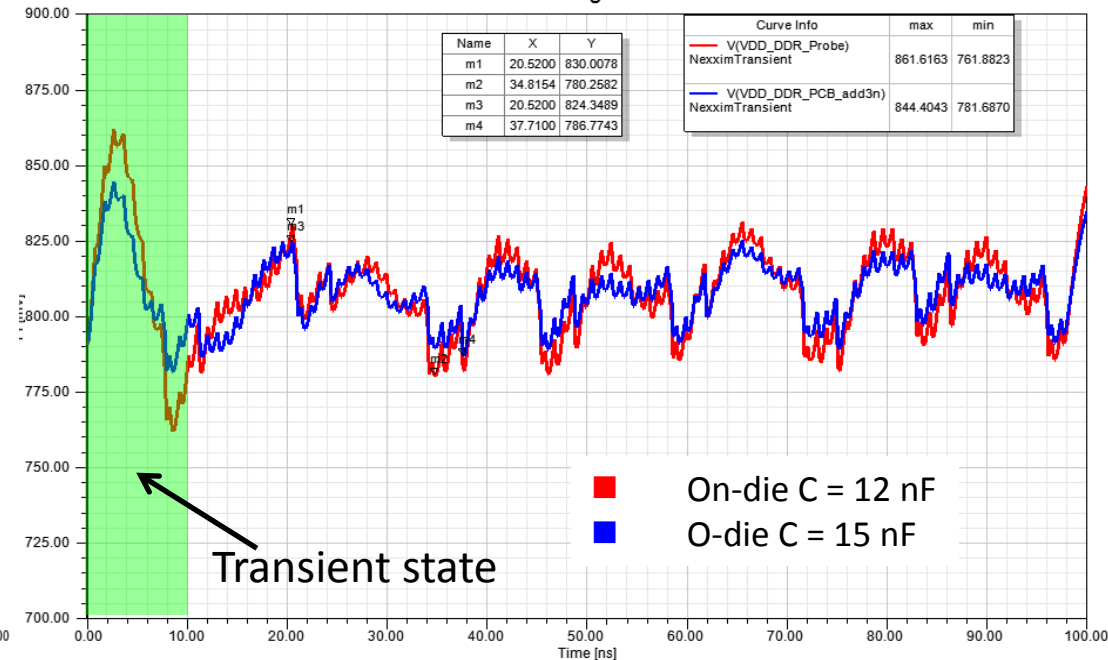
- Transient state (0 ~ 10ns):
  - On-die C => 12 nF: P2P Noise = 7.6% ~ -4.75%
  - On-die C => 15 nF: P2P Noise = 5.5% ~ -2.3%
- Steady state (10 ~ 200ns):
  - On-die C => 12 nF: P2P Noise = 3.8% ~ -2.5%
  - On-die C => 15 nF: P2P Noise = 3% ~ -1.6%

- SPEC: +/- 2% noise

LPDDR4X

Write mode Schematic

PRBS7 → **IBIS Chip model** → **PKG model** Horizon_X2aJ2a_3+2+3L_08082019-3.sip → **PCB** X2A_BALLMAP_V_08161600_for_4x_SI.BRD VRM → **DRAM model**

0.6V 1.1V

➢ **Toggling nets**
   ➢ **Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A**
   ➢ **Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A**
   ➢ **Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B**
   ➢ **Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B**
   ➢ **CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A**
   ➢ **CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B**
➢ **Chip model : dwc_ddrphy_txrxdq_ns_clipped_lpd4x.ibs, dwc_ddrphy_txrxdqs_ns_clipped_lpd4x.ibs, dwc_ddrphy_txrxca_ns_clipped_lpd4x.ibs**
   ➢ DQ : mal4drv27_dl4x_40
   ➢ DQS: mal4drv27_dl4x_40
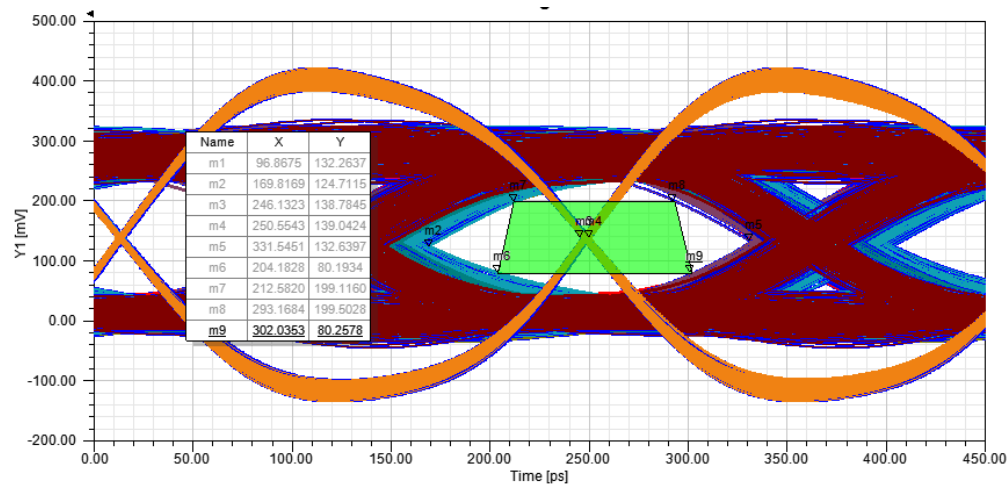   ➢ CA: mal4drv27_dl4x_40
   ➢ CLK: mal4drv27_dl4x_40
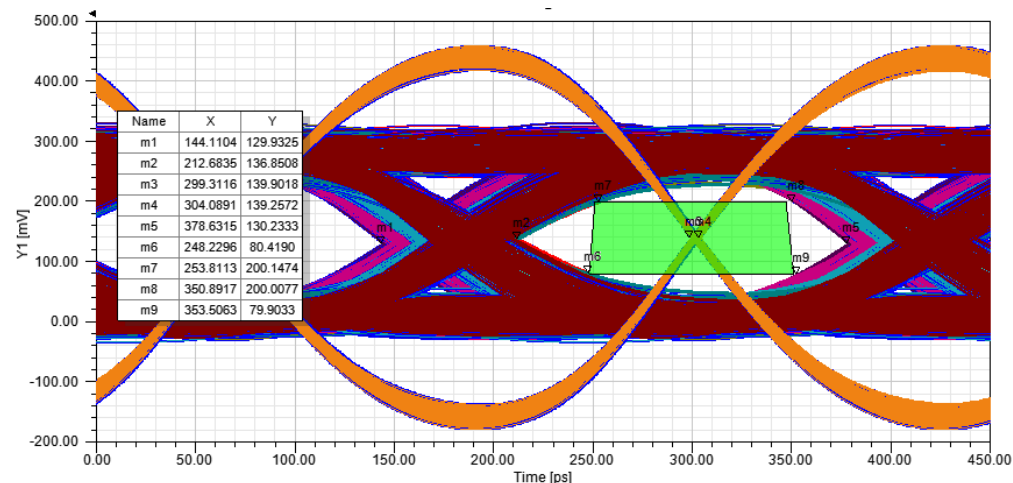➢ **On-die decap : 1nF & 24mohm, 3.6nF & 4.4mohm**
➢ **DRAM model : z11m_0p6v_at.ibs**
   ➢ DQ_IN_ODT40_VOH60_4266   ➢ CA_INPUT_ODT40_VOH60_4266
   ➢ DQS_IN_ODT40_VOH60_4266   ➢ CLK_INPUT_ODT40_VOH60_4266

DQ Write Mode

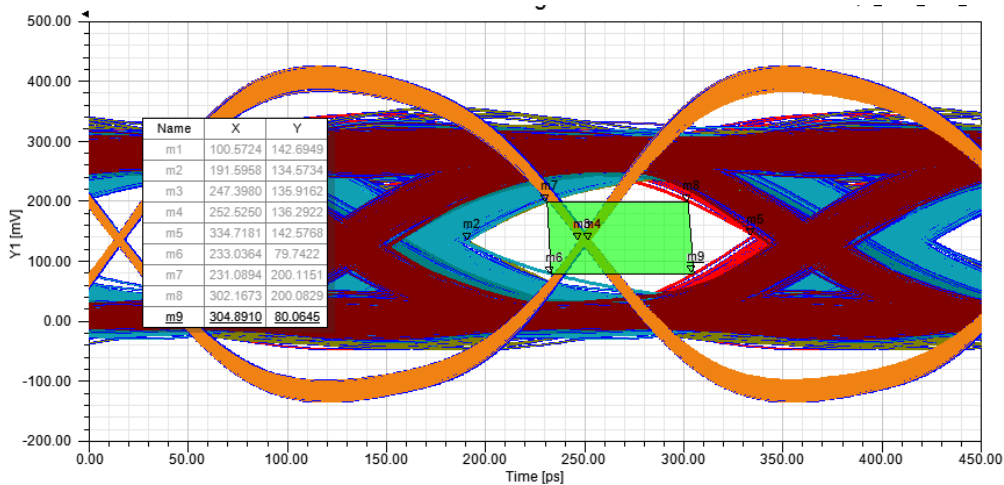Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)
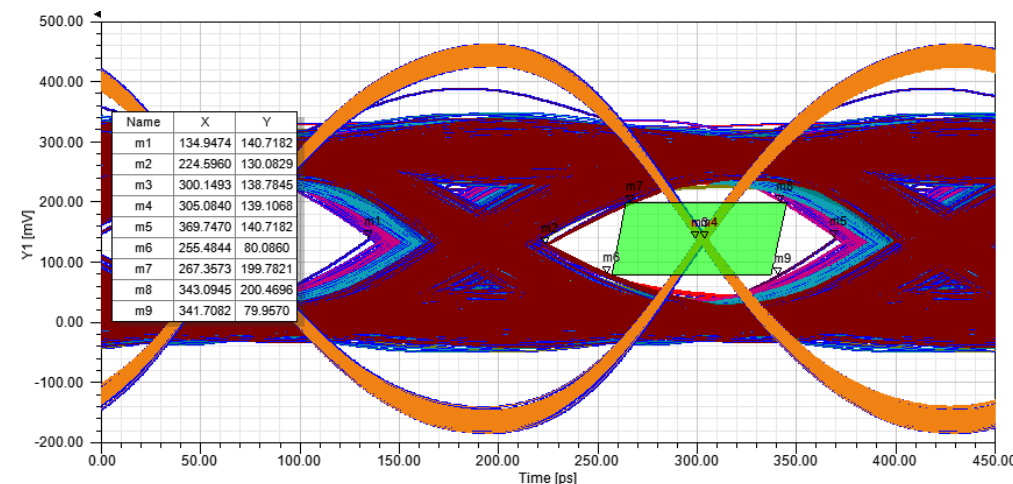

Name	X	Y
m1	96.8675	132.2637
m2	169.8169	124.7115
m3	246.1323	138.7845
m4	250.5543	139.0424
m5	331.5451	132.6397
m6	204.1828	80.1934
m7	212.5820	199.1160
m8	293.1684	199.5028
m9	302.0353	80.2578

DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A

Name	X	Y
m1	144.1104	129.9325
m2	212.6835	136.8508
m3	299.3116	139.9018
m4	304.0891	139.2572
m5	378.6315	130.2333
m6	248.2296	80.4190
m7	253.8113	200.1474
m8	350.8917	200.0077
m9	353.5063	79.9033

DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A

Name	X	Y
m1	100.5724	142.6949
m2	191.5958	134.5734
m3	247.3980	135.9162
m4	252.5250	136.2922
m5	334.7181	142.5768
m6	233.0364	79.7422
m7	231.0894	200.1151
m8	302.1673	200.0829
m9	304.8910	80.0645

DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B

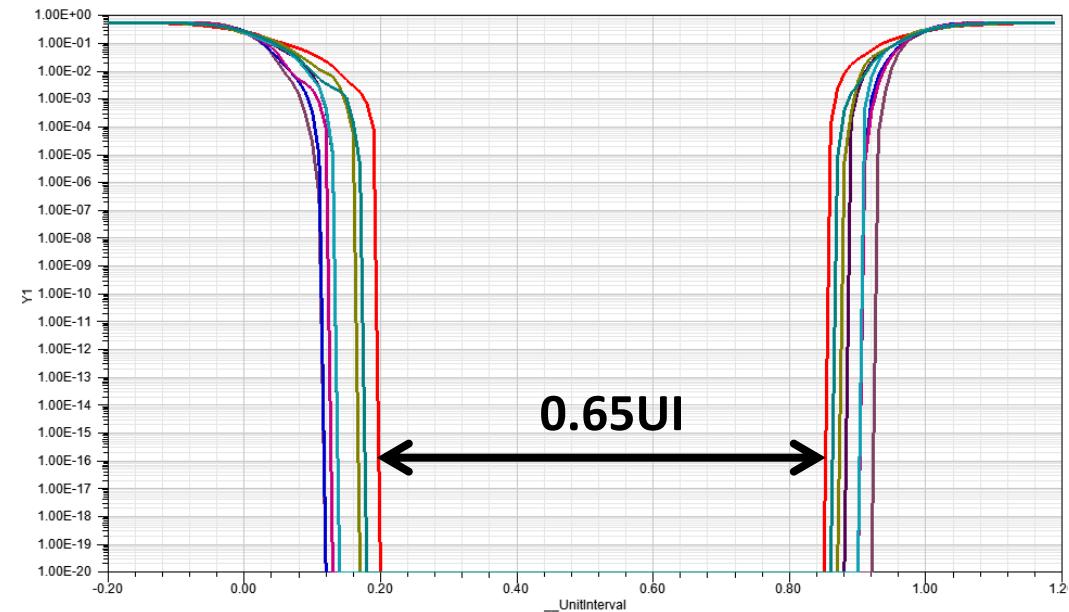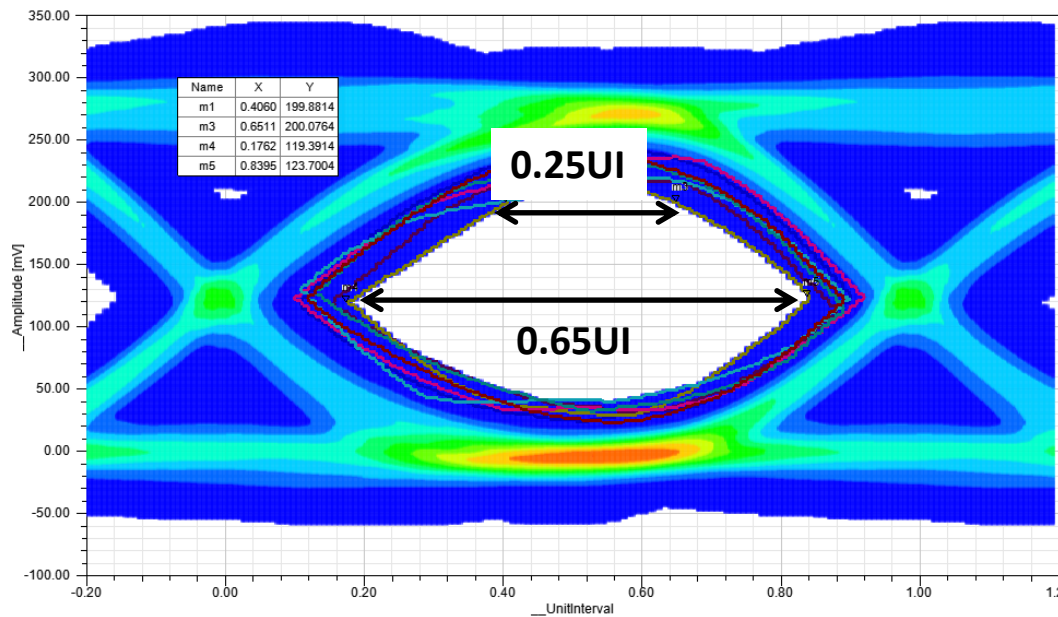| Name	X	Y
m1	134.9474	140.7182
m2	224.5960	130.0829
m3	300.1493	138.7845
m4	305.0840	139.1068
m5	369.7470	140.7182
m6	255.4844	80.0860
m7	267.3573	199.7821
m8	343.0945	200.4696
m9	341.7082	79.9570

DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

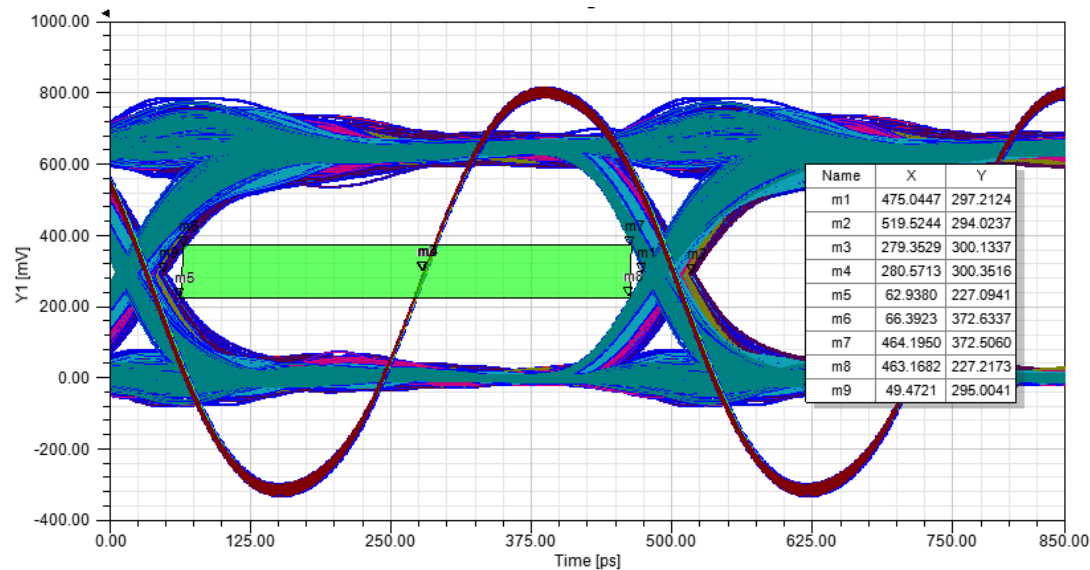# DQ Write Mode - Byte3 (stat.)

Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)

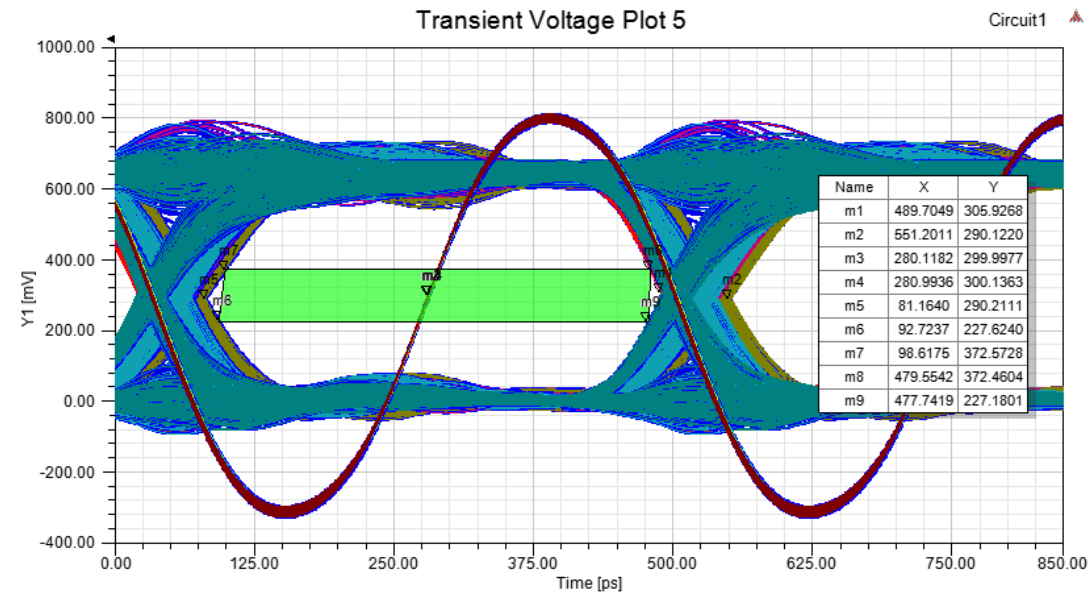**DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B**

CA Write Mode

Vac & Vdc: 0.3 +/- 0.0725V (372.5mv & 227.5mv)

Name	X	Y
m1	475.0447	297.2124
m2	519.5244	294.0237
m3	279.3529	300.1337
m4	280.5713	300.3516
m5	62.9380	227.0941
m6	66.3923	372.6337
m7	464.1950	372.5060
m8	463.1682	227.2173
m9	49.4721	295.0041

CA_1: DRAM_CA0_A ~ DRAM_CA5_A, DRAM_NCS0_A, DRAM_NCS1_A, DRAM_CK_C_A, DRAM_CK_T_A

Transient Voltage Plot 5 — Circuit1

Name	X	Y
m1	489.7049	305.9268
m2	551.2011	290.1220
m3	280.1182	299.9977
m4	280.9936	300.1363
m5	81.1640	290.2111
m6	92.7237	227.6240
m7	98.6175	372.5728
m8	479.5542	372.4604
m9	477.7419	227.1801

CA_2: DRAM_CA0_B ~ DRAM_CA5_B, DRAM_NCS0_B, DRAM_NCS1_B, DRAM_CK_C_B, DRAM_CK_T_B

Write Mode Simulation Result

DQ Write Mode

Items	Byte 1	Byte 2	Byte 3	Byte 3 (stat.)	Byte 4	SPEC
DQ Skew+Jitter (ps)	72	68	91	-	90	-
DQS Jitter (ps)	5	5	5	-	4	-
TdIPW_total (UI)	0.69	0.71	0.61	0.65	0.62	0.45
TdIVW_total (UI)	0.35	0.41	0.29	0.25	0.32	0.25

CA Write Mode

Items	CA_1	CA_2	SPEC
CA Skew+Jitter (ps)	45	61	-
CLK Jitter (ps)	1	1	-
TcIPW_total (UI)	0.91	0.87	0.6
TcIVW_total (UI)	0.85	0.82	0.3

Read mode Schematic
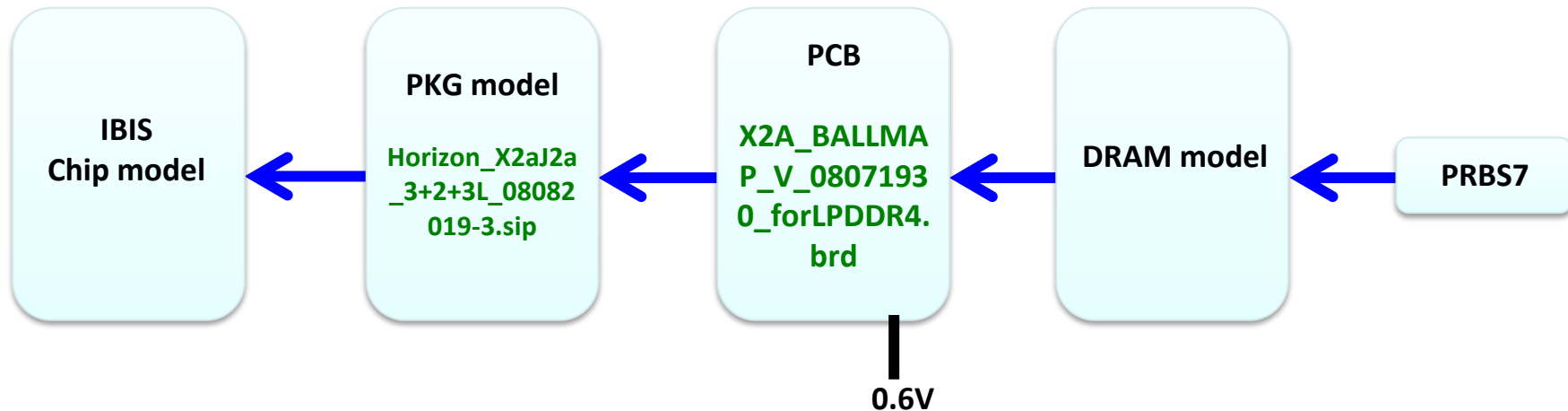
```
IBIS          ◄──  PKG model      ◄──  PCB              ◄──  DRAM model  ◄──  PRBS7
Chip model         Horizon_X2aJ2a       X2A_BALLMA
                   _3+2+3L_08082        P_V_0807193
                   019-3.sip            0_forLPDDR4.
                                        brd
                                         │
                                        0.6V
```

➢ **Toggling nets**
  ➢ **Byte 1: DRAM_DATA1_A ~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A**
  ➢ **Byte 2: DRAM_DATA8_A ~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A**
  ➢ **Byte 3: DRAM_DATA1_B ~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B**
  ➢ **Byte 4: DRAM_DATA8_B ~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B**
➢ **Chip model : dwc_ddrphy_txrxdq_ns_clipped_lpd4x.ibs, dwc_ddrphy_txrxdqs_ns_clipped_lpd4x.ibs**
  ➢ DQ : mal4drv27_dl4x_odt40
  ➢ DQS: mal4drv27_dl4x_odt40
➢ **On-die decap : 1nF & 24mohm**
➢ **DRAM model : z11m_0p6v_at.ibs**
  ➢ DQ_PD40_ODTDIS_VOH60_4266
  ➢ DQS_PD40_ODTDIS_VOH60_4266

DQ Read Mode

Vac & Vdc: 0.14 +/- 0.06V (200mv & 80mv)
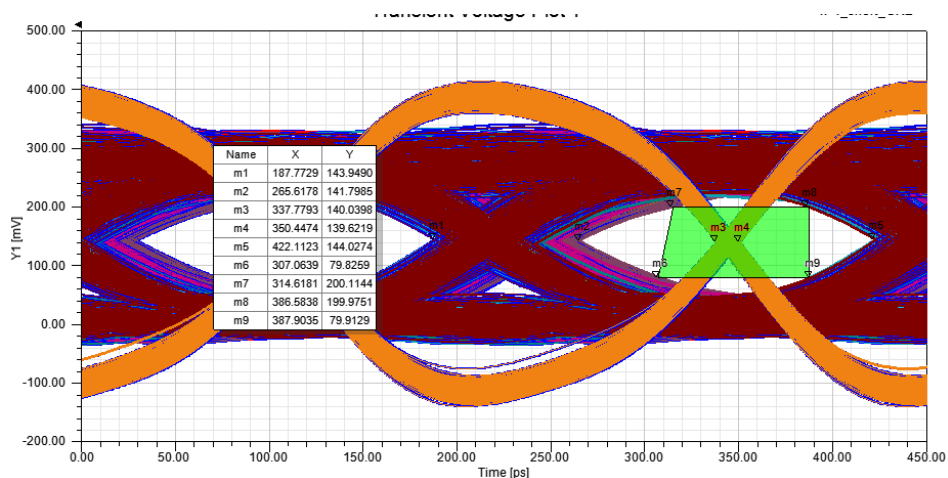
DRAM_DATA1_A~ DRAM_DATA7_A, DRAM_SDQS0_C_A, DRAM_SDQS0_T_A
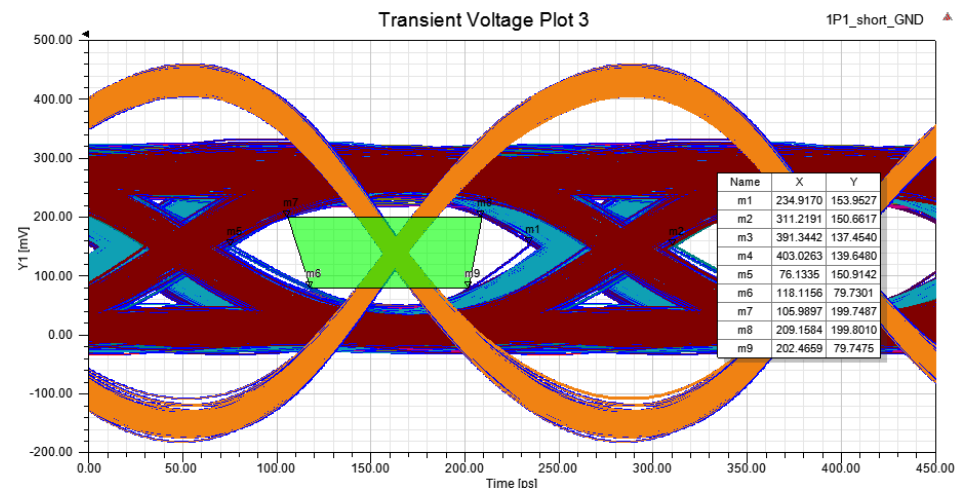
DRAM_DATA8_A~ DRAM_DATA15_A, DRAM_SDQS1_C_A, DRAM_SDQS1_T_A
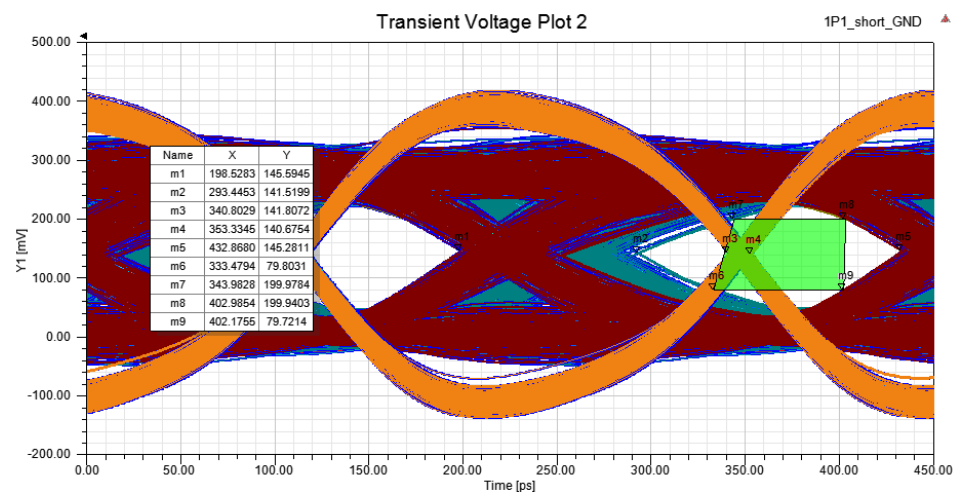
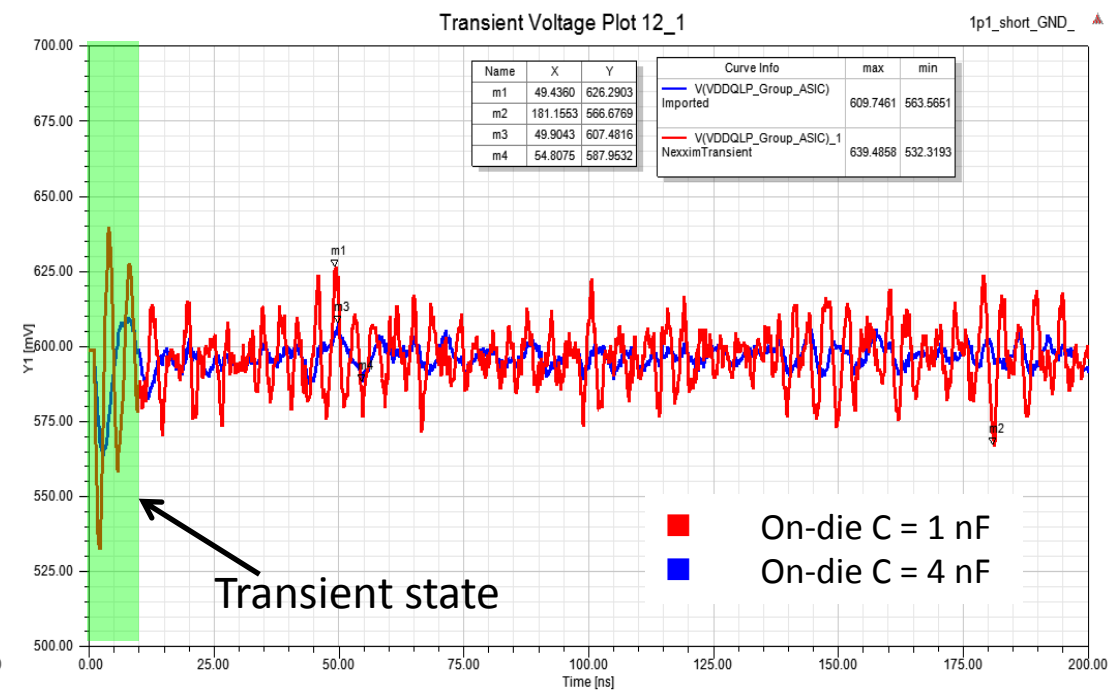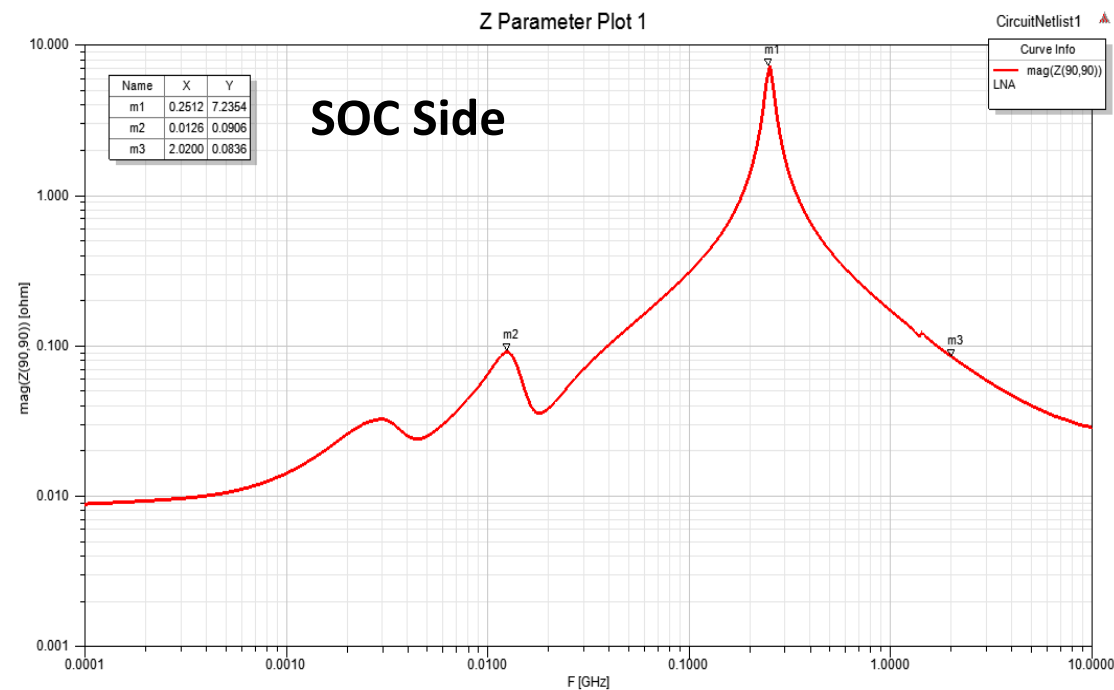DRAM_DATA1_B~ DRAM_DATA7_B, DRAM_SDQS0_C_B, DRAM_SDQS0_T_B
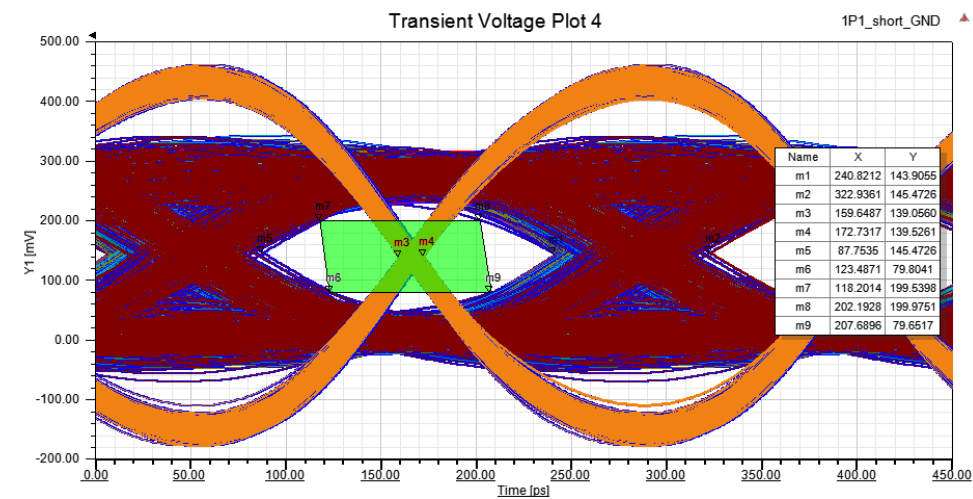
DRAM_DATA8_B~ DRAM_DATA15_B, DRAM_SDQS1_C_B, DRAM_SDQS1_T_B

Read Mode Simulation Result

DQ Read Mode

Items	Byte 1	Byte 2	Byte 3	Byte 4	SPEC
DQ Skew+Jitter (ps)	78	76	94	82	-
DQS Jitter (ps)	12	12	12	12	-
TdIPW_total (UI)	0.67	0.68	0.6	0.65	0.45
TdIVW_total (UI)	0.31	0.36	0.25	0.34	0.25

VDDQLP - Write Mode

SOC Side

Transient state

On-die C = 1 nF
On-die C = 4 nF

- Transient state (0 ~ 10ns):
  - On-die C => 1 nF: P2P Noise = 6.5% ~ -11.3%
  - On-die C => 4 nF: P2P Noise = 1.6% ~ -6%
- Steady state (10 ~ 200ns):
  - On-die C => 1 nF: P2P Noise = 4.3% ~ -4.7%
  - On-die C => 4 nF: P2P Noise = 1.1% ~ -2%
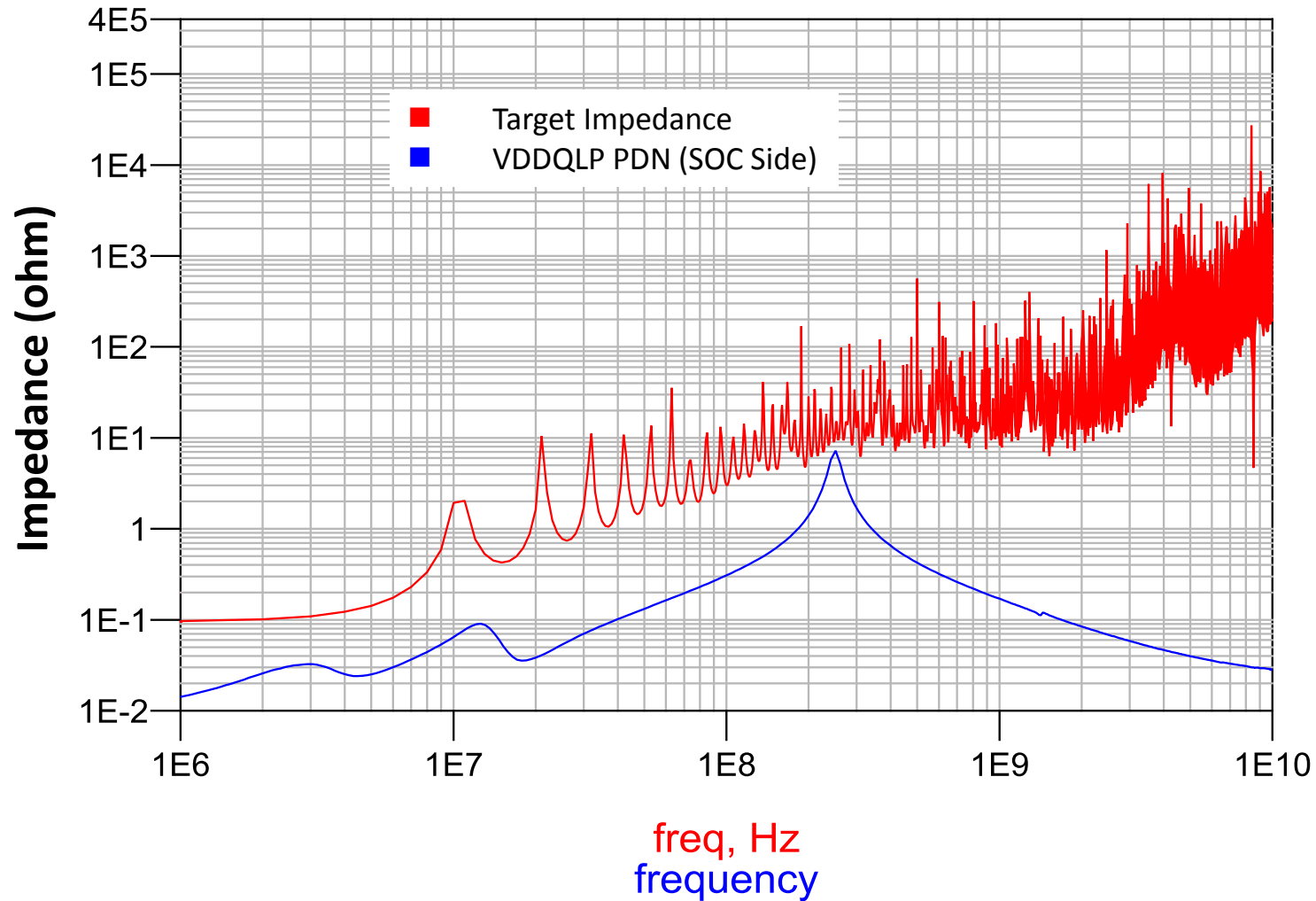
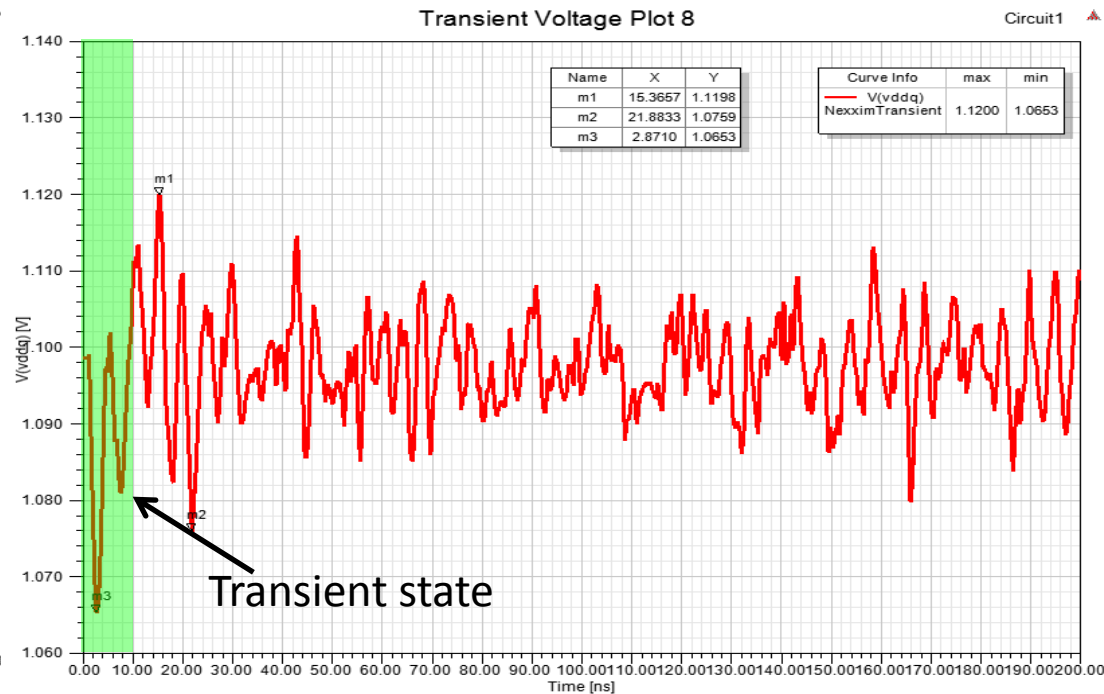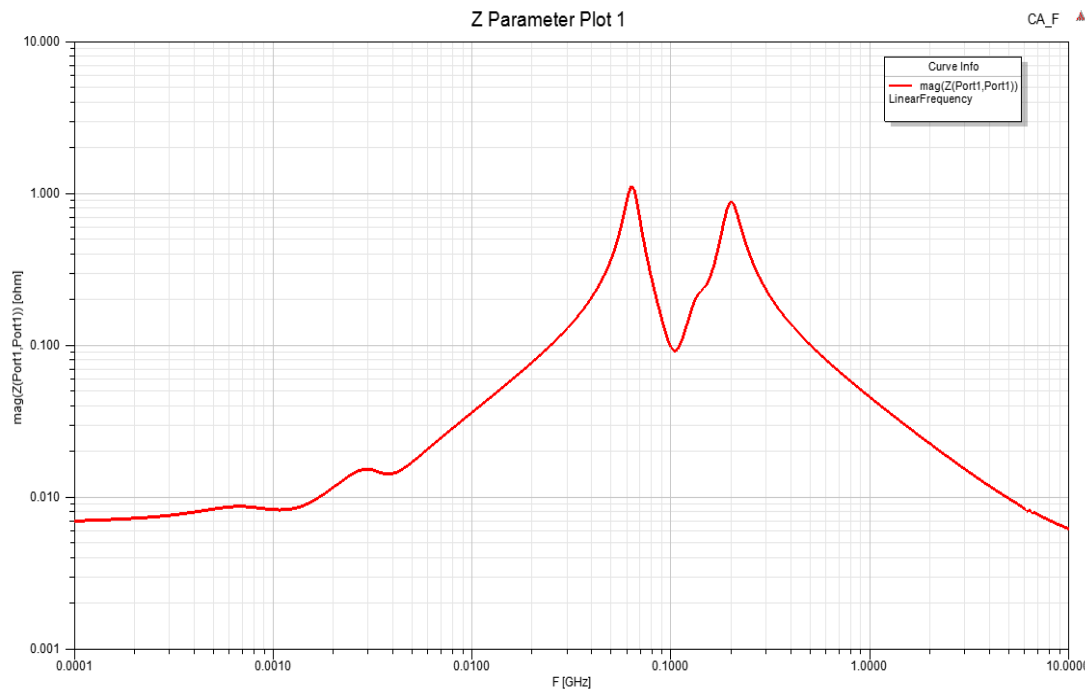- SPEC: +/- 2.5% noise

VDDQLP - Read Mode

DRAM Side (Z Parameter Plot 2)

SOC Side — P2P noise: 19mV (Transient Voltage Plot 7)

DRAM Side — P2P noise: 150mV (Transient Voltage Plot 5)
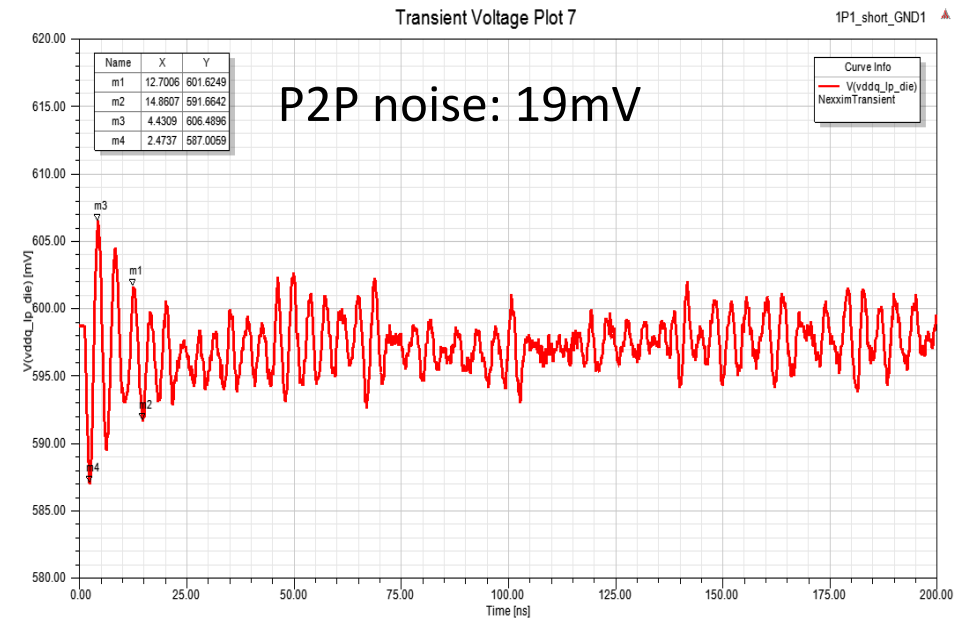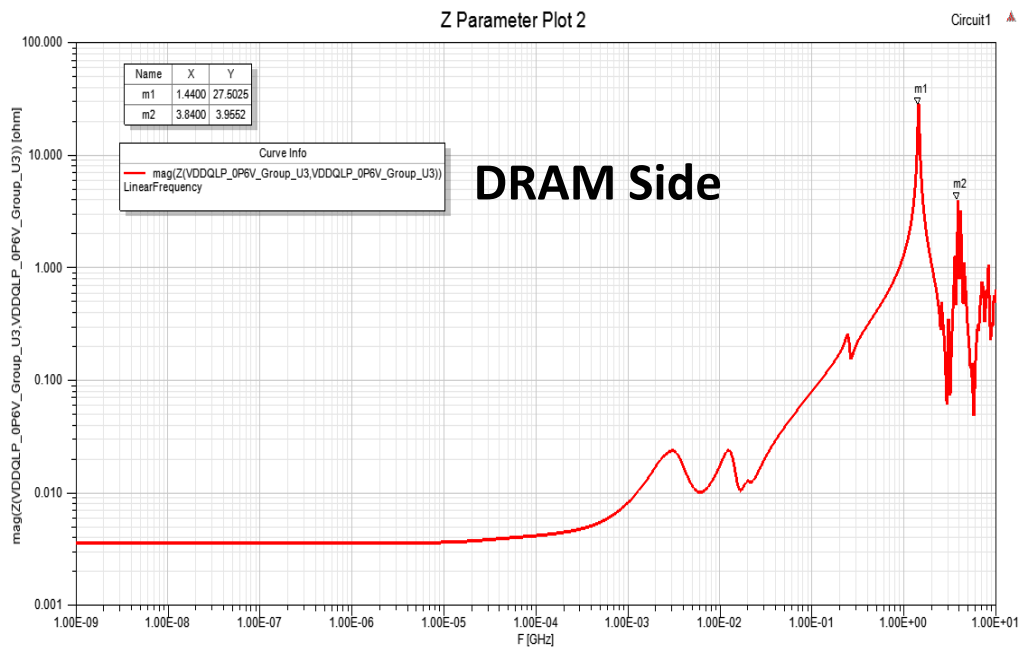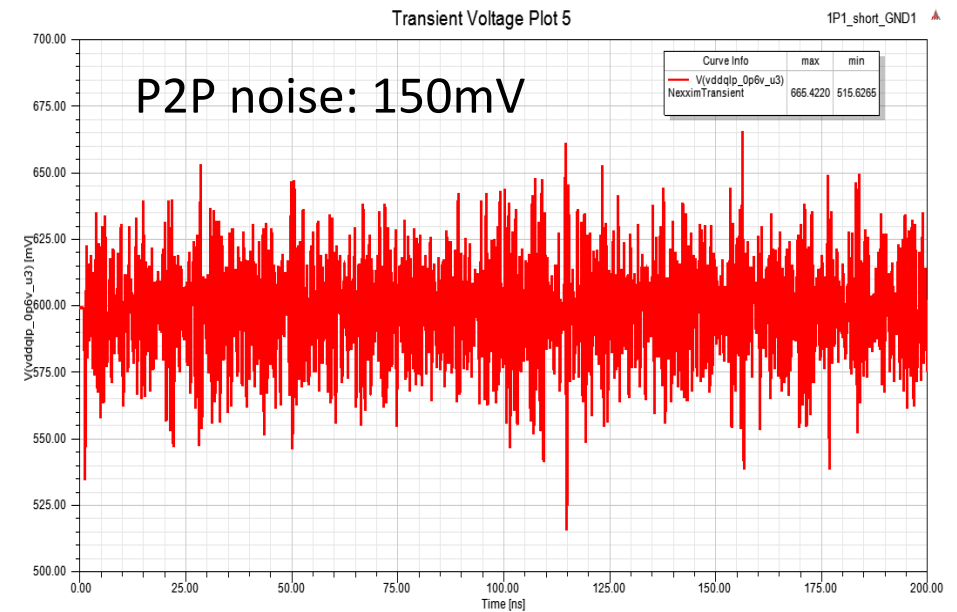
VDDQLP – Target Impedance

VDDQ_DDR- Write Mode

Z Parameter Plot 1 — CA_F

Transient Voltage Plot 8 — Circuit 1

Name	X	Y
m1	15.3657	1.1198
m2	21.8833	1.0759
m3	2.8710	1.0653

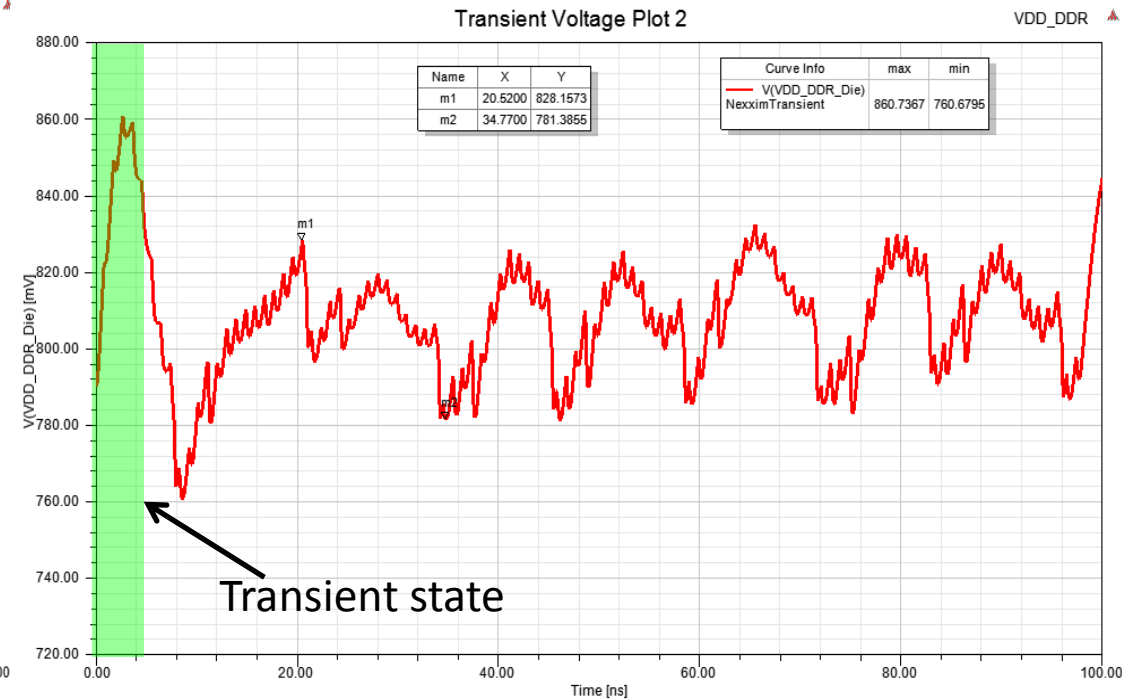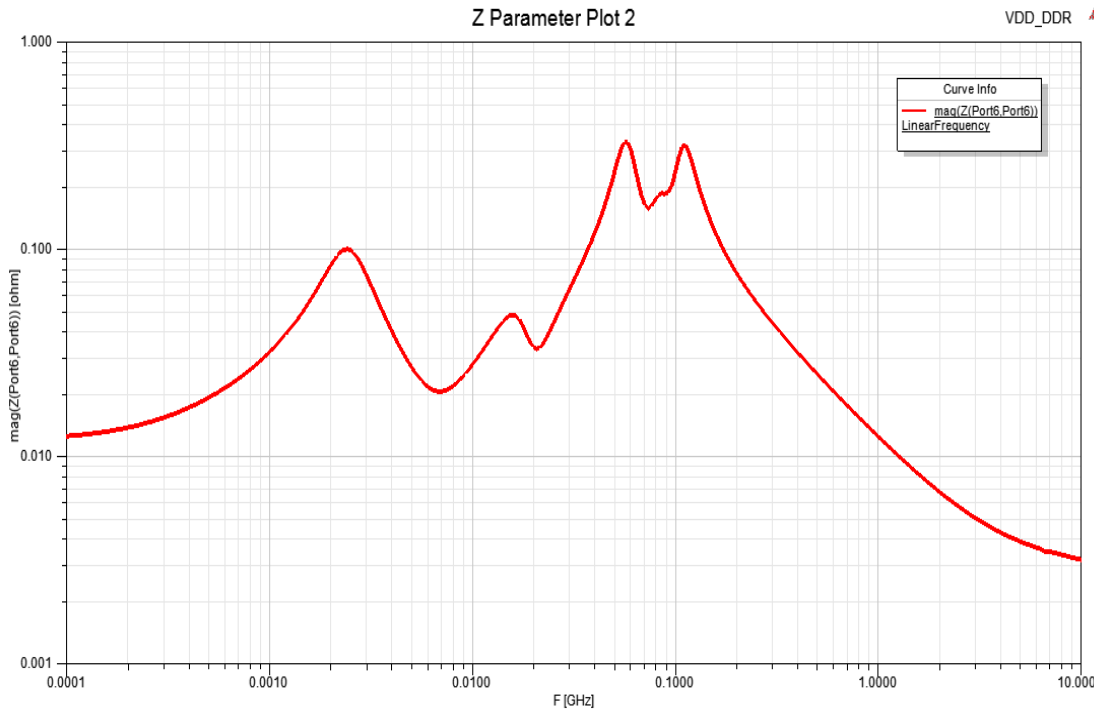| Curve Info	max	min
V(vddq) NexximTransient	1.1200	1.0653

Transient state

- Transient state (0 ~ 10ns):
  - On-die C => 3.6 nF: P2P Noise = 1.3% ~ -3.2%
- Steady state (10 ~ 200ns):
  - On-die C => 3.6 nF: P2P Noise = 1.8% ~ -2.2%

- SPEC: +/- 2.5% noise

VDD_DDR

Z Parameter Plot 2 — VDD_DDR

Transient Voltage Plot 2 — VDD_DDR

Transient state

- Transient state (0 ~ 10ns):
  - On-die C => 12nF: P2P Noise = 7.6% ~ -4.9%
- Steady state (10 ~ 200ns):
  - On-die C => 12 nF: P2P Noise = 3.5% ~ -2.4%

- SPEC: +/- 2% noise

Suggestion

➢ PCB routed skew limits:
  ✓ Length control for each byte: 2mm

Thank You

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