

Synopsys DesignWare IP Support Kick-off Meeting

For Horizon Sigiriya

Zheng Deng, Application Engineer

5th Nov 2021



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Agenda

- Contacts & Project Information
- Project Information (by **Horizon**)
- IP Support
- IP Training & Integration Reviews
- IP Documentation, Download and Notifications
- Support Resources Available Online
- Other useful info

Contacts and Project Information



Key Contact Information

• Customer Team

- Wei Wang (Key Contact/UFS IP Owner)
Shanghai (wei04.wang@horizon.ai)
- Herman Yu (Engineer Manager)
Shanghai (herman.yu@horizon.ai)
- Juncheng Shen (DDR/SPI IP owner)
Shanghai (juncheng.shen@horizon.ai)
- Yujie Ren (PCIE/ETH/PVT IP owner)
Shanghai (yujie.ren@horizon.ai)
- Austin.lin (PCIE/ETH IP owner)
Hongkong (austin.lin@horizon.ai)
- Stanley Sha (MIPI IP owner)
Taiwan (stanley.sha@horizon.ai)
- Wei Yao (DP/eDP/Uart/Timer/Wdt IP owner)
Shanghai (wei.yao@horizon.ai)
- Jianbing Hu (USB/I2S IP owner)
Shanghai (jianbing.hu@horizon.ai)
- Zhiwei Liu (USB IP owner)
Shanghai (zhiwei.liu@horizon.ai)
- Xuan Dong (I2C IP owner)
Shanghai (xuan.dong@horizon.ai)
- Wei Nie (DMA IP owner)
Shanghai (wei.nie@horizon.ai)
- Chaoqiang Chu (GPIO IP owner)
Shanghai (chaoqiang.chu@horizon.ai)

• Synopsys Team

• Post-sales IP Support

- Atharva Akolkar (AMBA Post-sales AE)
Bangalore (atharva@synopsys.com)
- Jaskaran Singh (AMBA Post-sales AE)
Bangalore (jasingh@synopsys.com)
- Lei Cheng (DSC Post-sales AE)
Shanghai (leic@synopsys.com)
- Dehuan Meng (DP/eDP controller Post-sales AE)
Beijing (dehuan@synopsys.com)
- Di Dai (USB controller Post-sales AE)
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- Songwei Chen (USB PHY Post-sales AE)
Shanghai (songweic@synopsys.com)
- Amy Yang (MIPI CSI/DSI Post-sales AE)
Shanghai (leiy@synopsys.com)
- Breeze Shen (MPHY Post-sales AE)
Shenzhen (ren@synopsys.com)
- Cara Wang (UFS controller Post-sales AE)
Shanghai (yangwa@synopsys.com)
- Jesse Yang (ETH controller Post-sales AE)
Shenzhen (jessey@synopsys.com)
- Zhengyi Chen (DDR PHY Post-sales AE)
Shanghai (zhengyi@synopsys.com)
- Xiaoqing Wang (DDR controller Post-sales AE)
Beijing (xiaoqing@synopsys.com)
- Liang Yin (Multi-PHY Post-sales AE)
Beijing (liangyin@synopsys.com)
- Terry Yang (PCIE controller Post-sales AE)
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- Chaoqiang Chu (GPIO IP owner)
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• Synopsys Team

• Pre-sales IP Support

- Zheng Deng (Presales AE)
Beijing (zheng.deng@synopsys.com)

• Program Manager

- Michael Yang (Program Manager)
Shanghai (yangyi@synopsys.com)

• Sales Team:

- Kenny Zhou (IP Product Solution Sales Manager)
Beijing (kun@synopsys.com)
- Tao Du (Executive Account Manager)
Beijing (dutao@synopsys.com)

Product License Information

Note: The correct Project ID and licensed product names are required for core support

- Official Project Name: **Sigiriya**
- The licenses are hosted at: **Horizon (Shanghai) Artificial, Bldg C, No.888, Huanhu West 2nd Rd,, Shanghai, 201306**
- Site ID: **42533**
- Project ID: **Sigiriya (1)**

Product code	Licensed products	Support start	Support end	Comments
E094-0	DWC AP LPDDR5/4/4X Controller	3 rd Nov 2021	2 nd Nov 2023	Config2, Port num TBD
D771-0	dwc_ap_lpddr54_phy_tsmc7ff18	3 rd Nov 2021	2 nd Nov 2023	
C413-0	DWC UFS G4 HC AND UNIPRO	3 rd Nov 2021	2 nd Nov 2023	
7270-0	DWC UFS HC SW	3 rd Nov 2021	2 nd Nov 2023	
C470-0	dwc_mipi_mphy_type1_22_tsmc7ff	3 rd Nov 2021	2 nd Nov 2023	Cust: Metal, Auto Enhance

(1) used during IP installation

Product License Information

Note: The correct Project ID and licensed product names are required for core support

Product code	Licensed products	Support start	Support end	Comments
F319-0	DWC AC PCIe 4.0 Premium AMBA	1 st Mar 2022	28 th Feb 2024	EA, subject to change
D936-0	DWC PCIe Software Sample	3 rd Nov 2021	2 nd Nov 2023	
C118-0	DWC AP Ethernet QOS	3 rd Nov 2021	2 nd Nov 2023	
C432-0	DWC Ether QOS TSN1 Add-on	3 rd Nov 2021	2 nd Nov 2023	
C433-0	DWC Ether QOS RxParser Add-on	3 rd Nov 2021	2 nd Nov 2023	
D473-0	DWC AP Ethernet XGMAC	3 rd Nov 2021	2 nd Nov 2023	
D475-0	DWC XGMAC TSN1 Add-on	3 rd Nov 2021	2 nd Nov 2023	
D476-0	DWC XGMAC RxParser Add-on	3 rd Nov 2021	2 nd Nov 2023	
D474-0	DWC AP Ethernet XPCS	3 rd Nov 2021	2 nd Nov 2023	
C777-0	DWC Ethernet PCS Multiport Add-on	3 rd Nov 2021	2 nd Nov 2023	
G539-0	DWC AP2 MP16G LP TSMC N7 X4	25 th Jan 2022	24 th Jan 2024	EA. Cust: SGMII-1.25G, QSGMII-5G

Product License Information

Note: The correct Project ID and licensed product names are required for core support

Product code	Licensed products	Support start	Support end	Comments
F382-0	DWC AC MIPI CSI2 HP Host Combo	4 th Nov 2021	3 rd Nov 2023	EA, subject to change
E115-0	DWC AP MIPI CD RX 3T4L 45 TSMC N7 NS	23 th Nov 2021	22 th Nov 2022	
B915-0	DWC AP MIPI CSI2 Device Ctlr	3 rd Nov 2021	2 nd Nov 2023	
F985-0	DWC AP MIPI DSI Host Ctrl	3 rd Nov 2021	2 nd Nov 2023	ConfigB
F983-0	DWC AP MIPI D T4 TSMC N7 NS	3 rd Nov 2021	2 nd Nov 2023	
9057-0	DWC MIPI DSI Host SW Sample	3 rd Nov 2021	2 nd Nov 2023	
9058-0	DWC MIPI CSI2 Host SW Sample	3 rd Nov 2021	2 nd Nov 2023	
B150-0	DWC MIPI CSI2 Device SW Sample	3 rd Nov 2021	2 nd Nov 2023	

Product License Information

Note: The correct Project ID and licensed product names are required for core support

Product code	Licensed products	Support start	Support end	Comments
E051-0	DWC VESA DSC Encoder ver 1.2a RTL	3 rd Nov 2021	2 nd Nov 2023	
G260-0	DWC DP-eDP Tx 1.4 with external DSC			
C289-0	DWC DP MultiPixel Mode Add-On	3 rd Nov 2021	2 nd Nov 2023	
C290-0	DWC DP MultiStrmTrsprrt Add-On	3 rd Nov 2021	2 nd Nov 2023	
56764-0	DP Integration CoStart			
A871-0	DWC USB 3.1 DRD-Single Port	3 rd Nov 2021	2 nd Nov 2023	
A875-0	DWC USB 3.1 Hibernation Add-On	3 rd Nov 2021	2 nd Nov 2023	
C391-0	dwc_usb31dptxphy_tsmc7ffns	3 rd Nov 2021	2 nd Nov 2023	Cust: Metal, Auto Enhance
C236-0	dwc_usb2_femtophy_otg_tsmc7ff18_x1ns	3 rd Nov 2021	2 nd Nov 2023	Cust: Metal, Auto Enhance

Product License Information

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Product code	Licensed products	Support start	Support end	Comments
3771-0	DWC APB Peripherals	3 rd Nov 2021	2 nd Nov 2023	
3768-0	DWC AMBA Fabric	23 th Nov 2021	22 th Nov 2022	
3772-0	DWC APB Advanced Peripherals	23 th Nov 2021	22 th Nov 2022	
A415-0	DWC AXI DMAC	3 rd Nov 2021	2 nd Nov 2023	
3889-0	DWC DMA Controller	23 th Nov 2021	22 th Nov 2022	
B858-0	DWC SSI	3 rd Nov 2021	2 nd Nov 2023	
F801-0	DWC SSI Internal DMA	3 rd Nov 2021	2 nd Nov 2023	
D470-0	DWC SPI to AHB Bridge add-on	3 rd Nov 2021	2 nd Nov 2023	

Project Information

Item	Description
Project Name	Sigiriya
Application	ADAS
Process Technology	TSMC automotive 7nm
Package	Flip-chip
Metal Stack	13M_1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2R
RTL Q/A Flow (LINT, CDC etc)	Spyglass
Verification Flow (tools, VIP, methodology)	VCS
Synthesis Flow (tools, methodology)	DC
Physical Design Flow (tools, methodology)	Innovas
System Validation flow (SW, H/W, methodology)	Haps
Project Schedule (start, RTL freeze, ES1 TO, production etc.)	TBD

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

- 384bit total subject to change, may be placed at EW, NS or as L-shape
- Controller follow “LPDDR54_ASILB_Config2” as shown in next page, AXI port number and settings are subject to change

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

set_configuration_parameter DDRCTL_PRODUCT_NAME 2;	DWC-AP-LPDDR54-Controller
set_configuration_parameter MEMC_DRAM_DATA_WIDTH 32	32bit memory datapath
set_configuration_parameter UMCTL2_INCL_ARB 1; # == default value.	AXI Configuration
set_configuration_parameter MEMC_NUM_RANKS 2;	2 ranks system
set_configuration_parameter MEMC_ECC_SUPPORT 1	ECC Support
set_configuration_parameter MEMC_SIDEHAND_ECC 0	No sideband ECC
set_configuration_parameter MEMC_INLINE_ECC 1	Inline ECC
set_configuration_parameter MEMC_USE_RM_W 1; # == default value.	RMW Required
set_configuration_parameter UMCTL2_SBR_EN 1	ECC Scrubber
set_configuration_parameter MEMC_NO_OF_ENTRY 64	64 entries per CAM
set_configuration_parameter MEMC_NO_OF_BLK_CHANNEL 16	16 BLK CHANNELS
set_configuration_parameter UMCTL2_VPRW_EN 1	QoS Enabled
set_configuration_parameter UMCTL2_OCPAR_EN 1	On-Chip Parity Enabled
set_configuration_parameter UMCTL2_OCPAR_ADDR_PARITY_WIDTH 1	On-chip parity address width
set_configuration_parameter DDRCTL_OCSAP_EN 1	On-Chip External SRAM Address Protection
set_configuration_parameter UMCTL2_REGPAR_EN 1	Registers Parity Protection
set_configuration_parameter UMCTL2_REGPAR_TYPE 0; # == default value.	1bit parity for every 32bit register for REGPAR
set_configuration_parameter UMCTL2_OCCAP_EN 1	On-Chip Command and Address Path Protection
set_configuration_parameter UMCTL2_HWFFC_EN 0;# ==default value.	No HWFFC support
set_configuration_parameter UMCTL2_FREQUENCY_NUM 1;# ==default value.	1 set of AC reg. No fast frequency support
set_configuration_parameter UMCTL2_WDATA_EXTRAM 1; # == default value.	External write data SRAM
set_configuration_parameter MEMC_PERF_LOG_ON 1	Performance log
set_configuration_parameter UMCTL2_A_NPORTS 2	2 AXI ports config
set_configuration_parameter UMCTL2_XPI_USE_INPUT_RAR 1	XPI read address output retime to aid timing
set_configuration_parameter UMCTL2_XPI_USE_RPR 1	XPI read data/parity retime to aid timing
set_configuration_parameter UMCTL2_EXCL_ACCESS 0; # == default value.	No Exclusive Access support
set_configuration_parameter UMCTL2_EXT_PORTPRIO 1	External Port priority enabled
set_configuration_parameter UMCTL2_A_LENW 8; # ==default value.	AXI AxLen width support up to 8bits
set_configuration_parameter UMCTL2_A_IDW 6	AXI ID width support up to 6bits
set_configuration_parameter UMCTL2_A_ADDRW 33	Max AXI address bit width

Project Information

AP LPDDR5 CTRL/PHY Configuration and Usage Details

set_configuration_parameter UMCTL2_A_TYPE_0 3; # == default value.	AXI4
set_configuration_parameter UMCTL2_PORT_DW_0 256; # == default value.	256bit port width for 1st AXI port
set_configuration_parameter UMCTL2_A_SYNC_0 1	1st AXI port SYNC interface
set_configuration_parameter UMCTL2_XPI_USE2RAQ_0 1	QoS uses dual RAQ for 1st AXI port
set_configuration_parameter UMCTL2_ASYNC_FIFO_N_SYNC_0 2;# == default value.	
set_configuration_parameter UMCTL2_STATIC_VIR_CH_0 0;# ==default value.	Disable Static VC support for 1st AXI port
set_configuration_parameter UMCTL2_NUM_VIR_CH_0 32	32 dynamic VC support for 1st AXI port
set_configuration_parameter UMCTL2_RRB_EXTRAM_0 1	External RRB SRAM for 1st AXI port
set_configuration_parameter UMCTL2_READ_DATA_INTERLEAVE_EN_0 1; # == default value.	Read data interleave support for 1st AXI port
set_configuration_parameter UMCTL2_AXI_RAQD_0 32	1st AXI port fifo sizing
set_configuration_parameter UMCTL2_AXI_WAQD_0 32	
set_configuration_parameter UMCTL2_AXI_RDQD_0 128	
set_configuration_parameter UMCTL2_AXI_WDQD_0 128	
set_configuration_parameter UMCTL2_AXI_WRQD_0 32	
set_configuration_parameter UMCTL2_A_TYPE_1 3; # == default value.	AXI4
set_configuration_parameter UMCTL2_PORT_DW_1 128	128bit port width for 2nd AXI port
set_configuration_parameter UMCTL2_A_SYNC_1 1	2nd AXI port SYNC interface
set_configuration_parameter UMCTL2_XPI_USE2RAQ_1 0; # == default value.	QoS uses single RAQ for 2nd AXI port
set_configuration_parameter UMCTL2_ASYNC_FIFO_N_SYNC_1 2;# == default value.	
set_configuration_parameter UMCTL2_STATIC_VIR_CH_1 0;# == default value.	Disable Static VC support for 2nd AXI port
set_configuration_parameter UMCTL2_NUM_VIR_CH_1 32	32 dynamic VC support for 2nd AXI port
set_configuration_parameter UMCTL2_RRB_EXTRAM_1 1	External RRB SRAM for 2nd AXI port
set_configuration_parameter UMCTL2_READ_DATA_INTERLEAVE_EN_1 0	Read data interleave support disabled for 2nd AXI port
set_configuration_parameter UMCTL2_AXI_RAQD_1 8	2nd AXI port fifo sizing
set_configuration_parameter UMCTL2_AXI_WAQD_1 32	
set_configuration_parameter UMCTL2_AXI_RDQD_1 16	
set_configuration_parameter UMCTL2_AXI_WDQD_1 128	
set_configuration_parameter UMCTL2_AXI_WRQD_1 32	
set_configuration_parameter MEMC_ENH_CAM_PTR 1;#== default value.	
set_configuration_parameter MEMC_ENH_RDWR_SWITCH 1; #== default value.	
set_configuration_parameter MEMC_RDWR_SWITCH_POL_SEL 1; #== default value.	

Project Information

AP MIPI DSI Host Controller Configuration

Parameter	B
DSI_HOST_AP	1
DSI_HOST_PHY	1
DSI_HOST_DPHY_NUMBER_OF_LANES	4
DSI_HOST_SNPS_PHY	0
DSI_HOST_DATAINTERFACE	4
DSI_HOST_DFLT_F_SYNC_TYPE	2
DSI_HOST_SNPS_SYNC_RD_FIFOS	1
DSI_HOST_DSC_ENC	0
DSI_HOST_PIXELMEMADDRDEPTH	4096
DSI_HOST_GENERICCMDADDRDEPTH	10
DSI_HOST_GENERICPLDADDRDEPTH	64
DSI_HOST_GENERICPLD_RAM_ADDRDEPTH	66
DSI_HOST_GENREADPLDADDRDEPTH	32
DSI_HOST_GENREADPLD_RAM_ADDRDEPTH	34

Project Information

PHY Customization

- Automotive Enhancement, Metal Stack Change
 - C470-0, dwc_mipi_mphy_type1_22_tsmc7ff
 - C391-0, dwc_usbc31dptxphy_tsmc7ffns
 - C236-0, dwc_usb2_femtophy_otg_tsmc7ff18_x1ns
- Support SGMII-1.25Gbps, QSGMII-5Gbps add-on
 - G539-0, DWC AP2 MP16G LP TSMC N7 X4

Project Information

Configuration and Usage Details

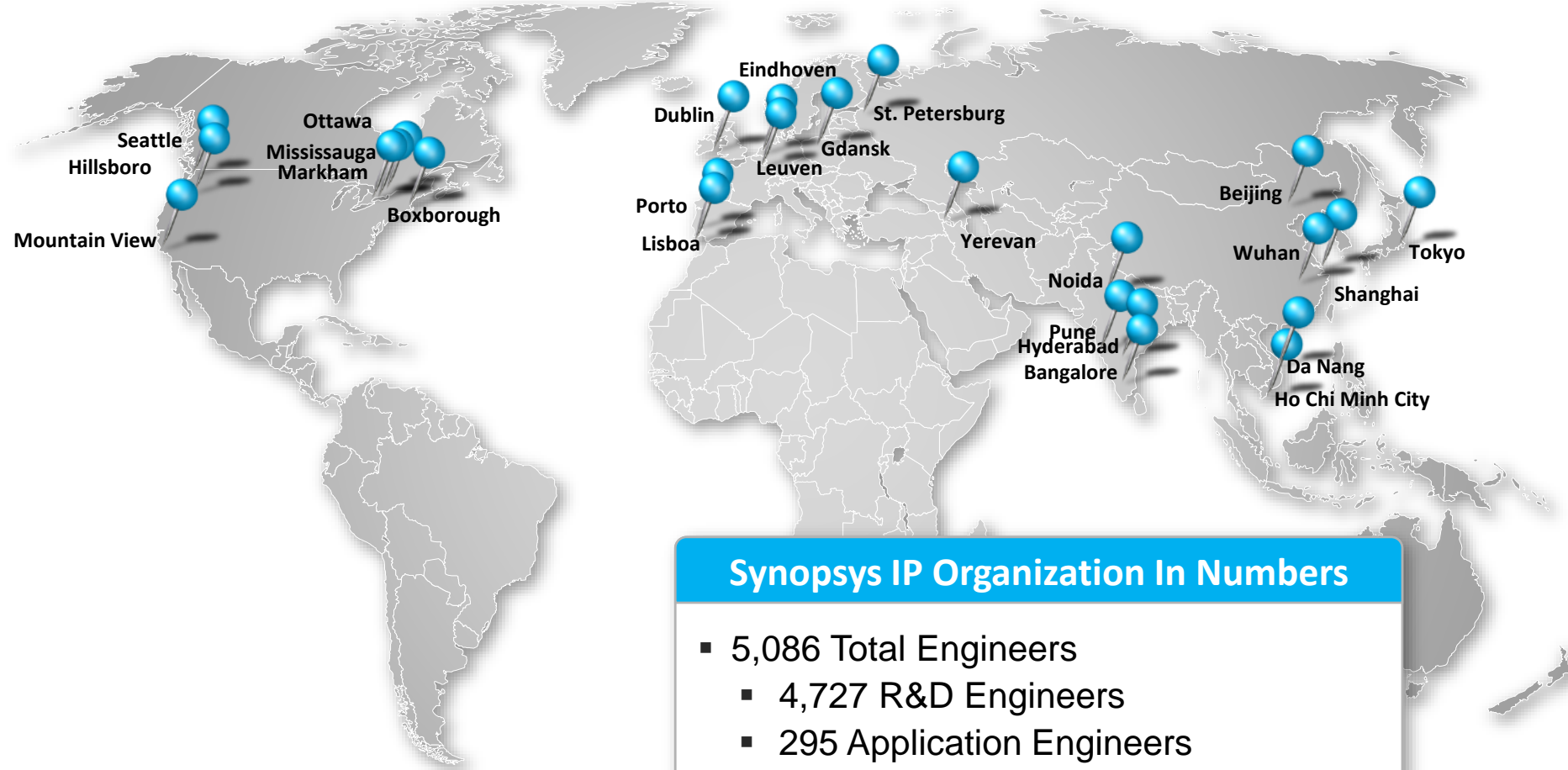
- **NOTE:**

Horizon's project milestones are still TBD, SNPS team will continue to actively follow up to ensure that the internal information is consistent with the Horizon project schedule.

IP Support



Global IP Development And Support



Synopsys IP Organization In Numbers

- 5,086 Total Engineers
 - 4,727 R&D Engineers
 - 295 Application Engineers
 - 64 Program Managers

Technical Support

- Provided by product experts supporting inquiries on
 - Protocol
 - Product architecture, features, specs,
 - Integration, implementation and simulation guidance
 - Silicon bring-up
- SolvNetPlus CRM
 - Main support channel
 - Advanced knowledgebase search
 - Conference calls for in-depth discussions
 - Supplemented by IP designers when deeper design know-how required
 - Detailed SolvNetPlus usage instructions are [here](#)

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PCIe 3.0 (Gen3) Premium Controller EP/RP/DM/SW 32-512 bits with AMBA bridge for Automotive applications
dwc_pcie_express_gen3_prem_amba (5.60a)
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PCIe 3.0 (Gen3) Standard Controller EP/RP/DM/SW 32-128 bits
dwc_pcie_express_gen3_std (5.60a)
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Subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARS), product updates and more.

To subscribe to a component, select from the list of components that you are entitled to below:

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- ☐ DesignWare Analog IP
- ☒ DesignWare Cores
 - ☒ ARC
 - ☒ Bluetooth
 - ☐ dwc_btle154combo_ant (0)
 - ☐ dwc_btle154combo_ble42 (1.00a)
 - ☐ dwc_btle154combo_ble5 (1.00a)
 - ☐ dwc_btle154combo_ble51 (1.00a)
 - ☐ dwc_btle154combo_ble51_mac (1.00a)
 - ☐ dwc_btle154combo_ble5_mac (1.00a)

More IP Resources

- News
- Videos
- Articles
- Customer Successes
- White Papers
- Webinars
- Blogs
- DesignWare Technical Bulletin
- IP Reuse Tools
- myDesignWare Subscriptions

You can manage all your IP subscriptions from a single page <http://www.mydesignware.com>

Several ways to subscribe ...

- You will receive notification emails for each event on the selected IP(s), eg a new release was published, or new STAR was found.
- Once subscribed, you will continue to receive notification emails even after your maintenance has expired, ... until you unsubscribe

dwc_pcie_express_gen4_prem

IP Directory Component Detail

Description: PCIe 4.0 (Gen4) Premium Controller EP/RP/DM/SW 32-512 bits
Name: dwc_pcie_express_gen4_prem
Version: 5.60a
STARs: Open and/or Closed STARs
myDesignWare: Subscribe for Notifications
Product Type: DesignWare Cores
Overview: Product Overview Website
Documentation: Show Documents...
Toolsets: Qualified Toolsets
Download: PCIe_CTLR
Product Code: 0000 0

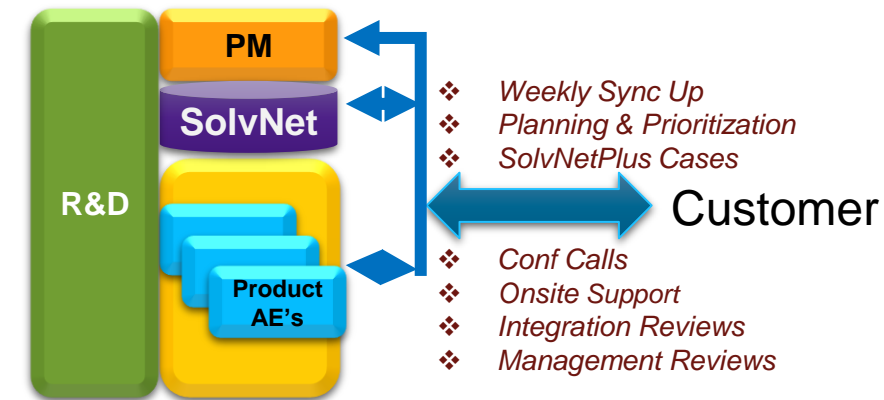
Additional

- We recommend all Project managers to register for IP notifications

Program Manager

Michael Yang

- SNPS's official channel for
 - Communicating Plan of Record & Schedule
 - Tracking the development and delivery of commitments in the SOW
 - Communicating internally and to Customer any changes to the plan of record
 - Publishing weekly program tracking reports
 - Change resolution process
- Customer's focal point for
 - Escalating issues & actions
 - Pulling in the designated experts as required
 - Coordinating special-topic technical meetings & reviews
 - Tracking actions and follow up
 - Mitigation plans of identified risks
 - Focusing SNPS teams in alignment with priorities and critical milestones



IP Training & Integration Reviews





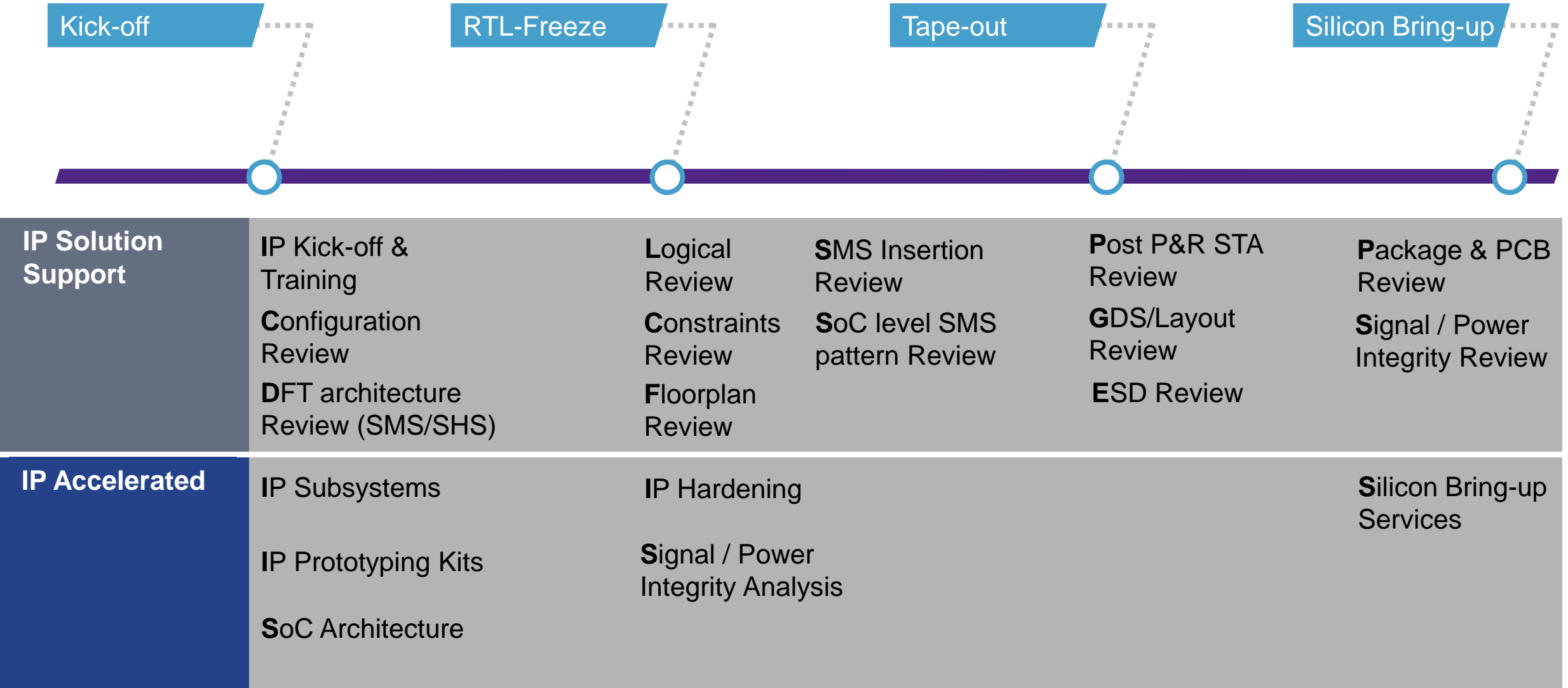
Close Partnership for Success

Align support plan at start & throughout the SOC design, verification & silicon bring-up

Plan & deploy the most effective support solutions by understanding design goals, challenges and risk items

Continuously adapt to project needs by proactive communication of SoC design milestones

Close Partnership for Success



IP Solution Support

IP TRAINING

- **Part of IP Core Support**
- **Interface IP:** Architecture; Usage & Integration; IP Configuration Guidance – register programming
- **Foundation IP:** Memory Compiler/Library portfolio, features & options; Instance/Library selection choice for optimal QoR; SMS training & customized consulting
- **Getting started on the IP:** Installing and understanding the IP deliverables

IP INTEGRATION REVIEWS

- **Part of IP Core Support**
- **Visual reviews based on detailed checklists** to ensure all IP integration & implementation & verification steps completed successfully
- Offering **timely guidance** in the initial, intermediate and final phases of project
- Avoids lengthy silicon debug cycles and expensive re-spins

Significantly reduce the risk of IP integration issues by including Synopsys reviews in your project plan

IP Training: DDR Signal & Power Integrity

DDR Interface

- Interface overview
- DDR Signal Types
- DDRn Synchronous Signaling

PHY IO ring implementation

- PHY SSTL IO library cell overview
- SSTL IO library Si/Pi features
- Si/Pi design constraints on IO ring
- ESD constraints
- Documentation overview

Implementation challenges

- Signal Integrity issues cause “real” problems
- Timing uncertainty
- Regions of timing uncertainty
- Static vs Dynamic uncertainty
- Sources of dynamic interconnect uncertainty

System Implementation

- PCB
- Package
- Skew
- Crosstalk
- Reflections
- Power delivery
- Decoupling
- Vref and VTT

Timing Budgets Calculation

- Timing Relationships
- Timing Budget
 - Read
 - Write
 - Command & Address (CA)
 - CK/CK# to DQS/DQS#

SI/PI Simulations

- Types of simulations
- Common conditions
- Interface model
- Example

IP programmability to improve SI/PI

- Data training
 - Deskew & Strobe Centering
 - Read/Write Leveling
 - VREF training
- IO related
 - Slew-rate control
 - ODT, Zout
- 2T timing
- Data bus inversion

Training slides are typically provided to customers for offline self-pace review, followed by Q&A either offline and/or live meetings to address follow-on questions

IP Integration Reviews

Collaborate to Succeed

Type Of Review	Applicable To	Purpose	Recommended Timeframe
IP Configuration	Solution: Controller + PHY	Review to ensure chosen configuration is suitable for application and there are no gross errors in selection (e.g., performance related parameters)	Project Start (after configuration has been finalized)
Logical Integration	Solution	Visual review of interconnections between controller, PHY, memories, etc.; connectivity for clocks, resets, debug access, Custom I/O and SoC interface; ensure proper connectivity across critical signals; review simulation results etc.	Minimum 4 weeks prior to RTL Freeze
Constraints	Solution	Review usage of combined PHY + controller SDC, deviations from SNPS provided deliverables, guidance to address violations/errors etc.	Minimum 4 weeks prior to RTL Freeze
SMS Insertion	SMS	Review the MBIST architecture and the insertion of various SMS components i.e. Server, sub-server, processors, wrapper etc.. Ensure that connectivity check patterns are validated successfully.	Minimum 4 weeks prior to RTL Freeze
SoC level SMS Pattern	SMS	Review the MBIST test pattern generation strategy considering factors like test time and peak power, provide guidance to optimize the patterns	Minimum 4 weeks prior to RTL Freeze
Floorplan	Solution	High level review of PHY + controller combined floorplan for improved routability, SI etc.	Minimum 4 weeks prior to RTL Freeze
Post P&R STA	Solution	Review detailed STA reports for the PHY + controller combo, ensure that constraints, and timing slacks are adequate across PVT	Minimum 4 weeks prior to tapeout

Customer owns all tool based Subsystem/SoC integration checks


IP Integration Reviews (cont.)

Collaborate to Succeed


Type Of Review	Applicable To	Purpose	Recommended Timeframe
GDS/Layout	PHY+PADs	Review physical layout for recommended guidelines (e.g.,RDL, supply/gnd isolation, clamps, clock nets, DRC/LVS waivers etc.)	Minimum 2 weeks prior to tapeout
ESD	PHY+PADs	ASIC-level ESD review to check for power/gnd assignments, cross-domain protections, SoC's ESD-ground etc.	Minimum 2 weeks prior to tapeout
Pre-TO	Solution	Final check to verify IP version, access to debug ports, Clk/Rst connectivity, any open STARs and sanity check	Minimum of 1 week prior to tapeout
Package / PCB	SoC	Visual review of customer's interface floorplan, package/PCB physical design, including guidelines for stack-up, signal trace width and impedance, power distribution network, reference clock routing to PHY, crosstalk mitigation, etc. Review floorplan at package/PCB pre-layout stage, follow by preliminary layout review, and a final layout review on improvements	After floorplan review
Signal and Power Integrity	TX/RX IO, Interposer, Package, PCB, RX/TX IOs (as applicable)	Review customer's SI/PI simulation report, assessing simulation coverage, results quality against pass criteria. An initial review of the simulation methodology and coverage, and a final review to verify the improvements	After package, PCB and interposer reviews

Flow for IP Integration Reviews


Customer – Opens a SolvNetPlus case

- Specify project name
 - Specify type of review requested
 - Provide (upload) info to be reviewed
- 

SNPS

- Communicates through SolvNetPlus case if further information is needed
 - Carefully reviews the data & provides feedback through SolvNetPlus case
 - Typical duration: 3 to 5 business days
- 

SNPS

- Provides review comments to customer through SolvNetPlus
 - Customer may request a WebEx call if desired
- 

Final Review (optional)

- After customer implements review recommendations a final review is carried out, to ensure all items were properly addressed
- Typical duration: 5 to 7 business days

Silicon Bring-up Service

Thorough Pre- to Post- Silicon Package



SI BRING-UP PLAN REVIEW

Align Schedule
Anticipate Needs
Structure Plan by Stages
Test Setup
Test Equipment
Test Sequence

Pre-silicon



PREEMPTIVE ON- SITE EXPERTISE

Synopsys Engr. on-site
Specific location & period
Broad scope of expertise
Short iteration cycles

Post-silicon



SI BRING-UP TECHN. MGMT.

Track & manage progress
Accelerated analysis &
resolution

Post-silicon



Synopsys Engineer Offering Broad Expertise

Protocol and Conformance Test Suite

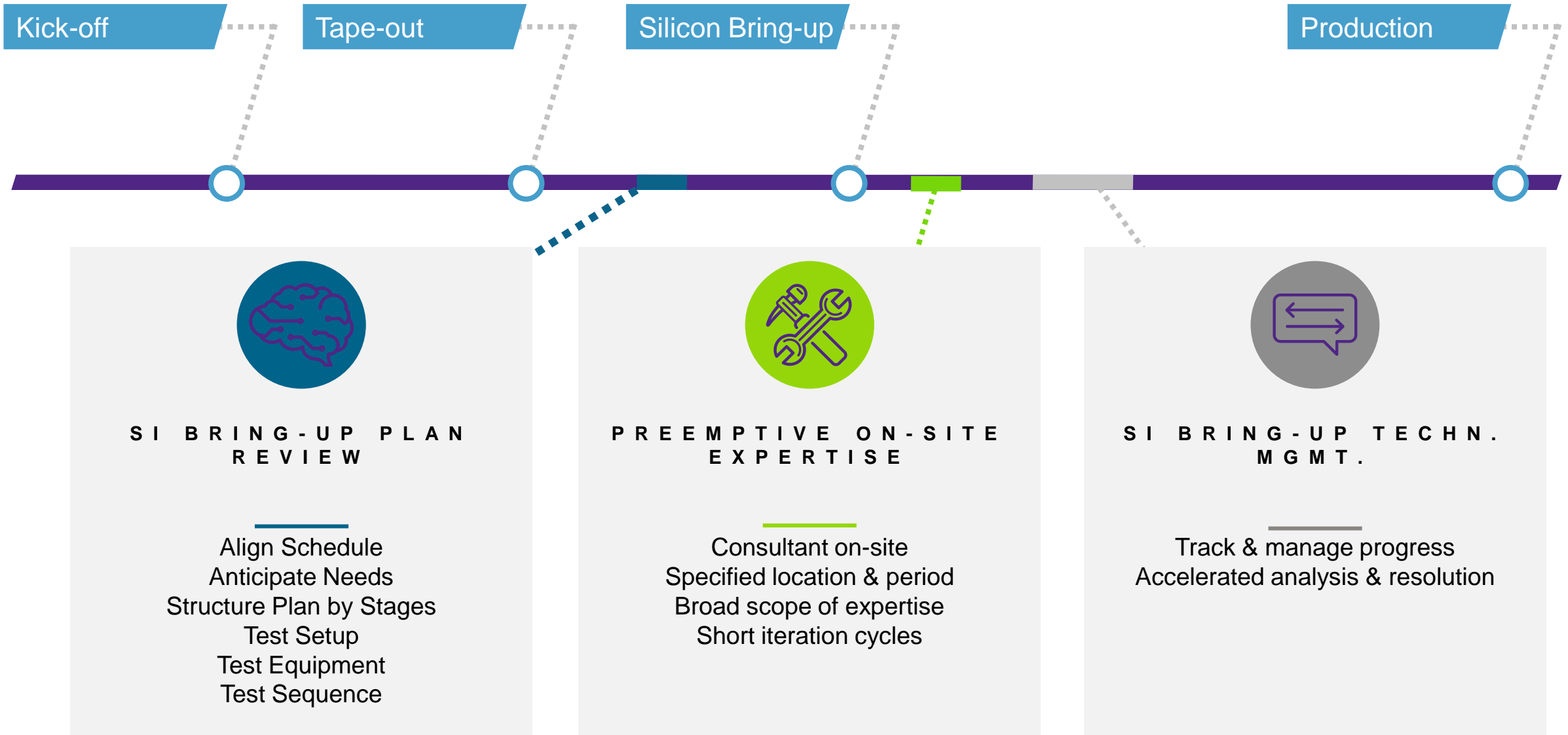
Package and PCB

Laboratory and metrology

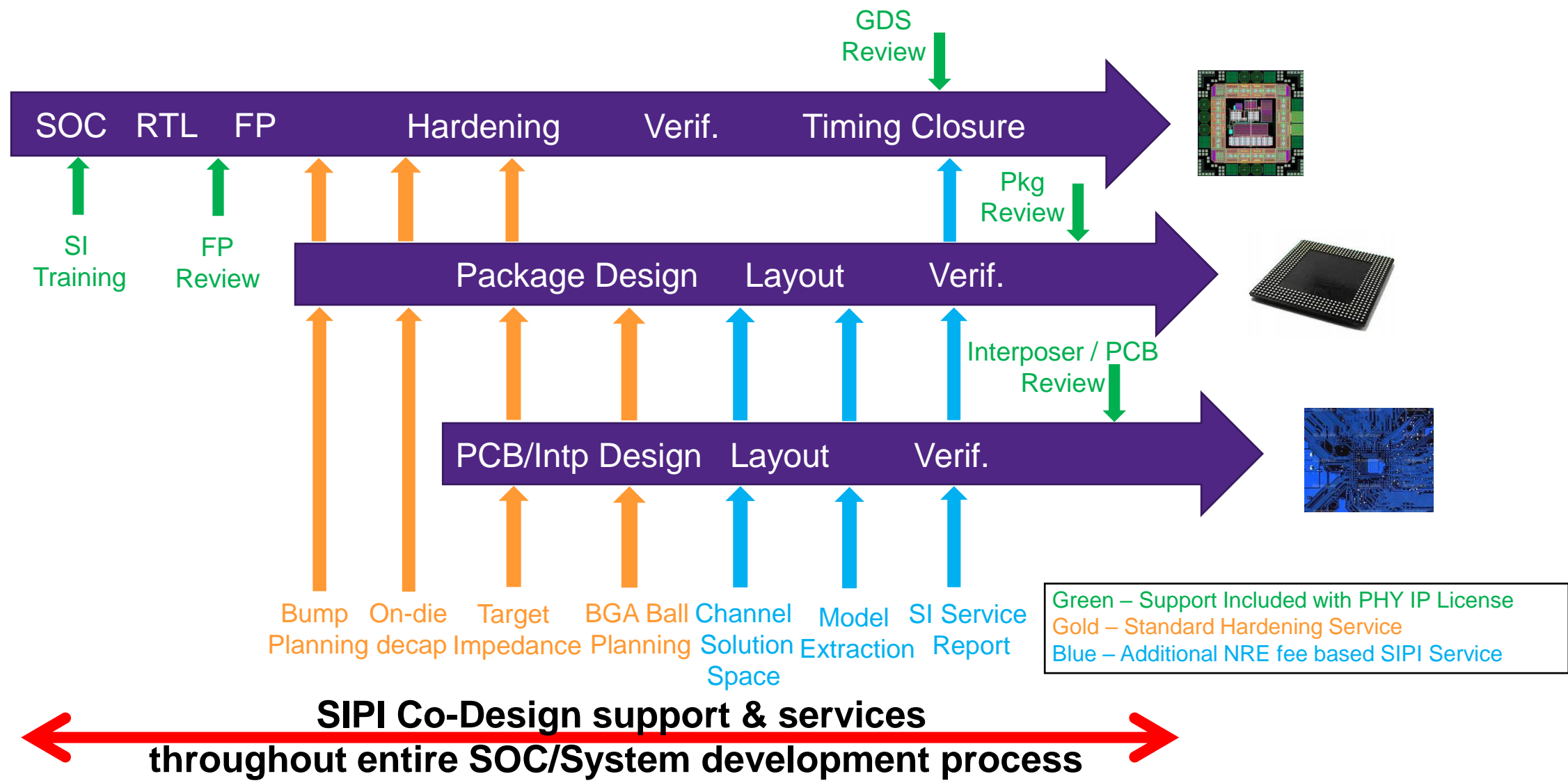
IP integration and usage requirements (RTL to Silicon)

Direct contact window to the multidisciplinary team designing and supporting the IP Solution

Silicon Bring-up Service - Thorough Pre- to Post- Silicon Package



Signal / Power Integrity Analysis Support & Service



Summary

- Close partnership for success
- Plan & deploy the most effective support solutions by understanding design goals, challenges and risk items
- Continuously adapt to project needs by proactive communication of SoC design milestones
- Quickly get up to speed on new IP usage and integration with IP Training
- Avoid lengthy silicon debugs and respins by taking advantage of offered reviews
- Accelerate IP integration and success through available customizable services

IP Documentation, Download and Notifications



DesignWare IP info Page

<http://www.mydesignware.com>

- Login to myDesignWare.com with your SolvNetPlus user ID and password

SYNOPSYS[®] SYNOPSYS.COM | REGISTRATION HELP | 帮助 | 帮助 | ヘルプ

SolvNetPlus

Sign In

Username

Password

Sign In

Need help signing in?

REGISTER - CREATE ACCOUNT FORGOT PASSWORD

© 2019 Synopsys, Inc. 新思 All Rights Reserved. | 京ICP备09052939 SIGN IN SUPPORT | TERMS OF USE | PRIVACY POLICY

DesignWare IP info Page

<http://www.mydesignware.com>

- Login to myDesignWare.com with your SolvNetPlus user ID and password
- Search for your IP or select it from your “myDesignWare list

The screenshot shows the myDesignWare website interface. At the top, there is a navigation bar with the Synopsys logo and links for SYNOPSYS.COM, REGISTRATION HELP, and help in multiple languages. Below this, the myDesignWare logo is displayed. A large banner features a blue and purple abstract design with the text: "COMPREHENSIVE PORTFOLIO OF HIGH-QUALITY IP SOLUTIONS" and "Synopsys offers the industry's broadest portfolio of silicon-proven IP solutions that enable designers to reduce integration risk and accelerate time-to-market." To the right of the banner, there is a "SEARCH TOOLS" section with a search bar labeled "Search for IP..." (highlighted with a red circle), and two buttons: "Analog IP Selector" and "Memory & Logic IP Selector". Below the banner, there is a section titled "DesignWare® IP Component Subscriptions" with a description: "Subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARs), product updates and more." It also includes a link to "Show Legend" and a list of subscription options: "DesignWare Analog IP" (highlighted with a red circle), "DesignWare Cores", "DesignWare Embedded Memory IP", "DesignWare Foundry Sponsored IP", "DesignWare Library IP", "DesignWare Logic Libraries", and "DesignWare STAR Memory System". On the right side, there is a "More IP Resources" section with links to News, Videos, Articles, Customer Successes, White Papers, Webinars, Blogs, DesignWare Technical Bulletin, IP Reuse Tools, and myDesignWare Subscriptions. The footer of the page shows the copyright notice "© 2019 Synopsys, Inc."

DesignWare IP info Page

<http://www.mydesignware.com>

- Login to myDesignWare.com with your SolvNetPlus user ID and password
- Search for your IP or select it from your “myDesignWare list
- Access to Component Details, List of STARs, Documentation, IP download

The screenshot displays the myDesignWare website interface. At the top, the Synopsys logo is visible alongside navigation links for SYNOPSYS.COM, REGISTRATION HELP, and language options (帮助, 帮助, ヘルプ). The main header reads "myDesignWare". Below this is a banner for "COMPREHENSIVE PORTFOLIO OF HIGH-QUALITY IP SOLUTIONS" with a description of Synopsys's silicon-proven IP solutions. The page is titled "DesignWare® IP Component Subscriptions" and includes a section for "Subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARs), product updates and more." A list of components is provided, with checkboxes for various IP types. On the right, a "SEARCH TOOLS" section contains a search bar. Below the search bar, the details for the "dwc_pcie_express_gen4_prem" IP component are shown. This section includes a table with fields such as Description, Name, Version, and Product Type. Key links like "STARs: Open and/or Closed STARs", "Documentation: Show Documents...", and "Download: PCIe_CTLR" are highlighted with red circles. The page also features a "myDesignWare Subscriptions" link at the bottom.

SYNOPSYS.COM | REGISTRATION HELP | 帮助 | 帮助 | ヘルプ

myDesignWare

COMPREHENSIVE PORTFOLIO OF HIGH-QUALITY IP SOLUTIONS
Synopsys offers the industry's broadest portfolio of silicon-proven IP solutions that enable designers to reduce integration risk and accelerate time-to-market.

DesignWare® IP Component Subscriptions
Subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARs), product updates and more.

To subscribe to a component, select from the list of components that you are entitled to below:

Show Legend...

- ☐ DesignWare Analog IP
- ☐ DesignWare Cores
- ☐ DesignWare Embedded Memory IP
- ☐ DesignWare Foundry Sponsored IP
- ☐ DesignWare Library IP
- ☐ DesignWare Logic Libraries
- ☐ DesignWare STAR Memory System

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SEARCH TOOLS

Search for IP...

dwc_pcie_express_gen4_prem

IP Directory Component Detail

Description: PCIe 4.0 (Gen4) Premium Controller EP/RP/DM/SW 32-512 bits
Name: dwc_pcie_express_gen4_prem
Version: 5.00.00
STARs: Open and/or Closed STARs
myDesignWare: Subscribe for Notifications
Product Type: DesignWare Cores
Overview: Product Overview Website
Documentation: Show Documents...
Download: PCIe_CTLR
Product Code: 0922-0

[Additional information for Synopsys employees](#)

myDesignWare Subscriptions

Access to STARs On-The-WEB

- <http://www.mydesignware.com>

Lists of Open and Fixed STARs

- By release version
- Click to get more details
 - Description
 - Versions
 - Configurations affected
 - Workaround
 - Target Fix
- More details may be available from the Support Team (open a SolvNetPlus case)

dwc_pci_express_gen4_prem STAR Report

Open STARs Fixed in 5.60a 5.50a 5.40a 5.30a 5.20a 5.10a

VIEW ALL HIDE ALL SORT BY SEVERITY

HIDE 9001564083 E2-Medium QOR - Use Virtual Clocks for Input/Output Delays

Title: QOR - Use Virtual Clocks for Input/Output Delays

Impacted Configuration:

All versions

Description:

Virtual clocks have been added to the synthesis constraints. These are used to constrain the interface pins. This enables automation of the synthesis flow, with respect to any specific virtual clock, relative to its equivalent physical clock, exclusive of the clock tree.

Before this enhancement,

Design Compiler used the physical clocks to clock the various timing paths including input and output pin constraints.

After this enhancement,

Design Compiler uses equivalent virtual clocks to model Input-Output delays, to more accurately model the latency.

For more information on virtual clock mapping, see "Synthesis Troubleshooting Guide" appendix of the *User Guide*.

VIEW	9001561152	E1-Low	Enhancement: ePTM Support - ePTM Capable bit is Added in PTM Capability . . .
VIEW	9001554799	E2-Medium	Enhancement: Lane Turn off in PIPE SerDes Architecture
VIEW	9001553192	B2-Medium	mac_phy_asyncpowerchangeack Behavior Non-Compliance to PIPE . . .
VIEW	9001552898	E2-Medium	Enhancement: Ack Latency Timer Underflow Prevention During Configuration

Subscribe to IP Notifications

- <http://www.mydesignware.com>

Silicon IP Products Markets Newsletter Customer Success News Resources [Download Brochure](#)

Home / DesignWare IP / IP Search

Search Results for: *pcie controller*

PCIe 3.0 (Gen3) Premium Controller EP/RP/DM/SW 32-512 bits with AMBA bridge for Automotive applications
dwc_pcie_express_gen3_prem_amba (5.60a)
Subscribe | STARS | More Information...

PCIe 3.0 (Gen3) Standard Controller EP/RP/DM/SW 32-128 bits
dwc_pcie_express_gen3_std (5.60a)
Subscribe | STARS | More Information...

SEARCH TOOLS

Search for IP...

Analog IP Selector

Memory & Logic IP Selector

myDesignWare

COMPREHENSIVE PORTFOLIO OF HIGH-QUALITY IP SOLUTIONS
Synopsys offers the industry's broadest portfolio of silicon-proven IP solutions that enable designers to reduce integration risk and accelerate time-to-market.

DesignWare® IP Component Subscriptions

Subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARS), product updates and more.

To subscribe to a component, select from the list of components that you are entitled to below:

Show Legend...

- ☐ DesignWare Analog IP
- ☒ DesignWare Cores
 - ☒ ARC
 - ☒ Bluetooth
 - ☐ dwc_btle154combo_ant (0)
 - ☐ dwc_btle154combo_ble42 (1.00a)
 - ☐ dwc_btle154combo_ble5 (1.00a)
 - ☐ dwc_btle154combo_ble51 (1.00a)
 - ☐ dwc_btle154combo_ble51_mac (1.00a)
 - ☐ dwc_btle154combo_ble5_mac (1.00a)

More IP Resources

- News
- Videos
- Articles
- Customer Successes
- White Papers
- Webinars
- Blogs
- DesignWare Technical Bulletin
- IP Reuse Tools
- myDesignWare Subscriptions

You can manage all your IP subscriptions from a single page <http://www.mydesignware.com>

Several ways to subscribe ...

- You will receive notification emails for each event on the selected IP(s), eg a new release was published, or new STAR was found.
- Once subscribed, you will continue to receive notification emails even after your maintenance has expired, ... until you unsubscribe

dwc_pcie_express_gen4_prem

IP Directory Component Detail

Description: PCIe 4.0 (Gen4) Premium Controller EP/RP/DM/SW 32-512 bits
Name: dwc_pcie_express_gen4_prem
Version: 5.60a
STARs: Open and/or Closed STARs
myDesignWare: Subscribe for Notifications
Product Type: DesignWare Cores
Overview: Product Overview Website
Documentation: Show Documents...
Toolsets: Qualified Toolsets
Download: PCIe_CTLR
Product Code: 0000-0

Additional

- We recommend all Project managers to register for IP notifications

Access to IP Documentation

- <http://www.mydesignware.com>

IP Documentation

- Data books
- Users Manual
- Installation guide
- Release Notes
- Application Notes ...

The screenshot displays the Synopsys website's IP Directory Component Detail page for the `dwc_pci_express_gen4_prem` component. The page features a purple header with the Synopsys logo and navigation links for Silicon IP, Products, Markets, Newsletter, Customer Success, News, and Resources. Below the header, a breadcrumb trail shows the path: Home / DesignWare IP / myDesignWare / dwc_pci_express_gen4_prem. The main content area is titled "IP Directory Component Detail" and contains a table with the following information:

Description:	PCIe 4.0 (Gen4) Premium Controller EP/RP/DM/SW 32-512 bits
Name:	dwc_pci_express_gen4_prem
Version:	5.60a
STARs:	Open and/or Closed STARs
myDesignWare:	Subscribe for Notifications
Product Type:	DesignWare Cores
Overview:	Product Overview Website
Documentation:	Hide Documents...

Below the table, the documentation is categorized into several sections:

- Databooks**
 - [DWC PCIe DM Databook](#)
 - [DWC PCIe DM Databook - with Change Tracking](#)
 - [DWC PCIe DM Registers](#)
 - [DWC PCIe DM Registers - with Change Tracking](#)
 - [DWC PCIe EP Databook](#)
 - [DWC PCIe EP Databook - with Change Tracking](#)
 - [DWC PCIe EP Registers](#)
 - [DWC PCIe EP Registers - with Change Tracking](#)
 - [DWC PCIe RC Databook](#)
 - [DWC PCIe RC Databook - with Change Tracking](#)
 - [DWC PCIe RC Registers](#)
 - [DWC PCIe RC Registers - with Change Tracking](#)
 - [DWC PCIe SW Databook](#)
 - [DWC PCIe SW Databook - with Change Tracking](#)
 - [DWC PCIe SW Registers](#)
 - [DWC PCIe SW Registers - with Change Tracking](#)
- Datasheets**
 - [DesignWare Dual Mode Controller IP for PCI Express Datasheet](#)
 - [DesignWare Embedded Endpoint Controller IP for PCI Express Datasheet](#)
 - [DesignWare Endpoint Controller IP for PCI Express Datasheet](#)
 - [DesignWare Root Port Controller IP for PCI Express Datasheet](#)
 - [DesignWare Switch Port Controller IP for PCI Express Datasheet](#)
- Doc Overview**
 - [DWC PCIe Documentation Overview](#)
- Installation Guide**
 - [DWC PCIe Installation Guide](#)
- Release Notes**
 - [DWC PCIe Release Notes](#)
- User Manuals**
 - [DWC PCIe User Guide](#)

Downloading the IP

- <http://www.mydesignware.com>

Check Readme file first

```
-----
This directory contains a .run file which is a self-extracting image that
contains a DesignWare IP product. The most recent version of this product
is also always available at the following URL:

https://www.synopsys.com/dw/dw1.php?e=PCIe_CTLR

To install this DesignWare IP product, download this file from the above
website or this FTP directory to a UNIX file server:

dw_iip_DWC_pcie_ctl_5.60a.run

Then issue the following command from a UNIX shell to view information
about .run command syntax:

% ./dw_iip_DWC_pcie_ctl_5.60a.run --help

Problems?
-----
o If the .run file does not execute properly, check your permissions.
  Some browsers do not set execute permission for downloaded files.

o Did the installation fail asking for a license? Make sure you have received
  a "project ID" string from your sales representative, a FLEXlm key specific
  to this product, and make sure LM_LICENSE_FILE or SNPSLMD_LICENSE_FILE is
  pointing at the correct license server for that key.
```

See Back up Slides
For more details on IP
download and installation

SYNOPSYS® SILICON DESIGN & VERIFICATION SILICON I

Silicon IP Products Markets Newsletter Customer Success N

Home ▾ / DesignWare IP ▾ / myDesignWare / dwc_pcie_express_gen

DesignWare Download

Directory: /MyProducts/ip/PCIe_CTLR

[SFTP/FTPS Download Instructions...](#)

File	Size	Date
checksum_info.txt	200 B	2019-11-22
dw_iip_DWC_pcie_ctl_5.60a.readme	2 KB	2019-11-22
dw_iip_DWC_pcie_ctl_5.60a.run	226 MB	2019-11-22

Component Versions and Subscriptions		
Component	Version	Notifications ¹
dwc_ap_ccix_25g_prem	5.60a	Subscribe
dwc_ap_ccix_25g_prem_amba	5.60a	Subscribe
dwc_ap_pcie_express_dm_gen2_128b_256b	5.60a	Subscribe
dwc_ap_pcie_express_dm_gen2_32b_64b	5.60a	Subscribe
dwc_ap_pcie_express_dm_gen3_128b_256b	5.60a	Subscribe
dwc_ap_pcie_express_dm_gen3_32b_64b	5.60a	Subscribe
dwc_ap_pcie_express_dm_gen4_128b_256b	5.60a	Subscribe

Support Resources Available Online



Comprehensive Online Support

myDesignWare

Subscribe for proactive release and bug fix notifications

The screenshot shows the myDesignWare page on the Synopsys website. It includes a navigation bar with links like TOOLS, IP, SYSTEMS, SERVICES, SOLUTIONS, SUPPORT, COMMUNITY, and COMPANY. Below the navigation bar, there's a section titled "myDesignWare" with a description: "myDesignWare enables you to receive product information that is of interest to you, such as product updates, technical articles, in-depth application notes and much more. With just a simple click, you can add or remove selected subscriptions at any time." There's also a link to "DesignWare Technical Bulletin" and a section for "DesignWare Component Subscriptions" with a table of components and their versions.

Component	Version	Remove
apb_monitor_vme	6.30a	<input type="checkbox"/>
OW0051	3.80a	<input type="checkbox"/>
dwc_pci_express_ep_128b_x16	4.01a	<input type="checkbox"/>
dwc_pci_express_ep_128b_x8	4.01a	<input type="checkbox"/>
dwc_pci_express_ep_32b_x1-a4	4.01a	<input type="checkbox"/>
dwc_pci_express_ep_64b_x1-a8	4.01a	<input type="checkbox"/>
dwc_pci_express_rc_64b_x1-a8	4.01a	<input type="checkbox"/>
dwc_usb3_phy		<input type="checkbox"/>
dwc_usb3_2_D_device-id	1.04a	<input type="checkbox"/>
dwc_usb3_lpm-hsic_phy-termc_05b	1.2a	<input type="checkbox"/>
OW_0811	1.10b	<input type="checkbox"/>
OW_apb_j2c	1.17a	<input type="checkbox"/>
OW_apb_ftc	2.03a	<input type="checkbox"/>
OW_ams_0t	DW00B_1010	<input type="checkbox"/>

SolvNetPlus

Synopsys Support Portal

The screenshot shows the SolvNetPlus sign-in page. It features the Synopsys logo and the text "SolvNetPlus". Below the logo, there's a "Sign In" section with fields for "Username" and "Password", and a "Sign In" button. At the bottom, there's a link for "Need help signing in?". The footer includes copyright information for 2019 Synopsys, Inc. and links for "REGISTER - CREATE ACCOUNT", "FORGOT PASSWORD", "SIGN IN SUPPORT", "TERMS OF USE", and "PRIVACY POLICY".

STARs On-The-Web

Complete Transparency on bugs

The screenshot shows the STARs On-The-Web report page for the component "dwc_pci_express_ep_128b_x16". It displays a list of open STARs (Synopsys Technical Assistance Reports) with columns for ID, Severity, and Description. The list includes 15 items, each with a "VIEW" link. The first few items are:

- 9000523771 B2-Medium Power Management: LTSSM Cannot Successfully Exit L1 When Core Clock ...
- 9000519992 B2-Medium Gen3: Documentation Error In The Register Map
- 9000519617 B2-Medium IATU A6 Non-SRIOV Core: Translation Of Function Number > 8
- 9000517963 B2-Medium DMA Blases Cycle Bit (CB) Check When Processing a Linked List (LL) Element ...
- 9000516190 B2-Medium DMA: Native DMA Linked List (LL) Element Data Not Stored in DMA Context ...
- 9000514662 B2-Medium LTSSM Delay When Moving From L0 To Recovery Upon Receipt of Insufficient ...
- 9000510759 B2-Medium Gen2/Gen3: Core Does Not Set Speed_Change Bit
- 9000509980 B1-Low coreConsultant Configuration Batch Script Does Not Preserve Changes to ...
- 9000508860 B2-Medium Replay Buffer Might Not Nullify TLP When Parity Error Detected
- 9000508791 B2-Medium Multifunction Endpoint with Virtual Channel Support Causes Incorrect ...
- 9000508758 B1-Low DMA Without Bridge Requires PCIe Core ECRC Support with ECRC Stripping
- 9000508757 B1-Low Gen3: Incorrect Default Value For EQ Registers in Programmable Table Mode
- 9000508650 B2-Medium AXI Bridge Graceful Reset: Core Asserts Bridge_Burst_not Output Signal Too ...
- 9000506185 B1-Low AXI4HB Bridge Master Leda Design Rule Checker Error
- 9000504662 B2-Medium Retry Buffer Auto-calculated Depth is Not Optimal
- 9000503861 B1-Low AXI Bridge Shared Slave: DBI Bursts Longer Than Sixteen Not Possible
- 9000503232 B1-Low Power Management Request To Enter L2 Sometimes Ignored

DesignWare IP Support

For products under a valid core support agreement



SolvNet**Plus**

ONLINE

solvnetplus.synopsys.com

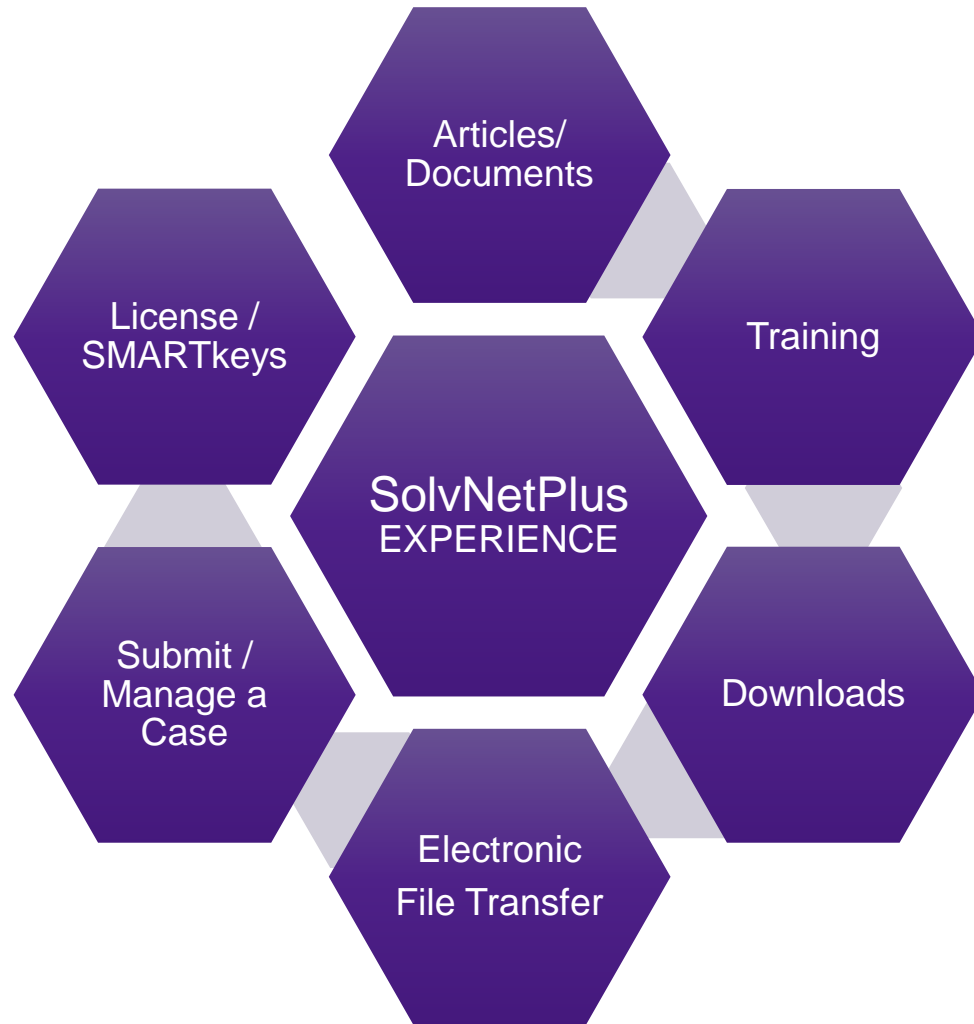
Most efficient method
Extensive Knowledgebase
Support by Worldwide Experts
Acknowledged Within 24hrs



EMAIL

support_center@synopsys.com

Opens SovNetPlus case
Less efficient routing



- Enhanced Search Experience
- Curated Technical Content
- Improved Case Self Service
- Intelligent Recommendations
- Secure Access

SolvNetPlus solvnetplus.synopsys.com

SYNOPSYS®

Integrated Customer
Experience Platform

SYNOPSYS®

SYNOPSYS.COM | REGISTRATION HELP | 帮助 | 帮助 | ヘルプ

SolvNetPlus

Sign In

Username

Password

Sign In

Need help signing in?

REGISTER - CREATE ACCOUNT | FORGOT PASSWORD

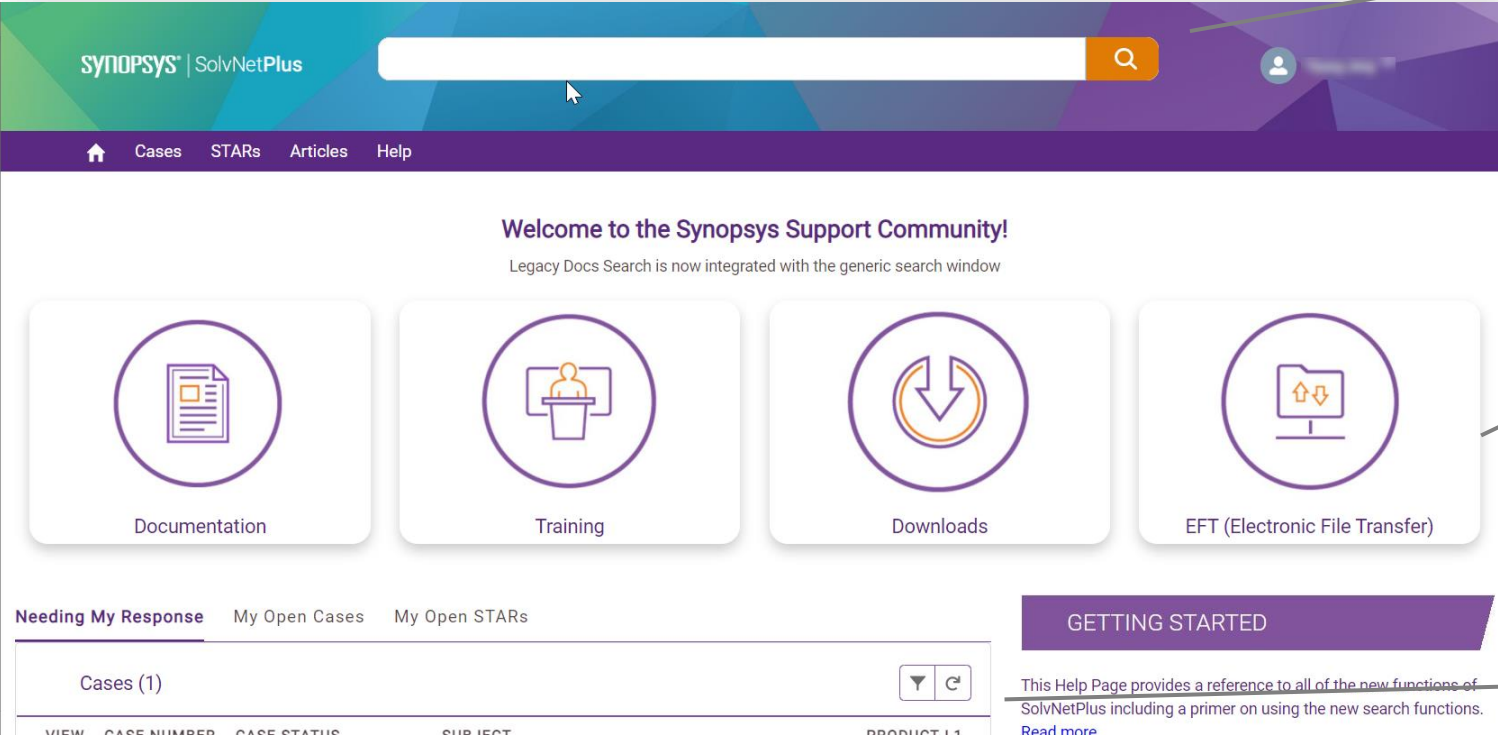
© 2019 Synopsys, Inc. 新思 All Rights Reserved. | 京ICP备09052939 | SIGN IN SUPPORT | TERMS OF USE | PRIVACY POLICY

**Login with
SolvNet(Plus)
credentials**

**Register if you
need an
account**

- Product support portal
- Search knowledgebase for licensed products
- Initiate a support case
- Manage support cases
- Keep track of STARs

SolvNetPlus Overview



Advanced
knowledgebase
search

Navigate to
resources

View cases and
STARs

SolvNetPlus Knowledgebase Search

SYNOPSYS®

Key Highlights

- **Single search interface**
Aggregates results from multiple sources
 - Knowledge Articles
 - Documentation
 - Training
 - Cases & STARs
- **Filters and facets**
Narrow down results
- **Case self-service**
Recommends context-based knowledge solutions
- **Advanced ML capabilities**
Help improve relevance of results over time

The screenshot shows the Synopsys SolvNetPlus Knowledgebase Search interface. The search bar at the top contains the text "MPLL frequency". The left sidebar displays various filters: Product L1 (DesignWare Cores), Product L2 (SERDES, USB, PCIe), Doc Type (Databook, Application Notes, Release Notes, User Guide, White Paper), and Product Line. The main content area shows search results for "MPLL frequency", including a result for "PCle4 PCS for the DesignWare Cores Multi-Protocol 20G PHY" and another for "DesignWare® Cores PCIe 4.0 LP PHY x4 for TSMC 7FF Databook".

SolvNetPlus Create a New Case (1)

Getting started

Navigate to cases

The screenshot shows the Synopsys SolvNetPlus interface. At the top, there's a search bar and a navigation menu with 'Cases', 'STARS', 'Knowledge Base', and 'Feedback'. Below the navigation, there are tabs for 'My Open', 'My Closed', and 'Needing My Response'. The 'My Open' tab is selected, showing a list of 7 open cases. Each case row includes a 'View' link, a case number, a subject, a case severity, a product L1, a case status, and a site. At the bottom of the page, there is a prominent purple button labeled 'Create a New Case'.

VIEW	CASE NUMBER	SUBJECT	CASE SEVERITY	PRODUCT L1	CASE STATUS	SITE
View	00000001	New feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01
View	00000002	Feature: add display	Medium	DesignNet+ Tools	Open	us01
View	00000003	Feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01
View	00000004	Feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01
View	00000005	Feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01
View	00000006	Feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01
View	00000007	Feature: add offer content Product Formatting/Pre-Approval	Medium	DesignNet+ Tools	Open	us01

Create a New Case

Click to create a case

SolvNetPlus Create a New Case (2)

Enter contact, project ID and product information

Select
Appropriate
Product Category

Select Product
Family or Type

Customer Information

Contact: Logo:

*Site:

Product Information

*Product L1:

Release:

Product L2:

OS Affected:

Available:
All Linux
All Wind...

Selected:

Project ID:

Licensed Product:

Recommended Solutions

DOCS - SILICON IP MORE

FILTERS

Docs - Silicon IP

DesignWare Cores PCI Express Controller Release Notes, Version 5.96a July 2

DesignWare Cores PCI Express Controller ... All rights reserved. ... This Synopsys software and all associated documentation are proprietary to Synopsys, ... All other use, reproduction, modification, or distribution of the Synopsys software ...

Docs - Silicon IP

DesignWare Cores Hi-Speed USB On-The-Go Controller Subsystem Linux Driver Software User Guide, Version 3.10b 6/5/201

Copyright Notice and Proprietary Information Notice ... The software and documentation are furnished under a license agreement and may be ... All technical data contained in this publication is subject to the export control ... 4 ... Contents

Docs - Silicon IP

DesignWare Cores SDRAM uPCTL (2.50a) uPCTL (2.50a) Datasheet 11/22/201

Select Site
where IP is
licensed

Select your
Project ID

Select the
Licensed
Product

SolvNetPlus Create a New Case (3)

Accelerate Issue Resolution with Knowledge Recommendations

Create Case

Customer Information

Contact Logo * Site

Product Information

* Product L1 Release

Product L2 OS Affected

Available: All, All Linux, All Wind... Selected:

Project ID Licensed Product

Summary

* Case Type * Case Severity

* Subject

Recommended Solutions

DOCS - SILICON IP MORE Clear All Filters

Product L2:

Docs - Silicon IP

Improving I/O Virtualization Performance with PCI Express 4/9/2010

Storage Figure 1: Non-virtualized system The virtualization of this system begins by ... Virtual System 1 Virtual Processors Virtual Memory Virtual I/O Storage ... Virtualization and resource isolation would prevent the system image with the ...

Docs - Silicon IP

DesignWare Cores PCI Express Controller Release Notes, Version 5.96a July 21

DesignWare Cores PCI Express Controller ... All rights reserved. ... This Synopsys software and all associated documentation are proprietary to Synopsys, ... All other use, reproduction, modification, or distribution of the Synopsys software ...

Docs - Silicon IP

DesignWare Cores PCI Express Controller Release Notes, Version 5.71a 6/15/2020

This Synopsys software and all associated documentation are proprietary to Synopsys, ... All other use, reproduction, modification, or distribution of the Synopsys software ... Contents ... This release note contains the following sections:

Select Sources and filter with facets

Recommends context based knowledge solutions

Recommendations may avoid the need for a case

SolvNetPlus Create a New Case (4)

Enter case details

Critical for
effective issue
communication

Summary

* Case Type

Installation

* Case Severity

Medium

* Subject

Meaningful short summary of situation

* Description

Provide as much detail as possible
- Which Interface, Module, Signal?
- Any useful info to help us understand the issue
- Number your questions (1,2,3) to get well structured, numbered answers
- After saving you can upload files

Customer Tag 1

Customer Tracking Number

Customer Tag 2

CC Contact

--None--
Add Request Manager Role
Add Role Manager
Add Role Manager

Cancel

Save

Severity of issue

Save!

SolvNetPlus Create a New Case (4)

Upload files or add more information

Case Number
00469683

Case Status
Open

Case Origin
4-Solvnets

Clone Case

Write a new comment...

Add Comment

Expand All Collapse All

CASE > 00469683

Attachments

Information
Unless notified otherwise technical data received by Synopsys on this server shall be deemed and treated by Synopsys as being classified under the Export Control Classification Number EAR99 on the Commerce Control List of the U.S. Export Administration Regulations for purposes of export from the United States. If the technical data is otherwise classified, you must provide alternative export control information before submitting the data on this server. If an export license is required, you must notify Synopsys prior to providing the data, by contacting support_center@synopsys.com

Upload Files

Upload any files

- Simulation waveforms
- Testcases
- Block diagrams
- etc.

SolvNetPlus Importance of Site ID, Project ID

- The **Site ID** is a unique number, that Synopsys uses to identify one specific customer site, a customer can have multiple site IDs.
- For each new project Synopsys and Customer define a unique **Project ID**
 - IP licenses are cut for one specific Site ID and one specific project ID
- When entering a new SolvNetPlus ticket, Users must enter their **Site ID**, a valid **Project ID** and select the related **Licensed product**
- The **Project ID** is also used during IP installation
 - during execution of .run file, when prompted, enter the project ID for source code installation (if no Project ID is entered, then the encrypted IP is installed)
- The **Project ID** was communicated to you by Synopsys Sales team
 - it does not appear “in clear text” in the license file you have received

SolvNetPlus View and Manage Cases

Navigate to cases

Click to manage case

Filter case list

Synopsys

SolvNetPlus

Search Synopsys SolvNetPlus....

Search

Logout

Home

Cases

STARs

Knowledge Base

Feedback

My Open

My Closed

Needing My Response

All Open

All Closed

My Open Cases (8)

Filter

Reset

Case Number

Starts with

Subject

Starts with

Case Severity

Product L1

Starts with

Case Status

Starts with

Site

Starts with

Date/Time Opened

Equals

Customer Tag 1

Starts with

Customer Tag 2

Starts with

Tracking Number

Starts with

VIEW	CASE NUMBER	SUBJECT	CASE SEVERITY	PRODUCT L1	CASE STATUS	SITE
View						
View						
View						
View						

Escalation Path



Customer Support Escalation Path

- SolvNetPlus is the primary support channel
- If your support needs aren't being met through SolvNetPlus,
 1. Let the AE assigned to the case know about your dissatisfaction
 2. Follow the escalation path below
 3. Please include the SolvNetPlus CASE number and reason for your escalation

	<i>Interface IP</i>	<i>Foundation IP</i>	
		Embedded Memories, IO Libraries	Logic Libraries
<i>Level 1</i>	Michael Yang , Flora Cheng (Shanghai) Program Manager		
<i>Level 2</i>	Rahul Sachdev Sr Director, Program Management	William Lau Group Director, R&D Engineering	Zeljko Tufekcic Sr Manager, Applications Engineering
			Sumita Mathai Sr Manager, Applications Engineering
<i>Level 3</i>	Jumana Muwafi SVP Engineering and Customer Support		

Other useful info



IP installation: Downloading an IP

- Download IPs from Synopsys web site
 - You can access the IP directly – if you know the link or
 - if you need to “search for an IP” use this link: <https://www.synopsys.com/dw/ipsearch.php>
- To Download an IP you will need
 - a valid SolvnetPlus account (containing the site ID where the IP was licensed)
 - a valid license (not expired) for this IP must be installed on your license server
 - We recommend you read the Readme first
 - Download from Linux or UNIX platform

dwc_pcie_express_gen4_prem

IP Directory Component Detail

Description: PCIe 4.0 (Gen4) Premium Controller EP/DP/DM/SW 32-512 bits
Name: dwc_pcie_express_gen4_prem
Version: 5.60a
STARs: Open and/or Closed STARs
myDesignWare: Subscribe for Notifications
Product Type: DesignWare Cores
Overview: Product Overview Website
Documentation: Show Documents...
Toolsets: Qualified Toolsets
Download: PCIe_CTLR
Product Code: 6932-0

Additional information for Synopsys employees

Readme

```
Synopsys DesignWare IP Products
=====
This directory contains a .run file which is a self-extracting image that
contains a DesignWare IP product. The most recent version of this product
is also always available at the following URL:

https://www.synopsys.com/dw/dw1.php?e=PCIe_CTLR

To install this DesignWare IP product, download this file from the above
website or this FTP directory to a UNIX file server:

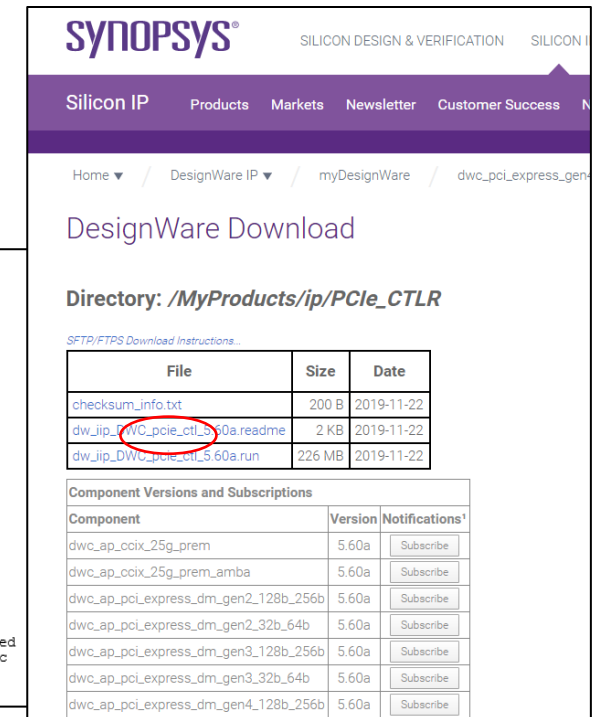
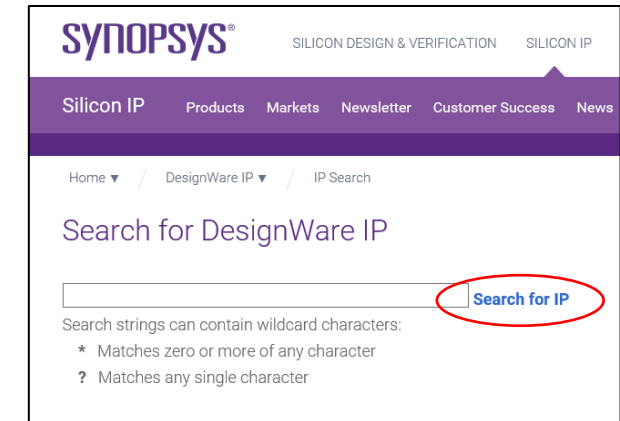
dwc_iip_DWC_pcie_ctl_5.60a.run

Then issue the following command from a UNIX shell to view information
about .run command syntax:

$ ./dwc_iip_DWC_pcie_ctl_5.60a.run --help

Problems?
-----
o If the .run file does not execute properly, check your permissions.
  Some browsers do not set execute permission for downloaded files.

o Did the installation fail asking for a license? Make sure you have received
  a "project ID" string from your sales representative, a FLEXlm key specific
  to this product, and make sure LM_LICENSE_FILE or SNPLMD_LICENSE_FILE is
  pointing at the correct license server for that key.
```



IP installation – Recommended Readings

- Before proceeding to IP installation
 - Read the download README (on each download page)
 - Read the IP install guide (available for each IP title)
 - Several steps are required to install an IP

dwc_pci_express_gen4_prem

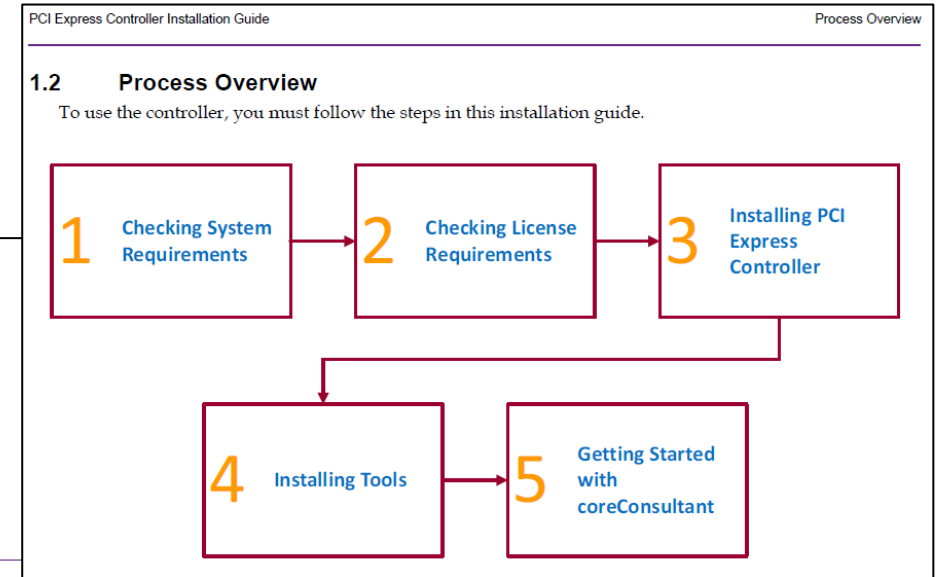
IP Directory Component Detail

Description:	PCIe 4.0 (Gen4) Premium Controller EP/RP/DM/SW 32-512 bits
Name:	dwc_pci_express_gen4_prem
Version:	5.60a
STARs:	Open and/or Closed STARs
myDesignWare:	Subscribe for Notifications
Product Type:	DesignWare Cores
Overview:	Product Overview Website
Documentation:	Show Documents...
Toolsets:	Qualified Toolsets
Download:	PCIe_CTLR
Product Code:	C922-0

[Additional information for Synopsys employees](#)

SYNOPSYS®

DesignWare® Cores PCI Express Controller Installation Guide

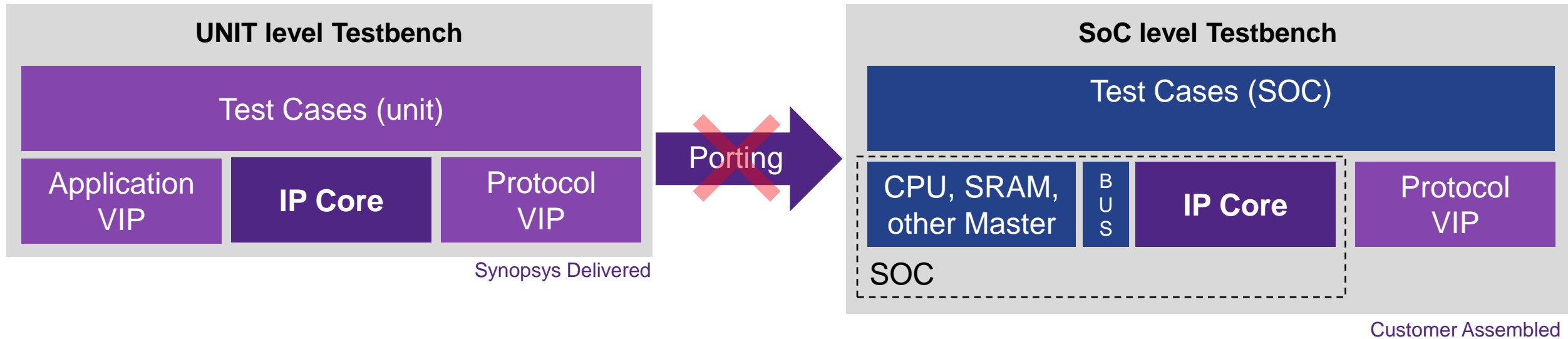


5.60a
November 2019

IP installation (install guide extract)

- When you have downloaded a .run file on your UNIX machine.
- Before executing the .run file
- You must set the SNPSLMD_LICENSE_FILE or LM_LICENSE_FILE environment variable to point at your license server that contains your license key.
- If you use both LM_LICENSE_FILE and SNPSLMD_LICENSE_FILE in your environment, ensure they are set to exactly the same value.
- To set environment variable type for example:
 - % setenv SNPSLMD_LICENSE_FILE
 \${SNPSLMD_LICENSE_FILE}:<my_license_file|port@host>
 - % setenv LM_LICENSE_FILE \${SNPSLMD_LICENSE_FILE}
- Talk to your IT department to know the right settings for LM_LICENSE_FILE and SNPSLMD_LICENSE_FILE variables i.e the logic path to your license server(s)

VIP Support in DesignWare Cores



- Selected DesignWare Cores Digital Controller IP include a VIP based UNIT level Testbench
- Purpose is to confirm the IP deliverables meet the requirements by verifying the interface level testing of the specific IP configuration out-of-the-box in coreConsultant
- Synopsys VIP licenses shipped with DesignWare Cores Digital Controller IP do not include Synopsys VIP support
 - To obtain Synopsys VIP support to build your SoC level verification environment you must obtain a separate Synopsys VIP license

IP Evaluation licenses

- Evaluation licenses are for Digital IP only
- Synopsys does not generate evaluation keys for PHY IP
- Evaluation licenses are limited in time (typically few weeks)
- The following actions are limited to the first 7 days of the evaluation period:
 - The access to IP data page (documentation, STARs, IP download)
 - IP download (download of .run file)
 - IP installation (extraction of IP core kit, i.e execution of .run file)
 - Subscribe to IP notifications (you will continue to receive IP notification after the 7 days until you unsubscribe)
- The following actions are allowed until the end of the evaluation period:
 - Configure an IP and Generate RTL source code using CoreConsultant (GUI tool)
 - Simulate the IP in it's standalone testbench (using Synopsys VIP)

EA (Early Adopter) release delivery

What:

- Specific IP product delivery, not (yet) a standard product, draft documentation only
- EA release may be only verified for the customer configuration (see EA release notes for details)
- Subject to Synopsys Sales and Marketing approval

• Why:

- To enable a customer with an early access to a new IP product or a set of features not yet available or not fully tested

• How:

- EA Delivery process different from Standard IP downloads (customer will receive specific instructions – ShipPortal)
- Specific paperwork and licenses key cutting required

• Logistic and Support:

- Customer to provide: host id, site id, project id, customer contact
- Tight support provided by Synopsys IP Product Engineering and/or IP support team
- Technical kick-off meeting organized to train the customer to specific IP usage
- If no dedicated PM assigned to this project, then the EA delivery is tracked by the Pre-sales AE

Thank You

