Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Memory Model Portfolio
FAQ for All Models

Document Version: **2.0**

Document Date: **July 2018**

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1. General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

2. Memory Model Portfolio

2.1 Introduction

The Cadence® Memory Model Portfolio is a pre-validated system-level emulation solution that provides memory device models for Cadence Palladium® XP, Palladium® XP II, and Palladium® Z1 series systems. An off-the-shelf plug-and-play library, the models in the Memory Model Portfolio (MMP) enable rapid deployment of high-performance system-level acceleration and emulation by providing an extensive array of high quality synthesizable models for industry-standard memory devices that are widely used in networking, storage, wireless, and multimedia applications. MMP memory device families include SDRAM, Flash, SRAM, Cellular SRAM, EEPROM, and various system level devices such as DFI PHY, eMMC, SD Card, UFS, and HMC.

MMP models can enable verification IP reuse by eliminating redundant implementations of memory models that have been customized for specific project environments. The MMP models are built to the specifications of real industry parts and/or are compliant with standards governed devices and protocols.

Additionally, MMP models offer the user high performance with little abstraction. They are tuned for high-end, cycle accurate performance during system level verification and optimized for emulation capacity.

Cadence MMP is a mature memory modeling technology that has been deployed in many emulation environments over many years. The MMP library models not only leverage Cadence's expertise and knowledge in memory modeling but are developed, tested, and qualified by Cadence in real user designs.

This user guide provides information that applies across the portfolio; the topics are not model specific and typically also not release specific. This user guide follows an anticipated MMP use flow. After mentioning some basics about the MMP portfolio documentation, support, licensing, and release, this user guide will discuss managing an MMP install. Install management covers subjects about the release such as downloading and patching an MMP release, navigating the release directory structure, and obtaining release notifications. Then the document turns to compile related topics followed by runtime and debugging related information.

2.2 MMP, Emulation, and Timing Verification

MMP memory models are provided as system level emulation models and **not** as verification IP. This solution addresses use models in the acceleration, transaction-based acceleration, STB, and In-Circuit emulation arenas. The question often arises: “why is it that MMP models do not support modeling of timing?” There are several reasons:

- Firstly, the models are implemented in fully synthesizable RTL as they are required to run in Palladium ICE use mode. Accurate modeling of timing is complex to do in RTL. The implementation of model timing is done through HW counters measuring time and this can be quite expensive in gates, especially considering that there are many timing parameters in a typical memory device datasheet.

- Secondly, at the lowest level it is not possible to model many of the timing parameters because Palladium is a cycle based emulator and therefore timing in fractions of clocks is not possible. Another key issue is that there is no testbench in ICE mode and no event based timing accurate simulator and therefore the Palladium has no concept of real time. In order to model timing at some level a known timing reference in the model is required. This, for example, is the reason for the 1MHz reference clock in the SPI and QSPI models.

- Finally, some functions like the request for erase and program timing modeling are very expensive in Palladium time. For example, a sector erase in the SPI takes minimum 30ms per the spec and up to 400ms. Since Palladium is on average 1000x slower than real life, these functions would take 30s up to several minutes. There are other parameters with even larger times that would result in emulation times of many minutes to complete. Users typically do not want to wait this length of time on an emulation platform as it is an expensive and highly shared resource. In the case of these types of functions we intentionally clock the state machines in the implementation with the Palladium fast clock (FCLK) to ensure they complete as fast as possible in the environment and avoid customers waiting for 20 minutes while a block erase command is running.

3. MMP Basics

This section contains information the user may want to be familiar with prior to purchase and prior to selecting specific models for emulation and acceleration use.

3.1 MMP Platform Support

MMP memory models are provided as system level emulation models and not as verification IP. These models are supported in Classic ICE and IXCOM flows on UXE platforms, including IXCOM SW mode. MMP is intended for use only in Palladium emulation and acceleration flows and is optimized for performance, fully synthesizable, and cycle accurate, but likewise has very limited protocol checking. For system level validation of an SOC on Palladium, MMP is the solution for getting the highest performance and efficiency out of the Palladium environment.

MMP Models are not supported in standalone simulation. For memory model requirements such as protocol based IP validation or the need for detailed timing accuracy in the standalone simulation domain we recommend using the MMAV / Denali products which support timing and other simulation-centric features.

MMP models can be run in IXCOM SW mode as a stepping stone to bring-up the design for IXCOM HW acceleration. The purpose of this step is to validate correctness of compile scripts for IXCOM HW acceleration and to allow users to run short smoke tests to validate that simulation initialization happens correctly, assuming the environment is not dependent on target equipment or other external components. Running full blown tests in IXCOM SW mode is not recommended (except for testing the build with some subset of smoke tests) because the IXCOM SW mode is not optimized for performance.

The memory models in the MMP portfolio will currently support Palladium XP, Palladium XP II, and Palladium Z1 use.

MMP 17.1.0 is compatible with UXE 17.1.0 (IES), UXE 17.5.0 (XCelium), VXE 15.1.0 (IES), and VXE 16.5.0 (XCelium) and their respective newer software releases.

3.2 MMP Catalogue

The MMP Catalogue, which is available in the `docs` directory at the top level of the MMP release contains:

- Up-to-date catalogue listing of all of the contents of the MMP release
- Listings for newer models not yet part of the release but which are available for beta engagements
- One or more pages for each model family with information about vendor, model name, size, and configuration for each available model
- Release level for each model family—Initial Release, Emerging Release, or Mainstream release. See Section 3.6 Model Release Levels for a full explanation of these model maturity levels
- Product levels for each model—mmp_basic or mmp_plus. See Section 3.3 on MMP Licensing and Section 3.7 on Model Product Levels.

- Special markings and notes for models that are in Beta status or have restricted access

Locating Specific Memory Devices

The memory device families listed in the catalogue include a listing of available configurations for that family and are partitioned by vendor.

Users should review the MMP Catalogue to find specific desired parts and configurations and then locate the model within the current MMP release directory structure according to the model name as listed in the MMP Catalogue.

NOTE : The user should thoroughly review the MMP Catalogue for compatible devices and substitute configurations when considering requests for a specific part from the support team.

Memory Device Specifications and Vendor Datasheets

MMP memory models are developed based on either a specification provided through a consortium or other body or based on a vendor datasheet. The title, date, and revision of the specification or datasheet used during model development is recorded in the model User Guide introduction section.

Corporate policy does not allow Cadence to distribute any specification or vendor datasheets to customers. Customers are responsible for acquiring these documents directly from the appropriate specification consortium or vendor.

Likewise, when requesting the implementation of new models it is incumbent upon the user to provide for each requested memory part the relevant vendor, title, date, and revision level for the device and, if the specification or vendor datasheet is draft or pre-publication, the contact information needed to obtain the specification or datasheet for analysis. Cadence and the MMP team will with due diligence attempt to acquire such *advance* specifications and datasheets via existing contacts.

3.3 MMP Licensing

The Memory Model Portfolio product is a licensed product with two product levels. The product level describes what set of models are accessible to user with their purchased product and licensing. The majority of models in the MMP library are available at the MMP_BASIC product level. Some advanced models with complex protocols and complex features are available only at the MMP_PLUS product level.

For details about which models reside in each product level, review the MMP Catalog, where MMP_PLUS models are marked with ***MMP_PLUS*** in the column at the left hand side of the page, or examine the MMP 18.1.0 release structure which contains two product hierarchies -- mmp_basic and mmp_plus – at the top level of the release. Both MMP_BASIC and MMP_PLUS models are assigned a release level and thus may have either a BETA or non-BETA status. BETA models of either product level are not available in the release structure but may be requested.

By purchasing the MMP product customers are granted a license to use the relevant models on Cadence Palladium emulation systems. The Palladium runtime implements a license checkout feature using FlexLM in the UXE/VXE software.

- Access to MMP_BASIC models requires the ACCEL_MEM_VIP license file feature. Access to MMP_BASIC AND MMP_PLUS models requires the ACCEL_MEM_PLUS license file feature.

- Both single user and multi user licenses are available for both product levels.

- Licensing is versioned according to major MMP release. MMP 18.1.0 release models check out license features from 18.1.0 license files. MMP 18.1.0 models do not check out license features from prior to 18.1.0 from license files.

- Each license allows a customer to download a single Palladium database. A customer can use any number of model instances and any number of memory model types in a Palladium DB. That DB, when downloaded, will require a single license checkout. See Section 3.1 MMP Platform Support.

- A Palladium database containing one or more MMP_PLUS models requires a single MMP_PLUS license checkout.

- The license checkout acts on a per download basis and occurs during the runtime host command in Classic ICE flow, during time=0 in IXCOM SW mode, and when the user swaps to hardware in the IXCOM flow.

- A single user license allows one user to download a database containing MMP IP to the Palladium system. A multi-user license allows up to 64 concurrent users to download to the Palladium. Customers with larger installations can purchase multiple copies of either type of license.

- Certain MMP Early Adoption programs may require access to additional license features.

Messaging for Releases MMP 17.1.0 and Earlier
The license checkout generates the following messaging on download:

- *INFO : MEM_IP.... Acquired 'ACCEL_MEM_VIP' license, version '1.0'*

License check-in generates the following messaging on completion of the run.:

- *INFO : MEM_IP: Checking in license.*

Messaging for Releases MMP 18.1.0 and Forward:
The license checkout generates the following messaging on download:

- *INFO : MMP.... Acquired 'ACCEL_MEM_VIP' license, version '18.1', type 'DDR_MOBILE'.*

- *INFO : MMP.... Acquired 'ACCEL_MEM_PLUS' license, version '18.1', type 'DDR_MOBILE'.*

License check-in generates the following messaging on completion of the run:

- *INFO : MMP.... Checking in 'ACCEL_MEM_VIP' license, version '18.1', type 'DDR_MOBILE'.*
- *INFO : MMP.... Checking in 'ACCEL_MEM_PLUS' license, version '18.1', type 'DDR_MOBILE'*

3.4 Model Documentation

For model specific information the individual user guides should be consulted. The `docs` directory at the top level of the release contains the MMP Catalogue, the current version of Release Notes, the user guides for the different model families, and several general MMP user guides that address MMP wide topics or features. Examples of MMP-wide features discussed in general user guide include Debug Display and this MMP FAQ.

For acceleration and emulation information, please reference the user guides mentioned in the Section titled *General Information*.

3.5 Model File Format

The memory models are currently provided in one format: that of encrypted RTL file(s) (*.vp for Verilog based models and *.vhdp for VHDL based models) that target use in the IXCOM flows and Classic ICE flow. The encrypted RTL (*.vp; *.vhdp) file(s) must be synthesized along with other design code prior to acceleration / emulation. Some model families also include wrapper files for various configurations (*.v).

3.6 Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3.7 Model Product Levels

All models in the Memory Model Portfolio are assigned a product level. This product level informs users what set of models are accessible with their purchased product and licensing. The majority of the models in the MMP library are available at the MMP_BASIC product level. Some advanced models with complex protocols and complex features are available only at the MMP_PLUS product level.

In the MMP 18.1.0 MMP Catalog and going forward, MMP_PLUS models are marked with ***MMP_PLUS*** in the column at the left hand side of the page. MMP_PLUS models are, like all models, assigned a release level and thus may have either a BETA or non-BETA status.

Access to MMP_BASIC models requires ACCEL_MEM_VIP licensing. Access to MMP_BASIC AND MMP_PLUS models requires ACCEL_MEM_PLUS licensing. Please see the MMP FAQ User Guide in the docs directory of the installed release of MMP 18.1.0 or later for additional details or consult with your Cadence sales representative.

4. Managing an MMP Install

This section addresses the maintenance activities of downloading an MMP release and the subsequent patching of the release if needed. Users are encouraged to work with the latest MMP release and patch level in order to take advantage of recent fixes. The mechanism for obtaining MMP product notifications is summarized. The release directory structure is described.

4.1 MMP Release Downloads

Just like other software or IP provided by Cadence there are major releases and, when necessary, patches. Currently, one major release is planned for each year.

An MMP major release is a product update that contains:

- Release directory structure with models and requisite side files, user guides
- Updated MMP catalogue in `docs` directory of release with a listing of all available models including newly introduced models that are available for beta use (IR), less mature models that continue to be available as beta use models (ER), and fully released models that are present in the release directory (MR)
- Release specific *Release Notes* document in `docs` directory of release that describes model level changes, bug fixes incorporated since last major release, and information about product changes
- Series of model specific and topical user guides in `docs` directory of release

Customers can directly download the complete library themselves and do not need to request individual models through the AE's or AMT's.

4.2 Obtaining and Installing Releases

The release is downloaded and installed just like other Cadence software using Installscape. Installscape will install a directory structure containing memory model files.

New MMP releases are available via Cadence downloads web site:
http://downloads.cadence.com

Locate the current MMP release from among the currently supported products list.
Click on the link for that product release. Follow the instructions on the DOWNLOADS site for downloading and installing Cadence releases

MMP release numbering now aligns with the other acceleration and emulation products.

The current release is MMP 18.1.0 (MMP181 on downloads page)

The MMP 16.1.0 (MMP161) release life cycle is ended and this release as well as earlier releases are no longer available or supported.

4.3 End of Release and End of Support

Upon scheduled “End of Release,” the MMP release life cycle for that major release is ended and the release is no longer available or supported. When a major MMP release reaches its scheduled “End of Release,” the release is removed from downloads.cadence.com, the associated patches are removed from support.cadence.com, and MMP R&D will require submitted issues to be reproduced in an actively supported release. Repairs are provided in updates and patches to the most recent release.

The End Release schedule is available at support.cadence.com by navigating to Support Home > Software > Product & Release Lifecycle > End Release Dates

The most recent major MMP release is MMP 18.1.0 (MMP181 on downloads page). The schedule for MMP End Release dates is below.

Release	Active Support Begins	Active Support Ends
MMP 16.1.0	6/15/2016	**Ended** (Dec 2017)
MMP 17.1.0	5/31/2017	12/16/2018
MMP 18.1.0	7/31/2018	12/16/2019

4.4 Release Directory Structure

The release directory structure is organized so that the top level has MMP-wide directories and two hierarchies that correspond to the two MMP product levels: mmp_basic and mmp_plus. Brief descriptions of these are as follows:

Directory	**Description**
mmp_version	File contains current MMP major release version number
common	Directory contains file(s) common to many models
docs	Directory contains Release Notes, MMP Catalog, general MMP-wide documentation such as MMP_FAQ_for_All_Models, MMP_Debug_Display, and all family specific model user guides.
misc	Directory contains qlinkSoftware and qlinkPatches scripts used for creating link releases and for applying official MMP patches
utils	Directory contains utility libraries for MMP
mmp_plus	Hierarchy contains MMP_PLUS models. Some models in mmp_plus may instantiate modules inside mmp_basic.

	User scripting should handle such inclusion by adding +incdir/-y options
mmp_basic	Hierarchy contains MMP_BASIC models.

The mmp_basic and mmp_plus hierarchies are both organized into types, vendors and specific parts. For example:

```
sdram/DDR3/micron/mt41j256m8.vp
```

4.5 MMP Patches and Engineering Hot Fixes

ENGINEERING PATCHES and HOT FIXES are intended to address bugs and occasional software enhancements with an emphasis on shorter turn-around time than for major releases. PATCHES and ENGINEERING HOT FIXES are tested to verify that they fix the reported customer problem, and do not undergo the full regression testing that is required by Cadence for other types of software releases.

4.5.1 Obtaining And Installing Patches and Engineering Hot Fixes

New software patches are available via Cadence Online Support (COS) web site:

http://support.cadence.com

On the support.cadence.com site you can navigate to the page as follows: From the pulldown menu: Tools -> Acceleration & Emulation.

Patches on the web site have been tar'ed and compressed to speed transfer. You can choose to download a compressed tar file for a single patch or download a compressed tar file that has all the patches available so far. For example, the file MMP_18.1.0.p1.tar.gz has only a single patch (MMP_18.1.0.p1).

The file MMP_18.1.0_patches.tar.gz is a cumulative compressed tarfile containing all patches released so far for release 18.1.0.

For any technical support issues please open a Case via http://support.cadence.com or send an email to mailto:support@cadence.com. When submitting a new Case via email to the Support Center, the email requires formatting the Subject line of your email with the keyword Submit. You can also send a direct request to our HSV Support Center mailto:cva_support@cadence.com.

Installing the Patch:

1. cd <install-dir>

2. chmod +w .

3. copy the compressed tarfile MMP_18.1.0.p1.tar.gz to the current directory.

4. gzip -d MMP_18.1.0.p1.tar.gz
   (This creates MMP_18.1.0.p1.tar in the current directory.)

5. If a directory named "patch" exists, make it writeable:
   % chmod +w patch

6. tar -xvf MMP_18.1.0.p1.tar
   (This creates file qlinkPatches and a subdirectory MMP_18.1.0.p1 in the patch directory).

7. Invoke qlinkPatches in one of two ways:
   1. Modify the first line in qlinkPatches to point to the correct perl path (version v5.6.1 or higher) and ensure that perl is specified with the -s switch. If there is no PERL executable present, please contact HSV support at the email address above. Invoke:
      qlinkPatches -n

      Select MMP_18.1.0.p1 from the list of patches (if any) and hit enter.

   2. If you prefer not to keep editing the first line in qlinkPatches, then you just need to invoke perl from the command line as follows:
      perl -s qlinkPatches -n

      Select MMP_18.1.0.p1 from the list of patches (if any) and hit enter.

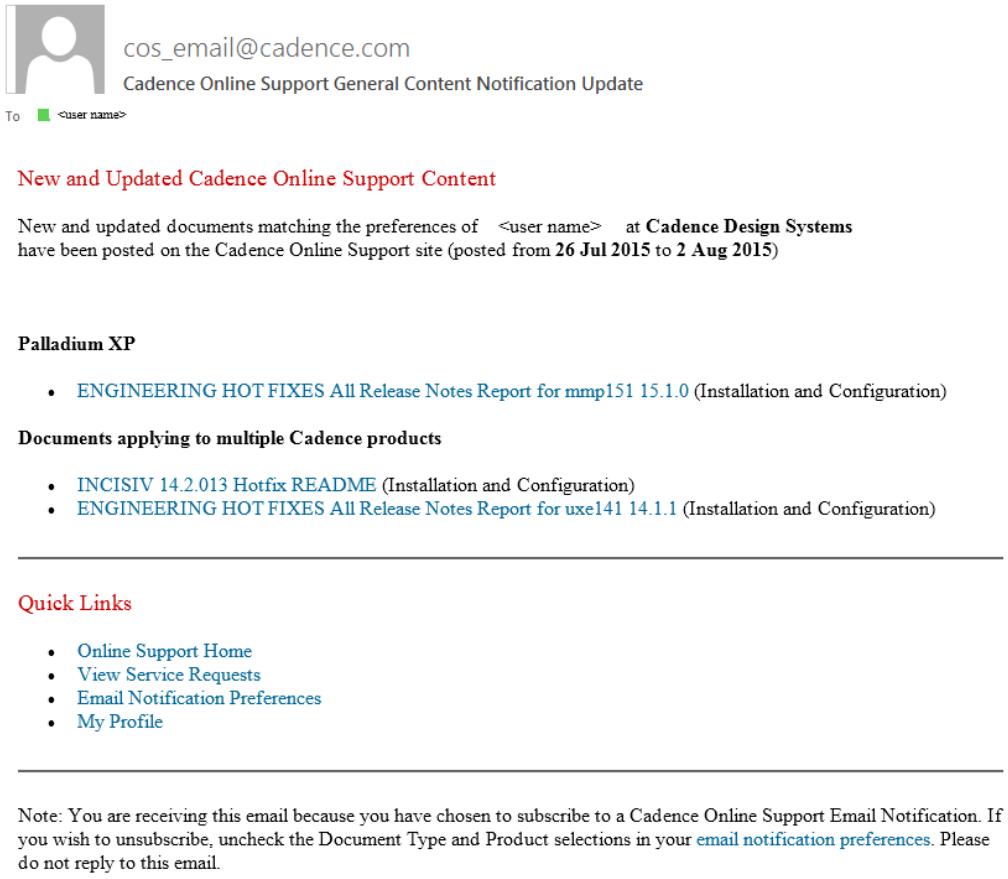
4.6 MMP Product Notifications

Cadence Online Support (COS) users have the capability to opt-in to content and release notifications. For release notifications, users opt-in by release. When a new release becomes available, notification settings for the previous release are inherited. Likewise, the user can manage their COS settings to receive notifications for the MMP product. Notifications include those for both official hot fixes (patches) and for major releases.

General directions for setting up release/update notifications at support.cadence.com are located under Support Home > My Support > My Account & Preferences > Notification Preferences :

Since MMP is a product feature within the Palladium XP, Palladium XP II, and Palladium Z1 products, first edit the product list to include an acceleration/emulation product, then, in step 4, edit the release list to include one or more of the MMP releases.

Once the notification preferences are set up the user should receive via email notifications for MMP product updates and releases. An example of the email notification for a MMP official patch update looks similar to the below with time stamp and affiliation information modified:



cos_email@cadence.com

Cadence Online Support General Content Notification Update

To <user name>

New and Updated Cadence Online Support Content

New and updated documents matching the preferences of <user name> at **Cadence Design Systems** have been posted on the Cadence Online Support site (posted from **26 Jul 2015** to **2 Aug 2015**)

Palladium XP

- ENGINEERING HOT FIXES All Release Notes Report for mmp151 15.1.0 (Installation and Configuration)

Documents applying to multiple Cadence products

- INCISIV 14.2.013 Hotfix README (Installation and Configuration)
- ENGINEERING HOT FIXES All Release Notes Report for uxe141 14.1.1 (Installation and Configuration)

Quick Links

- Online Support Home
- View Service Requests
- Email Notification Preferences
- My Profile

Note: You are receiving this email because you have chosen to subscribe to a Cadence Online Support Email Notification. If you wish to unsubscribe, uncheck the Document Type and Product selections in your email notification preferences. Please do not reply to this email.

Figure 1: MMP Product Official Hot Fix / Patch Update Notification

From the support home page, clicking on the *Acceleration and Emulation Customer Support* link should bring the user directly to the COS page for official patches provided by Acceleration and Emulation Customer Support, including those for the MMP product. On the page for each specific MMP release is a comprehensive Patch Report that lists the content of all relevant patches, as shown below, along with individual downloadable patch files and individual text formatted patch release notes.

```
Patch Report for Release mmp171 17.1.0
=======================================

Patch List: Patches are listed in order of release date.
Retracted patches, if any, are not included in this table.

patch      release date  mandatory?
-----------------------------------
17.1.0.p1   2017/11/15    No

Retracted Patches: This release has no retracted patches.


Obsoleted Patches: This table tells which patches obsolete other patches.
If patch B obsoletes A, and you install patch B, you do not need to
install patch A.

-----------------------------------
None


Bugs Fixed: This table lists the bugs fixed by each patch

patch      CCR        description
---------------------------------------
17.1.0.p1 1765666       DDR4: Request for new Micron 3DS DDR4 model
17.1.0.p1 1594540       FLASH_NAND: Optimize emulation flash models for additional performance
17.1.0.p1 1753332       FLASH_NAND: Request for Micron B17A NAND flash model
```

Figure 2: Example MMP Patch Report And List

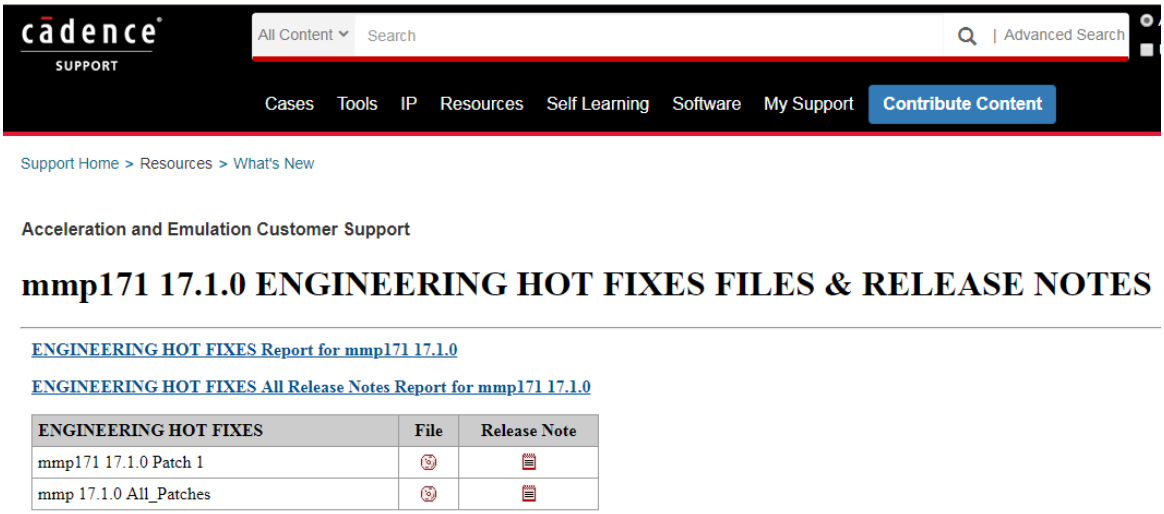


Figure 3: Example Screen for MMP Patch Files & Release Notes

5. MMP Model Compile Tips

This section lists some general suggestions for compiling MMP models within the Palladium environment.

- The memory models are provided in one format: that of encrypted RTL file(s) (*.vp for Verilog based models and *.vhdp for VHDL based models) that target use in the IXCOM SW and HW flows and Classic ICE flow. The encrypted RTL (*.vp; *.vhdp) file(s) must be synthesized along with other design code prior to acceleration / emulation. Some model families also include wrapper files for various configurations (*.v).

- For MMP releases 18.1.0 and onward, all MMP Verilog models require for IXCOM flow use the compile phase inclusion of SystemVerilog MMP utility library related files. Inclusion of this content requires +sv option and path plus filename access to the MMP utility files. The Classic ICE flow does not currently have a requirement for the MMP utility library.

  An IXCOM flow example is shown below:

```
ixcom -64 +sv -ua +dut+$mod_name \
  -incdir ../tb \
  -incdir <path to MMP install >/mmp_18.1/mmp_basic/sdram/LPDDR4/jedec \
  -incdir <path to MMP install >/mmp_18.1/utils/cdn_mmp_utils/sv \
  <path to MMP install >/mmp_18.1/utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
  <path to MMP install >/mmp_18.1/mmp_basic/sdram/LPDDR4/jedec/lpddr4_pd.vp \
  <path to MMP install >/mmp_18.1/mmp_basic/sdram/LPDDR4/jedec/jedec_lpddr4_4Gb.v \
  ../tb/tb_lpddr4_2ch.v
```

  For information about related runtime flow requirements for the MMP utility files, see the section *MMP Model Runtime Tips*.

- The individual user guides have specific information about compilation that usually includes an IXCOM scripting example. Any required side files are mentioned. The user guides for more complex models (e.g. UFS) also provide a list of the source files that are needed for compilation.

- Some models require +sv option for SystemVerilog to be applied during the compile and will error if it is not provided. The user guides for the respective models will indicate such.

- Some models require that the user source additional keepnet scripting as part of the emulation compile script to ensure that necessary nets (e.g. eMMC and its keepnet_FF.qel) are available for forcing at runtime.

6. MMP Model Runtime Tips

This section lists general runtime requirements and specific suggestions for runtime model configuration.

6.1 Runtime Requirements

For MMP releases 18.1.0 and onward, all MMP Verilog models require for use during runtime of IXCOM SW and IXCOM HW flows the loading of a dynamic library *libMMP_utils.so* located in the *utils/cdn_mmp_utils* directory of the MMP install. 64 bit and 32 bit versions of this library are available. MMP models do not require this dynamic library to be loaded during Classic ICE flows.

An IXCOM flow example is shown below:

```
xeDebug -64 --ncsim \
   -sv_lib ../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
   -input auto_xedebug.tcl
```

6.2 Manual Configuring of MMP Models

This section lists some specific suggestions for atypical, non-protocol based, runtime configuring MMP models within the Palladium environment.

Several user test scenarios evolved to rely on manual configuration of writeable mode registers or configuration registers defined in some major memory device families such as the SDRAM and the SPI type families. While MMP strongly recommends following protocol based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments. In the emulation domain targeted by MMP models, the model RTL relies on Palladium implementations of compiler directives to avoid over-optimization of relevant signals along with runtime forcing / releasing techniques for signals to make available manual configuration of such writeable registers.

One example of a need for manual configuration of SDRAM arises when design tests with DFI PHY controllers program the DFI PHY to handle the configuring of a DDRx or LPDDRx memory, including the mode register settings. In the emulation domain served by MMP models, the DFI PHY model does not support either of the optional DFI training interfaces—the PHY Initiated Training Interface or the PHY Master Interface. These designs and test environments may need to configure the DDRx / LPDDRx memory mode registers (MR) directly, without following the standard and recommended initialization sequence that invokes multiple Mode Register Write commands in order to properly configure the mode registers.

To support manual configuration methods some popular MMP memory models are equipped with

- exposed mode register or configuration register declarations
- exposed init_done signal declaration

- synthesis directives, such as keep_net directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing by the user
- user guide and RTL documentation of the mapping from internal signal names to datasheet or specification names for these writeable configuration registers

One may therefore craft a runtime script which arranges runtime forcing of the relevant nets to the desired values instead of the standard configuration commands and initialization sequence. Manual configuration of these models also requires scripting to bring the internal init_done signal high in order to signal to the model core that the initialization sequence is properly completed. This status can also be forced with runtime force commands applied to the model init_done signal.

Please examine the individual MMP model user guides for a list of configurable signals, a mapping to specification or datasheet naming. Mapping details are also provided in the RTL alongside exposed signal declarations. Note that some manually configurable models do NOT have an init_done signal. For example, the DDR2 core has no init_done signal.

Note about risk: Because this technique bypasses standard initialization there is no checking of value range, configuration sequencing, or integrity and internal consistency for the desired scenario. There are no alerts and no messaging to warn about or prevent illegitimate or inconsistent configurations. Any missing or incorrect values forced into configuration register or mode register settings may result in a non-functional or ill-behaved model. Debugging such scenarios is more difficult than average.

An example of forcing a mode register MR2 to be 8'h12 is shown below.

force tb.mmp0.lpddr4_chA.MR2 'h12

Examine the UXE or VXE User Guide for details about runtime force commands. Access the individual MMP model User Guides in the MMP release top level *docs* directory to obtain manual configuration info specific to that family. Review the individual institution specification or vendor datasheet for info about the memory part's mode registers or configuration registers and their fields and values.

7. MMP Model Debugging Tips

This section lists some general suggestions for debugging potential issues for MMP models within the Palladium environment.

- Is the latest MMP Release installed and being pointed to for compile?
- If there is an issue, is the issue reproducible with latest MMP Release?
- Is the clock toggling?
- Is the clock enable asserted (if model has one)?
- Is the reset connected and driven correctly?
- Is the initialization sequence for the model understood? If not, reference the device specification or MMP user guide for the model. Most models will not function or function correctly until initialization is performed correctly.
- **DEBUG DISPLAY FEATURE:**
    - Some commonly used (DDRx, LPDDRx) and more complex (e.g., UFS, HMC) of the MMP models have a DEBUG DISPLAY version available. This capability is based on the Verilog system task $display. The user is provided with some runtime controls that allow them to enable or disable this feature. In addition the controls allow the user to enable or disable specific types of debug messages. For additional detailed information please reference the MMP_Debug_Display.pdf.
- **REFERENCE WAVEFORMS:**
    - Some common models (DDRx, LPDDRx) have reference, or golden, waveforms available in the release within the model directory labeled “golden_waveform”. These waveforms usually show basic initialization, read, and write sequences. A “readme” file lists the content. The waveforms are provided in the VCD format as it is a common format between tools. The waveform database is accompanied by a *.svcf script to source important signals into the display. If a user needs reference waveforms for a model that does not have these in the release, a request may be submitted to Cadence emulation and acceleration support team.
- Some model pins are open drain and may need a pullup. Check the user guide for the individual model to determine if a model has such pins.
- Some models have a VCC_UP pin that can be used to mimic power on scenarios and must be high for normal operation. LPDDR3 is an example of such a model. Check the user guide for the individual model to determine if a model has such pins.
- DDR models and DDR like models require the user to handle the DQS delays (For HyperFlash RDS). See the model user guide for details.

- For Flash programming commands, has the memory been erased with a command or preload with FF"s prior to programming?

    - For Flash device models, the initial state of the memory array is the standard Palladium default of all 0's. Typically, real Flash devices are erased at the factory, with the erase value being FF. Flash programming commands typically require that the array is in the erase state prior to programming. Programming without an erased memory can result in undesired or unexpected results. Erasing the Flash MMP model can be achieved in multiple ways:
        a) Preload the array with a memory init file with all FF's using the Palladium memory –load command
        b) Set the memory using the Palladium memory –set command
        c) Configure the DUT controller to issue the necessary Flash erase commands to the required blocks prior to the programming commands

- Are all preloaded memories loaded before running? For example, tune memory or EXT_CSD reg for the eMMC models or parameter pages for NAND Flash models. These initialization files are typically necessary for the model to function correctly. Failure to load them can result in incorrect functionality.

- Palladium runtime memory load and dump operations support various data formats which can vary the user's load/dump performance and data file content. Please reference the UXE/VXE user guide and command reference manual for more information.

8. Revision History

The following table shows the revision history for this document

Date	Version	Revision
March 2015	1.0	Initial release
July 2015	1.1	Update Cadence naming on front page
September 2015	1.2	General updating including notes about sole model format as *.vp/*.vhdp.
November 2015	1.3	Update MMP platform support info (UXE 14.1.1 and newer)
January 2016	1.4	Clarify emulation flow support to confirm support for IXCOM SW mode and to add Palladium Z1 and VXEreferences.
July 2016	1.5	Remove hyphen in Palladium naming
May 2017	1.6	Update user guide for MMP 17.1.0 release, changes in patch installation notes, and changes in support page navigation and content.
September 2017	1.7	Added “End of Release” section to expand and clarify existing end of release info. Added “Memory Device Specifications and Vendor Datasheets.”
November 2017	1.8	Update Platform Support section to align with currently supported UXE releases.
June 2018	1.9	Update user guide for MMP 18.1.0 release, changes in platform and licensing page content.
July 2018	2.0	Addition of compile and runtime requirements for new utility library. Addition of section on runtime manual configuration support for some models.