Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Microwire Serial EEPROM
Palladium Memory Model
User Guide

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

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Microwire Serial EEPROM Memory Model

1. Introduction

The Cadence Palladium Microwire Serial EEPROM memory models are available with model sizes matching real Microwire Serial EEPROM manufactured by Atmel. Different sizes are available; please consult the memory model catalog for the current available list.

Available Microwire Serial EEPROM Memory models:

- at93c46d.vp : Atmel 1Kbit AT93C46D Microwire Serial EEPROM
- at93c46e.vp : Atmel 1Kbit AT93C46E Microwire Serial EEPROM
- at93c56a.vp : Atmel 2Kbit AT93C56A Microwire Serial EEPROM
- at93c56b.vp : Atmel 2Kbit AT93C56B Microwire Serial EEPROM
- at93c66a.vp : Atmel 4Kbit AT93C66A Microwire Serial EEPROM
- at93c66b.vp : Atmel 4Kbit AT93C66B Microwire Serial EEPROM
- at93c86a.vp : Atmel 16Kbit AT93C86A Microwire Serial EEPROM

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2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

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3. Features

General Features:

- 2Kbit/4Kbit Memory for Atmel AT93CxxA Microwire Serial EEPROM
- User-selectable Internal Organization
  - 1K: 128 x 8bit or 64 x 16bit
  - 2K: 256 x 8bit or 128 x 16bit
  - 4K: 512 x 8bit or 256 x 16bit
  - 16K: 2048 x 8bit or 1024 x 16bit
- Three-wire Serial Interface
- Sequential Read Operation
- 2 MHz Clock Rate
- Self-timed Write Cycle

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4. Devices Supported

The current models support for all the Microwire Serial EEPROM families of ATMEL. Please consult the appropriate vendor site for details on the parts they offer.

Device	Size	Description
AT93C46D	1Kbit	128x8 or 64x16 Microwire Serial EEPROM
AT93C46E	1Kbit	64x16 Microwire Serial EEPROM
AT93C56A	2Kbit	256x8 or 128x16 Microwire Serial EEPROM
AT93C56B	2Kbit	256x8 or 128x16 Microwire Serial EEPROM
AT93C66A	4Kbit	512x8 or 256x16 Microwire Serial EEPROM
AT93C66B	4Kbit	512x8 or 256x16 Microwire Serial EEPROM
AT93C86A	16Kbit	2048x8 or 1024x16 Microwire Serial EEPROM

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5. Model Block Diagram

5.1 Interface Diagram

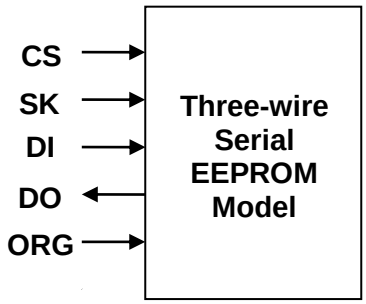

Figure 1: Atmel Microwire Serial EEPROM Model Interface

Table 1: Model Interface Signal Description

Signal	Description	I/O
CS	Chip Select	Input
SK	Serial Data Clock	Input
DI	Serial Data Input	Input
DO	Serial Data Output	Output
ORG	Internal Organization	Input

***Note**: The ORG pin must be connected to VCC or ground. When the ORG pin is connected to VCC, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected.*

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5.2 Connection Diagram

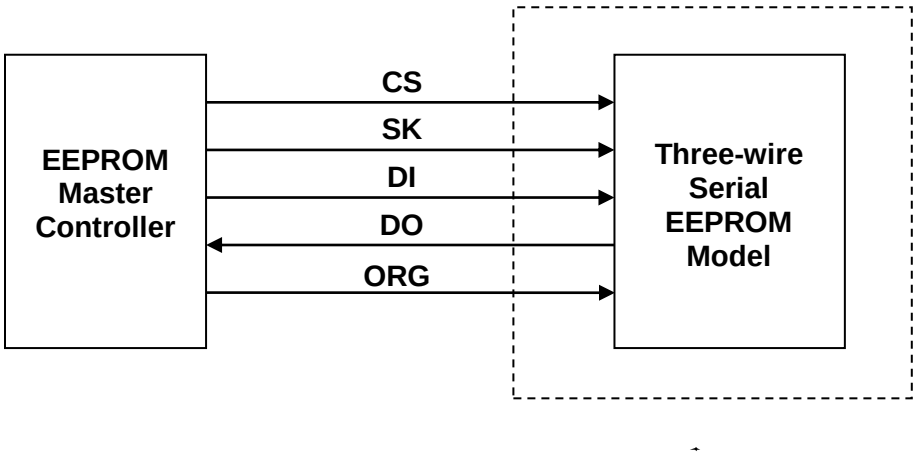

Figure 2: Microwire Serial EEPROM Model Connection Diagram

***Note**: The ORG pin can be connected to VCC or ground to select the x 16 organization or the x 8 organization. But note that, the dynamic switching between them is forbidden.*

6. Limitations

- **Initial Content of the EEPROM Memory —** The initial value of the EEPROM memory array is all 0's after download the model into the Palladium. If you want to use your own initial values, please import them manually using tools supplied by Palladium before running.

- **Ready/Busy Status Output —** When CS is brought “high” following the initiation of a valid programmable instruction, The DO pin outputs the Ready/Busy status of the part. The CS can be brought “high” immediately and don’t have to wait after being kept low for a minimum of 250 ns. A READY/BUSY status can always be obtained.

- **Configuration —** The AT93C46E part is only available with 16bit organization. The user is required to tie the ORG pin on the model to 1 to select the correct organization.

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7. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) of this model in the IXCOM flow is shown below.

```
ixcom -ua +dut+at93c56a \
    ./at93c56a.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile at93c56a.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog at93c56a.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol –keepAllFlipFlop
at93c56a
……

2)
vavlog at93c56a.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog at93c56a.vg at93c56a
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

8. Model Emulation Notes

Below are some considerations for building and running the Microwire Serial EEPROM model in Palladium emulation.

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- The Microwire Serial EEPROM model top-level declaration is unprotected as is the pd_memcore memory.
    - The main data array is called *U_pd_memcore.memcore*

- The top-level module in the Microwire Serial EEPROM modules is called “at93c56a” or “at93c66a” as needed. To use the model in your design, please instantiate the top-level module and map its ports to your actual wires. For more details of the top-level declaration, please open the netlist with a text viewer and search the string “module” to find out its exact name. Below is the port declaration of the top-level model of at93c56a:

```
module at93c56a (SK, CS, DI, DO, ORG);
    input SK;
    input CS;
    input DI;
    input ORG;
    output DO;
endmodule
```

- The initial content of EEPROM memory is all ‘0’ at start-up. The content of EEPROM can be initialized to all ‘1’ in Memory tab of questDebug GUI or by issuing commands in the questQel console as below:

```
QEL> memory -set <dspath>.U_pd_memcore.memcore
```

  To check the full path of the U_pd_memcore, please go to to the Memory tab in questDebug, or invoke the *memory* command in the questQEL console. Below is an example to get the memory path in the design.

```
QEL> memory
```

  The user can also erase the flash memory to all ‘1’ by invoking the Bulk Erase (BE) instruction after emulation has been started.

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Revision History

The following table shows the revision history for this document

Date	Version	Revision
Feb 2012	1.0	Initial version
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name. Update UXE / IXE documentation reference titles. Review and update user guide. Changed name from Three-wire Serial EEPROM to Microwire Serial EEPROM to align with catalogue entry.
March 2015	1.3	Update related publications list.
July 2015	1.4	Update Cadence naming on front page
September 2015	1.5	Add an example for compile
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming
January 2018	1.8	Modify header and footer
July 2018	1.9	Update for new utility library

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