Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Quad SPI Flash
Palladium Memory Model
User Guide

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

Quad SPI Flash Memory Model

1. Introduction

The Cadence Palladium Quad SPI Flash Memory model is now available in Verilog based format (*.vp) for some families with configurations matching real Quad SPI flash parts manufactured by Winbond.

Various sizes are available. Please consult the memory model catalog for the currently available configurations list.

Quad SPI Flash memory models available in Verilog based protected RTL (*.vp) format:

Vendor	Part Number	File Name of Reference Datasheet	Revision	Revision Date
Winbond	w25q256fv	w25q256fv.pdf	Rev H	February 11, 2015
	w25q256jw	Preliminary W25Q256JW DTR RevA 01302015.pdf	Rev A	January 30, 2015
Micron	mt25qu128aba (Beta)	MT25Q_QLHS_U_128_ABA_0.pdf	Rev I	May 2017
	mt25ql128aba (Beta)	MT25Q_QLHS_L_128_ABA_0.pdf	Rev I	September 2016
	mt25qu256aba (Beta)	MT25Q_QLJS_U_256_ABA_0.pdf	Rev I	July 2017
	mt25ql256aba (Beta)	MT25Q_QLJS_L_256_ABA_0.pdf	Rev I	July 2017
	mt25qu512abb (Beta)	MT25Q_QLKT_U_512_ABB_0.pdf	Rev E	June 2017
	mt25ql512abb (Beta)	MT25Q_QLKT_L_512_ABB_0.pdf	Rev E	June 2017
	mt25qu01gbbb (Beta)	MT25Q_QLKT_U_01G_BBB_0.pdf	Rev C	December 2017
	mt25ql01gbbb (Beta)	MT25Q_QLKT_L_01G_BBB_0.pdf	Rev E	December 2017
	mt25qu02gcbb (Beta)	MT25Q_QLKT_U_02G_CBB_0.pdf	Rev D	October 2016
	mt25ql02gcbb (Beta)	MT25Q_QLKT_L_02G_CBB_0.pdf	Rev C	October 2016
	mt25tu256 (Beta)	MT25T_QLHS_U_256_xBA_0.pdf	Rev D	September 2016
	mt25tl256 (Beta)	MT25T_QLHS_L_256_xBA_0.pdf	Rev F	June 2016
	mt25tu512 (Beta)	MT25T_QLJS_U_512_xBA_0.pdf	Rev D	February 2017
	mt25tl512 (Beta)	MT25T_QLJS_L_512_xBA_0.pdf	Rev G	June 2016
	mt25tu01g (Beta)	MT25T_QLKT_U_01G_xBB_0.pdf	Rev C	March 2017
	mt25tl01g (Beta)	MT25T_QLKT_L_01G_xBB_0.pdf	Rev E	October 2016

NOTE: The above Micron part models are currently available in Initial Release (IR) BETA program only. These models are not in the official MMP release. Please request access to these model via an FAE, the emulation support team, or the MMP support team.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Table 1: Release Level for MMP Models

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Features

The Winbond SPI memory model supports all the commands for 3-Byte address mode and 4-Byte address mode, SPI/Dual, SPI/Quad, SPI, and QPI mode.

Table 2: Feature List for Winbond Models

Features		Support		Notes
		w25q256fv	w25q256jw	
Write Operations	Write Enable	Yes	Yes	
	Write Disable	Yes	Yes	
	Write Enable for volatile status register	Yes	Yes	
Register Operations	Read Status Register-1	Yes	Yes	
	Write Status Register-1	Yes	Yes	
	Read Status Register-2	Yes	Yes	
	Write Status Register-2	Yes	Yes	
	Read Status Register-3	Yes	Yes	
	Write Status Register-3	Yes	Yes	
	Read Extended Address Register	Yes	Yes	
	Write Extended Address Register	Yes	Yes	
Program Operations	Page Program	Yes	Yes	
	Page Program with 4-Byte Address	No	Yes	
	Quad Page Program	Yes	Yes	
	Quad Page Program with 4-Byte Address	No	Yes	
Erase Operations	4KB Sector Erase	Yes	Yes	
	4KB Sector Erase with 4-Byte Address	No	Yes	
	32KB Block Erase	Yes	Yes	
	64KB Block Erase	Yes	Yes	
	64KB Block Erase with 4-Byte Address	No	Yes	
	Chip Erase	Yes	Yes	
	Program/Erase Suspend	Yes	Yes	
	Program/Erase Resume	Yes	Yes	
Power Operations	Power down	Yes	Yes	
	Release Power Down/ ID	Yes	Yes	
Read Operations	Read Data	Yes	Yes	
	Fast Read	Yes	Yes	
	Fast Read Dual Output	Yes	Yes	
	Fast Read Quad Output	Yes	Yes	
	Fast Read Dual I/O	Yes	Yes	
	Fast Read Dual I/O with Continuous Read Mode	Yes	Yes	
	Fast Read Quad I/O	Yes	Yes	
	Fast Read Quad I/O with Continuous Read Mode	Yes	Yes	
	Word Read Quad I/O	Yes	No	
	Word Read Quad I/O with Continuous Read Mode	Yes	No	
	Octal Word Read Quad I/O	Yes	No	
	Octal Word Read Quad I/O with Continuous Read Mode	Yes	No	
	Burst Read with Wrap	Yes	Yes	
	Set Burst with Wrap	Yes	Yes	
	Set Read Parameters	Yes	Yes	
	Read Data with 4-Byte Address	Yes	Yes	

	Fast Read with 4-Byte Address	Yes	Yes	
	Fast Read Dual Output with 4-Byte Address	Yes	Yes	
	Fast Read Quad Output with 4-Byte Address	Yes	Yes	
	Fast Read Dual I/O with 4-Byte Address	Yes	Yes	
	Fast Read Dual I/O with 4-Byte Address with Continuous Read Mode	Yes	Yes	
	Fast Read Quad I/O with 4-Byte Address	Yes	Yes	
	Fast Read Quad I/O with 4-Byte Address with Continuous Read Mode	Yes	Yes	
	DTR Fast Read	No	Yes	
	DTR Fast Read Dual I/O	No	Yes	
	DTR Fast Read Quad I/O	No	Yes	
	DTR Fast Read Quad I/O with Continuous Read Mode	No	Yes	
	DTR Burst Read with Wrap	No	Yes	
Identification Operations	Read Unique ID	Yes	Yes	
	Read JEDEC ID	Yes	Yes	
	Read SFDP Register	Yes	Yes	
	Read Manufacturer/Device ID	Yes	Yes	
	Read Manufacturer/Device ID Dual I/O	Yes	Yes	
	Read Manufacturer/Device ID Quad I/O	Yes	Yes	
Security Register Operations	Erase Security Registers	Yes	Yes	
	Program Security Registers	Yes	Yes	
	Read Security Registers	Yes	Yes	
Protection	Global Block Lock	Yes	Yes	
	Global Block Unlock	Yes	Yes	
	Individual Block Lock	Yes	Yes	
	Individual Block Unlock	Yes	Yes	
	Read Block Lock	Yes	Yes	
Mode Switch Operation	Enter 4-Byte Address Mode	Yes	Yes	
	Exit 4-Byte Address Mode	Yes	Yes	
	Enter QPI Mode	Yes	Yes	
	Exit QPI Mode	Yes	Yes	
Soft Reset	Enable Reset	Yes	Yes	
	Reset Device	Yes	Yes	

The Micron Quad SPI memory model supports all the commands for 3-Byte address mode and 4-Byte address mode, Extended SPI/Dual SPI/Quad SPI and DTR mode.

Table 3: Feature List for Micron Models

Features		Support	Notes
		mt25q* and mt25t*	
Software Reset Operations	Reset Enable (66h)	Yes	
	Reset Memory (99h)	Yes	
Read ID Operations	Read ID (9E/9Fh)	Yes	
	Multiple IO Read ID (AFh)	Yes	
	Read Serial Flash Discovery Parameter (5Ah)	Yes	
Read Memory Operations	Read (03h)	Yes	
	Fast Read (0Bh)	Yes	

	Dual Output Fast Read (3Bh)	Yes	
	Dual Input/Output Fast Read (BBh)	Yes	
	Quad Output Fast Read (6Bh)	Yes	
	Quad Input/Output Fast Read (EBh)	Yes	
	DTR Fast Read (0Dh)	Yes	
	DTR Dual Output Fast Read (3Dh)	Yes	
	DTR Dual Input/Output Fast Read (BDh)	Yes	
	DTR Quad Output Fast Read (6Dh)	Yes	
	DTR Quad Input/Output Fast Read (EDh)	Yes	
	Quad Input/Output Word Read (E7h)	Yes	
	4-Byte Read (13h)	Yes	
	4-Byte Fast Read (0Ch)	Yes	
	4-Byte Dual Output Fast Read (3Ch)	Yes	
	4-Byte Dual Input/Output Fast Read (BCh)	Yes	
	4-Byte Quad Output Fast Read (6Ch)	Yes	
	4-Byte Quad Input/Output Fast Read (ECh)	Yes	
	4-Byte DTR Fast Read (0Eh)	Yes	
	4-Byte DTR Dual Input/Output Fast Read (BEh)	Yes	
	4-Byte DTR Quad Input/Output Fast Read (EEh)	Yes	
Write Operations	Write Enable (06h)	Yes	
	Write Disable (04h)	Yes	
Read Register Operations	Read Status Register (05h)	Yes	
	Read Flag Status Register (70h)	Yes	
	Read Nonvolatile Configuration Register (B5h)	Yes	
	Read Volatile Configuration Register (85h)	Yes	
	Read Enhanced Volatile Configuration Register (65h)	Yes	
	Read Extended Address Register (C8h)	Yes	
	Read General Purpose Read Register (96h)	Yes	
Write Register Operations	Write Status Register (01h)	Yes	
	Write Nonvolatile Configuration Register (B1h)	Yes	
	Write Volatile Configuration Register (81h)	Yes	
	Write Enhanced Volatile Configuration Register (61h)	Yes	
	Write Extended Address Register (C5h)	Yes	
	Clear Flag Status Register (50h)	Yes	
Program Operations	Page Program (02h)	Yes	
	Dual Input Fast Program (A2h)	Yes	
	Extended Dual Input Fast Program (D2h)	Yes	
	Quad Input Fast Program (32h)	Yes	
	Extended Quad Input Fast Program (38h)	Yes	
	4-Byte Page Program (12h)	Yes	
	4-Byte Quad Input Fast Program (34h)	Yes	
	4-Byte Quad Input Extended Fast Program (3Eh)	Yes	
Erase Operations	32KB Subsector Erase (52h)	Yes	
	4KB Subsector Erase (20h)	Yes	
	Sector Erase (D8h)	Yes	
	Bulk Erase (C7/60h)	Yes	
	4-Byte Sector Erase (DCh)	Yes	
	4-Byte 4KB Subsector Erase (21h)	Yes	
	4-Byte 32KB Subsector Erase (5Ch)	Yes	
	Program/Erase Suspend (75h)	Yes	

Suspend/Resume Operations	Program/Erase Resume (7Ah)	Yes	
OTP Operations	Read OTP Array (4Bh)	Yes	
	Program OTP Array (42h)	Yes	
4-Byte Address Mode Operations	Enter 4-Byte Address Mode (B7h)	Yes	
	Exit 4-Byte Address Mode (E9h)	Yes	
Quad Protocol Operations	Enter Quad Input/Output Mode (35h)	Yes	
	Reset Quad Input/Output Mode (F5h)	Yes	
Deep Power-Down Operations	Enter Deep Power Down (B9h)	Yes	
	Release From Deep Power Down (ABh)	Yes	
Advanced Sector Protection Operations	Read Sector Protection (2Dh)	Yes	
	Program Sector Protection (2Ch)	Yes	
	Read Volatile Lock Bits (E8h)	Yes	
	Write Volatile Lock Bits (E5h)	Yes	
	Read Nonvolatile Lock Bits (E2h)	Yes	
	Write Nonvolatile Lock Bits (E3h)	Yes	
	Erase Nonvolatile Lock Bits (E4h)	Yes	
	Read Global Freeze Bit (A7h)	Yes	
	Write Global Freeze Bit (A6h)	Yes	
	Read Password (27h)	Yes	
	Write Password (28h)	Yes	
	Unlock Password (29h)	Yes	
	4-Byte Read Volatile Lock Bits (E0h)	Yes	
	4-Byte Write Volatile Lock Bits (E1h)	Yes	
Advanced Function Interface Operations	Interface Activation (9Bh)	No	
	Cyclic Redundancy Check (27h)	No	

Note:
1. Hold function is not supported for Micron parts.
2. All the 4-Byte address command and read/write extended address register commands are not supported for mt25qu128aba, mt25ql128aba, mt25tu256 and mt25tl256 parts.

4. Model Block Diagram

The following figure shows the QSPI model block diagram. The VCC power pin is not supported.

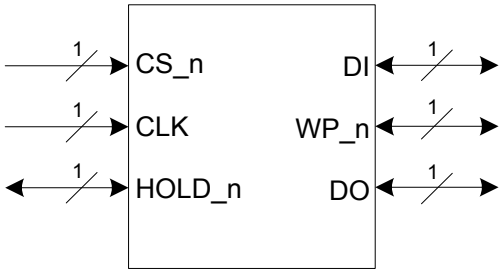

Figure 1: Winbond QSPI Model Block Diagram

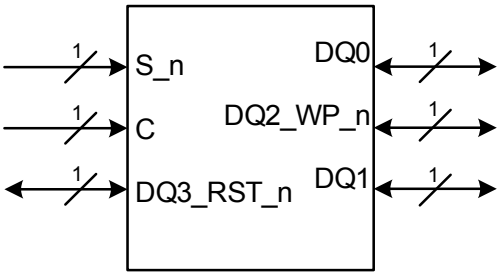

Figure 2: Micron QSPI Model Block Diagram

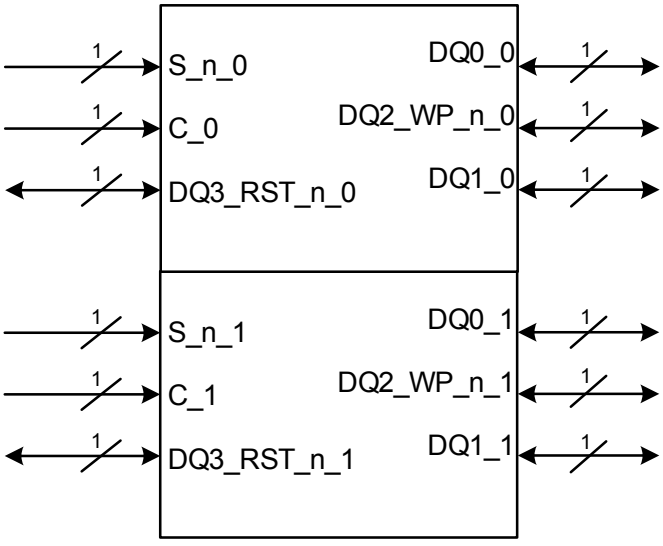

Figure 3: Micron 2-die QSPI Model Block Diagram

5. I/O Signal Description

The table below lists and describes the model I/O signals.

Table 4: Winbond QSPI Model I/O Signals

NAME	TYPE	DESCRIPTION
CS_n	Input	**Chip Select**: The SPI Chip Select pin enables and disables device operation. When CS_n is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. After power-up, CS_n must transition from high to low before a new instruction will be accepted.
CLK	Input	**Serial Clock:** The SPI Serial Clock Input pin provides the timing for serial input and output operations. Latches commands, address, and data on DI on the rising edge of CLK. Triggers output on DO (IO0-3) after the falling edge of CLK.
HOLD_n	I/O	**Hold:** The HOLD_n pin allows the device to be paused while it is actively selected. When HOLD_n is brought low, while CS_n is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored. When HOLD_n is brough high, device operation can resume. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD_n pin function is not available since the pin is used for IO3.
DI	I/O	**Serial Data Input:** Standard SPI instructions use the DI pin to serially write instructions, addresses or data to the device on the rising edge of the CLK input pin. It is also used as IO0 for Dual and Quad SPI and QPI instructions.
WP_n	I/O	**Write Protect:** The Write Protect pin can be used to prevent the Status Register from being written. When the QE bit of Status Register-2 is set for Quad I/O, the WP_n pin function is not available since this pin is used for IO2.
DO	I/O	**Serial data output:** Standard SPI uses the DO pin to read data or status from the device on the falling edge of CLK. It is also used as IO1 for Dual and Quad SPI and QPI instructions.

Table 5: Micron QSPI Model I/O Signals

NAME	TYPE	DESCRIPTION
S_n	Input	**Chip Select**: When S_n is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated.
C	Input	**Serial Clock:** Provides the timing of the serial interface. Command inputs are latched on the rising edge of the clock. In

NAME	TYPE	DESCRIPTION
		STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DQ3_RST_n	I/O	**DQ3/Reset:** For pin configurations that share the DQ3 pin with RESET_n, the RESET_n functionality is disabled in QIO-SPI mode.
DQ0	I/O	**Serial IO0:** The bidirectional DQ signals transfer address, data, and command information.
DQ2_WP_n	I/O	**DQ2/Write Protect:** Freezes the status register in conjunction with the enable/disable bit of the status register. During the extended-SPI protocol with QOFR and QIOFR instructions, and with QIO-SPI protocol, this pin function is an input/output as DQ2 functionality.
DQ1	I/O	**Serial IO1:** The bidirectional DQ signals transfer address, data, and command information.

6. Model Parameter Descriptions

The following table provides details on the user adjustable parameters for the Palladium QSPI Memory Model. These parameters may be modified when instantiating a QSPI wrapper or, if necessary, by modifying the HDL parameter declarations and default values which are exposed for access and debug visibility.

Table 6: User Adjustable Parameters

User Adjustable Parameter	Default Value	Description
col_width	8	The column address width
row_width	17	The row address width
trst_fclk_cycs	500	The number of fast clock cycles for 30us timer. After issuing enable reset then reset device command, tRST (30us) must elapse before issuing any other command. The parameter can be changed to a smaller number to shorten the time.

The following table provides some information about exposed localparams that are NOT user adjustable. On rare occasion the user may find one of these localparam needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

Table 7: Visible Non-User-Adjustable Localparam

Localparam	Default Value	Description
MANUFACTURER_ID	8'hEF	Manufacturer ID
DEVICE_ID_8	8'h18	Device ID for instruction ABh, 90h, 92h, 94h for Winbond w25q256jw
DEVICE_ID_16	16'h8019	Device ID for instruction 9Fh for Winbond w25q256jw
DEVICE_ID_SPI_8	8'h18	Device ID for instruction ABh, 90h, 92h, 94h in SPI Mode for Winbond w25q256fv
DEVICE_ID_QPI_8	8'h18	Device ID for instruction ABh, 90h, 92h, 94h in QPI Mode for Winbond w25q256fv
DEVICE_ID_SPI_16	16'h4019	Device ID for instruction 9Fh in SPI Mode for Winbond w25q256fv
DEVICE_ID_QPI_16	16'h6019	Device ID for instruction 9Fh in QPI Mode for Winbond w25q256fv

Note that there are additional exposed localparams in the model HDL that are not described here nor intended to be described here. These additional localparams are exposed for debugging purposes only and will not be described herein.

7. Address mapping

The array of the QSPI model is mapped into the internal memory of the Palladium system. This array is a two-dimensional array of signals. The array width is 8bit and the address of the memory array is byte address. The mapping of row and column addresses to the internal model array is as follows:

ARRAY_ADDR = {RA, CA}

The array name in the model is: memcore

8. Initialization Sequence

The QSPI Memory Model does not have any requirement for initialization sequence.

9. Status Registers

The QSPI Memory Model supports three status registers for Winbond models.

Table 8: Status Registers for Winbond

NAME	FIELDS	Default Value
Status Register-1	Bit7: SRP0 Bit6: TB Bit5-2: BP3-BP0 Bit1: WEL Bit0: BUSY	8'h00
Status Register-2	Bit7: SUS Bit6: CMP Bit5-3: LB3-LB1 Bit2: Reserved Bit1: QE Bit0: SRP1	8'h00
Status Register-3	Bit7: HOLD /RST Bit6-5: DRV1-DRV0 Bit4-3: Reserved Bit2: WPS Bit1: ADP Bit0: ADS	8'h60

The QSPI Memory Model supports below registers for Micron models.

Table 9: Registers for Micron

NAME	FIELDS	Default Value
Status Register	Bit7: Status register write enable/disable Bit5: TB Bit6,4-2: BP[3:0] Bit1: WEL	8'h00

	Bit0: Write in progress	
Flag Status Register	Bit7: Program or erase controller Bit6: Erase suspend Bit5: Erase Bit4: Program Bit3: Reserved Bit2: Program suspend Bit1: Protection Bit0: Addressing	8'h80
Nonvolatile Configuration Register	Bit15-12: Number of dummy clock cycles Bit11-9: XIP mode at power-on reset Bit8-6: Output driver strength Bit5: Double transfer rate protocol Bit4: Reset/hold Bit3: Quad I/O protocol Bit2: Dual I/O protocol Bit1: 128Mb segment select Bit0: Number of address bytes during command entry	16'hFFFF
Volatile Configuration Register	Bit7-4: Number of dummy clock cycles Bit3: XIP Bit2: Reserved Bit1-0: Wrap	8'hFB
Enhanced Volatile Configuration Register	Bit7: Quad I/O protocol Bit6: Dual I/O protocol Bit5: Double transfer rate protocol Bit4: Reset/hold Bit3: Reserved Bit2-0: Output driver strength	8'hFF
Sector Protection Register	Bit15-3: Reserved Bit2: Password protection lock Bit1: Sector protection lock Bit0: Reserved	16'hFFFF
Global Freeze Bit	Bit7-1: Reserved Bit0: Global freeze bit	8'h01

Note: The bit0 of Flag Status Register and bit0-1 of Nonvolatile Configuration Register are reserved for mt25qu128aba, mt25ql128aba, mt25tu256 and mt25tl256 parts.

10. Limitations

1. After download into the Palladium the initial value of the flash memory array is all 0's. Like real Flash parts the model only allows programming of 1's to 0's. The memory region of the Flash array being programmed must first either be erased with an erase command or initialized to all 1's through the user issuing a memory set command in Palladium runtime tools.
2. The CRC operation is not supported for Micron parts.

11. Compile and Emulation

The model is provided as protected RTL files (*.vp). The files need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64bit +sv -ua +dut+w25q256fv \
        ./w25q256fv.vp \
        -incdir ../../../utils/cdn_mmp_utils/sv \
        ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
        ……

xeDebug -64 --ncsim \
  -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
        -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis. The first uses script commands and the second uses command line commands:

```
1)
hdlInputFile w25q256fv.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog w25q256fv.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -
keepAllFlipFlop  w25q256fv
……

2)
vavlog w25q256fv.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog w25q256fv.vg
w25q256fv
……
```

For Micron 2-die parts below, the 2-die wrapper and 1-die core are needed when compile.

mt25tu256: mt25tu256.vp and mt25qu128aba.vp
mt25tl256: mt25tl256.vp and mt25ql128aba.vp
mt25tu512: mt25tu512.vp and mt25qu256aba.vp
mt25tl512: mt25tl512.vp and mt25ql256aba.vp
mt25tu01g: mt25tu01g.vp and mt25qu512abb.vp
mt25tu01g: mt25tl01g.vp and mt25qu512abb.vp

NOTE: It is common for Palaldium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-

ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

The user needs to set the main array 'memcore' and the buffer register 'membuf' to all '1'.

Below is a scripting example snippet showing the memory set for QSPI model. The user can change the QSPI Model instance name "qspi_inst" as needed.

```
……
xc xt0 zt0 run
xc memory -set qspi_inst.memcore
xc memory -set qspi_inst.membuf
……
```

For micron models, the below dat files are need for device id and SFDP register initialization:

```
xc memory -load %readmemh tb.flash_qspi_pd_inst.device_id_data -
file ./<PART_NUMBER>_dev_id.dat
xc memory -load %readmemh tb.flash_qspi_pd_inst.sfdp_reg -
file ./<PART_NUMBER>_sfdp.dat
```

For Micron 2-die parts below, the memory set and preload are needed for both die0 and die1. For example, for mt25tu256 part:

```
……
xc xt0 zt0 run
#Die0
xc memory -set tb.flash_qspi_pd_inst.die0.qspi_inst.memcore
xc memory -set tb.flash_qspi_pd_inst.die0.qspi_inst.membuf
xc memory -load %readmemh tb.flash_qspi_pd_inst.die0.device_id_data -
file ./mt25qu128aba _dev_id.dat
xc memory -load %readmemh tb.flash_qspi_pd_inst.die0.sfdp_reg -file ./
mt25qu128aba_sfdp.dat
#Die1
xc memory -set tb.flash_qspi_pd_inst.die1.qspi_inst.memcore
xc memory -set tb.flash_qspi_pd_inst.die1.qspi_inst.membuf
xc memory -load %readmemh tb.flash_qspi_pd_inst.die1.device_id_data -
file ./mt25qu128aba _dev_id.dat
```

```
xc memory -load %readmemh tb.flash_qspi_pd_inst.die1.sfdp_reg -file ./
mt25qu128aba_sfdp.dat
……
```

12. Debugging

The QSPI model has several debugging options techniques and tips that may assist the user in isolating a problem.

- For issues that may not be QSPI specific please review the *Memory Model Portfolio FAQ for All Models User Guide.*

- **Golden waveform:** A package with a reference waveform is available which shows the following command sequence:

  Winbond models:
  (1) Command - Enable Reset
  Command - Reset Device
  (2) Command - Write Enable
  Command - Write Status Register-1
  Command - Read Status Register-1
  Command - Write Enable
  Command - Write Status Register-2
  Command - Read Status Register-2
  Command - Write Enable
  Command - Write Status Register-3
  Command - Read Status Register-3
  (3) Command - Read Manufacturer Device ID
  Command - Read Manufacturer Device ID Dual IO
  Command - Read JEDEC ID
  Command - Read Unique ID
  Command - Read SFDP Register
  Command - Write Enable
  Command - Program Security Registers
  Command - Read Security Registers
  Command - Write Enable
  Command - Erase Security Registers
  (4) Command - Write Enable
  Command - Page Program
  Command - Read Data
  Command - Write Enable
  Command - Quad Page Program
  Command - Read Data
  Command - Fast Read
  Command - Fast Read Dual Output
  Command - Fast Read Dual IO
  Command - Read Data with 4 Byte Address
  Command - Fast Read Data with 4 Byte Address

Command - Fast Read Dual Output with 4 Byte Address
Command - Fast Read Dual IO with 4 Byte Address
Command - DTR Fast Read (w25q256jw only)
Command – DTR Fast Read Dual IO (w25q256jw only)
Command - Fast Read Quad Output
Command - Fast Read Quad Output with 4 Byte Address
Command - Fast Read Quad IO
Command - Word Read Quad IO
Command - Octal Word Read Quad Io
Command - Fast Read Quad IO with 4 Byte Address
Command - DTR Fast Read Quad IO (w25q256jw only)
Command - DTR Fast Read Quad IO with Continuous Read Mode (w25q256jw only)
Command - Set Burst with Wrap
Command - Fast Read Quad IO
Command - Fast Read Quad IO with 4 Byte Address
Command - Word Read Quad IO
(5) Command - Enter QPI Mode
Command - Write Enable
Command - Sector Erase
Command - Read Manufacturer Device ID
Command - Read JEDEC ID
Command - Write Enable
Command - Page Program
Command - Fast Read
Command - Fast Read Quad IO
Command - DTR Fast Read (w25q256jw only)
Command - DTR Fast Read Quad IO (w25q256jw only)
Command - DTR Fast Read Quad IO with Continuous Read Mode (w25q256jw only)
Command - Set Read Parameters
Command - Burst Read with Wrap
Command - DTR Burst Read with Wrap (w25q256jw only)
Command - Exit QPI Mode

Micron models:
(1) Hardware Reset operation
Software Reset opration
(2) Extended SPI Mode:
Read ID operation
Read SFDP operation
Program operation
Read operation
Fast Read operation
(3) Extended SPI Mode - DTR Mode:
Read ID operation
Read SFDP operation
Program operation
Read operation
Fast Read operation
(4) Dual SPI Mode:
Read ID operation
Read SFDP operation

Program operation
Read operation
Fast Read operation
(5) Dual SPI Mode - DTR Mode:
Read ID operation
Read SFDP operation
Program operation
Read operation
Fast Read operation
(6) Quad SPI Mode:
Read ID operation
Read SFDP operation
Program operation
Read operation
Fast Read operation
(7) Quad SPI Mode - DTR Mode:
Read ID operation
Read SFDP operation
Program operation
Read operation
Fast Read operation
(8) XIP operation

- **Debug Display:** The Palladium QSPI memory model has available a built-in debug methodology called MMP Debug Display that is based on the Verilog system task $display. Please see the *Palladium Memory Model Debug Display User Guide* in the release docs directory for additional information.

- **Manual Configuring of this MMP Model Family**

  This MMP model supports manual configuration by accompanying the model mode register or configuration register declarations with synthesis directives, such as keep_net directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing. For a general description of this support please see the user guide in the MMP release with path and filename docs/MMP_FAQ_for_All_Models.pdf.

  While MMP strongly recommends following protocol-based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments.

  The following table lists the internal register path and naming along with the specification or datasheet naming for model mode registers or configuration registers that are accompanied by keep_net synthesis directives in support of such manual configuration. ONLY writeable configuration registers or fields are supported thusly. Please read the relevant datasheet for details about individual register behavior and mapping to fields.

Table 10: Writeable Mode Register / Configuration Register Info

Hierarchical RTL Naming for Writeable Configuration Related Registers & Signals	Specification or Vendor Datasheet Naming for Configuration Related Registers	Access
For Winbond models		
<model_name>.ext_addr_reg	Extended Address Register	R/W
<model_name>.ADP	{ADP} Status Register	R/W
<model_name>.HOLD_RST	{HOLD/RST} Status Register	R/W
<model_name>.QE	{QE} Status Register	R/W
<model_name>.TB	{TB} Status Register	R/W
<model_name>.CMP	{CMP} Status Register	R/W
<model_name>.WPS	{WPS} Status Register	R/W
<model_name>.SRP	{SRP1, SRP0} Status Register	R/W
<model_name>.DRV	{DRV1, DRV0} Status Register	R/W
<model_name>.LB	{LB2, LB1} Status Register	R/W
<model_name>.BP	{BP3-BP0} Status Register	R/W
For Micron models		
<model_name>.status_reg	Status Register	R/W
<model_name>.flag_status_reg	Flag Status Register	R/W
<model_name>.nv_cfg_reg	Nonvolatile Configuration Register	R/W
<model_name>.v_cfg_reg	Volatile Configuration Register	R/W
<model_name>.enh_v_cfg_reg	Enhanced Volatile Configuration Register	R/W
<model_name>.sec_protection_reg	Security Register	R/W
<model_name>.ext_addr_reg	Extended Address Register	R/W

Revision History

The following table shows the revision history for this document

Date	Version	Revision
August 2015	1.0	Initial release
September 2015	1.1	Added note about synthesis options.
January 2016	1.2	Update for Palladium-Z1 and VXE
February 2016	1.3	Adjusted font larger for memory set example
April 2016	1.4	Removed BETA watermark; model non-BETA
May 2016	1.5	Added new model w25q256jw
July 2016	1.6	Remove hyphen in Palladium naming
March 2017	1.7	Removed w25q256jw BETA note. Memory part is now MR level (non BETA) Change model name to lower case
September 2017	1.8	Update for reference specification
January 2018	1.9	Add Micron parts. Modify header and footer.
April 2018	2.0	Add table for localparameter device id
June 2018	2.1	Add section for Manual configuration
July 2018	2.2	Update for new utility library