Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

I2C EEPROM
Palladium Memory Model
User Guide

Document Version: **2.1**

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Contents

General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

I2C EEPROM Memory Model

1. Introduction

The Cadence Palladium EEPROM Model is based on the I^2C specification and the Serial I2C EEPROM device specification from Atmel.

Different sizes from 1Kb up to 1024Kb are available in the release. Please consult the memory model catalog for the currently available list.

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	No	Yes

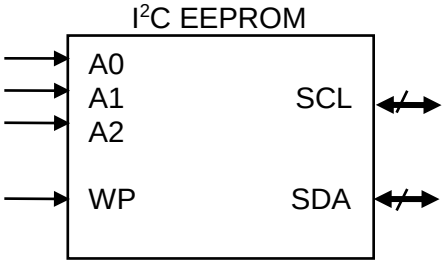
Access to Initial and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Configurations and Address

The following table lists the possible configurations. Not all configurations may be available.

Device Density	Data Bus Width (Bits)	Address		
		P2, P1, P0	1st Word (bits)	2nd Word (bits)
1Kb	8		7	
2Kb	8		8	
4Kb	8	P0	8	
8Kb	8	P1, P0	8	
16Kb	8	P2, P1, P0	8	
32Kb	8		4	8
64Kb	8		5	8
128Kb	8		6	8
256Kb	8		7	8
512Kb	8		8	8
1024Kb	8	P0	8	8

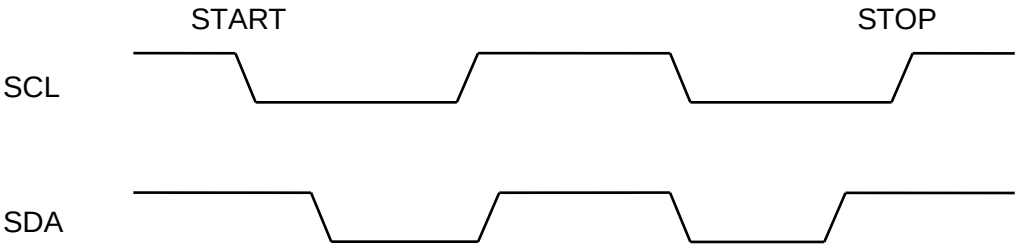
4. Model Block Diagram



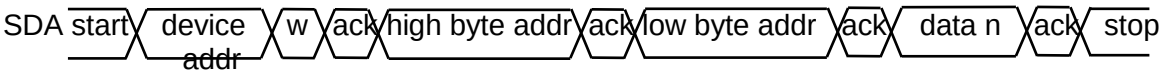
NAME	DESCRIPTION
A0	Address Input
A1	Address Input
A2	Address Input
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

5. Waveforms for Read/Write

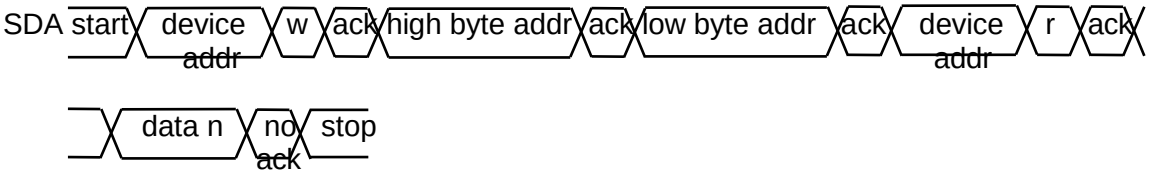
5.1. Basic



5.2. Write



5.3. Read



5.4. Write protect

Connecting the WP pin to GND will ensure normal write operations. When the WP pin is connected to VCC, all write operations to the memory are inhibited.

The status of the WP pin is sampled at the Stop condition for every Byte Write or Page Write command prior to the start of an internally self-timed Write operation. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle.

Microchip 24AA16H supports partial WP, the WP pin allows the user to write-protect half of the array (400h-7FFh) when the pin is tied to VCC. If the pin is tied to VSS the write protection is disabled.

6. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) of this model in the IXCOM flow is shown below.

```
ixcom -ua +dut+at24c01 \
    ./ at24c01.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile at24c01.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog at24c01.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
at24c01
……

2)
vavlog at24c01.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog at24c01.vg at24c01
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

7. Commands

The Wide I/O model accepts the following commands:

- Byte Wirte
- Page Write
- Acknowledge Polling
- Current Address Read
- Random Read
- Sequential Read

8. Revision History

The following table shows the revision history for this document

Date	Version	Revision
August 2011	1.0	Initial version
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.3	Remove emulation capacity info. Update related publications list.
July 2015	1.4	Update Cadence naming on front page
September 2015	1.5	Add compile and emulation section
October 2015	1.6	Add write protect function
November 2015	1.7	Update the partial write protect part
January 2016	1.8	Update for Palladium-Z1 and VXE
July 2016	1.9	Remove hyphen in Palladium naming
January 2018	2.0	Modify header and footer
July 2018	2.1	Update for new utility library