



# Technical Note

## LPDDR5 Clocking

### Background

The LPDDR5 clocking scheme differs from LPDDR4 in how they control command/address (CA) and data circuits: LPDDR4 uses CK<sub>t</sub>/CK<sub>c</sub> signals to control both CA and data circuits, but LPDDR5 uses CK<sub>t</sub>/CK<sub>c</sub> signals for the CA circuit and WCK<sub>t</sub>/WCK<sub>c</sub> signals for the data circuit.

LPDDR5 CK speed is slow (800 MHz MAX) and WCK speed is fast (3200 MHz MAX). 800 MHz is enough for CK to support the required CA command band width, but WCK must be faster to support 6400 Mb/s MAX for DDR data input/output.

The WCK to CK ratio is 4:1 for high data rate operation; WCK to CK is 2:1 for low data rate operation. By using WCK:CK = 2:1, enough command band width can be achieved for low data rate operation.

The primary purpose of splitting the CA and data clocks in LPDDR5 is to reduce power consumption. High-speed WCK runs only during read/write traffic, but low-speed CK runs continuously except during power-down mode or deep-sleep mode. Reducing the frequency for a clock that is always running and using a high-speed clock only during read/write traffic can reduce clock circuit power consumption.

**Table 1: LPDDR4/LPDDR5 Clocking Comparison**

	LPDDR4/LPDDR4X	LPDDR5
CA circuit clock	CK <sub>t</sub> /CK <sub>c</sub> (2133 MHz MAX)	CK <sub>t</sub> /CK <sub>c</sub> (800 MHz MAX)
CA	CA[5:0] (SDR input)	CA[6:0] (DDR input)
Data circuit clock	CK <sub>t</sub> /CK <sub>c</sub> (2133 MHz MAX)	WCK <sub>t</sub> /WCK <sub>c</sub> (3200 MHz MAX)
DQ, DMI	DDR I/O (4266 Mb/s MAX)	DDR I/O (6400 Mb/s MAX)



The diagram illustrates the architecture of an LPDDR5 DRAM controller, divided into two main functional blocks: the **Controller** and the **LPDDR5 DRAM**.

**Controller Block:**

- Oscillator:** Provides the initial clock signal to the PLL.
- PLL (Phase-Locked Loop):** Generates a stable clock signal, which is then divided by a **1/2 Divider**.
- Phase Controller:** Manages the timing and phase of the data signals, receiving input from the DRAM Controller and outputting to the DRAM Core.
- DRAM Controller:** Manages data flow and error handling, receiving signals from the DRAM Core and outputting to the DRAM Core.
- 1/2 Divider:** Divides the PLL clock signal to provide a lower frequency to the DRAM Core.
- CMD/ADD:** Receives commands and addresses from the DRAM Core and outputs them to the DRAM Core.
- RDQS\_t / RDQS\_c:** Receives read data signals from the DRAM Core and outputs them to the DRAM Core.
- Error Handling:** Manages errors during data transfer, receiving signals from the DRAM Core and outputting to the DRAM Core.

**LPDDR5 DRAM Block:**

- CMD/ADD 1.6 Gb/s:** Receives commands and addresses from the Controller and outputs them to the DRAM Core.
- CK\_t/CK\_c 800 MHz:** Receives clock signals from the Controller and outputs them to the DRAM Core.
- WCK\_t/WCK\_c 3.2 GHz:** Receives write clock signals from the Controller and outputs them to the DRAM Core.
- DQ 6.4 Gb/s:** Receives data signals from the DRAM Core and outputs them to the DRAM Core.
- RDQS\_t / RDQS\_c:** Receives read data signals from the DRAM Core and outputs them to the DRAM Core.
- 4-Phase Splitter:** Splits the clock signal into four phases (WCK2\_0/90/180/270) for the DRAM Core.
- DRAM Core:** The main memory array that stores and retrieves data.

The diagram shows the flow of data and control signals between these components, including error handling and phase control.

Pin	Speed	Unit
CK_t, CK-c	0.8	GHz
Command/Address	1.6	Gb/s per pin
WCK_t, WCK_c	3.2	GHz
DQ, DMI	6.4	Gb/s per pin
RDQS_t, RDQS_c	3.2	GHz



## TN-62-04: LPDDR5 Clocking LPDDR5 WCK synchronization

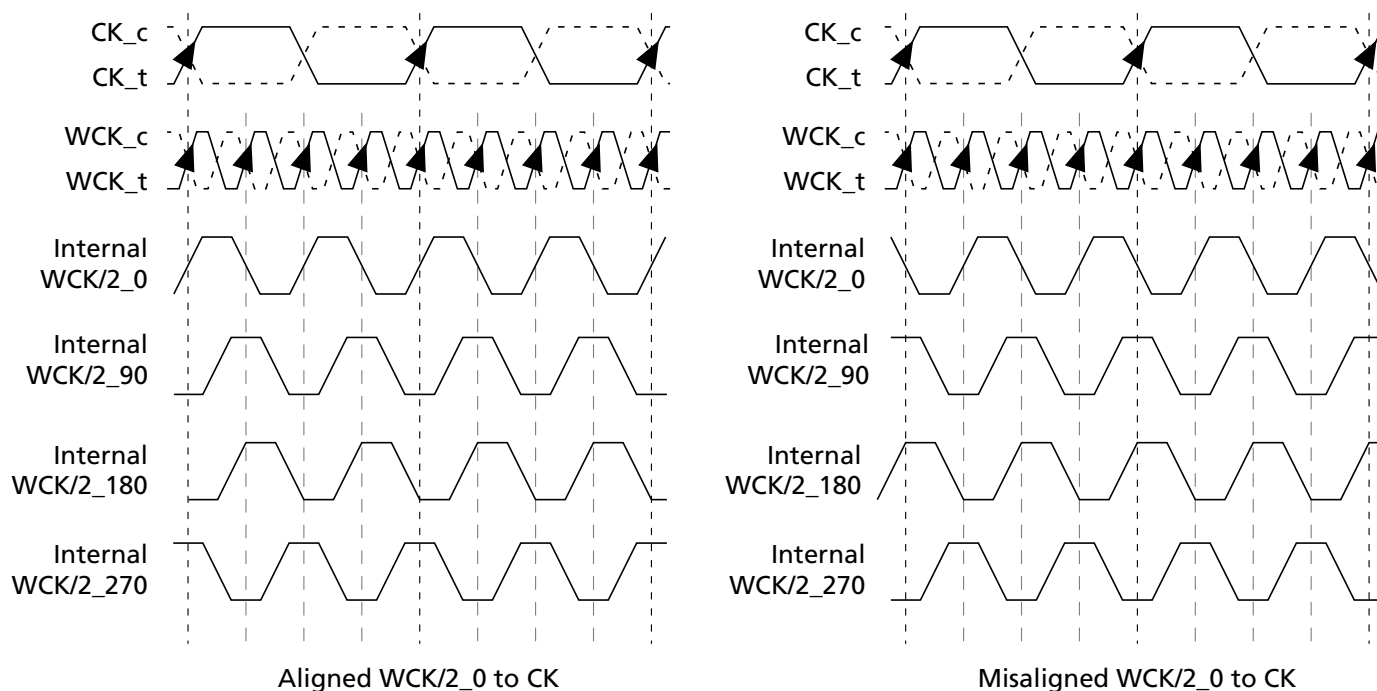
### LPDDR5 WCK synchronization

#### WCK2CK Synchronization

LPDDR5 WCK frequency is four times or twice higher than CK frequency, requiring a device to have a clock divider in the WCK clock tree. By dividing WCK, the operation speed of the device's internal circuits in the WCK domain is reduced to half. However, the WCK divider initial state is unpredictable and results in two different states in device:

1. Aligned with CK state.
2. Misaligned with CK state.

**Figure 2: WCK2CK Alignment (Left Figure is Aligned, Right Figure is Misaligned)**



The latency control unit inside the device performs clock domain change of WRITE or READ commands from CK domain to WCK domain. For error-free latency control, the latency control circuit must know whether the device is in aligned with CK state or misaligned with CK state. A device is able to reset or detect its state by a process called WCK2CK synchronization. When a device controller issues a CAS command with WCK2CK sync selected, it must provide the device with half frequency WCK pulse to relax ISI (inter-symbol interference) and the timing margin. The device will then synchronize WCK to CK. This operation is defined as WCK2CK synchronization.

#### CAS Command With WCK2CK Synchronization Bits

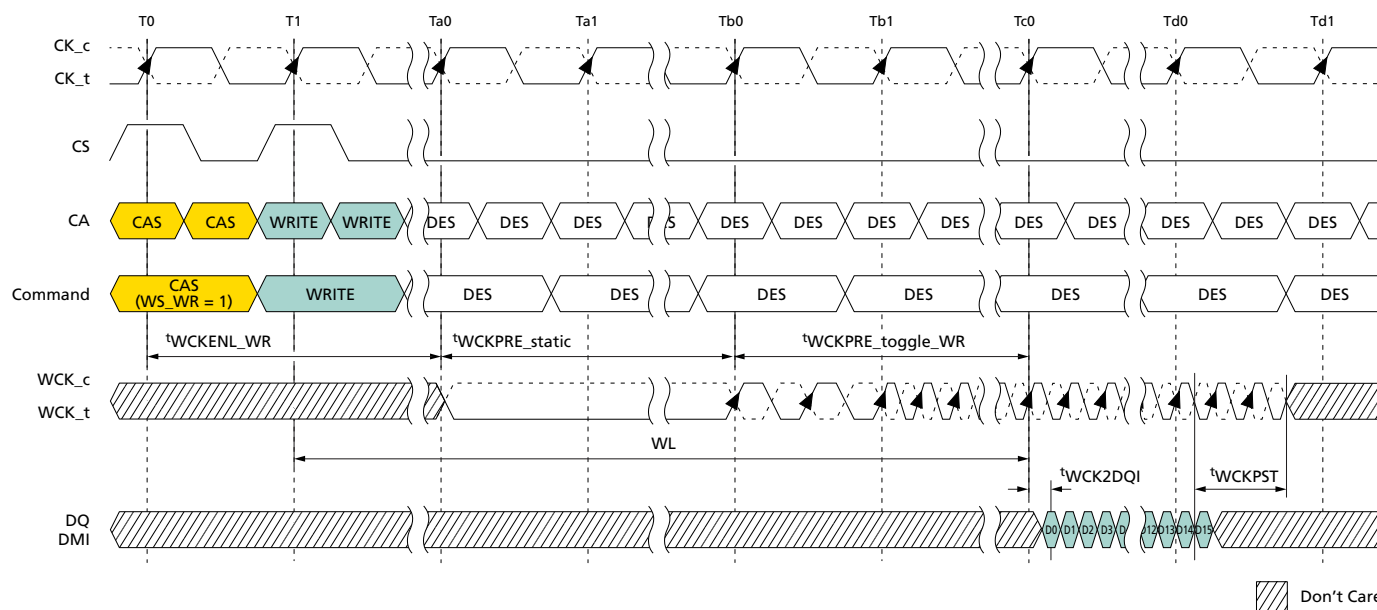
The WCK2CK synchronization process is initiated by a CAS command with the appropriate bit enabled. A CAS command with WCK2CK synchronization should be issued before the WRITE or READ command. The Command Truth Table shows the CAS command with WCK2CK synchronization bits (WS\_WR, WS\_RD, WS\_FS). A CAS command



The reason there are 3 different WCK2CK synchronization bits is that WCK2CK synchronization pattern position is different between those 3 cases.

Command	BK ORG (BG/ 16B/8B)	SDR CMD Pin CS	DDR COMMAND PINS							CK Edge
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS	R1
	Any	X	DC0	DC1	DC2	DC3	WRX	WXS	B3	F1

### Figure 3: WCK2CK Sync Followed by a WRITE Command

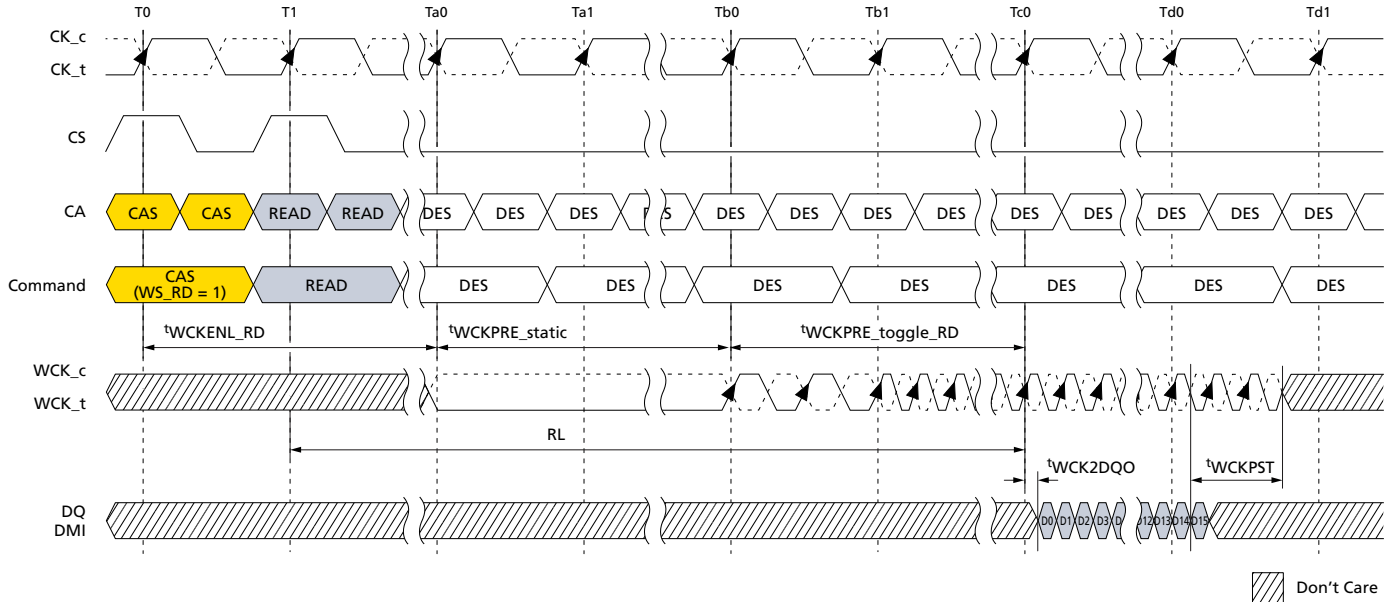




## TN-62-04: LPDDR5 Cloning LPDDR5 WCK synchronization

### WCK2CK SYNC Operation Followed Immediately by a READ Command

Figure 4: WCK2CK Sync Followed by a READ Command



### WCK2CK SYNC Operation With CAS(WS\_FS = 1)

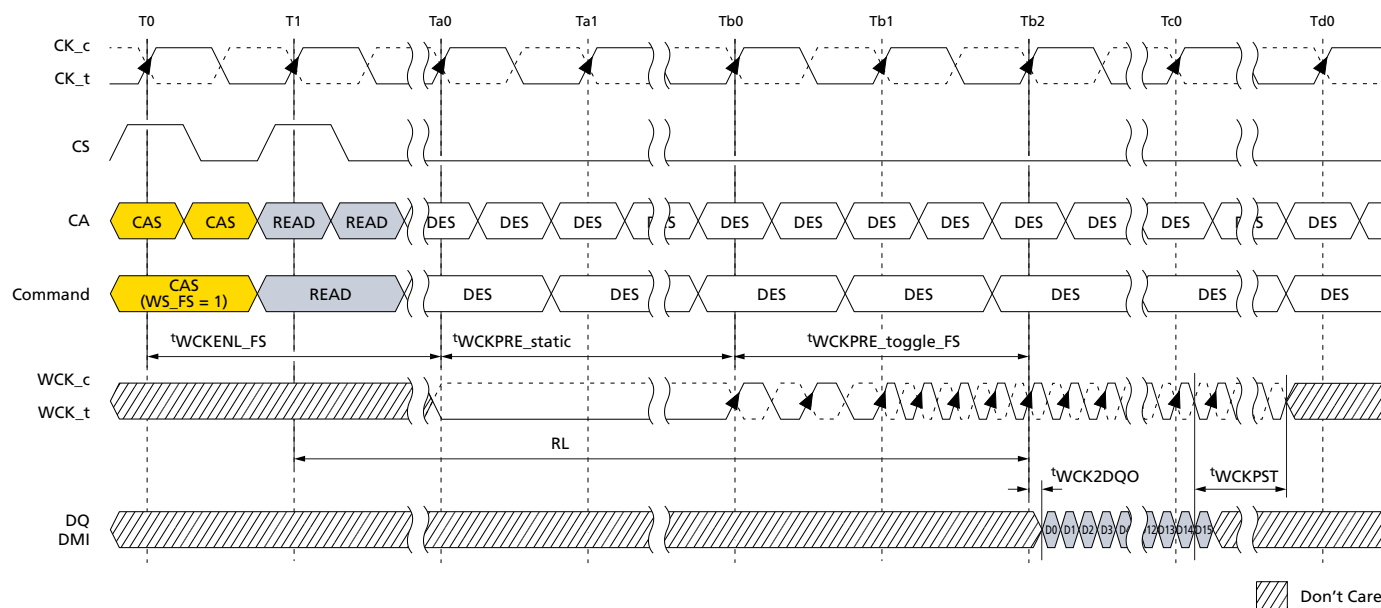
The WCK2CK SYNC operation is performed with minimum latency,  $t_{WCKENL\_FS}$ , when a CAS command with  $WS\_FS = 1$  is issued to a device. Using this command, the device controller can put the device into WCK2CK synchronized state as early as possible. CAS( $WS\_FS = 1$ ) is used as a standalone command unlike CAS( $WS\_RD/WR$ ) and can be issued to synchronize multi-ranks simultaneously.

After the CAS( $WS\_FS = 1$ ) command is issued, READ/WRITE commands as well as other commands such as ACTIVE and REFRESH can also be issued.

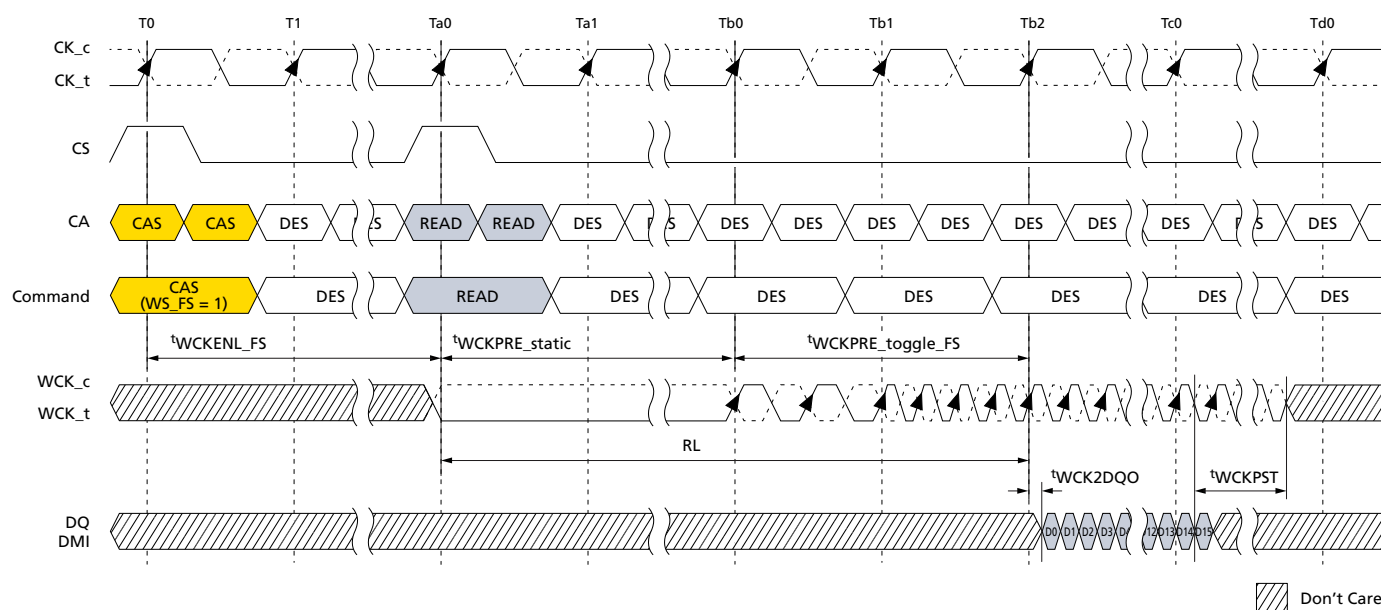


## TN-62-04: LPDDR5 Clacking LPDDR5 WCK synchronization

**Figure 5: Minimum Latency WCK2CK SYNC READ Operation With CAS( $WS\_FS = 1$ )**



**Figure 6: WCK2CK SYNC READ Operation With CAS( $WS\_FS = 1$ ) and Command Gap**



### Rank-to-Rank WCK2CK SYNC Operation

There are two different methods to control WCK2CK sync state of a two rank device.

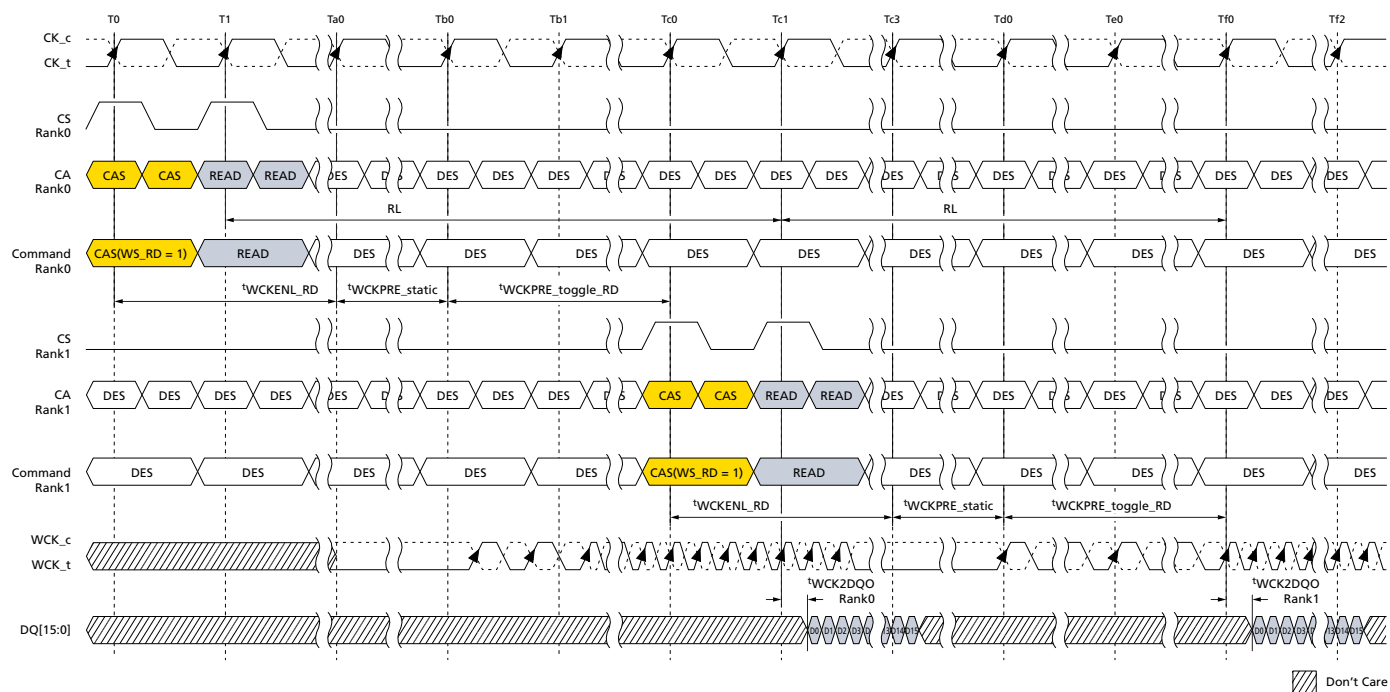
The first method is to start the WCK2CK sync process for rank 1 after completing a DQ data burst on rank 0. In this case,  $t_{WCKPST}$  of rank 0 and  $t_{WCKPRE}$  of rank 1 should be



## TN-62-04: LPDDR5 Clcking LPDDR5 WCK synchronization

guaranteed for the correct RDQS postamble of the READ operation of rank 0 and for the correct WCK2CK synchronization of rank 1 respectively.

**Figure 7: Minimum Gap Rank-to-Rank READ Operation With WCK2CK Sync After DQ Burst Complete in One Rank**

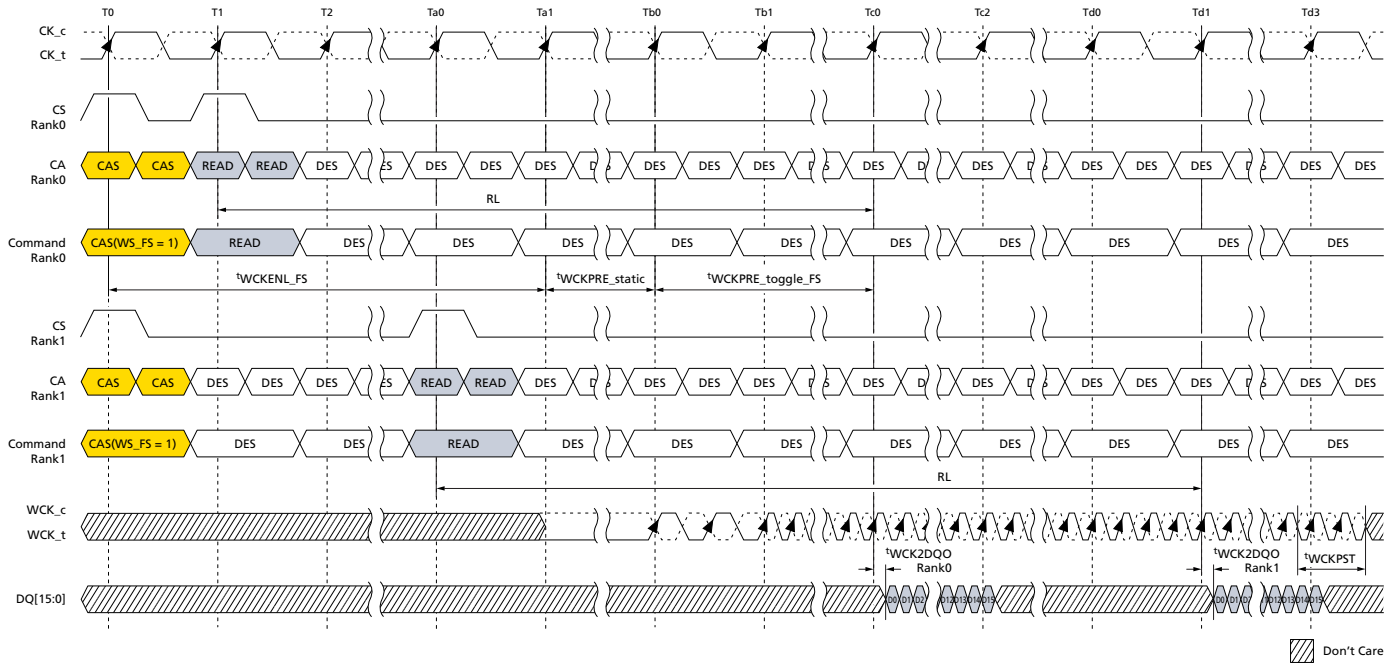


The second method is to start the WCK2CK sync process for both ranks simultaneously. When both ranks are not in a WCK2CK synced state and DQ bursts between two ranks are closed, a simultaneous CAS command with WS\_FS = 1 is recommended for efficient DQ bus utilization. If the subsequent DQ bursts of one rank are far from the preceding the burst of the other rank, extra power consumption due to WCK toggling should be considered. After synchronizing both ranks, if rank 0 is not used, CAS(WCK Sync off) command can be issued to rank 0 to save power.



## TN-62-04: LPDDR5 Clocking LPDDR5 WCK synchronization

**Figure 8: Simultaneous WCK2CK Sync for Multi-ranks (Especially Two Ranks)**





**TN-62-04: LPDDR5 Clocking  
Revision History****Revision History****Rev. A – 5/19**

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000  
www.micron.com/products/support Sales inquiries: 800-932-4992  
Micron and the Micron logo are trademarks of Micron Technology, Inc.  
All other trademarks are the property of their respective owners.  
This data sheet contains initial descriptions of products still under development.