LPDDR4/LPDDR5 PI Simulation Guide

EBU System Tooling Group

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PWL Model/CPM Model/Current Profile

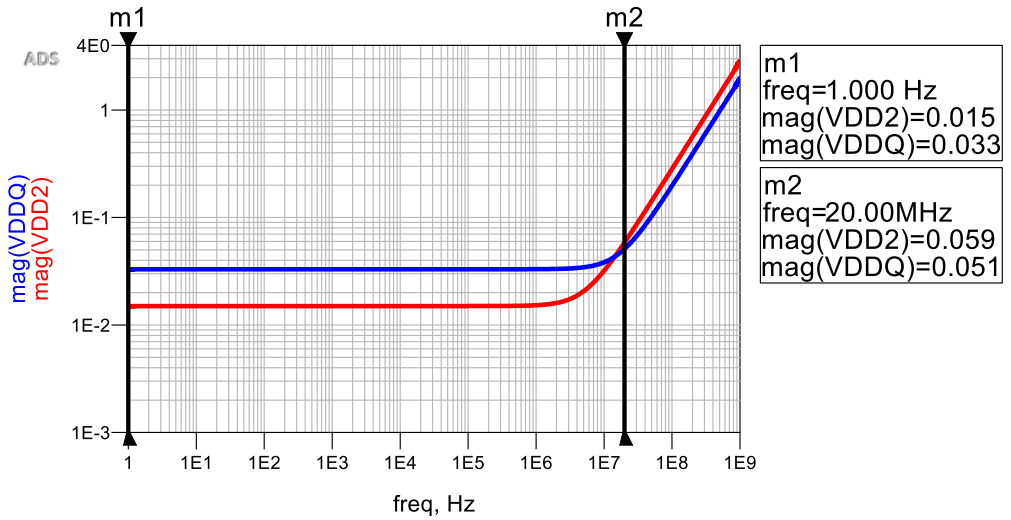
- Micron will not provide PWL model, CPM model and current profile to customers.

PCB Target Impedance

- Micron will provide PCB target impedance, which is based on loop resistance/inductance between VDD2/VDDQ and VSS from PMIC/regulator output to DRAM package BGA balls.
  - It does not include the DRAM package and silicon die.
  - Not considered PMIC too.
  - Recommend that PDN impedance be as low as possible.
  - The target is per DRAM part number and customer usage. Contact Micron for the target Value.

Parameter	VDD2 (1.1V)	VDDQ (0.6V)
DCR	≤15mΩ	≤33mΩ
Inductance	≤450pH	≤310pH

Target Impedance Example



PI Only Simulation Flow

1. The customers can run PI simulation for the PCB only. DRAM package and on-die de-coupling capacitance are not needed.
2. Compare the PCB PDN impedance with the target.
3. Optimize the PCB PI design until the PCB PDN impedance is lower than the target.

SI/PI Co-simulation

- Micron will provide on-die de-coupling model and package PDN model for I/O voltage(VDDQ).
- The customers should include the on-die de-coupling model and package PDN model for SI/PI co-simulation of read DQ signals.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