



Technical Note

LPDDR5 ZQ Calibration

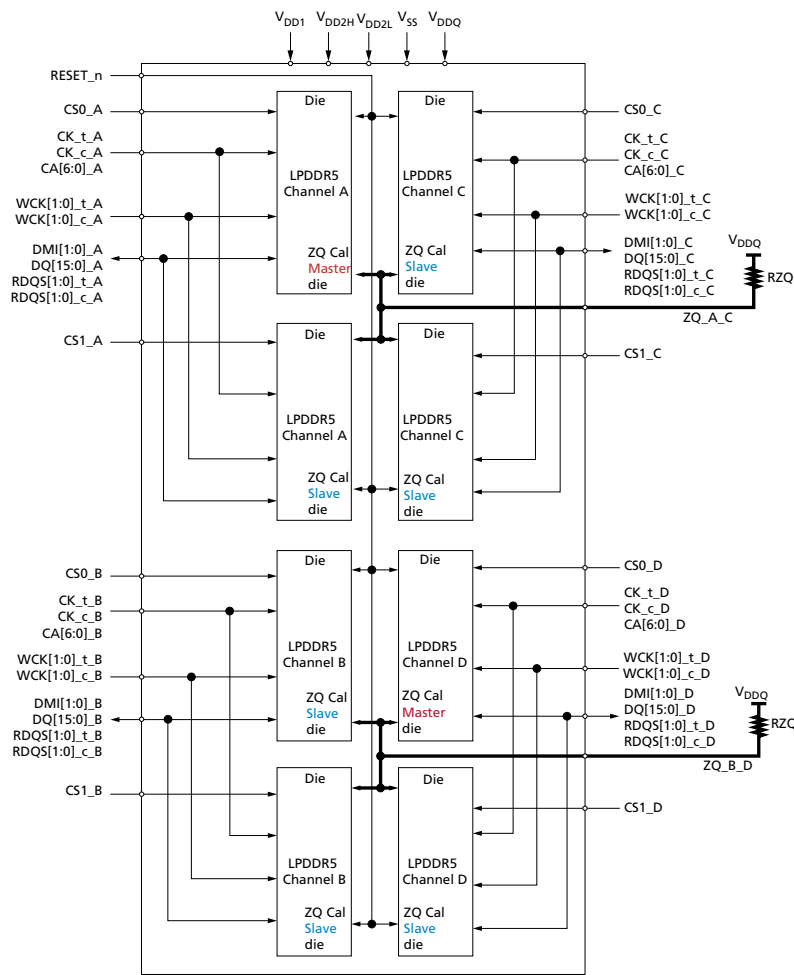
Overview

LPDDR5 supports two ZQ calibration modes: background calibration and command-based calibration. ZQ calibration mode is selected by setting MR28 OP[5].

ZQ calibration can only be performed when the V_{DDQ} voltage is set to nominal 0.5V DC or above.

The command related to ZQ calibration is issued to the master die. The slave die ignores the ZQCAL START command and most of the MR settings. (It accepts ZQCAL STOP, ZQCAL RESET, and ZQCAL LATCH commands). The designation of the ZQ master is hard-coded by the device vendor. The ZQ master is shown in MR4 OP[6].

Figure 1: Eight-Die, Quad-Channel Package Block Diagram





Background Calibration (Default)

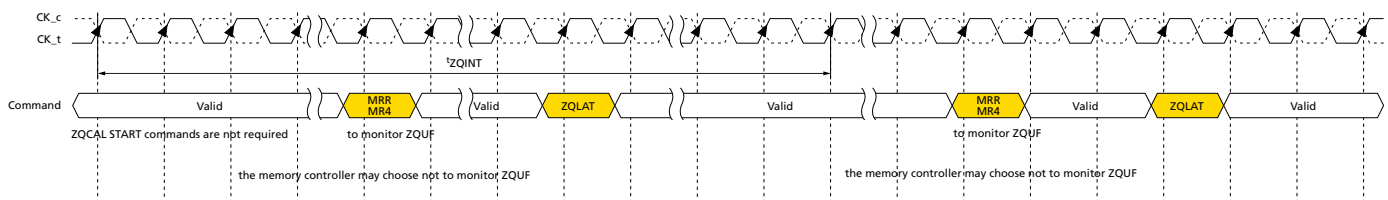
ZQCAL START commands are not required; any ZQCAL START commands received by the device are ignored. Recalibration is performed by the device within the time interval (t_{ZQINT}) specified in MR28 OP[3:2]

RZQ may be shared among a number of die, up to a maximum of NZQ. Self arbitration by the device ensures that up to NZQ die within a package can share a common external ZQ resistor and avoid conflicts. After background calibration is complete, the device sets ZQUF (MR4 OP[5]). This bit is reset by the ZQCAL LATCH command.

The ZQUF bit notifies the system that new calibration results are available and that a ZQCAL LATCH command should be issued to ensure that accurate calibration is consistently maintained. Setting ZQUF is unique to each die regardless of configuration or sharing the ZQ pin or pins. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCAL LATCH commands.

Latching ZQ calibration results is accomplished via the MPC ZQCAL LATCH command. A ZQCAL LATCH command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The results from the most recently completed calibration are always latched with each ZQCAL LATCH command. When a ZQCAL LATCH command executes, the ZQUF bit resets to 0 before expiration of t_{ZQLAT} .

Figure 2: Background ZQ Calibration Timing



Stopping background calibration and recalibration:

Background calibration mode must be stopped by setting ZQ Stop to 1 before entering DVFSQ. ZQ Stop may be reset to 0 when DVFSQ is no longer active.

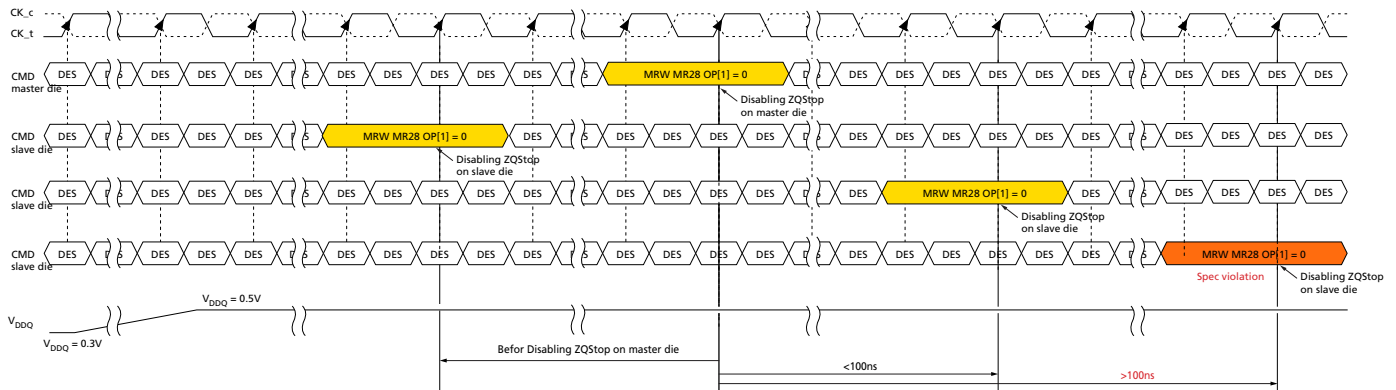
Important note:

To guarantee recalibration of all die that are sharing the ZQ resource within t_{ZQCAL} , the ZQ Stop bit should be reset to 0 for all slave die sharing the ZQ resource either before, or no later than, 100ns after ZQ Stop is reset on the ZQ master die.



TN-62-07: LPDDR5 ZQ Calibration Command-Based Calibration

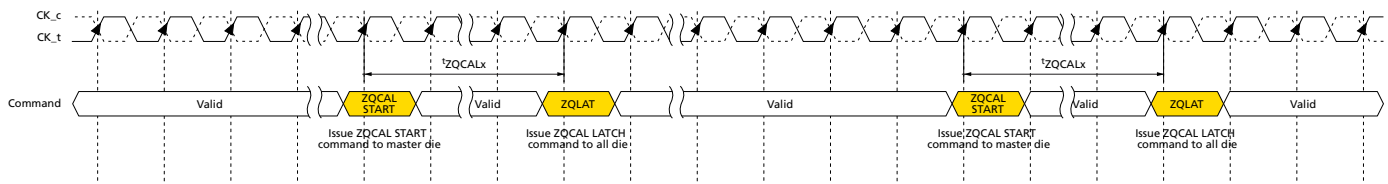
Figure 3: ZQ Stop Reset Timing



Command-Based Calibration

When command-based calibration mode is selected, a ZQCAL START command may be periodically issued to the ZQ master die in each device package. ZQCAL START commands issued to slave die are ignored.

Figure 4: Command-Based Calibration Timing



When the ZQ master die is placed in power-down or deep-sleep mode, ZQCAL START commands are ignored and recalibration does not occur for all die sharing the ZQ resources. All die are recalibrated only when the ZQ master die exits power-down or deep-sleep mode and receives a subsequent ZQCAL START command.

To guarantee recalibration of all die sharing the ZQ resource within t_{ZQCAL} , the ZQ Stop bit should be reset to 0 for all slave die sharing the ZQ resource either before, or no later than, 100ns after the ZQ Stop bit is reset on the ZQ master die.

In command-based calibration mode, following a ZQCAL START command, a ZQCAL LATCH command should be issued to each die after t_{ZQCAL4} , t_{ZQCAL8} , or $t_{ZQCAL16}$ has been met.

Any ZQCAL LATCH command that does not meet the corresponding t_{ZQCAL4} , t_{ZQCAL8} , or $t_{ZQCAL16}$ may latch the result of the most recently completed ZQ calibration.

A ZQCAL LATCH command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The value of ZQUF is undefined when command-based calibration mode is selected.



TN-62-07: LPDDR5 ZQ Calibration Op-Code Bit and Timing Definition for ZQ Calibration

Op-Code Bit and Timing Definition for ZQ Calibration

The following tables provide the op-code definition and timing specification for ZQ calibration.

Table 1: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
ZQUF	R	OP[5]	0b: No change in calibration code since last ZQ LATCH command 1b: Changes in calibration code since last ZQ LATCH command	4
ZQ Master		OP[6]	0b: Not a master die 1b: Master die for ZQ calibration purposes	5, 6
TUF (temperature update flag)		OP[7]	0b: No change in OP[4:0] since last MR4 read 1b: Change in OP[4:0] since last MR4 read (default)	1–3

- Notes:
- When MR4 OP[7] = 1b, the refresh multiplier reported in MR4 OP[4:0] has changed since the last MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.
 - MR4 OP[4:0] bits indicate the latest refresh rate whenever MR4 OP[7] = 1b.
 - See the Temperature Sensor section for information on the recommended frequency of reading MR4.
 - After the power-up initialization and reset sequences have completed, ZQUF MR4 OP[5] = 0b.
 - In command-based calibration mode, ZQCAL START commands only need to be issued to the ZQ master die to maintain accurate calibration. ZQCAL START commands received by non-ZQ master die are ignored. All die which share ZQ pin resources with a ZQ master die that receives a valid ZQCAL START command are calibrated. ZQCAL LATCH commands can be issued to each of these die after tZQCAL4 , tZQCAL8 , or tZQCAL16 has been met.
 - LPDDR5 packages with more than one ZQ pin might include more than one ZQ master die.

Table 2: MR28 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
ZQ Reset	W	OP[0]	0b: Normal operation (default) 1b: ZQ reset	1, 2
ZQ Stop		OP[1]	0b: Normal operation (default) 1b: Background ZQ calibration is halted after tZQSTOP	3, 4
ZQ Interval		OP[3:2]	00b: Background calibration Interval $\leq 32\text{ms}$ 01b: Background calibration Interval $\leq 64\text{ms}$ (default) 10b: Background calibration Interval $\leq 128\text{ms}$ 11b: Background calibration Interval $\leq 256\text{ms}$	5
ZQ Mode		OP[5]	0b: Background ZQ calibration (default) 1b: Command-based ZQ calibration	5

- Notes:
- See ZQCAL timing parameters for calibration latency and timing.
 - Asserting ZQ Reset sets the calibration values to their default setting.
 - When ZQ Stop is enabled, the ZQ resource is available for use by other devices.



TN-62-07: LPDDR5 ZQ Calibration Op-Code Bit and Timing Definition for ZQ Calibration

4. In command-based calibration mode ZQCAL START commands are ignored when MR28 OP[1] = 1b.
5. ZQ Interval and ZQ mode MR settings are only applicable to ZQ master die. These settings are ignored by ZQ slave die.

Table 3: MPC Command Definition for OP[7:0]

Function	Operand	Data
Commands	OP[7:0]	10000001b: START WCK2DQI INTERVAL OSCILLATOR
		10000010b: STOP WCK2DQI INTERVAL OSCILLATOR
		10000011b: START WCK2DQO INTERVAL OSCILLATOR
		10000100b: STOP WCK2DQO INTERVAL OSCILLATOR
		10000101b: ZQCAL START
		10000110b: ZQCAL LATCH
		All others reserved

Table 4: ZQ Calibration Timing

Parameter	Symbol	Min/Max	Value	Unit
ZQ CALIBRATION command to latch time, NZQ ≤ 4	t_{ZQCAL4}	Min	1.5	μs
ZQ CALIBRATION command to latch time, NZQ ≤ 8	t_{ZQCAL8}	Min	3	μs
ZQ CALIBRATION command to latch time, NZQ ≤ 16	$t_{ZQCAL16}$	Min	6	μs
ZQ calibration latch time	t_{ZQLAT}	Min	MAX(30ns, 4 nCK)	ns
ZQ calibration reset time	$t_{ZQRESET}$	Min	MAX(50ns, 3 nCK)	ns
Delay time from ZQ Stop bit set to ZQ resistor available	t_{ZQSTOP}	Max	30	ns
Background calibration interval	t_{ZQINT}	Max	Programmable: 32, 64, 128, or 256	ms
Maximum number of LPDDR5 devices (die) connected to a single ZQ resistor	NZQ	Max	16	Die
Maximum capacitive load on ZQ network	CZQ	Max	TBD	pF



Flow Chart Examples

The following flow charts are representative of one set of die that share a single ZQ resource. These are examples only; there may be other valid methods of operation.

Figure 5: Initialization to Background Calibration, No DVFSQ Support

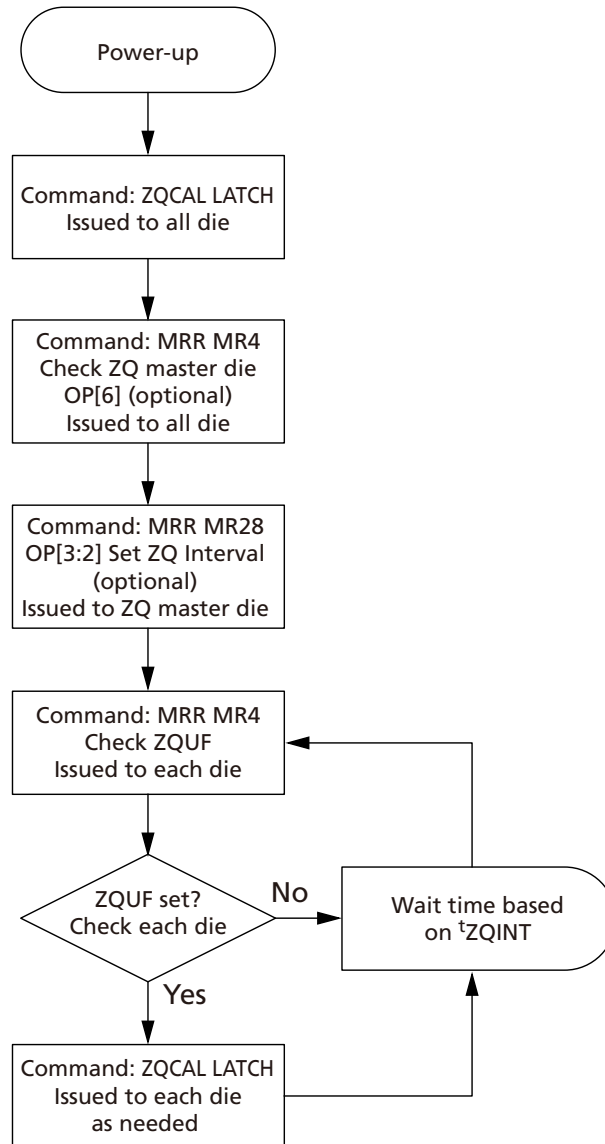
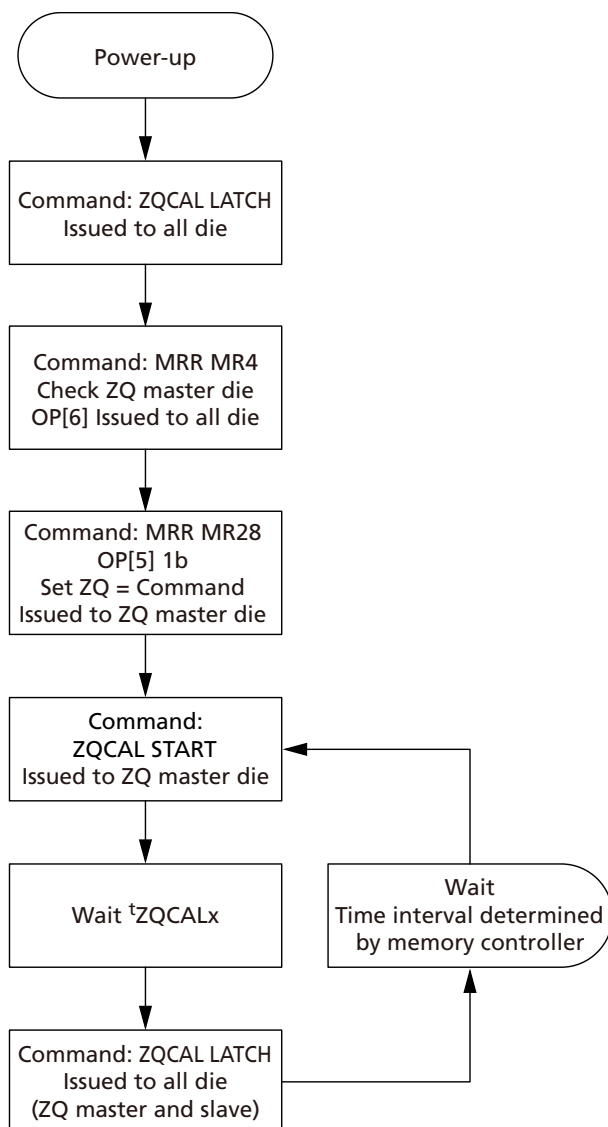




Figure 6: Initialization to Command-Based Calibration, No DVFSQ Support Option 1 (Check ZQ Master and ZQUF)



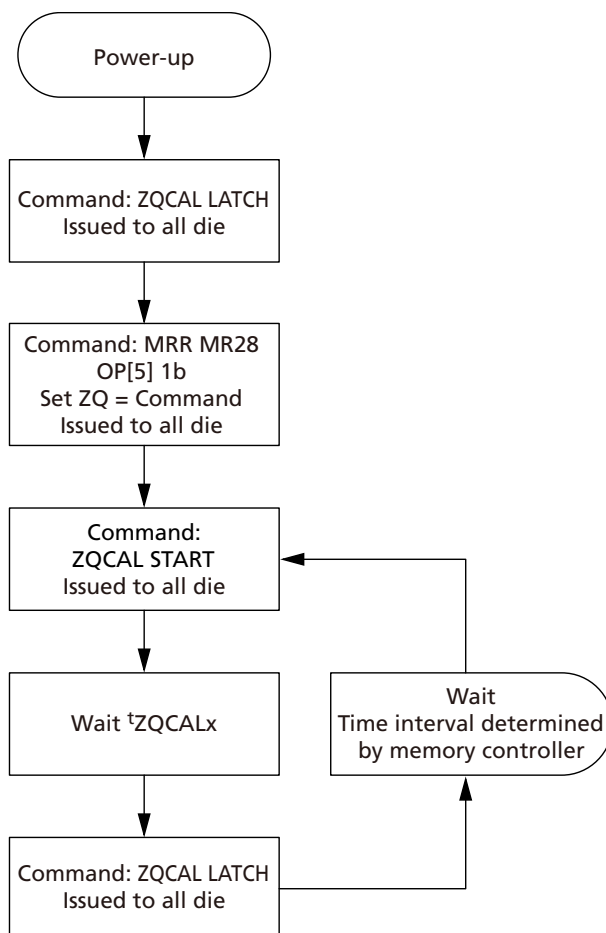
**Figure 7: Initialization to Command-Based Calibration, No DVFSQ Support, Option 2 (Ignore ZQ Master)**

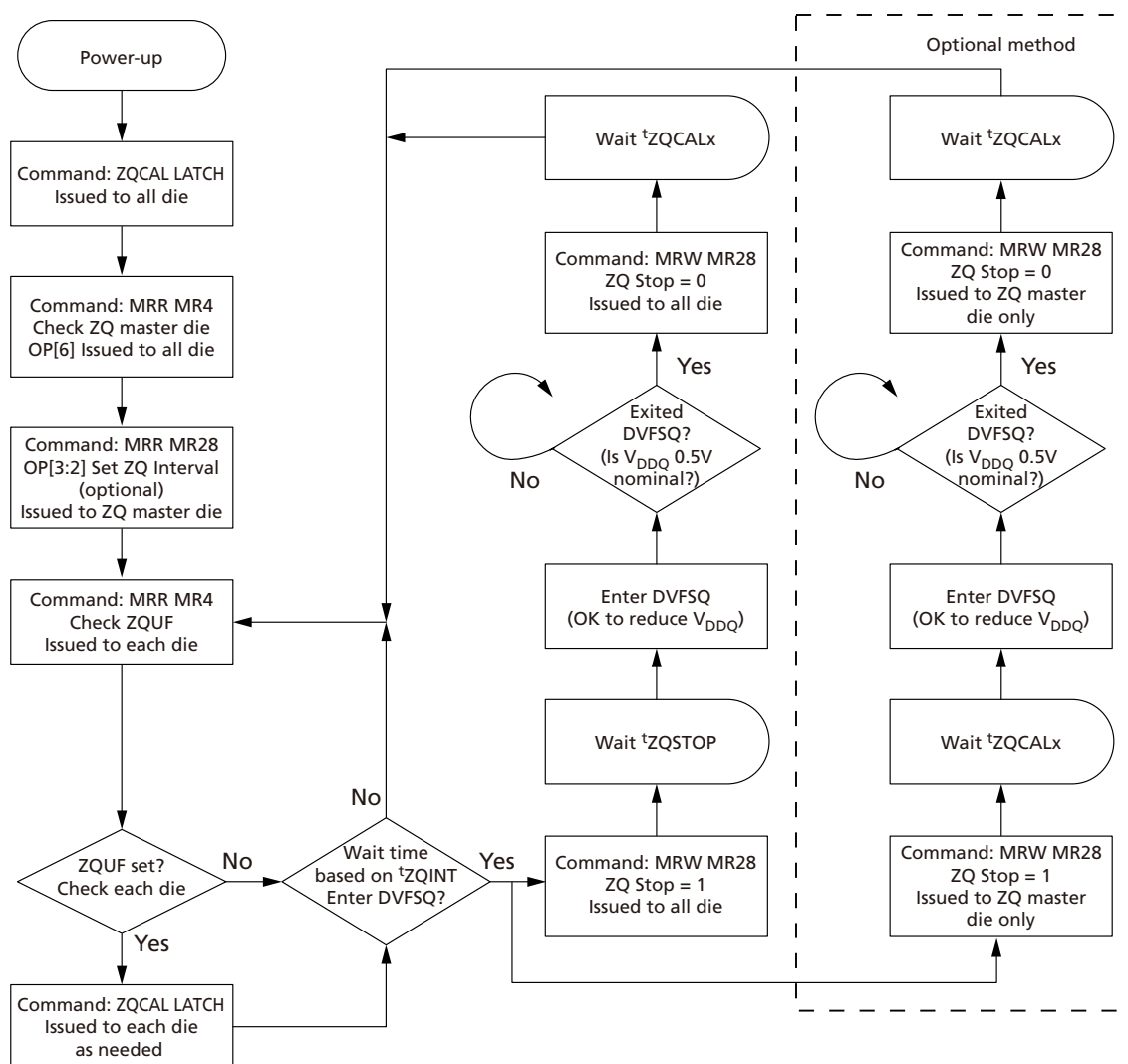
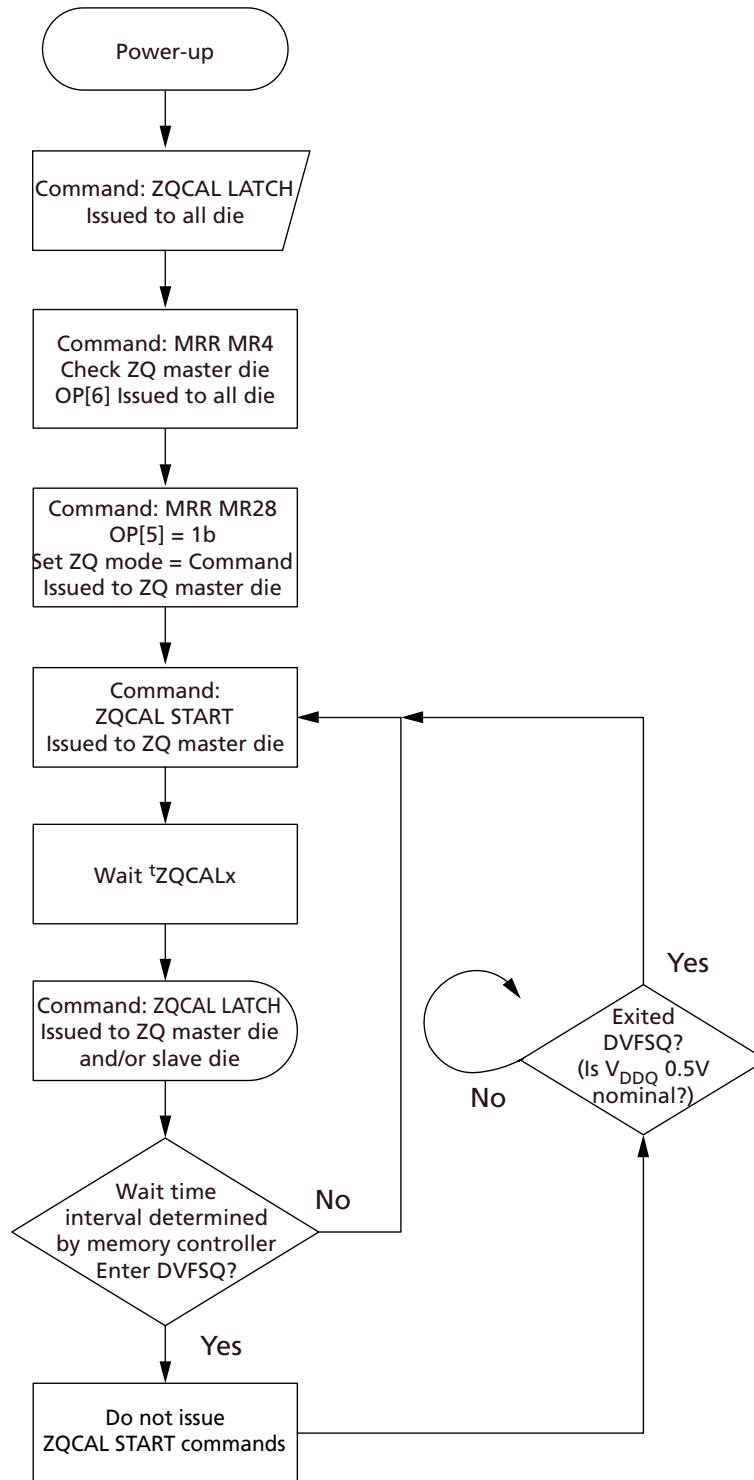

Figure 8: Initialization to Background Calibration With DVFSQ Support



Figure 9: Initialization to Command-Based Calibration With DVFSQ Support




TN-62-07: LPDDR5 ZQ Calibration Changing Between Calibration Modes

Changing Between Calibration Modes

Changing between calibration modes may be performed anytime after power-up and initialization time (T_f) when the device is not in power-down or deep-sleep mode.

Changing Between Calibration Modes When DVFSQ Is Not Active

Figure 10: Changing From Background to Command-Based Mode When DVFSQ Is Not Active

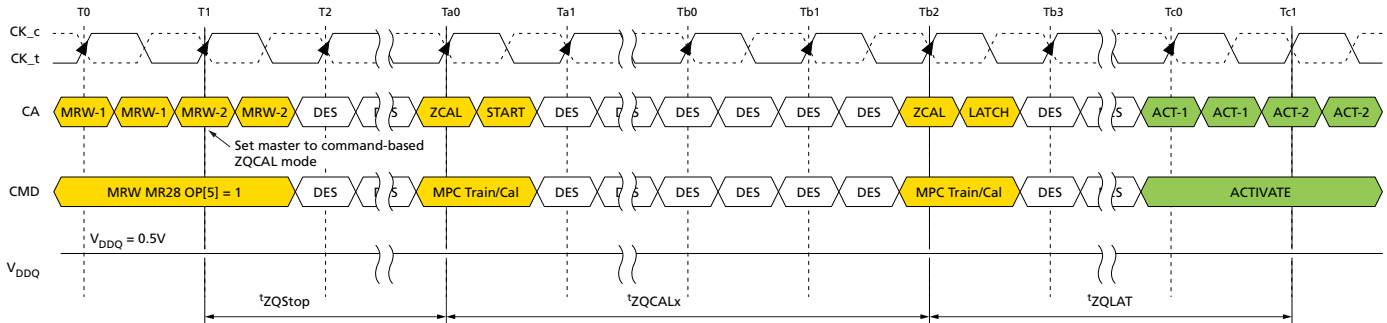
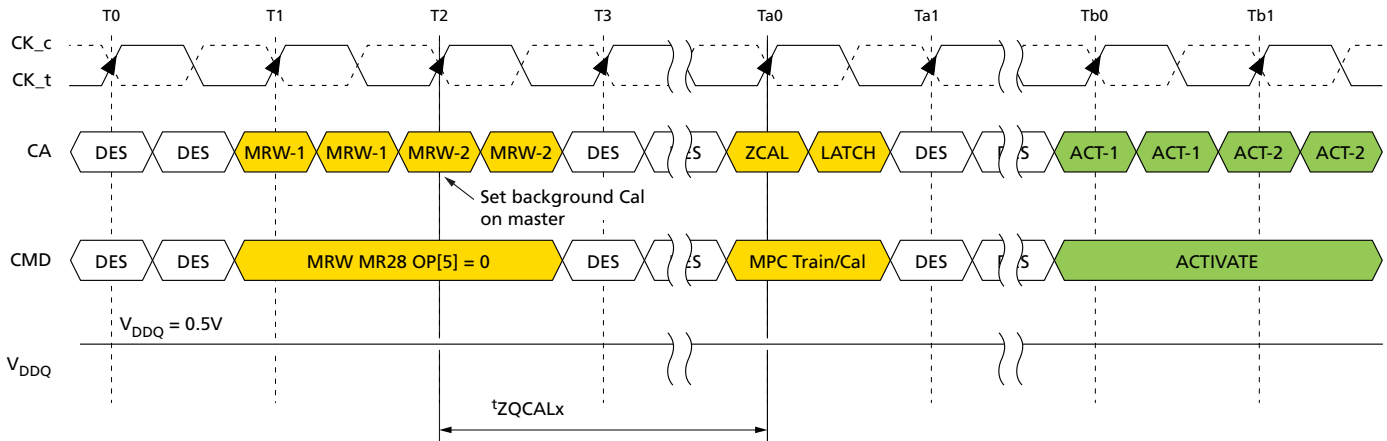
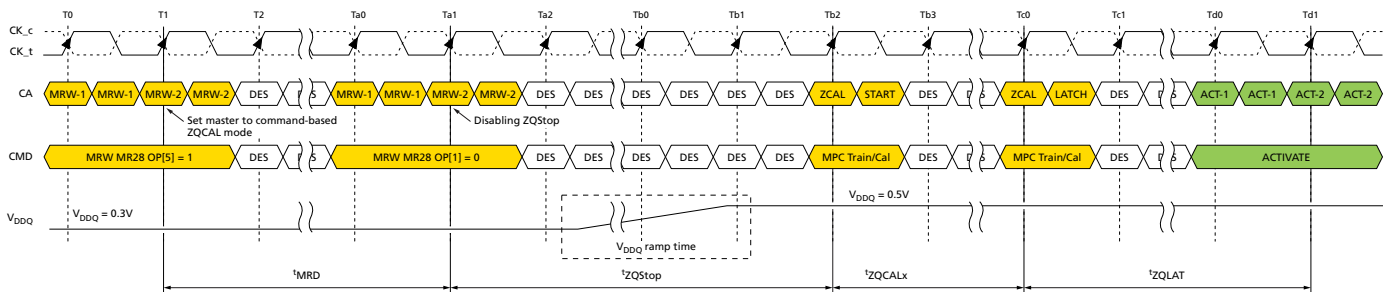


Figure 11: Changing From Command-Based to Background Mode When DVFSQ Is Not Active



Changing Between Calibration Modes When DVFSQ Is Active

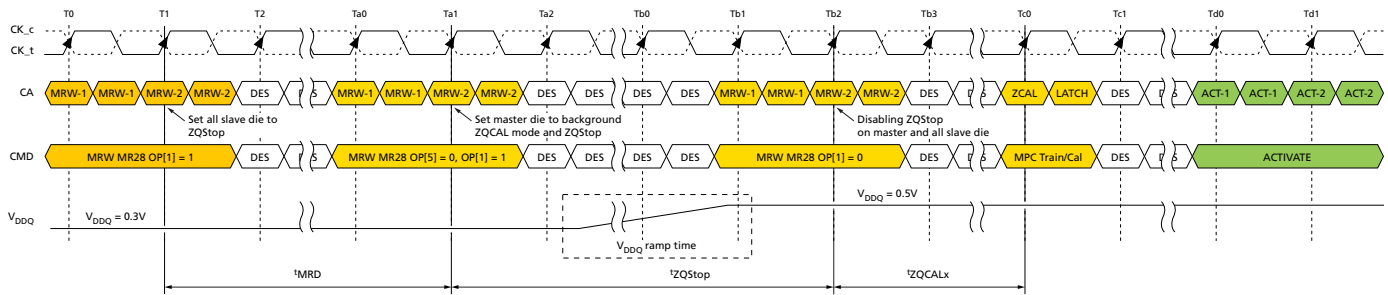
Figure 12: Changing From Background to Command-Based Mode When DVFSQ Is Active





TN-62-07: LPDDR5 ZQ Calibration ZQ External Resistor, Tolerance, and Capacitive Loading

Figure 13: Changing From Command-Based to Background Mode When DVFSQ Is Active



ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ CALIBRATION function, connect a 240 ohm, $\pm 1\%$ tolerance external resistor between the ZQ pin and V_{DDQ}.

The total capacitive loading on the ZQ pin is limited to CZQ.



Revision History

Rev. B – 03/2020

- Editing note for "Stopping background calibration and recalibration"

Rev. A – 12/19

- Initial release

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