General LPDDR5/LPDDR5X Specifications 2

AC/DC and Interface Specifications

Introduction

The three Micron general LPDDR5/LPDDR5X specifications listed below define minimum requirements for x16 or x8, single-channel, LPDDR5/LPDDR5X devices. They include general features, functionality, mode registers, AC and DC characteristics, and other device information.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers

- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications

- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

LPDDR5 and LPDDR5X devices support data rates per pin up to 6400 Mb/s and beyond 6400 Mb/s, respectively.

For specific device features, specifications, or details, refer to the product data sheets.

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Important Notes and Warnings

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.

The absolute maximum DC rating values are only stress ratings. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 1: Absolute Maximum DC Ratings

Parameter/Condition	Symbol	Min	Max	Unit	Note
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.1	V	1
V_{DD2H} supply voltage relative to V_{SS}	V_{DD2H}	–0.4	1.4	V	1
V_{DD2L} supply voltage relative to V_{SS}	V_{DD2L}	–0.4	1.4	V	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	–0.4	1.4	V	1
Voltage on any ball except V_{DD1} relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.4	V	
Storage temperature	T_{STG}	–55	125	°C	2

Notes: 1. See the Power-Up, Initialization, and Power-Off Procedure sections for relationships between power supplies.
2. Storage temperature is the case surface temperature on the center/top side of the LPDDR5 device. For the measurement conditions, refer to JESD51-2A.

DC Operating Conditions

Table 2: Recommended DC Operating Conditions

DRAM	Symbol		Low Frequency Voltage Specification				Z(f) Specification				Note
			Frequency: DC to 2 MHz				2 to 10 MHz		20 MHz		
			Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	
Core 1 power	V_{DD1}		1.70	1.80	1.95	V	100	mohm	170	mohm	1, 2, 9
Core 2 power/Input buffer power	V_{DD2H}		1.01	1.05	1.12	V	40	mohm	80	mohm	1, 2, 9
	V_{DD2L}, Dual VDD2 rail		0.87	0.90	0.97	V	120	mohm	190	mohm	1, 2, 9
	V_{DD2L}, Single VDD2 rail		1.01	1.05	1.12	V	120	mohm	190	mohm	1, 2, 9
I/O buffer power	V_{DDQ}	SPEC Range 1	0.47	0.5	0.57	V	40	mohm	80	mohm	2, 3, 6, 9
		SPEC Range 2	0.27	0.3	0.37	V					2, 4, 9
		Allowable Range 1	0.27	N/A	0.57	V	N/A	–	N/A	–	5, 6, 7, 8

Notes: 1. V_{DD1} generally uses significantly less current than V_{DD2H} and V_{DD2L}.
2. DC to 2 MHz voltage range includes all noise associated with the DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask as defined by V_{dIVW}.
3. SPEC Range 1 is intended for I/O operation with ODT enabled and disabled.
4. SPEC Range 2 is intended for I/O operation with ODT disabled.
5. I/O operation at V_{DDQ} levels outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.
6. Allowable range is valid only when DVFSQ is enabled.

7. 100mV tolerance (–30mV/+70mV) is applied to V_{DDQ} allowable ranges. Refer to the following figure for the V_{DDQ} tolerance definition in each allowable range.
8. Vendors may support LPDDR5 (MR8 OP[1:0] = 00b) 0.6V and LPDDR5X (MR8 OP[1:0] = 01b) 0.45V $_{DDQ,typ}$ as an option. Because ZQ calibration is optimized at V_{DDQ}= 0.5V, the output drive strength may not be guaranteed at LPDDR5 0.6V and LPDDR5X 0.45V. Contact Micron for details.
9. Z(f) is defined for all pins per voltage domain per channel. Z(f) does not include the DRAM package and silicon die.

Figure 1: DC Voltage Range

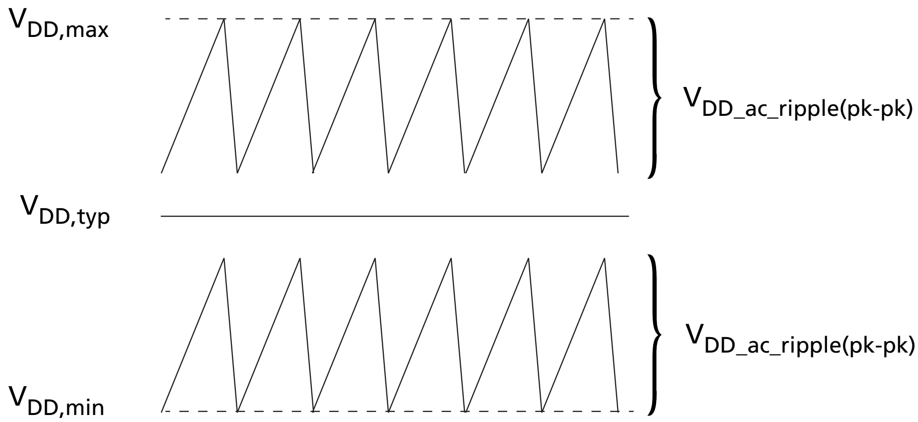


Figure 2: V_{DDQ} Tolerance Definition in Allowable Range

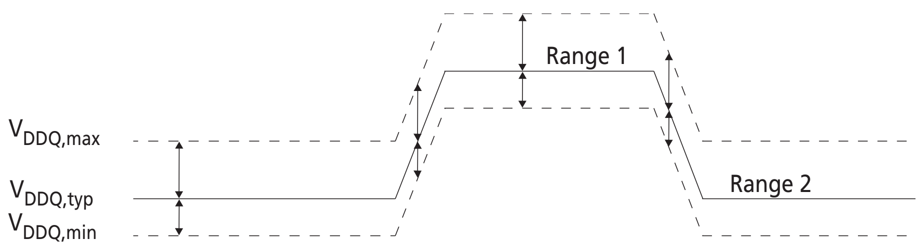
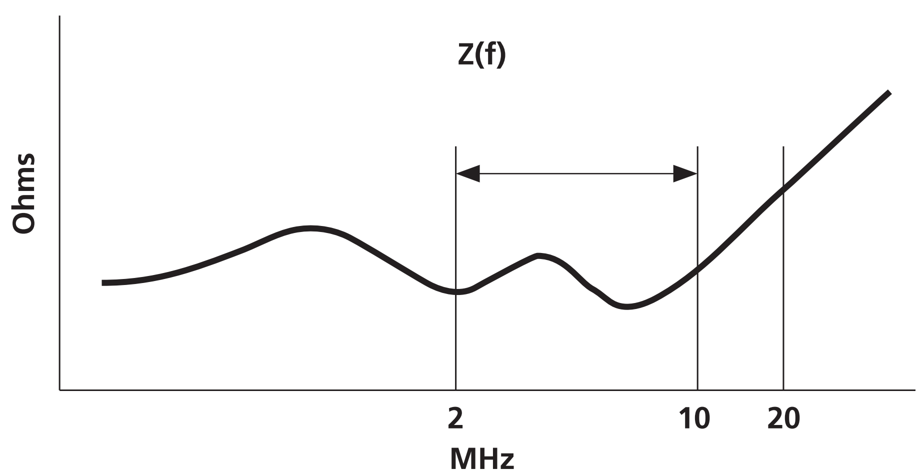
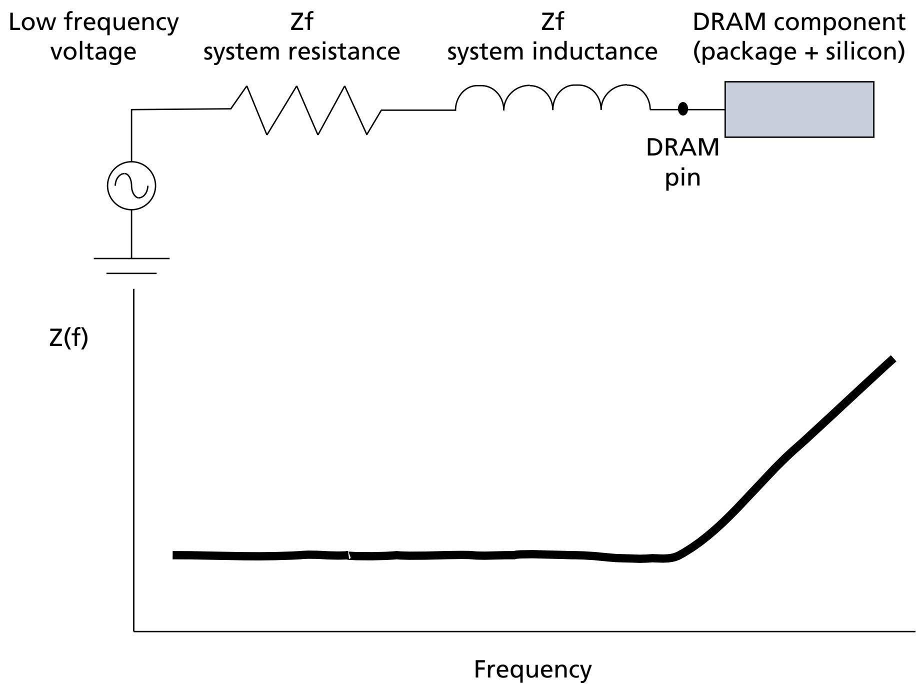


Figure 3: Zprofile/Z(f) of the System at the SDRAM Package Solder Ball (Without DRAM Component)



A simplified electrical system load model for Z(f) with the general frequency response is shown below. The resistance and inductance can be scaled to generalize the specific response to the device pin.

Figure 4: A Simplified Z(f) System Electrical Model and Frequency Response



Electrostatic Discharge Sensitivity Characteristics

Table 3: Electrostatic Discharge Sensitivity (ESD) Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Human body model (HBM)	ESD_{HBM}	1000	–	V	1
Charged-device model (CDM)	ESD_{CDM}	250	–	V	2

Notes: 1. Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures.
2. Refer to JS-002 for measurement procedures.

Input and I/O Pin Leakage Current

Table 4: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input leakage current	I_L	–8	8	μA	1, 2, 3
CS input leakage current	I_{LCS}	-16	16	μA	4, 5

Notes: 1. For CK_t, CK_c, WCK_t, WCK_c , CA, and RESET_n. Any input 0V ≤ V_{IN} ≤ V_{DDQ} (all other pins not under test = 0V).
2. ODT is disabled for CK_t, CK_c, WCK_t, WCK_c, and CA.
3. $V_{DD2L} = V_{DD2H}$.
4. I_{LCS} applies to CS ODT support device. For CS ODT non-support device, CS input leakage current shall meet I_L.
5. CS ODT is disabled.

Table 5: Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output leakage current	I_{OZ}	–10	10	μA	1, 2

Notes: 1. For DQ, RDQS_t, RDQS_c, and DMI. Any I/O 0V ≤ V_{OUT} ≤ V_{DDQ}.
2. I/O status is disabled; high impedance and ODTs are off and RESET_n = H.

RESET_n Signaling

Table 6: Input Level for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
RESET_n V_{IH}	V_{IH_RS}	0.8 × V_{DD2H}	V_{DD2H} + 0.2	V	1
RESET_n V_{IL}	V_{IL_RS}	–0.2	0.2 × V_{DD2H}		

Note: 1. The device uses CMOS with V_{DD2H} RESET_n signaling to ensure a stable RESET operation.

Pull-Up/Pull-Down Output Driver Characteristics and Calibration

Driver Characteristics and Calibration

This section defines the driver characteristics and calibration for all output pins (DQ, DMI, RDQS_t, and RDQS_c).

Table 7: Pull-Down Driver Characteristics and ZQ Calibration

$R_{ONPD,nom}$	Resistor	Min	Nom	Max	Unit
40 ohm	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 ohm	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 ohm	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 ohm	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

Notes: 1. All values are after ZQ calibration. See the Valid Calibration Points table. Without ZQ calibration, R_{ONPD} values are ±30%.
2. R_{ONPD} limits are defined at the same voltage and temperature as when ZQ calibration is done.

Table 8: Pull-Up Characteristics With ZQ Calibration

$V_{OHPU,nom}$	$V_{OH,nom}$ (mV)	Min	Nom	Max	Unit
$V_{DDQ} \times 0.5$	250	0.9	1	1.1	$V_{OH,nom}$

Notes: 1. All values are after ZQ calibration. Without ZQ calibration, $V_{OH,nom}$ values are ±30%.
2. $V_{OH,nom}$ (mV) values are based on a nominal V_{DDQ} = 0.5V, V_{DD2H} = 1.05V.
3. V_{OHPU} limits are defined at the same voltage and temperature as when ZQ calibration is done.
4. V_{OHPU} limits are defined for load termination that matches the SOC ODT setting (in MR17 OP[2:0]) selected at the time ZQ calibration was done. If the selected SOC ODT setting is MR17 OP[2:0] = 000b, then the V_{OHPU} limits are not defined.
5. V_{OHPU} limits are defined as DC levels when all the DQ drivers are driving HIGH.
6. Assume SOC ODT is defined at typical for $V_{OHPU,nom}$.

Table 9: Valid Calibration Points

$V_{OHPU,nom}$	ODT Value					
	240	120	80	60	48	40
$V_{DDQ} \times 0.5$	VALID	VALID	VALID	VALID	VALID	VALID

Note: 1. Once the output is calibrated for a given $V_{OH,nom}$ calibration point, the ODT value may be changed without recalibration.

Table 10: Unterminated Pull-Up Characteristics

$R_{ONUNPU,nom}$	Resistor	Min	Nom	Max	Unit
40 ohm	$R_{ON40UNPU}$	0.7	1	1.3	RZQ/6
60 ohm	$R_{ON60UNPU}$	0.7	1	1.3	RZQ/4
80 ohm	$R_{ON80UNPU}$	0.7	1	1.3	RZQ/3

Table 10: Unterminated Pull-Up Characteristics (Continued)

$R_{ONUNPU,nom}$	Resistor	Min	Nom	Max	Unit
120 ohm	$R_{ON120UNPU}$	0.7	1	1.3	RZQ/2
240 ohm	$R_{ON240UNPU}$	0.7	1	1.3	RZQ/1

Note: 1. R_{ONUNPU} is defined at $V_{OH} = V_{DDQ}/2$.

Table 11: Pull-Down Driver Characteristics in Enhanced DVFSC Mode

$R_{ONPDED,nom}$	Resistor	Min	Nom	Max	Unit
40 ohm	$R_{ON40PDED}$	0.45	1.0	1.75	RZQ/6
48 ohm	$R_{ON48PDED}$	0.45	1.0	1.75	RZQ/5
60 ohm	$R_{ON60PDED}$	0.45	1.0	1.75	RZQ/4
80 ohm	$R_{ON80PDED}$	0.45	1.0	1.75	RZQ/3
120 ohm	$R_{ON120PDED}$	0.45	1.0	1.75	RZQ/2
240 ohm	$R_{ON240PDED}$	0.45	1.0	1.75	RZQ/1

Table 12: Unterminated Pull-Up Characteristics in Enhanced DVFSC Mode

$R_{ONUNPUED,nom}$	Resistor	Min	Nom	Max	Unit
40 ohm	$R_{ON40UNPUED}$	0.45	1.0	1.75	RZQ/6
48 ohm	$R_{ON48UNPUED}$	0.45	1.0	1.75	RZQ/5
60 ohm	$R_{ON60UNPUED}$	0.45	1.0	1.75	RZQ/4
80 ohm	$R_{ON80UNPUED}$	0.45	1.0	1.75	RZQ/3
120 ohm	$R_{ON120UNPUED}$	0.45	1.0	1.75	RZQ/2
240 ohm	$R_{ON240UNPUED}$	0.45	1.0	1.75	RZQ/1

Note: 1. $R_{ONUNPUED}$ is defined at $V_{OH} = V_{DDQ}/2$.

I_{DD} Specification Parameters and Test Conditions

I_{DD} Measurement Conditions

The following definitions are used in the I_{DD} measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)}$ (MAX)
- HIGH: $V_{IN} \geq V_{IH(DC)}$ (MIN)
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following tables.

Table 13: Definition of Switching for CA Input Signals

CK_t Edge	R1	F1	R2	F2	R3	F3	R4	F4	R5	F5	R6	F6	R7	F7	R8	F8
CS	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
CA0	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H

Table 13: Definition of Switching for CA Input Signals (Continued)

CK_t Edge	R1	F1	R2	F2	R3	F3	R4	F4	R5	F5	R6	F6	R7	F7	R8	F8
CA1	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H

Notes: 1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 14: CA Pattern for I_{DD4R} for BG Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	READ	H	L	L	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	
R1	HIGH	DES	L	L	L	L	L	L	L	
F1	LOW		L	L	L	L	L	L	L	
R2	HIGH	READ	H	L	L	L	L	L	L	2
F2	LOW		L	H	L	H	L	L	L	
R3	HIGH	CAS (B3)	L	L	H	H	L	L	L	
F3	LOW		L	L	L	L	L	L	H	
R4	HIGH	READ	H	L	L	H	H	H	H	3
F4	LOW		L	H	H	L	H	H	L	
R5	HIGH	CAS (B3)	L	L	H	H	L	L	L	
F5	LOW		L	L	L	L	L	L	H	
R6	HIGH	READ	H	L	L	H	H	H	H	4
F6	LOW		L	H	L	H	H	H	L	
R7	HIGH	DES	L	L	L	L	L	L	L	
F7	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. Pattern A' is applied to DQ.
4. Pattern B' is applied to DQ.
5. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is BG mode.

Table 15: CA Pattern for I_{DD4R} for 16B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	READ	H	L	L	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	

Table 15: CA Pattern for I_{DD4R} for 16B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R1	HIGH	CAS (B3)	L	L	H	H	L	L	L	
F1	LOW		L	L	L	L	L	L	H	
R2	HIGH	READ	H	L	L	H	H	H	H	2
F2	LOW		L	H	H	L	H	H	L	
R3	LOW	DES	L	L	L	L	L	L	L	
F3	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is 16B mode. In the case of CKR = 2:1, the number of DES commands is increased to match ^{t}CCD.

Table 16: CA Pattern for I_{DD4R} for 8B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	READ	H	L	L	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	
R1	LOW	DES	L	L	L	L	L	L	L	
F1	LOW		L	L	L	L	L	L	L	
R2	LOW	DES	L	L	L	L	L	L	L	2
F2	LOW		L	L	L	L	L	L	L	
R3	HIGH	CAS (B3)	L	L	H	H	L	L	L	
F3	LOW		L	L	L	L	L	L	H	
R4	HIGH	READ	H	L	L	H	H	H	H	3
F4	LOW		L	H	H	L	H	H	L	
R5	LOW	DES	L	L	L	L	L	L	L	
F5	LOW		L	L	L	L	L	L	L	
R6	LOW	DES	L	L	L	L	L	L	L	4
F6	LOW		L	L	L	L	L	L	L	
R7	LOW	DES	L	L	L	L	L	L	L	
F7	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. Pattern A' is applied to DQ.
4. Pattern B' is applied to DQ.
5. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is 8B mode. In the case of CKR = 2:1, the number of DES commands is increased to match ^{t}CCD.

Table 17: CA Pattern for I_{DD4W} for BG Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	WRITE	L	H	H	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	

Table 17: CA Pattern for I_{DD4W} for BG Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R1	LOW	DES	L	L	L	L	L	L	L	
F1	LOW		L	L	L	L	L	L	L	
R2	HIGH	WRITE	L	H	H	L	L	L	L	2
F2	LOW		L	H	L	H	L	L	L	
R3	LOW	DES	L	L	L	L	L	L	L	
F3	LOW		L	L	L	L	L	L	L	
R4	HIGH	WRITE	L	H	H	H	H	H	H	1
F4	LOW		L	H	H	L	H	H	L	
R5	LOW	DES	L	L	L	L	L	L	L	
F5	LOW		L	L	L	L	L	L	L	
R6	HIGH	WRITE	L	H	H	H	H	H	H	2
F6	LOW		L	H	L	H	H	H	L	
R7	LOW	DES	L	L	L	L	L	L	L	
F7	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is BG mode.

Table 18: CA Pattern for I_{DD4W} for 16B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	WRITE	L	H	H	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	
R1	LOW	DES	L	L	L	L	L	L	L	
F1	LOW		L	L	L	L	L	L	L	
R2	HIGH	WRITE	L	H	H	H	H	H	H	2
F2	LOW		L	H	H	L	H	H	L	
R3	LOW	DES	L	L	L	L	L	L	L	
F3	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is 16B mode. In the case of CKR = 2:1, the number of DES commands is increased to match ^{t}CCD.

Table 19: CA Pattern for I_{DD4W}, 8B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R0	HIGH	WRITE	L	H	H	L	L	L	L	1
F0	LOW		L	H	H	L	L	L	L	
R1	LOW	DES	L	L	L	L	L	L	L	
F1	LOW		L	L	L	L	L	L	L	

Table 19: CA Pattern for I_{DD4W}, 8B Mode

Clock Cycle#	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	Note
R2	LOW	DES	L	L	L	L	L	L	L	2
F2	LOW		L	L	L	L	L	L	L	
R3	LOW	DES	L	L	L	L	L	L	L	
F3	LOW		L	L	L	L	L	L	L	
R4	HIGH	WRITE	L	H	H	H	H	H	H	1
F4	LOW		L	H	H	L	H	H	L	
R5	LOW	DES	L	L	L	L	L	L	L	
F5	LOW		L	L	L	L	L	L	L	
R6	LOW	DES	L	L	L	L	L	L	L	2
F6	LOW		L	L	L	L	L	L	L	
R7	LOW	DES	L	L	L	L	L	L	L	
F7	LOW		L	L	L	L	L	L	L	

Notes: 1. Pattern A is applied to DQ.
2. Pattern B is applied to DQ.
3. The pattern above is applied when WCK to CK frequency ratio (CKR) is 4:1 and bank organization is 8B mode. In the case of CKR = 2:1, the number of DES commands is increased to match ^{t}CCD.

Data Pattern DBI Off

Table 20: Data Patterns I_{DD4R} at DBI Off

DQ's – I_{DD4R} DBI Off											# of 1's
Type	BL	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
Pattern A	BL0	1	1	1	1	1	1	1	1	0	8
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	0	0	0	6
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	1	1	1	1	1	1	1	1	0	8
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	0	0	0	6
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	1	1	1	1	1	1	0	0	0	6
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	1	1	0	8
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	1	1	1	1	1	1	0	0	0	6
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	1	1	1	1	1	1	1	1	0	8
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4

Table 20: Data Patterns I_{DD4R} at DBI Off

DQ's – I_{DD4R} DBI Off											# of 1's
Type	**BL**	**DQ[7]**	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	
Pattern A'	BL0	1	1	1	1	1	1	1	1	0	8
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	0	0	0	6
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	1	1	1	1	1	1	1	1	0	8
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	0	0	0	6
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B'	BL0	0	0	0	0	0	0	1	1	0	2
	BL1	0	0	0	0	1	1	1	1	0	4
	BL2	1	1	1	1	1	1	0	0	0	6
	BL3	1	1	1	1	0	0	0	0	0	4
	BL4	1	1	1	1	1	1	1	1	0	8
	BL5	1	1	1	1	0	0	0	0	0	4
	BL6	0	0	0	0	0	0	0	0	0	0
	BL7	0	0	0	0	1	1	1	1	0	4
	BL8	1	1	1	1	1	1	0	0	0	6
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	1	1	0	2
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	0	0	0	0
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	1	1	0	8
	BL15	1	1	1	1	0	0	0	0	0	4
# of 1's		32	32	32	32	32	32	32	32	0	

Notes: 1. Pattern A' is defined by B3 ordering change based on pattern A.
2. Pattern B' is defined by B3 ordering change based on pattern B.

Table 21: Data Patterns I_{DD4W} at DBI Off

DQ's – I_{DD4W} DBI Off										
Type	**BL**	**DQ[7]**	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	**# of 1's**
Pattern A	BL0	1	1	1	1	1	1	1	1	0	8
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	0	0	0	6
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	1	1	1	1	1	1	1	1	0	8
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	1	1	1	1	1	1	0	0	0	6
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	1	1	1	1	1	1	0	0	0	6
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	1	1	1	1	1	1	1	1	0	8
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	1	1	1	1	1	1	0	0	0	6
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	1	1	1	1	1	1	1	1	0	8
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4
# of 1's		16	16	16	16	16	16	16	16	0	

Data Pattern DBI On

Table 22: Data Patterns I_{DD4R} at DBI On

DQ's – IDD4R DBI On										
Type	BL	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1's
Pattern A	BL0	0	0	0	0	0	0	0	0	1	1
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	1	1	1	3
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	0	0	1	1
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	1	1	1	3
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	0	0	0	0	0	0	1	1	1	3
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	0	0	1	1
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	0	0	0	0	0	0	1	1	1	3
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	0	0	0	0	0	0	0	0	1	1
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4

Table 22: Data Patterns I_{DD4R} at DBI On

DQ's – IDD4R DBI On										
Type	**BL**	**DQ[7]**	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	**# of 1's**
Pattern A'	BL0	0	0	0	0	0	0	0	0	1	1
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	1	1	1	3
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	0	0	1	1
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	1	1	1	3
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B'	BL0	0	0	0	0	0	0	1	1	0	2
	BL1	0	0	0	0	1	1	1	1	0	4
	BL2	0	0	0	0	0	0	1	1	1	3
	BL3	1	1	1	1	0	0	0	0	0	4
	BL4	0	0	0	0	0	0	0	0	1	1
	BL5	1	1	1	1	0	0	0	0	0	4
	BL6	0	0	0	0	0	0	0	0	0	0
	BL7	0	0	0	0	1	1	1	1	0	4
	BL8	0	0	0	0	0	0	1	1	1	3
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	1	1	0	2
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	0	0	0	0
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	0	0	1	1
	BL15	1	1	1	1	0	0	0	0	0	4
# of 1's		16	16	16	16	16	16	32	32	16	

Notes: 1. Pattern A' is defined by B3 ordering change based on pattern A.
2. Pattern B' is defined by B3 ordering change based on pattern B.

Table 23: Data Patterns I_{DD4W} at DBI On

DQ's – IDD4W DBI On										
Type	BL	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1's
Pattern A	BL0	0	0	0	0	0	0	0	0	1	1
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	0	0	0	0
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	1	1	0	2
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	1	1	1	3
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	0	0	1	1
	BL9	1	1	1	1	0	0	0	0	0	4
	BL10	0	0	0	0	0	0	0	0	0	0
	BL11	0	0	0	0	1	1	1	1	0	4
	BL12	0	0	0	0	0	0	1	1	0	2
	BL13	0	0	0	0	1	1	1	1	0	4
	BL14	0	0	0	0	0	0	1	1	1	3
	BL15	1	1	1	1	0	0	0	0	0	4
Pattern B	BL0	0	0	0	0	0	0	1	1	1	3
	BL1	1	1	1	1	0	0	0	0	0	4
	BL2	0	0	0	0	0	0	1	1	0	2
	BL3	0	0	0	0	1	1	1	1	0	4
	BL4	0	0	0	0	0	0	0	0	0	0
	BL5	0	0	0	0	1	1	1	1	0	4
	BL6	0	0	0	0	0	0	0	0	1	1
	BL7	1	1	1	1	0	0	0	0	0	4
	BL8	0	0	0	0	0	0	1	1	0	2
	BL9	0	0	0	0	1	1	1	1	0	4
	BL10	0	0	0	0	0	0	1	1	1	3
	BL11	1	1	1	1	0	0	0	0	0	4
	BL12	0	0	0	0	0	0	0	0	1	1
	BL13	1	1	1	1	0	0	0	0	0	4
	BL14	0	0	0	0	0	0	0	0	0	0
	BL15	0	0	0	0	1	1	1	1	0	4
# of 1's		8	8	8	8	8	8	16	16	8	

I_{DD} Specifications

Table 24: I_{DD} Specifications

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: $^tCK = {}^tCK,min; {}^tRC = {}^tRC,min$; CS is LOW between valid commands; CA bus inputs are switching: Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled; WCK inputs are stable	I_{DD01}	V_{DD1}	9
	I_{DD02H}	V_{DD2H}	
	I_{DD02L}	V_{DD2L}	
	I_{DD0Q}	V_{DDQ}	3
Idle power-down standby current: $^tCK = {}^tCK,min$; POWER-DOWN command is issued; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT is disabled WCK inputs are stable	I_{DD2P1}	V_{DD1}	
	I_{DD2P2H}	V_{DD2H}	
	I_{DD2P2L}	V_{DD2L}	
	I_{DD2PQ}	V_{DDQ}	3
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable	I_{DD2PS1}	V_{DD1}	
	$I_{DD2PS2H}$	V_{DD2H}	
	$I_{DD2PS2L}$	V_{DD2L}	
	I_{DD2PSQ}	V_{DDQ}	3
Idle non power-down standby current: $^tCK = {}^tCK,min$; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable	I_{DD2N1}	V_{DD1}	
	I_{DD2N2H}	V_{DD2H}	
	I_{DD2N2L}	V_{DD2L}	
	I_{DD2NQ}	V_{DDQ}	3
Idle non power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable	I_{DD2NS1}	V_{DD1}	
	$I_{DD2NS2H}$	V_{DD2H}	
	$I_{DD2NS2L}$	V_{DD2L}	
	I_{DD2NSQ}	V_{DDQ}	3
Active power-down standby current: $^tCK = {}^tCK,min$; CS is LOW; One bank is active; POWER-DOWN ENTRY command is issued; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable	I_{DD3P1}	V_{DD1}	9
	I_{DD3P2H}	V_{DD2H}	
	I_{DD3P2L}	V_{DD2L}	
	I_{DD3PQ}	V_{DDQ}	3
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD3PS1}	V_{DD1}	9
	$I_{DD3PS2H}$	V_{DD2H}	
	$I_{DD3PS2L}$	V_{DD2L}	8, 9
	I_{DD3PSQ}	V_{DDQ}	4
Active non power-down standby current: $^tCK = {}^tCK,min$; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD3N1}	V_{DD1}	9
	I_{DD3N2H}	V_{DD2H}	
	I_{DD3N2L}	V_{DD2L}	8, 9
	I_{DD3NQ}	V_{DDQ}	4

Table 24: I_{DD} Specifications

Parameter/Condition	Symbol	Power Supply	Note
Operating burst READ current BG mode: ^{t}CK = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One bank in each bank group 1 and 2 is active;** BL = 16 or 32; RL = RL,min; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2H}	V_{DD2H}	
	I_{DD4R2L}	V_{DD2L}	8
	I_{DD4RQ}	V_{DDQ}	5
Operating burst READ current 8B/16B mode: ^{t}CH = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One banks is active;** BL = 16 or 32 for 16B, BL32 for 8B; RL = RL,min; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2H}	V_{DD2H}	
	I_{DD4R2L}	V_{DD2L}	8
	I_{DD4RQ}	V_{DDQ}	5
Operating burst READ current 8B/16B mode with DVFSC or E-DVFSC: ^{t}CH = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One bank is active;** BL = 16 or 32 for 16B, BL32 for 8B; RL = RL,min; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	$I_{DD4RDVFSC1}$	V_{DD1}	11
	$I_{DD4RDVFSC2H}$	V_{DD2H}	
	$I_{DD4RDVFSC2L}$	V_{DD2L}	8, 11, 12
	$I_{DD4RDVFSCQ}$	V_{DDQ}	5, 11
Operating burst WRITE current BG mode: ^{t}CK = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One bank in each bank group 1 and 2 is active;** BL = 16 or 32; W L= WL,min; CA bus inputs are switching; 50% data change each burst transfer; RDQS_t is stable (if Link ECC is enabled); ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2H}	V_{DD2H}	
	I_{DD4W2L}	V_{DD2L}	8
	I_{DD4WQ}	V_{DDQ}	4
Operating burst WRITE current 8B/16B mode: ^{t}CH = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One banks is active;** BL = 16 or 32 for 16B, BL32 for 8B; WL = WL,min; CA bus inputs are switching; 50% data change each burst transfer; RDQS_t is stable (if Link ECC is enabled); ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2H}	V_{DD2H}	
	I_{DD4W2L}	V_{DD2L}	8
	I_{DD4WQ}	V_{DDQ}	4
Operating burst WRITE current 8B/16B mode with DVFSC or E-DVFSC: ^{t}CH = ^{t}CK,min; ^{t}WCK = ^{t}WCK,min; CS is LOW between valid commands **One bank is active;** BL = 16 or 32 for 16B, BL32 for 8B; WL = WL,min; CA bus inputs are switching; 50% data change each burst transfer; RDQS_t is stable (if Link ECC is enabled); ODT is disabled	$I_{DD4WDVFSC1}$	V_{DD1}	11
	$I_{DD4WDVFSC2H}$	V_{DD2H}	
	$I_{DD4WDVFSC2L}$	V_{DD2L}	8, 11, 12
	$I_{DD4WDVFSCQ}$	V_{DDQ}	4, 11
All-bank REFRESH burst current: ^{t}CK = ^{t}CK,min; CS is LOW between valid commands; ^{t}RC = ^{t}RFCab,min; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD51}	V_{DD1}	
	I_{DD52H}	V_{DD2H}	
	I_{DD52L}	V_{DD2L}	8
	I_{DD5Q}	V_{DDQ}	4
All-bank REFRESH burst current with E-DVFSC: ^{t}CK = 1.25ns (800 MHz); CKR=2:1; CS is LOW between valid commands; ^{t}RC = ^{t}RFCab,min; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is "Don't Care"; ODT is disabled; WCK inputs are stable and static	I_{DD5ED1}	V_{DD1}	
	$I_{DD5ED2H}$	V_{DD2H}	
	$I_{DD5ED2L}$	V_{DD2L}	8
	I_{DD5EDQ}	V_{DDQ}	4

Table 24: I_{DD} Specifications

Parameter/Condition	Symbol	Power Supply	Note
All-bank REFRESH average current: $^tCK = {}^tCK,min$; CS is LOW between valid commands; $^tRC = {}^tREFI$; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD5AB1}	V_{DD1}	
	$I_{DD5AB2H}$	V_{DD2H}	
	$I_{DD5AB2L}$	V_{DD2L}	8
	I_{DD5ABQ}	V_{DDQ}	4
All-bank REFRESH average current with E-DVFSC: ^tCK = 1.25ns (800 MHz); CKR=2:1; CS is LOW between valid commands; $^tRC = {}^tREFI$; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is "Don't Care"; ODT is disabled; WCK inputs are stable and static	$I_{DD5ABED1}$	V_{DD1}	
	$I_{DD5ABED2H}$	V_{DD2H}	
	$I_{DD5ABED2L}$	V_{DD2L}	8
	$I_{DD5ABEDQ}$	V_{DDQ}	4
Per-bank REFRESH average current: $^tCH = {}^tCK,min$; CS is LOW between valid commands; $^tRC = {}^tREFI/8$; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD5PB1}	V_{DD1}	
	$I_{DD5PB2H}$	V_{DD2H}	
	$I_{DD5PB2L}$	V_{DD2L}	8
	I_{DD5PBQ}	V_{DDQ}	4
Per-bank REFRESH average current with E-DVFSC: ^tCK = 1.25ns (800MHz); CKR=2:1; CS is LOW between valid commands; $^tRC = {}^tREFI/8$; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is "Don't Care"; ODT is disabled; WCK inputs are stable and static	$I_{DD5PBED1}$	V_{DD1}	
	$I_{DD5PBED2H}$	V_{DD2H}	
	$I_{DD5PBED2L}$	V_{DD2L}	8
	$I_{DD5PBEDQ}$	V_{DDQ}	4
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD61}	V_{DD1}	6, 7
	I_{DD62H}	V_{DD2H}	
	I_{DD62L}	V_{DD2L}	6, 7, 8
	I_{DD6Q}	V_{DDQ}	4, 6, 7, 8
Deep-sleep mode current: CK_t = LOW, CK_c = HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static	I_{DD6DS1}	V_{DD1}	6, 7
	$I_{DD6DS2H}$	V_{DD2H}	
	$I_{DD6DS2L}$	V_{DD2L}	6, 7, 8
	I_{DD6DSQ}	V_{DDQ}	4, 6, 7

Notes:
1. Published I_{DD} values are the maximum IDD values considering the worst case conditions of process, temperature, and voltage.
2. ODT disabled MR11 OP[6:4] = 000b
3. I_{DD} current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of V_{DDQ} and V_{DD2H}/V_{DD2L}.
5. Guaranteed by design with an output load = 5pF and R_{ON} = 40 ohm.
6. The 1x self refresh rate is the rate that the LPDDR5 device is refreshed internally during self refresh before going into the elevated temperature range.
7. This is the general definition that applies to full-array self refresh.
8. When MR13 OP[7] is high, single V_{DD2} rail, V_{DD2L} current shall be added to V_{DD2H} current.
9. I_{DD} values can be different according to the bank organization set by MR3 OP[4:3].
10. When DVFSC is enabled, the minimum ^tCK shall be set by following the DVFSC operating frequency.
11. I_{DD} values can be different according to the DVFSC set by MR19 OP[1:0].

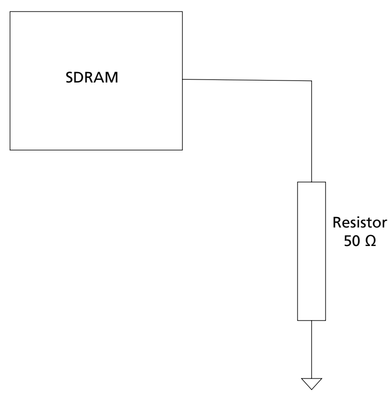
12. When the LPDDR5X device(MR8 OP[1:0]=01b) supports both DVFSC and E-DVFSC mode(MR41 OP[2:1]=10b), the value represents the VDD2L current whichever is bigger.

AC and DC Input/Output Measurement Levels

Driver Output Timing Reference load

Timing reference loads are not intended to be precise representations of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions. Generally, one or more coaxial transmission lines are terminated at the tester electronics.

Figure 5: Driver Output Reference Load for Timing and Slew Rate



Single-Ended Output Slew Rate

Figure 6: Single-Ended Output Slew Rate

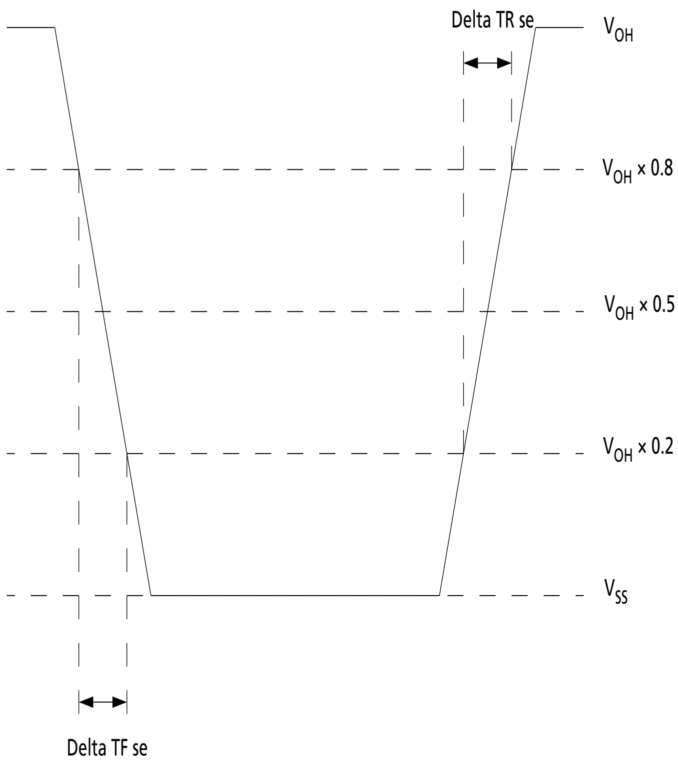


Table 25: Output Slew Rate (Single-Ended)

Parameter	Symbol	Min	Max	Unit	Note
Single-ended output slew rate	SRQse	TBD	TBD	V/ns	1
Output slew rate matching ratio (rise to fall)	–	TBD	TBD		

Notes: 1. Definitions for the table: SR = slew rate, Q = query output (like in DQ, which stands for data-in query output), se = single-ended signals.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between V_{OH} × TBD and V_{OH} × TBD.
5. Slew rates are measured under average SSO conditions with 50% of DQ signals per data byte switching.
6. The parameters for single ended apply to RDQS_t and RDQS_c when either RDQS_t or RDQS_c is disabled.

Differential Output Slew Rate

Figure 7: Differential Output Slew Rate

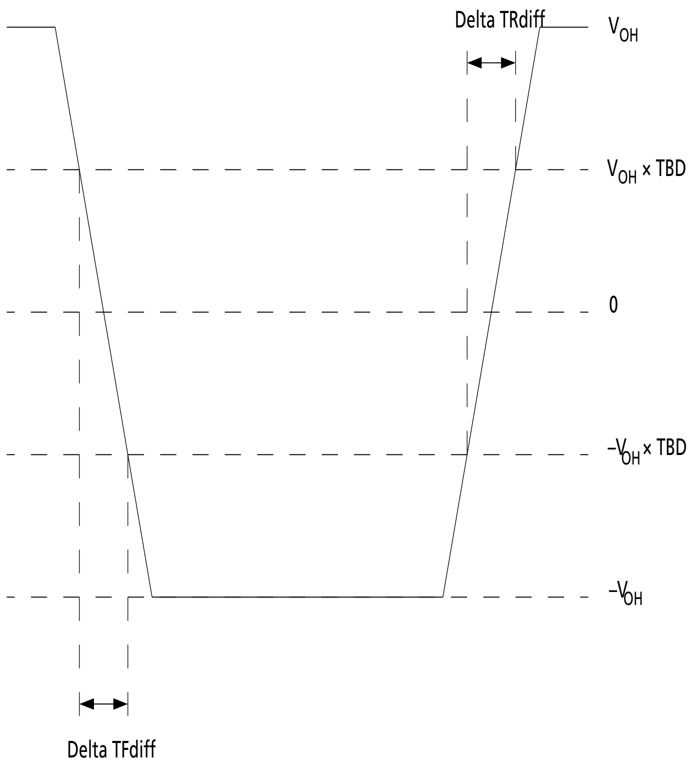
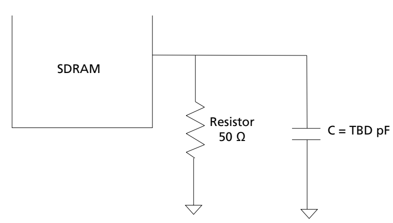


Table 26: Differential Output Slew Rate

Parameter	Symbol	Min	Max	Unit	Note
Differential output slew rate	SRQdiff	TBD	TBD	V/ns	1, 2, 3

Notes: 1. The output slew rate for falling and rising edges is defined and measured between $-V_{OH}$ x TBD and V_{OH} x TBD.
2. Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces $V_{OH(AC)}$ at high frequency close to Fmax, the signal using PRBS data pattern may not achieve a full swing at such conditions.
3. These values are measured with output reference load, as shown in the figure below, or guaranteed by design.



AC Overshoot/Undershoot

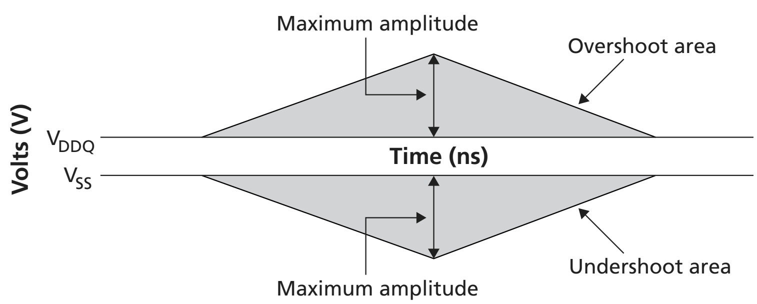
Table 27: AC Overshoot/Undershoot

Parameter	Min/Max	Value	Unit
Maximum peak amplitude allowed for overshoot area	Max	0.35	V
Maximum peak amplitude allowed for undershoot area	Max	0.35	V
Maximum overshoot area above V_{DD}/V_{DDQ}	Max	0.8	V-ns
Maximum undershoot area below V_{SS}	Max	0.8	V-ns

Table 28: AC Overshoot/Undershoot for LVSTL

Parameter	Min/Max	Data Rate (Mb/s)				Unit
		1600	3200	5500	6400	
Maximum peak amplitude allowed for overshoot area	Max	0.3	0.3	0.3	0.3	V
Maximum peak amplitude allowed for undershoot area	Max	0.3	0.3	0.3	0.3	V
Maximum overshoot area above V_{DD2H}/V_{DDQ}	Max	0.1	0.1	0.1	0.1	V-ns
Maximum undershoot area above V_{SS}	Max	0.1	0.1	0.1	0.1	V-ns

Figure 8: Overshoot and Undershoot Definition



Notes: 1. V_{DD} is V_{DD2H} for CA[6:0], CK_t/c, CS, and RESET_n. V_{DD} is V_{DDQ} for DQ, DMI, RDQS_t, and WCK_t/c.
2. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
3. Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

Differential Mode Input Voltage for CK

Differential Input Voltage for CK

The minimum input voltage needed to satisfy both the V_{indiff_CK} and $V_{indiff\_CK}/2$ specification at the input receiver and their measurement period is 1^tCK. V_{indiff_CK} is the peak-to-peak voltage centered on 0 volts differential and $V_{indiff\_CK}/2$ is max and min peak voltage from 0V.

Figure 9: CK Differential Input Voltage Definition

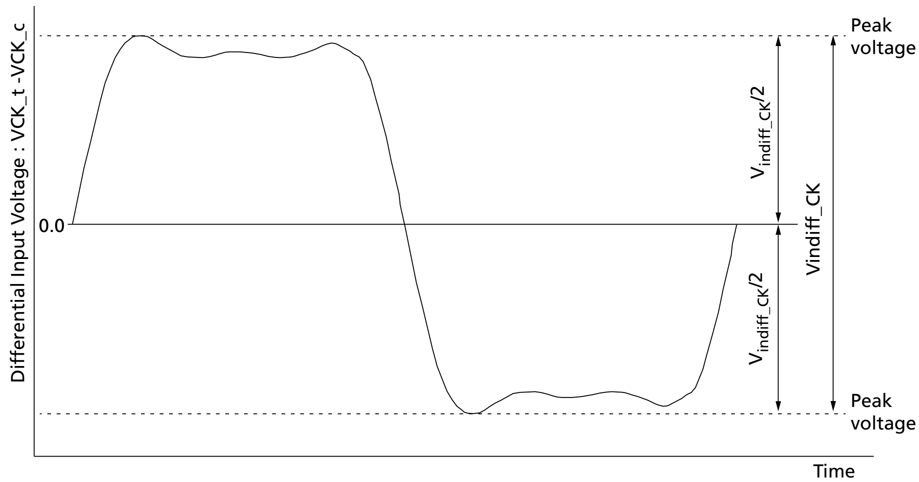


Table 29: CK Differential Input Voltage Timing

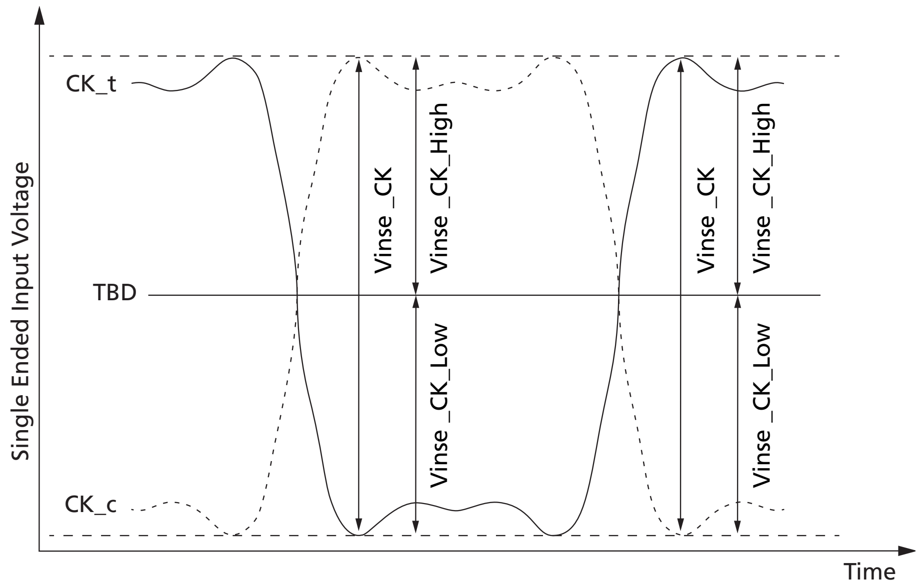
Parameter	Symbol	Clock Frequency										Unit	Note
		266 MHz		533 MHz		800 MHz		937 MHz		1066 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK differential input voltage	V_{indiff_CK}	350	–	350	–	350	–	350	–	350	–	mV	1, 2

Notes: 1. Refer to the latency table to match the clock rate to the data rate.
2. The peak voltage of differential CK signals is calculated in the following equation.
V_{indiff_CK} = (Max peak voltage) - (Min peak voltage)
Max peak voltage = Max(f(t))
Min peak voltage = Min(f(t))
$f(t) = V_{CK\_t} - V_{CK\_c}$

Single-Ended Input Voltage for CK

The minimum input voltage needed to satisfy both V_{inse_CK}, V_{inse_CK} High/Low specification at the input receiver.

Figure 10: Clock Single-Ended Input Voltage



Note: 1. TBD is the LPDDR5 SDRAM internal setting value determined by V_{REF} training.

Table 30: Clock Single-Ended Input Voltage

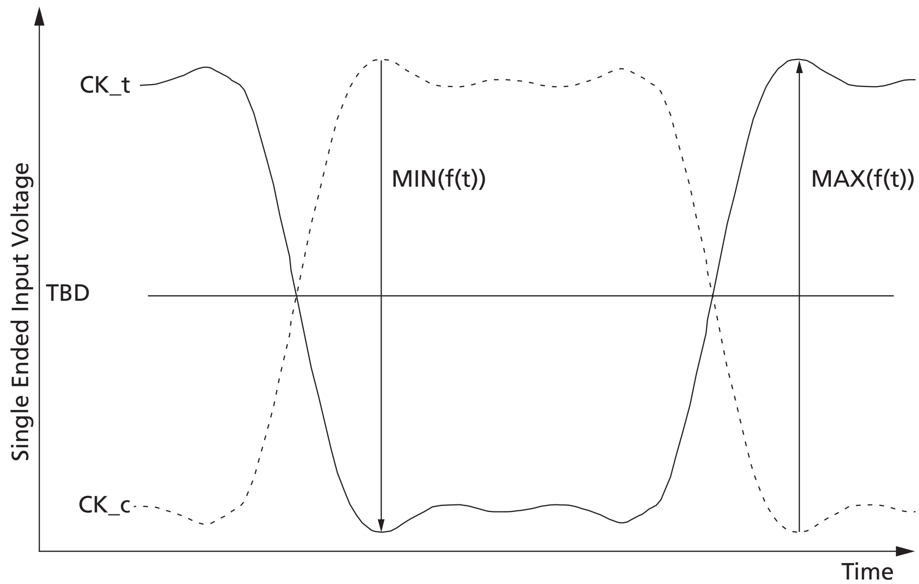
Parameter	Symbol	Clock Frequency										Unit	Note
		266 MHz		533 MHz		800 MHz		937 MHz		1066 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock single-ended input voltage	Vinse_CK	175	–	175	–	175	–	175	–	175	–	mV	
Clock single-ended input voltage HIGH from TBD	Vinse_CK_High	87.5	–	87.5	–	87.5	–	87.5	–	87.5	–	mV	
Clock single-ended input voltage LOW from TBD	Vinse_CK_Low	87.5	–	87.5	–	87.5	–	87.5	–	87.5	–	mV	

Peak Voltage Calculation Method

The peak voltage of differential clock signals are calculated in the following equation.

- $V_{IH.DIFF.peak}$ voltage = Max(f(t))
- $V_{IL.DIFF.peak}$ voltage = Min(f(t))
- $f(t) = V_{CK\_t} - V_{CK\_c}$

Figure 11: Definition of Differential Clock Peak Voltage

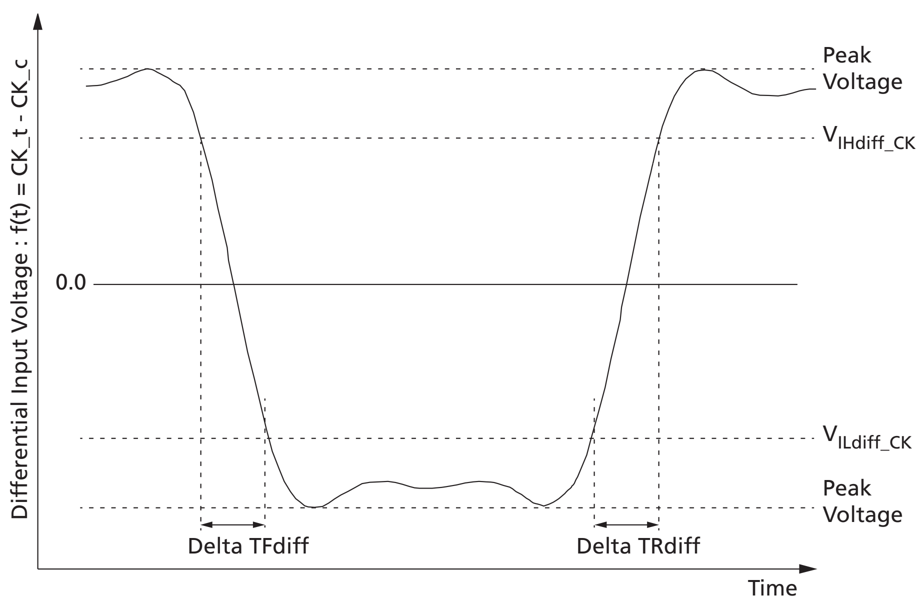


Note: 1. TBD is the LPDDR5 SDRAM internal setting value determined by V_{REF} training.

Differential Input Slew Rate Definition for CK

The input slew rate for differential signals (CK_t, CK_c) is defined and measured in the following figure and tables.

Figure 12: Differential Input Slew Rate Definition for CK_t, CK_c



Notes: 1. The differential signal rising edge slope from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic.
2. The differential signal falling edge slope from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic.

Table 31: Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	From	To	Defined by
Differential input slew rate for rising edge (CK_t-CK_c)	V_{ILdiff_CK}	V_{IHdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert/\Delta TRdiff$
Differential input slew rate for falling edge (CK_t-CK_c)	V_{IHdiff_CK}	V_{ILdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert/\Delta TFdiff$

Table 32: Differential Input Level for CK_t, CK_c

		Clock Frequency											
		266 MHz		533 MHz		800 MHz		937 MHz		1066 MHz			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Differential input HIGH	V_{IHdiff_CK}	145	–	145	–	145	–	145	–	145	–	mV	
Differential input LOW	V_{ILdiff_CK}	–	145	–	145	–	145	–	145	–	145	mV	

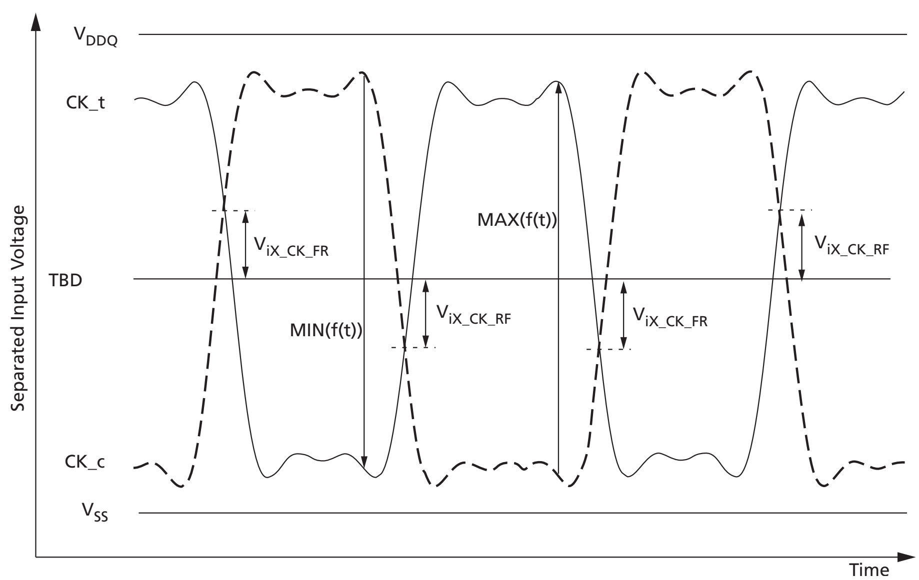
Table 33: Differential Input Slew Rate for CK_t, CK_c

		Clock Frequency											
		266 MHz		533 MHz		800 MHz		937 MHz		1066 MHz			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Differential input slew rate for CK	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns	

Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in the following table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complimentary signals to the mid level that is TBD.

Figure 13: Differential Input Cross Point Slew Rate Definition for CK_t, CK_c



Note: 1. The base level of $V_{IX\_CK\_FR}/V_{IX\_CK\_RF}$ is TBD that is LPDDR5 SDRAM internal setting value by V_{REF} training.

Table 34: Cross Point Voltage for Differential Input Signals (CK)

Parameter	Symbol	Clock Frequency										Unit	Note
		266 MHz		533 MHz		800 MHz		937 MHz		1066 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK differential input cross point voltage ratio	V_{IX}_CK_ratio	–	25	–	25	–	25	–	25	–	25	%	1, 2

Notes: 1. V_{IX}_CK_ratio is defined by this equation: V_{IX}_CK_ratio = $V_{IX\_CK\_FR}$/\|Min(f(t))\|
2. V_{IX}_CK_ratio is defined by this equation: V_{IX}_CK_ratio = $V_{IX\_CK\_RF}$/Max(f(t))

Differential Mode Input Voltage for WCK

Differential Input Voltage for WCK

The minimum input voltage needed to satisfy both the V_{indiff_WCK} and $V_{indiff\_WCK}/2$ specification at the input receiver. Their measurement period is 1^tWCK. V_{indiff_WCK} is the peak-to-peak voltage centered on 0 volts differential and $V_{indiff\_WCK}/2$ is max and min peak voltage from 0V.

Figure 14: WCK Differential Input Voltage

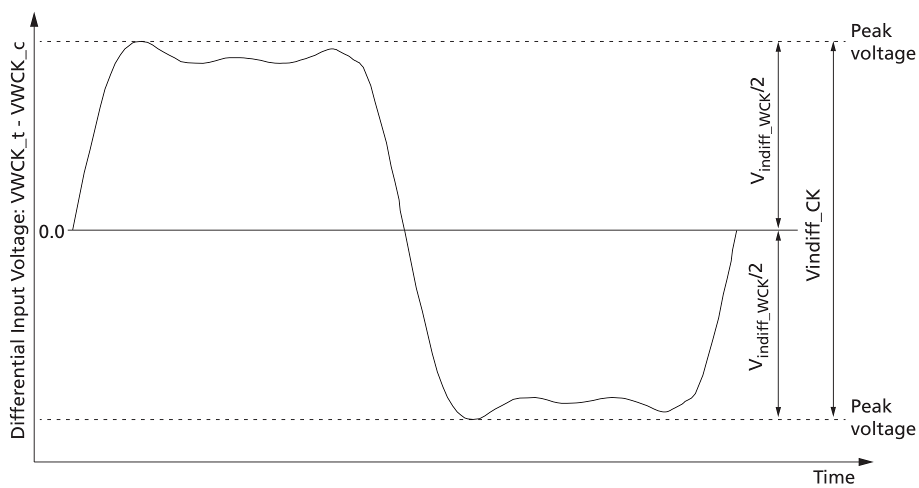


Table 35: WCK Differential Input Voltage

Parameter	Symbol	WCK Frequency (MHz)																Unit	Note
		800		1066		1600		2133		2750		3200		3750		4266.5			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WCK differential input voltage	$V_{indif-f\_WCK}$	300	–	300	–	300	–	280	–	280	–	280	–	280	–	280	–	mV	1, 2

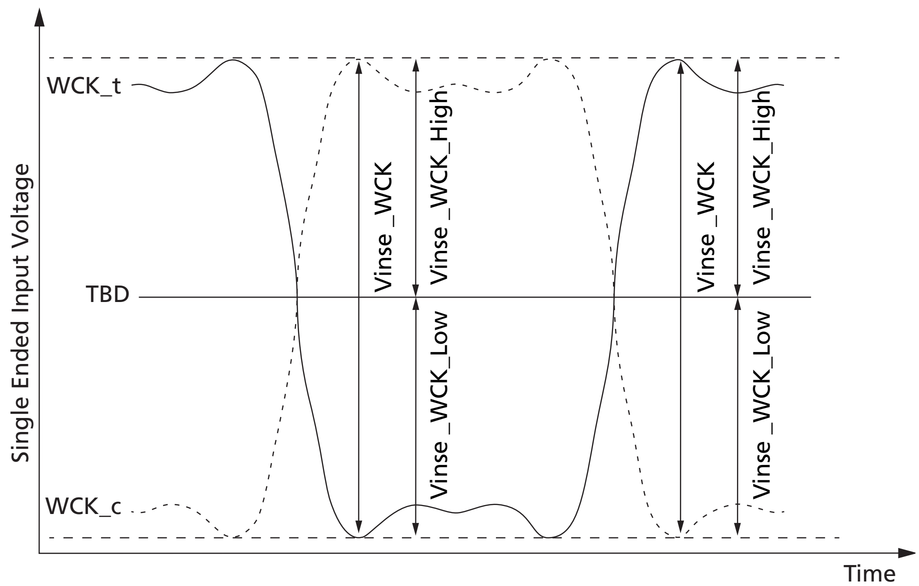
Notes: 1. Refer to the latency table to match the WCK frequency to the data rate.
2. The peak voltage of differential WCK signals is calculated in the following equation.
V_{indiff_WCK} = (Max peak voltage) - (Min peak voltage)

Max peak voltage = Max(f(t))
Min peak voltage = Min(f(t))
f(t) = V_{WCK_t} - V_{WCK_c}

Single-Ended Input Voltage for WCK

The minimum input voltage needed to satisfy both the Vinse_WCK, Vinse_WCK_High/Low specification at the input receiver.

Figure 15: WCK Single-Ended Input Voltage



Note: 1. TBD is the LPDDR5 SDRAM internal setting value by V_{REF} training.

Table 36: WCK Single-Ended Input Voltage

Parameter	Symbol	WCK Rate (MHz)																Unit	Note
		800		1066		1600		2133		2750		3200		3750		4266.5			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WCK single-ended input voltage	Vinse_WCK	150	–	150	–	150	–	140	–	140	–	140	–	140	–	140	–	mV	
WCK single-ended input voltage HIGH from TBD	Vinse_WCK_HIGH	75	–	75	–	75	–	75	–	75	–	75	–	75	–	75	–		
WCK single-ended input voltage LOW from TBD	Vinse_WCK_LOW	75	–	75	–	75	–	75	–	75	–	75	–	75	–	75	–		

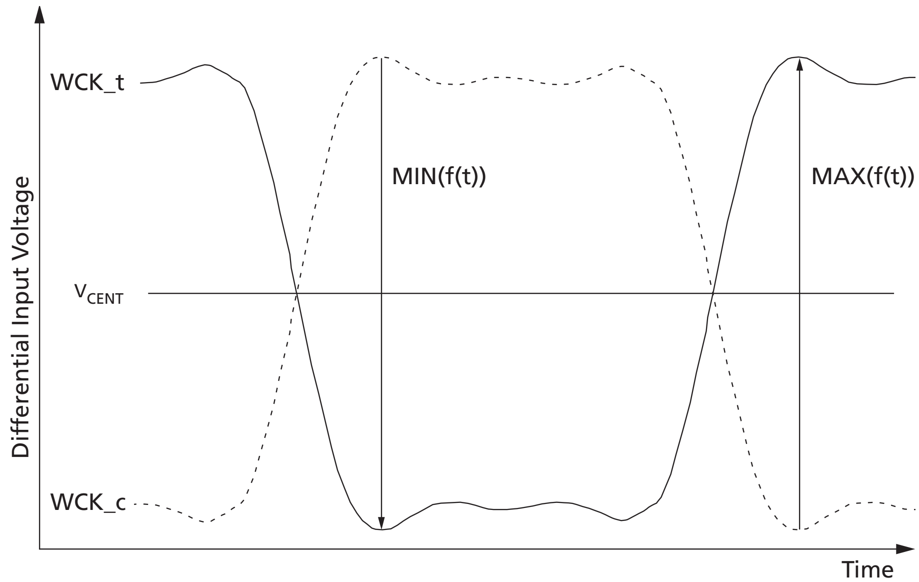
Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in the following equation.

- $V_{IH.DIFF.peak}$ voltage = Max(f(t))

- $V_{IL.DIFF.peak}$ voltage = Min(f(t))
- f(t) = V_{WCK_t} - V_{WCK_c}

Figure 16: Definition of Differential WCK Clock Peak Voltage

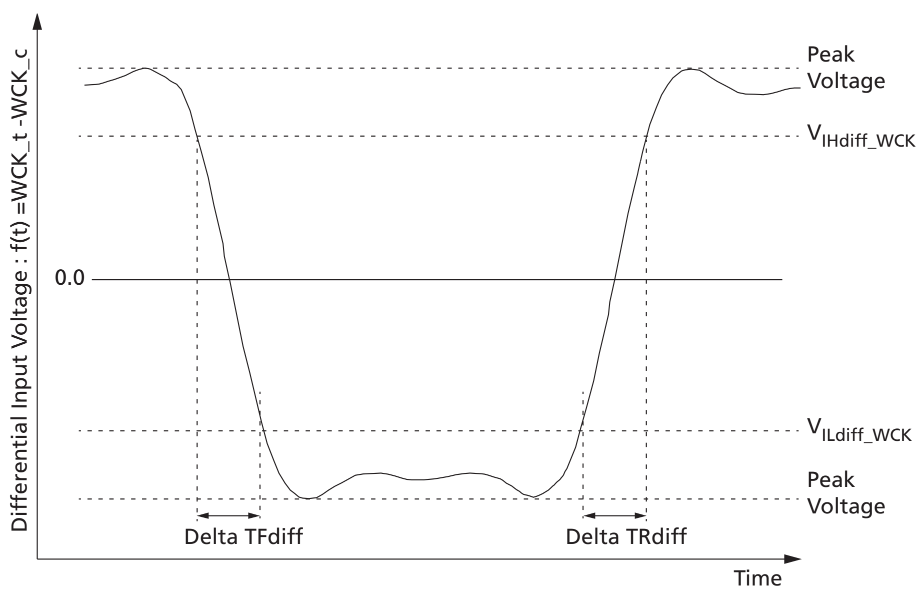


Note: 1. V_{cent} is the LPDDR5 SDRAM internal setting value determined by V_{REF} training.

Differential Input Slew Rate Definition for WCK

Input slew rates for differential signals (WCK_t, WCK_c) are defined and measured as shown in the following figure and tables.

Figure 17: Differential Input Slew Rate Definition for WCK_t, WCK_c



Notes: 1. The differential signal rising edge slope from V_{ILdiff_WCK} to V_{IHdiff_WCK} must be monotonic.
2. The differential signal falling edge slope from V_{IHdiff_WCK} to V_{ILdiff_WCK} must be monotonic.

Table 37: Differential Input Slew Rate Definition for WCK_t, WCK_c

Parameter	From	To	Defined by
Differential input slew rate for rising edge (WCK_t-WCK_c)	V_{ILdiff_WCK}	V_{IHdiff_WCK}	$\lvert V_{ILdiff\_WCK} - V_{IHdiff\_WCK} \rvert / \Delta TRdiff$
Differential input slew rate for falling edge (WCK_t-WCK_c)	V_{IHdiff_WCK}	V_{ILdiff_WCK}	$\lvert V_{ILdiff\_WCK} - V_{IHdiff\_WCK} \rvert / \Delta TFdiff$

Table 38: Differential Input Level for WCK_t, WCK_c

Parameter	Symbol	WCK Rate (MHz)																Unit
		800		1066		1600		2133		2750		3200		3750		4266.5		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential input HIGH	V_{IHdiff_WCK}	120	–	120	–	120	–	100	–	100	–	100	–	100	–	100	–	mV
Differential input LOW	V_{ILdiff_WCK}	–	120	–	120	–	120	–	100	–	100	–	100	–	100	–	100	

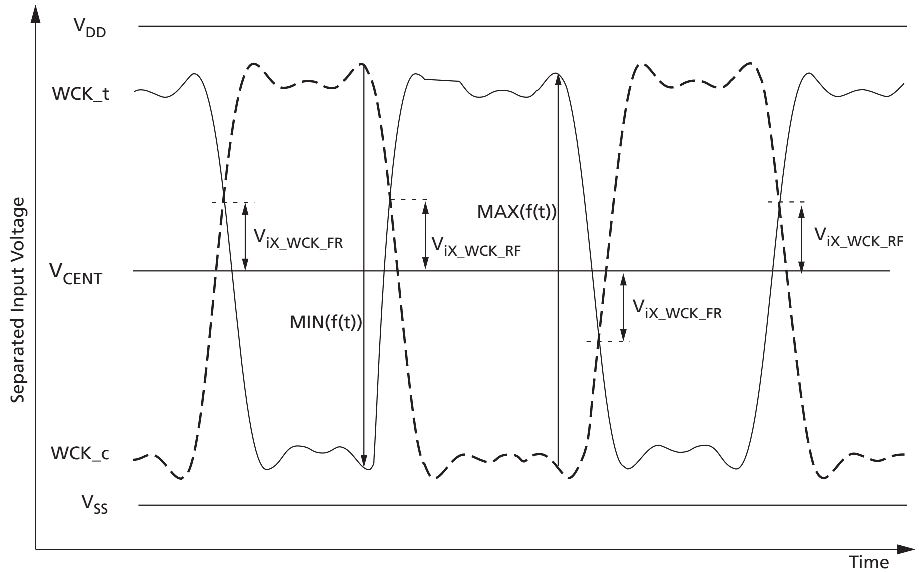
Table 39: Differential Input Slew Rate for WCK_t, WCK_c

Parameter	Symbol	WCK Rate (MHz)																Unit
		800		1066		1600		2133		2750		3200		3750		4266.5		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential input slew rate for WCK	SRIdiff_WCK	2	14	2	14	2	14	2	14	2	14	2	14	3	14	3	14	V/ns

Differential Input Cross Point Voltage for WCK

The cross point voltage of differential input signals (WCK_t, WCK_c) must meet the requirements shown in the following table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complementary signals to the mid level that is TBD.

Figure 18: V_{IX} Definition for WCK_t, WCK_c



Note: 1. The base level of $V_{IX\_WCK\_FR}/V_{IX\_WCK\_RF}$ is V_{CENT}.

Table 40: Cross Point Voltage for Differential Input Signals (WCK_t, WCK_c)

Parameter	Symbol	WCK Frequency (MHz)																Unit	Note
		800		1066		1600		2133		2750		3200		3750		4266.5			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WCK differential input cross point voltage ratio	$V_{IX_WCK_}$ratio	–	20	–	20	–	20	–	20	–	20	–	20	–	20	–	20	%	1, 2

Notes: 1. $V_{IX_WCK_}$ratio is defined by this equation: $V_{IX_WCK_}$ratio = $V_{IX\_WCK\_FR}/|Min(f(t))|$
2. $V_{IX_WCK_}$ratio is defined by this equation: $V_{IX_WCK_}$ratio = $V_{IX\_WCK\_RF}/Max(f(t))$

Single Ended Mode Input Voltage

Single-Ended CK Input Definitions

The minimum input voltage needs to satisfy both $V_{inse\_CK\_SE\_High}$ and $V_{inse\_CK\_SE\_Low}$ specification at the input receiver and their measurement period is 1^{t}CK. $V_{inse\_CK\_SE}$ is the peak to peak voltage centered on $V_{DDQ}/2$ and $V_{inse\_CK\_SE\_High}$ and $V_{inse\_CK\_SE\_Low}$ is maximum and minimum peak voltage from $V_{DDQ}/2$.

The minimum input voltage needs to satisfy both V_{inse_CK}, $V_{inse\_CK\_High}/V_{inse\_CK\_Low}$ specifications at input receiver.

Figure 19: Single-Ended CK Input Voltage

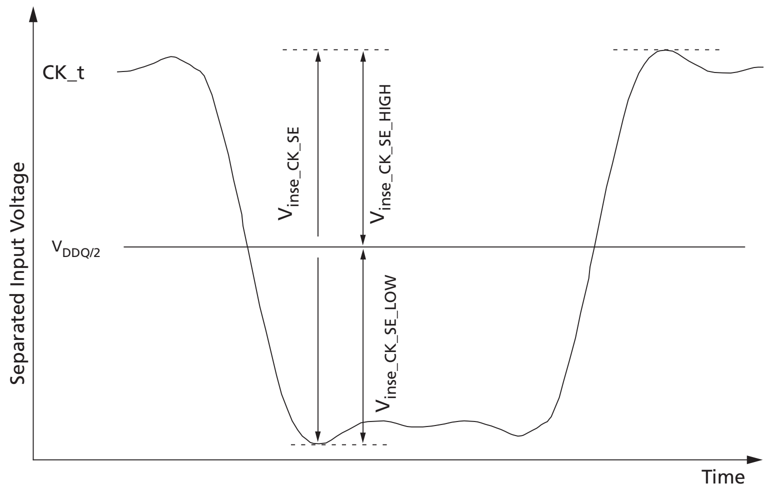
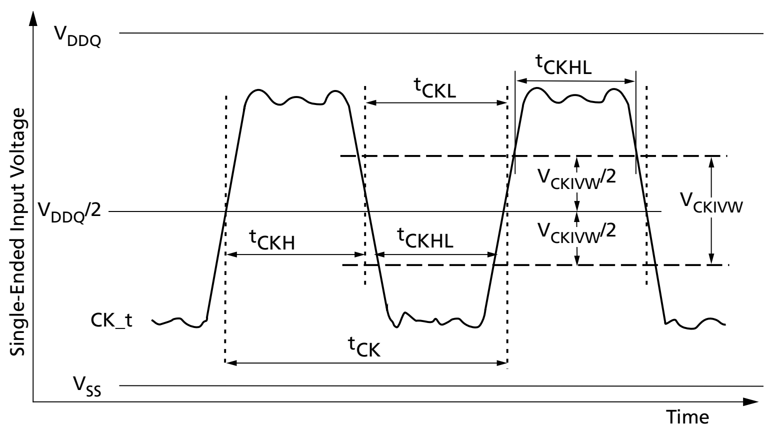


Figure 20: Single-Ended CK Pulse



Note: 1. Single-ended mode CK pulse definitions are defined shown below.

Table 41: Clock Single-Ended Input Parameters

Parameter	Symbol	CK Rate 400 MHz Min	CK Rate 400 MHz Max	Unit	Note
CK single-ended input voltage	$V_{inse\_CK\_SE}$	220	–	mV	
CK single-ended input voltage HIGH	$V_{inse\_CK\_SE\_High}$	110	–	mV	
CK single-ended input voltage LOW	$V_{inse\_CK\_SE\_Low}$	110	–	mV	
CK single-ended timing window	V_{CKIVW}	190	–	mV	
Clock single-ended CK pulse	$^{t}CKHL$	0.26	–	$^{t}CK(avg)$	
CK single-ended slew rate	SRICKSE	1	7	V/ns	1

Note: 1. Single-ended slew rate is measured at $V_{DDQ}/2 - V_{CKIVW}/2$ and $V_{DDQ}/2 + V_{CKIVW}/2$.

Single-Ended Input Voltage for WCK

The minimum input voltage needed to satisfy both the $V_{inse\_WCK\_SE\_High}$ and $V_{inse\_WCK\_SE\_Low}$ specifications at the input receiver measurement period is 1^tWCK. $V_{inse\_WCK\_SE}$ is the peak to peak voltage centered on $V_{DDQ}/2$ and $V_{inse\_WCK\_SE\_High}$ and $V_{inse\_WCK\_SE\_Low}$ max and min peak voltage are referenced to $V_{DDQ}/2$.

Figure 21: Single-Ended WCK Input Voltage

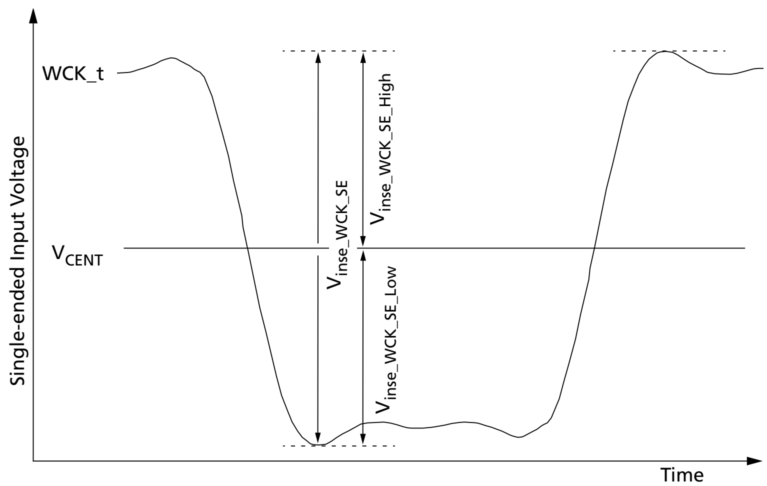


Figure 22: Single-Ended Mode WCK Pulse

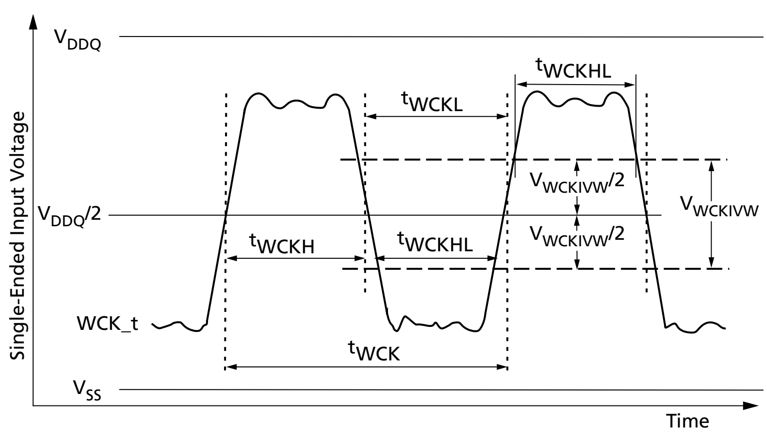


Table 42: WCK Clock Single-Ended Input Parameters

Parameter	Symbol	WCK Frequency 800 MHz Min	WCK Frequency 800 MHz Max	Unit	Note
WCK single-ended input voltage	$V_{inse\_WCK\_SE}$	220	–	mV	
WCK single-ended input HIGH voltage	$V_{inse\_WCK\_SE\_High}$	110	–	mV	
WCK single-ended input LOW voltage	$V_{inse\_WCK\_SE\_Low}$	110	–	mV	
WCK single-ended timing window	V_{WCKIVW}	180	–	mV	

Table 42: WCK Clock Single-Ended Input Parameters (Continued)

Parameter	Symbol	WCK Frequency 800 MHz Min	WCK Frequency 800 MHz Max	Unit	Note
Clock single-ended WCK pulse	^tWCKHL	0.23	–	$^tWCK(avg)$	1
WCK single-ended slew rate	SRIWCKSE	1	7	V/ns	

Note: 1. Single-ended slew rate is measured at $V_{DDQ}/2$ - $V_{WCKIVW}/2$ and $V_{DDQ}/2$ + $V_{WCKIVW}/2$.

Operating Temperature Range

Table 43: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit	Note
Standard	$T_{OPER\_standard}$	–25	85	°C	1, 2, 3
Elevated	$T_{OPER\_elevated}$	–25	105		

Notes: 1. The operating temperature is the case surface temperature on the center-top side of the device. For the measurement conditions, refer to JESD51-2A.
2. Some applications require operation of the device in the maximum temperature conditions within the elevated temperature range between a 85°C and 105°C case temperature. For the devices, derating may be necessary to operate in this range.
3. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determining the need for AC timing de-rating and/or monitoring the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the standard or elevated temperature ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

Table 44: Automotive Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit	Note
Standard	$T_{OPER\_standard}$	–25	85	°C	1
Automotive Grade 1	$T_{OPER\_auto\_grade1}$	–40	125		1, 2, 3, 4
Automotive Grade 2	$T_{OPER\_auto\_grade2}$	–40	105		
Automotive Grade 3	$T_{OPER\_auto\_grade3}$	–40	85		1, 3, 4

Notes: 1. Operating temperature is the case surface temperature on the center-top side of the device. For the measurement conditions, refer to JESD51-2A.
2. Automotive applications require operation of the device within the maximum temperature conditions over 85°C. For the devices, derating may be necessary to operate in this range (over 85°C).
3. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determining the need for AC timing de-rating and/or monitoring the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the standard or automotive temperature grades. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.
4. Automotive temperature conditions are only allowed for parts which specify the automotive temperature range guarantee in the data sheet.

AC Timings

Core AC Timings for LPDDR5

The two basic core AC timing tables and derived core AC timing tables are included in this section. The SDRAM status for one basic core AC timing table (x16 Mode/BG Mode) is x16, DVFSC is disabled, and write link ECC is disabled. The SDRAM status for the other basic core AC timing table (x16 Mode/16B Mode) is x16, DVFSC is enabled, and write link ECC is disabled. When the byte mode (x8) and/or write link ECC are enabled, ^{t}WR and ^{t}WTR values change and are described in the derivation tables.

Core AC Timings for DVFSC Disabled and Write Link ECC Disabled

Table 45: x16 Mode/BG Mode

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit
			67	133	200	266	344	400	467	533	600	688	750	800	
ACTIVATE-to-ACTIVATE command period (same bank)	^{t}RC	Min	^{t}RAS + ^{t}RPab with all-bank PRECHARGE ^{t}RAS + ^{t}RPpb with per-bank PRECHARGE												
RAS-to-CAS delay	^{t}RCD	Min	MAX(18ns, 2*n*CK)												
Row precharge time (all banks)	^{t}RPab	Min	MAX(21ns, 2*n*CK)												
Row precharge time (single bank)	^{t}RPpb	Min	MAX(18ns, 2*n*CK)												
Row active time	^{t}RAS	Min	MAX(42ns, 3*n*CK)												
		Max	MIN(9 × ^{t}REFI × refresh rate, 70.2)												µs
WRITE recovery time	^{t}WR	Min	MAX(34ns, 3*n*CK)												
Active bank-A to active bank-B	^{t}RRD	Min	MAX(5ns, 2*n*CK)												
Four-bank ACTIVATE window	^{t}FAW	Min	20												ns
READ burst end to PRECHARGE command delay	^{t}RBTP	Min	CKR = 2:1, MAX(7.5ns, 4*n*CK) - 4*n*CK												
		Min	CKR = 4:1, MAX(7.5ns, 2*n*CK) - 2*n*CK												
WRITE-to-READ delay	^{t}WTR_S	Min	MAX(6.25ns, 4*n*CK)												
	^{t}WTR_L	Min	MAX(12ns, 4*n*CK)												
PRECHARGE to PRECHARGE Delay	^{t}PPD	Min	2												*n*CK

Notes: 1. Clock frequency of BG mode supports is more than 400 MHz.
2. Values equal or less than 400 MHz are for reference for other tables.

Table 46: x16 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
WRITE-to-READ delay	^{t}WTR	Min	MAX(12ns, 4*n*CK)	

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 47: x16 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
Active bank-A to active bank-B	^{t}RRD	Min	MAX(10ns, 2*n*CK)	–
Four-bank ACTIVATE window	^{t}FAW	Min	40	ns
WRITE-to-READ delay	^{t}WTR	Min	MAX(12ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 48: x8 Mode/BG Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)	–
WRITE-to-READ delay	$^{t}WTR\_S$	Min	MAX(8.25ns, 4*n*CK)	–
	$^{t}WTR\_L$	Min	MAX(14ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 49: x8 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)	–
WRITE-to-READ delay	^{t}WTR	Min	MAX(14ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 50: x8 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
Active bank-A to active bank-B	^{t}RRD	Min	MAX(10ns, 2*n*CK)	–
Four-bank ACTIVATE window	^{t}FAW	Min	40	ns
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)	–
WRITE-to-READ delay	^{t}WTR	Min	MAX(14ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Core AC Timing for DVFSC Disabled and Write Link ECC Enabled

Table 51: x16 Mode/BG Mode

Item	Symbol	Min/Max	Data Rate (Mb/s) All Operating Points	Unit
WRITE recovery time	^tWR	Min	MAX(38ns, 3*n*CK)	–
WRITE-to-READ delay	^tWR_S	Min	MAX(10.25ns, 4*n*CK)	–
	$^tWTR\_L$	Min	MAX(16ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 52: x16 Mode/8B Mode

Item	Symbol	Min/Max	Data Rate (Mb/s) All Operating Points	Unit
Active bank-A to active bank-B	^tRRD	Min	MAX(10ns, 2*n*CK)	–
Four-bank ACTIVATE window	^tFAW	Min	40	ns
WRITE recovery time	^tWR	Min	MAX(38ns, 3*n*CK)	–
WRITE-to-READ delay	^tWTR	Min	MAX(16ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 53: x8 Mode/BG Mode

Item	Symbol	Min/Max	Data Rate (Mb/s) All Operating Points	Unit
WRITE recovery time	^tWR	Min	MAX(40ns, 3*n*CK)	–
WRITE-to-READ delay	$^tWTR\_S$	Min	MAX(12.25ns, 4*n*CK)	–
	$^tWTR\_L$	Min	MAX(18ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Table 54: x8 Mode/8B Mode

Item	Symbol	Min/Max	Data Rate (Mb/s) All Operating Points	Unit
Active bank-A to active bank-B	^tRRD	Min	MAX(10ns, 2*n*CK)	–
Four-bank ACTIVATE window	^tFAW	Min	40	ns
WRITE recovery time	^tWR	Min	MAX(40ns, 3*n*CK)	–
WRITE-to-READ delay	^tWTR	Min	MAX(18ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 Mode/BG Mode.

Core AC Timing for DVFSC Enabled and Write Link ECC Disabled

Table 55: x16 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
ACTIVATE-to-ACTIVATE command period (same bank)	^{t}RC	Min	^{t}RAS + ^{t}RPab with all-bank PRECHARGE ^{t}RAS + ^{t}RPpb with per-bank PRECHARGE						–
RAS-to-CAS delay	^{t}RCD	Min	MAX(19ns, 2*n*CK)						–
Row precharge time (all banks)	^{t}RPab	Min	MAX(21ns, 2*n*CK)						–
Row precharge time (single bank)	^{t}RPpb	Min	MAX(18ns, 2*n*CK)						–
Row active time	^{t}RAS	Min	MAX(42ns, 3*n*CK)						–
		Max	MIN(9 × ^{t}REFI × refresh rate, 70.2)						µs
WRITE recovery time	^{t}WR	Min	MAX(41ns, 3*n*CK)						–
Active bank-A to active bank-B	^{t}RRD	Min	MAX(5ns, 2*n*CK)						–
Four-bank ACTIVATE window	^{t}FAW	Min	20						ns
READ burst end to PRECHARGE command delay	^{t}RBTP	Min	CKR = 2:1, MAX(8.5ns, 4*n*CK) - 4*n*CK						–
		Min	CKR = 4:1, MAX(8.5ns, 2*n*CK) - 2*n*CK						–
WRITE-to-READ delay	^{t}WTR	Min	MAX(19ns, 4*n*CK)						–
PRECHARGE to PRECHARGE Delay	^{t}PPD	Min	2						*n*CK

Note: 1. The range of application for this table is up to 1600 Mb/s.

Table 56: x16 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
Active bank-A to active bank-B	^{t}RRD	Min	MAX(10ns, 2*n*CK)						–
Four-bank ACTIVATE window	^{t}FAW	Min	40						ns

Notes: 1. The rest of the core AC timing values are the same as x16 Mode/16B Mode.
2. The range of application for this table is up to 1600 Mb/s.

Table 57: x8 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
WRITE recovery time	^{t}WR	Min	MAX(43ns, 3*n*CK)						–
WRITE-to-READ delay	^{t}WTR	Min	MAX(21ns, 4*n*CK)						–

Notes: 1. The rest of the core AC timing values are the same as x16 Mode/16B Mode.
2. The range of application for this table is up to 1600 Mb/s.

Table 58: x8 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
Active bank-A to active bank-B	^tRRD	Min	MAX(10ns, 2*n*CK)						–
Four-bank ACTIVATE window	^tFAW	Min	40						ns
WRITE recovery time	^tWR	Min	MAX(43ns, 3*n*CK)						–
WRITE-to-READ delay	^tWTR	Min	MAX(21ns, 4*n*CK)						–

Notes: 1. The rest of the core AC timing values are the same as x16 Mode/16B Mode.
2. The range of application for this table is up to 1600 Mb/s.

Core AC Timings for LPDDR5X

The following Core AC parameters applies only to LPDDR5X SDRAM (MR8 OP[1:0]=01b).

Core AC Timings for DVFSC Disabled, Enhanced DVFSC Disabled, and Write Link ECC Disabled

Table 59: x16 Mode/BG Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit	Note
ACTIVATE-to-ACTIVATE command period (same bank)	^tRC	Min	^tRAS + ^tRPab with all-bank PRECHARGE ^tRAS + ^tRPpb with per-bank PRECHARGE		
RAS-to-CAS delay	^tRCD	Min	MAX(8ns, 2*n*CK)		1
			MAX(18ns, 2*n*CK)		2
Row precharge time (all banks)	^tRPab	Min	MAX(21ns, 2*n*CK)		
Row precharge time (single bank)	^tRPpb	Min	MAX(18ns, 2*n*CK)		
Row active time	^tRAS	Min	MAX(42ns, 3*n*CK)		
		Max	MIN(9 × ^tREFI × refresh rate, 70.2)	µs	
WRITE recovery time	^tWR	Min	MAX(34ns, 3*n*CK)		
Active bank-A to active bank-B	^tRRD	Min	MAX(3.75ns, 2*n*CK)		
Four-bank ACTIVATE window	^tFAW	Min	15	ns	
READ burst end to PRE-CHARGE command delay	^tRBTP	Min	CKR = 2:1, MAX(7.5ns, 4*n*CK) - 4*n*CK		
		Min	CKR = 4:1, MAX(7.5ns, 2*n*CK) - 2*n*CK		
WRITE-to-READ delay	$^tWTR\_S$	Min	MAX(6.25ns, 4*n*CK)		
	$^tWTR\_L$	Min	MAX(12ns, 4*n*CK)		
PRECHARGE to PRE-CHARGE Delay	^tPPD	Min	2	*n*CK	

Notes: 1. MAX(8ns, 2nCK) applies from ACT-2 command to WRITE command.
2. MAX(18ns, 2nCK) applies from ACT-2 command to READ and MASKED WRITE command and also to other instances in which ^{t}RCD is used to describe a timing constraint.
3. Clock frequency of BG mode support is more than 400 MHz.
4. Values equal or less than 400 MHz are for reference for other tables.

Table 60: x16 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) equal to or less than 800 MHz	Unit
WRITE-to-READ delay	^{t}WTR	Min	MAX(12ns, 4*n*CK)	

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode.

Table 61: x16 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
Active bank-A to active bank-B	^{t}RRD	Min	MAX(7.5ns, 2*n*CK)	–
Four-bank ACTIVATE window	^{t}FAW	Min	30	ns
WRITE-to-READ delay	^{t}WTR	Min	MAX(12ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode.

Table 62: x8 Mode/BG Mode

Item	Symbol	Min/Max	CK Frequency (MHz)							Unit
			467	533	600	688	750	800	1066	
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)							–
WRITE-to-READ delay	^{t}WTR_S	Min	MAX(8.25ns, 4*n*CK)							–
	^{t}WTR_L	Min	MAX(14ns, 4*n*CK)							–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode.

Table 63: x8 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) equal to or less than 800 MHz	Unit
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)	–
WRITE-to-READ delay	^{t}WTR	Min	MAX(14ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode.

Table 64: x8 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
Active bank-A to active bank-B	^{t}RRD	Min	MAX(7.5ns, 2*n*CK)	–
Four-bank ACTIVATE window	^{t}FAW	Min	30	ns
WRITE recovery time	^{t}WR	Min	MAX(36ns, 3*n*CK)	–

Table 64: x8 Mode/8B Mode (Continued)

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
WRITE-to-READ delay	^{t}WTR	Min	MAX(14ns, 4*n*CK)	–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode.

Core AC Timing for DVFSC Disabled, Enhanced DVFSC Disabled, and Write Link ECC Enabled

Table 65: x16 Mode/BG Mode

Item	Symbol	Min/Max	Data Rate (Mb/s)								Unit
			467	533	600	688	750	800	937	1066	
WRITE recovery time	^{t}WR	Min	MAX(38ns, 3*n*CK)								–
WRITE-to-READ delay	^{t}WTR_S	Min	MAX(10.25ns, 4*n*CK)								–
	^{t}WTR_L	Min	MAX(16ns, 4*n*CK)								–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode for DVFSC Disabled, Enhanced DVFSC Disabled, Write Link ECC Disabled.

Table 66: x16 Mode/8B Mode

Item	Symbol	Min/Max	Data Rate (Mb/s)								Unit
			467	533	600	688	750	800	937	1066	
Active bank-A to active bank-B	^{t}RRD	Min	MAX(7.5ns, 2*n*CK)								–
Four-bank ACTIVATE window	^{t}FAW	Min	30								ns
WRITE recovery time	^{t}WR	Min	MAX(38ns, 3*n*CK)								–
WRITE-to-READ delay	^{t}WTR	Min	MAX(16ns, 4*n*CK)								–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode for DVFSC Disabled, Enhanced DVFSC Disabled, Write Link ECC Disabled.

Table 67: x8 Mode/BG Mode

Item	Symbol	Min/Max	Data Rate (Mb/s)								Unit
			467	533	600	688	750	800	937	1066	
WRITE recovery time	^{t}WR	Min	MAX(40ns, 3*n*CK)								–
WRITE-to-READ delay	^{t}WTR_S	Min	MAX(12.25ns, 4*n*CK)								–
	^{t}WTR_L	Min	MAX(18ns, 4*n*CK)								–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode for DVFSC Disabled, Enhanced DVFSC Disabled, Write Link ECC Disabled.

Table 68: x8 Mode/8B Mode

Item	Symbol	Min/Max	Data Rate (Mb/s)								Unit
			467	533	600	688	750	800	937	1066	
Active bank-A to active bank-B	^{t}RRD	Min	MAX(7.5ns, 2*n*CK)								–
Four-bank ACTI-VATE window	^{t}FAW	Min	30								ns
WRITE recovery time	^{t}WR	Min	MAX(40ns, 3*n*CK)								–
WRITE-to-READ delay	^{t}WTR	Min	MAX(18ns, 4*n*CK)								–

Note: 1. The rest of the core AC timing values are the same as x16 mode/BG mode for DVFSC Disabled, Enhanced DVFSC Disabled, Write Link ECC Disabled.

Core AC Timing for DVFSC Enabled, Enhanced DVFSC Disabled, and Write Link ECC Disabled

Table 69: x16 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit	Note
			67	133	200	266	344	400		
ACTIVATE-to-ACTIVATE command period (same bank)	^{t}RC	Min	^{t}RAS + ^{t}RPab with all-bank PRECHARGE ^{t}RAS + ^{t}RPpb with per-bank PRECHARGE						–	
RAS-to-CAS delay	^{t}RCD	Min	MAX(9ns, 2*n*CK)						–	1
			MAX(19ns, 2*n*CK)							2
Row precharge time (all banks)	^{t}RPab	Min	MAX(21ns, 2*n*CK)						–	
Row precharge time (single bank)	^{t}RPpb	Min	MAX(18ns, 2*n*CK)						–	
Row active time	^{t}RAS	Min	MAX(42ns, 3*n*CK)						–	
		Max	MIN(9 × ^{t}REFI × refresh rate, 70.2)						µs	
WRITE recovery time	^{t}WR	Min	MAX(41ns, 3*n*CK)						–	
Active bank-A to active bank-B	^{t}RRD	Min	MAX(3.75ns, 2*n*CK)						–	
Four-bank ACTIVATE window	^{t}FAW	Min	15						ns	
READ burst end to PRECHARGE command delay	^{t}RBTP	Min	CKR = 2:1, MAX(8.5ns, 4*n*CK) - 4*n*CK						–	
		Min	CKR = 4:1, MAX(8.5ns, 2*n*CK) - 2*n*CK						–	
WRITE-to-READ delay	^{t}WTR	Min	MAX(19ns, 4*n*CK)						–	
PRECHARGE to PRECHARGE Delay	^{t}PPD	Min	2						*n*CK	

Notes: 1. MAX(9ns, 2nCK) applies from ACT-2 command to WRITE command.
2. MAX(19ns, 2nCK) applies from ACT-2 command to READ and MASKED WRITE command and also to other instances in which ^{t}RCD is used to describe a timing constraint.
3. The range of application for this table is up to 1600 Mb/s.

Table 70: x16 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
Active bank-A to active bank-B	^tRRD	Min	MAX(7.5ns, 2*n*CK)						–
Four-bank ACTIVATE window	^tFAW	Min	30						ns

Note: 1. The rest of the core AC timing values are the same as x16 mode/16B mode.

Table 71: x8 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
WRITE recovery time	^tWR	Min	MAX(43ns, 3*n*CK)						–
WRITE-to-READ delay	^tWTR	Min	MAX(21ns, 4*n*CK)						–

Notes: 1. The rest of the core AC timing values are the same as x16 mode/16B mode.
2. The range of application for this table is up to 1600 Mb/s.

Table 72: x8 Mode/8B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
Active bank-A to active bank-B	^tRRD	Min	MAX(7.5ns, 2*n*CK)						–
Four-bank ACTIVATE window	^tFAW	Min	30						ns
WRITE recovery time	^tWR	Min	MAX(43ns, 3*n*CK)						–
WRITE-to-READ delay	^tWTR	Min	MAX(21ns, 4*n*CK)						–

Note: 1. The rest of the core AC timing values are the same as x16 mode/16B mode.

Core AC Timing for DVFSC Disabled, Enhanced DVFSC Enabled, and Write Link ECC Disabled

Table 73: x16 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit	Note
			67	133	200	266	344	400		
ACTIVATE-to-ACTIVATE command period (same bank)	^tRC	Min	^tRAS + ^tRPab with all-bank PRECHARGE ^tRAS + ^tRPpb with per-bank PRECHARGE						–	
RAS-to-CAS delay	^tRCD	Min	MAX(9ns, 2*n*CK)						–	1
			MAX(20ns, 2*n*CK)							2
Row precharge time (all banks)	^tRPab	Min	MAX(23ns, 2*n*CK)						–	
Row precharge time (single bank)	^tRPpb	Min	MAX(20ns, 2*n*CK)						–	

Table 73: x16 Mode/16B Mode (Continued)

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit	Note
			67	133	200	266	344	400		
Row active time	^tRAS	Min	MAX(42ns, 3nCK)						–	
		Max	MIN(9 × ^tREFI × refresh rate, 70.2)						µs	
WRITE recovery time	^tWR	Min	MAX(41ns, 3nCK)						–	
Active bank-A to active bank-B	^tRRD	Min	MAX(3.75ns, 2nCK)						–	
Four-bank ACTIVATE window	^tFAW	Min	15						ns	
READ burst end to PRECHARGE command delay	^tRBTP	Min	CKR = 2:1, MAX(8.5ns, 4nCK) - 4nCK						–	
		Min	CKR = 4:1, MAX(8.5ns, 2nCK) - 2nCK						–	
WRITE-to-READ delay	^tWTR	Min	MAX(19ns, 4nCK)						–	
PRECHARGE to PRECHARGE Delay	^tPPD	Min	2						nCK	

Notes: 1. MAX(9ns, 2nCK) applies from ACT-2 command to WRITE command.
2. MAX(20ns, 2nCK) applies from ACT-2 command to READ and MASKED WRITE command and also to other instances in which ^tRCD is used to describe a timing constraint.
3. The range of application for this table is up to 3200 Mb/s.

Table 74: x8 Mode/16B Mode

Item	Symbol	Min/Max	CK Frequency (MHz)						Unit
			67	133	200	266	344	400	
WRITE recovery time	^tWR	Min	MAX(43ns, 3nCK)						–
WRITE-to-READ delay	^tWTR	Min	MAX(21ns, 4nCK)						–

Notes: 1. The rest of the core AC timing values are the same as x16 mode/16B mode.
2. The range of application for this table is up to 3200 Mb/s.

Temperature Derating AC Timing

Table 75: Temperature Derating AC Timing

Item	Symbol	Min/Max	CK Frequency (MHz) All Operating Points	Unit
DQ To WCK input offset	^{t}WCK2DQI_HF	Max	tWCK2DQI_HF + 15	ps
	^{t}WCK2DQI_LF	Max	tWCK2DQI_LF + 20	ps
WCK to DQ output offset	^{t}WCK2DQO_HF	Max	tWCK2DQO_HF + 35	ps
	^{t}WCK2DQO_LF	Max	tWCK2DQO_LF + 40	ps
ACTIVATE-to-ACTIVATE command period (same bank)	^{t}RC	Min	^{t}RC + 3.75	ns
RAS to CAS delay	^{t}RCD	Min	^{t}RCD + 1.875	ns
Row active time	^{t}RAS	Min	^{t}RAS + 1.875	ns
Row recharge time (all banks)	^{t}RPab	Min	^{t}RPab + 1.875	ns
Row recharge time (single bank)	^{t}RPpb	Min	^{t}RPpb + 1.875	ns

Notes: 1. Timing derating applies to operation from 85 °C (85 °C<) to 105 °C(≤105 °C).
2. Refer to product data sheet for products supporting temperatures greater than 105 °C.
3. The derated values are required only when MR4 OP[4:0] are 01101 or 01111.

Self Refresh, Power-Down, and Deep Sleep Related Timings

Table 76: Self Refresh AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Delay from SRE command to PDE	^{t}ESPD	Min	2	*n*CK	
Minimum self refresh time (ENTRY to EXIT)	^{t}SR	Min	MAX(15ns, 2*n*CK)	–	1
Exit self refresh to valid commands	^{t}XSR	Min	^{t}RFCab + MAX(7.5ns, 2*n*CK)	–	1

Notes: 1. Delay time has to satisfy both analog time (ns) and clock count (*n*CK). ^{t}ESPD will not expire until CK has toggled through at least 2 full cycles (2 × *n*CK) and 1.75ns has transpired.

Table 77: Power-Down AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Delay time from PDE and PDX	^{t}CSPD	Min	10ns + 1^{t}CK	ns	1, 2
Delay from valid command to PDE	^{t}CMDPD	Min	3	*n*CK	3
Valid clock requirement after PDE	^{t}CSLCK	Min	MAX(5ns, 3*n*CK)	ns	1
Valid clock requirement before PDX	^{t}CKCSH	Min	2	*n*CK	
Valid low requirement for CA before PDX	^{t}CACSH	Min	1.75	ns	
Exit power-down to next valid command delay	^{t}XP	Min	MAX(7ns, 3*n*CK)	ns	1

Table 77: Power-Down AC Timing (Continued)

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Minimum CS high pulse width at PDX	^{t}CSH	Min	3	ns	
Minimum CS low pulse duration at PDX	^{t}CSL	Min	4	ns	
Minimum CA low duration time at PDX	^{t}CSCAL	Min	1.75	ns	
Delay from MRW command to PDE	^{t}MRWPD	Min	MAX(14ns, 6*n*CK)	ns	1, 4
Delay from ZQCAL START command to PDE	^{t}ZQPD	Min	3	*n*CK	
Delay from MPC OSC Start/Stop Command to PDE	^{t}OSCPD	Min	MAX(40ns, 8*n*CK)	ns	

Notes: 1. Delay time has to satisfy both analog time (ns) and clock count (*n*CK). For example, ^{t}CSLCK will not expire until CK has toggled through at least three full cycles (3 × ^{t}CK) and 5ns has transpired.
2. ^{t}CK value is for the operating frequency at the time the PDE command is issued.
3. SRX command is included the valid command.
4. This MR change results in special delay time. See special timing in Mode Register Write to Power Down Entry figure for details. VREF(CA) setting: MR12 OP[6:0] V_{REF} Current Generator (V_{RCG}): MR16 OP[6]

Table 78: Deep-Sleep Mode AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Minimum interval between deep-sleep mode entry and exit	^{t}PDN	Min	10ns + 1^{t}CK	ns	1
Minimum deep-sleep mode duration time for DRAM compliance with I_{DDtbd} power specification	^{t}PDN_DSM	Min	4	ms	
Delay from deep-sleep mode exit to SRX	^{t}XSR_DSM	Min	200	µs	
Delay from deep-sleep mode exit to power-down exit	^{t}XDSM_XP	Min	190	µs	
Delay from PD/DSM entry to CS ODT off	^{t}PDECSODTOFF	Max	10ns + 1^{t}CK	ns	1
Delay from power-down exit to CS ODT on	^{t}PDXCSODTON	Max	20	ns	

Note: 1. 1^{t}CK for this timing is the ^{t}CK value of the operating frequency when the DSM ENTRY command is issued.

Mode Register, VRCG, and Frequency Set Point-Related Timings

Table 79: Mode Register Read/Write AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Additional time after ^{t}XP has expired until MRR command may be issued	^{t}MRRI	Min	^{t}RCD + 2*n*CK	ns	1
MODE REGISTER READ command period	^{t}MRR	Min	4 at CKR = 4:1 8 at CKR = 2:1	*n*CK	
MODE REGISTER WRITE command period	^{t}MRW	Min	MAX(10ns, 5*n*CK)	ns	
MODE REGISTER SET command delay	^{t}MRD	Min	MAX(14ns, 5*n*CK)	ns	

Table 79: Mode Register Read/Write AC Timing (Continued)

Parameter	Symbol	Min/Max	Value	Unit	Note
Stretched MODE REGISTER WRITE command period	^{t}MRW_L	Min	250 + 0.5 ^{t}CK	ns	
Stretched MODE REGISTER SET command delay	^{t}MRD_L	Min	250 + 0.5^{t}CK	ns	

Note: 1. In LPDDR5X, ^{t} RCD from ACT-2 to Read/Masked Write must be used

Table 80: VRCG Enable/Disable Timing

Parameter	Symbol	Min	Max	Unit
V_{REF} high-current mode enable time	^{t}VRCG_enable	–	150	ns
V_{REF} high-current mode disable time	^{t}VRCG_disable	–	100	ns

Table 81: V_{REFCA} Update Timing

Parameter	Symbol	Min/Max	All Operating Points	Unit	Note
$V_{REF(CA)}$ update timing	^{t}VREFCA_short	Min	200 + 0.5 ^{t}CK	ns	1, 2, 3, 4
	^{t}VREFCA_long	Min	200 + 0.5 ^{t}CK	ns	1, 2, 5
	^{t}VREFCA_weak	Min	1	ms	6

Notes: 1. $V_{REF(CA)}$ update timing depends on the value of the $V_{REF(CA)}$ setting: MR12 OP[6:0].
2. This value assumes that VRCG is set to high-current mode: MR16 OP[6] = 1b.
3. ^{t}CK for this timing is the ^{t}CK value of the operating frequency when the MRW is issued.
4. V_{REFCA_short} is for a single step-size increment/decrement change in $V_{REF(CA)}$ voltage.
5. V_{REFCA_long} is for at least two step-size increment/decrement changes including up to V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} changes in $V_{REF(CA)}$ voltage.
6. This value assumes that VRCG is set to normal operation: MR16 OP[6] = 0b.

Table 82: V_{REFDQ} Update Timing

Parameter	Symbol	Min/Max	All Operating Points	Unit	Note
$V_{REF(DQ)}$ update timing	^{t}VREFDQ_Short	Min	200 + 0.5 ^{t}CK	ns	1, 2, 3, 4
	^{t}VREFDQ_Long	Min	200+ 0.5 ^{t}CK	ns	1, 2, 5
	^{t}VREFDQ_Weak	Min	1	ms	6

Notes: 1. $V_{REF(DQ)}$ update timing depends on the value of the $V_{REF(DQ)}$ setting: MR14 OP[6:0] and MR15 OP[6:0].
2. This value assumes that VRCG is set to high-current mode: MR16 OP[6] = 1b.
3. ^{t}CK for this timing is the ^{t}CK value of the operating frequency when the MRW is issued.
4. V_{REFDQ_short} is for a single step-size increment/decrement change in $V_{REF(DQ)}$ voltage.
5. V_{REFDQ_long} is for at least two step-size increment/decrement changes including up to V_{REFmin} to V_{REFmax} or V_{REFmax} to V_{REFmin} change in $V_{REF(DQ)}$ voltage.

6. This value assumes that VRCG is set to normal operation: MR16 OP[6] = 0b.

Table 83: Frequency Set Point AC Timing Parameters

Parameter	Symbol	Min/Max	All Operating Points	Unit	Note
Frequency set point (FSP) switching time	^{t}FC_short	Min	200 + 0.5 ^{t}CK	ns	1, 2
	^{t}FC_long	Min	250 + 0.5 ^{t}CK		
Valid clock requirement after entering FSP change	^{t}CKFSPE	Min	MAX(7.5ns, 4*n*CK)	–	
Valid clock requirement before first valid command after FSP change	^{t}CKFSPX	Min	MAX(7.5ns, 4*n*CK)	–	

Notes: 1. FSP switching time depends on the value of the $V_{REF(CA)}$ setting: MR12 OP[6:0] of FSP-OP 0, 1, and 2. The details are shown in the following table. Any FSP change may affect the $V_{REF(DQ)}$ setting. The settling time of the $V_{REF(DQ)}$ level is the same as the $V_{REF(CA)}$ level.

2. ^{t}CK for this timing is the ^{t}CK value of the operating frequency when MRW is issued.

WCK-Related Timings

Table 84: ^{t}WCK2DQ AC Timing Parameters for E-DVFSC

Parameter	Symbol	Data Rate ≤6400 Mb/s Min/Max	Data Rate ≤6400 Mb/s Value	Data Rate >6400 Mb/s Min/Max	Data Rate >6400 Mb/s Value	Unit	Note
WCK to DQ offset (write)	^{t}WCK2DQI_HF	Min	300	Min	250	ps	
		Max	700	Max	600		
	^{t}WCK2DQI_LF	Min	300	Min	300	ps	
		Max	900	Max	900		
WCK to DQ Rx offset temperature variation (write)	^{t}WCK2DQI_temp_HF	Max	0.6	Max	0.5	ps/°C	
	^{t}WCK2DQI_temp_LF	Max	0.7	Max	0.7		
WCK to DQ Rx offset voltage variation (write)	^{t}WCK2DQI_volt_HF	Max	25	Max	25	ps/50mV	
	^{t}WCK2DQI_volt_LF	Max	50	Max	50		
	^{t}WCK2DQI_volt _HF_L	Max	50	Max	N/A		4
WCK to DQ offset (read)	^{t}WCK2DQO_HF	Min	650	Min	650	ps	
		Max	1600	Max	1600		
	^{t}WCK2DQO_LF	Min	650	Min	650	ps	
		Max	1900	Max	1900		
WCK to DQ offset temperature variation (read)	^{t}WCK2DQO_temp_HF	Max	1.5	Max	1.4	ps/°C	
	^{t}WCK2DQO_temp_LF	Max	1.8	Max	1.8		
WCK to DQ offset voltage variation (read)	^{t}WCK2DQO_volt_HF	Max	3.0	Max	2.5	ps/mV	
	^{t}WCK2DQO_volt_LF	Max	5.0	Max	5.0		
	^{t}WCK2DQO_volt_HF_L	Max	5.0	Max	N/A		4

Notes: 1. _HF means high frequency and _LF means low frequency.
2. _LF is used for 3200 Mb/s and below (≤3200 Mb/s). _HF is used for 3200 Mb/s and above(≥3200 Mb/s).
3. WCK2DQ AC parameters (HF/LF) can be selectable by MR18 OP[3]. Refer to MR18.
4. This parameter value is applied when MR18 OP[3] and MR19 OP[1:0] set as follows at the same time. - WCK Frequency Mode = High frequency mode: MR18 OP[3]=1b. - Enhanced DVFSC mode is enabled: MR19 OP[1:0]=10b.

Table 85: ^{t}WCK2DQ AC Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit	Note
DQ to WCK offset (write)	^{t}WCK2DQI_HF	Min	300	ps	1, 2, 3
		Max	700		
	^{t}WCK2DQI_LF	Min	300	ps	1, 2, 3
		Max	900		
DQ to WCK Rx offset temperature variation (write)	^{t}WCK2DQI_temp_HF	Max	0.6	ps/°C	1, 2, 3
	^{t}WCK2DQI_temp_LF	Max	0.7		
DQ to WCK Rx offset voltage variation (write)	^{t}WCK2DQI_volt_HF	Max	25	ps/50mV	1, 2, 3
	^{t}WCK2DQI_volt _LF	Max	50		
Absolute high clock pulse width	^{t}WCH(abs)	Min	43	^{t}WCK(avg)	
		Max	57		
Absolute low clock pulse width	^{t}WCL(abs)	Min	43	^{t}WCK(avg)	
		Max	57		
WCK to DQ offset (read)	^{t}WCK2DQO_HF	Min	650	ps	1, 2, 3
		Max	1600		
	^{t}WCK2DQO_LF	Min	650	ps	1, 2, 3
		Max	1900		
WCK to DQ offset temperature variation (read)	^{t}WCK2DQO_temp_HF	Max	1.5	ps/°C	1, 2, 3
	^{t}WCK2DQO_temp_LF	Max	1.8		
WCK to DQ offset voltage variation (read)	^{t}WCK2DQO_volt_HF	Max	3.0	ps/mV	1, 2, 3
	^{t}WCK2DQO_volt_LF	Max	5.0		

Notes: 1. _HF means high frequency and _LF means low frequency.
2. _LF is used for 3200 Mb/s and below (≤3200 Mb/s). _HF is used for 3200 Mb/s and above(≥3200 Mb/s).
3. WCK2DQ AC parameters (HF/LF) can be selectable by MR18 OP[3]. Refer to MR18.

Table 86: WCK Stop AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Valid write clock requirement after CAS(WS_OFF) command	^{t}WCKSTOP	Min	MAX(6ns, 2*n*CK)		

Table 87: WCK2CK Leveling Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit	Note
WCK_t/WCK_c drive start to WCK2CK leveling mode entry	^{t}WLWCKON	Min	2	^{t}CK	

Table 87: WCK2CK Leveling Timing Parameters (Continued)

Parameter	Symbol	Min/Max	Value	Unit	Note
First WCK_t/WCK_c edge after WCK2CK leveling mode is programmed	^{t}WLMRD	Min	MAX(14ns, 5^{t}CK)	ns	
Write leveling output delay	^{t}WLO	Min	0	ns	
		Max	MAX(20ns, 2^{t}CK)	ns	
WCK toggle interval	^{t}WCK_INT	Min	MAX(25ns, 2.5^{t}WCK)	ns	
WCK off delay after write leveling mode exit	^{t}WLWCKOFF	Min	MAX(14ns, 5^{t}CK)	ns	
DQ off delay after write leveling mode exit	^{t}WLDQOFF	Max	MAX(14ns, 5^{t}CK)	ns	
WCK cycle per WCK2CK phase detection	^{t}WCKTGGL	Min	7.5	^{t}WCK	1
		Max	7.5	^{t}WCK	
WCK to CK phase offset	^{t}WCK2CK	Min	MAX(–0.5^{t}WCK, TBD)	ps	2
		Max	MIN(0.5^{t}WCK, TBD)		
		Min	MAX(–0.25^{t}WCK, TBD)	ps	3
		Max	MIN(0.25^{t}WCK, TBD)		
WCK2CK leveling phase search range	^{t}WCK2CK_ leveling	Min	MAX(–0.5 × ^{t}WCK, TBD)	ps	4
		Max	MIN(0.5 × ^{t}WCK, TBD)	ps	

Notes: 1. 7.5 WCK cycles are required per WCK2CK phase detection.
2. When MR18 OP[7] = 0: WCK: CK = 4:1.
3. When MR18 OP[7] = 1: WCK: CK = 2:1.
4. The device will return correct ^{t}WCK2CK phase relation information in the WCK2CK leveling mode within the range specified. However, the maximum WCK to CK phase shift allowed for normal DRAM operation may be limited by ^{t}WCK2CK.

Table 88: ^{t}WCK to CK/DQ Offset Rank-to-Rank Variation

Parameter	Symbol	WCK Frequency Mode	Min/Max	Data Rate [Mb/s] 6400	Data Rate [Mb/s] 7500/8500	Unit	Note
WCK to CK offset rank-to-rank variation	^{t}WCK2CK_ rank2rank	All modes	Min	0	0	ps	1, 2, 3
			Max	100	90		
WCK to DQ input offset rank-to-rank variation	^{t}WCK2DQI_ rank2rank	High-frequency mode	Min	0	0	ps	1, 2, 3, 4, 5
			Max	150	140		
		Low-frequency mode	Min	0			
			Max	250			
WCK to DQ output offset rank-to-rank variation	^{t}WCK2DQO_ rank2rank	High-frequency mode	Min	0		ps	1, 2, 3, 4, 5
			Max	400			
		Low-frequency mode	Min	0			
			Max	650			

Notes: 1. The same voltage and temperature are applied to ^{t}WCK2DQI_rank2rank and ^{t}WCK2DQO_rank2rank AC parameters.
2. ^{t}WCK2CK_rank2rank, ^{t}WCK2DQI_rank2rank, and ^{t}WCK2DQO_rank2rank AC parameters are applied to multiple ranks per channel within a package consisting of the same design die.
3. ^{t}WCK2CK_rank2rank, ^{t}WCK2DQI_rank2rank, and ^{t}WCK2DQO_rank2rank AC parameters are applied to multi-byte mode die per channel that shares the same CK input within a package consisting of the same design die.
4. MR18 OP[3] = 0b in WCK low-frequency mode; MR18 OP[3] = 1b in WCK high-frequency mode.
5. WCK low-frequency mode is valid when write clock frequency is ≤ 1600 MHz.

Table 89: WCK Oscillator Matching Error Specification for High-Frequency Mode

Parameter	Symbol	Min	Max	Unit	Note
Write WCK oscillator matching error: voltage variation	$WOSC_{match\_volt}$	–7.5	7.5	ps	1, 2, 3, 5
Write WCK oscillator matching error: temperature variation	$WOSC_{match\_temp}$	–7.5	7.5	ps	1, 2, 3, 5
Write WCK oscillator offset: voltage variation	$WOSC_{offset\_volt}$	–100	100	ps	2, 5
Write WCK oscillator offset: temperature variation	$WOSC_{offset\_temp}$	–100	100	ps	2, 5
Read WCK oscillator matching error: voltage variation	$ROSC_{match\_volt}$	–20	20	ps	1, 2, 3, 6
Read WCK oscillator matching error: temperature variation	$ROSC_{match\_vtemp}$	–20	20	ps	1, 2, 3, 6
Read WCK oscillator offset: voltage variation	$ROSC_{offset\_volt}$	–200	200	ps	2, 6
Read WCK oscillator offset: temperature variation	$ROSC_{offset\_temp}$	–200	200	ps	2, 6

Notes: 1. $WOSC_{match}$ or $ROSC_{match}$ is the matching error between the actual WCK and WCK interval oscillator for voltage and temperature.
2. This parameter is characterized or guaranteed by design.
3. The input stimulus for ^{t}WCK2DQ is consistent for voltage and temperature conditions.
4. ^{t}WCK2DQ(V,T) delay is the average of WCK to DQ delay over the runtime period.
5. The matching error and offset of WOSC are from the WCK2DQI interval oscillator.
6. The matching error and offset of ROSC are from the WCK2DQO interval oscillator.
7. For elevated automotive-grade 1/2/3 temperature range, contact Micron for temperature variation specs.

Table 90: WCK Oscillator Matching Error Specification for Low-Frequency Mode

Parameter	Symbol	Min	Max	Unit	Note
Write WCK oscillator matching error: voltage variation	$WOSC_{match\_volt}$	-20.0	20.0	ps	1, 2, 3, 5
Write WCK oscillator matching error: temperature variation	$WOSC_{match\_temp}$	-20.0	20.0	ps	1, 2, 3, 5
Write WCK oscillator offset: voltage variation	$WOSC_{offset\_volt}$	-100	100	ps	2, 5
Write WCK oscillator offset: temperature variation	$WOSC_{offset\_temp}$	-100	100	ps	2, 5
Read WCK oscillator matching error: voltage variation	$ROSC_{match\_volt}$	-50	50	ps	1, 2, 3, 6
Read WCK oscillator matching error: temperature variation	$ROSC_{match\_vtemp}$	-50	50	ps	1, 2, 3, 6
Read WCK oscillator offset: voltage variation	$ROSC_{offset\_volt}$	-200	200	ps	2, 6
Read WCK oscillator offset: temperature variation	$ROSC_{offset\_temp}$	-200	200	ps	2, 6

Notes: 1. The $WOSC_{match}$ or $ROSC_{match}$ is the matching error between the actual WCK and WCK interval oscillator for voltage and temperature.
2. This parameter is characterized or guaranteed by design.
3. The input stimulus for ^{t}WCK2DQ is consistent for voltage and temperature conditions.
4. ^{t}WCK2DQ(V,T) delay is the average of the WCK to DQ delay over the runtime period.

5. The matching error and offset of WOSC are from WCK2DQI interval oscillator.
6. The matching error and offset of ROSC are from WCK2DQO interval oscillator.

Table 91: WCK2DQI/WCK2DQO Interval Oscillator AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Delay time from STOP WCK2DQI INTERVAL OSCILLATOR command to mode register readout	^{t}OSCODQI	Min	MAX(40ns, 8*n*CK)	ns	
Delay time from STOP WCK2DQ0 INTERVAL OSCILLATOR command to mode register readout	^{t}OSCODQO	Min	MAX(40ns, 8*n*CK)	ns	
Delay time from MPC OSC STOP command to MPC OSC START command	^{t} OSCINT	Min	MAX(40ns, 8*n*CK)	ns	

ZQ Calibration, Post Package Repair, and Training-Related Timings

Table 92: Command Bus Training AC Timing Table – Mode 1

Parameter	Symbol	Min/Max	WCK Frequency (MHz) All Operating Points (266 MHz to 3200 MHz)	Unit	Note
Static WCK period (CBT entry to WCK toggling start)	^{t}CBTWCKPRE _static	Min	MAX(20ns, 2*n*CK)	ns	
Set-up margin between DQ7 and WCK	^{t}WCK2DQ7H	Min	MAX(5ns, 12*n*WCK)	ns	
Hold margin between DQ7 and WCK	^{t}DQ7HWCK	Min	MAX(5ns, 12*n*WCK)	ns	
Clock and command valid after DQ7 HIGH	^{t}DQ7HCK	Min	MAX(5ns, 3*n*CK)	ns	
ODT CA change latency after DQ7 HIGH	^{t}DQ7FSP	Min	20	ns	
Valid clock requirement before CS HIGH	^{t}CKPRECS	Min	2^{t}CK + ^{t}XP (^{t}XP = MAX(7ns, 3*n*CK))	ns	
Valid clock requirement after CS HIGH	^{t}CKPSTCS	Min	MAX(7.5ns, 3*n*CK)	ns	
Delay time from DQ[7] HIGH to CA bus training	^{t}CAENT	Min	250	ns	
Asynchronous data read	^{t}ADR	Max	20	ns	
CA BUS TRAINING command to CA BUS TRAINING command delay	^{t}CACD	Min	RU(^{t}ADR/^{t}CK)	ns	1
Valid clock requirement before DQ7 LOW	^{t}DQ7LCK	Min	MAX(5ns, 3*n*CK)	ns	
DQ7 LOW to DQ driver off	^{t}MRZ	Min	1.5	ns	
DQ7 LOW to static WCK	^{t}DQ7LWCK	Min	MAX(5ns, 12*n*WCK)	ns	
Exit command bus training mode to next valid command delay	^{t}XCBT	Min	MAX(250ns, 5*n*CK)	ns	
Stable time for WCK ODT	^{t}CBTWCKODTFIX	Max	20	ns	
Turn off time for DQ ODT	^{t}CBTODTOFF	Max	20	ns	
Turn off time for NT-ODT	^{t}CBTNTODTOFF	Max	20	ns	

Note: 1. If ^{t}CACD is violated, the data for samples which violate ^{t}CACD may not be available except for the last sample (where ^{t}CACD after this sample is met). Valid data for the last sample is available after ^{t}ADR.

Table 93: Command Bus Training AC Timing Table – Mode 2

Parameter	Symbol	Min/Max	WCK Frequency (MHz) All Operating Points (266 MHz to 3200 MHz)	Unit	Note
Static WCK period (CBT entry to WCK toggling start)	^{t}CBTWCKPRE_static	Min	MAX(20ns, 2*n*CK)	ns	
Set-up margin between DQ7 and WCK	^{t}WCK2DQ7H	Min	MAX(5ns, 12*n*WCK)	ns	
Hold margin between DQ7 and WCK	^{t}DQ7HWCK	Min	MAX(5ns, 12*n*WCK)	ns	
Clock and command valid after DQ7 HIGH	^{t}DQ7HCK	Min	MAX(5ns, 3*n*CK)	ns	
ODT CA change latency after DQ7 HIGH	^{t}DQ7FSP	Max	20	ns	
DQ7 HIGH to valid DQ[6:0] input for $V_{REF(CA)}$ setting	^{t}DQ72DQ	Min	250	ns	
Valid clock requirement before CS HIGH	^{t}CKPRECS	Min	2^{t}CK + ^{t}XP (^{t}XP = MAX(7ns, 3*n*CK))	ns	
Valid clock requirement after CS HIGH	^{t}CKPSTCS	Min	MAX(7.5ns, 3*n*CK)	ns	
V_{REF} step time-long	^{t}VREF(CA)_long	Max	250 + 0.5^{t}CK	ns	1
V_{REF} step time-short	^{t}VREF(CA)_short	Max	200 + 0.5^{t}CK	ns	2
Data setup for V_{REF} training mode	^{t}DStrain	Min	MAX(5ns, 12*n*WCK)	ns	
Data hold for V_{REF} training mode	^{t}DHtrain	Min	MAX(5ns, 12*n*WCK)	ns	
Asynchronous data read	^{t}ADR	Max	20	ns	
CBT command input to DMI LOW	^{t}CA2DMIL	Min	30	ns	
DMI LOW to DQ driver off	^{t}MRZ	Min	1.5	ns	
DMI LOW to valid DQ input for $V_{REF(CA)}$ setting	^{t}CBTRTW	Min	MAX(20ns, 12*n*WCK)	ns	
CA BUS TRAINING command to CA BUS TRAINING command delay	^{t}CACD	Min	RU(^{t}ADR/^{t}CK)	^{t}CK	
Valid clock requirement before DQ7 LOW	^{t}DQ7LCK	Min	MAX(5ns, 3*n*CK)	ns	
DQ7 LOW to static WCK	^{t}DQ7LWCK	Min	MAX(5ns, 12*n*WCK)	ns	
Exit command bus training mode to next valid command delay	^{t}XCBT	Min	MAX(250ns, 5*n*CK)	ns	
Stable time for WCK ODT	^{t}CBTWCKODTFIX	Max	20	ns	
Turn off time for DQ ODT	^{t}CBTODTOFF	Max	20	ns	
Turn off time for NT-ODT	^{t}CBTINTODTOFF	Max	20	ns	

Notes: 1. $V_{REF(CA)\_long}$ is for at least a two step-size increment/decrement change including: $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change in V_{REF} voltage.

2. $V_{REF(CA)\_short}$ is for a single step-size increment/decrement change in V_{REF} voltage.

Table 94: ZQ Calibration Timing

Parameter	Symbol	Min/Max	Value	Unit
ZQ CALIBRATION Command to latch time, NZQ ≤ 4	$^tZQCAL4$	Min	1.5	µs
ZQ CALIBRATION Command to latch time, NZQ ≤ 8	$^tZQCAL8$	Min	3	µs
ZQ CALIBRATION Command to latch time, NZQ ≤ 16	$^tZQCAL16$	Min	6	µs
ZQ calibration latch time	^tZQLAT	Min	MAX(30ns, 4*n*CK)	ns
ZQ calibration reset time	$^tZQRESET$	Min	MAX(50ns, 3*n*CK)	ns
Delay time from ZQ Stop bit set to ZQ resistor available	^tZQSTOP	Max	30	ns
Background calibration interval	^tZQINT	Max	Programmable, 32, 64, 128, or 256	ms
Maximum number of LPDDR5 devices (die) connected to a single ZQ resistor	NZQ	Max	16	Die
Maximum capacitive load on ZQ network	CZQ_N	Max	TBD	pF

Table 95: Post-Package Repair Timing Parameters

Parameter	Symbol	Min	Max	Unit
PPR programming clock	^tCKPGM	1.25	200	ns
PPR programming time	^tPGM	2000	–	ms
PPR exit time	$^tPGM\_exit$	15	–	ns
New address setting time	^tPGMPST	500	–	µs

Table 96: Rx Offset Calibration Training Time Parameter

Parameter	Symbol	Min/Max	Value	Unit
Rx offset calibration training time	^tOSCAL	Max	3	µs

Table 97: Enhanced WCK Always-On Mode Timing

Parameter	Symbol	Min	Max	Unit
Delay from CAS WCK SUSPEND command to next READ, WRITE, or MASKED WRITE command	^tWCKSUS	4	-	nCK

Table 98: Read/Write-Based RDQS_t Training Mode Entry and Exit Timings

Parameter	Symbol	Min/Max	Value	Unit
Read/Write-based RDQS_t training mode entry	$^tRDQSTFE$	Min	MAX(35ns, 4*n*CK)	ns
Read/Write-based RDQS_t training mode exit	$^tRDQSTFX$	Min	MAX(35ns, 4*n*CK)	ms

Table 99: Enhanced RDQS Training Mode Entry and Exit Timing

Parameters	Symbol	Min/Max	Value	Unit
Enhanced RDQS toggle mode entry	^tERQE	Max	MAX(35ns, 4*n*CK)	ns

Table 99: Enhanced RDQS Training Mode Entry and Exit Timing (Continued)

Parameters	Symbol	Min/Max	Value	Unit
Enhanced RDQS toggle mode exit	^{t}ERQX	Max	MAX(35ns, 4*n*CK)	ns
ODT disable from enhanced RDQS toggle mode entry	^{t}RDQE_OD	Max	MAX(35ns, 4*n*CK)	ns
ODT enable from enhanced RDQS toggle mode exit	^{t}RDQX_OD	Max	MAX(35ns, 4*n*CK)	ns

ODT Related Timing

Table 100: Asynchronous ODT Turn On and Turn Off Timing

Parameter	All Operating Points	Unit
^{t}ODTon,min	1.5	ns
^{t}ODTon,max	3.5	ns
^{t}ODToff,min	1.5	ns
^{t}ODToff,max	3.5	ns

Table 101: Asynchronous NT ODT Turn On and Turn Off Timing for Write

Parameter	All Operating Frequencies	Unit
^{t}ODT_on,min	1.5	ns
^{t}ODT_on,max	3.5	ns
^{t}ODT_off,min	1.5	ns
^{t}ODT_off,max	3.5	ns

Table 102: NT ODT AC Timing

Parameter	Symbol	Min/Max	Value	Unit	Note
Delay from MRW command to NT ODT switching	^{t}NTODT	Max	Max (14ns, 5*n*CK)		1

Note: 1. ^{t}NTODT is defined as the delay time from MRW-2 command (the falling edge of the CK_t) to start point of ^{t}ODTon/^{t}ODToff. Which ^{t}ODTon or ^{t}ODToff applies depends on the previous NT ODT status.

Table 103: ODT Command/Address AC Timing Parameters

Parameters	Symbol	All Operating Points		Unit
		Min	Max	
ODT C/A value update time	^{t}ODTUP	250	–	ns

V_{DDQ} Ramp, DCM, and Write X Timing

Table 104: V_{DDQ} Ramp Rates

Parameter	Symbol	Min/Max	Value	Unit
V_{DDQ} slew rate V_{RCG} enabled	V_{DQSR1}	Max	20	mV/µs
V_{DDQ} slew rate V_{RCG} disabled	V_{DQSR2}	Max	4.8	mV/µs

Table 105: DCM Timing

Parameter	Symbol	Min/Max	WCK Frequency (MHz) All Operating Points (800 MHz to 3200 MHz)	Unit
Duty cycle monitor measurement time	^{t}DCMM	Min	2	µs

Table 106: Write X AC Timing

Parameter	Symbol	Min/Max	Value	Unit
Valid WCK requirement after write with write X	^{t}WR2WCK	Max	1.25	ns

CK and WCK AC Timings

CK Specifications

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the minimum/maximum values may result in malfunction of the device.

Definition of ^{t}CK(avg) and *n*CK

^{t}CK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CL_j \right) / N$$

Where N = 200

Unit "^{t}CK(avg)" represents the actual clock average ^{t}CK(avg) of the input clock under operation. Unit "nCK" represents one clock cycle of the input clock, counting the actual clock edges. ^{t}CK(avg) may change by up to ±1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

Definition of ^{t}CK(abs)

^{t}CK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

^{t}CK(abs) is not subject to production test.

Definition of ^{t}CH(avg) and ^{t}CL(avg)

^{t}CH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$^tCH(avg) = \left(\sum_{j=1}^{N} {}^tCH_j\right) / N \times {}^tCK(avg)$$

Where N = 200

^{t}CL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$^tCL(avg) = \left(\sum_{j=1}^{N} {}^tCL_j\right) / N \times {}^tCK(avg)$$

Where N = 200

Definition of ^{t}CH(abs) and ^{t}CL(abs)

^{t}CH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

^{t}CL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both ^{t}CH(abs) and ^{t}CL(abs) are not subject to production test.

Definition of ^{t}JIT(per)

^{t}JIT(per) is the single period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).

^{t}JIT(per) = MIN/MAX of (^{t}CKi - ^{t}CK(avg)) where i = 1 to 200.

^{t}JIT(per), act is the actual clock jitter for a given system.

^{t}JIT(per), allowed is the specified allowed clock period jitter.

^{t}JIT(per) is not subject to production test.

Definition of ^{t}JIT(cc)

^{t}JIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

^{t}JIT(cc) = MAX|{^{t}CK(i +1) - ^{t}CK(i)}|.

^{t}JIT(cc) defines the cycle to cycle jitter.

^{t}JIT(cc) is not subject to production test.

Table 107: Clock AC Timing

Parameter	Symbol	5 MHz		10 MHz		67 MHz		133 MHz		200 MHz		267 MHz		344 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	^{t}CK(avg)	200	200	100	200	14.93	200	7.5	200	5	200	3.75	200	2.9	200	ns
Average high pulse width	^{t}CH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}CK(avg)
Average low pulse width	^{t}CL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}CK(avg)
Absolute clock period	^{t}CK(abs)	Min: ^{t}CK(avg)min + ^{t}JIT(per)min Max: –														ns
Absolute high pulse width	^{t}CH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK(avg)
Absolute low pulse width	^{t}CL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK(avg)
Clock period jitter	^{t}JIT(per)	–11,200	11,200	–5600	5600	–840	840	–430	430	–280	280	–210	210	–170	170	ps
Maximum clock Jitter between consecutive cyc les	^{t}JIT(cc)	–	22,400	–	11,200	–	1680	–	860	–	560	–	420	–	340	ps

Table 108: Clock AC Timing

Parameter	Symbol	400 MHz		467 MHz		533 MHz		600 MHz		688 MHz		750 MHz		800 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	^{t}CK(avg)	2.5	200	2.15	200	1.875	200	1.667	200	1.453	200	1.333	200	1.25	200	ns
Average high pulse width	^{t}CH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}CK(avg)
Average low pulse width	^{t}CL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}CK(avg)
Absolute clock period	^{t}CK(abs)	Min: ^{t}CK(avg)min + ^{t}JIT(per)min Max: –														ns
Absolute high pulse width	^{t}CH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK(avg)
Absolute low pulse width	^{t}CL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK(avg)
Clock period jitter	^{t}JIT(per)	–140	014	–120	120	–110	110	–95	95	–85	85	–75	75	–70	70	ps

Table 108: Clock AC Timing (Continued)

Parameter	Symbol	400 MHz		467 MHz		533 MHz		600 MHz		688 MHz		750 MHz		800 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Maximum clock Jitter between consecutive cycles	^{t}JIT(cc)	–	280	–	240	–	220	–	190	–	170	–	150	–	140	ps

Table 109: Clock AC Timing

Parameter	Symbol	937.5 MHz		1066.5 MHz		Unit
		Min	Max	Min	Max	
Average clock period	^{t}CK(avg)	1066.7	200,000	937.6	200,000	ps
Average high pulse width	^{t}CH(avg)	0.46	0.54	0.46	0.54	^{t}CK(avg)
Average low pulse width	^{t}CL(avg)	0.46	0.54	0.46	0.54	^{t}CK(avg)
Absolute clock period	^{t}CK(abs)	Min: ^{t}CK(avg)min + ^{t}JIT(per)min Max: –				ps
Absolute high pulse width	^{t}CH(abs)	0.43	0.57	0.43	0.57	^{t}CK(avg)
Absolute low pulse width	^{t}CL(abs)	0.43	0.57	0.43	0.57	^{t}CK(avg)
Clock period jitter	^{t}JIT(per)	TBD	TBD	TBD	TBD	ps
Maximum clock Jitter between consecutive cycles	^{t}JIT(cc)	–	TBD	–	TBD	ps

WCK Specifications

The jitter specified is a random jitter meeting a Gaussian distribution. Input write clocks violating the min/max values may result in malfunction of the LPDDR5 device.

^{t}WCK(avg) is calculated as the average write clock period across any consecutive 200 cycle window, where each write clock period is calculated from rising edge to rising edge.

Definition of ^{t}WCK(avg) and *n*WCK

$$ {}^{t}\mathrm{WCK(avg)} = \left(\sum_{j=1}^{N} {}^{t}\mathrm{WCK}_j \right) / N $$

Where N = 200

Unit "^{t}WCK(avg)" represents the actual write clock average ^{t}WCK(avg) of the input write clock under operation. Unit "*n*WCK" represents one write clock cycle of the input write clock, counting the actual write clock edges. ^{t}WCK(avg) may change by up to ±1% within a 100 write clock cycle window, provided that all jitter and timing specifications are met.

Definition of ^{t}WCK(abs)

^{t}WCK(abs) is defined as the absolute write clock period, as measured from one rising edge to the next consecutive rising edge.

^{t}WCK(abs) is not subject to production test.

Definition of ^{t}WCKH(avg) and ^{t}WCKL(avg)

^{t}WCKH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$ {}^{t}\mathrm{WCKH(avg)} = \left(\sum_{j=1}^{N} {}^{t}\mathrm{WCKH}_j \right) / \left(N \times {}^{t}\mathrm{WCK(avg)}\right) $$

Where N = 200

^{t}WCKL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$ {}^{t}\mathrm{WCKL(avg)} = \left(\sum_{j=1}^{N} {}^{t}\mathrm{WCKL}_j \right) / N \times {}^{t}\mathrm{WCK(avg)} $$

Where N = 200

Definition for ^{t}WCKH(abs) and ^{t}WCKL(abs)

^{t}WCKH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge.

^{t}WCKL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge.

Both ^{t}WCKH(abs) and ^{t}WCKL(abs) are not subject to production test.

Definition for ^{t}JIT(per)

^{t}JIT(per) is the single period jitter defined as the largest deviation of any signal ^{t}WCK from ^{t}WCK(avg).

^{t}JIT(per) = MIN/MAX of (^{t}WCKi - ^{t}WCK(avg)) where i = 1 to 200.

^{t}JIT(per), act is the actual write clock jitter for a given system.

^{t}JIT(per), allowed is the specified allowed write clock period jitter.

^{t}JIT(per) is not subject to production test.

Definition for ^{t}JIT(cc)

^{t}JIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles.

^{t}JIT(cc) = MAX|{^{t}WCK(i +1) - ^{t}WCK(i)}|.

^{t}JIT(cc) defines the cycle to cycle jitter.

^{t}JIT(cc) is not subject to production test.

Definition for ^{t}ERR(2per)

^{t}ERR(2per) is defined as the cumulative error across 2 consecutive cycles from ^{t}WCK(avg). ^{t}ERR(2per) is not subject to production test.

$$^t\mathrm{ERR(nper)} = \left(\sum_{j=i}^{i+N-1} {^t\mathrm{WCKj}}\right) - (N \times {^t}\,\mathrm{WCK(avg)})$$

Where N = 2

Definition for ^{t}ERR(3per)

^{t}ERR(3per) is defined as the cumulative error across 3 consecutive cycles from ^{t}WCK(avg). ^{t}ERR(3per) is not subject to production test.

$$^t\mathrm{ERR(nper)} = \left(\sum_{j=i}^{i+N-1} {^t\mathrm{WCKj}}\right) - (N \times {^t}\,\mathrm{WCK(avg)})$$

Where N = 3

Definition for ^{t}ERR(4per)

^{t}ERR(4per) is defined as the cumulative error across 4 consecutive cycles from ^{t}WCK(avg). ^{t}ERR(3per) is not subject to production test.

$$^t\mathrm{ERR(nper)} = \left(\sum_{j=i}^{i+N-1} {^t\mathrm{WCKj}}\right) - (N \times {^t}\,\mathrm{WCK(avg)})$$

Where N = 4

Table 110: Write Data Clock AC Timing

Parameter	Symbol	WCK Frequency (MHz)												Unit
		266		566		800		1067		1375		1600		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Average write clock period	^{t}WCK(avg)	3.76	50	1.877	50	1.25	50	0.938	50	0.728	50	0.625	50	ns
Average high pulse width	^{t}WCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}WCK(avg)
Average low pulse width	^{t}WCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}WCK(avg)
Absolute write clock period	^{t}WCK(abs)	Min: ^{t}WCK(avg)min + ^{t}JIT(per)min Max: –												ns
Absolute high write clock pulse width	^{t}WCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}WCK(avg)
Absolute low write clock pulse width	^{t}WCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}WCK(avg)
Write clock period jitter tJIT(per)	Clock period jitter ^{t}JIT(per)	–190	190	–95	95	–70	70	–56	56	–46	46	–40	40	ps
Maximum write clock jitter between consecutive cycles	^{t}JIT(cc)	–	380	–	190	–	140	–	112	–	92	–	80	ps
Cumulative error across 2 cycles	^{t}JIT(2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	^{t}JIT(3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	^{t}JIT(4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Table 111: Write Data Clock AC Timing

Parameter	Symbol	WCK Frequency (MHz)												Unit
		1867		2134		2400		2750		3000		3200		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Average write clock period	^{t}WCK(avg)	0.536	50	0.469	50	0.417	50	0.364	50	0.334	50	0.313	50	ns
Average high pulse width	^{t}WCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}WCK(avg)
Average low pulse width	^{t}WCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	^{t}WCK(avg)
Absolute write clock period	^{t}WCK(abs)	Min: ^{t}WCK(avg)min + ^{t}JIT(per)min Max: –												ns
Absolute high write clock pulse width	^{t}WCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}WCK(avg)
Absolute low write clock pulse width	^{t}WCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}WCK(avg)
Write clock period jitter tJIT(per)	Clock period jitter ^{t}JIT(per)	–34	34	–30	30	–28	28	–26	26	–24	24	–22	22	ps
Maximum write clock jitter between consecutive cycles	^{t}JIT(cc)	–	68	–	60	–	56	–	52	–	48	–	44	ps
Cumulative error across 2 cycles	^{t}JIT(2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	^{t}JIT(3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	^{t}JIT(4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Table 112: Write Data Clock AC Timing

Parameter	Symbol	WCK Frequency (MHz)				Unit
		3750		4266.5		
		Min	Max	Min	Max	
Average write clock period	^{t}WCK(avg)	266.7	50,000	234.4	50,000	ps

Table 112: Write Data Clock AC Timing (Continued)

Parameter	Symbol	WCK Frequency (MHz)				Unit
		3750		4266.5		
		Min	Max	Min	Max	
Average high pulse width	$^tWCKH(avg)$	0.46	0.54	0.46	0.54	$^tWCK(avg)$
Average low pulse width	$^tWCKL(avg)$	0.46	0.54	0.46	0.54	$^tWCK(avg)$
Absolute write clock period	$^tWCK(abs)$	Min: $^tWCK(avg)min + {}^tJIT(per)min$ Max: –				ns
Absolute high write clock pulse width	$^tWCKH(abs)$	0.43	0.57	0.43	0.57	$^tWCK(avg)$
Absolute low write clock pulse width	$^tWCKL(abs)$	0.43	0.57	0.43	0.57	$^tWCK(avg)$
Write clock period jitter $^tJIT(per)$	Clock period jitter $^tJIT(per)$	TBD	TBD	TBD	TBD	ps
Maximum write clock jitter between consecutive cycles	$^tJIT(cc)$	–	TBD	–	TBD	ps
Cumulative error across 2 cycles	$^tJIT(2per)$	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	$^tJIT(3per)$	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	$^tJIT(4per)$	TBD	TBD	TBD	TBD	ps

AC Parameters for Single-Ended

The AC timing shown in the following table is applied under conditions of single-ended (SE) mode.

Table 113: SE from/to Differential FSP and Additional Period for MRW AC Timing

Parameter	Symbol	Min/Max	Data Rate ≤1600 Mb/s	Unit
Frequency set point parameters for switching from/to differential clock				
Valid clock requirement after entering FSP, when changing between SE and differential modes	$^tCKFSPE\_SE$	Min	MAX(15ns, 8nCK)	–
Valid clock requirement before first valid command after an FSP change between SE and differential modes	$^tCKFSPX\_SE$	Min	MAX(15ns, 8nCK)	–
Additional period for after an MRW command				
Post clock for MRW	$^tMRW\_PST$	Min	2	*n*CK

Table 114: Single-Ended Delta CK and WCK Specifications

Parameter/Symbol	Min/Max	Data Rate ≤1600 Mb/s	Unit	Note
V_{REF} for single-ended CK	–	$V_{DD2}/2$	–	
V_{REF} for single-ended WCK	–	$V_{DD2}/2$	–	
$^tCIVW1$	Min	0.52	UI	UI = 0.5 ^tCK
$^tCIVW2$	Min	0.35	UI	
$^tDIVW1$	Min	0.52	UI	UI = 0.5 ^tCK
$^tDIVW2$	Min	0.35	UI	UI = 0.5 ^tWCK
^tQSH	Min	^tWCKH - 0.1	$^tWCK(avg)$	UI = 0.5 ^tWCK
^tQSL	Min	^tWCKL - 0.1	$^tWCK(avg)$	
$^tWCK2CK$	Min	MAX(–0.25 × ^tWCK - 100ps, TBD)	PS	At WCK = 800 MHz, 2:1 mode WCK/CK asymmetrical
	Max	MIN(0.25 × ^tWCK +100ps, TBD)		

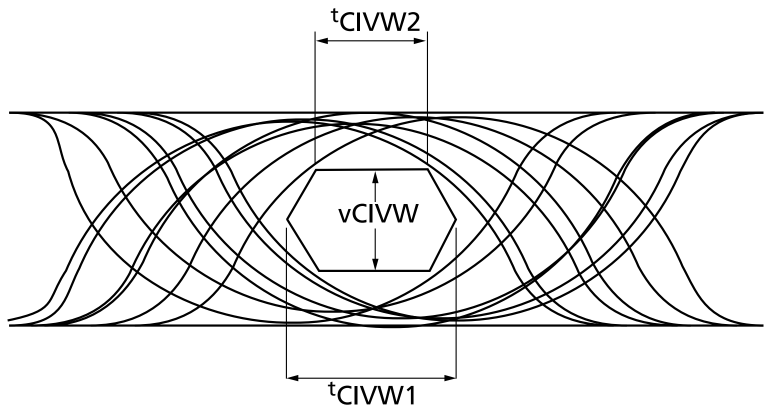
CA Rx Specification

CA Rx Mask and Single Pulse Definition

The CA Rx mask is defined as hexagonal mask shape as shown below. All CA signals apply to the same compliance mask and operate in double-data rate mode.

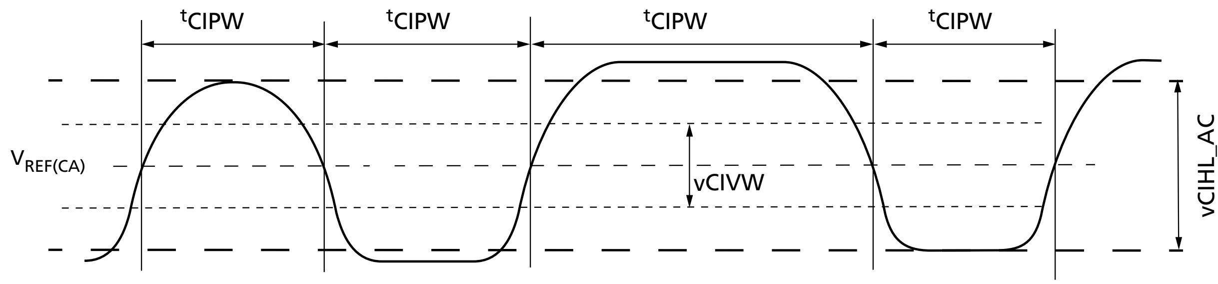
The receiver mask (Rx Mask) defines the area that the input signal must not encroach on for the DRAM input receiver to successfully capture a valid input signal.

Figure 23: CA Rx Mask Definition



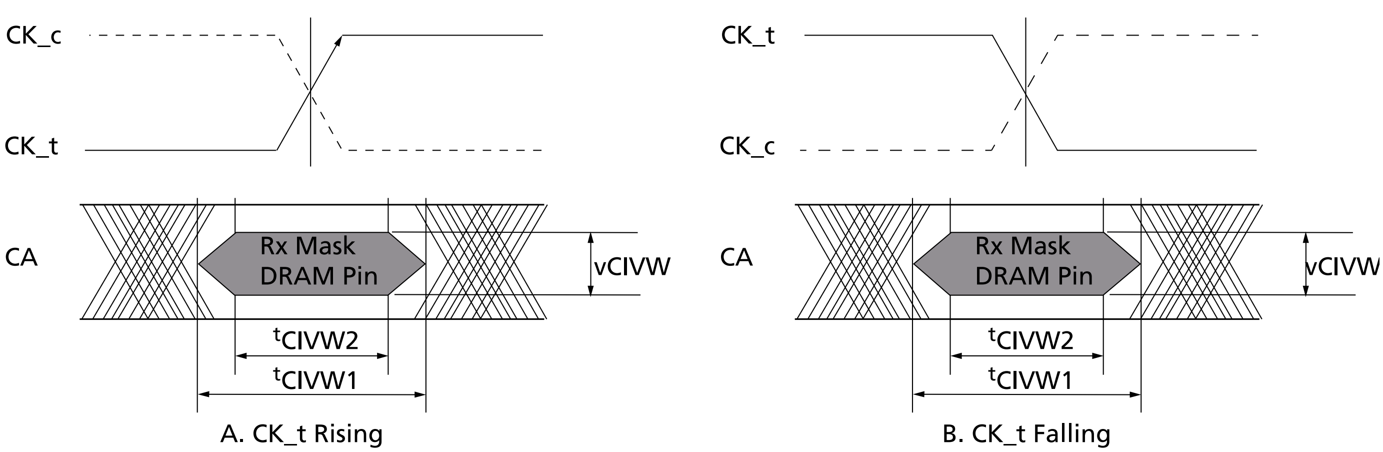
CA Rx Single Pulse Definition

Figure 24: CA Rx Single Pulse Definition



Notes: 1. Single pulse includes any cycle of the pulse.
2. $V_{REF(CA)}$ is the calculated value based on V_{DDQ} and MR12.

Figure 25: DRAM Pin CA Timings



Minimum CA eye should be $V_{REF(CA)}$ aligned.

Differential CK Mode Definition

All of the CA timings associated with DRAM pins are measured from CK_t/CK_c (differential mode)/CK (single-ended mode) to the center (midpoint) of the ^{t}CIVW1 and ^{t}CIVW2 window taken at the midpoint and vCIVW voltage level. The CA Rx mask window center is around the CK_t/CK_c cross point (differential mode)/CK (single-ended mode).

Table 115: CA Rx Specifications

<table>
<tr><th rowspan="2">Item</th><th rowspan="2">Symbol</th><th rowspan="2">Min/ Max</th><th colspan="14">CK Frequency (MHz)</th><th rowspan="2">Unit</th><th rowspan="2">Note</th></tr>
<tr><th>67[9]</th><th>133</th><th>200</th><th>266</th><th>344</th><th>400</th><th>467</th><th>533</th><th>600</th><th>688</th><th>750</th><th>800</th><th>937.5</th><th>1066.5</th></tr>
<tr><td colspan="19">Rx mask</td></tr>
<tr><td>CA Rx mask width at $V_{REF(CA)}$</td><td>^{t}CIVW1</td><td>Min</td><td colspan="14">0.3</td><td>UI</td><td>1, 2</td></tr>
<tr><td>CA Rx mask width at vCIVW</td><td>^{t}CIVW2</td><td>Min</td><td colspan="14">0.18</td><td>UI</td><td>1, 2</td></tr>
<tr><td>CA Rx mask height</td><td>vCIVW</td><td>Min</td><td colspan="14">155</td><td>mV</td><td>3</td></tr>
<tr><td colspan="3">Rx single pulse</td><td colspan="16"></td></tr>
<tr><td>CA Rx pulse width</td><td>^{t}CIPW</td><td>Min</td><td colspan="14">0.6</td><td>UI</td><td>4</td></tr>
<tr><td>CA Rx pulse amplitude</td><td>vCI-HL_AC</td><td>Min</td><td colspan="14">190</td><td>mV</td><td>5</td></tr>
<tr><td colspan="19">CA V_{REF}</td></tr>
<tr><td rowspan="2">CA V_{REF}</td><td rowspan="2">$V_{REF(CA)}$</td><td>Min</td><td colspan="14">75</td><td>mV</td><td>8</td></tr>
<tr><td>Max</td><td colspan="14">350</td><td>mV</td><td>8</td></tr>
<tr><td colspan="19">CA mask offset</td></tr>
<tr><td>CA to CA offset</td><td>^{t}CA2CA</td><td>Max</td><td colspan="14">100</td><td>ps</td><td>6</td></tr>
<tr><td>CA to CA offset shared CA</td><td>^{t}CA2-CA_share</td><td>Max</td><td colspan="14">150</td><td>ps</td><td>7</td></tr>
</table>

Notes: 1. The CA Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact for frequencies >TBD MHz and max voltage of TBD mV pk-pk from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise has to comply to the component Min-Max DC operating conditions.
2. Rx mask voltage vCIVWl (MAX) must be centered around $V_{REF(CA)}$.
3. The CA single input pulse signal amplitude into the receiver must meet or exceed vCIHL AC at any point over the total UI. No timing requirement above that level. vCIIHL AC is the peak-to-peak voltage centered around $V_{REF(CA)}$ such that vCIHL_AC/2 min must be met both above and below $V_{REF(CA)}$.
4. The CA only minimum input pulse width is defined at the $V_{REF(CA)}$.
5. vCIHL_AC does not have to be met when no transitions are occurring.
6. ^{t}CA2CA is defined as the fastest CA[x] mask center to the slowest CA[y] mask center.
7. ^{t}CA2CA_share is defined between dies which are in the same PKG and share same power supplies.
8. $V_{REF(CA)}$ is defined as % of $V_{REF(CA)}$ code x V_{DDQ}.
9. The Rx voltage and absolute timing requirements apply for all CA operating frequencies at or below 67 for all speed bins. For example ^{t}CIVW1 (ns) = 2.24ns at or below 67 MHz CK frequencies.

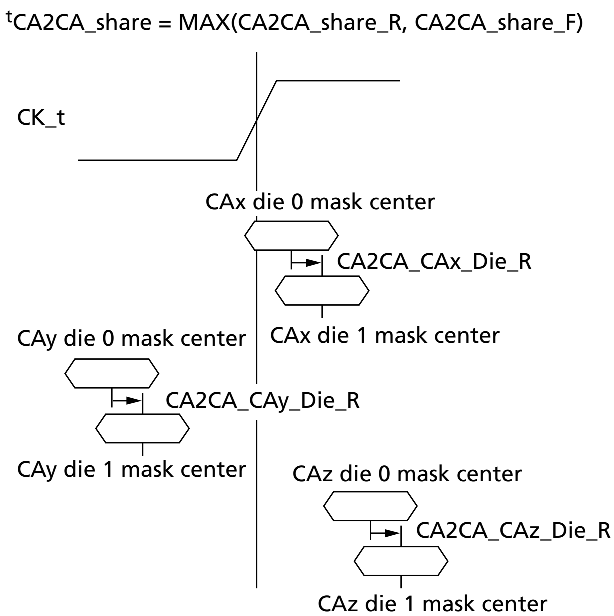
^{t}CA2CA_share Definition

For cases where the CA signals are shared between two die in the same package that utilize the same power supplies (byte mode), ^{t}CA2CA_share is required.

^{t}CA2CA_share_R Definition

CA2CA_share_R = MAX(CA2CA_CAi_Die_R) if MIN(CA2CA_CAi_Die_R) ≥ 0 |MAX(CA2CA_CAi_Die_R) - MIN(CA2CA_CAi_Die_R)| if MAX(CA2CA_CAi_Die_R) ≥ 0 and MIN(CA2CA_CAi_Die_R) < 0 |MIN(CA2CA_CAi_Die_R)| if MAX(CA2CA_CAi_Die_R) < 0

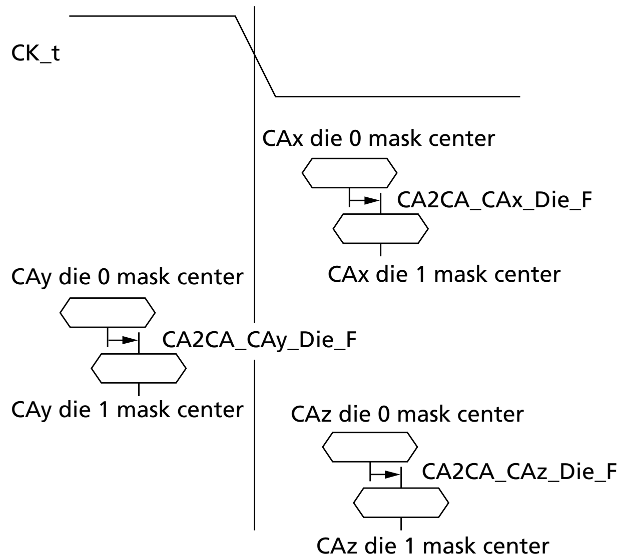
Figure 26: CK_t Rising Edge CA Mask



^{t}CA2CA_share_F Definition

CA2CA_share_F = MAX(CA2CA_CAi_Die_F) if MIN(CA2CA_CAi_Die_F) ≥ 0 |MAX(CA2CA_CAi_Die_F) - MIN(CA2CA_CAi_Die_F)| if MAX(CA2CA_CAi_Die_F) ≥ 0 and MIN(CA2CA_CAi_Die_F) < 0 |MIN(CA2CA_CAi_Die_F)| if MAX(CA2CA_CAi_Die_F) < 0

Figure 27: CK_t Falling Edge CA Mask



CS Rx Specification

CS Rx Mask and Single Pulse Definition

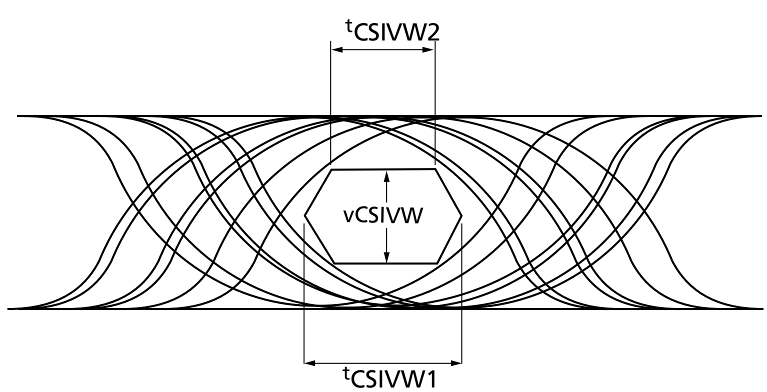
CS Rx is defined as either asynchronous or synchronous mode. The asynchronous mode Rx spec applies during power down/deep sleep mode and exit from power down/deep sleep mode. Synchronous mode applies when not in exit mode.

CS Rx Mask and Single Pulse Definition for Synchronous Mode

CS Rx mask for synchronous mode is defined as a hexagonal mask shape as shown below. CS signals apply the same compliance mask and operate in single data rate mode.

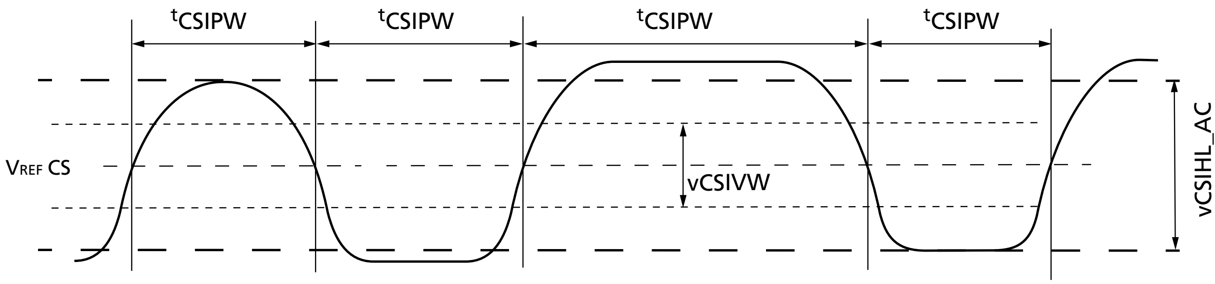
The receiver mask (Rx Mask) defines the area that the input signal must not encroach on for the DRAM input receiver to successfully capture a valid input signal.

Figure 28: Synchronous Mode CS Rx Mask Definition



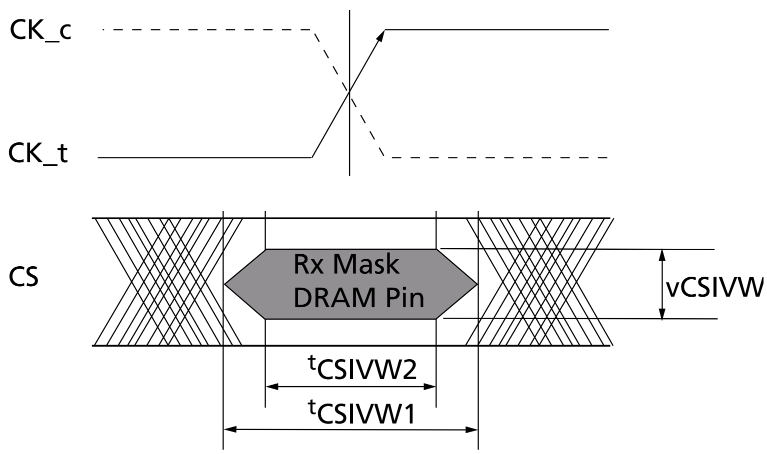
CS Rx Single Pulse Definition

Figure 29: Synchronous Mode CS Rx Single Pulse Definition



Note: 1. Single pulse includes any cycle of pulse.

Figure 30: Synchronous Mode CS Timing at DRAM Pin



Note: 1. Timing terms are measured from CK_t/CK_c (differential mode)/CK (single-end mode) to the center (midpoint) of the ^{t}CSIVW1 and ^{t}CSIVW2 window taken at the midpoint and vCSIVW voltage levels.

CS Rx Input Level Definition for Asynchronous Mode

The CS Rx specification for power-down mode is defined and shown in the following figure. CS has to be lower than V_{ILPD} to remain in power-down mode or deep-sleep mode. To exit from power-down or deep-sleep mode, CS must satisfy V_{IHPD} and power-down/deep-sleep timing specifications.

Figure 31: Asynchronous Mode V_{IHPD} and V_{ILPD} at Power-Down Exit

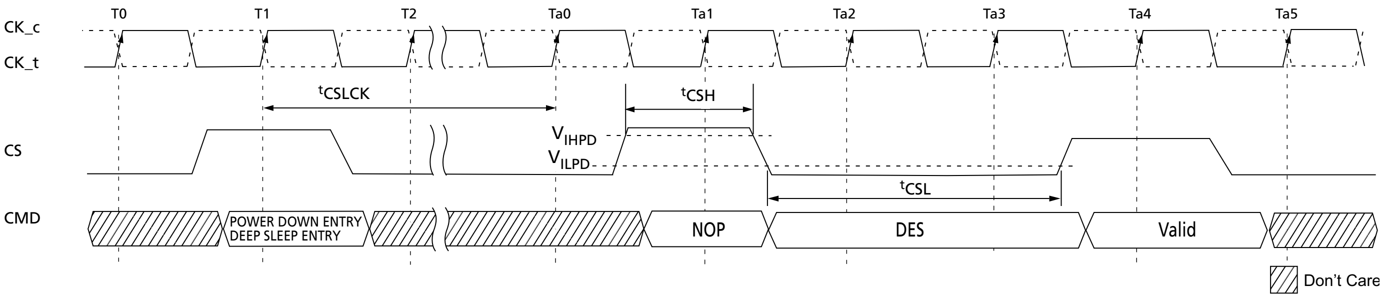


Table 116: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)														Unit	Note
			67.6	133	200	266	344	400	467	533	600	688	750	800	937.5	1006.5		
Rx mask																		
CS Rx mask height	vCSIVW	Min	180												TBD		mV	2
CS Rx mask width at V_{REF}CS	tCSIVW1	Min	0.3												TBD		UI	1
CS Rx mask width at VCSIVW	tCSIVW2	Min	0.22												TBD		UI	1
Rx single pulse																		
CS Rx pulse amplitude	vCSI-HL_AC	Min	240												TBD		mV	3
CS reference voltage	VREFCS		$V_{DD2H}/3$														mV	
CS Rx pulse width	tCSIPW	Min	0.6												TBD		UI	
Power down																		
CS V_{IL} during power down/deep sleep	V_{ILPD}	Max	130														mV	4
CS V_{IH} during power down/deep sleep	V_{IHPD}	Min	550														mV	5
		Max	V_{DD2H} + 200															

Notes:
1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; no timing requirement above a certain level. vCSIIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.

5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.
6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^{t}CSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.

DQ, DMI, Parity, and DBI Rx Specification

DQ, DMI, Parity, DBI Rx Mask, and Single Pulse Definition

LPDDR5 DQ, DMI, Parity, and DBI Rx mask is defined as the hexagonal mask shown below. The mask (vDIVW, ^{t}DIVW1, ^{t}DIVW2) defines the area that the input signal must not encroach on for the DQ input receiver to successfully capture an input signal.

Figure 32: DQ, DMI, Parity, and DBI Rx Mask Definition

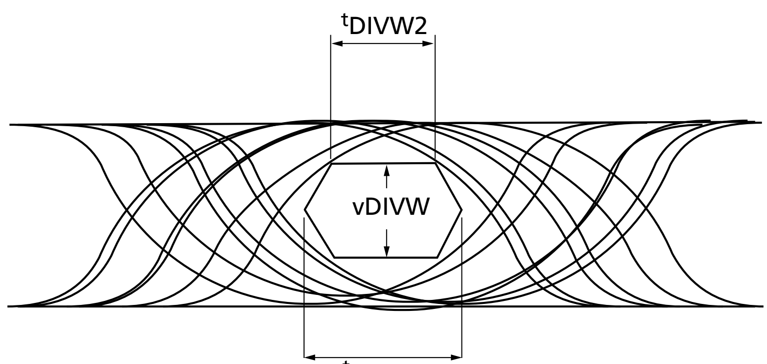
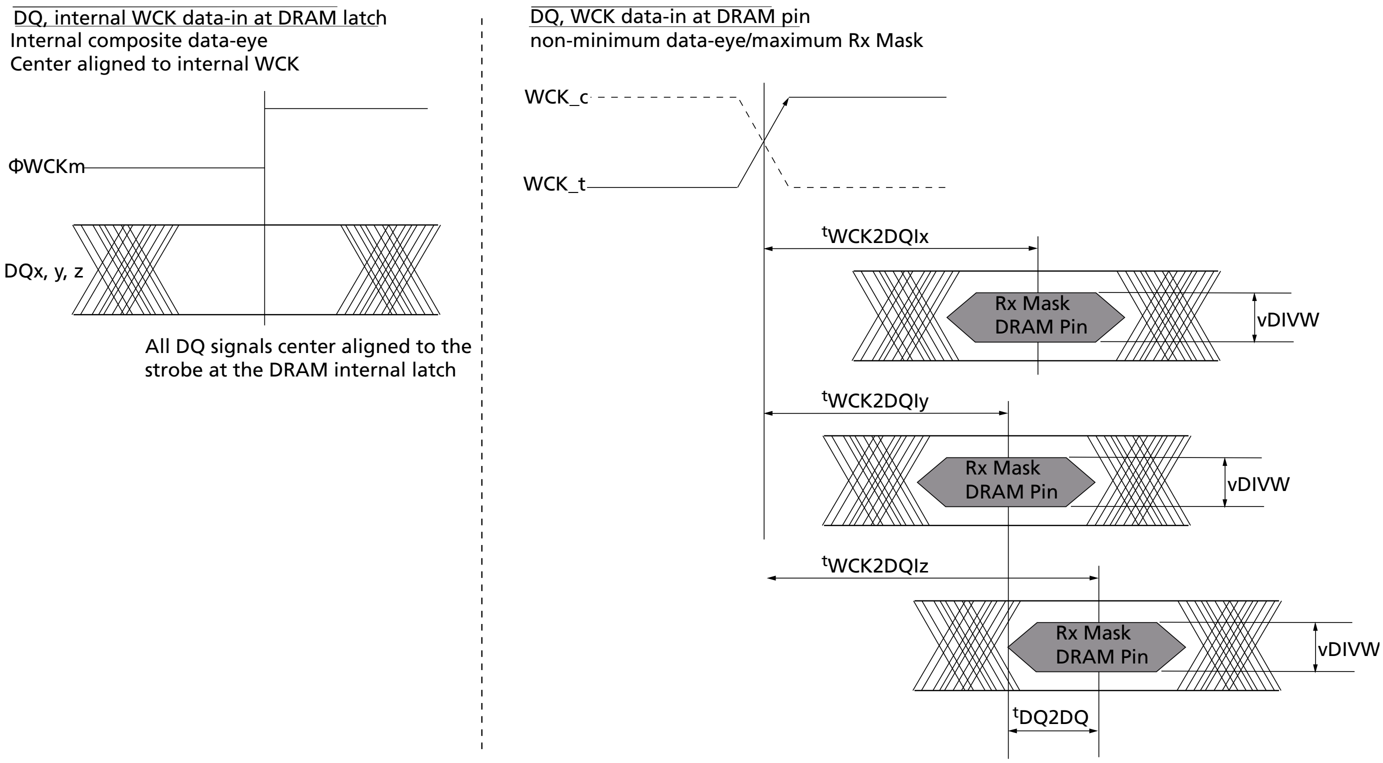


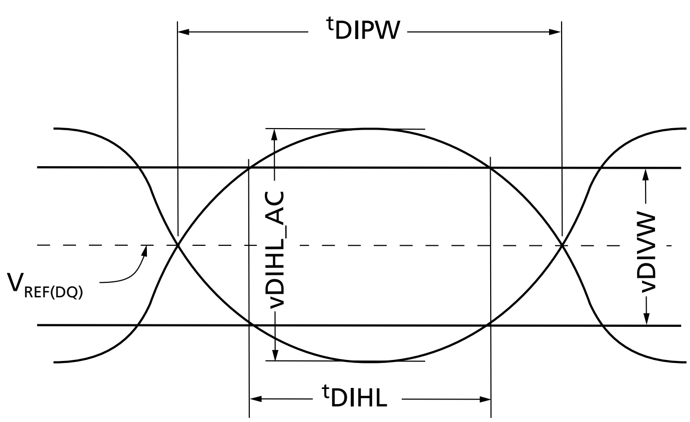
Figure 33: DQ to WCK, ^{t}WCK2DQI, and ^{t}DQ2DQ Timing at the DRAM Pins Referenced from the Internal Latch.



Notes: 1. ^{t}WCK2DQI is measured at the center (midpoint) of the ^{t}DIVW window.
2. DQIz represents the max ^{t}WCK2DQI in this example.
3. DQIy represents the min ^{t}WCK2DQI in this example.

DQ, DMI, Parity and DBI Rx single pulse definition is shown below.

Figure 34: DQ, DMI, Parity, and DBI Rx Single Pulse Definition



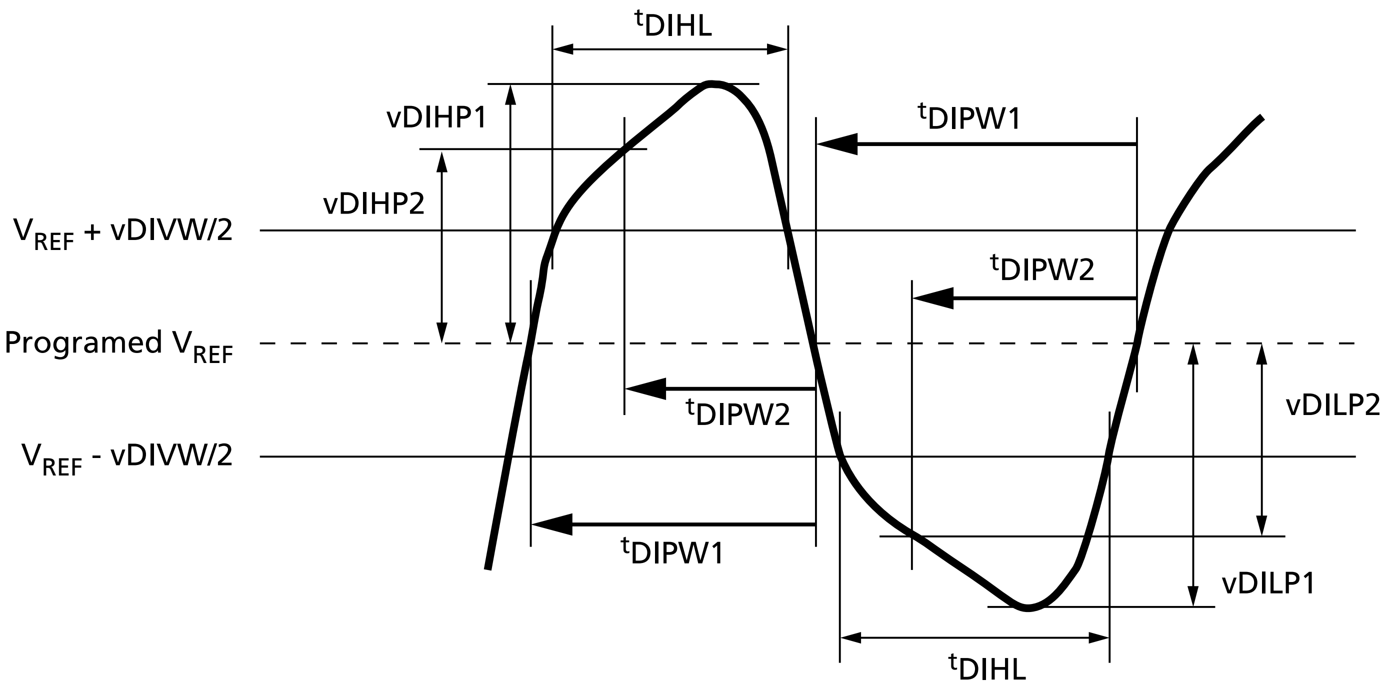
Notes: 1. Single pulse includes any cycle of pulse.
2. $V_{REF(DQ)}$ is a calculated value based on V_{DDQ} and MR14/MR15.

Table 117: DQ, DMI, Parity, and DBI Rx Mask and Single-Pulse Specification

Item	Symbol	Min/ Max	WCK Frequency (MHz)														Unit	Note
			266[8]	533	800	1067	1375	1600	1867	2134	2400	2750	3000	3200	3750	4266		
Rx mask																		
DQ Rx mask height	vDIVW	Min	100												80		mV	1, 2, 6
DQ Rx mask width at $V_{REF(DQ)}$	$^tDIVW1$	Min	0.35												0.35		UI	1, 6
DQ Rx mask width at vDIVW	$^tDIVW2$	Min	0.18												0.18		UI	1, 6
Rx single pulse																		
DQ Rx pulse amplitude	vDIHL_AC	Min	140												N/A		mV	3, 5
DQ Rx pulse width	^tDIPW	Min	0.45												N/A		UI	4, 5
DQ Rx pulse width above/below vDIVW	^tDIHL	Min	0.25												N/A		UI	4, 5
DQ V_{REF}																		
DQ V_{REF}	$V_{REF(DQ)}$	Max	225												180		mV	
		Min	75														mV	
DQ to DQ Offset	^tDQ2DQ	Max	30												TBD		ps	7

Notes:
1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBDmV peak to peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. DQ single-input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI. vDIHL AC is the peak-to-peak voltage centered around $V_{REF(DQ)}$ such that the vDIHL_AC/2 minimum has to be met both above and below $V_{REF(DQ)}$.
4. The DQ-only minimum input pulse width is defined at the $V_{REF(DQ)}$.
5. Refer to LPDDR5X single pulse spec section for Pulse definition for 3750MHz and 4255 MHz.
6. Mask specifications ($^tDIVW1$, $^tDIVW2$ and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
7. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 266 MHz for all speed bins. For example $^tDIVW1$ (ns) = 656.7ps at or below 266 MHz WCK frequency.

Figure 35: LPDDR5X DQ Single Pulse Definition



Note: 1. vDIHL_AC/2 = vDIHP1 = vDILP1. Programmed V_{REF}DQ is defined as percentage of MR14/15 code * V_{DDQ}.

Table 118: DQ Single Input Pulse

Item	Symbol	Min/ Max	WCK Frequency (MHz) 3750	4266	Unit	Notes
DQ Rx pulse width at V_{REF} DQ	$^tDIPW1$	Min	0.45		UI	1
DQ Rx pulse reference	$^tDIPW2$	Min	0.26		UI	1
DQ Rx pulse width at V_{REF} DQ +/- vDIVW/2	^tDIHL	Min	0.21		UI	1
DQ Rx pulse amplitude from programmed V_{REF} DQ	vDIHP1	Min	70		mV	
	vDILP1	Max	–70		mV	
DQ Rx early pulse amplitude from programmed V_{REF} DQ	vDIHP2	Max	55		mV	
	vDILP2	Min	–55		mV	

Notes: 1. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code * V_{DDQ}.

DQ and DQS Output Timing

Table 119: READ AC Timing

Parameter	Symbol	Min/Max	Value	Unit
RDQS_c low-impedance time from CK_t, CK_c	$^tLZ(RDQS)$	Min	(RL × ^{t}CK) + ^{t}WCK2CK (Min) + ^{t}WCK2DQO (Min) - (^{t}RPRE (Max) × ^{t}CK) - TBD	ps

Table 119: READ AC Timing (Continued)

Parameter	Symbol	Min/Max	Value	Unit
RDQS_c high-impedance time from CK_t, CK_c	^{t}HZ(RDQS)	Max	(RL × ^{t}CK) + ^{t}WCK2CK (Max) + BL/n_min + (RPST (Max) × ^{t}CK) - TBD	ps
DQ low-impedance time from CK_t, CK_c	^{t}LZ(DQ)	Min	(RL × ^{t}CK + ^{t}WCK2CK (Min) + ^{t}DQSQ (Min) - TBD	ps
DQ high-impedance time from CK_t, CK_c	^{t}HZ(DQ)	Max	(RL × ^{t}CK) + ^{t}WCK2CK (Max) + ^{t}WCK2DQO (Max) + BLn_min - TBD	ps

Table 120: DQ and DQS Output Timing

Notes 1 applies to entire table.

Parameter	Symbol	Data Rate (Mb/s)				Unit	Note
		3200/5500/6400		7500/8533			
		Min	Max	Min	Max		
RDQS_t/_c to DQ skew per byte group	^{t}DQSQ	-	0.26	-	0.33	UI	1, 2, 3, 4, 7, 8
DQ eye width per pin	^{t}QW	^{t}WCKH/L(abs) (Min) – 0.17	-	^{t}WCKH/L(abs) (Min) – 0.17	-	UI	1, 2, 5, 7, 8
Average 1UI jitter of RDQS (Duty-Cycle jitter)	^{t}jitRD-QS_1UI(avg)	-0.017	0.017	-0.017	0.017	UI	
Absolute 1UI jitter of RDQS	^{t}jitRD-QS_1UI(abs)	-0.039	0.039	-0.039	0.039	UI	1, 2, 6, 7, 8
Absolute 2UI jitter of RDQS	^{t}jitRD-QS_2UI(abs)	-0.03	0.03	-0.03	0.03	UI	1, 2, 6, 7, 8
Absolute 3UI jitter of RDQS	^{t}jitRD-QS_3UI(abs)	-0.056	0.056	-0.056	0.056	UI	1, 2, 6, 7, 8
Absolute 4UI jitter of RDQS	^{t}jitRD-QS_4UI(abs)	-0.035	0.035	-0.035	0.035	UI	1, 2, 6, 7, 8
Remainder of absolute 1UI jitter of RDQS with average 1UI jitter removed	^{t}jitRDQS_1UI	-0.022	0.022	-0.022	0.022	UI	1, 2, 6, 7, 8, 9
Remainder of absolute 3UI jitter of RDQS with average 1UI jitter removed	^{t}jitRDQS_3UI	-0.039	0.039	-0.039	0.039	UI	1, 2, 6, 7, 8, 10

Notes: 1. These parameters are defined over voltage and temperature after DCA.
2. These parameter value is defined after duty cycle adjustment is applied.
3. These parameters are a function of WCK input clock jitter ^{t}WCKH and ^{t}WCKL. Note for ^{t}WCKL(abs)min of 0.43tck = 0.86 UI
4. These parameters are defined as min/max across all DQ pins per byte group. This includes the across pin variation within a byte group.
5. Equation applies to ^{t}WCKH/L(abs) MIN = 0.43 ...0.46^{t}WCK. If tWCKH/L(abs) MIN >= 0.46^{t}WCK then ^{t}QW = 0.75UI. Example1: If ^{t}WCKH/L(abs) MIN is 0.43tWCK then tQW MIN = tWCKH/L(abs) MIN - 0.17 UI = 0.86 UI - 0.17UI = 0.69UI.

Example2: If ^{t}WCKH/L(abs) MIN is 0.46tWCK then tQW MIN = tWCKH/L(abs) MIN - 0.17 UI = 0.92 UI - 0.17UI = 0.75UI.
Example3: If ^{t}WCKH/L(abs) MIN is 0.48tWCK then tQW MIN = 0.75UI.

6. This parameter is defined as ^{t}jitRDQS_NUI = ^{t}RDQS_NUI – N*UI where N= 1,2,3,4 and UI is the unit interval. Example ^{t}jitRDQS_2UI= ^{t}RDQS_2UI – 2*UI.
7. When operating in WCK low frequency mode (MR18 OP[3]=0b), <3200 data rate timing parameters are applied.
8. When operating in WCK high frequency mode (MR18 OP[3]=1b), 3200/5500/6400 data rate timing parameters are applied.
9. ^{t}jitRDQS_1UI MAX = ^{t}jitRDQS_1UI(abs) MAX - ^{t}jitRDQS_1UI(avg) MAX; ^{t}jitRDQS_1UI MIN = ^{t}jitRDQS_1UI(abs) MIN - ^{t}jitRDQS_1UI(avg) MIN
10. ^{t}jitRDQS_3UI MAX = ^{t}jitRDQS_3UI(abs) MAX - ^{t}jitRDQS_1UI(avg) MAX; ^{t}jitRDQS_3UI MIN = ^{t}jitRDQS_3UI(abs) MIN - ^{t}jitRDQS_1UI(avg) MIN

DQ NUI Tx Jitter Specification

DQ-to-RDQS Differential Jitter

The DRAM DQ-to-RDQS differential jitter is defined to support both SOC matched and unmatched DQ-RDQS input receiver (Rx) types over number of UI (NUI) of mismatch. All output timings are referenced to RDQS for source synchronous timing relationships. The appropriate RDQS preamble mode must be selected to support the unmatched SOC Rx. It is the responsibility of the SOC and the system to ensure that the advanced RDQS preamble edges are robust for system operation.

The NUI DQ-to-RDQS output timing is defined as ^{t}RDQS_NUI in conjunction with ^{t}DQSQ, where NUI defines the number of UI that RDQS shifts from the corresponding DQ as shown in the figure below.

Figure 36: NUI DQ-to-RDQS Output Timing Definition

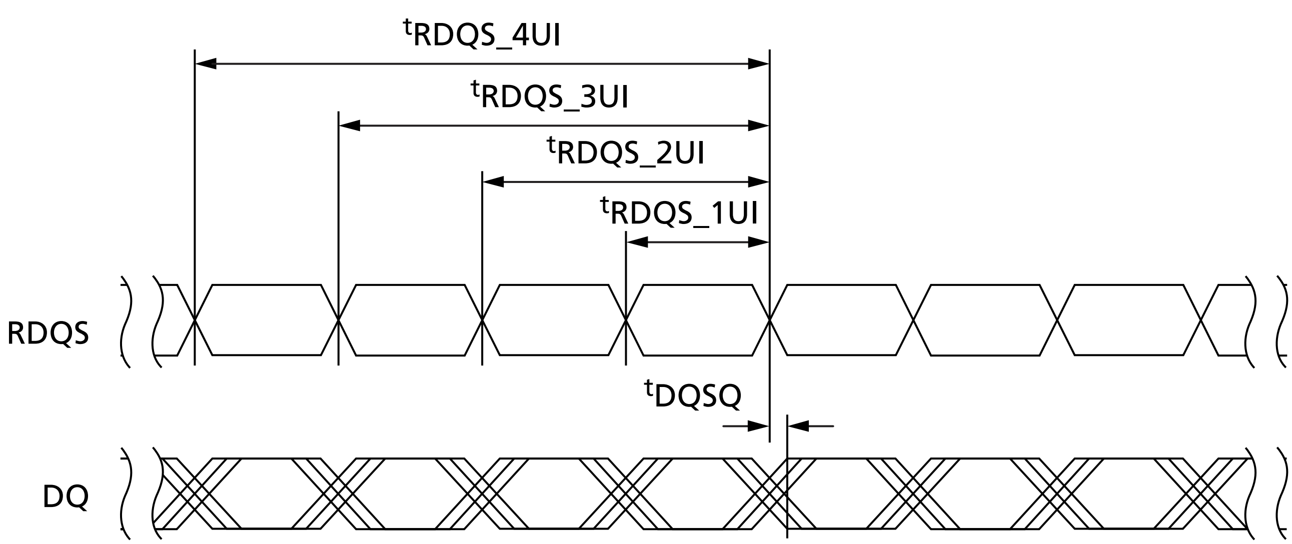
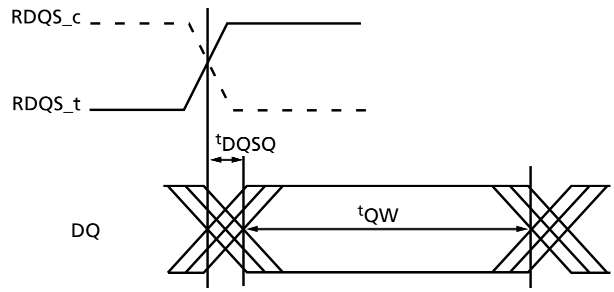
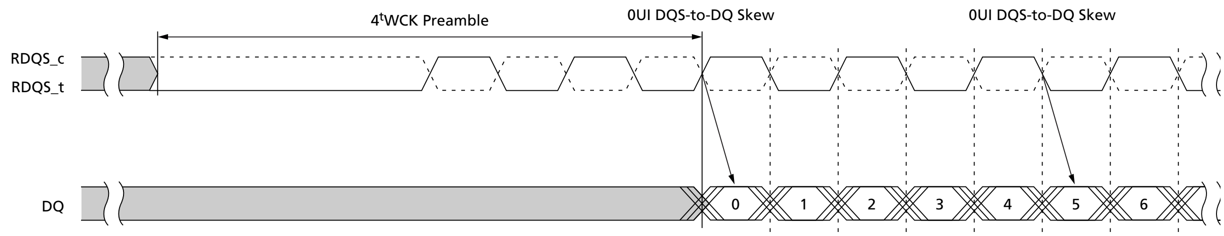


Figure 37: DQ eye width per pin (^tQW)



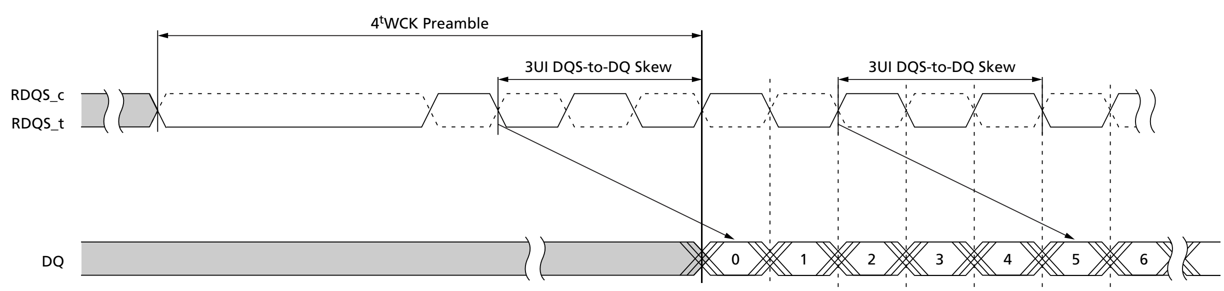
The figures below include examples of 0 and 3UI mismatch using the 4 ^{t}WCK RDQS read preamble of 2^{t}WCK static + 2^{t}WCK toggle.

Figure 38: Read Burst Example for Pin DQx Depicting Bits 0 and 5 Relative to the RDQS Edge for 0 UI Mismatch



Note: It is the responsibility of the SOC and system to ensure the advanced RDQS preamble edges are robust for system operation.

Figure 39: Read Burst Example for Pin DQx Depicting Bits 0 and 5 Relative to the RDQS Edge for 3 UI Mismatch



Note: It is the responsibility of the SOC and system to ensure the advanced RDQS preamble edges are robust for system operation.

Input/Output Capacitance

Table 121: Input/Output Capacitance

Parameter	Symbol	Min/ Max	Data Rate (Mb/s)			Unit	Note
			533–5500	6400	7500-8533		
Input capacitance, CK_t and CK_c	CCK	Min	0.3	0.3	0.3	pF	1, 2
		Max	1.4	0.8	0.8		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	0.0	0.0	pF	1, 2, 3
		Max	0.09	0.09	0.09		
Input capacitance, WCK_t and WCK_c	CWCK	Min	0.3	0.3	0.3	pF	1, 2
		Max	1.0	0.9	0.8		
Input capacitance delta, WCK_t and WCK_c	CDWCK	Min	0.0	0.0	0.0	pF	1, 2, 4
		Max	0.09	0.09	0.09		
Input capacitance, all other input-only pins	CI	Min	0.3	0.3	0.3	pF	1, 2, 5
		Max	1.4	0.8	0.8		
Input capacitance delta, all other input-only pins	CDI	Min	-0.1	-0.1	-0.1	pF	1, 2, 6
		Max	0.1	0.1	0.1		
Input/output capacitance, DQ and DMI	CIO	Min	0.3	0.3	0.3	pF	1, 2, 7
		Max	1.0	0.9	0.8		
Input/output capacitance delta, DQ and DMI	CDIO	Min	-0.1	-0.1	-0.1	pF	1, 2, 9
		Max	0.1	0.1	0.1		
Output capacitance, RDQS_t and RDQS_c	COO	Min	0.3	0.3	0.3	pF	1, 2
		Max	1.0	0.9	0.8		
Output capacitance delta, RDQS_t and RDQS_c	CDOO	Min	0.0	0.0	0.0	pF	1, 2, 8
		Max	0.1	0.1	0.1		
Input/output capacitance, ZQ pin	CZQ	Min	0.0	0.0	0.0	pF	1, 2
		Max	5.0	5.0	5.0		

Notes:
1. This parameter applies to the die device including IO capacitance and RDL if needed (does not include package capacitance, such as the bond wire).
2. This parameter is not subject to production tests. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SS} applied and all other pins floating).
3. Absolute value of CCK_t-CCK_c.
4. Absolute value of CWCK_t-CWCK_c.
5. CI applies to CS CA[6:0].
6. CDI = CI - 0.5 × (CCK_t + CCK_c).
7. DMI loading matches DQ.
8. Absolute value of CRDQS_t-CRDQS_c.
9. CDIO = CIO – Average(CDQn, CDMI) in byte-lane.

Revision History

Rev. G – 04/2022

- Updated note in Recommended DC Operating Conditions
- Added table: Pull-Down Driver Characteristics in enhanced DVFSC Mode
- Added table: Unterminated Pull-Up Characteristics in enhanced DVFSC mode
- Table update: IDD Specification table
- Multiple tables updated to add LPDDR5X speed range values:
  – CK Differential Input Voltage Timing
  – Clock Single-Ended Input Voltage
  – Differential Input Level for CK_t, CK_c
  – Differential Input Slew Rate for CK_t, CK_c
  – Cross Point Voltage for Differential Input Signals (CK)
  – WCK Differential Input Voltage
  – WCK Single-Ended Input Voltage
  – Differential Input Level for WCK_t, WCK_c
  – Differential Input Slew Rate for WCK_t, WCK_c
  – Cross Point Voltage for Differential Input Signals (WCK_t, WCK_c)
  – tWCK to CK/DQ Offset Rank-to-Rank Variation
- Table update: LPDDR5X Core AC Timing table updated to add E-DVFSC enabled values
- Temperature De-Rating AC Timing update
- Table update: Mode Register Read/Write AC Timing table update, added tMRD_L,tMRW_L
- Table update: WCK Oscillator Matching Error Specification for Low-Frequency Mode

Rev. F – 10/2021

- Added new table: Core AC Timings for LPDDR5X
- Command Bus Training AC Timing Table update, splitting the table into table for mode 1 and table for mode 2
- Table update: DQ, DMI, Parity, and DBI Rx Mask and Single-Pulse Specification
- New section: LPDDR5X DQ single input pulse definition

Rev. E – 12/2020

Update to reflect latest JEDEC or adding LPDDR5X parameters

- Absolute Maximum DC rating table update
- Recommended DC operating conditions table update
- Deleteing tFC_middle parameter
- tWCK2DQ AC timing Parameters table update
- New table: WCK stop AC timing
- New Table : NT-ODT AC timing
- Clock AC timing table update
- Write Data Clock AC timing table update
- CA Rx specifications table update
- DQ, DMI, Parity, and DBI Rx Mask and Single-Pulse Specification table update
- DQ and DQS Output Timing table update
- Input/Output Capacitance table update

Rev. D – 04/2020

- Core AC timings: Text change from Link ECC to Write Link ECC
- Input leakage current table update
- Added tOSCPD to power down AC timing table
- tPDN spec. update
- Changed tWCK2DQI_LF max value from 900ps to TBD
- tWCK2DQI_ rank2rank max, tWCK2DQO_ rank2rank max LF mode spec update
- Added Table : WCK2DQI/WCK2DQO Interval Oscillator AC Timing
- Typo correction for tWR2WCK: Min spec to Max spec
- Typo correction for tWCK(avg) max value
- DQ and DQS Output timing table update

Rev. C – 02/2020

All the updates are based on JEDEC JESD209-5A except Temperature Derating AC Timing Table.

- Recommended DC operating condition table
- Added ESD specification table
- Added Differential Output Slew Rate table
- Updated Temperature Derating AC Timing Table. (JEDEC spec. is still TBD)
- Added Notes to Table 59
- Added tXDSM_XP, tPDECSODTOFF, tPDXCSODTON in Table60
- Added VREFCA update timing table
- Added VREFDQ update timing table
- Updated WCK2CK Leveling Timing Parameters Table
- Updated WCK Oscillator Matching Error Specification for HF Mode Table
- Updated WCK Oscillator Matching Error Specification for LF Mode Table
- Updated Command Bus Training AC Timing Table
- Added Enhanced WCK Always On Mode Timing Table
- VREFCA value update
- tQW value update
- Updated legal status to Production

Rev. B – 04/2019

- Typo correction: VREFCAmax 350-->367mV
- Typo correction: VDQSR2 0.5-->4.8 mV/us
- data pattern correction for IDD4R DBI off Pattern B BL1
- Unit correction SRIdiff_WCK
- Unit correction VWCKIVW,tWCKHL,SRIWCKSE
- tPDN spec TBD-->10ns,1nCK
- correction tWLDQOFF min-->max
- tWCK to CK/DQ offset rank to rank variation table update
- 4 new spec added to CBT: tXCBT,tCBTWCKODTFIX,tCBTODTOFF,tCBTNTODTOFF
- DQ and DQS output timing: TBD spec fixed
- Added single ended CK/WCK input voltage specification for differential mode and reorganized section order.

Rev. A – 01/2019

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.