Silicon Creations

Jitter Analysis Document

Application Note Addendum

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SILICON CREATIONS LLC., 49 Highway 23 NE, Suwanee, GA 30024.

For support email support@siliconcr.com

1 Contents

Contents

1 Contents **2**

2 Jitter Overview **5**

3 Statistical Nature of Jitter **6**

4 Period Jitter **8**
4.1 Random jitter . . . 8
4.2 Supply noise jitter . . . 10
4.3 Reference Rate Correction Jitter . . . 15
4.3.1 Period Jitter Transfer . . . 15
4.3.2 Integrated Reference Clock Phase Noise (1A) . . . 16
4.3.3 Supply Noise Jitter . . . 16
4.3.4 Fixed Offset (4) . . . 17
4.3.5 Random Long Term Jitter (5) . . . 17
4.3.6 Total Reference Rate Jitter . . . 17
4.4 Total Period Jitter . . . 18

5 Cycle-to-cycle Jitter **19**

6 Long Term Jitter **20**
6.1 Random jitter . . . 20
6.2 Supply noise jitter . . . 22
6.2.1 Long term jitter from VCO supply noise . . . 23
6.2.2 Long Term jitter from Output path supply noise . . . 28
6.2.3 Long Term jitter from Reference path supply noise . . . 28
6.3 Total Long term Jitter . . . 29

7 Reference Clock Guidelines **29**
7.1 Reference Clock Duty-Cycle: . . . 29
7.2 Period Jitter Limit (PJ): . . . 30
7.3 Long term Jitter Limit (LTJ): . . . 30
7.4 Frequency Tolerance: . . . 30
7.5 Signal Levels: . . . 31
7.6 General Guidelines: . . . 31

8 Appendix **32**

8.1 Period Jitter (PJ) . . . 32
8.2 Cycle-to-Cycle Jitter (CCJ) . . . 32
8.3 Long Term Jitter (LTJ), Accumulated jitter, phase jitter, N-cycle jitter . . . 32
8.4 Time-Interval Error (TIE) . . . 33

List of Figures

1 Two common jitter measurements . . . 5
2 Random period jitter with thermal noise . . . 8
3 Random period jitter specified in datasheet for Case 1 . . . 8
4 Random period jitter with 1/f noise . . . 9
5 Random period jitter specified in datasheet for Case 2 . . . 9
6 Typical PLL output clock path . . . 10
7 Typical PLL output path delays . . . 11
8 Typical supply noise waveform . . . 11
9 PLL output path delay variation with supply noise . . . 12
10 Output path delay and sensitivity specified in the datasheet . . . 12
11 PLL output path delay variation with supply noise . . . 13
12 External clock path included . . . 14
13 Reference Rate Noise Components of a Generic PLL . . . 15
14 PLL Phase Noise Plot . . . 16
15 Cycle to cycle jitter . . . 19
16 Effect of spread spectrum modulation . . . 19
17 Random Long time Jitter vs. VCO frequency . . . 20
18 Random Long Term jitter specified in the datasheet . . . 20
19 Random Long Term Jitter in time domain . . . 21
20 Random Long Term Jitter in frequency domain . . . 21
21 Integrated jitter specified in datasheet . . . 22
22 Long Term jitter due to output clock path . . . 22
23 Long Term Supply Noise Sensitivity . . . 23
24 Supply Noise in mV . . . 24
25 Supply Noise Sensitivity specified in datasheet . . . 24
26 Supply Noise in period . . . 24
27 Phase error due to supply noise . . . 25
28 Supply noise, brick-wall high-pass filtered supply noise . . . 25
29 Supply Noise in mV . . . 26
30 Period Variation due to supply noise . . . 26
31 Phase error due to supply noise . . . 27
32 Reference clock path . . . 28
33 Reference clock path delay . . . 29

34 Reference Clock Duty Cycle 29
35 Reference Clock Period Jitter 30
36 Reference Clock Long Term Jitter 30
37 Reference Clock Frequency Tolerance 30
38 Connecting PLL with different core supply voltage 31
39 Period Jitter 32
40 Long Term Jitter 32

List of Tables

1 Double-sided sigma probabilities up to 10σ 7
2 Sample size vs. Sigma (σ) confidence level 7

2 Jitter Overview

PLL datasheets may specify multiple types of jitter. The following diagram shows a simple process for deciding which type of jitter is relevant.

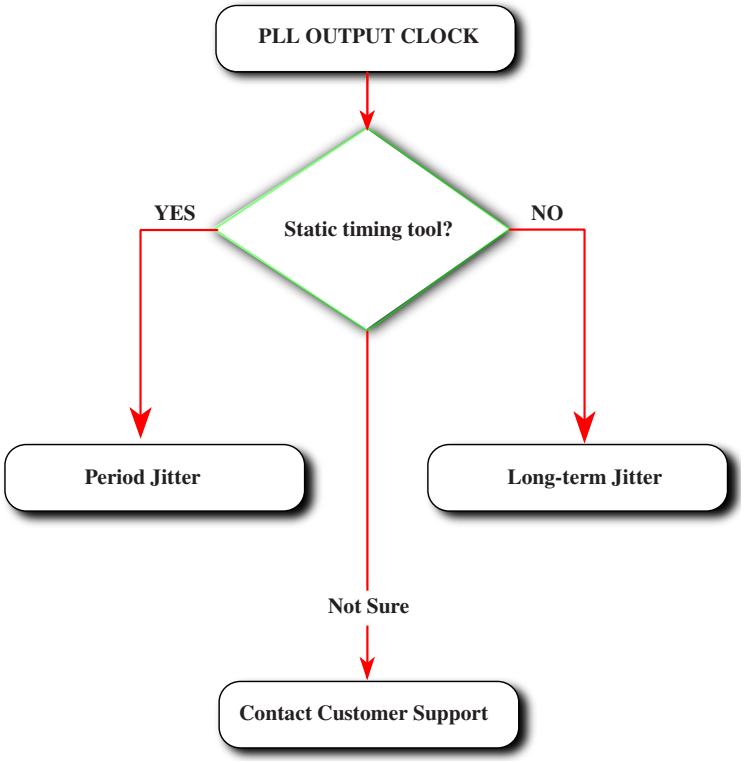

Figure 1: Two common jitter measurements

- **Period Jitter**
  - Defines clock uncertainty for static timing
  - Consists of multiple components
    - Random
      - Statistical methods used to estimate
      - ± 6 to 8 sigma used to bound the worst-case peak-peak jitter
    - Supply-noise induced
    - Reference Spur

- Can be measured in time or frequency domain
- Common Applications
  - Digital Logic, Processor and memory clocks
  - Synchronous interface, Synchronous timing

- **Long term Jitter (LTJ)**
  - Relevant for circuits sensitive to accumulated phase error
  - Consists of multiple components
    - Random
      - Typically defined in RMS value
    - Supply-noise induced
    - Reference clock phase jitter
  - Can be measured in time or frequency domain
    - Time domain measurements must define hold off times
      - Several hundreds of reference clock periods is common
    - Frequency domain jitter is measured as integral of phase noise
      - Integration range based on application
      - Filter may be applied to phase noise before integration for some applications
  - Common Applications
    - Serdes & Data Converter applications
    - CODEC's and RF communications
    - Timing between asynchronous clock domains

3 Statistical Nature of Jitter

Jitter has a significant statistical component when random noise is involved. If a large number of samples are measured, the jitter will have a deterministic component which is bounded, and a random component which usually holds to a normal Gaussian distribution. Random RMS jitter is the value of 1σ of the random, or unbounded portion of this distribution. A

common approximation of peak-to-peak jitter is ±6*RMS, which results in about 1 part out of 1 billion being outside of the boundary.

Table 1 below shows the percentage of samples that are within the distribution up to the sigma value.

Table 1: Double-sided sigma probabilities up to 10σ

Sigma	Probabilities (Double-Sided)
1	68.26%
2	95.45%
3	99.73%
4	100% – 6.334E-3% = 99.993666%
6	100% – 1.973E-7%
7	100% – 2.56E-10%
8	100% – 1.244E-13%
10	100% – 1.524E-21%

Another way to view the probability is to look at the sample size required to predict the confidence level for a given value of sigma as shown in Table 2.

Table 2: Sample size vs. Sigma (σ) confidence level

Sample Size	Sigma (σ)
10	±1.282
100	±2.327
1,000	±3.090
10,000	±3.719
100,000	±4.265
1,000,000	±4.754
10,000,000	±5.200
100,000,000	±5.612
1,000,000,000	±5.998
1,000,000,000,000	±7.035
1,000,000,000,000,000	±7.941

4 Period Jitter

Period jitter consists of several components. The dominant components are random noise, supply noise and, reference spur.

4.1 Random jitter

Random jitter depends on VCO frequency and output clock period as shown in the following figures.

Case 1 (Common with dual-voltage, higher BW PLLs):

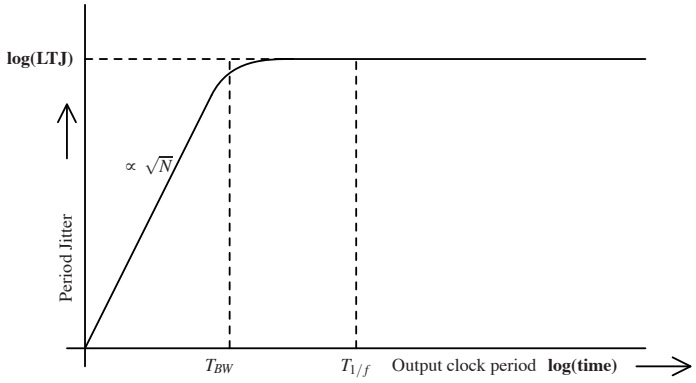

Figure 2: Random period jitter with thermal noise

For $t < T_{BW}$:

$$\text{Jitter} \propto \sqrt{\frac{F_{\text{VCOMAX}}}{F_{\text{VCO}}}} \times \sqrt{\frac{F_{\text{VCOMAX}}}{F_{\text{OUT}}}} \tag{1}$$

For $t \geq T_{\text{BW}}$:

$$\text{Jitter} = \text{Long Term Jitter (LTJ)} \tag{2}$$

Period Jitter (random)	ps (RMS)			1	@ FVCOMax = 1GHz Random jitter scales as $\sqrt{\frac{FVCOMax}{FVCO}} \times \sqrt{\frac{FVCOMax}{FOUT}}$

Figure 3: Random period jitter specified in datasheet for Case 1

PLL datasheet specifies random period jitter. Please refer to datasheet for a specific PLL.

Generic Numerical Example :

- FVCOMAX: 1GHz
- FVCO: 800MHz
- FOUT: 100MHz
- Period jitter specified in datasheet: 1ps
- RMS Jitter at VCO Output: 1ps* $\sqrt{\frac{1000MHz}{800MHz}}$* $\sqrt{\frac{1000MHz}{100MHz}}$ = 3.54ps

From Table 2, for timing error less than 1 in 1 billion samples, the output peak-to-peak (two-sided) random jitter (for $\pm 6\sigma$) = 2*6*3.54ps = 42.48ps

Case 2 (Common with core voltage/LAINT/LBINT PLLs):

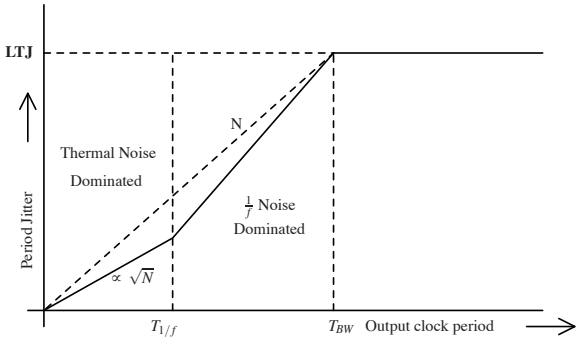

Figure 4: Random period jitter with 1/f noise

For $t < T_{BW}$:

$$\text{Jitter} \propto \sqrt{\frac{F_{\text{VCOMAX}}}{F_{\text{VCO}}}} \times \frac{F_{VCOMAX}}{F_{\text{OUT}}} \tag{3}$$

For $t \geq T_{\text{BW}}$:

$$\text{Jitter} = \text{Long Term Jitter (LTJ)} \tag{4}$$

Period Jitter (random)	ps (RMS)			1	@ FVCOMax = 1GHz Random jitter scales as $\sqrt{\frac{FVCOMax}{FVCO}} \times \frac{FVCOMax}{FOUT}$

Figure 5: Random period jitter specified in datasheet for Case 2

Generic Numerical Example :

- FVCOMAX: 1GHz
- FVCO: 800MHz
- FOUT: 100MHz
- Period jitter specified in datasheet: 1ps
- RMS Jitter at VCO Output: 1ps* $\sqrt{\frac{1000MHz}{800MHz}} * \frac{1000MHz}{100MHz}$ = 11.18ps

From Table 2, for timing error less than 1 in 1 billion samples, the output peak-to-peak (two-sided) random jitter (for $\pm 6\sigma$) = 2*6*11.18ps = 134.16ps

The actual value for each PLL will vary. Refer to the datasheet for a specific PLL.

4.2 Supply noise jitter

Every PLL output path consists of several CMOS components (eg, level shifters, muxes, buffers, dividers etc.). Each element has intrinsic delay proportional to the supply voltage. The figures below shows a typical PLL output clock path and a corresponding timing diagram.

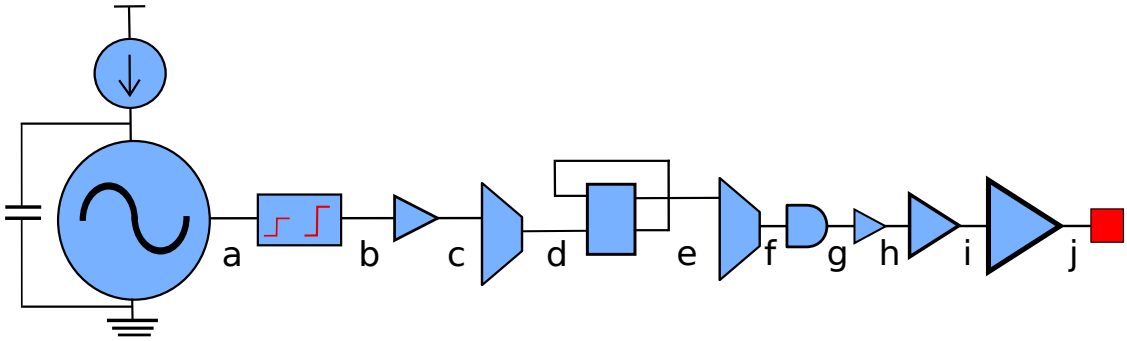

Figure 6: Typical PLL output clock path

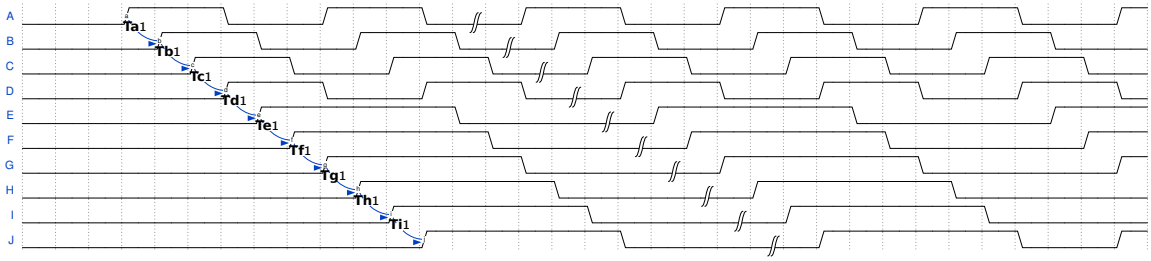

Figure 7: Typical PLL output path delays

Total nominal output path delay $T_{nom} = \sum_a^i T1 = \sum(Ta1 + Tb1 + Tc1 + Td1 + Te1 + Tf1 + Tg1 + Th1 + Ti1)$

On chip supply noise is almost always dominated by switching noise from CMOS logic gates.

Here's an example of supply noise waveform.

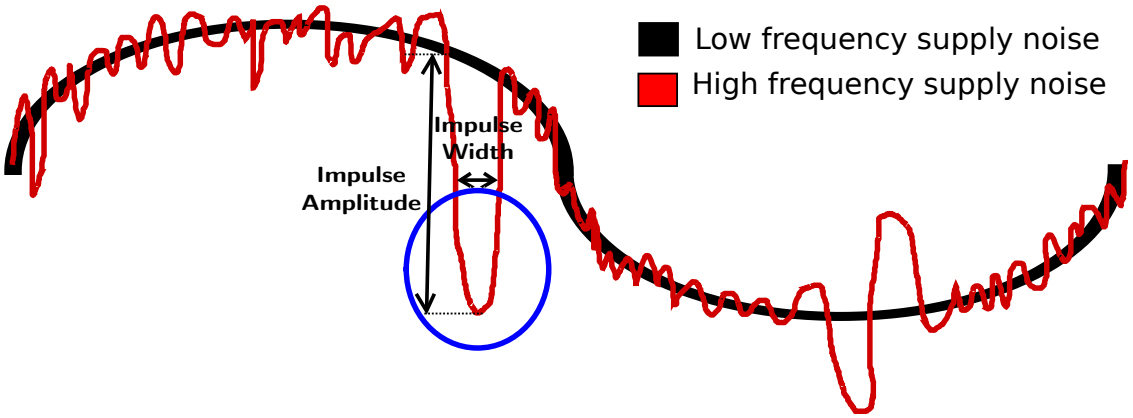

Figure 8: Typical supply noise waveform

The low frequency noise (period longer than propogation delay) does not affect period jitter. Since the voltage does not change much from one edge to the next edge, the delay does not change much.

Supply voltage variations results in delay variations for respective gates. If the value of (VDD-VSS) seen by each logic gate changes from one clock edge to the next, the net change in delay contributes to jitter.

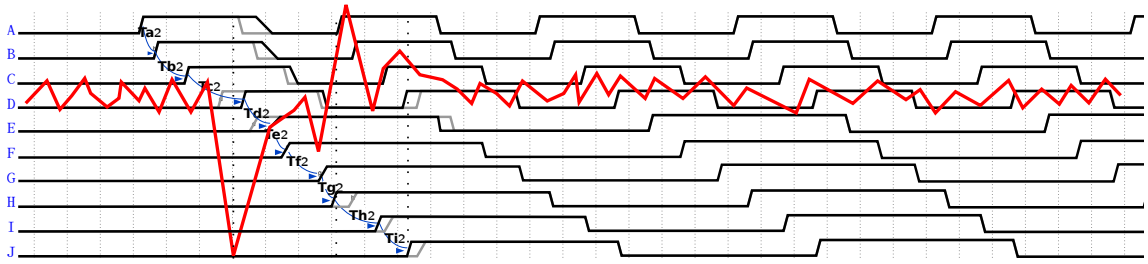

Figure 9: PLL output path delay variation with supply noise

Total output path delay $T_{var} = \sum_a^i T2 = \sum(Ta2+Tb2+Tc2+Td2+Te2+Tf2+Tg2+Th2+Ti2)$

Period Jitter= $\sum_a^i T1$ - $\sum_a^i T2$

For example, if the delay from the first edge and the second edge is the same, then no jitter is added.

Peak-to-peak supply noise jitter can be expressed as:

$$\left(\frac{\text{Noise Impulse width}}{\text{Output path delay}}\right) * \text{Output path delay sensitivity} * \text{Noise Impulse Amplitude} \quad (5)$$

Most PLL datasheets specify output path delay and output path delay sensitivity to supply noise for various output configurations. Here's a generic example:

Total Output delay	ps			100	POSTDIV1=1, POSTDIV2=1
Total Output delay sensitivity	ps/mV			1.0	POSTDIV1=1, POSTDIV2=1
Total Output delay	ps			200	POSTDIV1>1, POSTDIV2=1
Total Output delay sensitivity	ps/mV			2.0	POSTDIV1>1, POSTDIV2=1

Figure 10: Output path delay and sensitivity specified in the datasheet

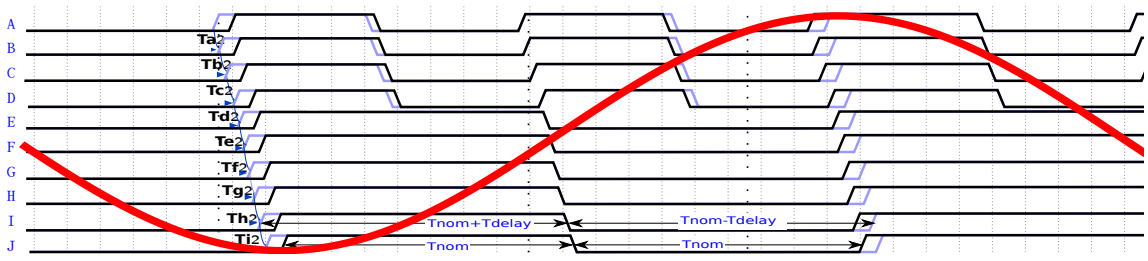

Figure 11: PLL output path delay variation with supply noise

When the pulse-width is not known we should assume the worst-case scenario, which occurs when the pulse edge (or max amplitude) corresponding to the first clock edge followed by the next pulse edge (or min amplitude) corresponding to the next clock edge, as shown in Figure 11.

In such a case the delay variation can be seen as

(Tnom + Δdelay) − (Tnom − Δdelay) = 2∗Output path delay sensitivity

Generic Numerical Example 1 (Typical Case):

- Impulse Width = 50ps
- Output path delay = 100ps
- Output path delay sensitivity = 1ps/mV
- Impulse Amplitude = 50mV
- Peak-to-peak supply noise jitter: $\frac{50\text{ps}}{100\text{ps}} * 1\ \frac{\text{ps}}{\text{mv}} * 50\text{mV} = 25\text{ps}$

Generic Numerical Example 2 (Worst Case):

- Noise: Sine wave @ $\frac{\text{Fout}}{2}$
  - peaks and valleys aligned to clock transitions (figure above)
- Output path delay sensitivity = $1\ \frac{\text{ps}}{\text{mv}}$
- Noise Amplitude = 50mV
- Peak-to-peak supply noise jitter: $2 * 1\ \frac{\text{ps}}{\text{mv}} * 50\text{mV} = 100\text{ps}$

Note that worst-case results in twice the delay sensitivity. In practice, this scenario has rarely observed but mentioned here to show a theoretical worst-case condition.

Generic Numerical Example 3:

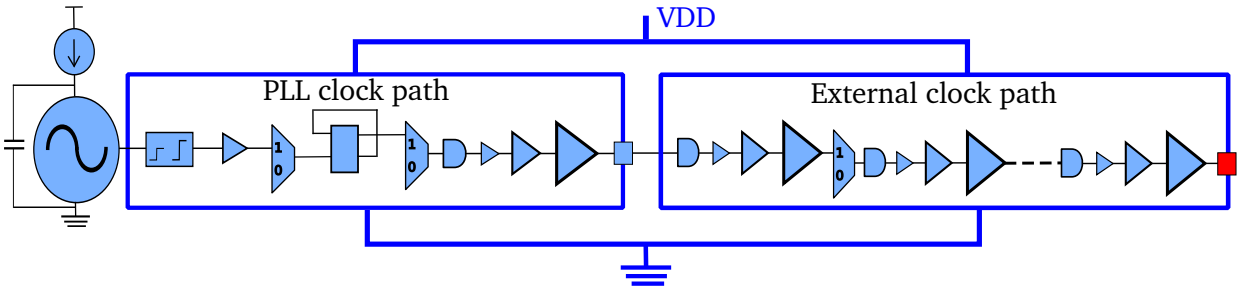

Figure 12: External clock path included

It is often the case that the external clock tree delay is much larger than the PLL clock path delay. In such a case the resultant peak-to-peak period jitter may be expressed as follows:

$$\left(\frac{\text{PLL clock path delay + External clock delay}}{\text{External clock tree delay}}\right) * \text{External clock tree jitter} \qquad (6)$$

- PLL clock path delay = 100ps
- External clock path delay = 1ns
- External clock path jitter = 50ps
- Peak-to-peak supply noise jitter: $\left(\frac{1ns+100ps}{1ns}\right)$ * 50ps = 55ps

4.3 Reference Rate Correction Jitter

Reference rate correction jitter consists of four dominant components. These are reference clock jitter, fixed offset, VDDHV supply noise jitter and intrinsic PLL jitter.

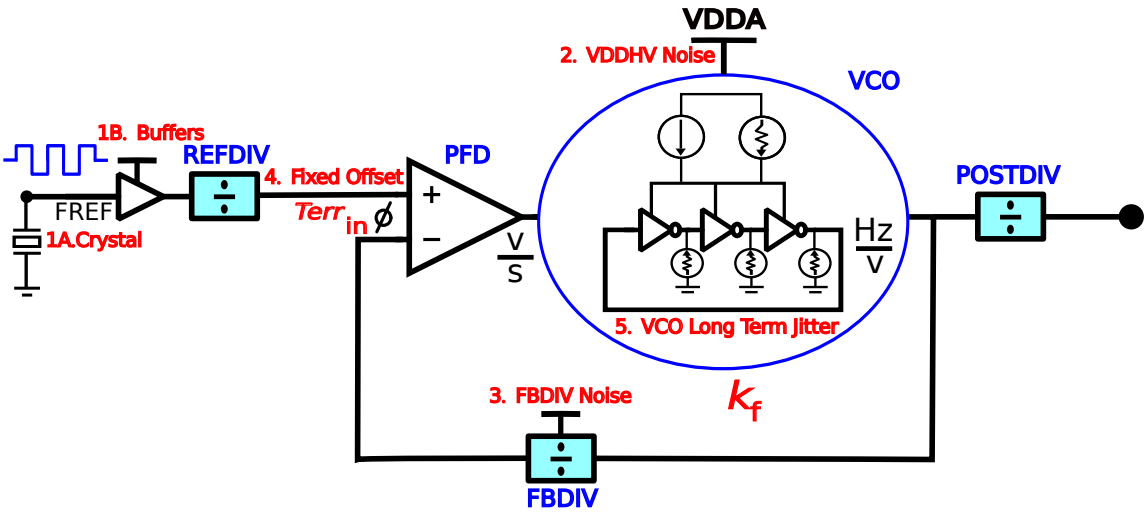

Figure 13: Reference Rate Noise Components of a Generic PLL

4.3.1 Period Jitter Transfer

Period Jitter Transfer is defined as a short term change in period at VCO output due to a short term change at PFD input (T_{err}). For cases where input phase error is equal or larger than VCO period, this analysis may be pessimistic.

$$\text{Period Jitter Transfer} = Terr_{\text{in}} * K_{\text{f}} \tag{7}$$

where K_f is the forward-path gain of the PLL and is specified in the datasheet for specific PLLs.

$$\text{Total Period Jitter} = Terr_{\text{in}} * K_{\text{f}} * POSTDIV \tag{8}$$

- POSTDIV is the divide ratio of the output clock divider

4.3.2 Integrated Reference Clock Phase Noise (1A)

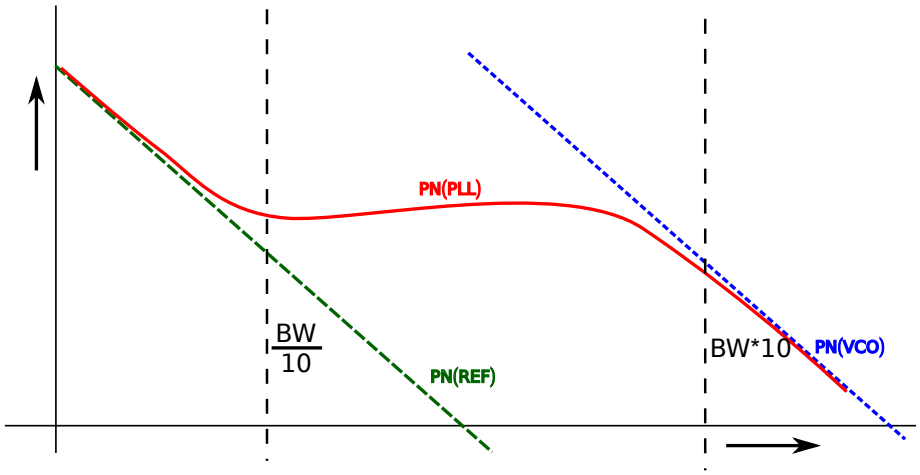

Figure 14: PLL Phase Noise Plot

Reference clock random jitter is the integration of reference clock phase noise from decade below PLL bandwidth to Nyquist rate (i.e. FREF/REFDIV/2).

4.3.3 Supply Noise Jitter

4.3.3.1 Reference Clock Buffers (1B)

Reference clock buffer noise can be included in the reference clock phase noise measurements(1A) if data is available or it can be estimated as approximately 5% of total on-chip reference buffer delay.

Generic Numerical Example:

- Total buffer delay : 10ns
- Jitter from reference buffers (5% of total delay) : 50ps

4.3.3.2 VDDHV (VCO) Supply Noise (2)

For Long term jitter from VCO supply noise, refer to Section 6.2.1. From the generic numerical example 1, VCO supply noise is 159fs RMS, peak jitter (for 6σ) is 0.954ps. For reference rate correction calculations, peak should be considered.

4.3.3.3 Feedback Divider (3)

Jitter due to VDDREF noise is typically too small to consider.

4.3.4 Fixed Offset (4)

Most PLLs have a fixed offset. If it is a significant contributor to the period jitter, it is specified in the datasheet.

4.3.5 Random Long Term Jitter (5)

For random long term jitter, refer to Section 6.1. From the generic numerical example 1, random long term jitter is 1.11ps RMS, peak jitter (for 6σ) is 6.66ps. For reference rate correction calculations, peak should be considered.

4.3.6 Total Reference Rate Jitter

Total reference rate period jitter can now be calculated from the previously defined components.

Peak Reference Rate Jitter = [Sum of all Components] * $K_f * POSTDIV$

Generic Numerical Example:

- 1A. Integrated reference phase noise jitter = 10ps
- 1B. Reference buffer noise = 50ps
- 2. VDDHV Supply noise jitter = 0.954ps
- 4. Fixed offset = 10ps
- 5. Random long term jitter = 6.66ps
- K_{PLL} = 0.015
- POSTDIV = 10
- Total Peak Reference Rate Jitter: [10ps + 50ps + 10ps + 6.66ps + 0.964ps] * 0.015 * 10 = 11.64ps

This calculation is valid for condition where $Terr_{in} << T_{vco}$.

4.4 Total Period Jitter

For STA, we consider one-sided Peak Period Jitter.

Peak Period Jitter = Peak Random Jitter + Peak Supply Noise jitter + Peak Reference Rate Jitter

Generic Numerical Example:

- FVCOmax = 1000MHz
- Fout = 100MHz
- Peak Random jitter = 21.24ps
- Peak Supply noise jitter (typical case) =12.5ps
- Peak reference rate jitter= 2.33ps
- Total Peak period jitter: 21.24ps + 12.5ps + 11.64ps = 45.38ps

For STA, in a worst-case scenario, both minimum period (setup time) and maximum period (hold time) could equal to the (one-sided) peak period jitter, as calculated above.

5 Cycle-to-cycle Jitter

Cycle to cycle jitter is the first derivative of period jitter. It is used for systems where there is a large modulation which makes it's impossible to measure period jitter. For example, in the case of a spread spectrum modulation, with a typical 3% spread and 1% period jitter, it's not possible to measure period jitter.

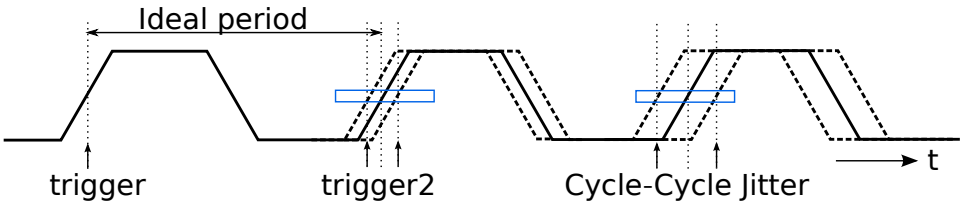

Figure 15: Cycle to cycle jitter

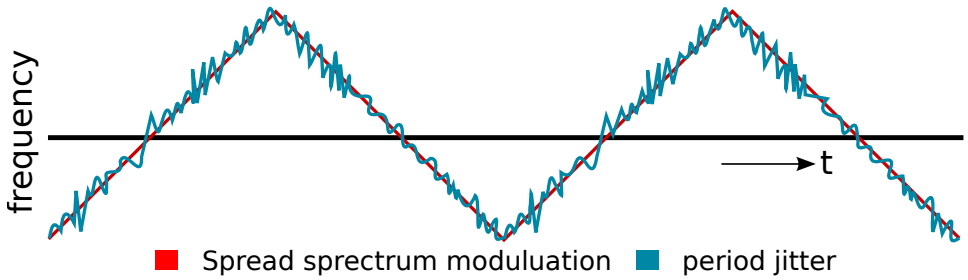

Figure 16: Effect of spread spectrum modulation

- Random component of cycle to cycle jitter is equal to $\sqrt{2}$ times RJ of Period Jitter.
- Deterministic component of cycle to cycle jitter is the same as Period Jitter.

6 Long Term Jitter

Long Term jitter consists of several components. The dominant components are random noise, supply noise and, reference clock.

6.1 Random jitter

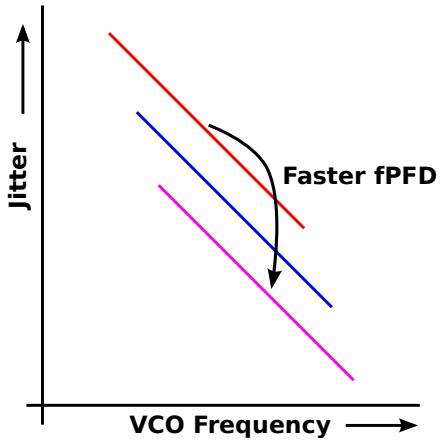

Figure 17: Random Long time Jitter vs. VCO frequency

Random jitter depends on PFD and VCO frequency and can be expressed as:

$$\text{Jitter} \propto \sqrt{\frac{F_{\text{PFDNOM}}}{F_{\text{PFD}}}} \times \sqrt{\frac{F_{\text{VCOMAX}}}{F_{\text{VCO}}}} \tag{9}$$

Most datasheets specify long term random jitter. A generic example is shown in figure below. Refer to datasheet for a specific PLL.

Long term jitter	ps (RMS)			1.41	@ FVCOMax=1GHz, FPFDnom=25MHz Jitter scales as $\sqrt{\frac{FPFD_{\text{nom}}}{FPFD}} \times \sqrt{\frac{FVO_{\text{max}}}{FVCO}}$

Figure 18: Random Long Term jitter specified in the datasheet

Generic Numerical Example 1:

- FPFDnom = 25MHz
- FPFD = 50MHz
- FVCOmax = 1GHz
- FVCO = 800MHz
- Long Term jitter specification from datasheet = 1.41ps
- Random long term jitter: $\sqrt{\frac{25MHz}{50MHz}} * \sqrt{\frac{1GHz}{800MHz}} * 1.41ps = 1.11ps$

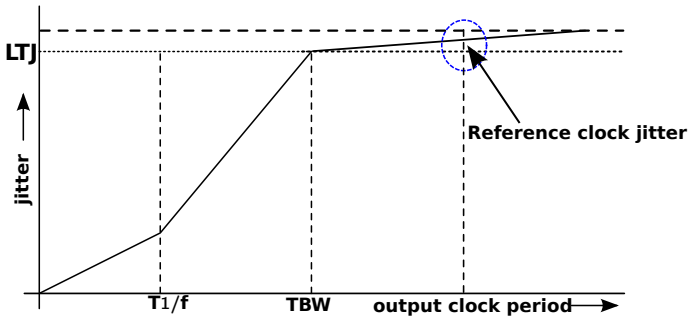

Figure 19: Random Long Term Jitter in time domain

Random long term jitter must be specified at large hold off times, typically in the range of 1000s of PFD clock cycles. It can be represented in time domain as shown in the above figure. The numerical equivalent in the frequency domain can be represented as shown below. Integration range is specified for long term jitter.

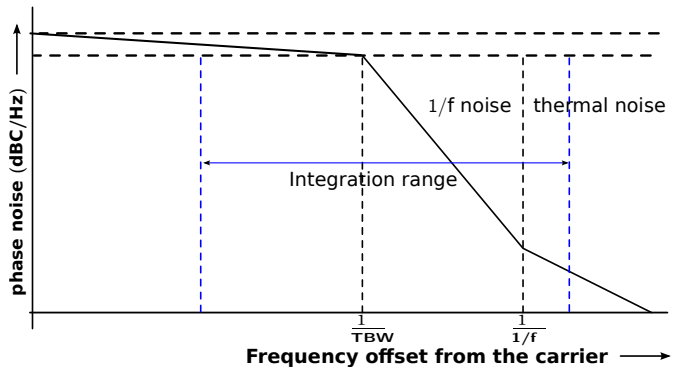

Figure 20: Random Long Term Jitter in frequency domain

Integrated Jitter Range: 10kHz to Nyquist	ps (RMS)			1	@ FVCOMax= 1GHz, FPFDnom=25MHz Jitter scales as $\sqrt{\frac{FPFDnom}{FPFD}} \times \sqrt{\frac{FVCOmax}{FVCO}}$

Figure 21: Integrated jitter specified in datasheet

Typically, the upper integration limit is set to Nyquist, since integrating up to Nyquist is basically integrating down to clock period (there is no phase noise below clock period).

Typically, spectrum analyzers measure SSB noise, so there's a $\sqrt{2}$ factor between time-domain and frequency-domain results. These are numerically equivalent results if we were to measure double side-band.

Generic Numerical Example 2:

- FPFDnom = 25MHz
- FPFD = 50MHz
- FVCOmax = 1GHz
- FVCO = 800MHz
- Integrated jitter specification from datasheet = 1ps
- Integrated jitter: $\sqrt{\frac{25MHz}{50MHz}} * \sqrt{\frac{1GHz}{800MHz}} * 1ps = 0.79ps$

6.2 Supply noise jitter

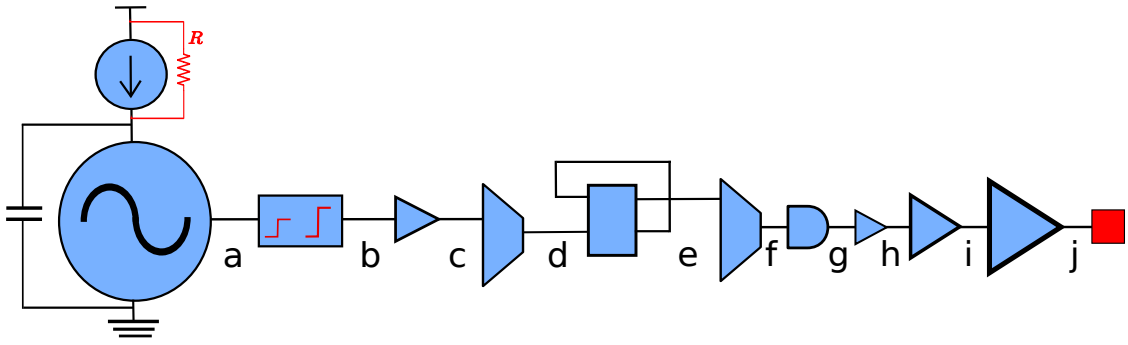

Figure 22: Long Term jitter due to output clock path

Supply noise jitter comes from three components.

- VCO frequency change
- Reference clock path delay change
- Output path delay change

6.2.1 Long term jitter from VCO supply noise

Changes in the VCO supply noise has small but non-zero effect on the VCO frequency.

Below the PLL BW, as noise frequency increases more phase error accumulates. The PLL loop compensates for accumulated phase error. Above the PLL BW, phase error accumulates less as noise frequency goes high.

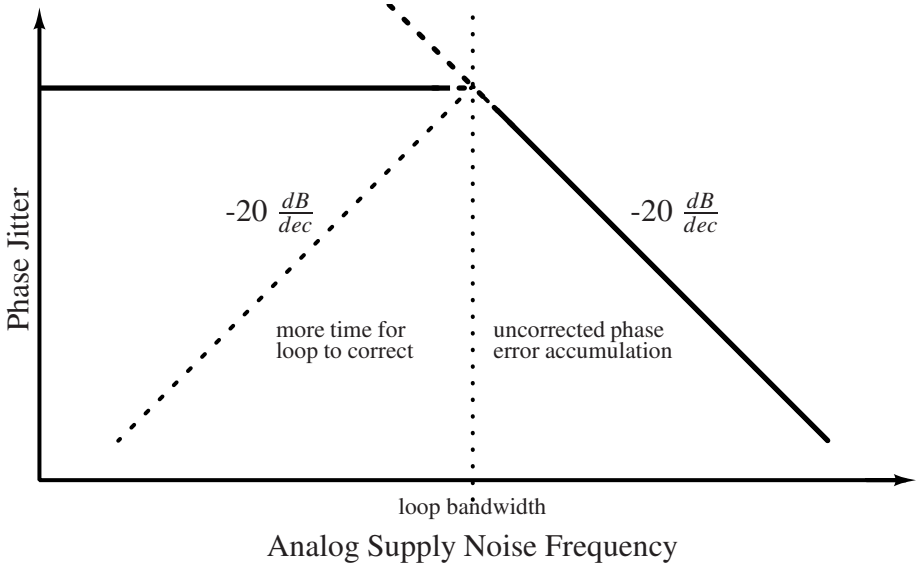

Figure 23: Long Term Supply Noise Sensitivity

Generic Example 1:

Figure 24: Supply Noise in mV

Supply noise sensitivity of long term jitter	fs/mV			1	@ Fvcomax=1GHz

Figure 25: Supply Noise Sensitivity specified in datasheet

The waveform in Figure 26 shows the period variation given the supply noise waveform and the specified supply noise sensitivity shown in Figure 24 and Figure 25.

Figure 26: Supply Noise in period

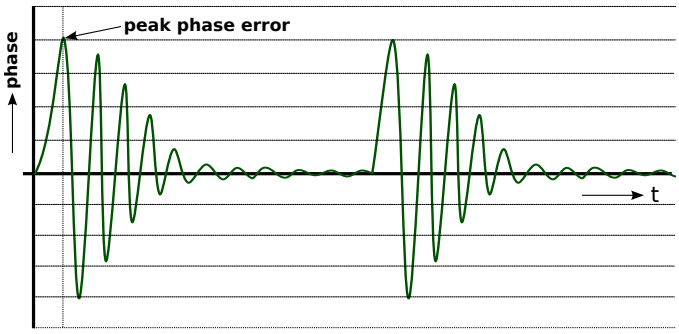

Figure 27: Phase error due to supply noise

Integral of the period variation shown in Figure 26 gives the peak phase error due to the supply noise.

Generic Example 2:

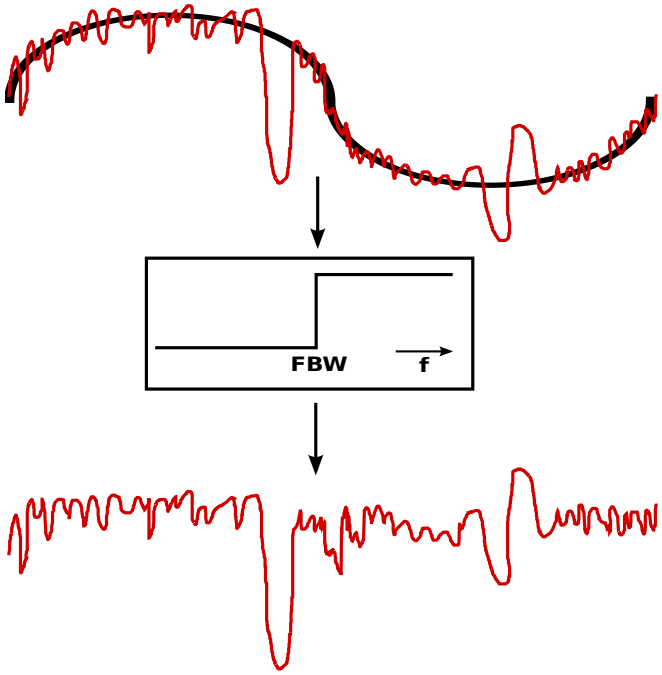

Figure 28: Supply noise, brick-wall high-pass filtered supply noise

The Figure 28 illustrates that the supply noise frequency components below the PLL's band-

width do not accumulate and contribute to phase error.

Generic Example 3:

The following example shows a sinusoidal supply noise waveform. This noise is observed when switching regulators are involved.

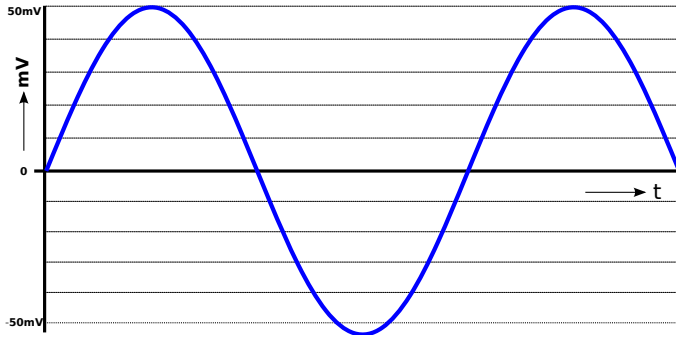

Figure 29: Supply Noise in mV

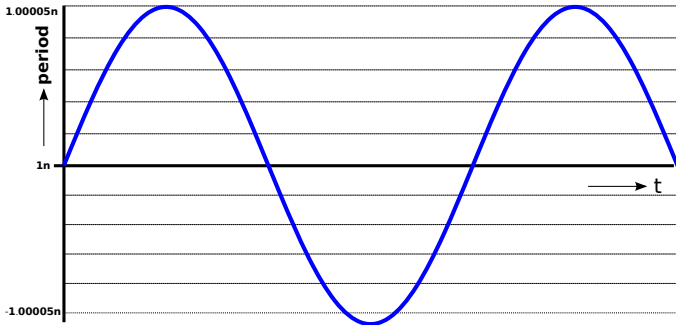

Figure 30: Period Variation due to supply noise

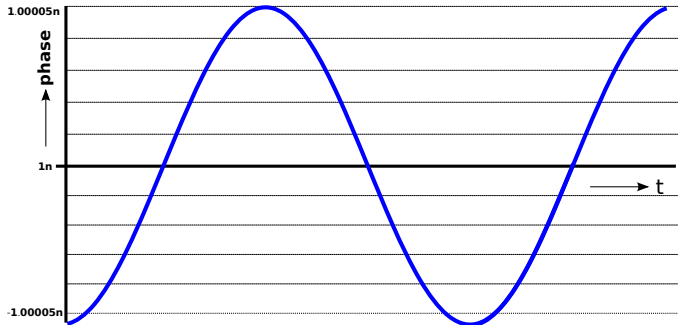

Figure 31: Phase error due to supply noise

For $F_{\text{noise}} \geq F_{\text{BW}}$, supply noise is scaled by the factor :

$$\frac{^{F}\text{VCOMAX}}{^{F}\text{NOISE}} \times \frac{^{V}\text{NOISE}}{\pi}$$

For $F_{\text{noise}} < F_{\text{BW}}$, supply noise is scaled by the factor :

$$\frac{^{F}\text{VCOMAX}}{^{F}\text{BW}} \times \frac{^{V}\text{NOISE}}{\pi}$$

Generic Numerical Example 1:

- FVCOmax = 1000MHz
- FBW =10MHz
- *Fnoise =20MHz*
- Noise Amplitude = 10mV
- Supply noise sensitivity specified in datasheet = 1fs/mV
- Total accumulated phase jitter: $\frac{1\text{fs}}{\text{mV}} * \frac{1000\text{MHz}}{20\text{MHz}} * \frac{10\text{mV}}{\pi}$
- Total accumulated phase jitter = 0.159ps

Generic Numerical Example 2:

- FVCOmax = 1000MHz

- FBW =10MHz
- *Fnoise =1MHz*
- Noise Amplitude = 10mV
- Supply noise sensitivity specified in datasheet = 1fs/mV
- Total accumulated phase jitter: $\frac{1fs}{mV} * \frac{1000MHz}{10MHz} * \frac{10mV}{\pi}$
- Total accumulated phase jitter = 0.318ps

6.2.2 Long Term jitter from Output path supply noise

Long Term jitter does not have any dependency on the edge to edge jitter but will depend on the output path delay. So for the output path, long term jitter is exactly equal to the delay sensitivity. Therefore

Long Term delay from the output path = (Max. path delay - Min. path delay) (10)

6.2.3 Long Term jitter from Reference path supply noise

If the total reference clock delay varies slowly (less than PLL BW), the PLL will follow and the output phase will move accordingly. Low frequency noise (period longer than propagation delay) on the reference clock power supply will modulate the reference clock delay, which will be followed by the PLL. Therefore, propagation delay of the reference clock path should be minimized when long term jitter is a concern.

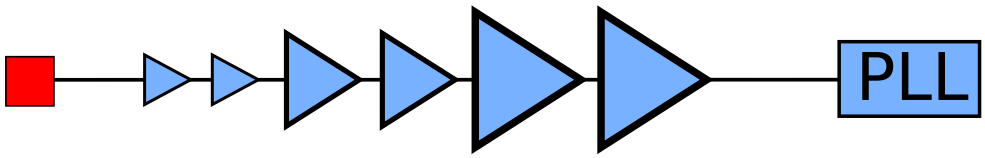

Figure 32: Reference clock path

Although reference clock jitter has minimum affect on period jitter, the delay in the reference path can contribute to long term jitter.

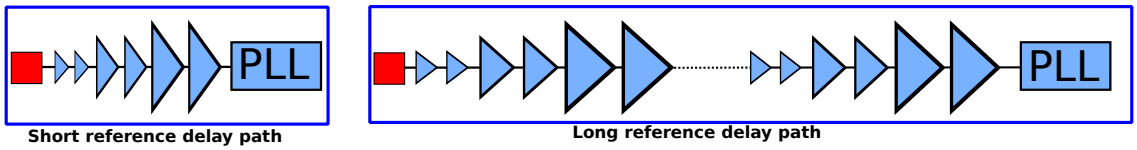

Figure 33: Reference clock path delay

Longer the delay, longer the difference between maximum and minimum delay, which will translate to long term jitter.

6.3 Total Long term Jitter

Total long term Jitter can now be calculating from the previously defined components.

LTJ = [2 * Sigma(σ) * Random Jitter (RMS)] + VCO Supply noise jitter + Reference clock path supply noise jitter + Output clock path supply noise jitter

Intrinsic long term jitter dominates since low frequency noise is uncommon in modern SOCs. However care should be taken to avoid the effect of low frequency noise. For PLL where long term jitter is important, supply should be provided from a properly designed LDO or well filtered switching supply.

7 Reference Clock Guidelines

7.1 Reference Clock Duty-Cycle:

- PLL is only sensitive to the rising edge of the incoming reference clock.
- Pulse-width of the reference clock should be greater than one flip-flop's [setup+hold] time.

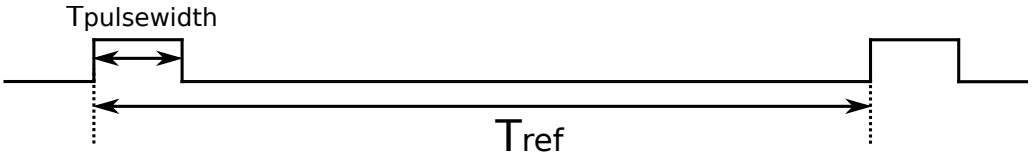

Figure 34: Reference Clock Duty Cycle

7.2 Period Jitter Limit (PJ):

- PLL's output period jitter is approximately equal to $\left[\frac{\text{Input period jitter}}{100}\right]$.
- Reference jitter should be limited to a level that allows for the output jitter specification to be met.

Figure 35: Reference Clock Period Jitter

7.3 Long term Jitter Limit (LTJ):

- PLL's output long term jitter will follow the long term jitter of the input reference clock.
- The Output long term jitter is given by the summation of the reference clock long term jitter and the intrinsic jitter of the PLL.
- The resulting jitter should be lower than the output long term jitter requirement.

Figure 36: Reference Clock Long Term Jitter

7.4 Frequency Tolerance:

- PLL's output frequency tolerance is exactly equal to the input frequency tolerance.
- The reference clock's frequency tolerance should be specified at the system level based on the PLL's output frequency tolerance specification.

Figure 37: Reference Clock Frequency Tolerance

7.5 Signal Levels:

- All signal inputs to the PLL should be full swing CMOS between ground and core supply voltage.
- PLL inputs and outputs do not have level-shifters.

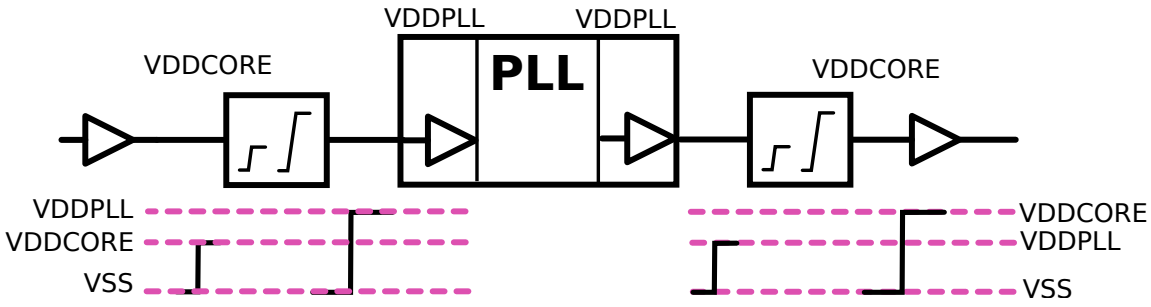

Figure 38: Connecting PLL with different core supply voltage

7.6 General Guidelines:

- Reference clock derived from a crystal typically has a very low long term jitter compared to the PLL and therefore long term jitter can be ignored.
- An estimate of reference clock long term phase jitter is given as $\left(\frac{\text{reference clock delay}}{100}\right)$.
- Period jitter is typically a function of supply noise impulse amplitude and pulse width. Refer to Section 6.2.

8 Appendix

The purpose of this section is to provide some general jitter definitions. It's an attempt to provide a simple estimate of the expected jitter of the PLL.

8.1 Period Jitter (PJ)

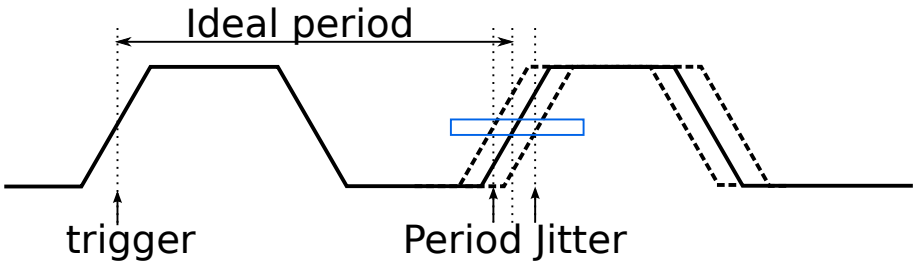

Figure 39: Period Jitter

8.2 Cycle-to-Cycle Jitter (CCJ)

CCJ is a measure of output period changes from one cycle to the next. If using spectrum spectrum, the period jitter guideline apply and the random component of CCJ can be quantified as $\sqrt{2}$ times the period jitter.

8.3 Long Term Jitter (LTJ), Accumulated jitter, phase jitter, N-cycle jitter

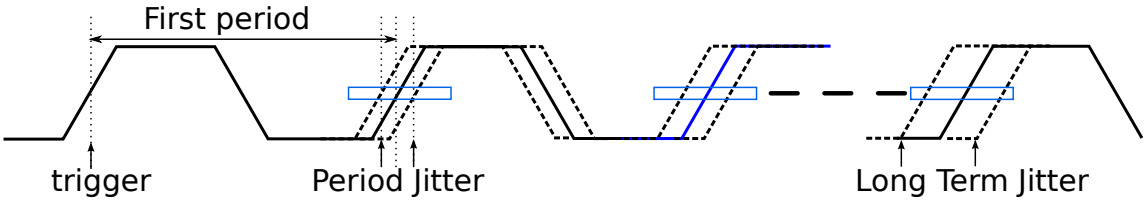

Figure 40: Long Term Jitter

Long Term jitter is also called as accumulated jitter, phase jitter. N-cycle jitter is also equivalent to long term jitter, when N>loop time constant.

8.4 Time-Interval Error (TIE)

If measuring TIE, the long term jitter guidelines apply and the random component of TIE can be quantified as $\frac{1}{\sqrt{2}}$ times the long term jitter. Also, if integrated phase noise measured on a spectrum analyzer, it's equivalent to TIE.