Technical Note

LPDDR5 Bank Architecture

Introduction

This technical note describes LPDDR5 SDRAM bank architecture. Unlike previous-generation LPDDR devices, LPDDR5 achieves a higher data rate by employing a bank group architecture with three different bank modes. Users can choose the appropriate LPDDR5 bank mode depending on their specific operating frequency and burst length requirements. This document explains why LPDDR5 architecture uses three bank modes and provides information about each mode, including burst operation, addressing and burst length definitions.

Prefetch and Data Granularity

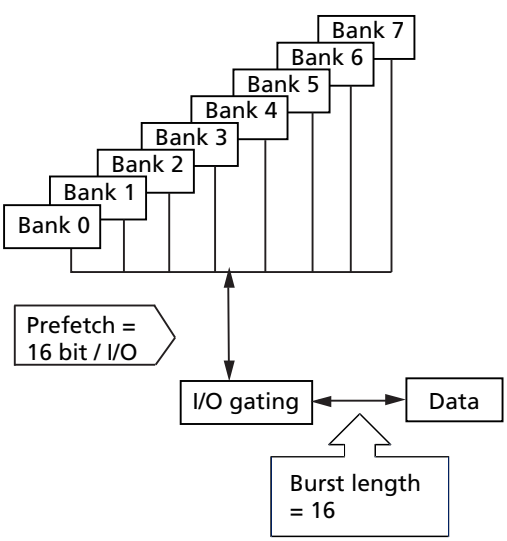
The standard approach to achieving a higher data rate in DRAM architectures is to increase prefetch size. For example, LPDDR2 uses a 4n prefetch, LPDDR3 uses a 8n prefetch, and LPDDR4 uses a 16n prefetch, where n equals number of I/Os. However, increasing the prefetch size also increases data granularity, which is the data size transferred between the LPDRAM device and the memory controller when a READ or WRITE command is issued. For example, for a single-channel die in 16 I/O mode, data granularity is calculated using the following equation:

(16 I/Os x BL16)/8 = 32 bytes

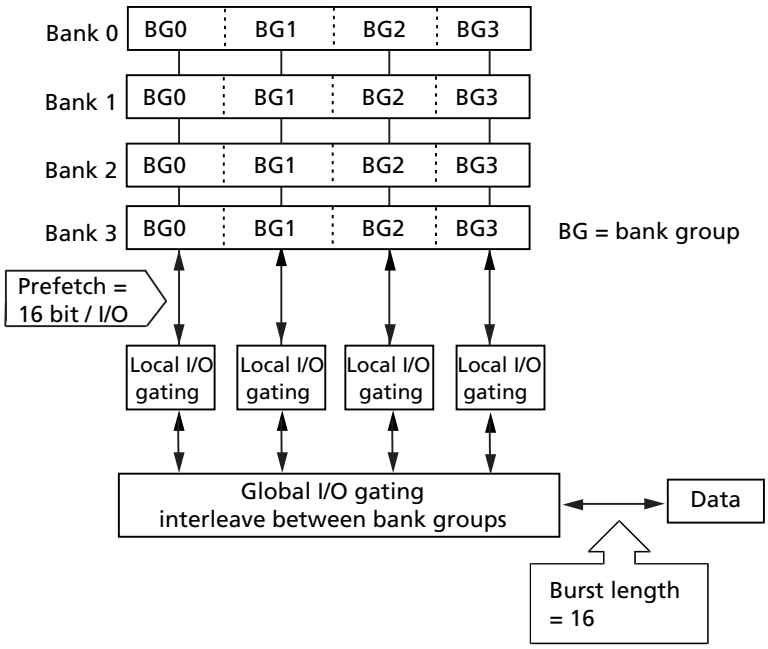
If data granularity is too large, some data may be wasted. In order to keep the same data granularity, LPDDR5 uses the same prefetch size as LPDDR4 (a 16n prefetch) while employing a bank group architecture to reach a higher data rate. In a bank group architecture, each bank group has local I/O gating connected to global I/O gating. The column command interval between different bank groups can also be shortened because of the local I/O gating for each bank group. The column command interval between the same bank group is longer due to local I/O gating column turnaround time.

In comparison, LPDDR4 ^{t}CCD (READ to READ or WRITE to WRITE command interval) is always limited by I/O gating column turnaround time because LPDDR4 only has one I/O gating type (local). If prefetch is doubled, column turnaround time doubles as burst length doubles.

Figure 1: LPDDR4 vs. LPDDR5 Bank Architecture



LPDDR4 Single-Bank Group



LPDDR5 4-Bank x 4-Bank Groups

LPDDR5 Bank Modes

LPDDR5 supports three bank modes for different system configuration needs. The native burst length determined by data prefetch size varies depending on which bank mode is enabled.

Each mode is abbreviated as follows:

- BG mode = 4 banks, 4-bank groups
- 16B mode = 16 banks, no bank groups
- 8B mode = 8 banks, no bank groups

The supported data rate and burst length for each bank/bank group organization is as follows:

- BG mode: more than 3200 Mb/s (>3200 Mb/s); BL16 and BL32
- 16B mode: less than or equal to 3200 Mb/s (≤3200 Mb/s); BL16 and BL32
- 8B mode: all data rate ranges; BL32 only

Bank Mode Configurations

Example block diagrams for each LPDDR5 bank mode configuration are shown below.

Figure 2: BG Mode Configuration Example

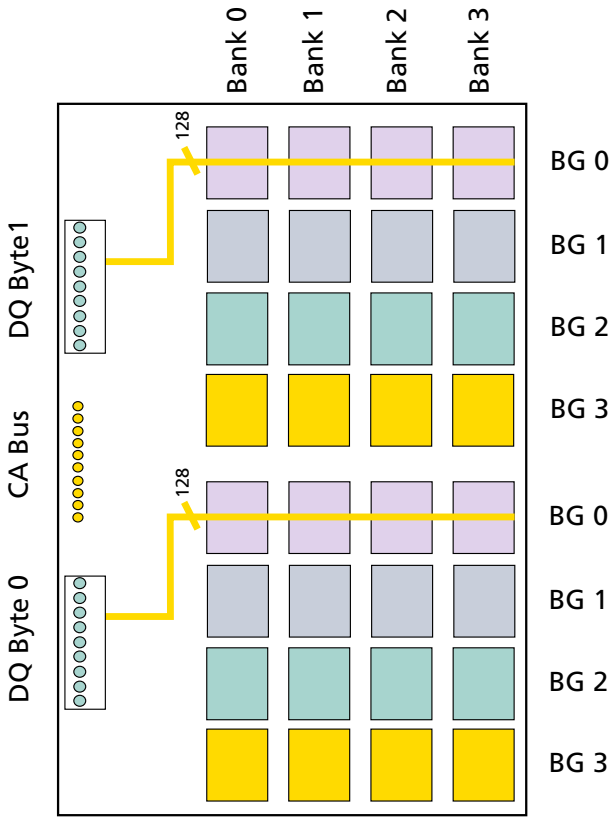


Figure 3: 16B Mode Configuration Example

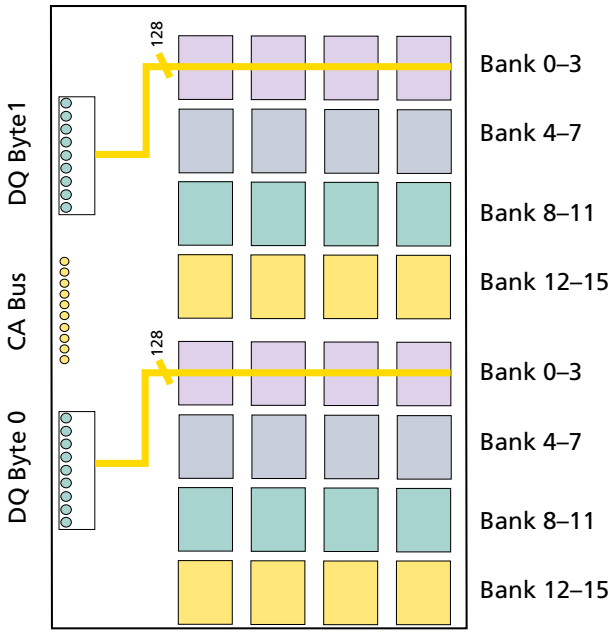
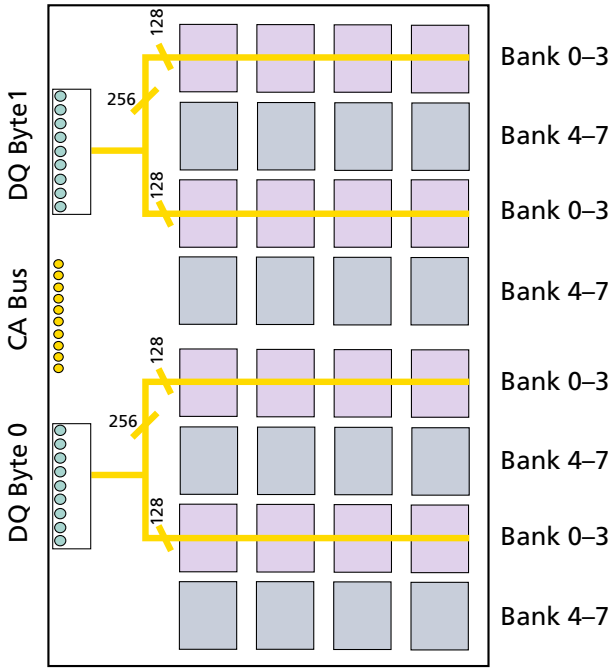


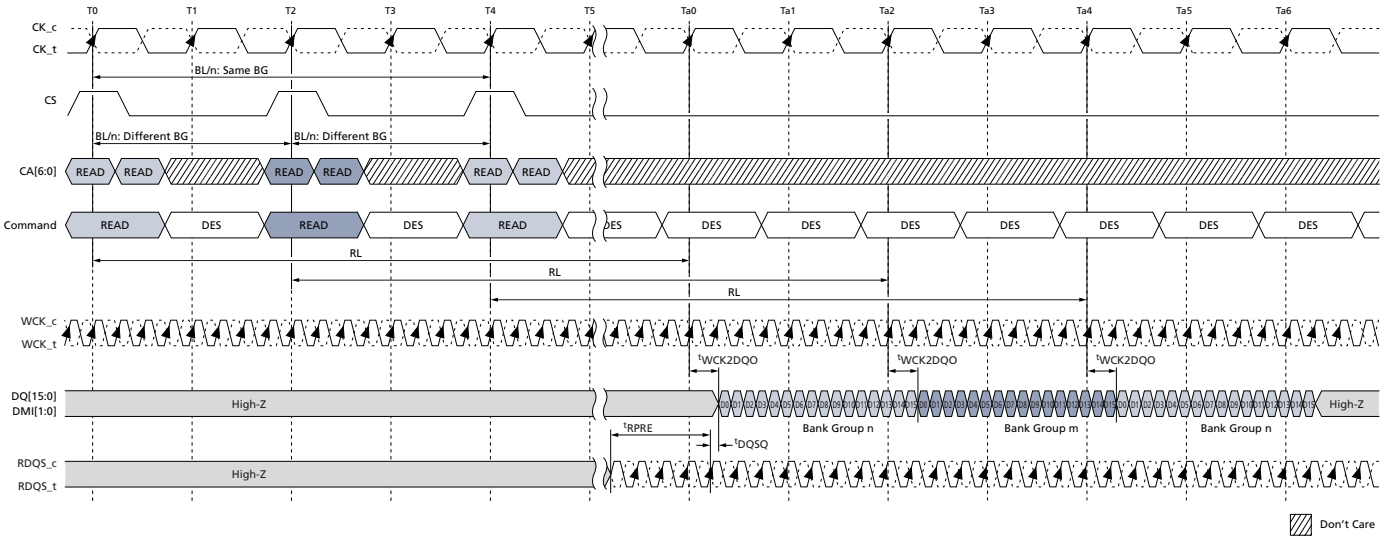
Figure 4: 8B Mode Configuration Example



Burst Operation

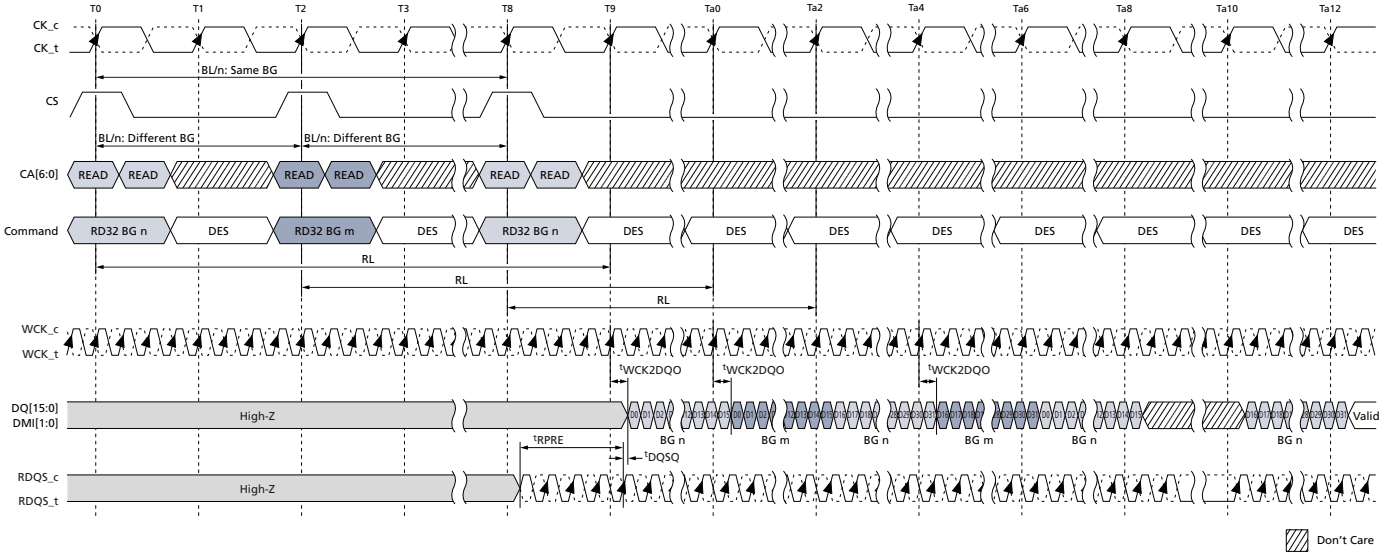
READ/WRITE command behavior in LPDDR5 is dependant on the selected bank mode. Read data output behavior for each mode type is shown in the following figures (the CAS command and WCK input are omitted). See the READ and WRITE Operation sections of the LPDDR5 data sheet for details.

Figure 5: READ Operation, BG Mode, CKR = 4:1, BL16



Notes:
1. MR3 OP[4:3] = 00; BG; MR18 OP[7] = 0; CKR = 4:1; BL = 16
2. ^{t}WCK2CK is 0ps for this instance.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 6: READ Operation, BG Mode BL32, BG Interleave CKR = 4:1

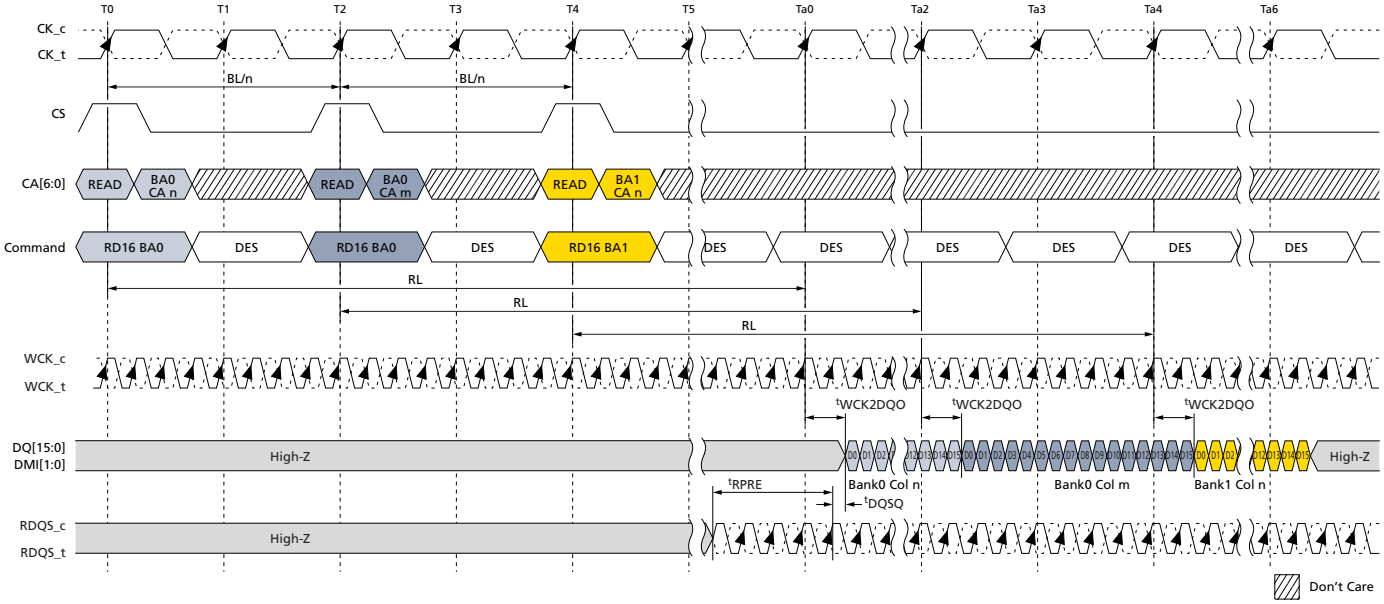


Notes:
1. MR3 OP[4:3] = 00; BG, MR18 OP[7] = 0; CKR = 4:1; BL = 32
2. ^{t}WCK2CK is 0ps for this instance.
3. DES commands are shown for ease of illustration; Other commands may be valid at these times.

The BG mode architecture only supports BL32 in an interleaved fashion when the WCK:CK ratio (CKR) is 4:1. BL32 interleaved reads output the first word of DQ[15:0] RL from the READ command. The second word consisting of DQ[31:16] begins to be driven after an 8^{t}WCK gap from the end of the first word. If correctly implemented, READ (BL16) commands and READ32 (BL32) commands can be mixed; however, after a READ32 (BL32) command is issued, issuing a READ (BL16)/READ32 (BL32) command after three clocks is prohibited to avoid read data conflict.

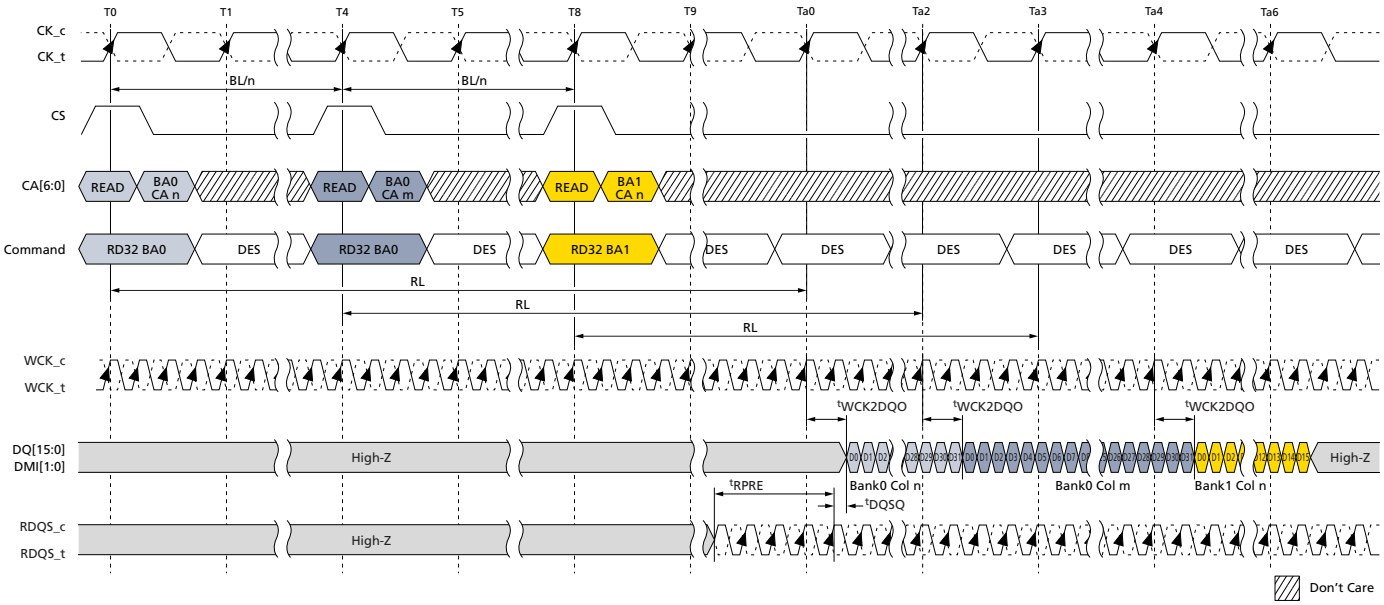
The relationship between preceding WRITE32 (BL32) and WRITE (BL16)/WRITE32 (BL32) commands is the same as preceding READ32 (BL32) and READ (BL16)/READ32 (BL32) commands.

Figure 7: READ Operation 16B Mode, CKR = 4:1, BL16



Notes:
1. MR3 OP[4:3] = 10; 16B; MR18 OP[7] = 0; CKR = 4:1; BL = 16
2. ^{t}WCK2CK is 0ps for this instance.
3. DES commands are shown for ease of illustration; Other commands may be valid at these times.

Figure 8: READ Operation 16B Mode, CKR = 4:1, BL32

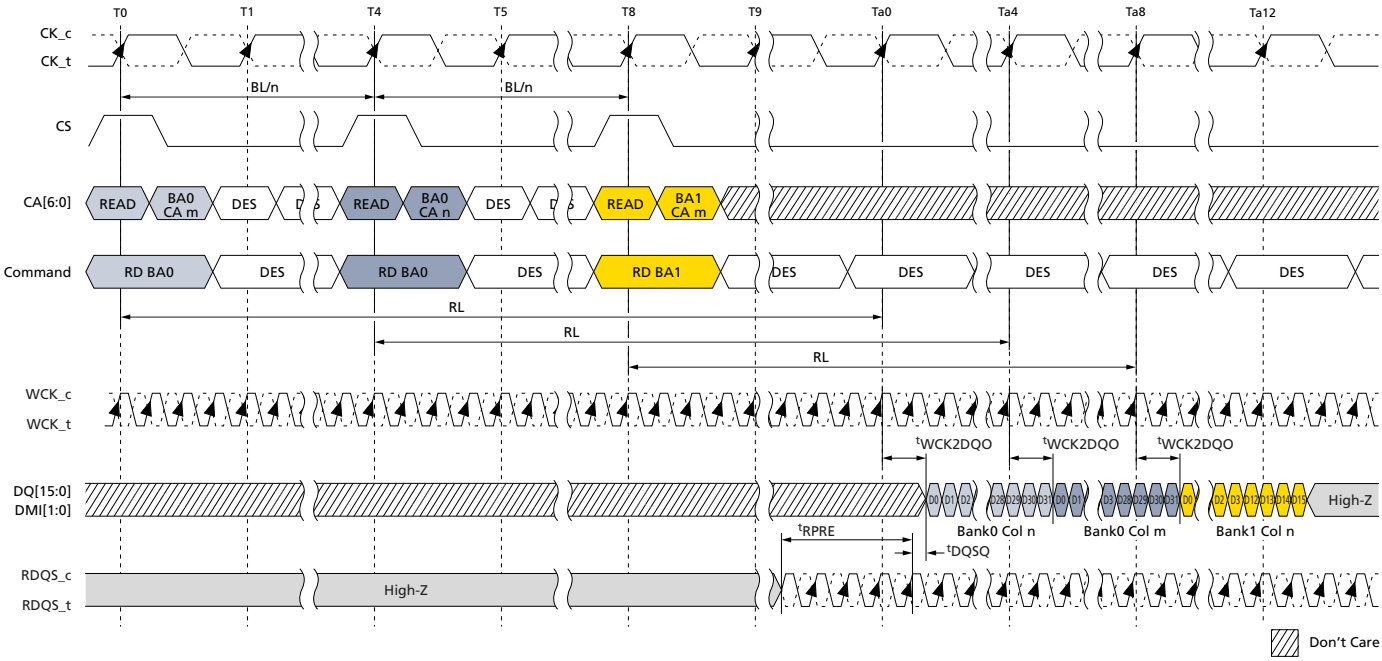


Notes:
1. MR3 OP[4:3] = 10; 16B; MR18 OP[7] = 0; CKR = 4:1; BL = 32
2. ^{t}WCK2CK is 0ps for this instance.

3. DES commands are shown for ease of illustration; Other commands may be valid at these times.

In 8B mode (shown below), the native burst length is 32. Only BL32 is supported.

Figure 9: Consecutive READ Operation, 8B Mode, CKR = 4:1



Notes:
1. MR3 OP[4:3] = 01; 8B; MR18 OP[7] = 0; CKR = 4:1; BL = 32
2. ^{t}WCK2CK is 0ps for this instance.
3. DES commands are shown for ease of illustration; Other commands may be valid at these times.

Addressing

Because LPDDR5 users should switch between bank modes depending on burst length and operating frequency, it is important to understand addressing changes between bank modes in order to determine where the data is located.

Table 1: Address Mapping Between BG, 16B, and 8B Modes

Address Mapping Between 8B, BG, and 16B Modes			
BG Mode	**16B Mode**	**8B Mode**	**Description**
BA[1:0]	BA[1:0]	BA[1:0]	Bank address least significant bits (LSBs)
BG[0]	BA[2]	BA[2]	8B/16B bank address = bank group LSB
BG[1]	BA[3]	B[4]	8B burst most significant bit (MSB) address becomes bank group or bank address
B[3:0]	B[3:0]	B[3:0]	Burst address LSBs
C[5:0]	C[5:0]	C[5:0]	Column addresses
R[16:0]	R[16:0]	R[16:0]	Row addresses

Note: 1. BA[3:0]: Bank address, BG[1:0]: Bank group address, B[4]: Burst starting address

Table 2: x16 Mode, BG Mode Addressing

BG Mode Addressing (Single-Channel)									
Density per Die	**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration	8Mb x16 DQ x 4 banks x 4BG	12Mb x16 DQ x 4 banks x 4BG	16Mb x16 DQ x 4 banks x 4BG	24Mb x16 DQ x 4 banks x 4BG	32Mb x16 DQ x 4 banks x 4BG	48Mb x16 DQ x 4 banks x 4BG	64Mb x16 DQ x 4 banks x 4BG	96Mb x16 DQ x 4 banks x 4BG	128Mb x16 DQ x 4 banks x 4BG
Bits	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Number of banks	4	4	4	4	4	4	4	4	4
Number of bank groups	4	4	4	4	4	4	4	4	4
Array prefetch bits	256	256	256	256	256	256	256	256	256
Rows per bank	8192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Columns	64	64	64	64	64	64	64	64	64
Page size (bytes)	2048	2048	2048	2048	2048	2048	2048	2048	2048
Native burst length	16	16	16	16	16	16	16	16	16
Number of I/Os	16	16	16	16	16	16	16	16	16
Bank addresses	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]
Bank group addresses	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]
Row addresses	R[12:0]	R[13:0] (R12 = 0 when R13 = 1)	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]

Table 2: x16 Mode, BG Mode Addressing (Continued)

BG Mode Addressing (Single-Channel)									
Density per Die	**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Column addresses	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst start address boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.
4. Row address input that violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

Table 3: x16 Mode, 16B Mode Addressing

16B Mode Addressing (Single-Channel)									
Density per Die	**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration	8Mb x16 DQ x16 banks	12Mb x16 DQ x16 banks	16Mb x16 DQ x16 banks	24Mb x16 DQ x16 banks	32Mb x16 DQ x16 banks	48Mb x16 DQ x16 banks	64Mb x16 DQ x16 banks	96Mb x16 DQ x16 banks	128Mb x16 DQ x16 banks
Bits	2,147, 483,648	3,221, 225,472	4,294, 967,296	6,442, 450,944	8,589, 934,592	12,884, 901,888	17,179, 869,184	25,769, 803,776	34,359, 738,368
Number of banks	16	16	16	16	16	16	16	16	16
Array prefetch bits	256	256	256	256	256	256	256	256	256
Rows per bank	8192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Columns	64	64	64	64	64	64	64	64	64
Page size (bytes)	2048	2048	2048	2048	2048	2048	2048	2048	2048
Native burst length	16	16	16	16	16	16	16	16	16
Number of I/Os	16	16	16	16	16	16	16	16	16
Bank group addresses	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]
Row addresses	R[12:0]	R[13:0] (R12 = 0 when R13 = 1)	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]
Column addresses	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst start address boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.
4. Row address input that violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

Table 4: x8 Mode, BG Mode Addressing

BG Mode Addressing (Single-Channel)									
Density per Die		**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration		16Mb x8 DQ x 4 banks x 4BG	24Mb x8 DQ x 4 banks x 4BG	32Mb x8 DQ x 4 banks x 4BG	48Mb x8 DQ x 4 banks x 4BG	64Mb x8 DQ x 4 banks x 4BG	96Mb x8 DQ x 4 banks x 4BG	128Mb x8 DQ x 4 banks x 4BG	192Mb x8 DQ x 4 banks x 4BG	256Mb x8 DQ x 4 banks x 4BG
Bits		2,147, 483,648	3,221, 225,472	4,294, 967,296	6,442, 450,944	8,589, 934,592	12,884, 901,888	17,179, 869,184	25,769, 803,776	34,359, 738,368
Number of banks		4	4	4	4	4	4	4	4	4
Number of bank groups		4	4	4	4	4	4	4	4	4
Array prefetch bits		128	128	128	128	128	128	128	128	128
Rows per bank		16,384	24,576	32,768	49,152	65,536	98,304	131,072	196,608	262,144
Columns		64	64	64	64	64	64	64	64	64
Page size (Bytes)		1024	1024	1024	1024	1024	1024	1024	1024	1024
Native burst length		16	16	16	16	16	16	16	16	16
Number of I/Os		8	8	8	8	8	8	8	8	8
BG mode	Bank addresses	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]
	Bank group addresses	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]	BG[1:0]
Row addresses		R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]	R[17:0] (R16 = 0 when R17 = 1)	R[17:0]
Column addresses		C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses		B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst start address boundary		128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.
4. Row address input which violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

Table 5: x8 Mode, 16B Mode Addressing

16B Mode Addressing (Single-Channel)									
Density per Die		**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration		16Mb x8 DQ x16 banks	24Mb x8 DQ x16 banks	32Mb x8 DQ x16 banks	48Mb x8 DQ x16 banks	64Mb x8 DQ x16 banks	96Mb x8 DQ x16 banks	128Mb x8 DQ x16 banks	192Mb x8 DQ x16 banks	256Mb x8 DQ x16 banks
Bits		2,147, 483,648	3,221, 225,472	4,294, 967,296	6,442, 450,944	8,589, 934,592	12,884, 901,888	17,179, 869,184	25,769, 803,776	34,359, 738,368
Number of banks		16	16	16	16	16	16	16	16	16
Array prefetch bits		128	128	128	128	128	128	128	128	128
Rows per bank		16,384	24,576	32,768	49,152	65,536	98,304	131,072	196,608	262,144
Columns		64	64	64	64	64	64	64	64	64
Page size (Bytes)		1024	1024	1024	1024	1024	1024	1024	1024	1024
Native burst length		16	16	16	16	16	16	16	16	16
Number of I/Os		8	8	8	8	8	8	8	8	8
16B mode	Bank group addresses	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]
Row addresses		R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]	R[17:0] (R16 = 0 when R17 = 1)	R[17:0]
Column addresses		C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses		B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst start address boundary		128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.
4. Row address input which violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

Table 6: x16 Mode, 8B Mode Addressing

8B Mode Addressing (Single-Channel)									
Density per Die	**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration	16Mb x16 DQ x8 banks	24Mb x16 DQ x8 banks	32Mb x16 DQ x8 banks	48Mb x16 DQ x8 banks	64Mb x16 DQ x8 banks	96Mb x16 DQ x8 banks	128Mb x16 DQ x8 banks	192Mb x16 DQ x8 banks	256Mb x16 DQ x8 banks
Bits	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Number of banks	8	8	8	8	8	8	8	8	8
Number of bank groups	1	1	1	1	1	1	1	1	1
Array prefetch bits	512	512	512	512	512	512	512	512	512
Rows per bank	8192	12288	16384	24576	32768	49152	65536	98304	131072
Columns	64	64	64	64	64	64	64	64	64
Page size (Bytes)	4096	4096	4096	4096	4096	4096	4096	4096	4096
Native burst length	32	32	32	32	32	32	32	32	32
Number of I/Os	16	16	16	16	16	16	16	16	16
Bank addresses	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
Bank group addresses	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Row addresses	R[12:0]	R[13:0] (R12 = 0 when R13 = 1)	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]
Column addresses	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]
Burst start address boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.

4. Row address input which violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

Table 7: x8 Mode, 8B Mode Addressing

8B Mode Addressing (Single-Channel)									
Density per Die	**2Gb**	**3Gb**	**4Gb**	**6Gb**	**8Gb**	**12Gb**	**16Gb**	**24Gb**	**32Gb**
Configuration	32Mb x8 DQ x8 banks	48Mb x8 DQ x8 banks	64Mb x8 DQ x8 banks	96Mb x8 DQ x8 banks	128Mb x8 DQ x8 banks	192Mb x8 DQ x8 banks	256Mb x8 DQ x8 banks	384Mb x8 DQ x8 banks	512Mb x8 DQ x8 banks
Bits	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Number of banks	8	8	8	8	8	8	8	8	8
Number of bank groups	1	1	1	1	1	1	1	1	1
Array prefetch bits	256	256	256	256	256	256	256	256	256
Rows per bank	16384	24,576	32,768	49,152	65,536	98,304	131,072	196,608	262,144
Columns	64	64	64	64	64	64	64	64	64
Page size (Bytes)	2048	2048	2048	2048	2048	2048	2048	2048	2048
Native burst length	32	32	32	32	32	32	32	32	32
Number of I/Os	8	8	8	8	8	8	8	8	8
Bank addresses	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
Bank group addresses	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Row addresses	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]	R[17:0] (R16 = 0 when R17 = 1)	R[17:0]
Column addresses	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]	C[5:0]
Burst addresses	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]	B[4:0]
Burst start address boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit

Notes:
1. The lower three burst addresses B[2:0] are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. For non-binary memory densities, only half the row address space is valid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.

4. Row address input which violates the restriction described in note 3 may result in undefined or vendor-specific behavior. Consult the memory vendor for more information.

BL/n Specification

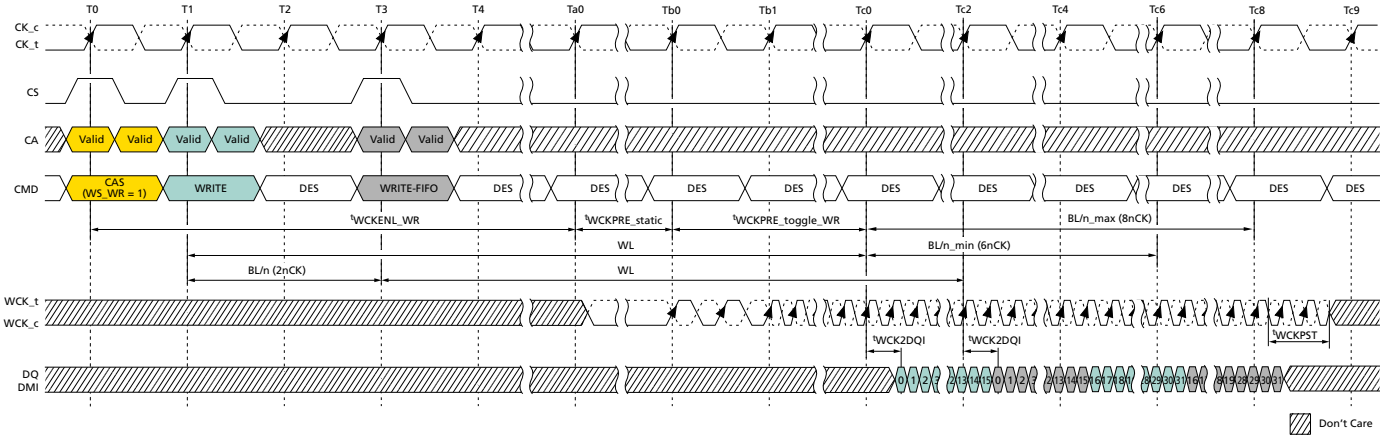
Effective burst length (BL/n) is newly defined in LPDDR5 and consists of BL/n, BL/n_min and BL/n_max. By using the effective BL/n definition (shown below), command interval and timing specifications can be simplified and the number of timing diagrams can be reduced.

Table 8: Effective Burst Length (BL/n) Definitions

WCK:CK Ratio	Bank/BG Organization	Bank-to-Bank Constraints	I/O Speed (WCK Frequency)	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
2:1	16B mode	Any bank to bank	≤1600 MHz	BL16	4 × tCK (BL/4)	4 × tCK (BL/4)	4 × tCK (BL/4)
				BL32	8 × tCK (BL/4)	8 × tCK (BL/4)	8 × tCK (BL/4)
	8B mode	Any bank to bank		BL32	8 × tCK (BL/4)	8 × tCK (BL/4)	8 × tCK (BL/4)
		MRR, WFF, RFF, RDC, [8]		BL16	8 × tCK (BL/2)	8 × tCK (BL/2)	8 × tCK (BL/2)
4:1	16B mode	Any bank to bank	≤1600 MHz	BL16	2 × tCK (BL/8)	2 × tCK (BL/8)	2 × tCK (BL/8)
				BL32	4 × tCK (BL/8)	4 × tCK (BL/8)	4 × tCK (BL/8)
	BG Mode	Same BG	>1600 MHz	BL16	4 × tCK (2 × BL/8)	2 × tCK (BL/8)	4 × tCK (2 × BL/8)
		Different BG			2 × tCK (BL/8)		
		Same BG	>1600 MHz	BL32	8 × tCK (2 × BL/8)	6 × tCK (1.5 × BL/8)	8 × tCK (2 × BL/8)
		Different BG			2 × tCK (0.5 × BL/8)		
	8B mode	Any bank to bank	Any frequency	BL32	4 × tCK (BL/8)	4 × tCK (BL/8)	4 × tCK (BL/8)
		MRR, WFF, RFF, RDC[8]		BL16	4 × tCK (BL/4)	4 × tCK (BL/4)	4 × tCK (BL/4)

Notes:
1. BL/n is the minimum column to column cycle time, tCCD (MIN).
2. BL/n_min is the minimum burst data transfer time on the DQ bus.
3. BL/n_max is the required column array cycle time to allow next column array cycle.
4. BL/n, BL/n_min, and BL/n_max are parameters in a CK domain.
5. BL/n, BL/n_min, and BL/n_max are same in an 8B or 16B mode.
6. In case of same BG in a BG mode, BL/n = BL/n_max > BL/n_min.
7. In case of different BG in a BG mode, BL/n = BL/n_min < BL/n_max for BL16, BL/n < BL/n_min < BL/n_max for BL32.
8. For MRR, WFF, RFF, and RDC commands in an 8B mode, normal WRITE/READ operation timings (BL32) are applied to WCK2CK SYNC Off and ODT/Non-target ODT.

Figure 10: Write Timing Diagram (BG Mode, CKR = 4:1, BL32) Example for BL/n, BL/n_min, and BL/n_max



Revision History

Rev. A – 4/19

- Initial release

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