Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

SPI NAND
Palladium Memory Model
User Guide

Document Version: 1.15

Document Date: July 2018

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

SPI NAND Memory Model

1. Introduction

The Cadence Palladium SPI NAND Palladium memory models are based upon the *Micron, Macronix ,Winbond and Gigadevice SPI NAND* datasheets referenced below.

Vendor	Part Number	Reference Datasheet
Micron	mt29f1g01aaadd	MT29F1G01AAADD - Rev K - 07/2014
	mt29f2g01aaaed	MT29F2G01AAAED - Rev I - 07/2014
	mt29f4g01aaadd	MT29F4G01AAADD - Rev I - 07/2014
Macronix	mx35lf1ge4ab	MX35LFxGE4AB - Rev 1.2 - 08/19/2015
	mx35lf2ge4ab	MX35LFxGE4AB - Rev 1.2 - 08/19/2015
Winbond	w25n01gvxxig/it	W25N01GV - Rev G - 03/21/2016
	w25n01gwxxig/it	W25N01GW - Rev A - 10/17/2015
	w25m02gvxxig/it	W25M02GV - Rev B - 07/01/2015
	w25m02gwxxig/it	W25M02GW - Rev C - 02/13/2018
	w25n01jwxxig/it	W25N01JW - Rev 0.2 – 05/19/2017
Gigadevice	gd5f1gq4xb	GD5FxGQ4xBxIG - Rev 1.3 - 03/15/2016
	gd5f1gq4xc	GD5FxGQ4xC - Rev 1.4 - 04/01/2016
	gd5f2gq4xb	GD5FxGQ4xBxIG - Rev 1.3 - 03/15/2016
	gd5f2gq4xc	GD5FxGQ4xC - Rev 1.4 - 04/01/2016
	gd5f4gq4xb	GD5F4GQ4xBxIG - Rev 1.3 - 03/15/2016
	gd5f4gq4xc	GD5F4GQ4xC - Rev 1.4 - 04/01/2016

Please consult the memory model catalog for the currently available configurations list.

SPI NAND Flash Memory models available in protected RTL (*.vp) formats:

- mt29f1g01aaadd : Micron 1Gbit SPI NAND Flash
- mt29f2g01aaaed : Micron 2Gbit SPI NAND Flash
- mt29f4g01aaadd : Micron 4Gbit SPI NAND Flash

- mx35lf1ge4ab : Macronix 1Gbit Serial NAND Flash
- mx35lf2ge4ab : Macronix 2Gbit Serial NAND Flash

- w25n01gvxxig/it : Winbond 3V 1Gbit Serial SLC NAND Flash
- w25n01gwxxig/it : Winbond 1.8V 1Gbit Serial SLC NAND Flash
- w25m02gvxxig/it : Winbond 3V 2Gbit (2 x 1Gbit) Serial SLC NAND Flash
- w25m02gwxxig/it : Winbond 1.8V 2Gbit (2 x 1Gbit) Serial SLC NAND Flash
- w25n01jwxxig/it(Beta) : Winbond 1.8V 1Gbit Serial SLC NAND Flash(DTR)

- gd5f1gq4ub/uc : Gigadevice 3.3V 1Gbit SPI NAND Flash
- gd5f1gq4rb/rc : Gigadevice 1.8V 1Gbit SPI NAND Flash
- gd5f2gq4ub/uc : Gigadevice 3.3V 2Gbit SPI NAND Flash
- gd5f2gq4rb/rc : Gigadevice 1.8V 2Gbit SPI NAND Flash
- gd5f4gq4ub/uc : Gigadevice 3.3V 4Gbit SPI NAND Flash
- gd5f4gq4rb/rc : Gigadevice 1.8V 4Gbit SPI NAND Flash

2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

3. Features

The SPI NAND Palladium memory models are based upon *Micron, Macronix, Winbond and GigaDevice SPI NAND datasheets*. Below tables lists which features are supported and which are unsupported. Please refer to the specific *SPI NAND datasheets* for more detailed information.

NOTE: The Winbond w25n01jwxxig/it part models are currently available in Initial Release (IR) BETA program only. These models are not in the official MMP release. Please request access to these model via an FAE, the emulation support team, or the MMP support team.

Table 1: Features List for Micron and Macronix Models

FEATURE	SUPPORT	NOTE
Write operations (Write Enable and Write Disable)	Yes	
Features operations (Get Feature and Set Feature)	Yes	
Read Operations (Page Read and Read ID)	Yes	
Power-on Read	Yes	Only the mx35lf1ge4ab and mx35lf2ge4ab support
Parameter Page	Yes	
UniqueID Page	Yes	
Program Operation (Page Program, Rand Data Program and Internal Data Move)	Yes	
Block Operation (Block Erase, Block Lock Feature, OTP feature, Status Register)	Yes	
Error Management	No	All blocks are valid for SPI NAND model.
ECC Protection	Partial	The spare area (64bytes) of each page is supported, but the internal ECC calculation and detection and correction are NOT supported.
SPI Power UP	Partial	The RESET command is supported, but the alternative SPI Power-up is NOT supported.

Table 2: Feature List for Winbond Models

FEATURE		SUPPORT	NOTE
Power On Read		Yes	After power up, the data in page 0 will be automatically loaded into the Data Buffer
Reset Operations	Device RESET	Yes	
	RESET Enable + RESET Memory	Yes	NOR compatible
Die Active Operations	Software Die Select	Yes	Only the w25m02gv and w25m02gw support this feature
Identification Operations	JEDEC ID	Yes	
Register Operations	Read Status Register	Yes	
	Write Status Register	Yes	
	Write Data Learning Pattern	Yes	Only the w25n01jw support this feature
Write Operations	Write Enable	Yes	
	Write Disable	Yes	
Deep Power Down	Deep Power-down	Yes	Only the w25n01jw support this feature
	Release Deep Power-down	Yes	Only the w25n01jw support this feature
Bad Block Management Operations	BB Management (Swap Blocks)	Partial	This function is not supported; the operation only updates LUT.
	Read BBM LUT	Yes	
ECC Operations	Last ECC failure Page Address	Partial	The command is supported, but the internal ECC calculation is NOT supported. The model returns Page Address = 0x0000.
Erase Operations	Block Erase	Yes	
Program Operations	Program Data Load (Reset Buffer)	Yes	
	Random Program Data Load	Yes	
	Quad Program Data Load (Reset Buffer)	Yes	
	Random Quad Program Data Load	Yes	
	Program Execute	Yes	
Read Operations	Page Data Read	Yes	
	Read	Yes	
	Fast Read	Yes	
	Fast Read with 4-Byte Address	Yes	
	Fast Read Dual Output	Yes	
	Fast Read Dual Output with 4-Byte Address	Yes	
	Fast Read Quad Output	Yes	
	Fast Read Quad Output with 4-Byte Address	Yes	

FEATURE		SUPPORT	NOTE
	Fast Read Dual I/O	Yes	
	Fast Read Dual I/O with 4-Byte Address	Yes	
	Fast Read Quad I/O	Yes	
	Fast Read Quad I/O with 4-Byte Address	Yes	
	DTR Fast Read	Yes	Only the w25n01jw support this feature
	DTR Fast Read with 4-Byte Address	Yes	Only the w25n01jw support this feature
	DTR Fast Read Dual Output	Yes	Only the w25n01jw support this feature
	DTR Fast Read Quad Output	Yes	Only the w25n01jw support this feature
	DTR Fast Read Dual I/O	Yes	Only the w25n01jw support this feature
	DTR Fast Read Dual I/O with 4-Byte Address	Yes	Only the w25n01jw support this feature
	DTR Fast Read Quad I/O	Yes	Only the w25n01jw support this feature
	DTR Fast Read Quad I/O with 4-Byte Address	Yes	Only the w25n01jw support this feature

Table 3: Feature List for Gigadevice Models

FEATURE	SUPPORT	NOTE
Write operations (Write Enable and Write Disable)	Yes	
Features operations (Get Feature and Set Feature)	Yes	
Read Operations (Page Read and Read ID)	Yes	
Power on Read with internal ECC	Partial	The power on read is supported, but the internal ECC calculation is NOT supported.
Program Operation (Page Program, Rand Data Program and Internal Data Move)	Yes	
Block Operation (Block Erase, Block Lock Feature, OTP feature, Status Register)	Yes	
ECC Protection	Partial	The spare area (128/256bytes) of each page is supported, but the internal ECC calculation and detection and correction are NOT supported.
SPI Power UP	Partial	The RESET command is supported, but the alternative SPI Power-up is NOT supported.

4. Configurations

Table 4: Configurations list the available memory model configurations. Not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

Table 4: Configurations of Micron and Macronix Models

Memory Size	RA	CA	Configuration
1 Gb	16	12	1024 blocks x 64 pages x 2112 bytes
2 Gb	17	12	2048 blocks x 64 pages x 2112 bytes
4 Gb	18	12	4096 blocks x 64 pages x 2112 bytes

Table 5: Configurations of Winbond Models

Memory Size	Die	PA	CA	Configuration
1 Gb	NA	16	12	1024 blocks x 64 pages x 2112 bytes
2 Gb	2	16	12	2 dies x 1024 blocks x 64 pages x 2112 bytes

Table 6: Configurations of Gigadevice Models

Memory Size	RA	CA	Configuration
1 Gb	***16***	***12***	***1024 blocks x 64 pages x 2176 bytes***
2 Gb	***17***	***12***	***2048 blocks x 64 pages x 2176 bytes***
4 Gb	***17***	***13***	***2048 blocks x 64 pages x 4352 bytes***

NOTE: The Winbond w25n01jwxxig/it part models are currently available in Initial Release (IR) BETA program only. These models are not in the official MMP release. Please request access to these model via an FAE, the emulation support team, or the MMP support team.

5. Model Block Diagram

The following figures show the SPI NAND model block diagrams. The VCC power pin is not supported.

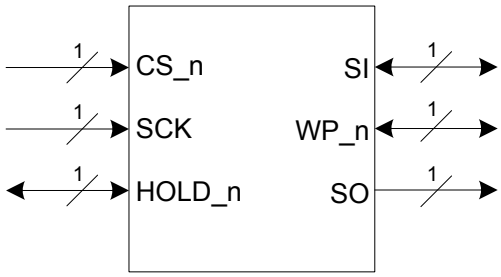
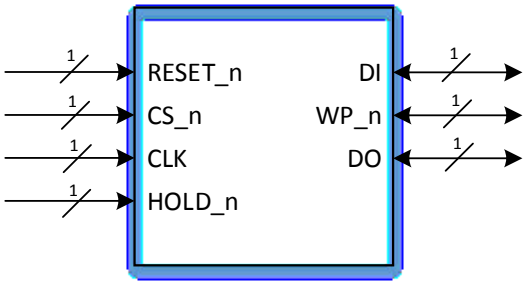


Figure 1: Micron and Macronix SPI NAND Model Block Diagram



NOTE: Only the w25n01jw support RESET_n Pin

Figure 2: Winbond SPI NAND Model Block Diagram

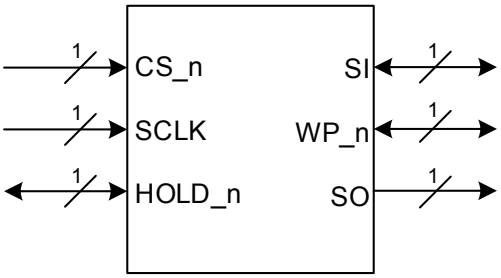


Figure 3: Gigadevice SPI NAND Model Block Diagram

6. I/O Signal Description

The tables below list and describe the model I/O signals.

Table 7: SPI NAND Model I/O Signals (Micron and Macronix Models)

NAME	TYPE	DESCRIPTION
CS_n	Input	**Chip Select**: Places the device in active power mode when driven LOW. Deselects the device and places SO at High-Z when HIGH. After power-up, the device requires a falling edge on CS_n before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. Single command and address sequences and array-based operations are registered on CS_n.
SCK	Input	**Serial Clock:** Provides serial interface timing. Latches commands, address, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK.
HOLD_n	I/O	**Hold:** Pauses any serial communication with the device without deselecting it. When driven LOW, SO is at High-Z, and all inputs at SI and SCK are ignored. Requires that CS_n also be driven LOW. HOLD_n must not be driven by the host during x4 read operations. It acts as SO3 by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK.
SI	I/O	**Serial Data Input:** Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. SI must not be driven by the host during x2 or x4 read operations. It acts as SO0 by issuing a READ FROM CACHE x2 or x4 command with data being clocked out of the device at the falling edge of SCK.
WP_n	I/O	**Write Protect:** When LOW, prevents overwriting block-lock bits if the block register write disable (BRWD) bit is set. WP_n must not be driven by the host during x4 read operations. It acts as SO2 by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK.
SO	output	**Serial data output:** Transfers data serially out of the device on the falling edge of SCK. It acts as SO1 in x2 and x4 read operation

Table 8: SPI NAND Model I/O Signals (Winbond Models)

NAME	TYPE	DESCRIPTION
RESET_n	Input	**Reset Input:** Hardware Reset, low active. Drive this pin low for a minimum period of ~1us (tRESET) will reset the device to its initial power-on state. (only the w25n01jw support RESET_n Pin)
CS_n	Input	**Serial Clock Input:** Enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress.
CLK	Input	**Serial Clock:** Provide the timing for serial input and output operations.
HOLD_n	I/O	**Hold Input (Data Input Output 3):** During Standard and Dual SPI operations, the HOLD_n pin allows the device to be paused while it is actively selected. When HOLD_n is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD_n is brought high, device operation can resume. The HOLD_n function can be useful when multiple devices are sharing the same SPI signals. The HOLD_n pin is active low. It acts as IO3 During Quad SPI operations.
DI	I/O	**Data Input (Data Input Output 0):** Serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. It acts as IO0 During Dual and Quad SPI operations.
WP_n	I/O	**Write Protect Input (Data Input Output 2):** used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin. It acts as IO2 Quad SPI operations.
DO	I/O	**Data Output (Data Input Output 1):** Transfers data serially out of the device on the falling edge of CLK. It acts as IO1 During Dual and Quad SPI operations.

Table 9: SPI NAND Model I/O Signals (Gigadevice Models)

NAME	TYPE	DESCRIPTION
CS_n	Input	Chip Select input, active low
SCLK	Input	Serial Clock input
HOLD_n	I/O	Hold input, active low / Serial Data Input Output3
SI	I/O	Serial Data Input / Serial Data Input Output 0
WP_n	I/O	Write Protect, active low / Serial Data Input Output 2
SO	output	Serial Data Output / Serial Data Input Output 1

7. Model Parameter Descriptions

The following tables provide details the user adjustable parameters for the Palladium SPI NAND memory models. These parameters may be modified when instantiating a SPI NAND wrapper or, if necessary, by modifying the HDL parameter declarations and default values which are exposed for access and debug visibility.

Table 10: User Adjustable Parameters (Micron and Macronix Models)

User Adjustable Parameter	Default Value	Description
row_width	16	The row address width
col_width	12	The column address width
num_of_fclk_cyc_1ms	5000	The number of fast clock cycles for 1ms timer. After issuing the RESET command, 1ms must elapse before issuing any other command. The parameter can be changed to a smaller number to shorten power-up time.

Table 11: User Adjustable Parameters (Winbond Models)

User Adjustable Parameter	Default Value	Description
die_id	0	Die ID. (Only used in multiple die model)
device_id	0xAA21	Device ID.
def_buf_mode	1	Default Buffer Mode. 0: Continuous Read Mode; 1: Buffer Read Mode.
def_die_status	0	Default Die Status. 0: Inactive; 1: Active;
mult_die_en	0	Multiple-die enable. For single die model set to 0. For multiple die model, set to 1.
pa_width	16	Page address width (block/page)
ca_width	12	Column address width
num_of_fclk_cyc_500us	2500	The number of fast clock cycles for 500us timer. After issuing the RESET command, 500us must elapse before issuing any other commands. This parameter can be changed to a smaller number to shorten power-up time.

Table 12: User Adjustable Parameters (Gigadevice Models)

User Adjustable Parameter	Default Value	Description
ra_width	16	The row address width
ca_width	12	The column address width
num_of_fclk_cyc_500us	2500	The number of fast clock cycles for 500us timer. After issuing the RESET command, 500us must elapse before issuing any other command. The parameter can be changed to a smaller number to shorten power-up time.

The following table provides some information about exposed parameters and localparams that are NOT user adjustable. On rare occasion the user may find one of these parameters or localparam needs adjusting for their configuration. If this case arises, please contact Cadence emulation or MMP support.

Table 13: Visible Non-User-Adjustable Localparams (Micron and Macronix Models)

Parameter / Localparam	Default Value	Description
page_width	6	The width of page address
block_width	row_width-page_width	The width of block address
size_of_page	2112	The size of one page (data area and spare area)

Table 14: Visible Non-User-Adjustable Localparams (Winbond Models)

Parameter / Localparam	Default Value	Description
page_width	6	The width of page address
block_width	pa_width-page_width	The width of block address
size_of_page	2112	The size of one page (data area and spare area)
size_of_spare	64	The size of spare area per page
num_of_lp_link	20	Number of logic-physical memory block links
manufacture_id	0xEF	Manufacture ID 0xEF: Winbond Serial Flash

Table 15: Visible Non-User-Adjustable Localparams (Gigadevice Models)

Parameter / Localparam	Default Value	Description
page_width	6	The width of page address
block_width	ra_width-page_width	The width of block address
size_of_page	2176	The size of one page (data area and spare area) For 1Gb/2Gb Part, page size is 2176 Bytes. For 4Gb Part, page size is 4352 Bytes.
manufacture_id	0xC8	Manufacture ID 0xC8: Gigadevice
device_id	0xA148	Device ID
gen_version	“C”	Generation “B” : B Version Part “C” : C Version Part

Note that there are additional exposed localparams in the model HDL that are not described here nor intended to be described here. These additional localparams are exposed for debugging purposes only and will not be described herein.

8. Address mapping

The array of the SPI NAND model is mapped into the internal memory of the Palladium system. This array is a two dimensional array of signals. The array width is 8bit and the address of the memory array is byte address. The mapping of row/page and column addresses to the internal model array is as follows:

ARRAY_ADDR = {RA, CA} // Micron, Macronix and Gigadevice models

ARRAY_ADDR = {PA, CA} // Winbond Model

For Gigadevice 1Gb/2Gb models, the 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

For Gigadevice 4Gb models, the 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4351 are valid. Bytes 4352 through 8191 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

For other models, the 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only byte 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

The array name in the model is: memcore

9. Commands

The SPI NAND memory model supports the commands listed in below tables. Please refer to the relevant SPI NAND vendor datasheet for details about the timing and bus cycles for each command.

Table 16: Command List of Micron and Macronix Models

Command Sequence	OP Code	SUPPORT	
		Micron	Macronix
BLOCK ERASE	D8h	Yes	Yes
GET FEATURE	0Fh	Yes	Yes
PAGE READ	13h	Yes	Yes
PROGRAM EXECUTE	10h	Yes	Yes
PROGRAM LOAD	02h	Yes	Yes
PROGRAM LOAD x4	32h	No	Yes
PROGRAM LOAD RANDOM DATA	84h	Yes	Yes
PROGRAM LOAD RANDOM DATA x4	34h	No	Yes
READ FROM CACHE	03h, 0Bh	Yes	Yes
READ FROM CACHE x2	3Bh	Yes	Yes
READ FROM CACHE x4	6Bh	Yes	Yes
READ ID	9Fh	Yes	Yes
RESET	FFh	Yes	Yes
SET FEATURE	1Fh	Yes	Yes
WRITE DISABLE	04h	Yes	Yes
WRITE ENABLE	06h	Yes	Yes
Internal ECC Status Read	7Ch	No	No

Table 17: Command List of Winbond Models

Command Sequence	OP Code	SUPPORT	NOTE
Device RESET	FFh	Yes	
Software Die Select	C2h	Yes	Only the w25m02gv part supports this command
JEDEC ID	9Fh	Yes	
Read Status Register	0Fh / 05h	Yes	
Write Status Register	1Fh / 01h	Yes	
Write Enable	06h	Yes	
Write Disable	04h	Yes	
BB Management(Swap Blocks)	A1h	Yes	
Read BBM LUT	A5h	Yes	
Last ECC failure Page Address	A9h	Yes	
Block Erase	D8h	Yes	
Program Data Load(Reset Buffer)	02h	Yes	
Random Program Data Load	84h	Yes	
Quad Program Data Load (Reset Buffer)	32h	Yes	

Command Sequence	OP Code	SUPPORT	NOTE
Random Quad Program Data Load	34h	Yes	
Program Execute	10h	Yes	
Page Data Read	13h	Yes	
Read	03h	Yes	
Fast Read	0Bh	Yes	
Fast Read with 4-Byte Address	0Ch	Yes	
Fast Read Dual Output	3Bh	Yes	
Fast Read Dual Output with 4-Byte Address	3Ch	Yes	
Fast Read Quad Output	6Bh	Yes	
Fast Read Quad Output with 4-Byte Address	6Ch	Yes	
Fast Read Dual I/O	BBh	Yes	
Fast Read Dual I/O with 4-Byte Address	BCh	Yes	
Fast Read Quad I/O	EBh	Yes	
Fast Read Quad I/O with 4-Byte Address	ECh	Yes	
DTR Fast Read	0Dh	Yes	Only the w25n01jw support this feature
DTR Fast Read with 4-Byte Address	0Eh	Yes	Only the w25n01jw support this feature
DTR Fast Read Dual Output	3Dh	Yes	Only the w25n01jw support this feature
DTR Fast Read Quad Output	6Dh	Yes	Only the w25n01jw support this feature
DTR Fast Read Dual I/O	BDh	Yes	Only the w25n01jw support this feature
DTR Fast Read Dual I/O with 4-Byte Address	BEh	Yes	Only the w25n01jw support this feature
DTR Fast Read Quad I/O	EDh	Yes	Only the w25n01jw support this feature
DTR Fast Read Quad I/O with 4-Byte Address	EEh	Yes	Only the w25n01jw support this feature

Table 18: Command List of Gigadevice Models

Command Sequence	OP Code	SUPPORT	
		B Version	C Version
Write Enable	06h	Yes	Yes
Write Disable	04h	Yes	Yes
Get Features	0Fh	Yes	Yes
Set Feature	1Fh	Yes	Yes
Page Read (to cache)	13h	Yes	Yes
Read From Cache	03h	Yes	Yes
Fast Read From Cache	0Bh	No	Yes
Read From Cache x 2	3Bh	Yes	Yes
Read From Cache x 4	6Bh	Yes	Yes
Read From Cache Dual IO	BBh	Yes	Yes
Read From Cache Quad IO	EBh	Yes	Yes
Read ID	9Fh	Yes	Yes

Command Sequence	OP Code	SUPPORT	
		B Version	C Version
Program Load	02h	Yes	Yes
Program Load x4	32h	Yes	Yes
Program Execute	10h	Yes	Yes
Program Load Random Data	84h	Yes	Yes
Program Load Random Data x4	C4h/34h	Yes	Yes
Block Erase	D8h	Yes	Yes
Reset	FFh	Yes	Yes

Note:
1. Program and Erase - Flash data bits may be individually programmed from the erased 1 state to the programmed logical 0 (low) state. A data bit of 0 cannot be programmed back to a 1. A succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1. Programming the same word location more than once with different 0 bits will result in the logical AND of the previous data and the new data being programmed.
2. All locations of the cache/buffer register will be set to all 1's (FFh) only after completion of PROGRAM EXECUTE.

10. Initialization Sequence

For Macronix models, about 1ms is needed after power on to load page 0 data into cache to support power-on read feature. After that, the model can be fully accessible.

For Micron models, the power-on read feature is not supported. There is no special requirement for initialization sequence.

For Winbond and GigaDevice models, about 500us is needed after power on to load page 0 data into cache/buffer to support power-on read feature. After that, the model can be fully accessible.

11. Parameter Page

The follow tables show the Parameter Page data structure and default values for the available SPI NAND memory models.

Table 19: Parameter Page Data Structure (Micron and Macronix Models)

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		00h, 00h
6-7	Features supported		00h, 00h
8-9	Optional commands supported		06h, 00h
10-31	Reserved		00h
32-43	Device manufacturer	MT29F1G01AAADD MT29F2G01AAAED MT29F4G01AAADD	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
		MX35LF1GE4AB MX35LF2GE4AB	4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device model	MT29F1G01AAADD	4Dh, 54h, 32h, 39h, 46h, 31h, 47h, 30h, 31h, 41h, 41h, 41h, 44h, 44h, 48h, 34h, 20h, 20h, 20h, 20h

Byte	Description		Value
		MT29F2G01AAAED	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 31h, 41h, 41h, 41h, 45h, 44h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F4G01AAADD	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 31h, 41h, 41h, 41h, 44h, 44h, 48h, 43h, 20h, 20h, 20h, 20h
		MX35LF1GE4AB	4Dh, 58h, 33h, 35h, 4Ch, 46h, 31h, 47h, 45h, 34h, 41h, 42h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MX35LF2GE4AB	4Dh, 58h, 33h, 35h, 4Ch, 46h, 32h, 47h, 45h, 34h, 41h, 42h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID	MT29F1G01AAADD MT29F2G01AAAED MT29F4G01AAADD	2Ch
		MX35LF1GE4AB MX35LF2GE4AB	C2h
65-66	Data code		00h, 00h
67-79	Reserved		00h
80-83	Number of data bytes per page		00h, 08h, 00h, 00h
84-85	Number of spare bytes per page		40h, 00h
86-89	Number of data bytes per partial page		00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page		10h, 00h
92-95	Number of pages per block		40h, 00h, 00h, 00h
96-99	Number of blocks per unit	mt29f1g01aaadd	00h, 04h, 00h, 00h
		mt29f2g01aaaed	00h, 08h, 00h, 00h
		mt29f4g01aaadd	00h, 10h, 00h, 00h
		mx35lf1ge4ab	00h, 04h, 00h, 00h
		mx35lf2ge4ab	00h, 08h, 00h, 00h
100	Number of logic units		01h
101	Number of address cycles		00h
102	Number of bits per cell		01h
103-104	Bad blocks maximum per unit	mt29f1g01aaadd	14h, 00h
		mt29f2g01aaaed	50h, 00h
		mt29f4g01aaadd	50h, 00h
		mx35lf1ge4ab	14h, 00h
		mx35lf2ge4ab	28h, 00h
105-106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		01h
108-109	Block endurance for guaranteed valid blocks		00h
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of ECC bits		00h
113	Number of interleaved address bits		00h
114	Interleaved operation attributes		00h
115-127	Reserved		00h
128	I/O pin capacitance		0Ah
129-130	Timing mode support		00h, 00h
131-132	Program cache timing		00h, 00h
133-134	tPROG maximum page program time	mt29f1g01aaadd	84h, 03h
		mt29f2g01aaaed	84h, 03h

Byte	Description		Value
		mt29f4g01aaadd	84h, 03h
		mx35lf1ge4ab	58h, 02h
		mx35lf2ge4ab	58h, 02h
135-136	tBERS maximum block erase time	mt29f1g01aaadd	10h, 27h
		mt29f2g01aaaed	10h, 27h
		mt29f4g01aaadd	10h, 27h
		mx35lf1ge4ab	ACh, 0Dh
		mx35lf2ge4ab	ACh, 0Dh
137-138	tR maximum page read time	mt29f1g01aaadd	64h, 00h
		mt29f2g01aaaed	64h, 00h
		mt29f4g01aaadd	64h, 00h
		mx35lf1ge4ab	46h, 00h
		mx35lf2ge4ab	46h, 00h
139-140	tCCS minimum		00h, 00h
141-163	Reserved		00h
164-165	Vendor-specific revision number	mt29f1g01aaadd	01h, 00h
		mt29f2g01aaaed	00h, 00h
		mt29f4g01aaadd	00h, 00h
		mx35lf1ge4ab	00h, 00h
		mx35lf2ge4ab	00h, 00h
166-253	Vendor specific	mt29f1g01aaadd	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 02h, 02h, B0h, 0Ah, B0h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 01h
		mt29f2g01aaaed	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
		mt29f4g01aaadd	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
		mx35lf1ge4ab	00h

Byte	Description		Value
		mx35lf2ge4ab	00h
254-255	Integrity CRC		Set at test
256-511	Value of bytes 0-255		
512-767	Value of bytes 0-255		
768+	Additional redundant parameter pages		00h

Table 20: Parameter Page Data Structure (Winbond Models)

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		00h, 00h
6-7	Features supported		00h, 00h
8-9	Optional commands supported		06h, 00h
10-31	Reserved		00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	w25n01gvxxig w25n01gvxxit	57h, 32h, 35h, 4Eh, 30h, 31h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		w25n01gwxxit w25n01gwxxit	57h, 32h, 35h, 4Eh, 30h, 31h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		w25m02gvxxig w25m02gvxxit	57h, 32h, 35h, 4Dh, 30h, 32h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		w25m02gwxxig w25m02gwxxit	57h, 32h, 35h, 4Dh, 30h, 32h, 47h, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		w25n01jwxxit w25n01jwxxit	57h, 32h, 35h, 4Eh, 30h, 31h, 4Ah, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID		EFh
65-66	Data code		00h, 00h
67-79	Reserved		00h
80-83	Number of data bytes per page		00h, 08h, 00h, 00h
84-85	Number of spare bytes per page		40h, 00h
86-91	Reserved		All 00h
92-95	Number of pages per block		40h, 00h, 00h, 00h
96-99	Number of blocks per unit		00h, 04h, 00h, 00h
100	Number of logic units		01h
101	Number of address cycles		00h
102	Number of bits per cell		01h
103-104	Bad blocks maximum per unit		14h, 00h
105-106	Block endurance	w25n01gvxxig/it w25n01gwxxig/it w25m02gvxxig/it	01h, 06h
		w25n01jwxxig/it w25m02gvxxig/it	01h, 05h

Byte	Description	Value
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115-127	Reserved	All 00h
128	I/O pin capacitance	08h
129-132	Reserved	All 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum page read time	32h, 00h
139-163	Reserved	All 00h
164-165	Vendor specific revision number	00h, 00h
166-253	Vendor specific	All 00h
254-255	Integrity CRC	Set at test
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
768+	Additional redundant parameter pages	All 00h

12. UniqueID Page

The follow table shows the UniqueID Page data structure and default values.

Table 21: UniqueID Page Data Structure

Byte	Value
000h-00Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
010h-01Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
020h-02Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
030h-03Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
040h-04Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
050h-05Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
060h-06Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
070h-07Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
080h-08Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
090h-09Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
0A0h-0AFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
0B0h-0BFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
0C0h-0CFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
0D0h-0DFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
0E0h-0EFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
0F0h-0FFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
100h-10Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
110h-11Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
120h-12Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
130h-13Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
140h-14Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
150h-15Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
160h-16Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
170h-17Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
180h-18Fh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
190h-19Fh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
1A0h-1AFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
1B0h-1BFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
1C0h-1CFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
1D0h-1DFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h
1E0h-1EFh	55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh
1F0h-1FFh	AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h, AAh, 55h

13. Limitations

1. Unsupported features are listed in Table 1: Features List for Micron and Macronix Model and Table 2: Feature List for Winbond Model and Table 3: Feature List for Gigadevice Models.
2. ECC: The spare area of each page is available but the ECC internal calculation and detection and correction are not supported.

14. Compile and Emulation

Each model is provided as protected RTL files (*.vp). The files need to be synthesized prior to the back-end Palladium compile. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64 +sv -ua +dut+mt29f1g01aaadd \
    ./mt29f1g01aaadd.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……

xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two example for Palladium classic ICE synthesis:

```
1)
hdlInputFile mt29f1g01aaadd.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog mt29f1g01aaadd.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
mt29f1g01aaadd
……

2)
vavlog mt29f1g01aaadd.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog mt29f1g01aaadd.vg
mt29f1g01aaadd
……

For Winbond Multiple die Model, two protected RTL files (*.vp) need to
to be synthesized.

For the “w25m02gvxxig” part, w25m02gvxxig.vp and w25n01gvxxig.vp is
needed.
For the “w25m02gvxxit” part, w25m02gvxxit.vp and w25n01gvxxit.vp is
needed.
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations that are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as “.”, whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

There are two data files that need to be preloaded for initialization of data.

Table 22: SPI NAND Model Preload Data File List

DATA FILE NAME	DESCRIPTIONS
xxx_parameter_page.dat	For Parameter Page information 'xxx' is the model part number name for different size: mt29f1g01aaadd / mt29f2g01aaaed / mt29f4g01aaadd / mx35lf1ge4ab / mx35lf2ge4ab w25n01gvxxig/ w25n01gvxxit/ w25n01gwxxig/ w25n01gwxxit/ w25m02gvxxig/ w25m02gvxxit/ w25m02gwxxig/ w25m02gwxxit/ w25n01jwxxig/ w25n01jwxxit/
uniqueid_page.dat	For UniqueID page information

Note:
1. For Gigadevice models, there are no data files that need to be preloaded.

The user should preload all the initial dat files for the SPI NAND Parameter Page and UniqueID Page initialization as listed in Table 22: SPI NAND Model Preload Data File List.

For Micron, Macronix and Gigadevice models ,the user also needs to set the main array 'memcore' and the cache register 'cache_reg' to all '1'.

For Winbond models ,the user also needs to set the main array 'memcore' and the data buffer register 'data_buf' to all '1'.

Below is a scripting example snippet showing the preloading of the dat files into the SPI NAND model. The user can change the SPI NAND model instance name "spi_nand_inst" as needed.

Example for Micron and Macronix models

```
……
xc xt0 zt0 run
xc memory -load %readmemh spi_nand_inst.parameter_page -file mt29f1g01aaadd_parameter_page.dat
xc memory -load %readmemh spi_nand_inst.uniqueid_page -file uniqueid_page.dat
xc memory -set spi_nand_inst.memcore
xc memory -set spi_nand_inst.cache_reg
……
```

Example for Single Die Winbond models

```
……
xc xt0 zt0 run
xc memory -load %readmemh spi_nand_inst.parameter_page -file w25n01gvxxig_parameter_page.dat
xc memory -load %readmemh spi_nand_inst.uniqueid_page -file uniqueid_page.dat
xc memory -set spi_nand_inst.memcore
xc memory -set spi_nand_inst.data_buf
……
```

Example for two-die Winbond model(s)

```
……
xc xt0 zt0 run
xc memory -load %readmemh spi_nand_inst.spi_nand_die0.parameter_page -file
w25m02gvxxig_parameter_page.dat
xc memory -load %readmemh spi_nand_inst.spi_nand_die1.parameter_page -file
w25m02gvxxig_parameter_page.dat

xc memory -load %readmemh spi_nand_inst.spi_nand_die0.uniqueid_page -file uniqueid_page.dat
xc memory -load %readmemh spi_nand_inst.spi_nand_die1.uniqueid_page -file uniqueid_page.dat

xc memory -set spi_nand_inst.spi_nand_die0.memcore
xc memory -set spi_nand_inst.spi_nand_die1.memcore

xc memory -set spi_nand_inst.spi_nand_die0.data_buf
xc memory -set spi_nand_inst.spi_nand_die1.data_buf
……
```

Example for Gigadevice models

```
……
xc xt0 zt0 run
xc memory -set spi_nand_inst.memcore
xc memory -set spi_nand_inst.cache_reg
……
```

15. Debugging

The SPI NAND model has several debugging options techniques and tips that may assist the user in isolating a problem.

- For issues that are may not be SPI NAND specific please review the *Memory Model Portfolio FAQ for All Models User Guide.*

- **Golden waveform:** A package with a reference waveform is available which shows the following command sequence:

Command sequence for Micron and Macronix models:

(1) Command – RESET
(2) Command – Set Feature to unlock all blocks
Command – Get Feature
(3) Command – Write Enable
Command – Program Load
Command – Program Execute
Command – Get Feature to check status OIP
Command – Write Disable
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache x2
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache x4
(4) Command – Internal Data Move (Page Read – Write Enable – Program Load Random Data – Program Execute)
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache x2
Command – Page Read
Command – Get Feature to check status OIP
Command – Read From Cache x4
(5) Command – Read ID
(6) Command – Read Parameter Page
(7) Command – Read UniqueID Page
(8) Command – Write OTP Space
Command – Read OTP Space
Command – Exit OTP Space
(9) Command – Block Erase

Command sequence for Winbond models:
(w25n01gvxxig/it, w25n01gwxxig/it, w25m02gvxxig/it, w25m02gwxxig/it)

(1) Function - Device Reset
command – Device Reset
command – Read Status Register(Wait Reset Done)
(2) Function – unlock all blocks
Command – Write Status Register(Protection Register)
Command – Read Status Register(Protection Register)

(3) Function – Write Main Array then Read Check
command – Write Enable
Command – Program Data Load
Command – Program Execute
Command – Read Status Register(Wait Program Done)
Command – Write Disable
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Dual Output
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Quad Output
(4) Function – Internal Data Move then Read Check
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Write Enable
Command – Randon Program Data Load
Command – Program Execute
Command – Read Status Register(Wait Program Done)
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Dual Output
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Quad Output
(5) Function – Read ID
Command – JEDEC ID
(6) Function – Read Parameter Page
Command – Write Status Register(Configuration Register)
command – Page Data Read(Page=0x01)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(7) Function – Read UniqueID Page
Command – Write Status Register(Configuration Register)
command – Page Data Read(Page=0x00)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(8) Function – Write OTP Space
Command – Write Status Register(Configuration Register)
Command – Write Enable
Command – Program Data Load
Command – Program Execute(page=0x02)
Command – Read Status Register(Wait Program Done)
Command – Write Disable
(9) Function – Read OTP Space
Command – Write Status Register(Configuration Register)
Command – Page Data Read(Page=0x02)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(10) Function – Exit OTP Space
Command – Write Status Register(Configuration Register)
(11) Function – Block Erase
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
Command – Write Enable

Command – Block Erase
Command – Read Status Register(Wait Block Erase Done)
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read

Command sequence for Winbond models:
(w25n01jwxxig/it)

(1) Function - Device Reset
command – Device Reset
command – Read Status Register(Wait Reset Done)
(2) Function – unlock all blocks
Command – Write Status Register(Protection Register)
Command – Read Status Register(Protection Register)
(3) Function – Write Main Array then Read Check
command – Write Enable
Command – Program Data Load
Command – Program Execute
Command – Read Status Register(Wait Program Done)
Command – Write Disable
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Dual Output
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Quad Output
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – DTR Fast Read
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – DTR Fast Read Dual Output
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – DTR Fast Read Quad Output

(4) Function – Internal Data Move then Read Check
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Write Enable
Command – Randon Program Data Load
Command – Program Execute
Command – Read Status Register(Wait Program Done)
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read with 4-Byte Address
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Dual I/O
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read Quad I/O
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – DTR Fast Read with 4-Byte Address
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)

Command – DTR Fast Read Dual I/O
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – DTR Fast Read Quad I/O
(5) Function – Read ID
Command – JEDEC ID
(6) Function – Read Parameter Page
Command – Write Status Register(Configuration Register)
command – Page Data Read(Page=0x01)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(7) Function – Read UniqueID Page
Command – Write Status Register(Configuration Register)
command – Page Data Read(Page=0x00)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(8) Function – Write OTP Space
Command – Write Status Register(Configuration Register)
Command – Write Enable
Command – Program Data Load
Command – Program Execute(page=0x02)
Command – Read Status Register(Wait Program Done)
Command – Write Disable
(9) Function – Read OTP Space
Command – Write Status Register(Configuration Register)
Command – Page Data Read(Page=0x02)
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
(10) Function – Exit OTP Space
Command – Write Status Register(Configuration Register)
(11) Function – Block Erase
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read
Command – Write Enable
Command – Block Erase
Command – Read Status Register(Wait Block Erase Done)
Command – Page Data Read
Command – Read Status Register(Wait Page Read Done)
Command – Fast Read

Command sequence for Gigadevice models:

(1) Function – Device Reset
Command – Device Reset
Command – Get feature(Wait Reset Done)
(2) Function – unlock all blocks
Command – Set feature(Protection Register)
Command – Get feature(Protection Register)
(3) Function – Write Main Array then Read Check
Command – Program Load
Command – Write Enable
Command – Program Execute
Command – Get feature(Wait Program Done)
Command – Write Disable
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Read From Cache
Command – Page Read
Command – Get feature(Wait Page Read Done)

Command – Read From Cache x2
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Set feature(Quad SPI Enable)
Command – Read From Cache x4
Command – Set feature(Quad SPI Disable)
(4) Function – Internal Data Move then Read Check
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Write Enable
Command – Program Load Random Data
Command – Program Execute
Command – Get feature(Wait Program Done)
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Read From Cache
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Read From Cache x2
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Set feature(Quad SPI Enable)
Command – Read From Cache x4
Command – Set feature(Quad SPI Disable)
(5) Function – Check ID
Command – Read ID
(6) Function – Write OTP Space
Command – Set feature(Feature Register)
Command – Program Load
Command – Write Enable
Command – Program Execute(page=0x02)
Command – Get feature(Wait Program Done)
Command – Write Disable
(7) Function – Read OTP Space
Command – Set feature(Feature Register)
Command – Page Read(Page=0x02)
Command – Get feature(Wait Page Read Done)
Command – Read From Cache
(8) Function – Exit OTP Space
Command – Set feature(Feature Register)
(9) Function – Block Erase
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Read From Cache
Command – Write Enable
Command – Block Erase
Command – Get feature(Wait Block Erase Done)
Command – Page Read
Command – Get feature(Wait Page Read Done)
Command – Read From Cache

- **Debug Display:** The Palladium SPI NAND memory models have available a built-in debug methodology called MMP Debug Display that is based on the Verilog system task $display. Please see the *Palladium Memory Model Debug Display User Guide* in the release docs directory for additional information.

- **Manual Configuring of this MMP Model Family**

  This MMP model supports manual configuration by accompanying the model mode register or configuration register declarations with synthesis directives, such as keep_net directives, that instruct the compiler to ensure that the relevant nets remain available for runtime forcing. For a general description of this support please see the user guide in the MMP release with path and filename *docs/MMP_FAQ_for_All_Models.pdf*.

  While MMP strongly recommends following protocol-based commands to configure MMP models, MMP recognizes that the design test environment may desire to trade off the risks inherent in streamlining or circumventing the initialization sequence part of the protocol in order to better support some testing environments.

  The following table lists the internal register path and naming along with the specification or datasheet naming for model mode registers or configuration registers that are accompanied by keep_net synthesis directives in support of such manual configuration. ONLY writeable configuration registers or fields are supported thusly. Please read the relevant datasheet for details about individual register behavior and mapping to fields.

Table 23: Writeable Mode Register / Configuration Register Info

Hierarchical RTL Naming for Writeable Configuration Related Registers & Signals	Specification or Vendor Datasheet Naming for Configuration Related Registers	Access
Registers for the Micron and Macronix models		
<model_name>.block_lock	Block Lock Register	R/W
<model_name>.otp	OTP Register	R/W
Registers for the Winbond models		
<model_name>.SRP	{SRP1, SRP0} Protection Register/ Status Register-1	R/W
<model_name>.BP	{BP3, BP2, BP1, BP0} Protection Register/ Status Register-1	R/W
<model_name>.TB	{TB} Protection Register/ Status Register-1	R/W
<model_name>.WP_E	{WP-E} Protection Register/ Status Register-1	R/W
<model_name>.OTP_L	{OTP-L} Configuration Register/ Status Register-2	R/W
<model_name>.OTP_E	{OTP-E} Configuration Register/ Status Register-2	R/W
<model_name>.SR1_L	{SR1-L} Configuration Register/ Status Register-2	R/W
<model_name>.ECC_E	{ECC-E} Configuration Register/ Status Register-2	R/W
<model_name>.BUF	{BUF} Configuration Register/ Status Register-2	R/W
<model_name>.QE	{QE} Configuration Register/ Status Register-2 Note:Only available for w25n01jwxxig/it	R/W
<model_name>.ODS	{ODS1, ODS0} Status Register-4	R/W

	Note:Only available for w25n01jwxxig/it	
<model_name>.DLP_E	{DLP-E} Status Register-4 Note:Only available for w25n01jwxxig/it	R/W
<model_name>.HS	{HS} Status Register-4 Note:Only available for w25n01jwxxig/it	R/W
<model_name>.DLP	{DLP7-DLP0} Extended Register Note:Only available for w25n01jwxxig/it	R/W
Registers for the Gigadevice models		
<model_name>.BRWD	{BRWD} Protection Register	R/W
<model_name>.BP	{BP2, BP1, BP0} Protection Register	R/W
<model_name>.INV	{INV} Protection Register	R/W
<model_name>.CMP	{CMP} Protection Register	R/W
<model_name>.OTP_PRT	{OTP_PRT} Feature Register	R/W
<model_name>.OTP_EN	{OTP_EN} Feature Register	R/W
<model_name>.ECC_EN	{ECC_EN} Feature Register	R/W
<model_name>.QE	{QE} Feature Register	R/W

Revision History

The following table shows the revision history for this document

Date	Version	Revision
June 2015	1.0	Initial release
July 2015	1.1	Update Cadence naming on front page
September 2015	1.2	Added note about synthesis options.
January 2016	1.3	Update for Palladium-Z1 and VXE
May 2016	1.4	Added Macronix part support
July 2016	1.5	Remove hyphen in Palladium naming. Remove BETA watermark for model release.
November 2016	1.6	Not clear cache register after Read from cache command, the cache register will be cleared only after completion of PROGRAM EXECUTE and RESET commands.
January 2017	1.7	Add Winbond part support
February 2017	1.8	Update Initialization Sequence
February 2017	1.9	Add power on read feature for winbond models Add Gigadevice part support. Update Initialization Sequence
March 2017	1.10	Change model name to lower case. Change Beta notes to move Winbond SPI Nand from Beta to non-Beta.
September 2017	1.11	Add Reference Datasheet table for all parts
January 2018	1.12	Modify header and footer
May 2018	1.13	Add Winbond Part w25m02gwxxig/it and w25n01jwxxig/it Add section for Manual configuration
June 2018	1.14	Remove Beta notations for GigaDevice SPI NAND gd5f*
July 2018	1.15	Update for new utility library