Technical Note

LPDDR5 Power Reduction

Introduction

This technical note describes the power-reduction features of Micron's high-performance LPDDR5 SDRAM devices compared to previous-generation LPDDR devices. For example, LPDDR5 improves energy efficiency (pJ/bit) while achieving a 6400 Mb/s maximum data rate per pin, which is 1.5 times faster than LPDDR4 (at 4266 Mb/s).

This technical note also provides the calculations Micron used to measure this power reduction, along with specific examples of the measured results to help users better understand how the features can benefit their systems.

Table 1: Summary of LPDDR5 Power Reduction Features

Bold features in this table are either new concepts in LPDDR5 or have been improved since LPDDR4X.

Feature	Details	Notes
Lower power supply	LPDDR4: V_{DD1} = 1.8V, V_{DD2} = 1.1V, V_{DDQ} = 0.6V	Refer to Figure 1.
	LPDDR5: V_{DD2H} = 1.05V, V_{DD2L} = 0.9V, V_{DDQ} = 0.5V (terminated) or 0.3V (unterminated)	
Split clock architecture	Low-speed CA CK: CK 800 MHz MAX	Low-speed CK contributes to internal CA circuit power reduction.
	High-speed data clock: WCK 3200 MHz MAX	High-speed data clock WCK only runs during read/write traffic, which reduces power.
Single-ended CK, WCK, RDQS	SOC CK/WCK Tx power is reduced by half. LPDDR5 RDQS Tx power is reduced by half.	Single-ended CK: CK is less than or equal to 400 MHz. Single-ended WCK/RDQS: WCK is less than or equal to 800 MHz.
Disabling on-die termination (ODT) for CA, DQ, WCK	Termination power is reduced at low frequencies.	DC termination power with ODT is reduced. Only data H period termination power is reduced.
DVFSC	Some LPDDR5 peripheral circuits are changed to low-voltage V_{DD2L}(0.9V) power rail at a low frequency.	DVFSC can be used at 1600 Mb/s or below.
DVFSQ	V_{DDQ} voltage is changed from 0.5V to 0.3V.	Users must determine MAX frequency for DVFSQ after signal integrity evaluation. DVFSQ can only be used with DQ ODT disabled to ensure enough DQ swing.
Deep-sleep mode	Power is reduced compared to self refresh. Exit time is very long.	Frequent deep-sleep mode entry/exit is not recommended.
Partial array self refresh (PASR), **partial array auto refresh (PAAR)**	Only segment mask is supported in LPDDR5. LPDDR5 also supports segment mask for AUTO REFRESH command.	I_{DD6} and I_{DD6DS} are reduced when enabling PASR. I_{DD5}, I_{DD5AB}, and I_{DD5pb} are reduced when enabling PAAR.

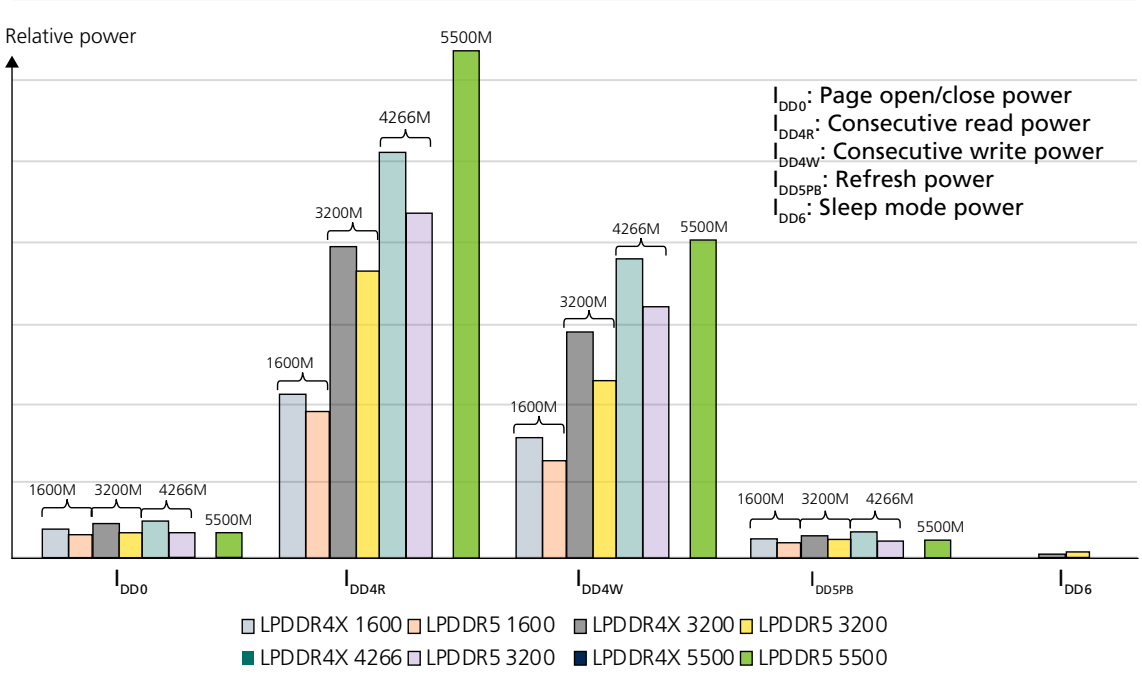
Table 1: Summary of LPDDR5 Power Reduction Features (Continued)

Bold features in this table are either new concepts in LPDDR5 or have been improved since LPDDR4X.

Feature	Details	Notes
Write X	DQ is not needed when writing all 0s to LPDDR5.	First-generation LPDDR5 only supports all-0 writes during WRITE X operation. Second-generation LPDDR5 supports all-0 writes and all-1 write control per byte during WRITE X operation.
Data copy	When the DQ[1:7] data pattern is the same as DQ0, only DQ0 is used. When the DQ[9:15] data pattern is the same as DQ8, only DQ8 is used.	-
Fine-step refresh rate multiplier	LPDDR4: Supports only x2 and x4 refresh rate multipliers at low temperatures	-
	LPDDR5: Supports much finer step multipliers to optimize A_{REF} interval	
Optimized refresh mode	Reduces refresh power for frequent self refresh entry/exit if LPDDR5 controller can follow optimized timing control requirements	-

Users can experience power reduction benefits by simply using LPDDR5. As shown in the figure below, all the LPDDR5 I_{DD}s are reduced compared to LPDDR4X, with the exception of I_{DD6}, which is almost equivalent.

Figure 1: 12Gb LPDDR4X vs. 12Gb LPDDR5 I_{DD} Comparison



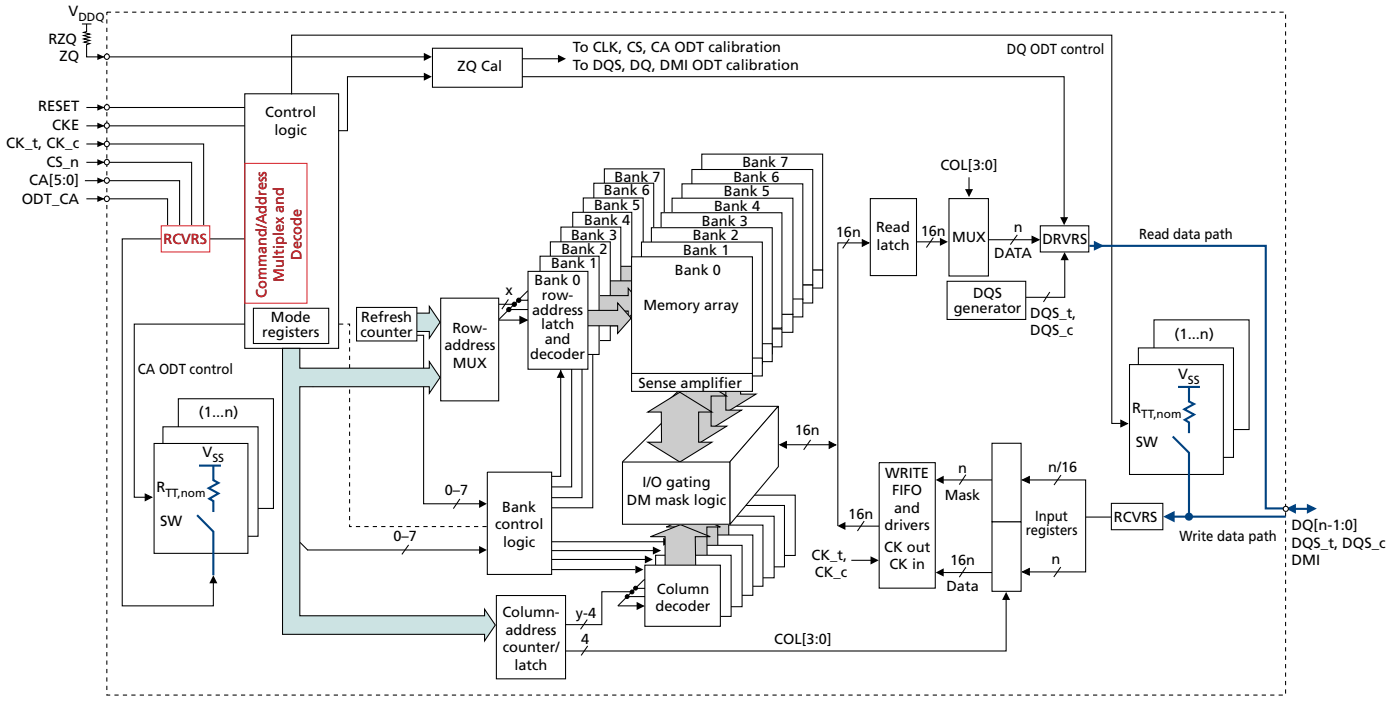
Power Reduction Estimate for Each Feature

Split Clock Architecture

While LPDDR4 devices use a high-speed (2133 MHz maximum) clock for both CA and DQ circuits, LPDDR5 uses a low-speed (800 MHz maximum) CA clock for CA circuits and a high-speed (3200 MHz maximum) data clock for data circuits. The high-speed WCK can be stopped when there is no data traffic to reduce power. The low-speed clock contributes to CA circuit power savings.

The items in red in the figure below highlight where LPDDR5 devices reduce power consumption compared to LPDDR4X by using a low-speed CK.

Figure 2: Split Clock Architecture Power Reduction



The I_{DD} values reduced in Micron's first-generation LPDDR5 are shown in the left column of the table below. These values are reduced by approximately 9mA at 800 MHz CK per die when CK Rx is enabled using the following equation:

I_{DD} reduction = 9mA x f_{ck}/800 MHz

at f_{ck} MHz CK.

The I_{DD} values in the right column of the table are not reduced because either the clock is stopped or the CK Rx is disabled.

Table 2: LPDDR5 I_{DD} Reduction

Reduced	Not Reduced
I_{DD0}	I_{DD2NS}

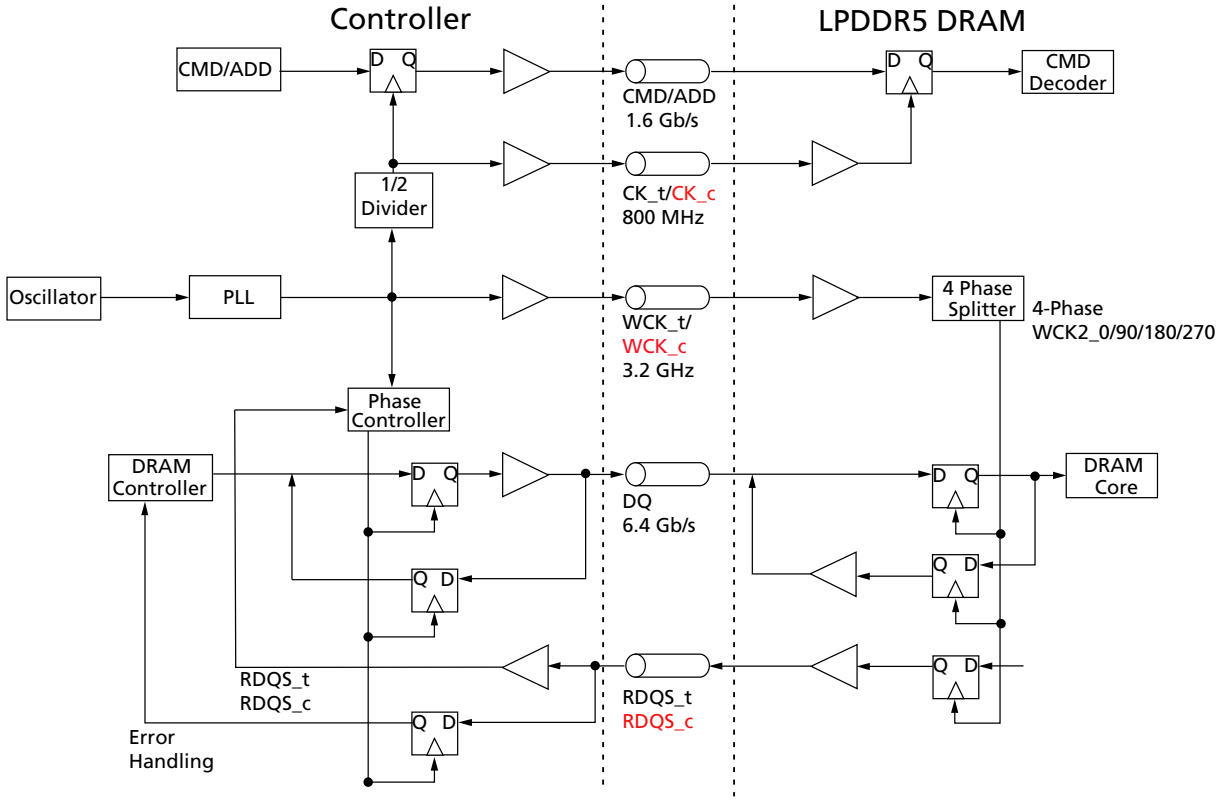
Table 2: LPDDR5 I_{DD} Reduction (Continued)

Reduced	Not Reduced
I_{DD2N}	I_{DD2P}
I_{DD3N}	I_{DD2PS}
I_{DD4R}	I_{DD3NS}
I_{DD4W}	I_{DD3P}
I_{DD5}	I_{DD3PS}
I_{DD5AB}	I_{DD6}
I_{DD5PB}	I_{DD6DS}

Single-Ended Signals (CK, WCK, and RDQS) at Low Frequency

When LPDDR5 operates at a low speed, single-ended CK, WCK, and RDQS signals can be used to save power. This reduces RDQS driver power of LPDDR5 or reduces CK and WCK driver power of LPDDR5 controller because it only needs to drive half of the differential signals. The items in red in the figure below highlight where the signal driver device stops driving in single-ended mode.

Figure 3: Single-Ended Mode Signaling



This LPDDR5 single-ended power reduction can be calculated using the following equation:

$$P = C \times f \times V_{SW}^2$$

where C = capacitive load for the signal, f = frequency of the signal, V_{SW} = signal swing.

The table below shows the signals that the driver device can drive in single-ended mode, which achieves driver power reduction. The table also shows single-ended power reduction examples for each signal type at a low frequency (300mV signal swing), per x16-wide channel, in unterminated conditions, as well as the power reduction type.

Table 3: LPDDR5 Single-Ended Power Reduction Information

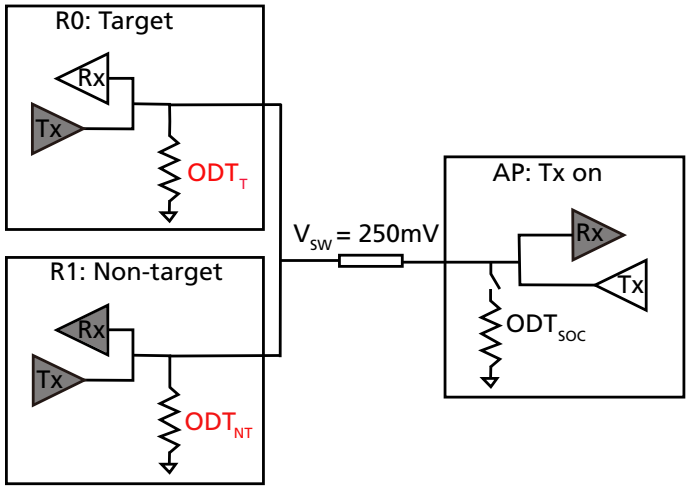
Signal	Driven by SOC or LPDDR5 in Single-Ended Mode	Power Reduction Equation Example	Reduction Type
WCK	WCK0_t and WCK1_t	2 pins x C x f_{WCK} x $0.3V^2$	SOC-side power reduction
RDQS	RDQS0_t and RDQS1_t	2 pins x C x f_{WCK} x $0.3V^2$	LPDDR5-side power reduction
CK	CK_t	1 pin x C x f_{CK} x $0.3V^2$	SOC-side power reduction

Notes:
1. SOC must drive WCK0_t, WCK0_c, WCK1_t, and WCK1_c in differential mode.
2. LPDDR5 must drive RDQS0_t, RDQS0_c, RDQS1_t, and RDQS1_c in differential mode.
3. SOC must drive CK_t and CK_c in differential mode.

Disabling ODT for CA, DQ, and WCK at Low Frequency

Disabling ODT reduces interface power. As shown in the figure below, when ODT is disabled, DC power for the items in red are reduced.

Figure 4: ODT Power Reduction for DQ Pins



DC power reduction per 1 DQ pin in an unterminated condition can be calculated using the following equation:

$$P = V_{SW}^2/(R_{ODT} \times 0.5)$$

when comparing when ODT is enabled versus disabled. Multiplying by 0.5 means that only data H period consumes termination power because ODT is terminated to V_{SS}.

LPDDR5 assumes 0.5 x V_{DDQ} = 250mV signal swing for terminated conditions, so V_{SW} should be 250mV in the ODT disable power reduction calculation shown above. When there are 16 DQ pins, 2 DMI pins, and 4 WCK pins per x16-wide channel, the power reduction for the DQ bus is calculated as follows:

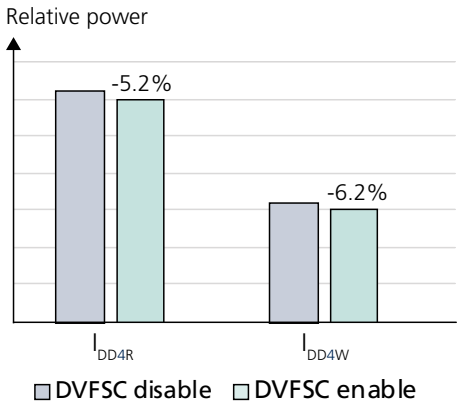
$$P = 250mV^2/R_{ODT} \times 0.5 \times 22$$

Because the LPDDR5 CA bus is considered low speed with a 800 MHz maximum CK, it is recommended to always disable ODT for CA after confirming signal integrity.

DVFSC Power Reduction

When DVFSC is enabled in Micron's first-generation LPDDR5 devices, I_{DD4R}, and I_{DD4W} can be reduced, as shown in the figure below. If the system is mostly operating at a low speed, enabling DVFSC is effective to reduce power.

Figure 5: 12Gb LPDDR5 DVFSC Power Reduction (at 1600 Mb/s)



Note: Enabling DVFSC has a timing penalty for ^{t}RCD, ^{t}WR, ^{n}WR, ^{t}RBTP, ^{n}RBTP, and RL. Refer to the product data sheet for more information.

A rough estimate of power reduction for DVFSC at particular data rate is calculated using the following equation:

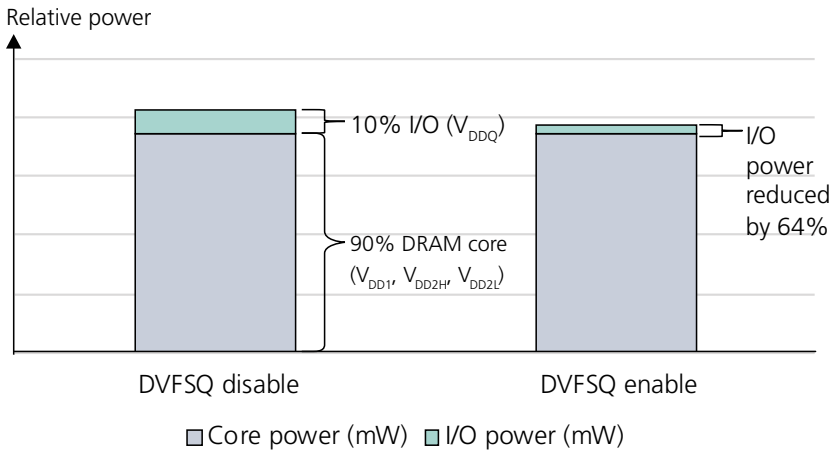
$$I_{DD4R\_DVFSC\_reduction(mW)} \times I_{DD4R\_time\%} + I_{DD4W\_DVFSC\_reduction(mW)} \times I_{DD4W\_time\%}$$

DVFSQ Power Reduction

V_{DDQ} is used as the LPDDR5 driver power supply during reads. Enabling DVFSQ reduces LPDDR5 I/O power during reads.

The figure below compares power reduction when DVFSQ is disabled and enabled at 3200 Mb/s when DQ ODT is off and Cload = 3pF. Approximately 90% power is consumed by the LPDDR5 core and 10% is consumed by I/O when DVFSQ is disabled. The I/O power portion is reduced by 64% when DVFSQ is enabled.

Figure 6: 12Gb LPDDR5 DVFSQ Power Reduction (at 3200 Mb/s)



Signal integrity must be evaluated before using the DVFSQ feature. DVFSQ power reduction is roughly calculated using the following equation:

$$P = C \times f_{WCK} \times [V_{SW1}^2 \times - V_{SW2}^2] \times n$$

where n is the number of switching signals. V_{SW1} = 500mV and V_{SW2} = 300mV, assuming unterminated mode comparison between DVFSQ enabled and DVFSQ disabled.

For example, assuming 50% of 16 DQ and 2 DMI pins are switching and 4 RDQS pins are always toggling, n is (16/2) + (2/2) + 4 = 13.

Deep-Sleep Mode Power Reduction

Deep-sleep mode is an additional self refresh mode with longer exit time that enables the device to manage internal circuits for low-current consumption specified by I_{DD6DS}. Deep-sleep mode exit time is ^{t}XSR_DSM = 200µs, which is roughly 1000 times longer than ^{t}XSR.

After the device enters deep-sleep mode, deep-sleep mode must be maintained for a relatively long period of time to sufficiently reduce self refresh current. It is functionally possible for the device to exit quickly after deep-sleep mode is issued; however, a short duration of deep-sleep mode has little effect on reducing I_{DD6} current.

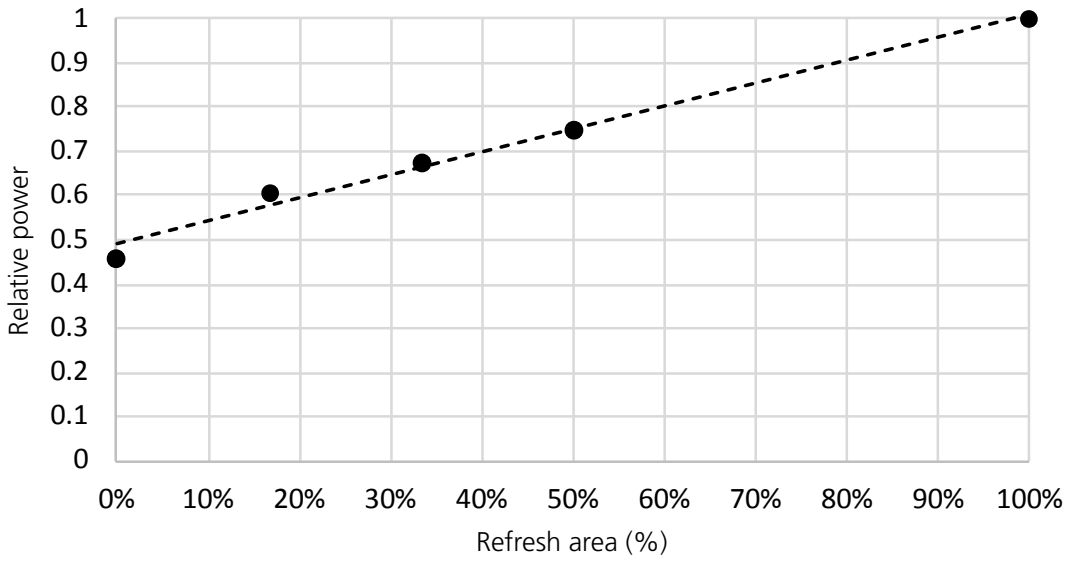
In Micron's first-generation 12Gb LPDDR5 devices, a 5.5% power reduction is expected when comparing deep-sleep mode with self refresh mode when the temperature is 25°C.

PASR, PAAR Power Reduction

PASR bank mask support is not included in the LPDDR5 specification. LPDDR5 only supports segment mask PASR as well as segment mask for the AUTO REFRESH command. In segment mask PASR, or PAAR, the masked segment does not perform the REFRESH operation for self refresh or auto refresh. Users can mask the segment with no data or not retain the data.

The figure below shows and example of power reduction percentage in Micron first-generation LPDDR5.

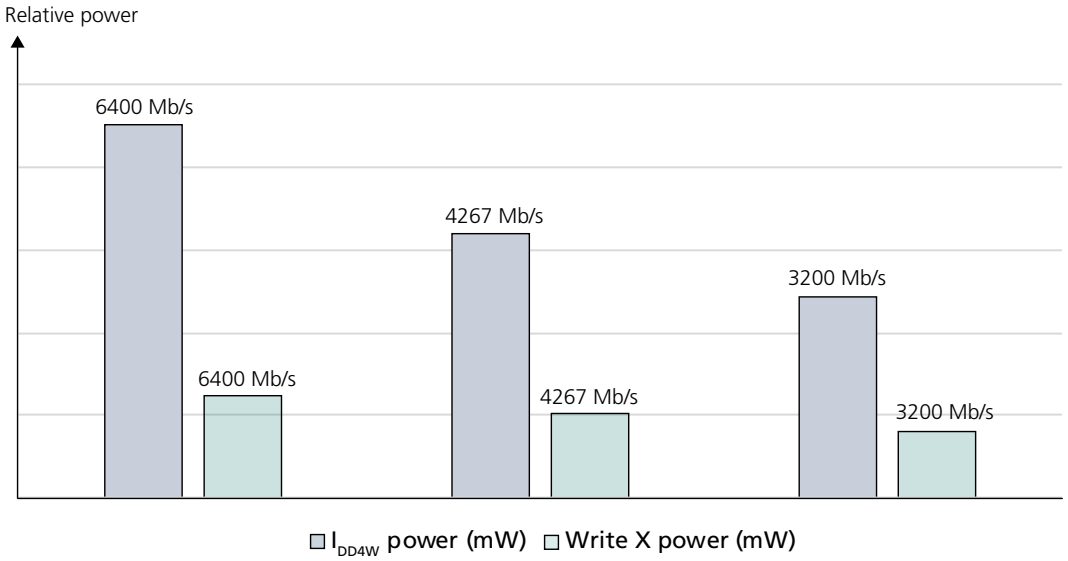
Figure 7: 12Gb LPDDR5 PASR Power Reduction at 25°C



Write X Power Reduction

During WRITE X operation, all 0s are written to the LPDDR5 device when CAS command with WRX bit = 1 is issued. DQ pins are used for the WRITE X operation. Therefore, power reduction for both SOC and LPDDR5 is expected. On the LPDDR5 side, consecutive WRITE X operation power is approximately 30% of consecutive normal WRITE operation power defined by I_{DD4W}.

Figure 8: Write X Power Reduction



Power reduction when using write X is calculated using the following equation:

$P = I_{DD4W}$ power x 70% x write X%

In typical smartphone usage, roughly 30% of the write traffic is all-0 write (that is, write X % = 30%).

Typical System Usage Results

While Micron recommends using power reduction features as much as possible to achieve longer battery life in portable devices, such as smartphones, some limitations to enabling these power reduction features with LPDDR5 are as follows:

- DVFSC maximum: 1600 Mb/s data rate
- Single-ended CK: 400 MHz maximum
- Single-ended WCK/RDQS: WCK maximum 800 MHz
- DVFSQ maximum frequency: TBD in JEDEC; this is determined by signal integrity evaluation.

The table below shows a typical smartphone frequency distribution that Micron captured in a usage analysis. With the exception of the benchmark software, LPDDR5 was mostly used at mid/low frequency, so many power reduction features could be enabled.

Table 4: Typical Smartphone Usage

Application	2736 MHz	2093 MHz	1805 MHz	1555 MHz	1018 MHz	768 MHz	682 MHz	547 MHz	451 MHz	300 MHz	200 MHz
3DMark_Slingshot[1]	81%	1%	4%	4%	5%	1%	0%	0%	4%	0%	0%
3DMark_Ex[1]	3%	0%	0%	1%	6%	2%	3%	7%	76%	0%	1%
4k_video_play	0%	0%	0%	0%	0%	0%	4%	37%	30%	22%	7%
Music	0%	0%	0%	0%	0%	0%	0%	0%	43%	56%	1%
Menu	0%	0%	0%	0%	0%	0%	1%	0%	21%	77%	0%

Note: 1. 3DMark is a benchmark software developed by UL Benchmarks.

Based on the frequency distribution above, and a read/write/refresh percentage analysis by Micron for the listed smartphone applications, power reduction was estimated as shown in the table below:

Table 5: Power Reduction in Typical System Usage

LPDDR5 Power Reduction Feature	% Power Reduction in a Typical Task	Notes
Single-ended CK, WCK, RDQS	Play video: 0.9%	CK, WCK: SOC I/O power reduction; RDQS: LPDDR5 I/O power reduction; this assumes Cload = 3pF for the signals
	Play music: 0.9%	
	Menu: 0.5%	
Disabling LPDDR5 ODT for DQ, DMI, WCK	Play video: 10.5 %	-
	Play music: 8.4%	
	Menu: 6.4%	
DVFSC	Play video: 3%	-
	Play music: 1%	
	Menu: 1%	

Table 5: Power Reduction in Typical System Usage (Continued)

LPDDR5 Power Reduction Feature	% Power Reduction in a Typical Task	Notes
DVFSQ	Play video: 3.5%	This assumes Cload = 3pF for all signals
	Play music: 3.8%	
	Menu: 1.4%	
Write X	Play video: 1.0%	Roughly 30% of the write traffic is all-0 write; write X% = 30%
	Play music: 0.6%	
	Menu: 0.5%	
Deep-sleep mode	Sleep: 5.5%	Comparison between self refresh and deep-sleep mode

Conclusion

Several power reduction features are available in LPDDR5 devices. While some limitations exist, Micron recommends using as many features as possible for system power reduction after signal integrity, system stability, and system performance are evaluated.

Revision History

Rev. A – 03/2020

- Initial release

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