Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

Memory Model Portfolio
MMP 18.1.0
Release Notes

Document Version: 1.0

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Contents

1. General Information

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

2. Memory Model Portfolio MMP 18.1.0

2.1 Introduction

The Cadence Memory Model Portfolio (MMP) provides memory device models for emulation on the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems.

2.2 Release Structure and Model File Formats

The memory models are currently provided in one format: that of encrypted RTL file(s) (*.vp for Verilog based models and *.vhdp for VHDL based models) that target use in the IXCOM flows and Classic ICE flow. The encrypted RTL (*.vp; *.vhdp) file(s) must be synthesized along with other design code prior to acceleration / emulation. Some model families also include wrapper files for various configurations (*.v).

The release is organized into types, vendors and specific parts. For example:

```
sdram/DDR3/micron/mt41j256m8.vp
```

Files used by multiple model types or families are located in local or top level *common* directories according to user guide instructions. For example, the clock block file named mmp_spi_clk_gen.v that is used by SPI/SPI EEPROM/QSPI/OSPI families is located in the top level *common* directory.

```
common/mmp_spi_clk_gen.v
```

MMP releases occur on a once per year basis while official MMP patches are generated with higher frequency between major releases. Models may move from release levels requiring Beta arrangements (IR, ER) to non-Beta release levels (MR) within an official patch release provided sufficient testing and validation has occurred.

Users are encouraged to work with the latest MMP release and patch level in order to take advantage of recent fixes.

2.3 Platform Support

MMP 18.1.0 is compatible with UXE 17.1.0 (IES), UXE 17.5.0 (XCelium) and VXE 16.1.0 (IES), VXE 16.5.0 (XCelium) and their newer software releases.

2.4 Documentation

The `docs` directory of the release contains a catalog titled "Memory_Model_Portfolio_Catalog_<release number>.pdf" that lists all the current contents of the MMP release. In addition, User Guides for different model families are provided.

2.5 Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, and may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

2.6 Model Product Levels

All models in the Memory Model Portfolio are assigned a product level. This product level informs users what set of models are accessible with their purchased product and licensing. The majority of models in the MMP library are available at the MMP_BASIC product level. Some advanced models with complex protocols and complex features are available only at the MMP_PLUS product level.

In the MMP 18.1.0 MMP Catalog and going forward, MMP_PLUS models are marked with ***MMP_PLUS*** in the column at the left hand side of the page. MMP_PLUS models are, like all models, assigned a release level and thus may have either a BETA or non-BETA status.

Access to MMP_BASIC models requires ACCEL_MEM_VIP licensing. Access to MMP_BASIC AND MMP_PLUS models requires ACCEL_MEM_PLUS licensing. Please see the MMP FAQ User Guide in the docs directory of the installed release of MMP 18.1.0 or later for additional details or consult with your Cadence sales representative.

3. MMP 18.1.0 Detailed Information

3.1 Summary

- NEW MODELS
  - Addition of more Micron DDR4 3DS parts at non-Beta (MR) level in the MMP_BASIC product level
  - Addition of Numonyx 1.8V QSPI parts n25q256a31, n25q256a11 at non-Beta (MR) level in the MMP_BASIC product level
  - Addition of Micron MLC ONFI 4.0 NAND parts: MT29F*G08C*, MT29F*T08C* at non-Beta (MR) level in the MMP_BASIC product level
  - Addition of LPDDR5 and LPDDR5 x8 JEDEC parts at Beta (MR) level in the MMP_PLUS product level
  - Addition of Cypress Hyperflash s26k*t parts at BETA (IR) level in the MMP_BASIC product level
  - Addition of QSPI Macronix part mx25u3235f and changed mx25u3235 to mx25u3235e in the MMP_BASIC product level
  - Additional parts in LPDDR4, LPDDR4X, LPDDR4 x8 single channel in the MMP_BASIC product level
  - Addition of Micron OSPI mt35xu02g at non-Beta (MR) level in the MMP_BASIC product level
  - Addition of Macronix QSPI part mx25u25645g at non-Beta (MR) level in the MMP_BASIC product level
  - Added more Micron Octal SPI mt35xu* configurations in the MMP_BASIC product level
  - Addition of Micron mt25q* and mt25t* (2-die) QSPI parts at Beta (IR) level in the MMP_BASIC product level
  - Expanded Toshiba NAND Toggle DDR2.0 parts, including TLC parts, at Beta (IR) level in the MMP_BASIC product level
  - Addition of Winbond SPI NAND (Advanced) w25n01jw* parts at BETA (IR) level in the MMP_BASIC product level
  - Addition of Winbond SPI NAND multi-die w25m02gw* parts at non-BETA (MR) level in the MMP_BASIC product level
  - Addition of AP Memory Octal SPI PSRAM aps*08l parts at BETA (IR) level in the MMP_BASIC product level

- MODEL RELEASE LEVEL CHANGES
  - Uplevel of GDDR6 parts from Beta (IR) level to non-Beta (MR) level in the MMP_BASIC product level.

- Uplevel of LPDDR4 x8 parts from Beta (IR) level to non-Beta (MR) level in the MMP_BASIC product level.
- Uplevel of UFS 2.1 parts from Beta (IR) level to non-Beta (MR) level in the MMP_BASIC product level.
  - (Note: UFS 2.0 parts are now removed from catalog per 2017 announcement in release notes for MMP 17.1.0
- Addition & uplevel of WINBOND PSRAM x8 IO w955d8mky to non-Beta MR level in the MMP_BASIC product level.
- Uplevel of Cypress HyperRam s27k* and s70k* to non-Beta MR level in the MMP_BASIC product level.
- Addition and uplevel of JSC Cellular RAM OctaRAM parts jsc*ss*8agdy parts at non-Beta (MR) level in the MMP_BASIC product level.
- The UFS 2.0 model has been retired and is no longer listed in the MMP catalog. It is replaced going forward by UFS 2.1 model which is non-Beta (MR) level.
- Uplevel of JEDEC and Samsung DDR4 LRDIMM from BETA (IR) level to non-BETA (MR) level in the MMP_PLUS product level.
- Addition and uplevel of Micron B16A & B17A Fortisflash ONFI 4.0 TLC NAND from BETA (IR) level to non-BETA (MR) level in the MMP_PLUS product level.
- Addition and uplevel of Toshiba BiCs4 Toggle DDR3 from BETA (IR) level to non-BETA (MR) level in the MMP_PLUS product level.
- Uplevel of GigaDevice SPI NAND gd5f* from Beta (IR) level to non-Beta (MR) level in the MMP_BASIC product level.

- MODEL UPDATES
  - Update LPDDR4 parts to specification revision JESD209-4B (February 2017)
  - Update DDR4 parts to JEDEC specification revision JESD79-4B (June 2017)

- FEATURES AND DOCUMENTATION
  - All new models documented in user guides.

  - The MMP 18.1.0 release structure and relevant MMP wide documentation, such as MMP Catalog (Memory_Model_Portfolio_Catalog_18.1.0.pdf), MMP 18.1.0 Release Notes (MMP18.1.0_Release_Notes.pdf), and MMP_FAQ_for_All_Models (MMP_FAQ_for_All_Models.pdf), are now updated to reflect the presence of new Memory Model Portfolio product levels. See announcements below related to current and anticipated changes in MMP content. Please also see the MMP FAQ User Guide in

the ***docs*** directory of the installed release of MMP 18.1.0 or later for additional details about MMP products and licensing or consult with your Cadence sales representative.

- All SDRAM models that include a SWI Smart Memory interface have been updated with the latest enhanced interface. See SWI documentation for details.

- Addition of Debug Display feature for all new Verilog-based models. See user guide titled “MMP_Debug_Display.pdf” for additional information.

- Addition of reference waveforms for all new model families. The release includes reference waveform packages in directories labeled “golden_waveform”

- Updated MMP_FAQ_for_All_Models.pdf

- Fixes for various problems and issues with MMP models since the last major release (MMP17.1.0) as per CCR’s listed in section 3.2 Fixes and Enhancements

- GENERAL ANNOUNCEMENTS
  - The MMP 18.1.0 library release structure and content as well as relevant MMP wide documentation, such as MMP Catalog (Memory_Model_Portfolio_Catalog_18.1.0.pdf), MMP 18.1.0 Release Notes (MMP18.1.0_Release_Notes.pdf), and MMP_FAQ_for_All_Models (MMP_FAQ_for_All_Models.pdf), now reflect the presence of new Memory Model Portfolio product levels. This product level informs users what set of models are accessible with their purchased product and licensing. The majority of models in the MMP library are available at the MMP_BASIC product level. Some advanced models with complex protocols and complex features are available only at the MMP_PLUS product level.
    - In the MMP 18.1.0 MMP Catalog, MMP_PLUS models are marked with ***MMP_PLUS*** in the column at the left hand side of the page. MMP_PLUS models are, like all models, assigned a release level and thus may have either a BETA or non-BETA status.
    - Access to MMP_BASIC models requires ACCEL_MEM_VIP licensing. Access to MMP_BASIC AND MMP_PLUS models requires ACCEL_MEM_PLUS licensing. Please see the MMP FAQ User Guide in the ***docs*** directory of the installed release of MMP

18.1.0 or later for additional details or consult with your Cadence sales representative.

- IMPORTANT: For MMP releases 18.1.0 and onward, all MMP Verilog models require for IXCOM flow use the compile phase inclusion of SystemVerilog MMP utility library related files. IXCOM flows require the *cdn_mmp_utils.svh* and *cdn_mmp_utils.sv* files located within the *utils/cdn_mmp_utils/sv* directory of the MMP install. Inclusion of this content requires the +sv option and path plus filename access to the MMP utility files. Access to the utility files can be accomplished using standard explicit path+file naming or implicit options such as -incdir. Please see the MMP FAQ User Guide (MMP_FAQ_for_All_Models.pdf) in the ***docs*** directory of the installed release of MMP 18.1.0 or later for additional details.

- IMPORTANT: For MMP releases 18.1.0 and onward, all MMP Verilog models require for use during runtime of IXCOM SW and IXCOM HW flows the loading of a dynamic library *libMMP_utils.so* located in the *utils/cdn_mmp_utils* directory of the MMP install. 64 bit and 32 bit versions of this library are available. MMP models do not require this dynamic library to be loaded during Classic ICE flows. Please see the MMP_FAQ_for_All_Models (MMP_FAQ_for_All_Models.pdf) in the ***docs*** directory of the installed release of MMP 18.1.0 or later for additional details.

- Replacement of SPI, QSPI, and OSPI VHDL models by Verilog models: A long term effort to replace existing MMP VHDL models for SPI families with Verilog model for same is ongoing. As the Verilog SPI, QSPI, OSPI models reach non-Beta maturity level they will be transitioned into official MMP patches or MMP major releases and, at the same time, the counterpart VHDL model will be immediately retired out of the release. The MMP Catalog revision history will record all such transitions.

3.2 Fixes and Enhancements

The following issues and enhancement requests have been addressed in MMP 18.1.0 release:

CCR	Family	Description
1765666	DDR4	Create new Micron 3DS DDR4 model
1797505	DDR4	Add MMP_ to non-specific verilog macro
1903241	DDR4	Request for DDR4 256GB 2 rank 8 high 3DS RDIMM model
1907064	DDR4	DQS should be z before initialization completes
1918201	DDR4	DDR4 3DS DIMM CKE inputs should not be bus
1929009	DDR4	DDR4 RDIMM DQS bus width incorrect
1805510	DDR4	ddr4_udimm for-generate & if-else generate need labels
1785650	DDR4	Data width of training data does not equal data_bits parameter value
1960874	DDR4	DDR4 update to JESD79-4B (June 2017)
1869669	DFI	Update DFI model to DFI4.0 specification
1582905	NAND FLASH	Request for ONFI4.0 MLC models
1594540	NAND FLASH	Some models need port count reduced to optimize emulation performance
1753332	NAND FLASH	Request for Micron B17A NAND flash model
1783752	NAND FLASH	ONFI NAND flash is limiting speed in 1x mode
1791957	NAND FLASH	DQS does not toggle during Status Read command
1798842	NAND FLASH	Memory becomes all 0 during cache program command
1800206	NAND FLASH	Remove PA0 is don't care feature
1802305	NAND FLASH	Model is reading incorrect data during cache read
1815747	NAND FLASH	Get Features command not working in NV-DDR2 mode
1818826	NAND FLASH	Cache Read End command causes next read command to fail
1832506	NAND FLASH	Extendable busy times for ftProg, tRead, tErase in ONFI 4.0 & TDDR2 TLC
1848211	NAND FLASH	Read ID output does not align with DQS in NV-DDR2 mode
1880930	NAND FLASH	Request for new ToggleDDR models - Toshiba BiCS4
1887764	NAND FLASH	Nand Flash ToggleDDR2 model request
1893709	NAND FLASH	Request to extend Erase, Program, Read times in ONFI4 & TDDR2 models
1895112	NAND FLASH	Remove Re_n = 0 requirement
1920344	NAND FLASH	ToggleDDR2 status polling not working within Get Features command
1925299	NAND FLASH	Multiplane read fails when enhanced status read cmd occurs after busy period
1943821	NAND FLASH	Last byte of page not read out correctly in NV-DDR2 mode
1861065	NOR FLASH	Nor flash sync read port support for Protium
1775351	QSPI	MX25U3235.vgp - OE signal of QSPI issue in QPI (4-4-4) Mode
1777460	QSPI	Provide 1.8V version of N25Q256A model (N25Q256A31 and N25Q256A11)
1782355	QSPI	Doesn’t perform erase & program cmd when bp[2:0] = 111 and the cmp =1
1792671	QSPI	mem_param read address bits is not correct
1794718	QSPI	MX25U3235E / MX25U3235F parts instead of MX25U3235
1801429	QSPI	Rename MX25U3235 to include final alpha; create MX25U3235F part
1804326	QSPI	Fix QSPI model mx25u51245g to support CE command using 60h
1850328	QSPI	Create new Micron QSPI model MT25QU256ABA
1850706	QSPI	Add new Quad SPI model mx25u25645g
1909245	QSPI	Change constant value of device id to be defined as localparam
1780517	GDDR5	Protium XDRAM update for GDDR5 and GDDR6

CCR	Family	Description
1889428	GDDR5M	gddr5m multiple driver error
1891397	GDDR5M	Row bits misalignment
1909048	GDDR5M	GDDR5M col_addr assignmemt missing msb in 8gb and 16gb models
1655008	GDDR5X	GDDR5X mmp model ixcom compile reports RTL_IGNORE_SENSE warning
1574410	GENERAL	Debug Display to output register value if register is forced & value changes
1575671	GENERAL	Add per-type and per-instance enabling of Debug Display plusargs at runtime
1575708	GENERAL	Add per-type enabling of Debug Display plusargs at compile time
1681554	GENERAL	Debug Display: Implement an initial, informative banner
1727658	GENERAL	Update new SM IF for LPDDR4/3/2 and DDR4/3 models
1775683	GENERAL	Change LPDDR4 timescale; standardize model timescale decl to 1ps/1ps
1785610	GENERAL	mt18jsf51272az_udimm has parameters that should be localparams
1836829	GENERAL	Implement an emulation model for JEDEC LPDDR5
1932575	GENERAL	Manual configuration of writeable registers by forcing for some models
1854864	HBM	Read DBI bit is not set to 1 when 4 bit changes and previous DBI was 1
1875319	HBM	HBM PTM update
1885757	HBM	HBM model from MMP works fine in IXCOM flow but doesn't work in ICE
1914734	HBM	HBM tCCDS and tCCDL parameters needs adjust for pseudo channel mode
1953938	HBM	Fix HBM PTM issue when 2 PS channels access XDRAM enable both active
1806209	HYPERFLASH	New Cypress HyperFlash model - s26k*t
1873753	HYPERFLASH	Hyperflash: wrong value for the Status register bit0 upon evaluate successfully
1748598	LPDDR4	Implement Micron LPDDR4 models for MMP catalogue
1748601	LPDDR4	Update LPDDR4 to JEDEC spec rev level JESD209-4B (FEBRUARY 2017)
1799689	LPDDR4	Request to support MRS18&MRS19 in LPDDR4 model
1830834	LPDDR4	Update LPDDR4 model to latest spec JESD209-4B
1905949	LPDDR4	LPDDR4 : Remove dqs_window glitch, remove preamble cycle glitch
1755631	MMC	Emmc model - reset issue
1781808	MMC	Block write issue when block length is set & not multiple of (1<<MEMCORE_DATA_WIDTH_MULT_LOG2)
1790855	MMC	CMD12 can't stop transaction when CMD12 end bit aligned with DATA end bit
1791379	MMC	Write CRC error flag was not cleared correctly
1800319	MMC	DATA_STROBE is 1 cycle less in HS400 mode when receive write cmd (CMD25) with CRC error
1806886	MMC	Add debug display feature for eMMC5.0 model
1839208	MMC	eMMC5.0 samsung 64GB wrapper has wrong ADDR_WIDTH value
1801414	OSPI	RESET# pin in the Octal SPI Flash models
1803237	OSPI	OSPI: mx25um51245g: update model to datasheet REV. 1.2 December, 2016
1804847	OSPI	Extended Jedec ID info missing for MT35XU512ABA1G12
1824973	OSPI	mt35xu512: For some case PP cmds & Erase cmds can not work
1849615	OSPI	Require for a new micron 2G octal SPI memory model MT35XU02G
1855720	OSPI	Add new Micron Octal SPI models to fill out MT35XUxx series
1889596	OSPI	Open command mapping information of the OSPI VHDL models
1806384	PSRAM	New Memory Model Request : x8 PSRAM
1657236	PSRAM	Numonyx PSRAM failing write and read operations
1893409	OctaRAM	Create new model OctaRAM
1783980	SPI NAND	WEL not cleared after Block erase cmd Program Execute cmd
1922012	SPI NAND	New Winbond SPI NAND model development
1925505	SPI NAND	Winbond SPI NAND: add 2Gb part w25m02gw support to existing model
1754718	UFS	UFS update for PTM and performance optimization

CCR	Family	Description
1867661	UFS	Unipro DL layer link startup issue when working in PWM-G0 mode
1875151	UFS	UFS read product name string descriptor issue
1907935	UFS	Report LUN command should be valid for normal logic units
1921226	UFS	Fix one garbage byte written into internal command receiving buffer
1946174	UFS	Fix UFS read device health descriptor issue

4. MMP PATCHES and ENGINEERING HOT FIXES

ENGINEERING PATCHES and HOT FIXES are intended to address urgent bugs with emphasis on quick turn-around time. PATCHES and ENGINEERING HOT FIXES are only tested to verify that they fix the reported customer problem, and do not undergo the full regression testing that is required by Cadence for other types of software releases.

4.1 OBTAINING AND INSTALLING PATCHES

Obtaining Patches:

New software patches are available via Cadence Online Support (COS) web site:

http://support.cadence.com

On the support.cadence.com site you can navigate to the page as follows: From the pulldown menu: Tools -> Acceleration & Emulation.

Patches on the web site have been tar'ed and compressed to speed transfer. You can choose to download a compressed tar file for a single patch or download a compressed tar file that has all the patches available so far. For example, the file MMP_18.1.0.p1.tar.gz has only a single patch (MMP_18.1.0.p1).

The file MMP_18.1.0_patches.tar.gz is a cumulative compressed tarfile containing all patches released so far for release 18.1.0.

For any technical support issues please open a Case via http://support.cadence.com or send an email to mailto:support@cadence.com. When submitting a new Case via email to the Support Center, the email requires formatting the Subject line of your email with the keyword Submit. You can also send a direct request to our HSV Support Center mailto:cva_support@cadence.com.

Installing the Patch:

1. cd <install-dir>

2. chmod +w .

3. copy the compressed tarfile MMP_18.1.0.p1.tar.gz to the current directory.

4. gzip -d MMP_18.1.0.p1.tar.gz
   (This creates MMP_18.1.0.p1.tar in the current directory.)

5. If a directory named "patch" exists, make it writeable:
   % chmod +w patch

6. tar -xvf MMP_18.1.0.p1.tar

(This creates file qlinkPatches and a subdirectory MMP_18.1.0.p1 in the patch directory).

7. Invoke qlinkPatches in one of two ways:
   1. Modify the first line in qlinkPatches to point to the correct perl path (version v5.6.1 or higher) and ensure that perl is specified with the -s switch. If there is no PERL executable present, please contact HSV support at the email address above. Invoke:

      qlinkPatches -n

      Select MMP_18.1.0.p1 from the list of patches (if any) and hit enter.

   2. If you prefer not to keep editing the first line in qlinkPatches, then you just need to invoke perl from the command line as follows:

      perl -s qlinkPatches -n

      Select MMP_18.1.0.p1 from the list of patches (if any) and hit enter.

5. Revision History

The following table shows the revision history for this document

Date	Version	Revision
July 2018	1.0	Initial release