Hardware System Verification (HSV)
Vertical Solutions Engineering (VSE)

EF3.0-NAND Flash
Palladium Memory Model
User Guide

BETA

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General Information

The Cadence Memory Model Portfolio provides memory device models for the Cadence Palladium XP, Palladium XP II and Palladium Z1 series systems. Optimizing the acceleration and/or emulation flow on these platforms for MMP memory models may require information outside the scope of the MMP user guides and related MMP documentation.

1.1 Related Publications

For basic information regarding emulation and acceleration, please refer to the following documents:

For Palladium XP and Palladium XP II:

UXE User Guide
UXE Library Developer's Guide
UXE Known Problems and Solutions
UXE Command Reference Manual
Palladium XP Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in UXE

For Palladium Z1:

VXE User Guide
VXE Library Developer's Guide
VXE Known Problems and Solutions
VXE Command Reference Manual
Palladium Z1 Planning and Installation Guide
Palladium Target System Developer's Guide
What's New in VXE

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EF3.0-NAND Flash Palladium Memory Models

1. Introduction

The Cadence Palladium EF3.0-NAND Flash Models are based on the following data sheet specifications of EF3.0-NAND devices:

Samsung EF(Error Free)-NAND 3.0 M-die datasheet Rev. 0.1 Jan. 29, 2011

The models do not include the internal microcontroller which supports switching between dual and single channel modes. Therefore, single channel mode is not supported.

The models support both asynchronous and synchronous or DDR interface however some functions are supported in asynchronous interface only. Please check the data sheet for more details.

Generally the models are available in several configurations with model sizes to match real devices manufactured by the vendors.

However currently only one size is available, please consult the memory model catalog for the current available list.

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2. Model Release Levels

All models in the Memory Model Portfolio are graded with a release level. This release level informs users of the current maturity and status of the model. All families in the library are graded at one of these levels.

The different levels give an overall indication of the amount of testing, level of quality and feature availability in the model. For details on supported features check the User Guide for that particular model family.

There are three release levels for models in the MMP release.

Release Level		Model Status	Available in Release	Listed in Catalog	Requires Beta Agreement
Mainstream Release	MR	Fully released and available in the catalog for all customers to use.	Yes	Yes	No
Emerging Release	ER	Model has successfully completed Beta engagement(s). Most, but not all features have been tested. Documentation is available.	No	Yes	Yes
Initial Release	IR	Model has completed initial development and has been released to Beta customer(s). The model may have missing features, may not be fully tested, may not have documentation. Model may contain defects.	No	Yes	Yes

Access to Initial Release and Emerging Release versions of the models will require a Beta Agreement to be signed before the model can be delivered.

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3. Configurations

The following table lists the configurations specified in the data sheet listed above. It is possible that not all configurations are available from all vendors. Please consult the appropriate vendor site for details on the parts they offer.

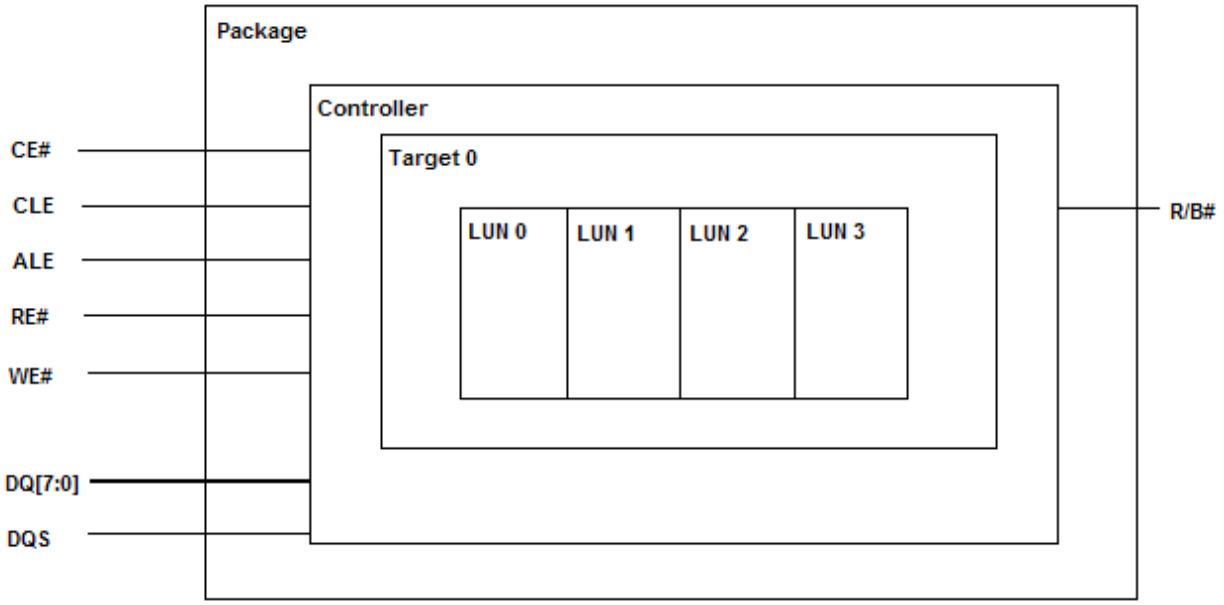
Model	Density	Level	# of CAU per CE	# of CE#	I/O	Interface
KLEBG4GW1M	**32GB**	**MLC**	**8**	**2**	**Common**	**Sync/Async**

Notes: MLC = 2bits/cell, 128 pages per block, 2K blocks per CAU
Common I/O = 1 set of pins
(pin set: ALE,CLE,DQ,DQS,RE#,WE#,RB#)
CAU, and LUN are used interchangeably
Target and CE# are used interchangeably
Synchronous, DDR, and Toggle refer to the same interface
EF3.0-NAND models have 8KB (8192+32 bytes) per page

4. Model Block Diagram

These models are implemented modularly based on the LUN core, which is instantiated as many times as needed within each model. The user does not need to instantiate the core directly. The user instantiate the model based on the model's number of LUNs.

A block diagram of a model that has 4 CAUs or LUNs is shown below.



The following block diagram shows a model that has 8 LUNs.

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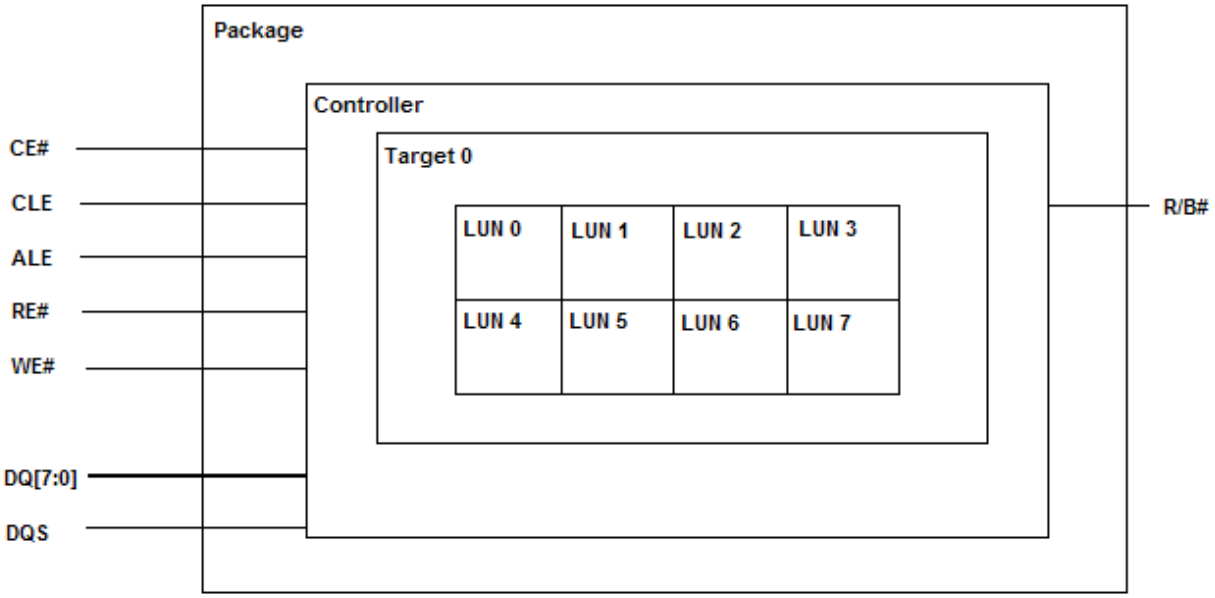

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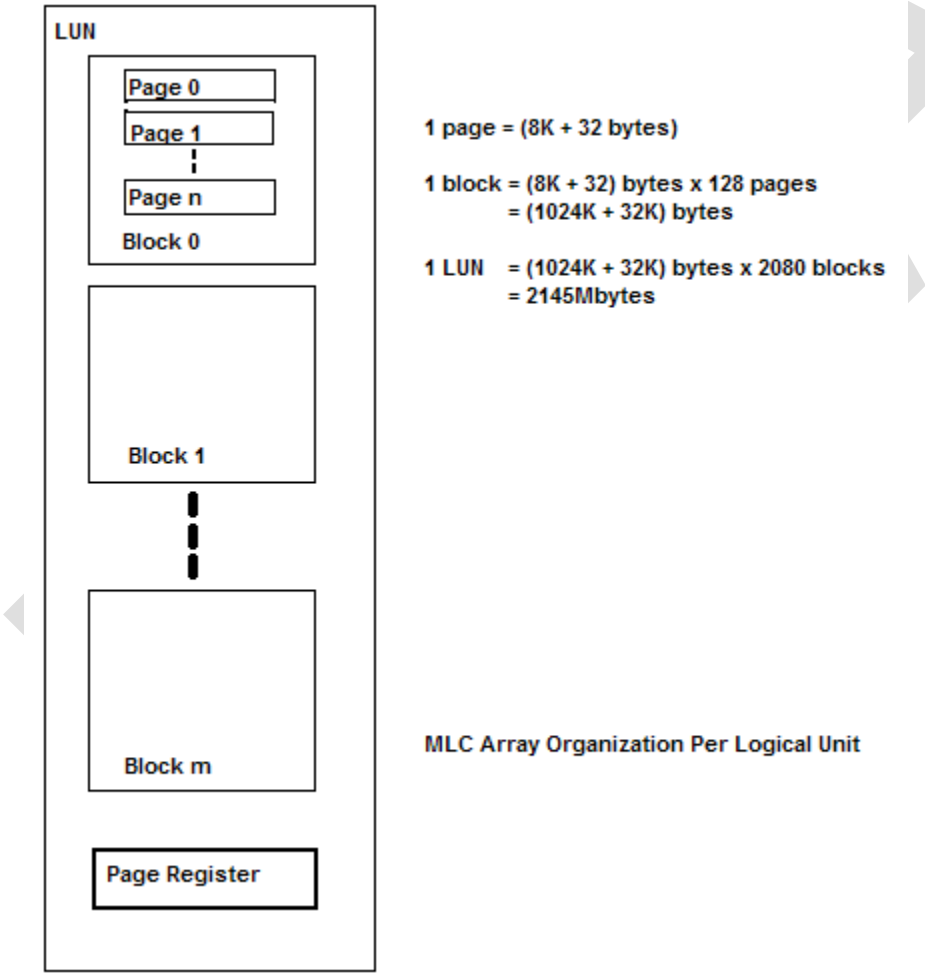
5. Address mapping

The array of the EF3.0-NAND Flash model is mapped into the internal memory of the Palladium system. This array is a single two dimensional array. The mapping of lun, block, page and column addresses to the internal model array is as follows:

ARRAY_ADDR = { LA, BA, PA, CA}

This information is required if the memory needs to be preloaded with user data. Here are the array organization and addressing cycle table for MLC models.

Array Organization for MLC Array



Address Cycle Table for MLC Array

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Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	CA13	CA12	CA11	CA10	CA9	CA8
Third	BA0	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1
Fifth	LOW	LA3	LA2	LA1	LA0	BA11	BA10	BA9
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Notes:
CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

Column addresses 8224 (2020h) through 16383 (3FFFh) are invalid, out of bounds, does not exist in the device, and cannot be addressed.

Blocks 2080 through 4095 are invalid, do not exist in the device, and cannot be addressed.

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6. Feature Address Mapping

In the EF3.0-NAND Flash data sheet there are up to 64K possible feature addresses and the largest data size is the scratch pad which is one perfect page size. For a page size of 8224 bytes, a 64K x 16K or 1GB array is needed if using one page per feature address. In order to minimize memory usage the Palladium models implement a 512 x 32 or 16KB mapped array. The following table provides the mapping for each feature address. This mapping allows for a page size of 32 bytes and multiple pages are allocated to features that are larger than 32 bytes. For example the scratch pad is allocated 257 pages at the end of the array. The table is useful for creating a data file to preload the feat_array for features such as Die Unique ID and Marketing Name. The path to the feat_array is <path.to.model.inst>.feat_array. Addresses are in hex.

A1	A2	feat_array	Feature Name	bytes
80	01	0000	Power State	1
80	04	0020	Allow saving debug info	1
80	05	0040	Idle Counter	4
80	10	0060	FW/FWA Update	4
80	12	0080	FW Versions	64
80	13	00c0	FWA Versions	4
80	20	00e0	Drive Strength	1
80	21	0100	Device Clock Frequency	1
80	22	0120	Impedance Calibration Enable	1
80	24	0140	Impedance Calibration Override	2
80	30	0160	Program Failed Pages	512
80	31	0360	Program Retired Pages	512
80	32	0560	Program Ignored Pages	512
80	33	0760	Clear Program Error Lists	1
80	40	0780	DQS# Enable	1
80	41	07a0	RE Enable	1
80	42	07c0	Vref Enable	1
80	50	07e0	Number of Die Prog in Parallel	1
80	51	0800	Number of Die Read in Parallel	1
80	52	0820	Number of Die Erase in Parrallel	1
80	60	0840	Current Channel FW Updatable	1
80	61	0860	Current Channel BFH capable	1
80	70	0880	Cyclic Redundancy Check (CRC)	1
80	71	08a0	Peak Power Management (PPM) Disable	1
80	72	08c0	Single Host Channel (SHC) Mode Enable	1
80	80	08e0	Physical page size	4
80	81	0900	ECC chunk size	4
80	82	0920	ECC code size	4
80	83	0940	CAU Physical Pairing	64
80	90	0980	Current FW version	16
80	91	09a0	FW size	2
80	A0	09c0	Package assembly code	16
80	A1	09e0	Controller unique ID	16
81	A1	0a00	Controller HW ID	16

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90	00	0a20	Enable bitflips/1KB data collection	1
90	10	0a40	Enable In Depth Health Monitoring	1
90	11	0a60	Get In Depth Health Monitoring Grades	2
90	20	0a80	Get Device Temperature	2
A0	00	0aa0	Set Debug Data Generic Configuration	4
A0	01	0ac0	Set Debug Data Vendor Specific Config	4
A0	08	0ae0	Delete Debug Data	1
82	00	0b00	NAND die 00 unique ID	16
82	01	0b20	NAND die 01 unique ID	16
82	02	0b40	NAND die 02 unique ID	16
82	03	0b60	NAND die 03 unique ID	16
83	00	0b80	NAND die 00 Chip ID	8
83	01	0ba0	NAND die 01 Chip ID	8
83	02	0bc0	NAND die 02 Chip ID	8
83	03	0be0	NAND die 03 Chip ID	8
84	00	0c00	CAU 00 Bad Block Bitmap Array	256
84	01	0d00	CAU 01 Bad Block Bitmap Array	256
84	02	0e00	CAU 02 Bad Block Bitmap Array	256
84	03	0f00	CAU 03 Bad Block Bitmap Array	256
85	00	1000	Die 00 NAND Marketing Name	10
85	01	1020	Die 01 NAND Marketing Name	10
85	02	1040	Die 02 NAND Marketing Name	10
85	03	1060	Die 03 NAND Marketing Name	10
80	03	1fe0	Scratch Pad	8224

Please note that even though all feature address locations can be set and get not all features are supported. The following features are supported:

Low Power Mode
Normal DDR Mode
Normal Async Mode
Scratch Pad
CRC for Type A Page Read, Get Features, Page Program, Set Features

All other features are unsupported.

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7. ID Operations

7.1. READ ID

The READ ID parameters for addresses 00h and 30h have been hardcoded into each model. Therefore user data file is not required.

7.2. READ PARAMETER PAGE

The data for the parameter page is provided in the <model_name>_param.dat file. This data file should be preloaded into the model if the user wants to read device parameters from the model. The path to each model's parameter page is as follows:

<path.to.model.inst>.param_page

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8. Commands

The EF3.0-NAND Flash model accepts the following commands:

- Page Read
- Page Program
- Block Erase
- Reset
- Read ID
- Read Status
- Multipage Read
- Multipage Program
- Multipage Prep
- Multiblock Erase
- Get Next Operation Status
- Operation Status
- Read Serial Output
- Controller Status
- Read Device Parameters
- Set Features
- Get Features

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The following table shows the command set as described in the EF3.0-NAND data sheet.

Function	1st Set	Address Cycles	2nd set	Mode Used
Legacy Commands				
Page Read	00h	6	30h	Low Power
Page Program	80h	6	10h	Low Power
Block Erase	60h	4	D0h	Low Power
Reset	FFh	-	-	Both
Read ID	90h	1	-	Both
Read Status	70h	-	-	Low Power
Extended Commands				
Multipage Read	07h----0Ah	4,8	37h	Normal
Multipage Program	87h----8Ah	4	17h	Normal
Multipage Prep	B0h	3	B8h	Normal
Multiblock Erase	67h----6Ah	4	D7h	Normal
Get Next Operation Status	77h	-	-	Both
Operation Status	7Dh	-	-	Both
Read Serial Output	7Ah	-	-	Both
Controller Status	79h	-	-	Both
Read Device Parameters	92h	1	97h	Both
Set Features	EFh	2	E7h	Both
Get Features	EEh	2	E7h	Both

Notes from EF3.0-NAND data sheet:

1. Commands like Multipage Read, Multipage Program, and Multiblock Erase have two types of 1st commands. The first type (XXh---) is the one used in all pages/blocks other than the last. The second type (---XXh) is used only for the last page/block.
2. For commands with a 2nd set, if a new 1st set command is issued before the confirm command (2nd set) on the previous operation, then the previous operation is discarded. For example, if the host first issues a EEh command (without E7h), and then issues either a command with only a 1st set (e.g. 77) or a complete command with a 1st and 2nd set (92h---97h), the device shall ignore the first incomplete EEh command.
3. Once a multiple pages/blocks operation is in progress the host shall only send homogeneous commands per the ongoing operation until there are no commands in progress and the operation status queue is cleared.
4. Commands that are supported in Normal mode shall be supported in both asynchronous mode and DDR mode. The host shall guarantee that the correct protocol is followed for both async and DDR models.
5. All DDR input/output shall have an even number of bytes.
6. Whe setting to Normal Mode, the host shall set either to enter async mode or DDR mode. Only at the Low Power Ready Model shall the device be able to switch between async mode or DDR mode.

9. Compile and Emulation

The model is provided as a protected RTL file(s) (*.vp). The file(s) need to be synthesized prior to the back-end Palladium compilation. An example of the command for compilation (including synthesis) and run of this model in the IXCOM flow is shown below.

```
ixcom -64 +sv -ua +dut+<model_name> \
    ./<model_name>.vp \
    ./ppn16g.vp ./ppn_2.vp \
    -incdir ../../../utils/cdn_mmp_utils/sv \
    ../../../utils/cdn_mmp_utils/sv/cdn_mmp_utils.sv \
    ……
```


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```
xeDebug -64 --ncsim \
    -sv_lib ../../../utils/cdn_mmp_utils/lib/64bit/libMMP_utils.so -- \
    -input auto_xedebug.tcl
```

The script below shows two examples for Palladium classic ICE synthesis:

```
1)
hdlInputFile <model_name>.vp
hdlImport -full -2001 -l qtref
hdlOutputFile -add -f verilog <model_name>.vg
hdlSynthesize -memory -keepVhdlCase -keepRtlSymbol -keepAllFlipFlop
<model_name>
……

2)
vavlog <model_name>.vp

vaelab -keepRtlSymbol -keepAllFlipFlop -outputVlog <model_name>.vg
<model_name>
……
```

NOTE: It is common for Palladium flows to require –keepallFlipFlop since it removes optimizations which are in place by default. For example, without –keepAllFlipFlop, HDL-ICE can remove flops with constant inputs and merge equivalent FF. The picture above is modified a bit when ICE ATB mode (–atb) is used since then a constant input FF is only optimized out when there is no initial value for it or the initial value is the same as the constant input value.

It is also common for Palladium flows to require –keepRtlSymbol. This option enables the HDL Compiler to keep original VHDL RTL symbols, such as ".", whenever possible. In other words, it maps VHDL RTL signal name a.b to the netlist entry, \a.b. Without this modifier, the signal name would otherwise be converted to a_b in the netlist.

If the recommended compile script includes the aforementioned options, the user must include them to avoid affecting functionality of the design.

10. Initialization Sequence

The EF3.0-NAND Flash model requires that the memory controller or host follows the initialization sequence as documented in the specification. The sequence basically entails the following steps.

1. The Low Power asynchronous interface is active by default for each target.
2. The RESET (FFh) command must be the first command issued to the target (CE#). The target will become busy. The RESET busy time can be monitored with the R/B# pin or checked by polling the status register with the 70h status command.
3. Read configuration data from the model using READ ID, READ PARAMETER PAGE, etc.
4. Issue Set Features command to set power mode.

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5. The model is now initialized and ready for normal operation.

The model requires that these steps are performed in the correct sequence in order to complete initialization. The model will not respond to any others commands unless this sequence is completed.

11. Model Size

To reduce memory utilization each CAU has only 32 blocks but the actual device has 2080 blocks. If larger size is needed please contact Customer Support.

12. Limitations

1. Set Features command supports only a few basic features such as crc, power modes, async and ddr interfaces, and scratch pad. Please see the Feature Address Mapping section for more details.
2. ECC is not supported.
3. Model does not check illegal sequence of command cycles.
4. Model does not check for attempts to program a bit to 1, user should make sure the block is erased before program.
5. The model does not support dynamically switching between Dual and Single Host modes of operation. The current model only supports Dual Host mode.
6. Model does not support timing parameters, except tRHOH.
7. The time to program a page or erase a block is 1 fclk (fast clock) per address location.

13. Timing Parameter tRHOH

The model does not generally support timing parameters because it is cycle based. However tRHOH (an asynchronous mode parameter that controls RE# HIGH to output hold) is supported in number of fclks (fast clocks). The user may define a macro at compile time to hold the data by a number of fclks after RE# goes high. Use this macro only if data output is not already held long enough. The model holds the data valid for 2 fclks by default. The data can be held 3 additional fclks by using the following example command line option in ixcom flow:

```
vlan +define+tRHOH=3
```

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14. User Guide Revision

The following table shows the revision history for this document

Date	Version	Revision
September 2013	1.0	Initial Release
July 2014	1.1	Repaired doc property title. Updated legal.
September 2014	1.2	Remove version from UG file name. Update UXE / IXE documentation reference titles.
November 2014	1.3	Remove emulation capacity info. Update related publications list.
March 2015	1.4	Add timing parameter limitation and a section on tRHOH.
July 2015	1.5	Update Cadence naming on front page
January 2016	1.6	Update for Palladium-Z1 and VXE
July 2016	1.7	Remove hyphen in Palladium naming
January 2018	1.8	Modify header and footer
July 2018	1.9	Update for new utility library

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