Micron Joint Development Proposal W/ SOC Partner

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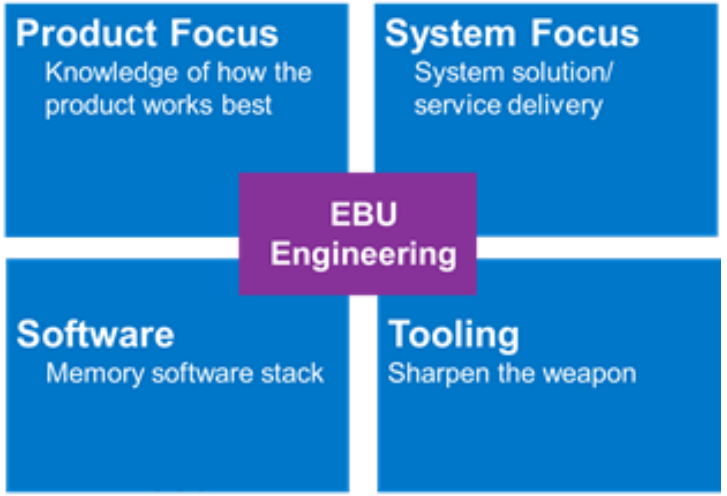
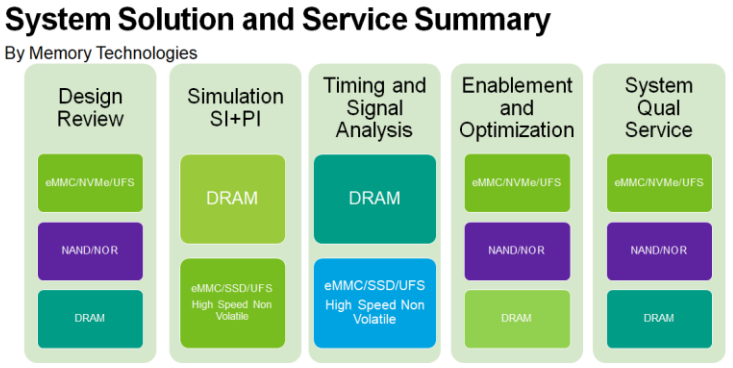
12/22/2020

System Lab Solution & Collaborations

- Closer, Leadership and Strong teams
- Solution from design to production
- Cover all embedded products and technologies





Problems We are facing & Our Advantages

Fast Technologies Pace

Micron 12 months cadences on litho and technologies /Design changes

- 110s (running) , 130s (designing)

SOC

- LP4/LP4x/LP5/LP5x/GDDR6
- Driven by market needs in a very fast pace
  - Performance /feature/cost concern and collaborations

Booming applications and customer designs

Different applications/end customers

- Request to system robustness under different applications
  - System Function/ Workloads/Temperature
  - System Variance (PCB Design and Process)
- Enormous customer Issues debug support and innovations

What we should do

Leverage advantages from both sides

- Strong presence on R&D team
- Micron – Shanghai DRAM/other Develop Team and System Team
- SOC – China/APAPC based design and other teams

Proposal

Pre silicon

- **Joint Simulation on SOC DRAM Controller Design and Micron DRAM**
- **How it works**
  - Leverage micron verification team & DRAM models with customer SOC DRAM simulation input (VCD format) , to validate future products/litho at “Very early validation before silicon out
- **Values**
  - Cover future Micron DID/SOC models
  - Reduce risk by early alignment and solution/fix
  - Proved ROI positive per Micron experience

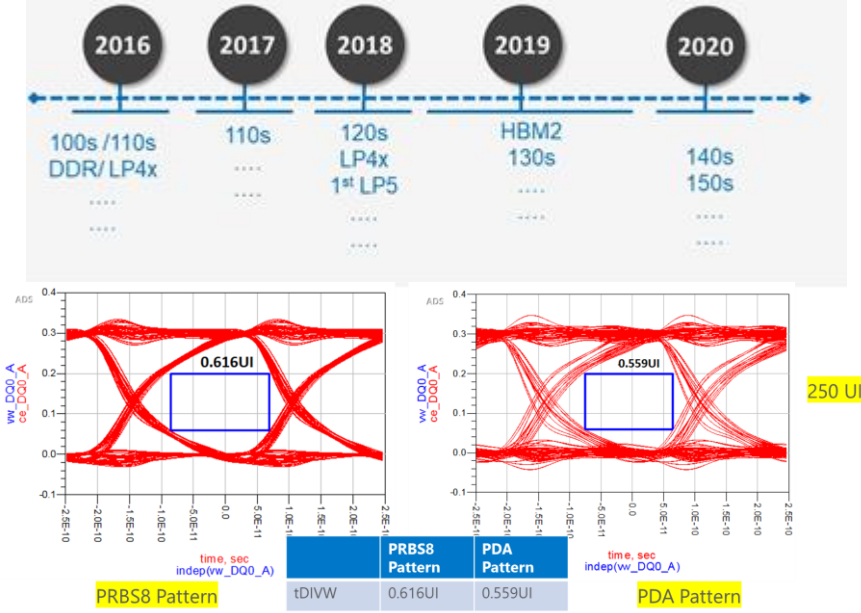
1st Silicon and Reference Board (partially doing)

- Pre and Post PCB Simulation for SI/PI Simulation
- **PDA simulation for worst pattern (Reference only)**
- **Timing and Signal measurement**
- **DRAM training /initialization/timing – Strongly recommendation**
- **Values**
  - Understand and evaluate the margins
  - Identify improvements area for next generation/ system solution

Customer Support (New)

- DRAM Test mode Entry enablement for debug- complementary measurements for engineering experiments
  - Test mode can provide a way to toggle DRAM timing/delay/features by leverage DRAM internal testing
- Other debug method /tools/ innovations

DRAM Verification Plan



Initialization and Tuning Flow Validation and Optimization