Product Specification

(Preliminary)

Product Name: VGM128064C3W01

Product Code: M00980

Customer
Approved by Customer
Approved Date:

Designed By	Checked By	Approved By	
		R&D	QA
2012.1.17	2012.1.18	2012.1.17	2012.1.18

CONTENT

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
Y01	Initial release	2012-01-13	

1 Overview

VGM128064C3W01 is a monochrome OLED display module with 128×64 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

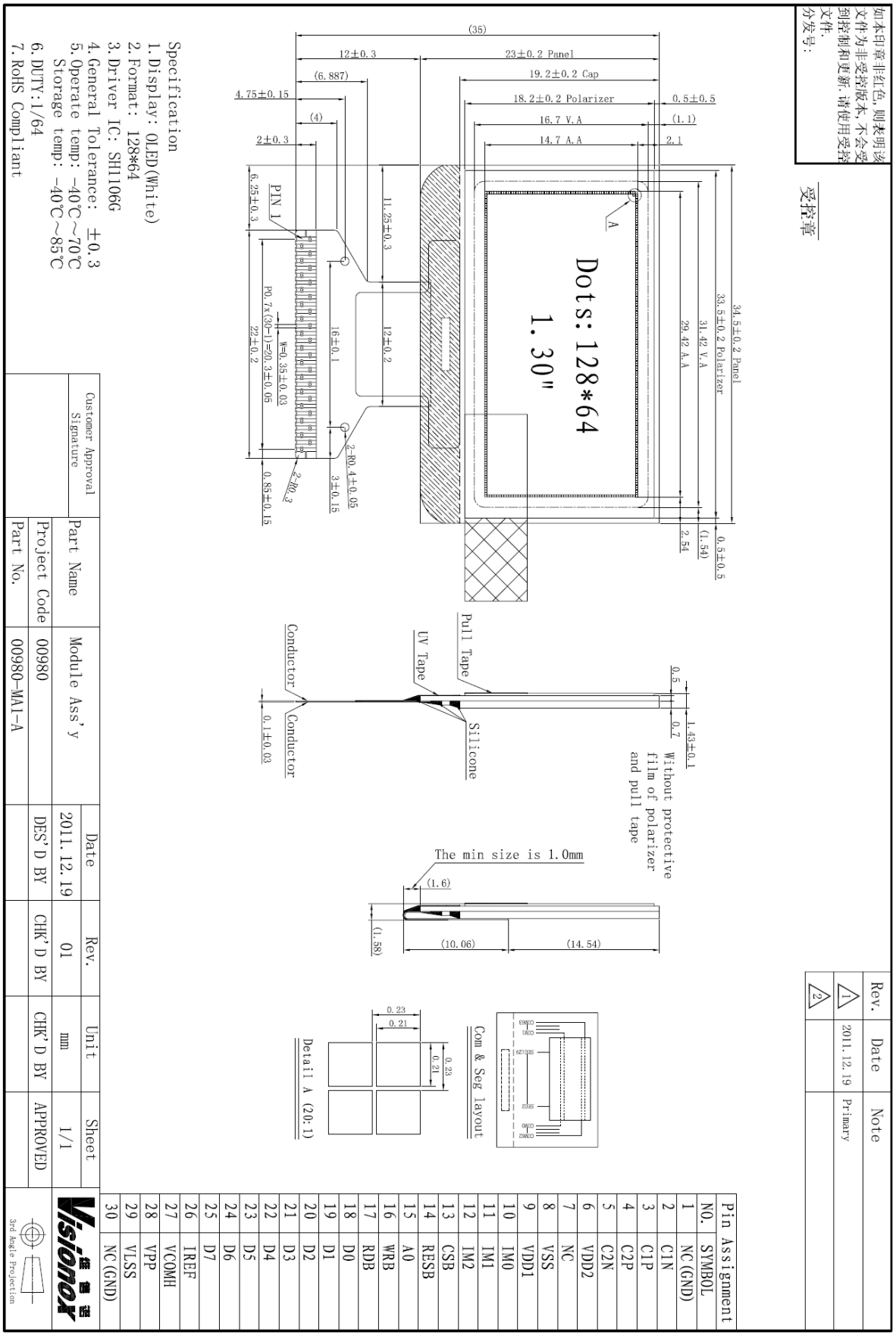
2 Features

- Display Color: White
- Dot Matrix:128×64
- Driver IC: SH1106G
- Interface: 8-bit 8080,8-bit 6800, I^2C, 3-wire & 4-wire SPI
- Wide range of operating temperature: -40℃ to 70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×64(H)	-
2	Dot Size	0.21(W)×0.21(H)	mm^2
3	Dot Pitch	0.23(W)×0.23 (H)	mm^2
4	Aperture Rate	83	%
5	Active Area	29.42(W)×14.7 (H)	mm^2
6	Panel Size	34.5(W)×23 (H) ×1.2(T)	mm^3
7	Module Size	34.5 (W)×35(H) ×1.43(T)	mm^3
8	Diagonal A/A Size	1.30	inch
9	Module Weight	TBD	gram

4 Mechanical Drawing



Pin Assignment		
NO.	SYMBOL	
1	NC(GND)	
2	C1N	
3	C1P	
4	C2P	
5	C2N	
6	VDD2	
7	NC	
8	VSS	
9	VDD1	
10	IM0	
11	IM1	
12	IM2	
13	CSB	
14	RESB	
15	A0	
16	WRB	
17	RDB	
18	D0	
19	D1	
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	
26	IREF	
27	VCOMH	
28	VPP	
29	VLSS	
30	NC(GND)	

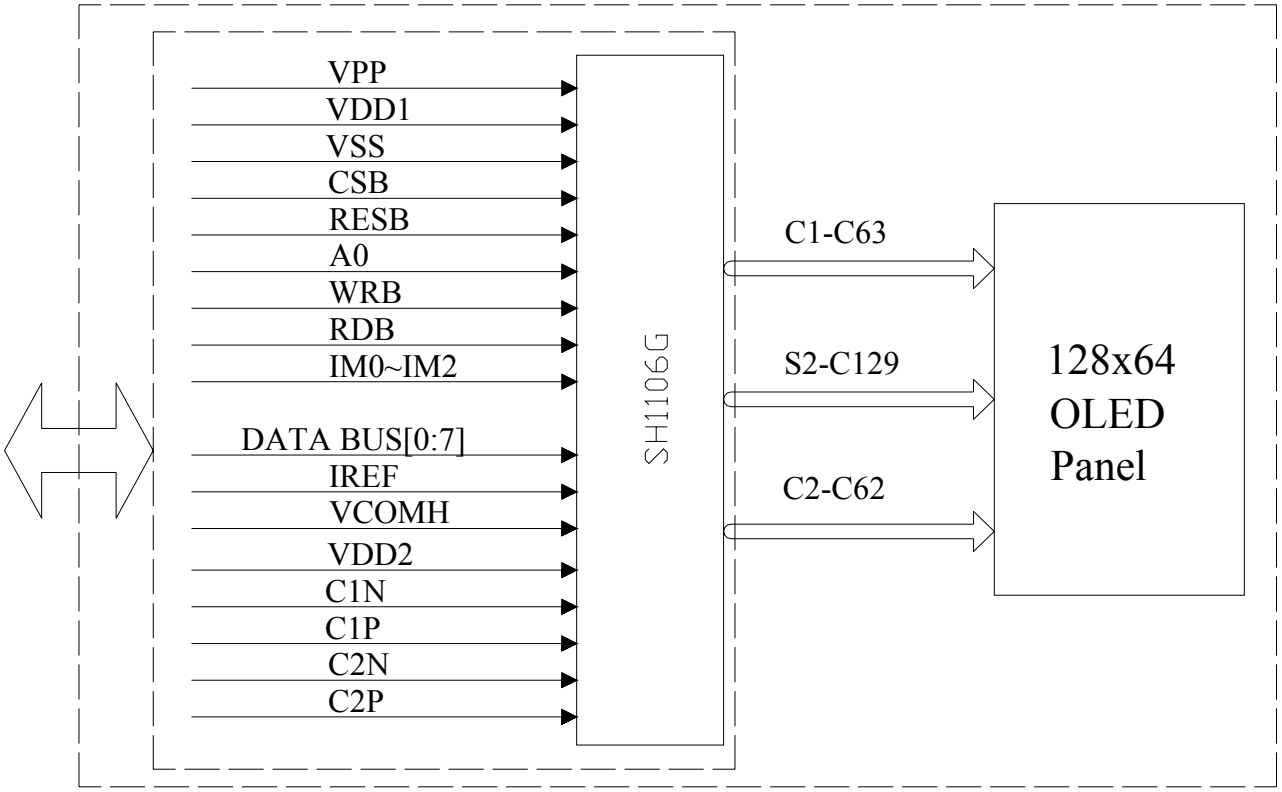
5 Module Interface

<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>No Connection.</td></tr>
<tr><td>2</td><td>C1N</td><td rowspan="2">Connect to charge pump capacitor.
These pins are not used and should be disconnedted when Vpp is supplied externally.</td></tr>
<tr><td>3</td><td>C1P</td></tr>
<tr><td>4</td><td>C2P</td><td rowspan="2">Connect to charge pump capacitor.
These pins are not used and should be disconnedted when Vpp is supplied externally.</td></tr>
<tr><td>5</td><td>C2N</td></tr>
<tr><td>6</td><td>VDD2</td><td>3.0 – 4.2V power supply pad for Power supply for charge pump circuit.
This pin can be disconnected or connect to VDD1 when VPP is supplied externally</td></tr>
<tr><td>7</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>9</td><td>VDD1</td><td>Power supply input: 1.65 - 3.5V</td></tr>
<tr><td>10</td><td>IM0</td><td rowspan="3">These are the MPU interface mode select pads.
<table>
<tr><td></td><td>8080</td><td>I2C</td><td>6800</td><td>4-wire SPI</td><td>3-wire SPI</td></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>11</td><td>IM1</td></tr>
<tr><td>12</td><td>IM2</td></tr>
<tr><td>13</td><td>CSB</td><td>This pad is the chip select input. When CSB= “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>14</td><td>RESB</td><td>This is a reset signal input pad. When RESB is set to “L”, the settings are initialized. The reset operation is performed by the RESB signal level.</td></tr>
<tr><td>15</td><td>A0</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I2C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>16</td><td>WRB</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU WRB signal. The signals on the data bus are latched at the rising edge of the WRB signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When WRB = “H”: Read.
When WRB= “L”: Write.</td></tr>
<tr><td>17</td><td>RDB</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the RDB signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU , this is active HIGH. This is used as an enable clock
input of the 6800 series MPU.
When RDB= “H”: Enable.
When RDB = “L”: Disable.</td></tr>
</table>

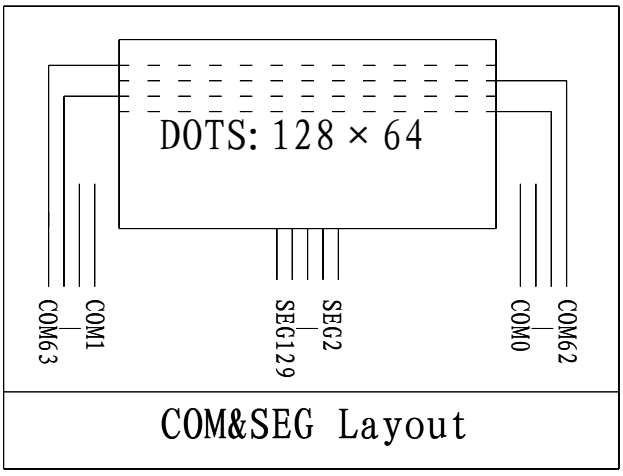
18~25	D0~D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the I2C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDAI). At this time, D2 to D7 are set to high impedance.
26	IREF	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10μA.
27	VCOMH	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.
28	VPP	OLED panel power supply. Generated by internal charge pump. Connect to capacitor. It could be supplied externally.
29	VLSS	Ground.
30	NC(GND)	No Connection.

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
DC Supply Voltage	VDD1	-0.3	+3.6	V	IC maximum rating
	VDD2	-0.3	+4.3	V	IC maximum rating
OLED Operating voltage	VPP	-0.3	+13.5	V	IC maximum rating
Operating Temp.	Top	-40	+70	℃	-
Storage Temp	Tstg	-40	+85	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD1	22±3°C, 55±15%R.H	1.65	3.0	3.5	V
	VDD2	22±3°C, 55±15%R.H	2.4	3.7	4.2	V
OLED Driver Supply Voltage	VPP	22±3°C, 55±15%R.H	11.5	12	12.5	V
High-level Input Voltage	V_{IH}	-	0.8×VDD1	-	VDD1	V
Low-level Input Voltage	V_{IL}	-	VSS	-	0.2×VDD1	V
High-level Output Voltage	V_{OH}	-	0.8×VDD1	-	VDD1	V
Low-level Output Voltage	V_{OL}	-	VSS	-	0.2×VDD1	V

Note : The VPP input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1) VPP = 12V (External)	90	120	-	cd/m^2
		All pixels ON(1) (VPP generated by internal DC/DC)	60	80	-	
Sleep mode current Consumption in VDD1&VDD2	ISP	During sleep,TA=+25℃ VDD1=3V,VDD2=3V(2)	-	-	5	uA
Sleep mode current Consumption in VPP		During sleep,TA=+25℃ VPP=9V(2)	-	-	5	uA
Normal Mode Power Consumption	Pt	All pixels ON(1) VPP = 12V (External)	-	TBD	TBD	mW
		All pixels ON(1) (VPP generated by internal DC/DC)	-	TBD	TBD	mW
C.I.E(White)	(x)	x,y(CIE1931)	TBD	0.30	TBD	-
	(y)		TBD	0.33	TBD	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1):

Normal Mode test conditions are as follows:

- Driving voltage : 12V
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/64
- Driving voltage : VDD2:3.7V(VPP Generated by Internal DC/DC).
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/64

Note(2):

Sleep Mode test conditions are as follows:
- Disable Charge Pump:0XAD,0X8A.
- Set \Display OFF:0XAE

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system,and can reduce current consumption nearly to a static current value if no access is made from the microprocessor.The internal status in the sleep mode is as follows:
-Stops the oscillator circuit and DC-DC circuit.
-Stops the OLED drive and outputs HZ as the segment/common driver output.
-Holds the display data and operation mode provided before the start of the sleep mode.
-The MPU can access to the huilt-in display RAM.

8.3 AC Electrical Characteristics

(1) 8080-Series MPU Parallel Interface Timing Characteristics

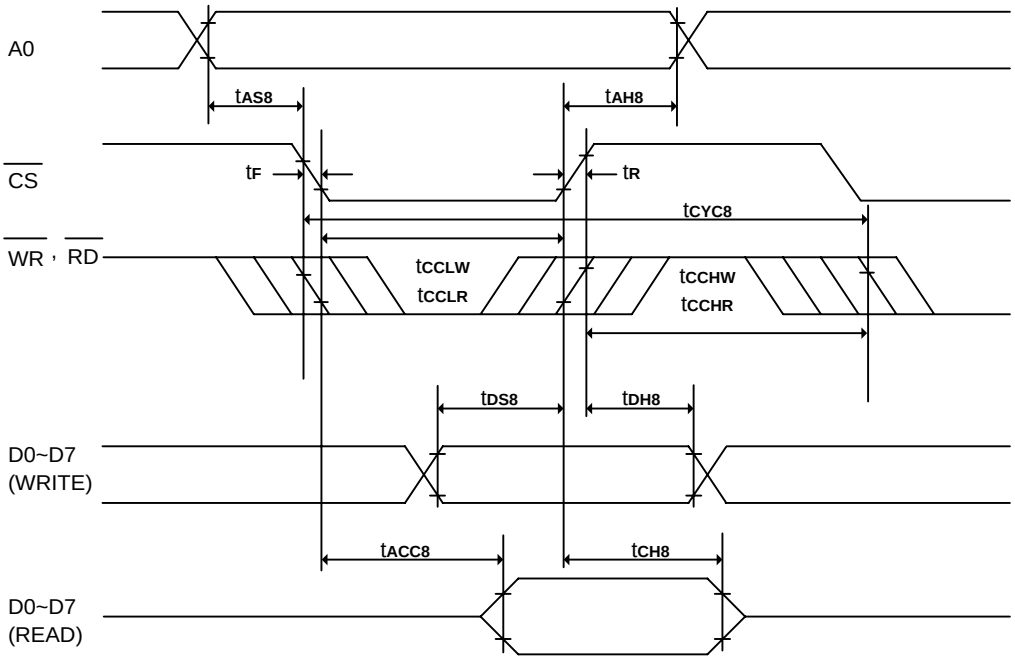
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	600	-	-	ns	
tas8	Address setup time	0	-	-	ns	
tah8	Address hold time	0	-	-	ns	
tds8	Data setup time	80	-	-	ns	
tdh8	Data hold time	30	-	-	ns	
tch8	Output disable time	20	-	140	ns	CL = 100pF
tacc8	$\overline{RD}$ access time	-	-	280	ns	CL = 100pF
tcclw	Control L pulse width (WR)	200	-	-	ns	
tcclr	Control L pulse width (RD)	240	-	-	ns	
tcchw	Control H pulse width (WR)	200	-	-	ns	
tcchr	Control H pulse width (RD)	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	300	-	-	ns	
tas8	Address setup time	0	-	-	ns	
tah8	Address hold time	0	-	-	ns	
tds8	Data setup time	40	-	-	ns	
tdh8	Data hold time	15	-	-	ns	
tch8	Output disable time	10	-	70	ns	CL = 100pF
tacc8	$\overline{RD}$ access time	-	-	140	ns	CL = 100pF
tcclw	Control L pulse width (WR)	100	-	-	ns	
tcclr	Control L pulse width (RD)	120	-	-	ns	
tcchw	Control H pulse width (WR)	100	-	-	ns	
tcchr	Control H pulse width (RD)	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

8080-series parallel interface characteristics



(2)6800-Series MPU Parallel Interface Timing Characteristics

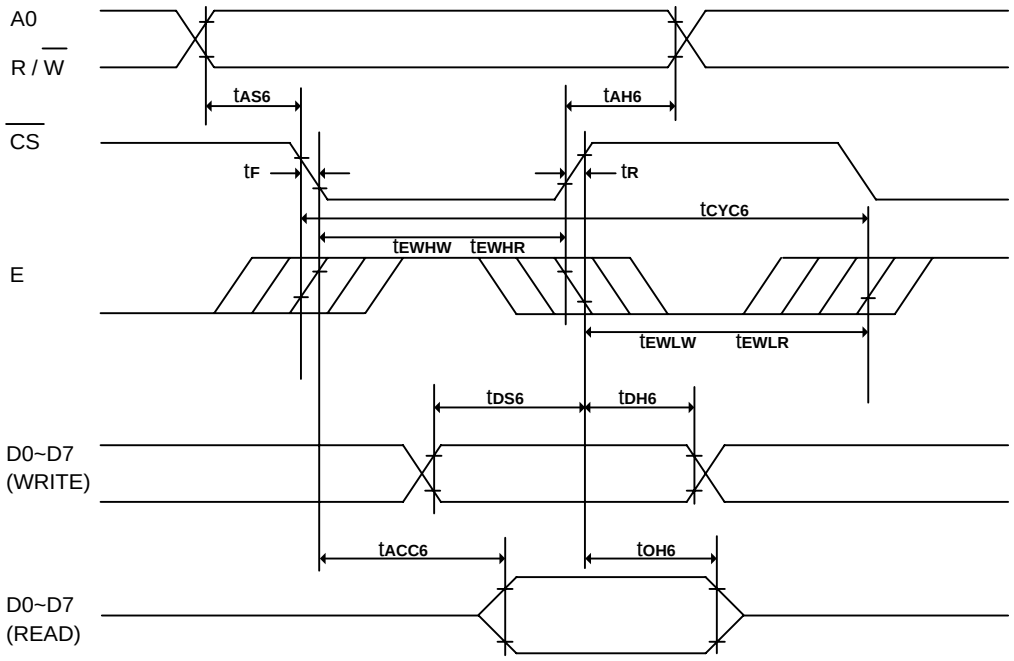
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC6	System cycle time	600	-	-	ns	
tAS6	Address setup time	0	-	-	ns	
tAH6	Address hold time	0	-	-	ns	
tDS6	Data setup time	80	-	-	ns	
tDH6	Data hold time	30	-	-	ns	
tOH6	Output disable time	20	-	140	ns	CL = 100pF
tACC6	Access time	-	-	280	ns	CL = 100pF
tEWHW	Enable H pulse width (Write)	200	-	-	ns	
tEWHR	Enable H pulse width (Read)	240	-	-	ns	
tEWLW	Enable L pulse width (Write)	200	-	-	ns	
tEWLR	Enable L pulse width (Read)	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC6	System cycle time	300	-	-	ns	
tAS6	Address setup time	0	-	-	ns	
tAH6	Address hold time	0	-	-	ns	
tDS6	Data setup time	40	-	-	ns	
tDH6	Data hold time	15	-	-	ns	
tOH6	Output disable time	10	-	70	ns	CL = 100pF
tACC6	Access time	-	-	140	ns	CL = 100pF
tEWHW	Enable H pulse width (Write)	100	-	-	ns	
tEWHR	Enable H pulse width (Read)	120	-	-	ns	
tEWLW	Enable L pulse width (Write)	100	-	-	ns	
tEWLR	Enable L pulse width (Read)	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

6800-series parallel interface characteristics



(3)Serial Interface Timing Characteristics(For 4 wire SPI)

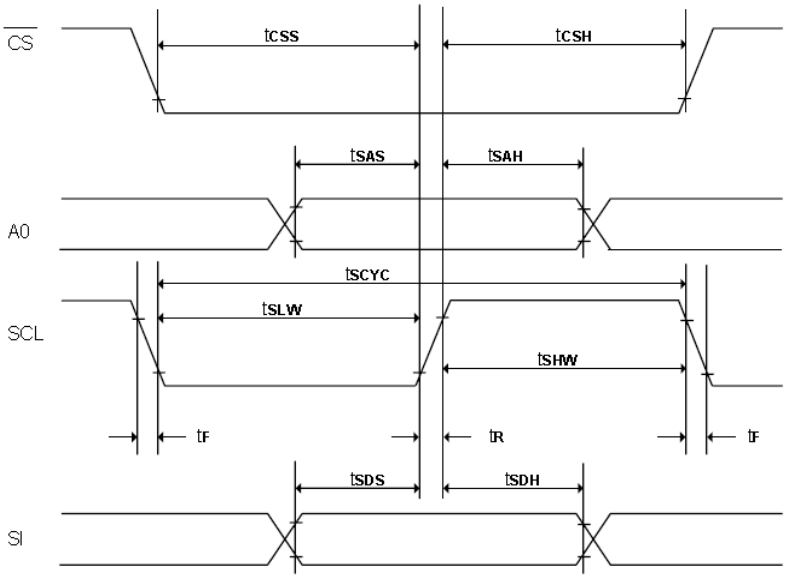
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

Serial Interface characteristics



(4)Serial Interface Timing Characteristics(For 3 wire SPI)

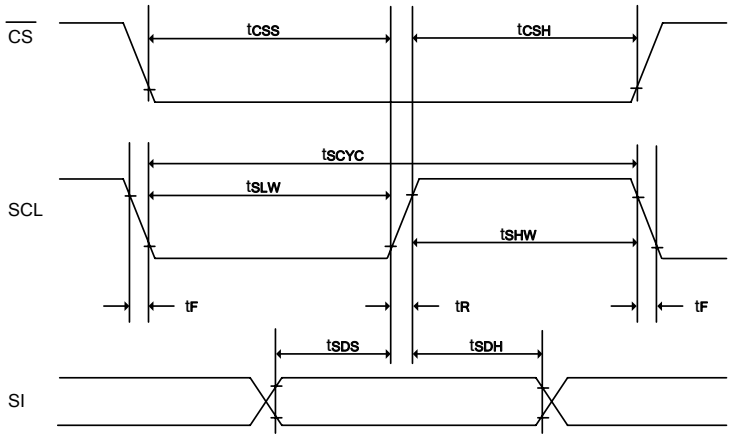
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse	100	-	-	ns	
t_{SLW}	Serial clock L pulse	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

Serial Interface characteristics

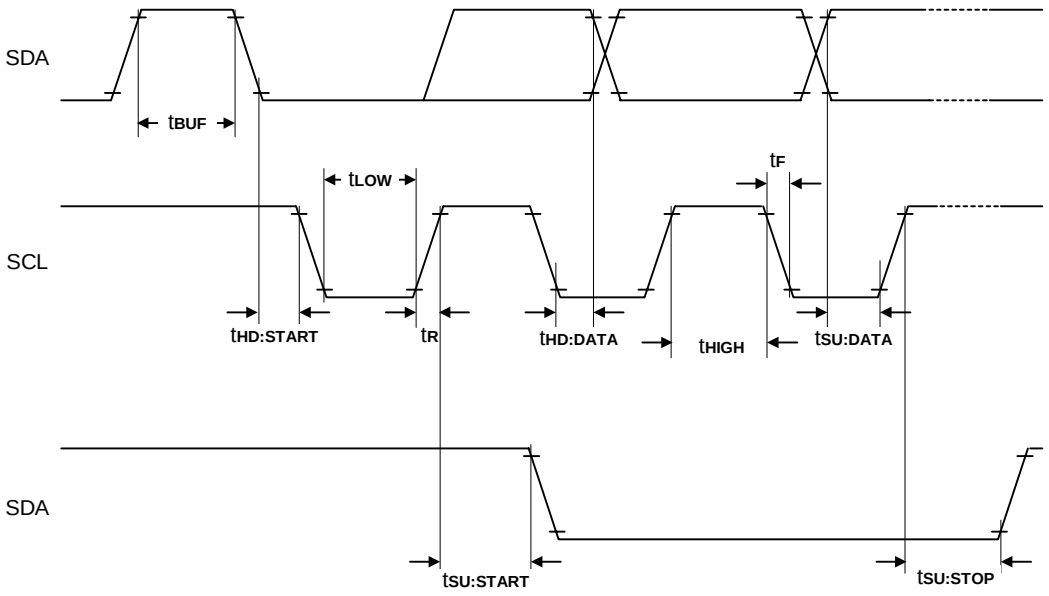


(5)I² C Interface Timing Characteristics

(VDD1 = 1.65V to 3.5V, TA = 25°C)

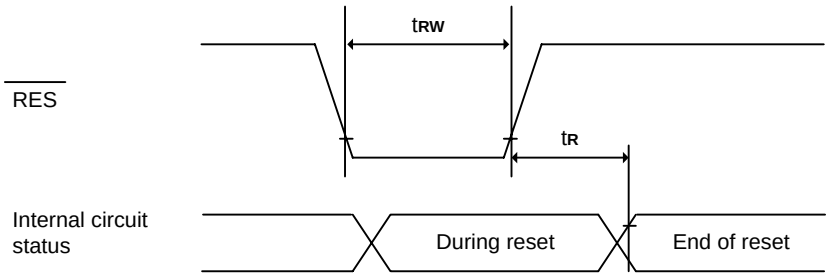
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	uS	
THigh	SCL clock H pulse width	0.6	-	-	uS	
TSU:data	data setup time	100	-	-	nS	
THD:data	data hold time	0	-	0.9	uS	
Tr	SCL，SDA rise time	20+0.1Cb	-	300	nS	
Tf	SCL，SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
TSu:sTArt	Setup timefor re-START	0.6	-	-	uS	
THD:start	START Hold time	0.6	-	-	uS	
Tsu:stop	Setup time for STOP	0.6	-	-	uS	
TBUF	Bus free times between STOP and START condition	1.3	-	-	uS	

Serial Interface characteristics



9 Functional Specification and Application Circuit

9.1 Reset Timing



(VDD1 = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	

(VDD1 = 2.4 - 3.5V, T_A = +25°C)

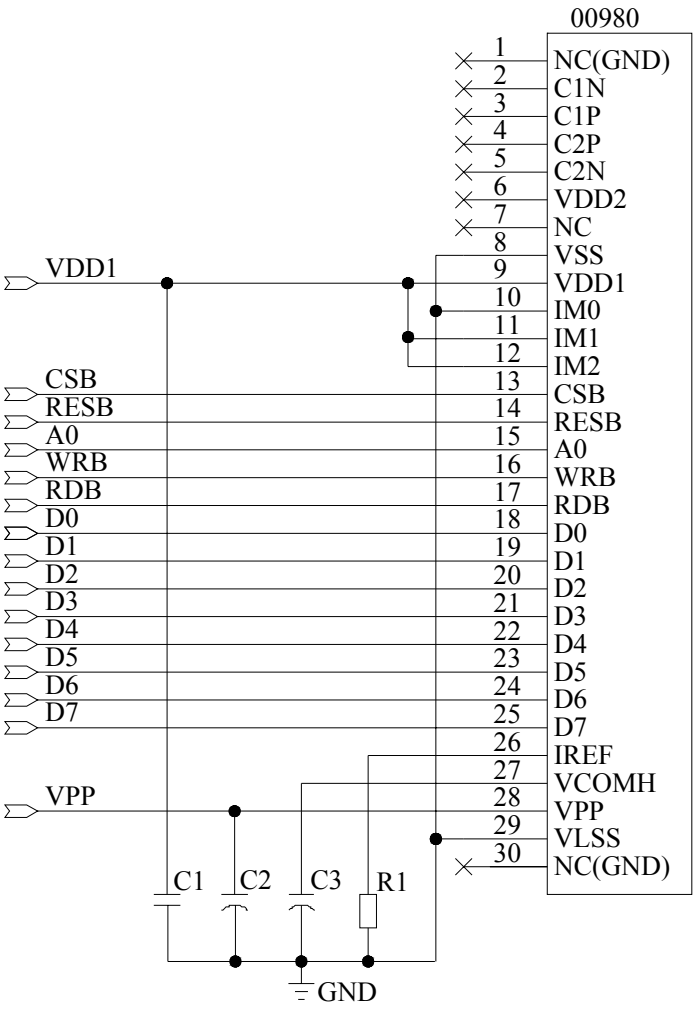
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	5.0	-	-	μs	

9.2 Application Circuit

9.2.1 Under external VPP Mode,the charge Pump Setting (ADh) must be set as follow:

ADh:DC-DC Control Mode Set 8Ah:DC-DC is disable

(1).The configuration for 8080-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[7:0], RDB, WRB, A0, RESB,CSB

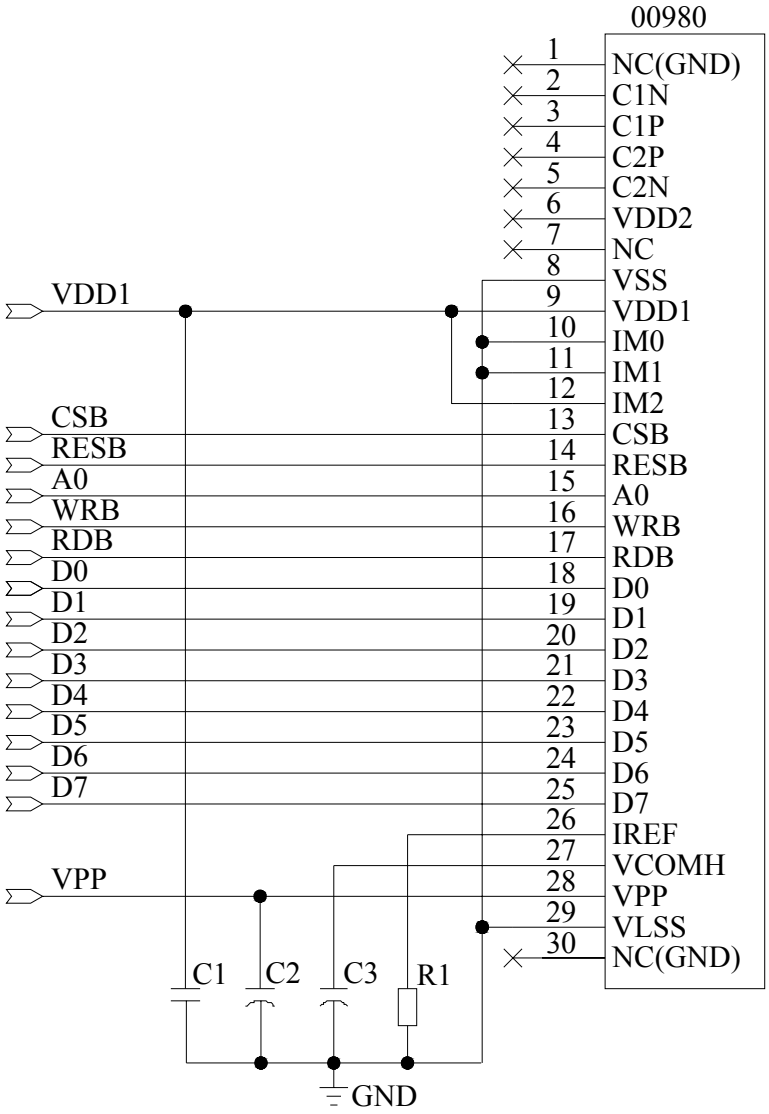
Recommended components

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 760Kohm.ROHS

(2).The configuration for 6800-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[7:0], RDB, WRB, A0, RESB,CSB

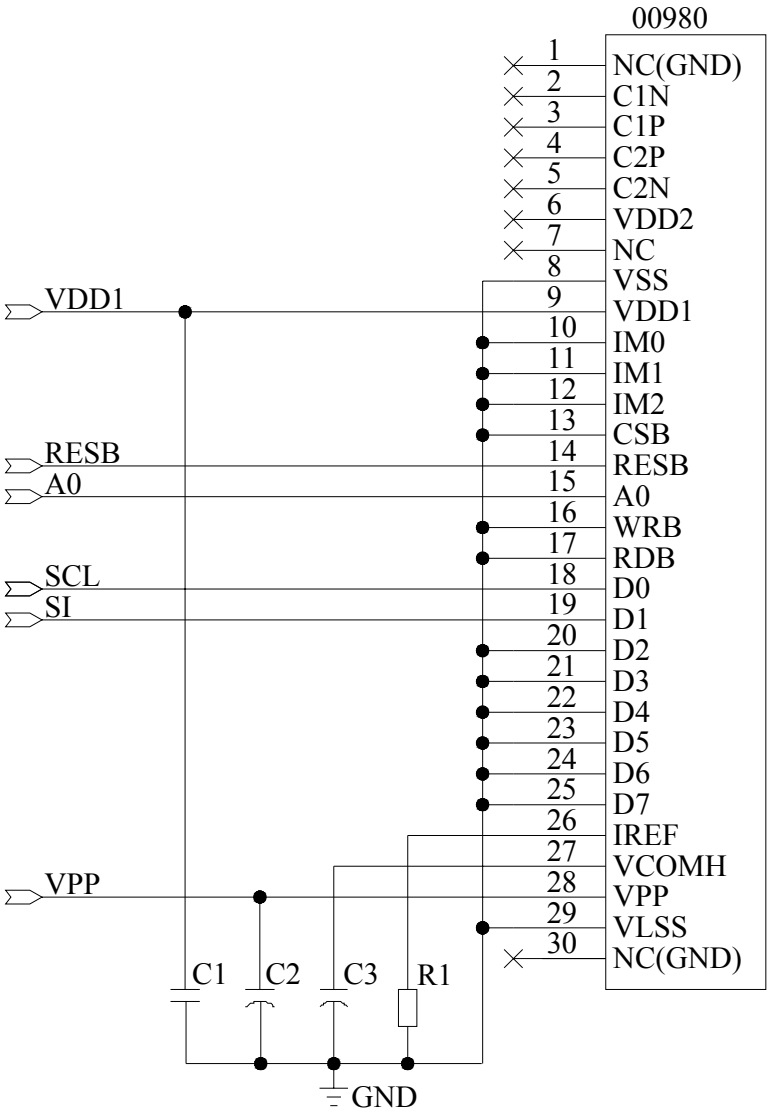
Recommended components

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 760Kohm.ROHS

(3).The configuration for 4-wire SPI interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SI,A0, RESB

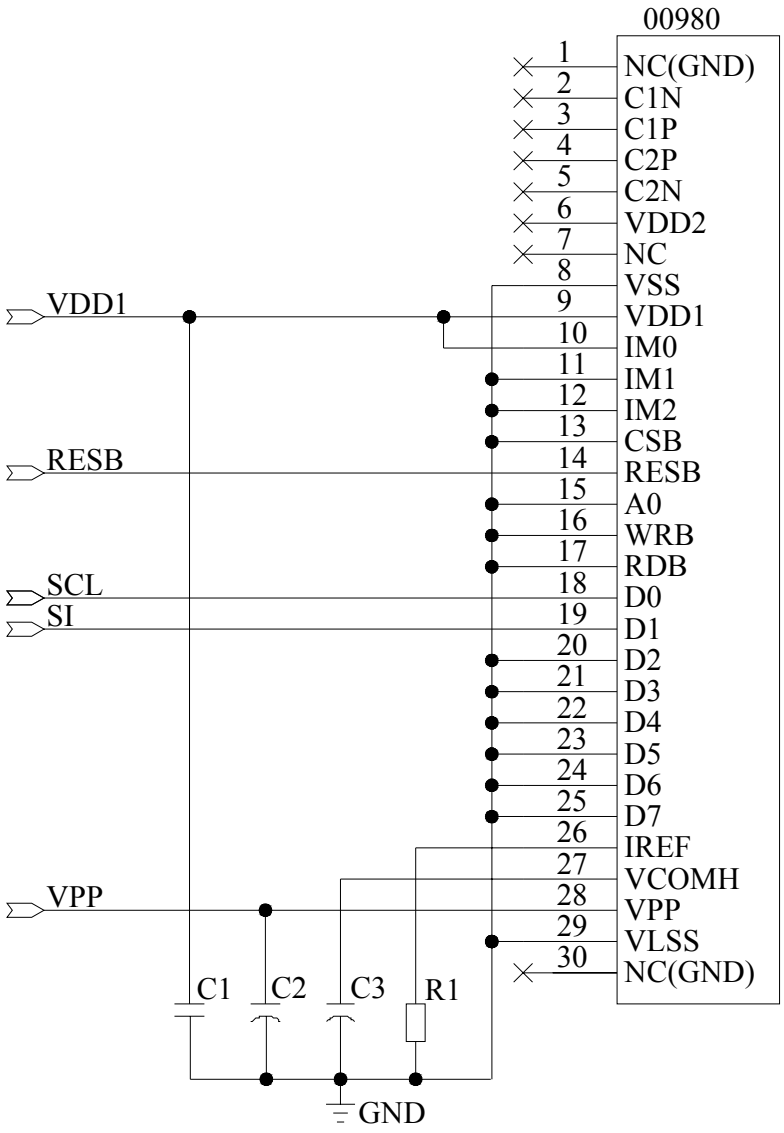
Recommended components

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 760Kohm.ROHS

(4).The configuration for 3-wire SPI interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SI,RESB

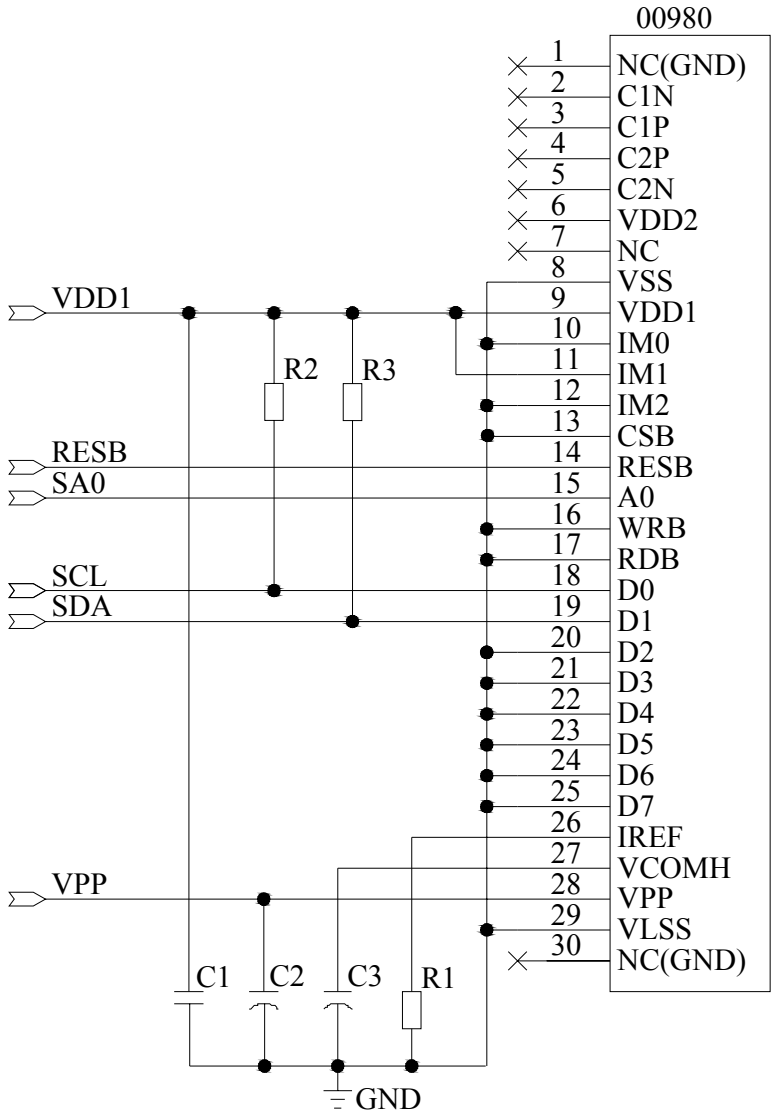
Recommended components

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 760Kohm.ROHS

(5).The configuration for I² C interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SDA,SA0, RES

Recommended components

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1: 0.1uF-0603-X7R±10%.ROHS

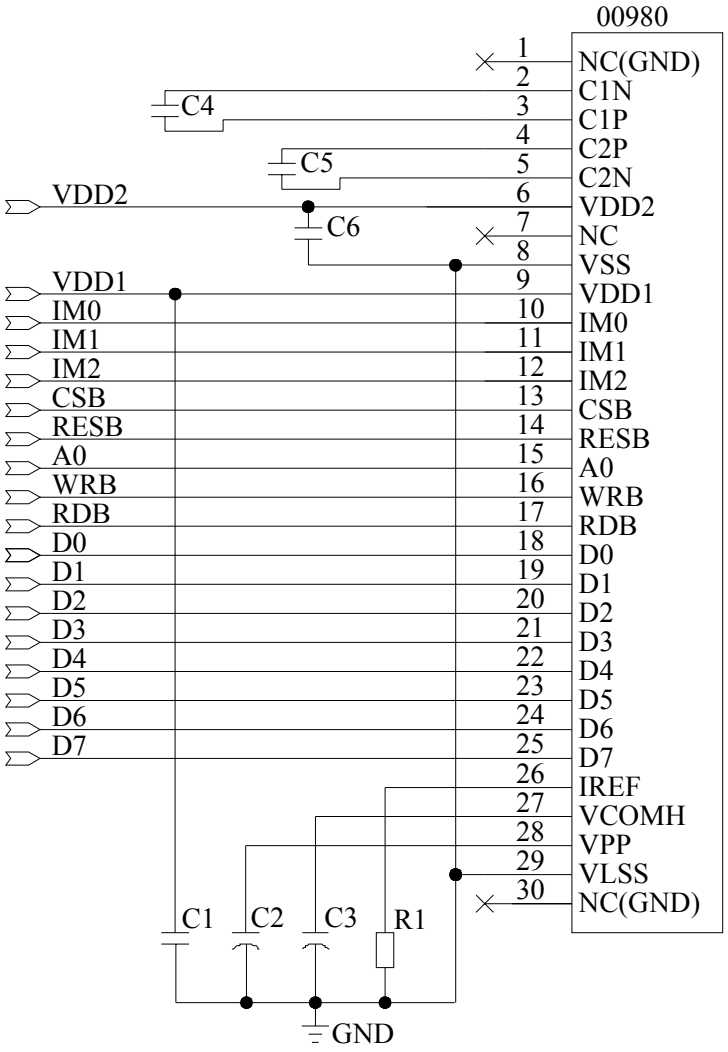
R1: 0603 1/10W +/-5% 760Kohm.ROHS

R2,R3: 0603 1/10W +/-5% 10Kohm.ROHS

9.2.2 Under Internal DC/DC Mode,the charge Pump Setting (ADh) must be set as follow:

ADh: DC-DC Control Mode Set 8Bh:DC-DC is will be turned on when display on

The configuration for VPP Generated by Internal DC/DC Circuit is shown in the following diagram:



Pin connected to MCU interface: D[7:0], RDB, WRB, A0, RESB,CSB,IM0,IM1,IM2

Recommended components

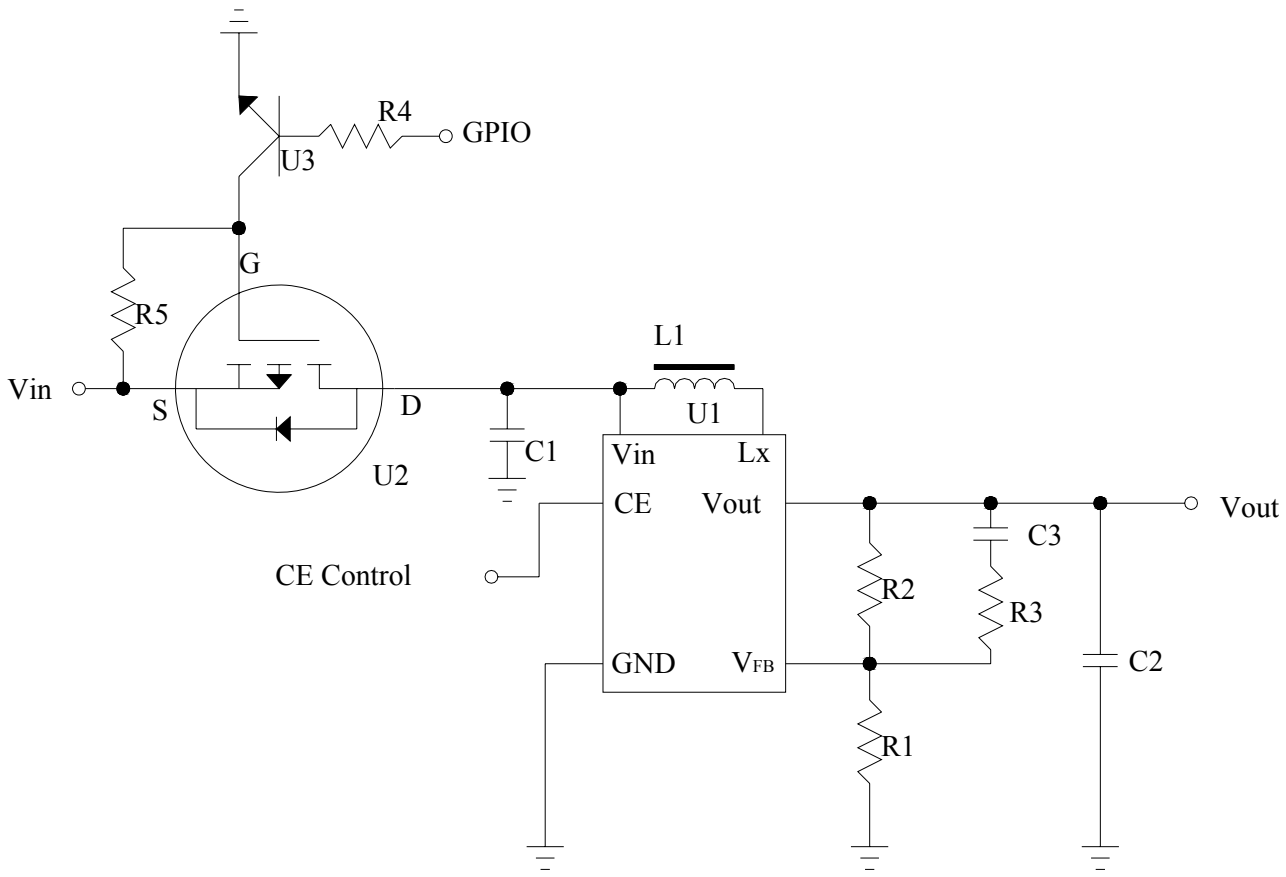
C1: 0.1uF-0603-X7R±10%.ROHS

C2,C3,C6: 4.7μF/25V.ROHS (Tantalum Capacitors)

C4,C5: 1μF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 390Kohm.ROHS

9.3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-1% 10Kohm.ROHS
The R2	: 0603 1/10W +/-1% 110Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338P
The U3	: 8050

9.4 Display Control Instruction

Refer to SH1106G IC Specification.

9.5 Recommended Software Initialization

TBD

10 Package Specification

TBD

11 Reliability

11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	85℃,240hrs	4
2	Low Temperature (Non-operation)	-40℃,240hrs	4
3	High Temperature (Operation)	70℃,240hrs	4
4	Low Temperature (Operation)	-40℃,240hrs	4
5	High Temperature / High Humidity (Operation)	60℃,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40℃~85℃(-40℃/30min;transit/3min;85℃/30min;transit/3min) 1cycle: 66min,30cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
2. The degradation of polarizer is ignored for item 5.
3. The tolerance of temperature is ±3℃, and the tolerance of relative humidity is ±5%.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance:≥50% of initial value.
4. Current consumption: within ± 50% of initial value.

11.2 Lifetime

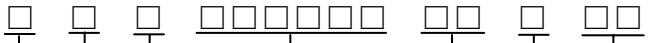
End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	13,000	-	hrs	120 cd/m^2, 50% alternating checkerboard, 22±3°C, 55±15% RH

11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.

12 Illustration of OLED Product Name



Flow No. :

01~99

Display Color :

R—red

G—green

B—blue

Y—yellow

W—white

A—area color

F—full color

Panel Flow No. :

A0~A9, B0~B9…Z0~Z9

Display Format :

Graphic—columns and rows

Character—characters and line number

Segment—segment number

Icon—pixel number

Product Type :

P—panel

M—module

Display Type :

G—graphic

C—character

S—segment

I—Icon

M—mixed

Company :

V—Visionox

13 Outgoing Quality Control Specifications

13.1 Sampling Method

(1) GB/T 2828.1-2003/ISO2859-1：1999, inspection level Ⅱ, normal inspection, single sample inspection

(2) AQL: Major 0.65; Minor 1.0

13.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C

Humidity: 55±15%R.H

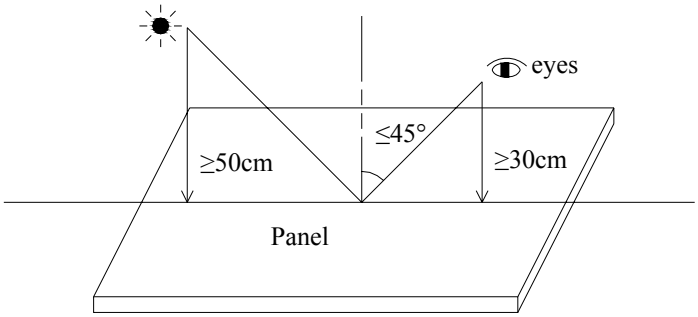
Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

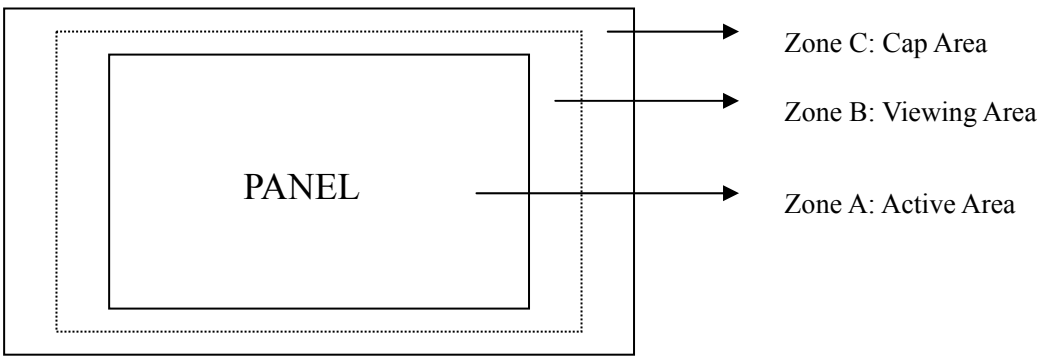
Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)

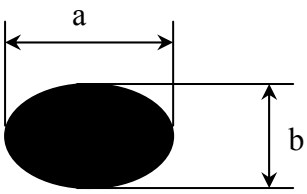


13.3 Quality Assurance Zones

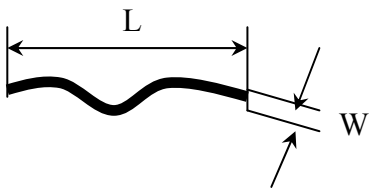


13.4 Inspection Standard

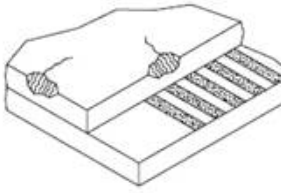
Definition of Φ&L&W (Unit: mm)

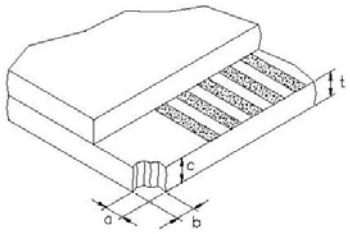
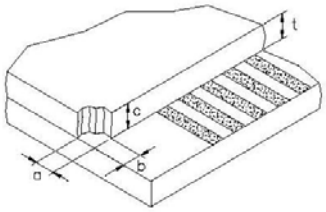
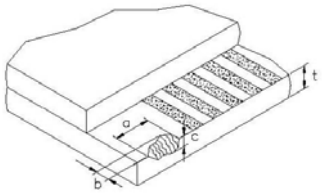
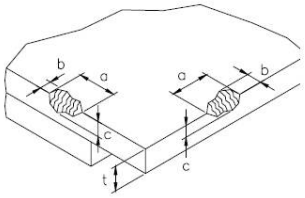
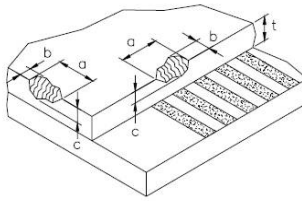


Φ=(a+b)/2



Ⅰ. Appearance Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.15</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.30</td><td>3</td></tr>
<tr><td>Φ>0.30</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>Scratch/line on the glass/Polarizer</td><td>
<table>
<tr><td rowspan="2">Width (mm)</td><td rowspan="2">Length (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>W≤0.03</td><td>---</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.08</td><td>L≤5.0</td><td>3</td></tr>
<tr><td>W>0.08</td><td>---</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ>0.5</td><td>0</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<Φ≤0.5</td><td>3</td></tr>
<tr><td>Φ≤0.2</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>4</td><td>Any Dirt & Scratch on Polarizer’s Protective Film</td><td>Ignore for not affect the polarizer.</td><td>Acceptable</td></tr>
<tr><td>5</td><td>Glass Crack</td><td>  Propagation crack is not acceptable.</td><td>Major</td></tr>
</table>

6	Corner Chip	 t= Glass thickness Accept a≤2.0mm or b≤2.0mm, c≤t	Minor
7	Corner Chip on Cap Glass	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
8	Chip on Contact Pad	 t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)	Minor
9	Chip on Face of Display	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
10	Chip on Cap Glass	 t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t	Minor
11	Stain on Surface	Stain removable by soft cloth or air blow is acceptable.	Minor
12	TCP/FPC Damage	(1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.	Minor
13	Dimension Unconformity	Checking by mechanical drawing.	Major

Ⅱ. Displaying Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Black/White spot
Dirty spot
Foreign matter</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Pieces Permitted</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.10</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td>3</td></tr>
<tr><td>Φ>0.20</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>No Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>3</td><td>Irregular Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>4</td><td>Missing Line
(row or column)</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>5</td><td>Short</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>6</td><td>Flicker</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>7</td><td>Abnormal Color</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>8</td><td>Luminance NG</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>9</td><td>Over Current</td><td>Refer to the SPEC.</td><td>Major</td></tr>
</table>

14 Precautions for operation and Storage

14.1 Precautions for Operation

(1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).

(2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.

(3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.

(4) Do not attempt to disassemble or process the OLED module.

(5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.

(6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

(7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.

(8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

14.2 Soldering

(1) Soldering should be performed only on the I/O terminals.

(2) Use soldering irons with proper grounding and no leakage.

(3) Iron: no higher than 300℃ and 3~4 sec during soldering.

14.3 Precautions for Storage

(1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.

(2) Keep the environment temperature between 10℃ and 35℃ and the relative humidity less than 60%. Avoid high temperature and high humidity.

(3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.

(4) Do not leave any article on the OLED module surface for an extended period of time.

14.4 Warranty period

Visionox Display Co., Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition.