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Digital Circuits

Review of Digital Circuits
Digital Circuits Lab
HW
Quiz

A digital system is one in which the electronic information is encoded in a discrete number of states (typically two: high and low). Compare this to an analog signal that is made of a continuously variable voltage signal level. Conversion between analog and digital (A to D) and back (D to A) is often used to couple analog systems (the environment, sensors) with computational systems (MCU, IC's). Information on an analog system can be easily represented as a voltage level. Information in a digital system needs to be represented with an appropriate number system.

Number systems:
Information on a digital system is represented using a combination of on/off or high/low signals; binary signals. Using this binary representation, numbers can be created using the base 2 number system. Here, a number is represented as:

$$N = b_n*2^n + \ldots + b_2*2^2 + b_1*2^1 + b_0*2^0.$$

For example, the number 7 can be represented as:

$$7 = 0*2^4 + 1*2^2 + 1*2^1 + 1*2^0 = 0111_{binary}$$

The left-most bit in a binary number is called the most significant digit, while the right-most is called the least significant. The most significant bit (MSB) carries the largest numerical value; the least significant bit (LSB) carries the smallest.

Each digit in a binary number is stored in a bit. A set of bits grouped together to form a number is called a byte. This can be thought of as a word and becomes the basic unit for passing information in a digital system. Typical byte or word sizes are 8-bit, 16 bit, 32 bit, etc. Sometimes they are grouped in sets of 4 and this set may be called a nibble. (Who comes up with these names?). There are two nibbles in an 8-bit number. Note that exponentially larger numbers can be passed with larger byte size binary representations. For example, an 8-bit number can at most represent 256 distinct values. However, a 16-bit number can represent 65536 distinct values, and so on. To get this number, simply create a number of all ones and determine its decimal value, or remember that 256 = 2^8, 65536=2^{18}, etc. (Note that in an 8-bit number, the MSB multiplier is 2^7. However, an 8-bit number's maximum value is 2^8. The remaining value comes from the sum of all values below the most significant digit plus one. Add the one to include representation of zero)

Binary arithmetic is similar to base 10 arithmetic, with some additional rules included to handle subtraction and negative numbers.

<u>Negative numbers in binary:</u>
Negative numbers in binary are represented with a 1 in the MSB. Note however that it is up to the program designer to specify whether negative numbers will be used. In order to determine whether a specific command is intended for a binary system using

Binary
hex ←
decimal.
4 bit → 1 digit dec.
4 bit → 1 bit hex

Binary coded Decimal
BCD

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negative numbers, look for clue words like "negative" or "two's complement." Using negative numbers reduces the available positive value resolution by half with at times little additional gain. Arithmetic to handle negative numbers is called two's-complement. Note: In the decimal system, every number below zero is considered negative. In binary number systems, every number above the mid-byte value is considered negative.

Another common number system that we will see in using the MCU is the hexadecimal system, a base 16 number system. Digits in base 16 go from 0 to F. Machine language (for example, our .s19 files) is expressed in hexadecimal. The table below lists conversions between decimal, binary and hexadecimal systems.

Comparing number systems		
Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	10000	10
17	10001	11

Practice: Binary numbers

Digital Logic:

With digital systems, we can design circuits to do many things including the following:

- Count events
- Time events
- Trigger events
- Perform logic
- Anything you can dream-up

Using the very basic binary (on/off) number system and relatively simple logic operations discussed below, we can derive a sophisticated computer system.

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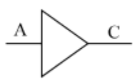
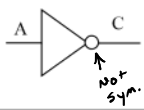
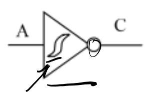
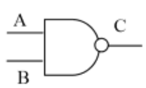
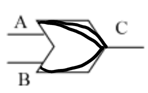
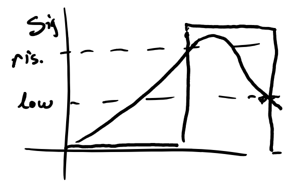
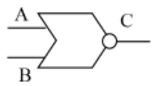
Combinatory logic

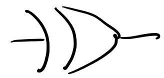
Not

Combinatory logic provides a rule set in which binary inputs are combined and produce an output based on a set of standard logic operations: AND, OR, NAND, NOR and XOR. Any of these logic operations can be handily incorporated into your design circuit using readily available IC's (integrated circuits) called gates. The table below presents theses logic operations, their symbol, truth table and typical gate.

Gate	Symbol	Operation	Truth table	Typical IC	Software
Buffer		Clean-up signal, improve impedance matching	A C 0 0 1 1	7400	C = a
Inverter	 Not sym.	Inverts signal, improves impedance	A C 0 1 1 0	7400	C ~= a
Schmitt trigger		Buffer to clean-up signal. Contains hysteresis: on a rising edge, it flips at 3 V, falling about 1.5 V	A C 0 1 1 0	7400	if statements.
AND		Output is the AND of the inputs	A B C 0 0 0 1 0 0 0 1 0 1 1 1	7400	&
NAND		Inverts the output of the AND	A B C 0 0 1 1 0 1 0 1 ~~0~~1 1 1 ~~1~~0	7400	~&
OR		Output is the OR of the inputs	A B C 0 0 0 1 0 1 0 1 1 1 1 1	7400	|



NOR		Inverts the signal of the OR	A B C 0 0 1 1 0 0 0 1 0 1 1 0	7400



XOR

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0

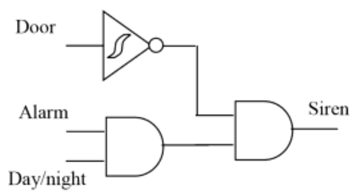
These gates in IC form are created as combinations of transistors, with the internal design available in spec sheets and electronics texts. The IC's listed above come in quad, hex, etc. form, containing four, six, etc. gates on each chip.

Example: Consider a security circuit system that should be designed to trigger based on the following logic:

> If the system is armed, and if it is dark outside (nighttime), and if the door is opened, then sound an alarm.

A truth table and symbolic circuit to complete this simple task could look like this:
A=Alarm on (1) or off (0), B=light sensor light (1) or dark (0) and C= door sensor open (0) closed (1).

A (on/off)	B (light)	C (door)	D (alarm)
0	0/1	0/1	0
1	0	0	0
1	1	1	0
1	1	0	1



This unit provides the logic component of our simple circuit. In mechatronics, we need to complete all parts of this circuit, including choosing appropriate sensors, interfacing these sensors with our logic system, and then interfacing the output to appropriate actuators. In general, sensors are low power output devices, and require high impedance interface. Similarly, output devices such as actuators require a significant level of power and thus amplifier units in the interface. Logic signals are low power (typically 1-15 mA).

7400 Series IC:
http://en.wikipedia.org/wiki/7400_series

The 7400 series ICs are the family of TTL (and follow-on CMOS) circuits commonly used in electronics applications, and contain a large variety of logic gates, flip-flops, counters and many other devices. The following two tables summarize a few of the available products in the 7400 series and the naming convention:

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Part number	Description	Datasheet
7400	quad 2-input NAND gate	HC/HCT
741G00	single 2-input NAND gate	
7401	quad 2-input NAND gate with open collector outputs	
741G01	single 2-input NAND gate with open drain output	
7402	quad 2-input NOR gate	HC/HCT
741G02	single 2-input NOR gate	
7403	quad 2-input NAND gate with open collector outputs	HC/HCT
741G03	single 2-input NAND gate with open drain output	
7404	hex inverter	HC/HCT
741G04	single inverter	
7405	hex inverter with open collector outputs	HC
741G05	single inverter with open drain output	
7406	hex inverter buffer/driver with 30 V open collector outputs	
741G06	single inverting buffer/driver with open drain output	
7407	hex buffer/driver with 30 V open collector outputs	
741G07	single non-inverting buffer/driver with open drain output	
7408	quad 2-input AND gate	HC/HCT
741G08	single 2-input AND gate	
7409	quad 2-input AND gate with open collector outputs	
741G09	single 2-input AND gate with open drain output	
7410	triple 3-input NAND gate	HC/HCT
7411	triple 3-input AND gate	HC/HCT
7412	triple 3-input NAND gate with open collector outputs	
7413	dual Schmitt trigger 4-input NAND gate	
7414	hex Schmitt trigger inverter	HC/HCT
741G14	single Schmitt trigger inverter	
7415	triple 3-input AND gate with open collector outputs	
7416	hex inverter buffer/driver with 15 V open collector outputs	
7417	hex buffer/driver with 15 V open collector outputs	
741G17	single Schmitt-trigger buffer	
7418	dual 4-input NAND gate with Schmitt trigger inputs	
7419	hex Schmitt trigger inverter	
7420	dual 4-input NAND gate	HC/HCT
7421	dual 4-input AND gate	HC
7422	dual 4-input NAND gate with open collector outputs	

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Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate @1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic	500	4	10	3.3	1963	the first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.
DTL	Diode–transistor logic	25		10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)		1.65 - 3.6	2004	First GHz 7400 series logic
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8		31	-5.2	1962	first integrated logic circuit commercially produced
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	

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There are two basic technologies used to produce typical IC's: TTL and CMOS:

TTL: Transistor-transistor-logic devices are designed to run at voltages between 0 and 5 V. A TTL gate generally defines a low as a voltage less than 0.7 V, and a high as a voltage greater than 2 V. TTL devices are generally stable, rugged, not very static sensitive and use more power than CMOS devices. They come in a number of varieties, for example L are reduced power consumption (low power) versions.

CMOS: Complementary metal oxide semiconductor devices perform the same functions but over a much wider voltage range (ex. 0 to 15V) with the logic switch levels depending on the supply voltage. Their advantage is that they consume very little power. However, they are less rugged and susceptible to static electricity. These are the chips you should not touch with your hands until you remove all static electricity.

CMOS and TTL devices can be used together in the same circuit, but the voltage levels must be within the TTL range.

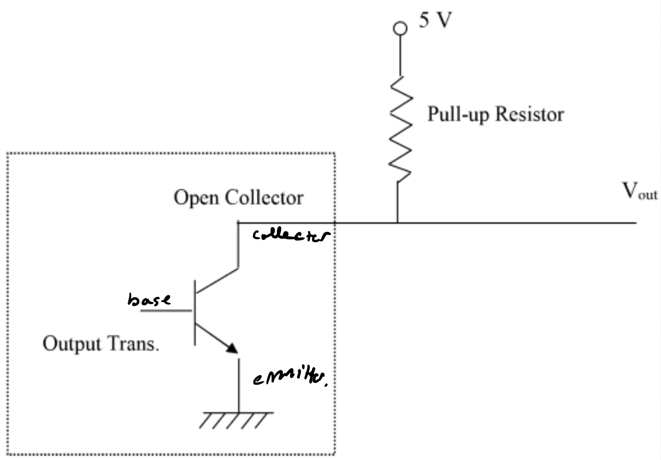
The labeling system for TTL devices follows the convention:

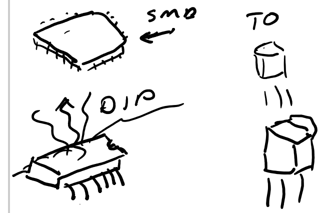
AAxxyzz

With AA the manufacturer's symbol, xx 54 for military, 74 for commercial quality, y the type of internal design (none = standard TTL, L = low power, LS = low power schottky) and finally zz is specifies the device type (example: 00 = QUAD NAND, 01 = ___)

Open Collector Outputs:

Certain IC's are open collector output devices; devices that terminate with the collector of a transistor. Such outputs require a small circuit to complete the transistor circuit. This circuit consists of a properly chosen pull-up resistor. Examples of open collector output devices include the Polaroid ultrasonic rangers and the 7401, 7403, 7405, 7406 TTL devices.





typ. 16.

20mA

200 mA +

5 A.

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Sequential Logic:

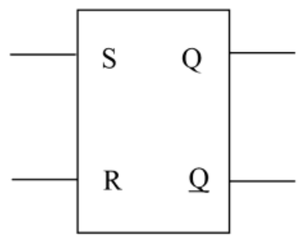
Sequential logic devices perform their operations based on specific timing or sequence of events. These occur in systems such as clocked systems and event counting. Events or triggers can include rising or falling edges of a digital signal. Often, a sequential logic system will perform the logic operation based on a clock or other triggered event, and in the meantime stay in a holding pattern. A number of devices that use this kind of logic including various flip-flops, counters and timers.

Flip-flop

A flip-flop forms the basic memory storage device in digital systems. The most basic form of flip flop is the RS flip-flop (Set and reset). The output of the flip-flop is set high when S = 1, and is reset to low when R = 1. In the meantime, the output of the flip-flop is constant. This flip-flop is shown in the following figure and truth table.

Truth Table for RS flip-flop

Inputs		Outputs	
S	**R**	**Q**	**$\overline{Q}$**
0	0	Q_0	$\overline{Q_0}$
1 ~~0~~	0	1	0
0	1	0	1
1	1	NA	NA



RS flip-flop rules:

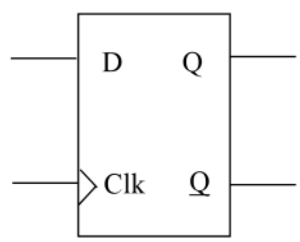
1. When S = 1 and R = 0, the flip-flop is set such that Q = 1 and $\overline{Q}$ = 0.
2. When S = 0 and R = 1, the flip-flop is reset such that Q = 0 and $\overline{Q}$ = 1.
3. When both S = 0 and R = 0, the flip-flop is unchanged.
4. The state S = 1 and R = 1 is not allowed and the output is not determined.

An RS flip-flop is formed of two inverters and two NAND gates combined with feedback.

Clocks can be added to flip-flops such that the flip-flop state is determined at specific clock (for example rising edge) cycles.

D Flip-flops

A D flip-flop is a clocked flip-flop whose output, Q is the same value as D at each rising clock cycle.



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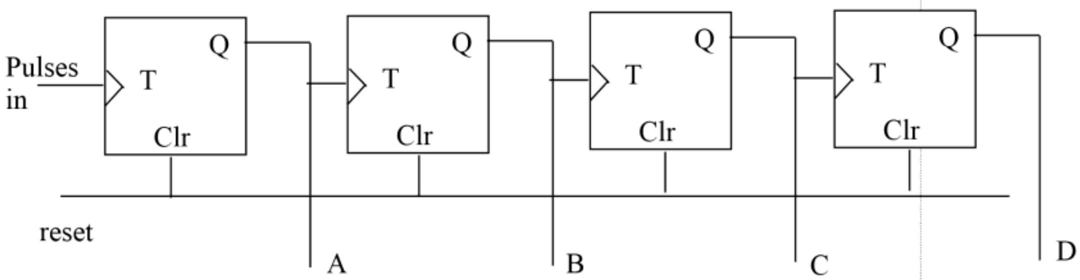
One use of a D flip-flop is to determine the direction of a rotating system that produces two output waves with some phase shift. With one wave the clock and the other the input, the output will be positive or negative depending on whether the input signal leads the clock or lags the clock.

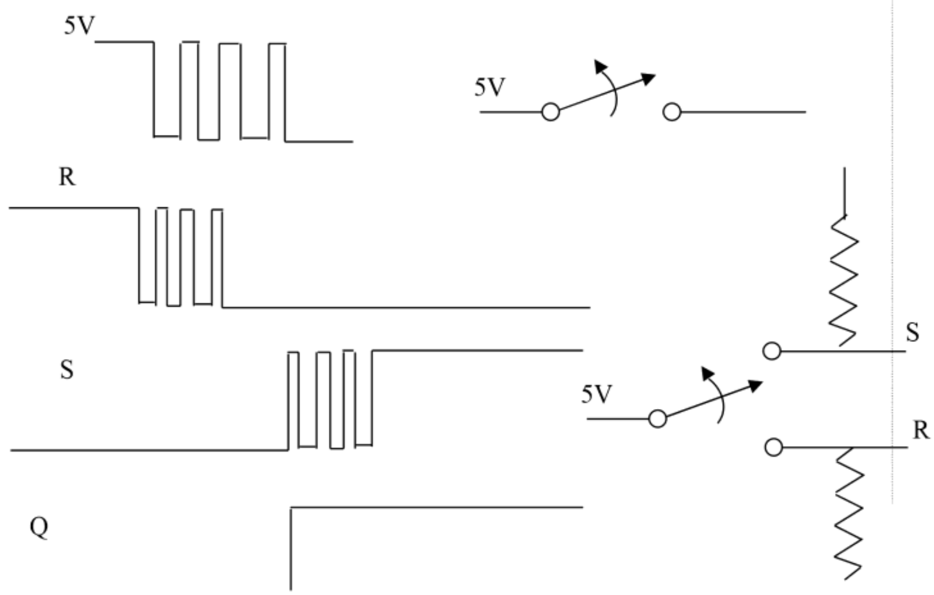
JK Flip-flops
A JK flip-flop is similar to a clocked RS flip-flop except that the state of both inputs high now causes the output to toggle.

Applications:

Pulse Counting
The circuit below demonstrates a scheme for pulse counting using T flip flops. This scheme outputs a four-bit binary number, ABCD.



Switch Debouncing
When a mechanical switch opens or closes mechanical vibrations cause the voltage signal to bounce for a small period before coming to rest at a new state. This can often cause difficulties in adding logic, for example if we were trying to count the number of times a door opens by counting rising edges on a switch. An RS flip-flop with set and reset inputs over the switch can correct this issue (see figure below).



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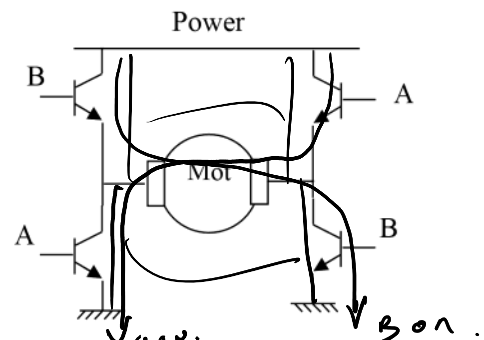
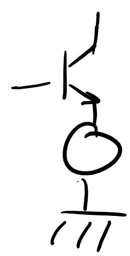
555 Timer:
Refer to Radio Shack electronics notebooks for samples of circuits using the 555 timer and Lab 1.

Power IC's:
Power transistors provide a means to amplify output logic signals to a level of power needed to drive output devices. One arrangement of these is in creating an H-bridge. An H-bridge is formed using four transistors and can provide bi-directional power to a device such as a motor. The figure below shows a schematic of an H-bridge:





Note: It is common to place a small ceramic capacitor between the *Vcc* and ground lead on an IC and to put a larger capacitor over the power supply line leading to a digital circuit.

A	B	Motor	
0	0	off	free spinning
1	0	CW	
0	1	CCW	
1	1	Dynamic Braking	

1 KHz or up.

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Spec Sheet: 7400

4. Functional diagram

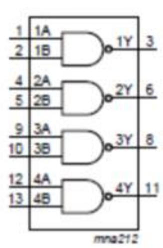


Fig 1. Logic symbol

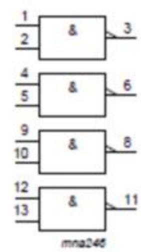


Fig 2. IEC logic symbol

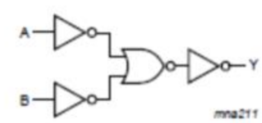


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

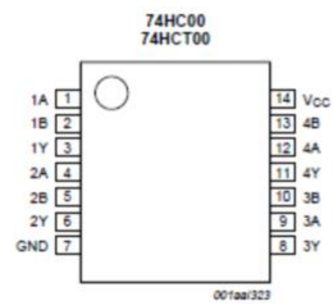
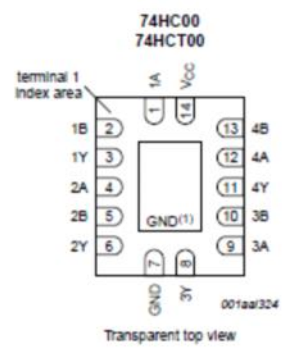


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input

Table 2. Pin description *...continued*

Symbol	Pin	Description
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

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8. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 µA; V_{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	-	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	-	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	µA

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Spec Sheet: SN754410 Quadruple Half-H Driver

SN754410
QUADRUPLE HALF-H DRIVER

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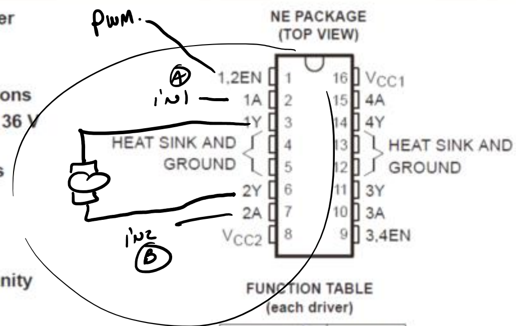
- **1-A Output-Current Capability Per Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Designed for Positive-Supply Applications**
- **Wide Supply-Voltage Range of 4.5 V to 36 V**
- **TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **Input Hysteresis Improves Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **No Output Glitch During Power Up or Power Down**
- **Improved Functional Replacement for the SGS L293**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each driver)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

description

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V.

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SN754410
QUADRUPLE HALF-H DRIVER

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APPLICATION INFORMATION

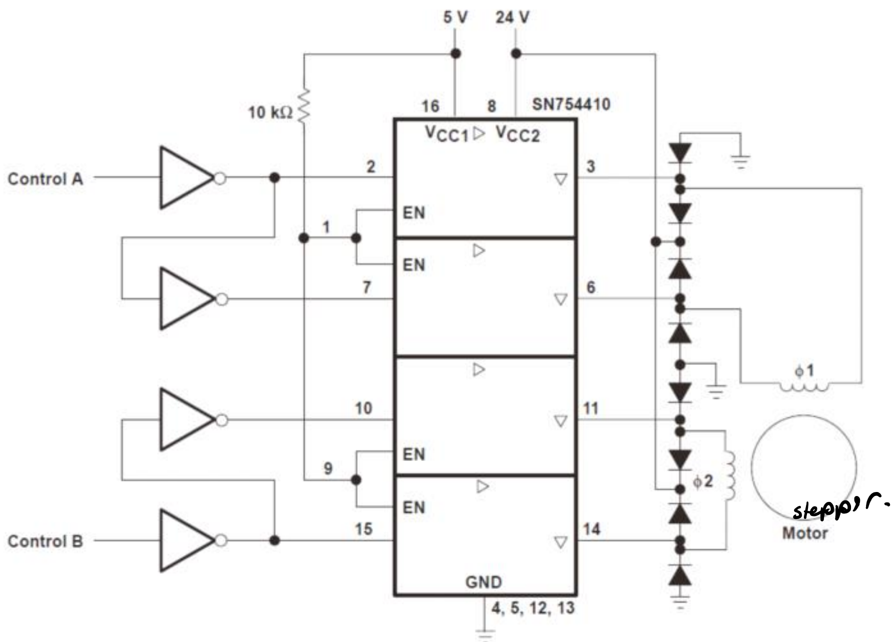

Figure 3. Two-Phase Motor Driver

SN754410
QUADRUPLE HALF-H DRIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output supply voltage range, V_{CC1} (see Note 1)	−0.5 V to 36 V
Output supply voltage range, V_{CC2}	−0.5 V to 36 V
Input voltage, V_I	36 V
Output voltage range, V_O	−3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms)	±2 A
Continuous output current, I_O	±1.1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075 mW
Operating free-air temperature range, T_A	−40°C to 85°C
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

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recommended operating conditions

	MIN	MAX	UNIT
Output supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3‡	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.