

# HH-D02 NearLink Development Board Specifications

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# Table of contents

1 Overview	3
1.1 Main specifications	5
2 Hardware description	6
2.1 Function layout	6
2.2 Pin definition	8
2.3 Dimensions	9
2.4 Functional block diagram	9

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# 1 Overview

#### model:HH-D02

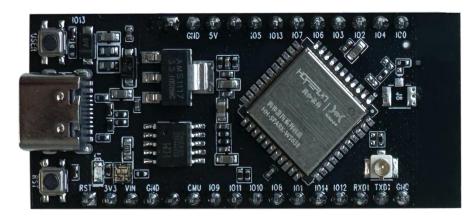


Figure 1-1 HH-D02 NearLink development board

The HH-D02 adopts the HiSilicon NearLink WS63E solution. The solution has support for 802.11b/g/n/ax wireless communication protocol, is also compatible with BLE5.3 protocol, has BLE Mesh and BLE gateway capabilities; supports SLE1.0 protocol and SLE gateway function; has radar human activity detection capability; can be based on Oniro lightweight system develops IoT scene functions and is an ideal choice for the field of IoT smart terminals.

HH-D02 has the following features:

# Stable and reliable communication capabilities

♦ Supports reliability communication algorithms such as TPC, automatic rate adjustment, and weak interference immunity in complex environments.

# Flexible networking capabilities

- Supports BLE Mesh networking
- ♦ Supports three networking methods: Wi-Fi, BLE or SLE

# Complete network support

Supports IPv4/IPv6 network functions



- ♦ Supports DHCPv4/DHCPv6 Client/Server
- ♦ Supports DNS Client function
- ♦ Supports mDNS function
- ♦ Supports CoAP/MQTT/HTTP/JSON basic components

# Powerful security engine

- Hardware implementation of AES128/256 encryption and decryption algorithm
- Hardware implementation of HASH-SHA256 and HMAC\_SHA256 algorithms
- ♦ Hardware implementation of RSA and ECC signature verification algorithms
- Hardware implements true random number generation, meeting FIPS140-2 random testing standards
- ♦ Hardware supports TLS/DTLS acceleration
- ♦ Hardware supports national secret algorithms SM2, SM3, SM4
- ♦ Internally integrated EFUSE, supporting secure storage, secure boot, and hardware ID
- ♦ Internally integrated MPU features support memory isolation features

# Open operating system

- Open operating system Oniro provides an open, efficient and secure system development and operating environment
- Rich mechanisms for low power consumption, small memory footprint, high stability, and high real-time performance.
- Flexible protocol support and expansion capabilities
- ♦ Secondary development interface



Multi-level development interface: operating system adaptation interface and system diagnostic interface, link layer interface, network layer interface



# 1.1 Main specifications

Table 1-1 Main specifications of HH-D02 NearLink development board

module	Specification description						
	High-performance 32bit microprocessor, maximum operating frequency						
CPU	240MHz						
subsystem	Embedded SRAM 606KB, ROM 300KB						
	Embedded 4MB Flash						
	1 SPI interface, 1 QSPI interface, 2 I2C interfaces, 1 I2S interface, 3 UART						
Peripheral	interfaces, 19 GPIO interfaces, 6 ADC inputs, 8 PWM (Note: the above						
interface	interfaces are implemented through multiplexing)						
	External crystal clock frequency 24MHz, 40MHz						
	Wi-Fi mode STA, Soft-AP and sniffer modes						
	Security mechanism WPS / WEP / WPA / WPA2 / WPA3						
Software	Encryption type UART Download						
	Software Development SDK						
	Network protocol IPv4, TCP/UDP/HTTP/FTP/MQTT						
	• 1×1 2.4GHz frequency band (ch1 ~ ch14)						
Wi-Fi	PHY supports IEEE 802.11b/g/n/ax MAC supports IEEE 802.11d/e/i/k/v/w						
	● Supports 802.11n 20MHz/40MHz bandwidth, support 802.11ax 20MHz						
	bandwidth						
	Supported maximum rate: 150Mbps@HT40 MCS7, 114.7Mbps@HE20 MCS9						
	Built-in PA and LNA, integrated TX/RX Switch, Balun, etc.						
	• Supports STA and AP forms. When used as an AP, it supports up to 6 STAs.						
	Supports A-MPDU, A-MSDU						
	Supports Block-ACK						
	Supports QoS to meet different business service quality requirements						
	Supports WPA/WPA2/WPA3 personal, WPS2.0						
	Supports RF self-calibration scheme						
	Supports STBC and LDPC						
	Supports radar sensing function						
	Bluetooth Low Energy (BLE)						
	• Supports BLE 4.0/4.1/4.2/5.0/5.1/5.2						
	<ul> <li>Supports 125Kbps, 500Kbps, 1Mbps, 2Mbps rates</li> </ul>						
Bluetooth	Supports multicast						
	Supports Class 1						
	Supports high power 20dBm						
	Supports BLE Mesh, support BLE gateway						
	Sparklink Low Energy (SLE)						
	Support SLE 1.0						
NearLink	Supports SLE 1MHz/2MHz/4MHz, maximum air interface rate 12Mbps						
	Supports Polar channel coding						
	Supports SLE gateway						
Other	Power supply voltage input: typical value 5V						



informatio	•	Operating temperature: -40°C ~ +85°C
n		

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# 2 Hardware description

#### 2.1 Function layout

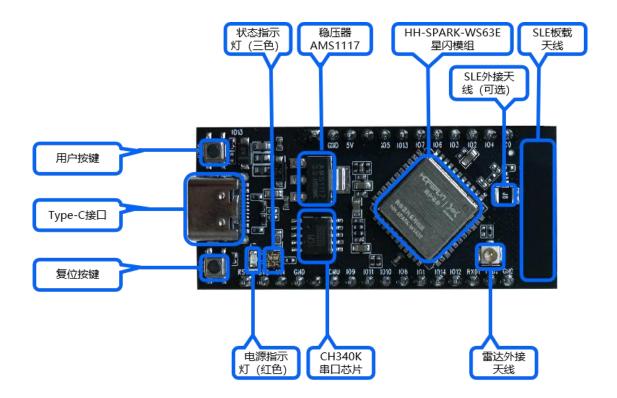


Figure 2-1 HH-D02 NearLink Development Board Functions

#### 1) User buttons

The USER button is a user-defined button. The switch S2 reports the "pressed/released" state to the WS63E via the GPIO13 pin. Its functionality is customizable through software.

# 2) Type-C interface

Provides power to the main board and the entire kit. Can be connected to a computer for serial debugging or system flashing.

#### 3) Reset button

RST is the reset button, used to reset the main board.

# 4) Power indicator light (red)

No.8 Pages 12 pages in total



Indicates the power status. The power indicator lights up when the system is powered on normally.

#### 5) Status indicator light (three colors)

Used to indicate the use of related IO port status, and the user controls it through PWM.

#### 6) Voltage regulator AMS1117

Converts 5V serial power to 3.3V for the chip's power supply.

#### 7) CH340K USB to serial port chip

When using the serial function, the driver for this chip must be installed on the PC.

# 8) HH-SPARK WS63E module

Highly integrated 2.4G Wi-Fi 6, BLE, and SLE with features such as high-speed transmission, low latency, high performance, and low power consumption. Includes a Type-C USB interface and a variety of pin functions.

#### 9) SLE onboard antenna

Used to enhance SLE/BLE/Wi-Fi signals

#### 10) SLE external antenna (optional)

Enhances SLE/BLE/Wi-Fi signals using the 1st-generation IPEX interface.

Can be used in special scenarios requiring strong signals by replacing and soldering a resistor.

# 11) Radar external antenna

Enhances radar signals, using the 1st-generation IPEX interface.



# 2.2 Pin definition



Figure 2-2 HH-D02 NearLink development board interface

Table 2-1 HH-D02 NearLink development board interface

		Table 2	-1 HH-DUZ NearLink development board interface
seri	name	type	Function
al			
num			
ber			
1	NC		Not connected
2	GND	PWR	power ground
3	5V	PWR	Power supply, 5V
4	NC		Not connected
5	GPIO05	10	GPIO05, SSI_DATA, SPI1_IO2, UART2_CTS, PWM5,DFT_JTAG_TCK
6	GPIO13	IO	GPIO13, UART_CTS, DFT_JTAG_TDO, JTAG_TMS
7	GPIO07	IO	GPIO07, PWM7, UART2_RXD, SPI0_SCK, I2S_MCLK, ADC0
8	GPIO06	10	GPIO06, PWM6, UART2_RTS, SPI1_SCK, DFT_JTAG_TDI, SPI0_OUT
9	GPIO03	10	GPIO03, PWM3, SPI1_IO1
10	GPIO02	10	GPIO02, PWM2, SPI_IO3
11	GPIO04	10	GPIO4, SSI_CLK, PWM4, SPI1_IO1, DFT_JTAG_TMS, JTAG_ENABLE
12	GPIO00	10	GPIO00, PWM0, SPI1_CSN, JTAG_TDI
13	GND	PWR	power ground
14	TXD1	10	UART1_TXD, GPIO15, I2C1_SDA
15	RXD1	10	UART1_RXD, GPIO16, I2C1_SCL
16	GPIO12	10	GPIO12, PWM4, I2S_DI, ADC5
17	GPIO14	10	GPIO14, DFT_JTAG_TRSTN, UART1_RTS
18	GPIO01	10	GPIO01, PWM1, SPI1_IO0, JTAG_MODE
19	GPIO08	10	GPIO08, PWM0, UART2_TXD, SPI0_CS1_N, ADC1
20	GPIO10	10	GPIO10, PWM2, SPI0_CS0_N, I2S_SCLK, ADC3
21	GPIO11	10	GPIO11, PWM3, SPI0_IN, I2S_LRCLK, ADC4
22	GPIO09	10	GPIO09, PWM1, SPI0_OUT, I2S_DO, JTAG_TDO, ADC2
23	NC		Not connected
24	NC		Not connected
25	GND	PWR	power ground
26	COME	PWR	Power supply, 5V



27	3V3	PWR	Power supply, 3.3V
28	RST	IO	RESET signal of main chip



#### 2.3 Dimensions

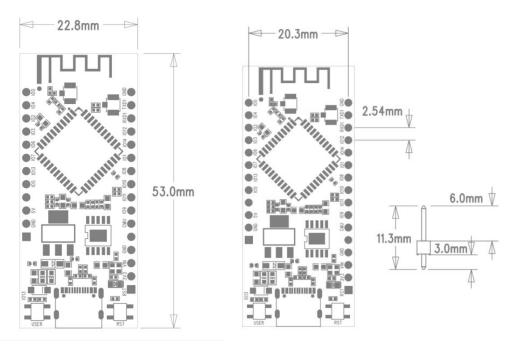


Figure 2-3 HH-D02 NearLink development board and pin header dimensions

# 2.4 Functional block diagram

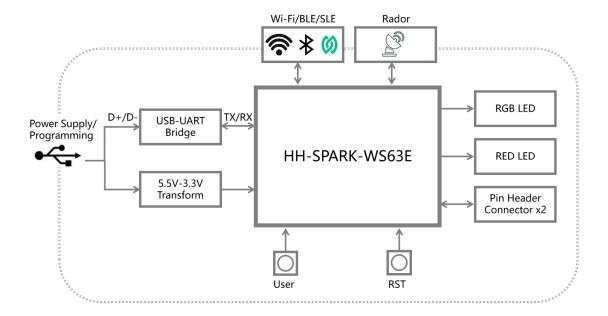


Figure 2-4 HH-D02 NearLink development board functional block diagram

No.12 Pages 12 pages in total