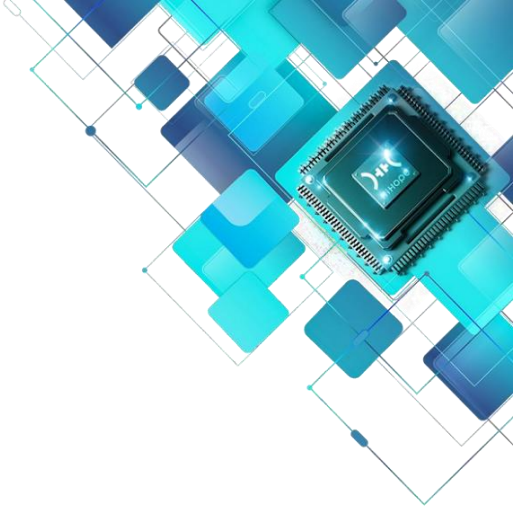
HOPERUN Information Technology 潤和軟件



# HH-D01 NearLink Development Board Specification V1.2

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# 1 Overview

**Model:**HH-D01

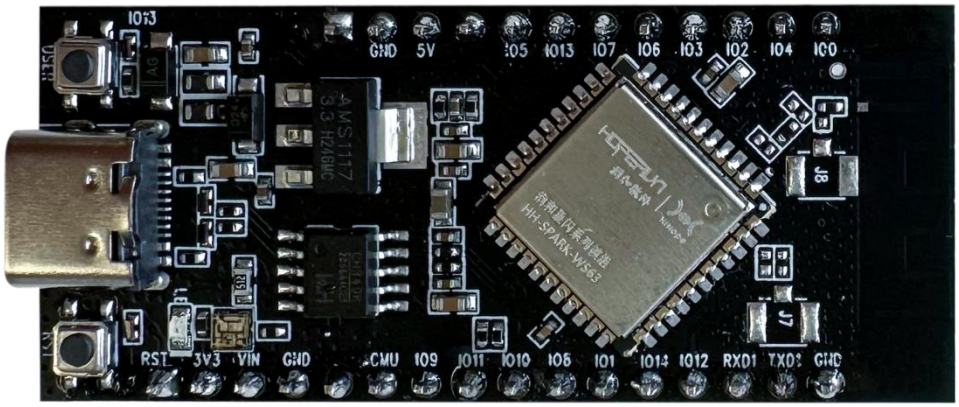


Figure 1-1 HH-D01 NearLink Development Board

The HH-D01 adopts the HiSilicon NearLink WS63 solution, offering support for the 802.11b/g/n/ax wireless communication protocols, and is also compatible with the BLE5.3 protocol.

- It features BLE Mesh and BLE gateway capabilities.
- Supports the SLE1.0 protocol and SLE gateway functionality.
- Enables IoT scenario development based on the lightweight Oniro system.

This makes it an ideal choice in the field of IoT smart terminals.

HH-D01 has the following features:

- **Stable and reliable communication capabilities**

✧ Supports reliable communication algorithms such as TPC, automatic rate, and weak interference immunity in complex environments

- **Flexible networking capabilities**

✧ Support BLE Mesh networking

✧ Supports three networking methods: Wi-Fi, BLE or SLE

● **Complete network support**

✧ Support IPv4/IPv6 network functions

✧ Support DHCPv4/DHCPv6 Client/Server

✧ Support DNS Client function

✧ Support mDNS function

✧ Support CoAP/MQTT/HTTP/JSON basic components

● **Powerful security engine**

✧ Hardware implementation of AES128/256 encryption and decryption algorithm

✧ Hardware implementation of HASH-SHA256 and HMAC_SHA256 algorithms

✧ Hardware implementation of RSA and ECC signature verification algorithms

✧ Hardware implements true random number generation, meeting FIPS140-2 random testing standards

✧ Hardware supports TLS/DTLS acceleration

✧ Hardware supports national secret algorithms SM2, SM3, SM4

✧ Internally integrated EFUSE, supporting secure storage, secure boot, and hardware ID

✧ Internally integrated MPU features support memory isolation features

● **Open operating system**

✧ Open operating system Oniro provides an open, efficient and secure system development and operating environment

✧ Rich low power consumption, small memory, high stability, high real-time mechanism

✧ Flexible protocol support and expansion capabilities

✧ Secondary development interface

✧ Multi-level development interface: operating system adaptation interface and system diagnostic interface, link layer interface, network layer interface

## 1.1 Main specifications

Table 1-1 Main specifications of HH-D01 NearLink development board

| Module | Specification description |
|---|---|
| **Wi-Fi** | ● 1×1 2.4GHz frequency band (ch1 ~ ch14)<br>● PHY supports IEEE 802.11b/g/n/ax MAC supports IEEE 802.11d/e/i/k/v/w<br>● Support 802.11n 20MHz/40MHz bandwidth, support 802.11ax 20MHz bandwidth<br>● Supported maximum rate: 150Mbps@HT40 MCS7, 114.7Mbps@HE20 MCS9<br>● Built-in PA and LNA, integrated TX/RX Switch, Balun, etc.<br>● Supports STA and AP forms. When used as an AP, it supports up to 6 STAs.<br>● Support A-MPDU, A-MSDU<br>● Support Block-ACK<br>● Support QoS to meet different business service quality requirements<br>● Support WPA/WPA2/WPA3 personal, WPS2.0<br>● Supports RF self-calibration scheme<br>● Supports STBC and LDPC |
| **Bluetooth** | ● Bluetooth Low Energy (BLE)<br>● Support BLE 4.0/4.1/4.2/5.0/5.1/5.2<br>● Supports 125Kbps, 500Kbps, 1Mbps, 2Mbps rates<br>● Support multicast<br>● Support Class 1<br>● Support high power 20dBm<br>● Support BLE Mesh, support BLE gateway |
| **NearLink** | ● Sparklink Low Energy (SLE)<br>● Support SLE 1.0<br>● Support SLE 1MHz/2MHz/4MHz, maximum air interface rate 12Mbps<br>● Supports Polar channel coding<br>● Support SLE gateway |
| **CPU subsystem** | ● High-performance 32bit microprocessor, maximum operating frequency 240MHz<br>● Embedded SRAM 606KB, ROM 300KB<br>● Embedded 4MB Flash |
| **Peripheral interface** | ● 1 SPI interface, 1 QSPI interface, 2 I2C interfaces, 1 I2S interface, 3 UART interfaces, 19 GPIO interfaces, 6 ADC inputs, 8 PWM (Note: the above interfaces are implemented through multiplexing)<br>● External crystal clock frequency 24MHz, 40MHz |
| **Software** | ● Wi-Fi mode STA, Soft-AP and sniffer modes<br>● Security mechanism WPS / WEP / WPA / WPA2 / WPA3<br>● Encryption type UART Download<br>● Software Development SDK<br>● Network protocol IPv4, TCP/UDP/HTTP/FTP/MQTT |
| **Other** | ● Supply voltage input: typical 5V |

| | |
|---|---|
| **information** | ● Operating temperature: -40℃ ~ +85℃ |

# 2 Hardware description

## 2.1 Function layout

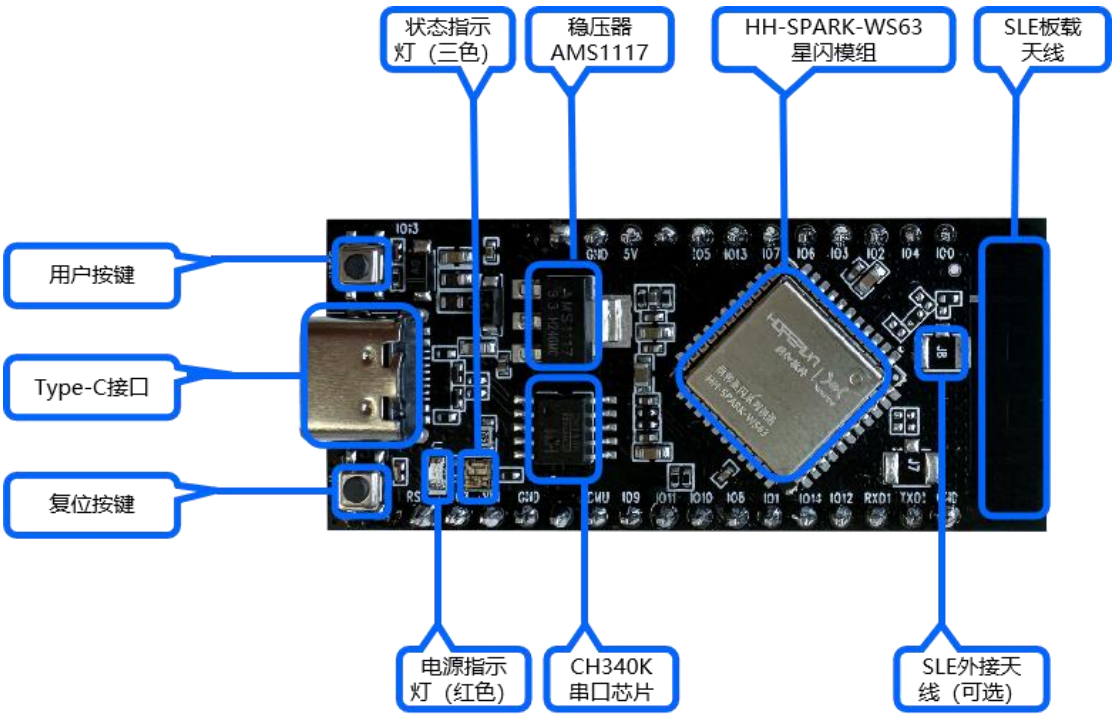


Figure 2-1 HH-D01 NearLink Development Board Functions

1) **User buttons**

USER is a user-defined button, and switch S2 reports the "pressed/released" status to WS63E through the GPIO13 pin. Functionality is customized by software.

2) **Type-C interface**

It can power the motherboard and the entire package, or connect to a computer for serial port debugging and system programming.

3) **reset button**

RST is the reset button, which can reset the motherboard.

4) **Power indicator light (red)**

It is used to indicate the power status. The power indicator light turns on after normal power-on.

5) **Status indicator light (three colors)**

Used to indicate the use of related IO port status, and the user controls it through PWM.

6) **Voltage regulator AMS1117**

Used to convert the 5V power supply of the serial port into the 3.3V power supply of the chip.

7) **CH340K USB to serial port chip**

When using the serial port function, the driver for the chip needs to be installed on the PC.

8) **HH-SPARK_WS63E module**

Highly integrated with 2.4G Wi-Fi 6, BLE and SLE, it features high-speed transmission, low latency, high performance, low power consumption, Type-C USB interface and rich pin functions.

9) **SLE onboard antenna**

Used to enhance SLE/BLE/Wi-Fi signals

10) **SLE external antenna (optional)**

It is used to enhance the SLE/BLE/Wi-Fi signal, using the 1st generation IPEX interface. It can be used in special scenarios that require a strong signal, which can be achieved by replacing the welding resistor.

## 2.2 Pin definition


Figure 2-2 HH-D01 NearLink development board interface

Table 2-1 HH-D01 NearLink development board interface

| serial number | name | type | Function |
|---|---|---|---|
| 1 | NC | | Not connected |
| 2 | GND | PWR | power ground |
| 3 | 5V | PWR | Power supply, 5V |
| 4 | NC | | Not connected |
| 5 | GPIO05 | IO | GPIO05，SSI_DATA，SPI1_IO2，UART2_CTS，PWM5,DFT_JTAG_TCK |
| 6 | GPIO13 | IO | GPIO13，UART_CTS，DFT_JTAG_TDO，JTAG_TMS |
| 7 | GPIO07 | IO | GPIO07，PWM7，UART2_RXD，SPI0_SCK，I2S_MCLK，ADC0 |
| 8 | GPIO06 | IO | GPIO06，PWM6，UART2_RTS，SPI1_SCK，DFT_JTAG_TDI，SPI0_OUT |
| 9 | GPIO03 | IO | GPIO03，PWM3，SPI1_IO1 |
| 10 | GPIO02 | IO | GPIO02，PWM2，SPI_IO3 |
| 11 | GPIO04 | IO | GPIO4，SSI_CLK，PWM4，SPI1_IO1，DFT_JTAG_TMS，JTAG_ENABLE |
| 12 | GPIO00 | IO | GPIO00，PWM0，SPI1_CSN，JTAG_TDI |
| 13 | GND | PWR | power ground |
| 14 | TXD1 | IO | UART1_TXD，GPIO15，I2C1_SDA |
| 15 | RXD1 | IO | UART1_RXD，GPIO16，I2C1_SCL |
| 16 | GPIO12 | IO | GPIO12，PWM4，I2S_DI，ADC5 |
| 17 | GPIO14 | IO | GPIO14，DFT_JTAG_TRSTN，UART1_RTS |
| 18 | GPIO01 | IO | GPIO01，PWM1，SPI1_IO0，JTAG_MODE |
| 19 | GPIO08 | IO | GPIO08，PWM0，UART2_TXD，SPI0_CS1_N，ADC1 |
| 20 | GPIO10 | IO | GPIO10，PWM2，SPI0_CS0_N，I2S_SCLK，ADC3 |
| 21 | GPIO11 | IO | GPIO11，PWM3，SPI0_IN，I2S_LRCLK，ADC4 |
| 22 | GPIO09 | IO | GPIO09，PWM1，SPI0_OUT，I2S_DO，JTAG_TDO，ADC2 |
| 23 | NC | | Not connected |
| 24 | NC | | Not connected |
| 25 | GND | PWR | power ground |

| | | | |
|---|---|---|---|
| 26 | COME | PWR | Power supply, 5V |
| 27 | 3V3 | PWR | Power supply, 3.3V |
| 28 | RST | IO | RESET signal of main chip |

## 2.3 Dimensions

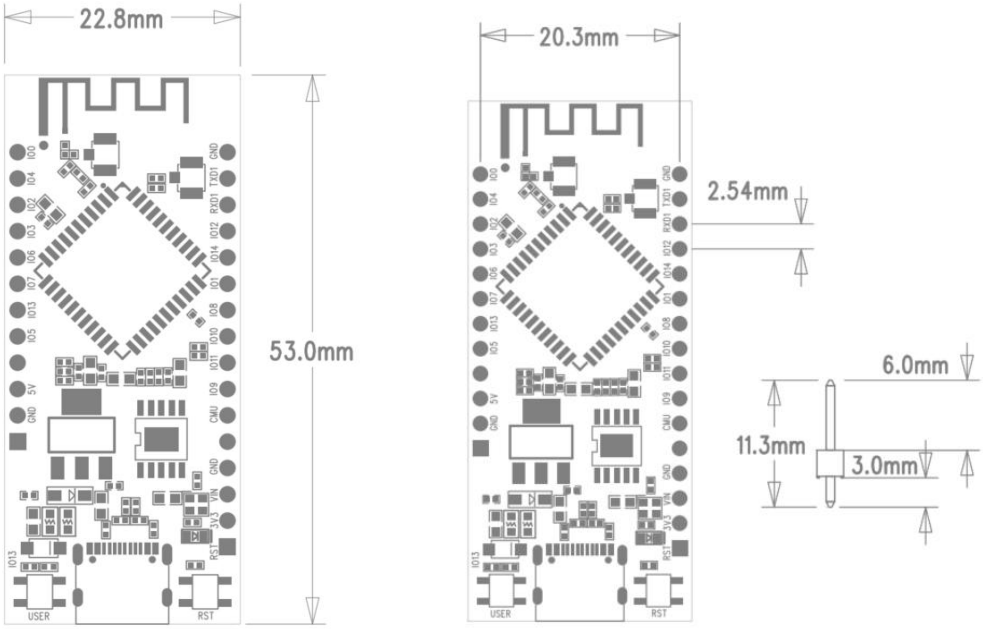


Figure 2-3 HH-D01 NearLink development board and pin header dimensions

## 2.4 Functional block diagram

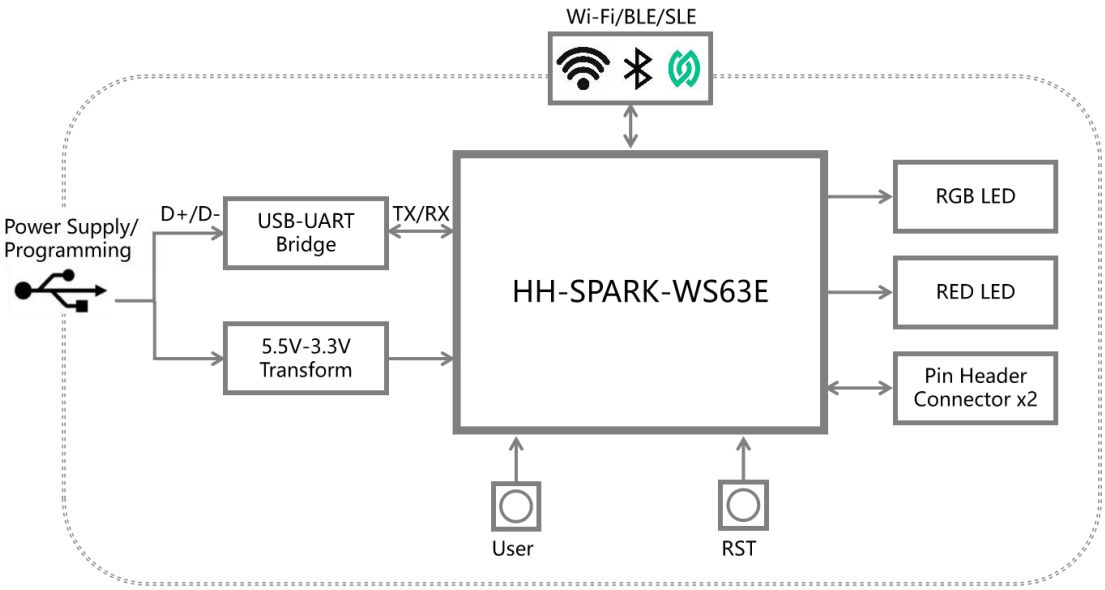


Figure 2-4 HH-D01 NearLink development board functional block diagram

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