no	operation	F	ALU-OP	add/sub	reg-dest	REG-WRITE	reg-scr	M-Write
1	**and**	**00**	00000	**11**	01	1	0	0
2	**or**	**01**	00000	**11**	01	1	0	0
3	**xor**	**10**	00000	**11**	01	1	0	0
4	**eqv**	**11**	00000	**11**	01	1	0	0
5	**add**	**00**	00001	**00**	01	1	0	0
6	**sub**	**01**	00001	**01**	01	1	0	0
7	**slt**	**10**	00001	**11**	01	1	0	0
8	**seq**	**11**	00001	**11**	01	1	0	0
no	**operation**	**F**	**ALU-OP**	**add/sub**	**reg-dest**	**REG-WRITE**	**reg-scr**	**M-Write**
9	**andi**	**X**	00100	**11**	01	1	0	0
10	**ori**	**X**	00101	**11**	01	1	0	0
11	**xori**	**X**	00110	**11**	01	1	0	0
12	**eqvi**	**X**	00111	**11**	01	1	0	0
13	**addi**	**X**	01000	**11**	01	1	0	0
14	**slti**	**X**	01001	**11**	01	1	0	0
15	**seqi**	**X**	01010	**11**	01	1	0	0
16	**sll**	**X**	01011	**11**	01	1	0	0
17	**srl**	**X**	01100	**11**	01	1	0	0
18	**ror**	**X**	01101	**11**	01	1	0	0
19	**beq**	**X**	01110	**11**	XX	0	1	0
20	**bnq**	**X**	01111	**11**	XX	0	1	0
21	**lw**	**X**	10000	**11**	01	1	X	0
22	**sw**	**X**	10001	**11**	XX	0	X	1
no	**operation**		**ALU-OP**	**add/sub**	**reg-dest**	**REG-WRITE**	**reg-scr**	**M-Write**
23	**beqz**	**X**	10100	**11**	XX	0	1	0
24	**bnez**	**X**	10101	**11**	XX	0	1	0
25	**bltz**	**X**	10110	**11**	XX	0	1	0
26	**bgez**	**X**	10111	**11**	XX	0	1	0
27	**bgtz**	**X**	11000	**11**	XX	0	1	0
28	**blez**	**X**	11001	**11**	XX	0	1	0
29	**jr**	**X**	11010	**11**	XX	0	1	0
30	**jalr**	**X**	11011	**11**	XX	1	1	0
31	**set**	**X**	11100	**11**	01	1	X	0
32	**sset**	**X**	11101	**11**	01	1	1	0
no	**operation**		**ALU-OP**	**add/sub**	**reg-dest**	**REG-WRITE**	**reg-scr**	**M-Write**
33	**j**	**X**	**xxxxx**	**11**	XX	0	X	0
34	**jal**	**X**	**xxxxx**	**11**	XX	1	X	0

M-Read	MemToReg	pcnext	branch	b-all	j-src
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
M-Read	**MemToReg**	**pcnext**	**branch**	**b-all**	**j-src**
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	00	00	x	xxx	0
0	XX	10	1	000	0
0	XX	10	1	001	0
1	01	00	x	xxx	0
0	XX	00	x	xxx	0
M-Read	**MemToReg**	**pcnext**	**branch**	**b-all**	**j-src**
0	XX	10	1	010	0
0	XX	10	1	011	0
0	XX	10	1	100	0
0	XX	10	1	101	0
0	xx	10	1	110	0
0	XX	10	1	111	0
0	XX	11	x	xxx	0
0	10	11	x	xxx	1
0	00	00	x	xxx	0
0	00	00	x	xxx	0
M-Read	**MemToReg**	**pcnext**	**branch**	**b-all**	**j-src**
0	XX	01	x	xxx	0
0	10	01	x	xxx	1

Control Signal
000001101100000000xxxx0
000001101100000000xxxx0
000001101100000000xxxx0
000001101100000000xxxx0
000010001100000000xxxx0
000010001100000000xxxx0
000010001100000000xxxx0
000010001100000000xxxx0
Control Signal
001001101100000000xxxx0
001011101100000000xxxx0
001101101100000000xxxx0
001111101100000000xxxx0
010001101100000000xxxx0
010011101100000000xxxx0
010101101100000000xxxx0
010111101100000000xxxx0
011001101100000000xxxx0
011011101100000000xxxx0
0111011XX0100XX1010000
0111011XX0100XX1010000
1000011011X010100xxxx0
1000111XX0X10XX00xxxx0
Control Signal
1010011XX0100XX1010100
1010111XX0100XX1010110
1011011XX0100XX1011000
1011111XX0100XX1011010
1100011XX0100xx1011100
1100111XX0100XX1011110
1101011XX0100XX11xxxx0
1101111XX11001011xxxx1
1110011011X000000xxxx0
111011101110000000xxxx0
Control Signal
xxxxx11XX0X00XX01xxxx0
xxxxx11XX1X001001xxxx1