Fayoum University
Faculty Of Engineering

Single Cycle Processor

Computer Architecture

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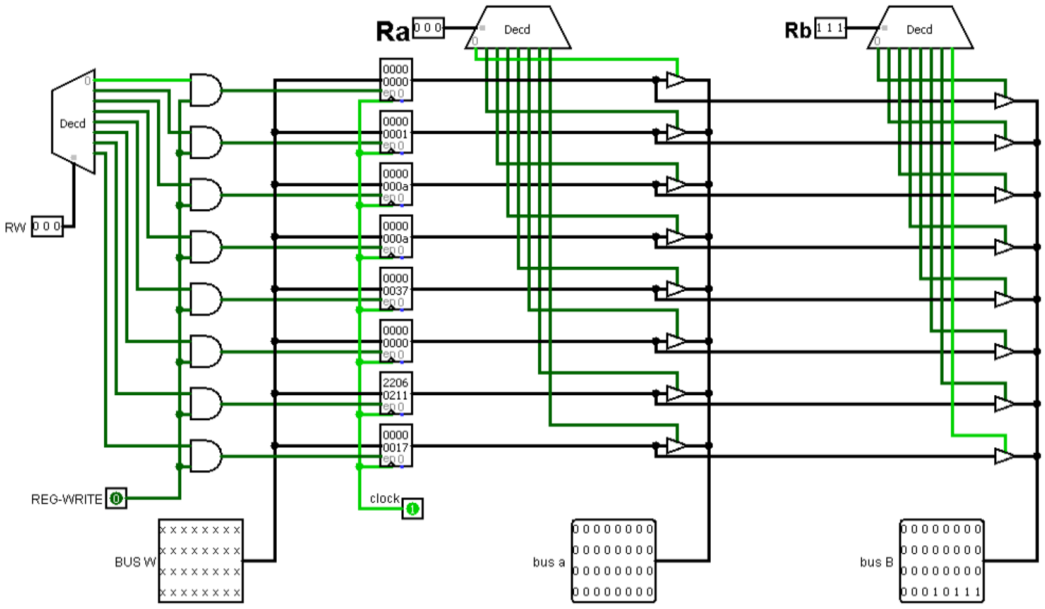
The description of each component:

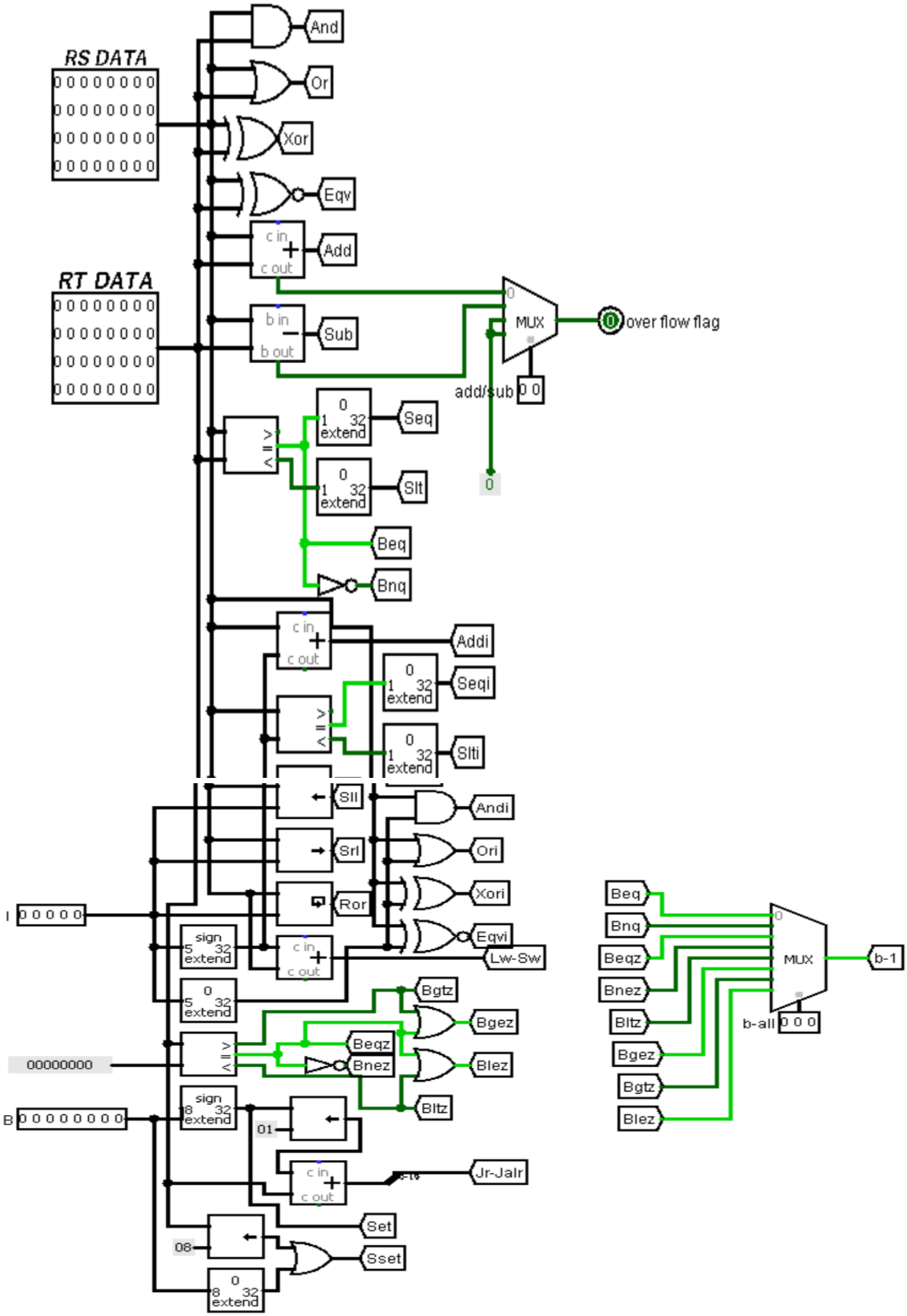
1. Register File

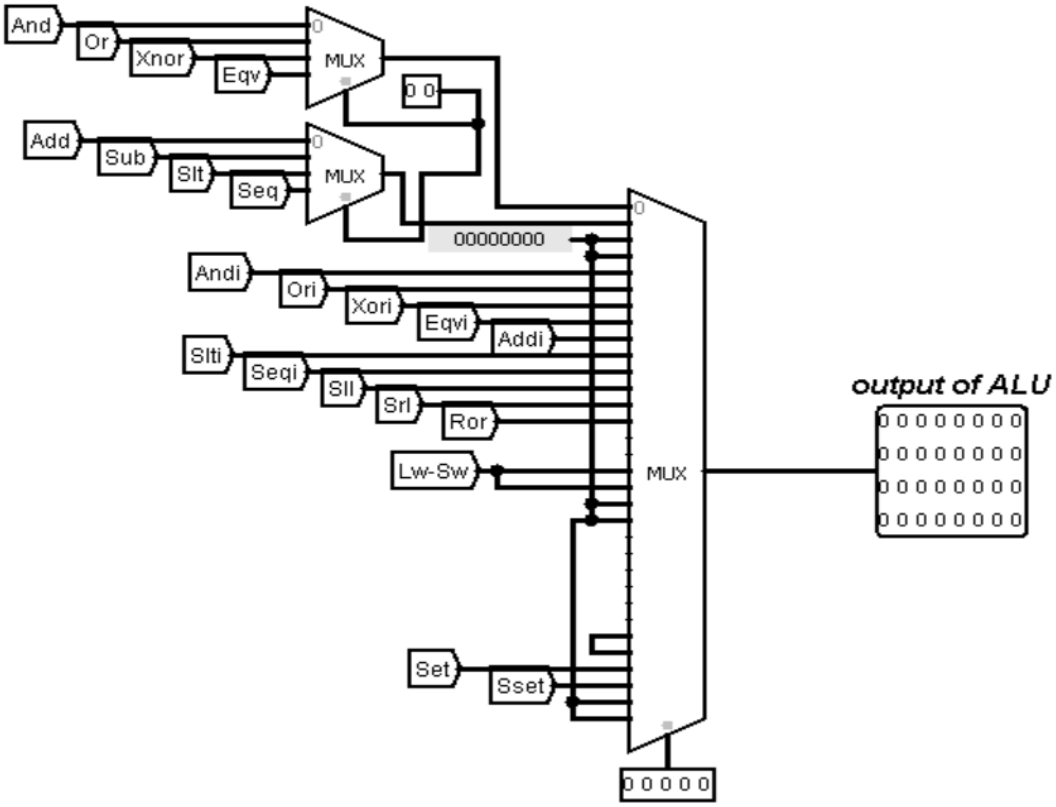
Array of processor registers which are temporary storage locations inside the CPU that hold data and addresses. The register file is the component that contains all the general-purpose registers of the microprocessor. A few CPUs also place special registers such as the PC and the status register in the register file. Other CPUs keep them separate.



2. ALU

An arithmetic-logic unit (ALU) is the part of a computer processor (CPU) that carries out arithmetic and logic operations on the operands in computer instruction words. The ALU does the following operations: R-Type (AND- OR- XOR- EQV- Add- Sub- Slt- SEQ), I-Type(AndI- ORI- XORI- EQVI- AddI- SLTI- SEQI- SLL- SRL- ROR- BEQ- BNE- LW- SW), B-Type (BEQZ- BNEZ- BLTZ- BGEZ- BGTZ- BLEZ- JR- JALR- SET- SSET) and J-Type (J- JAL).

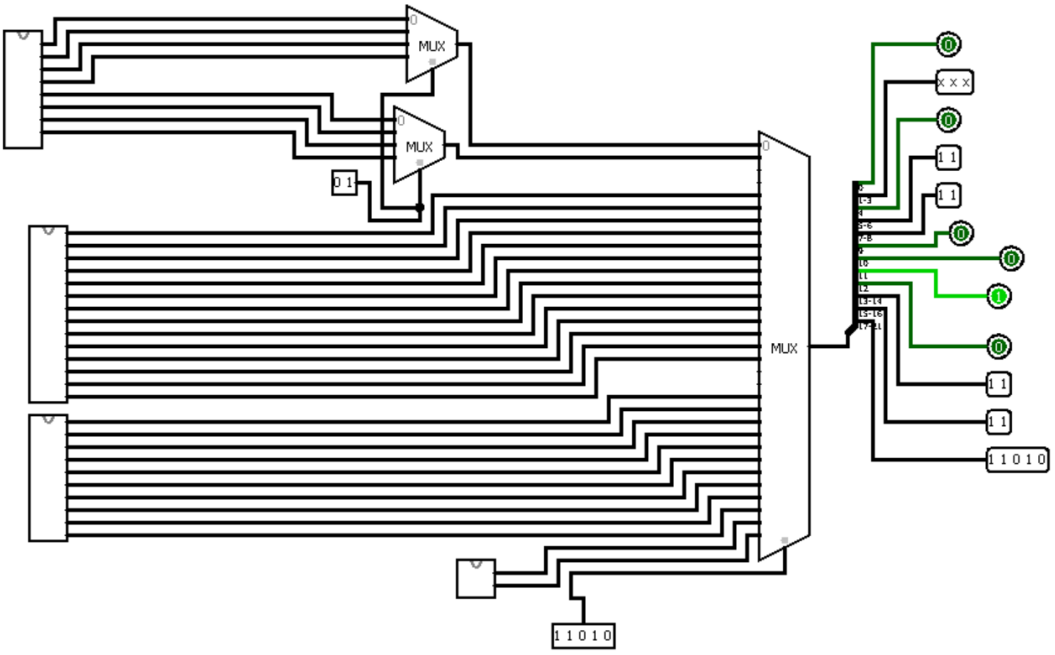

RS DATA
RT DATA
And
Or
Xor
Eqv
Add
Sub
MUX
over flow flag
add/sub
Seq
Slt
Beq
Bnq
Addi
Seqi
Slti
Sll
Srl
Ror
Andi
Ori
Xori
Eqvi
Lw-Sw
Bgtz
Bgez
Blez
Bltz
Beqz
Bnez
Jr-Jalr
Set
Sset
sign extend
extend
Beq
Bnq
Beqz
Bnez
Bltz
Bgez
Bgtz
Blez
MUX
b-all
b-1



3. Control Unit

The control unit of the central processing unit regulates and integrates the operations of the computer. It selects and retrieves instructions from the main memory in proper sequence and interprets them so as to activate the other functional elements of the system at the appropriate moment.

no	operation	F	op-code	ALU-OP	add/sub	reg-dest	REG-WRITE	reg-scr	M-Write	M-Read	MemToReg	pcnext	branch	b-all	j-src
1	and	0	0x00	0x00	11	01	1	0	0	0	00	00	x	xxx	0
2	or	1	0x00	0x00	11	01	1	0	0	0	00	00	x	xxx	0
3	xor	2	0x00	0x00	11	01	1	0	0	0	00	00	x	xxx	0
4	eqv	3	0x00	0x00	11	01	1	0	0	0	00	00	x	xxx	0
5	add	0	0x01	0x01	00	01	1	0	0	0	00	00	x	xxx	0
6	sub	1	0x01	0x01	01	01	1	0	0	0	00	00	x	xxx	0
7	slt	2	0x01	0x01	11	01	1	0	0	0	00	00	x	xxx	0
8	seq	3	0x01	0x01	11	01	1	0	0	0	00	00	x	xxx	0
no	operation		op-code	ALU-OP	add/sub	reg-dest	REG-WRITE	reg-scr	M-Write	M-Read	MemToReg	pcnext	branch	b-all	j-src
9	andi	xx	0x04	0x04	11	01	1	0	0	0	00	00	x	xxx	0
10	ori	xx	0x05	0x05	11	01	1	0	0	0	00	00	x	xxx	0
11	xori	xx	0x06	0x06	11	01	1	0	0	0	00	00	x	xxx	0
12	eqvi	xx	0x07	0x07	11	01	1	0	0	0	00	00	x	xxx	0
13	addi	xx	0x08	0x08	11	01	1	0	0	0	00	00	x	xxx	0
14	slti	xx	0x09	0x09	11	01	1	0	0	0	00	00	x	xxx	0
15	seqi	xx	0x0A	0x0A	11	01	1	0	0	0	00	00	x	xxx	0
16	sll	xx	0x0B	0x0B	11	01	1	0	0	0	00	00	x	xxx	0
17	srl	xx	0x0C	0x0C	11	01	1	0	0	0	00	00	x	xxx	0
18	ror	xx	0x0D	0x0D	11	01	1	0	0	0	00	00	x	xxx	0
19	beq	xx	0x0E	0x0E	11	XX	0	1	0	0	XX	10	1	000	0
20	bnq	xx	0x0F	0x0F	11	XX	0	1	0	0	XX	10	1	001	0
21	lw	xx	0x10	0x10	11	01	1	X	0	1	01	00	x	xxx	0
22	sw	xx	0x11	0x11	11	XX	0	X	1	0	XX	00	x	xxx	0
no	operation		op-code	ALU-OP	add/sub	reg-dest	REG-WRITE	reg-scr	M-Write	M-Read	MemToReg	pcnext	branch	b-all	j-src
23	beqz	xx	0x14	0x14	11	XX	0	1	0	0	XX	10	1	010	0
24	bnez	xx	0x15	0x15	11	XX	0	1	0	0	XX	10	1	011	0
25	bltz	xx	0x16	0x16	11	XX	0	1	0	0	XX	10	1	100	0
26	bgez	xx	0x17	0x17	11	XX	0	1	0	0	XX	10	1	101	0
27	bgtz	xx	0x18	0x18	11	XX	0	1	0	0	xx	10	1	110	0
28	blez	xx	0x19	0x19	11	XX	0	1	0	0	XX	10	1	111	0
29	jr	xx	0x1A	0x1A	11	XX	0	1	0	0	XX	11	x	xxx	0
30	jalr	xx	0x1B	0x1B	11	XX	1	1	0	0	10	11	x	xxx	1
31	set	xx	0x1C	0x1C	11	01	1	X	0	0	00	00	x	xxx	0
32	sset	xx	0x1D	0x1D	11	01	1	1	0	0	00	00	x	xxx	0
no	operation		op-code	ALU-OP	add/sub	reg-dest	REG-WRITE	reg-scr	M-Write	M-Read	MemToReg	pcnext	branch	b-all	j-src
33	j	xx	0x1E	X	11	XX	0	X	0	0	XX	01	x	xxx	0
34	jal	xx	0x1F	X	11	XX	1	X	0	0	10	01	x	xxx	1



4. Data Path

A data-path is a collection of functional units, such as arithmetic logic unit or multipliers that perform data processing operations, registers and buses. Along with the control unit it composes the central processing unit. Simply the control unit receives external instructions or commands which it converts to into a sequence of control signals that the control unit applies to the data-path to implement a sequence of register transfer level operations.