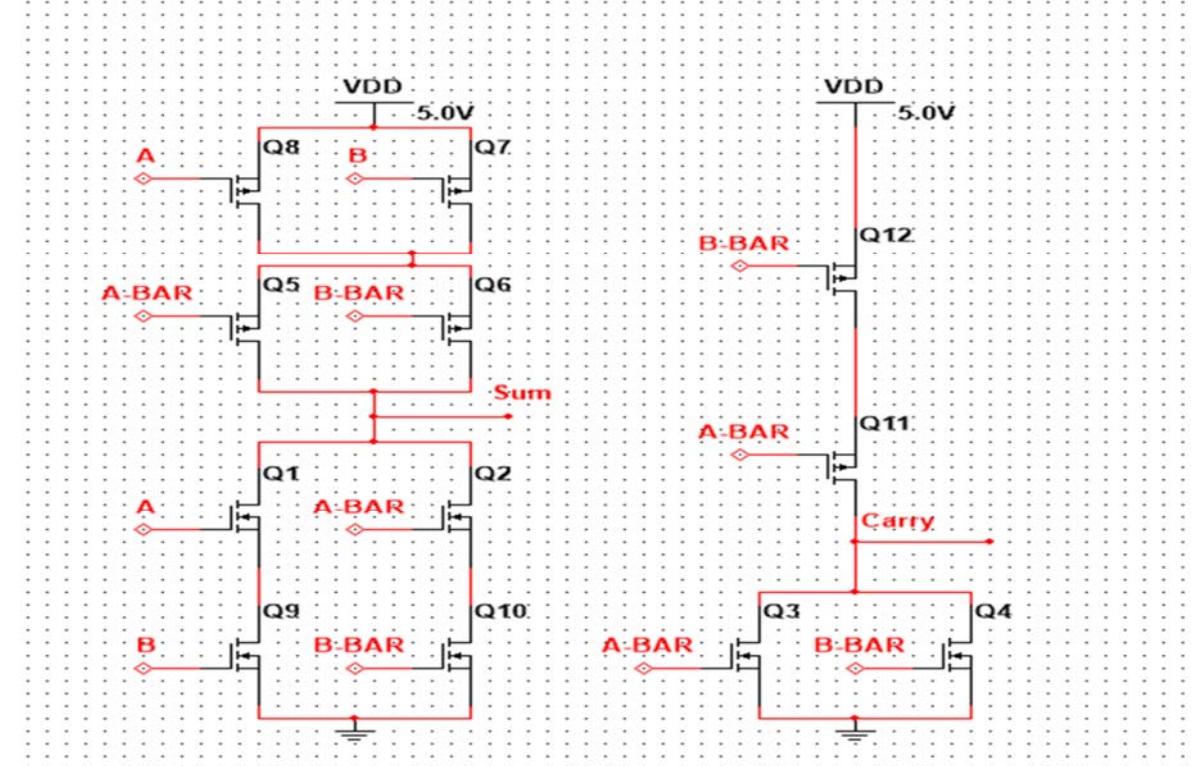


## Final project report

حسام معتز حسام

### I. Logic characterization

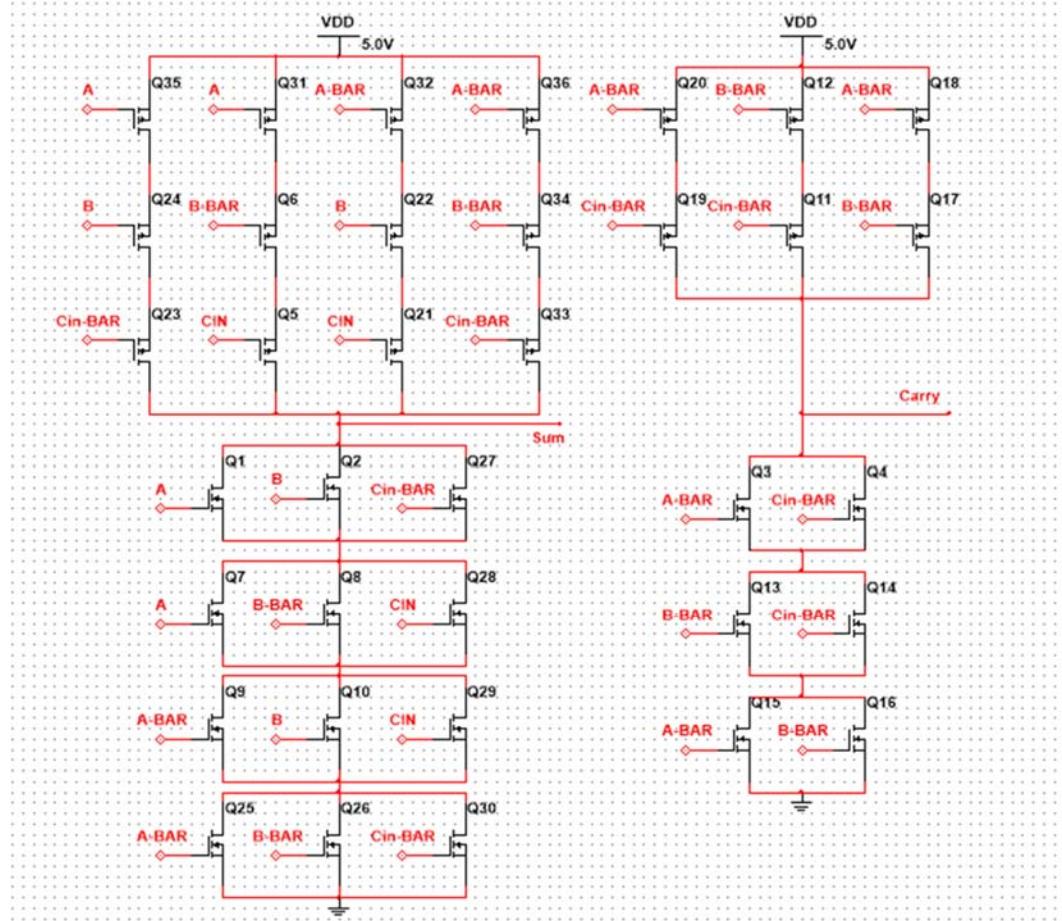
Schematic for HA



Truth table(s) for HA

A	B	Sum	Cout (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Schematic for FA



Truth table(s) for FA

A	B	Cin	Sum	Cout (carry)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

HA logic equations

$$\text{Sum} = A \oplus B \quad \text{Cout} = AB$$

FA logic equations

$$\text{Sum} = A \oplus B \oplus \text{Cin} \quad \text{Cout} = AC_{\text{in}} + BC_{\text{in}} + AB$$

## II. Pin design

Total number of input pins

There are four 5-bit input numbers that are added together. We also have one clock and one VDD as well as one GND. Thus, the total number of input pins is 23

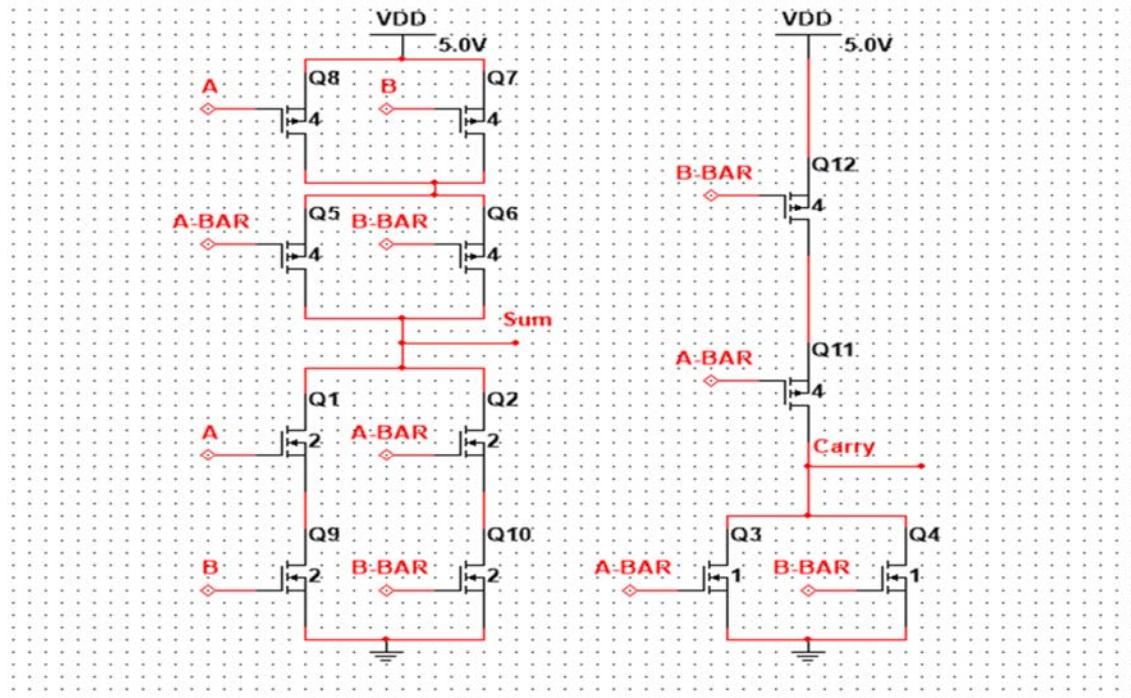
Total number of output pins

The FA has 7 output pins. Therefore, the total number of output pins is 7.

Pin name	Pin type (in, out, inout)	Type (signal, power, clock)
A0	In	Signal
A1	In	Signal
A2	In	Signal
A3	In	Signal
A4	Out	Signal
Cout	Out	Signal
VDD	In	Power
GND	In	Power
Clk	In	Clock

## III. Circuit characterization

HA schematics with sizing



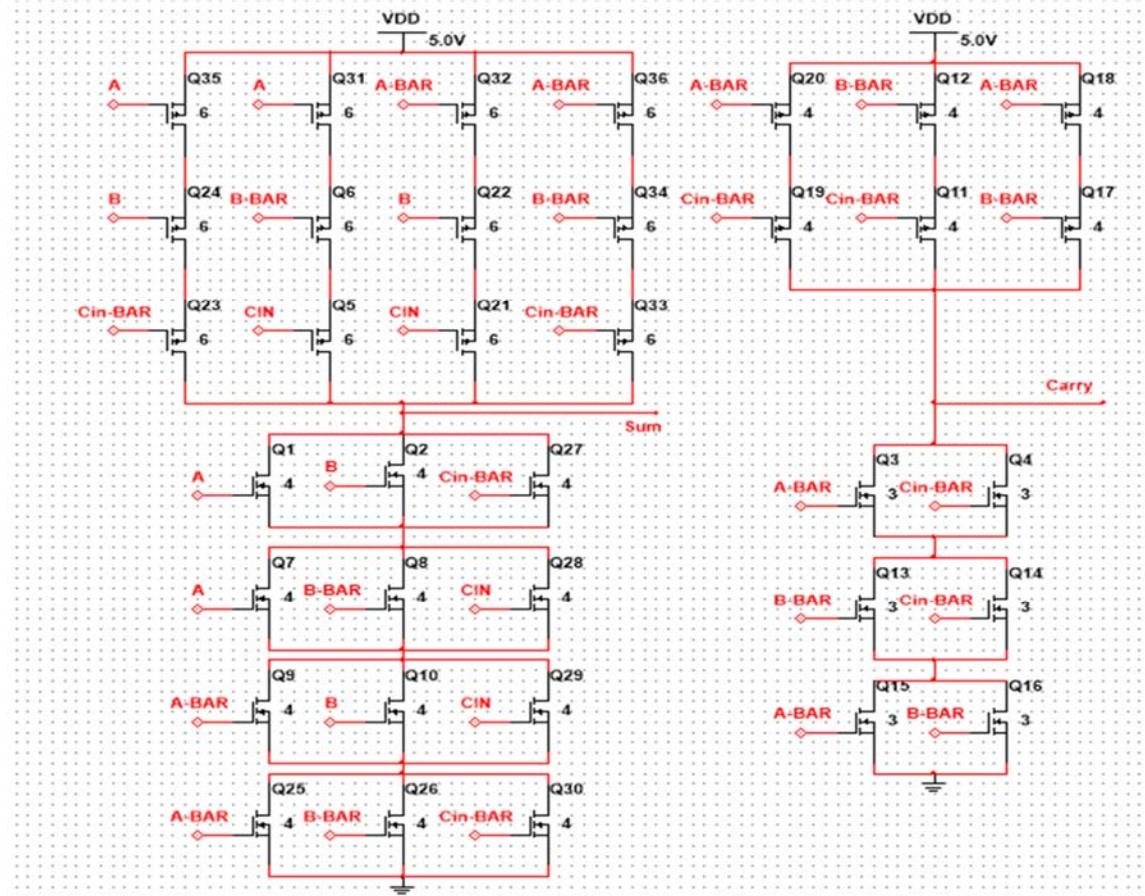
HA delay characterization (Sum)

	W. case	B. case	Ext factor w.case	Ext factor w. case
HL	12 RoCo	6 RoCo	$1 + (C_x / 12 C_o)$	$1 + (C_x / 12 C_o)$
LH	12 RoCo	6 RoCo	$1 + (C_x / 12 C_o)$	$1 + (C_x / 12 C_o)$

HA delay characterization (Cout)

	W. case	B. case	Ext factor w.case	Ext factor w. case
HL	6 RoCo	3 RoCo	$1 + (C_x / 6 C_o)$	$1 + (C_x / 6 C_o)$
LH	6 RoCo	6 RoCo	$1 + (C_x / 6 C_o)$	$1 + (C_x / 6 C_o)$

FA schematics with sizing



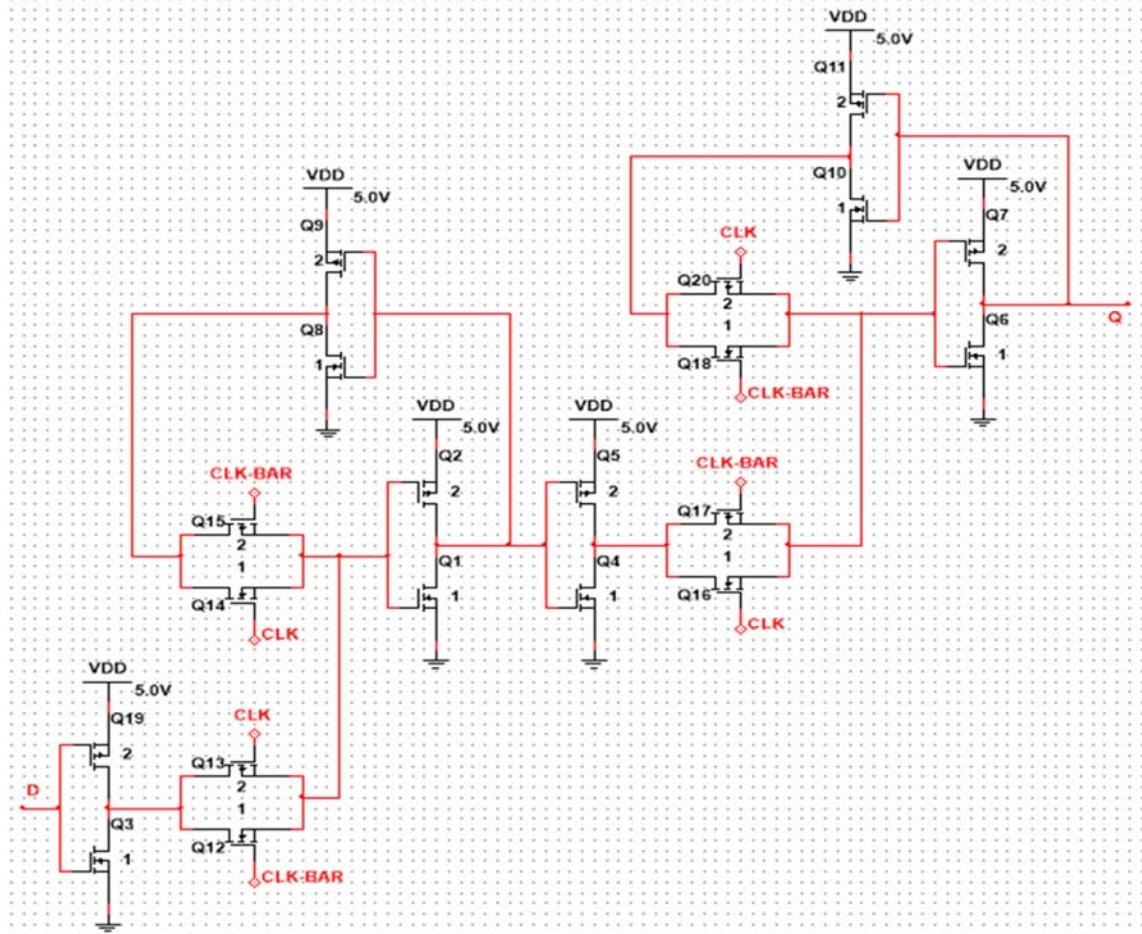
FA delay characterization (Sum)

	W. case	B. case	Ext factor w.case	Ext factor w. case
HL	36 RoCo	12 RoCo	$1 + (C_x / 36 C_o)$	$1 + (C_x / 36 C_o)$
LH	36 RoCo	9 RoCo	$1 + (C_x / 36 C_o)$	$1 + (C_x / 36 C_o)$

### FA delay characterization (Cout)

	W. case	B. case	Ext factor w.case	Ext factor w. case
HL	18 RoCo	9 RoCo	$1 + (C_x / 18 C_0)$	$1 + (C_x / 18 C_0)$
LH	18 RoCo	6 RoCo	$1 + (C_x / 18 C_0)$	$1 + (C_x / 18 C_0)$

### FF schematic with sizing



### Unloaded setup time calculation

$$t_{su} = t_{I1} + t_{T1} + t_{I2} + t_{I3}$$

$$t_{I1} = RC = R_{I1} (C_{dnI1} + C_{dpI1} + C_{dnT1} + C_{dpT1}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) = 6R_0C_0$$

$$\begin{aligned} t_{T1} &= RC = (R_{nT1} \parallel R_{pT1}) (C_{dnT1} + C_{dpT1} + C_{dnT2} + C_{dpT2} + C_{gnI2} + C_{gpI2}) = (R_0/2) (C_0 + \\ &2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 4.5R_0C_0 \end{aligned}$$

$$t_{I2} = RC = R_{I2} (C_{dnI2} + C_{dpI2} + C_{gnI3} + C_{gpI3} + C_{gnI4} + C_{gpI4}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 9R_0C_0$$

$$t_{I3} = RC = R_{I3} (C_{dnI3} + C_{dpI3} + C_{dnT2} + C_{dpT2}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) = 6R_0C_0$$

$$t_{su} = 6R_0C_0 + 4.5R_0C_0 + 9R_0C_0 + 6R_0C_0 = 25.5R_0C_0$$

**Unloaded CQ delay calculation**

$$t_{cq} = t_{T3} + t_{I5}$$

$$t_{T3} = RC = (R_{nT3} \parallel R_{pT3}) (C_{dnT3} + C_{dpT3} + C_{dnT4} + C_{dpT4} + C_{gnI5} + C_{gpI5}) = (R_0/2) (C_0 + 2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 4.5R_0C_0$$

$$t_{I5} = RC = R_{I5} (C_{dnI5} + C_{dpI5} + C_{gnI6} + C_{gpI6}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) = 6R_0C_0$$

$$t_{cq} = 4.5R_0C_0 + 6R_0C_0 = 10.5R_0C_0$$

**Setup time external delay factor derivation**

$$t_{su} = t_{I1} + t_{T1} + t_{I2} + t_{I3}$$

$$t_{I1} = RC = R_{I1} (C_{dnI1} + C_{dpI1} + C_{dnT1} + C_{dpT1}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) = 6R_0C_0$$

$$t_{T1} = RC = (R_{nT1} \parallel R_{pT1}) (C_{dnT1} + C_{dpT1} + C_{dnT2} + C_{dpT2} + C_{gnI2} + C_{gpI2}) = (R_0/2) (C_0 + 2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 4.5R_0C_0$$

$$t_{I2} = RC = R_{I2} (C_{dnI2} + C_{dpI2} + C_{gnI3} + C_{gpI3} + C_{gnI4} + C_{gpI4}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 9R_0C_0$$

$$t_{I3} = RC = R_{I3} (C_{dnI3} + C_{dpI3} + C_{dnT2} + C_{dpT2}) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) = 6R_0C_0$$

$$t_{su} = 6R_0C_0 + 4.5R_0C_0 + 9R_0C_0 + 6R_0C_0 = 25.5R_0C_0$$

Since the external capacitance is at the output of the FF, it won't affect the setup time. Hence, we don't have an external delay factor for setup time.

CQ delay external delay factor derivation

$$t_{cq} = t_{T3} + t_{I5}$$

$$t_{T3} = RC = (R_{nT3} \parallel R_{pT3}) (C_{dnT3} + C_{dpT3} + C_{dnT4} + C_{dpT4} + C_{gnI5} + C_{gpI5}) = (R_0/2) (C_0 + 2C_0 + C_0 + 2C_0 + C_0 + 2C_0) = 4.5R_0C_0$$

$$t_{I5} = RC = R_{I5} (C_{dnI5} + C_{dpI5} + C_{gnI6} + C_{gpI6} + C_x) = R_0 (C_0 + 2C_0 + C_0 + 2C_0) + R_0 C_x = 6R_0C_0 + R_0C_x$$

$$t_{cq} = 4.5R_0C_0 + 6R_0C_0 + R_0C_x = 10.5R_0C_0 (1 + (C_x / 10.5C_0))$$

Hence, the external factor is  $(1 + (C_x / 10.5C_0))$

Insert table for register delay here

$t_{su}$	$t_{cq}$	$t_{su}$ Ext. factor	$t_{cq}$ Ext. factor
25.5 RoCo	10.5 RoCo	-	$1 + (C_x / 10.5 C_0)$

#### IV. Synthesis

Number of CMOS gates

HA has 2 CMOS, FA has 2 CMOS, FF has 10 CMOS. The circuit has 3HA, 13FA, 39FF

Therefore total number of CMOS is 422

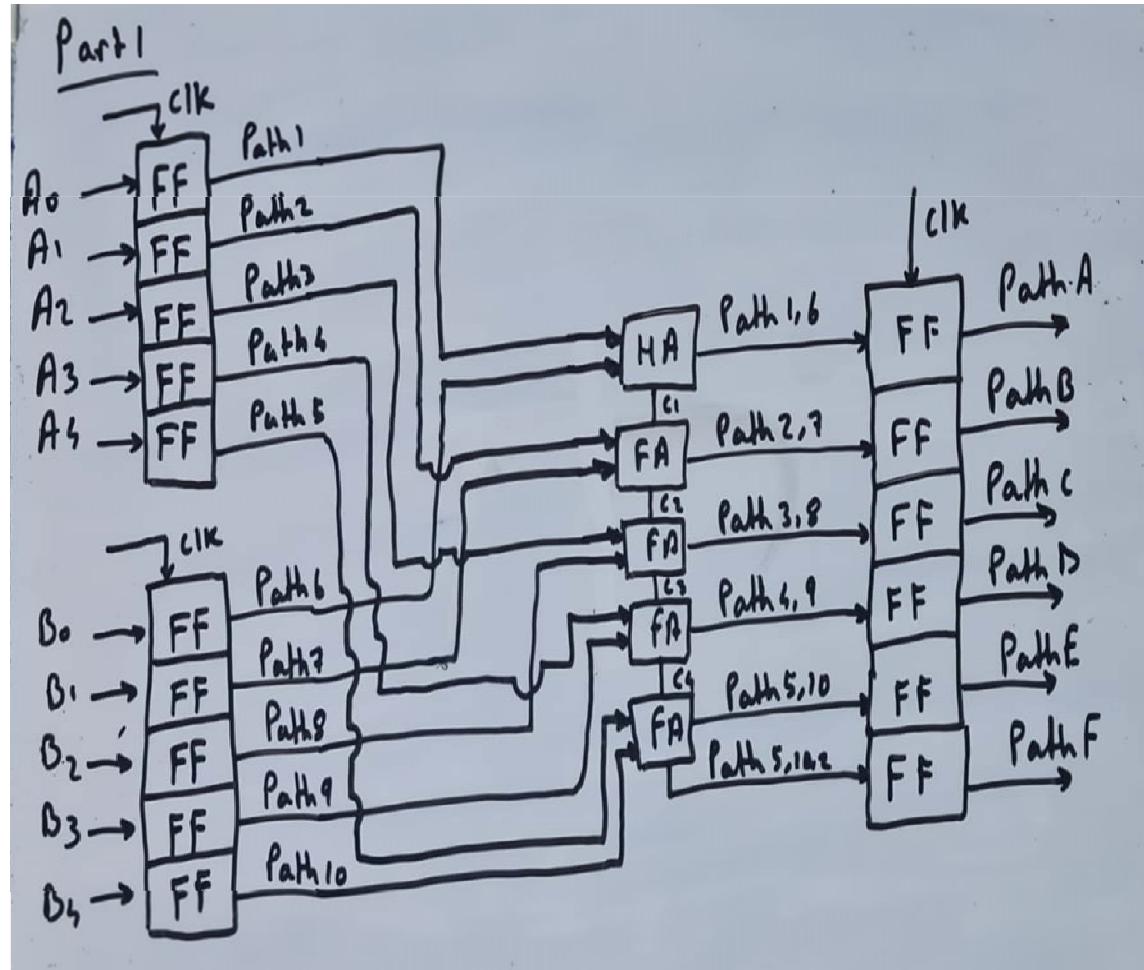
Number of transistors

Total number of transistors is 1284

Diagram of connections of cells (not placement and routing). Please number the paths as path1, path2, etc.

I divided the full chip into 3 main register parts

### Part 1



Then we will calculate its path delay calculations, best and worst cases

#### Worst case:

Longest path or critical path

FF->path1->HA->C1->FA->C2->FA->C3->FA->C4->FA->PATH5,10->FF

$$T_{lh} = T_{lh} = t_{CQ} + t_{HAcarry} + t_{FACarry} + t_{FACarry} + t_{FACarry} + t_{FASum} + t_{SU} = 368R_0C_0$$

#### Best case:

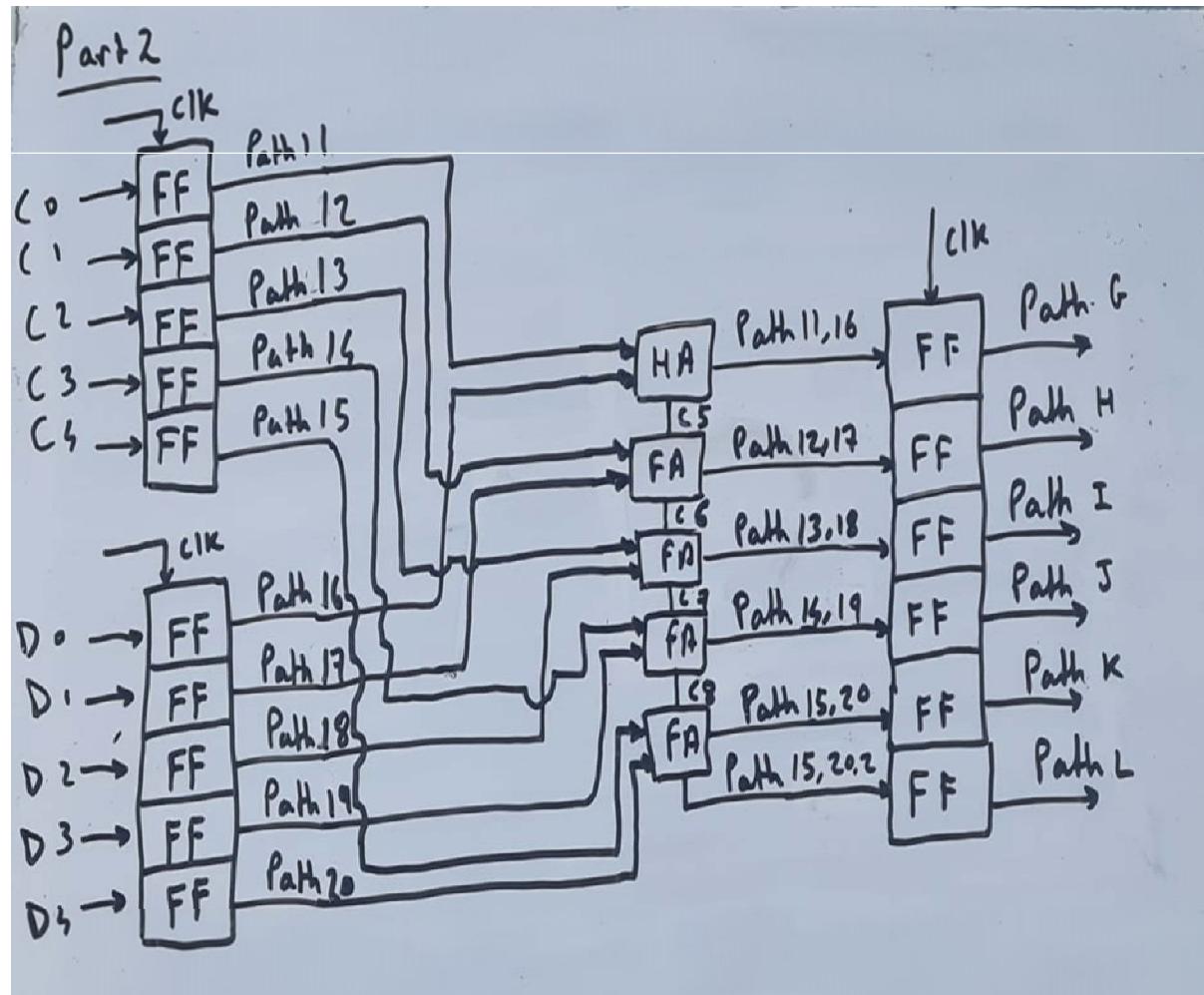
Longest path or critical path

FF->path1->HA->C1->FA->C2->FA->C3->FA->C4->FA->PATH5,10->FF

$$T_{lh} = t_{CQ} + t_{HAcarryHL} + t_{FACarryHL} + t_{FACarryHL} + t_{FACarryHL} + t_{FASumHL} + t_{SU} = 204R_0C_0$$

$$T_{lh} = t_{CQ} + t_{HAcarryLH} + t_{FACarryLH} + t_{FACarryLH} + t_{FACarryLH} + t_{FASumLH} + t_{SU} = 194.75R_0C_0$$

## Part 2



Then we will calculate its path delay calculations, best and worst cases

### Worst case:

Longest path or critical path

FF->path11->HA->C5->FA->C6->FA->C7->FA->C8->FA->PATH15,20->FF

$$T_{lh} = T_{lh} = t_{CQ} + t_{HAcarry} + t_{FACarry} + t_{FACarry} + t_{FASum} + t_{SU} = 368R_0C_0$$

### Best case:

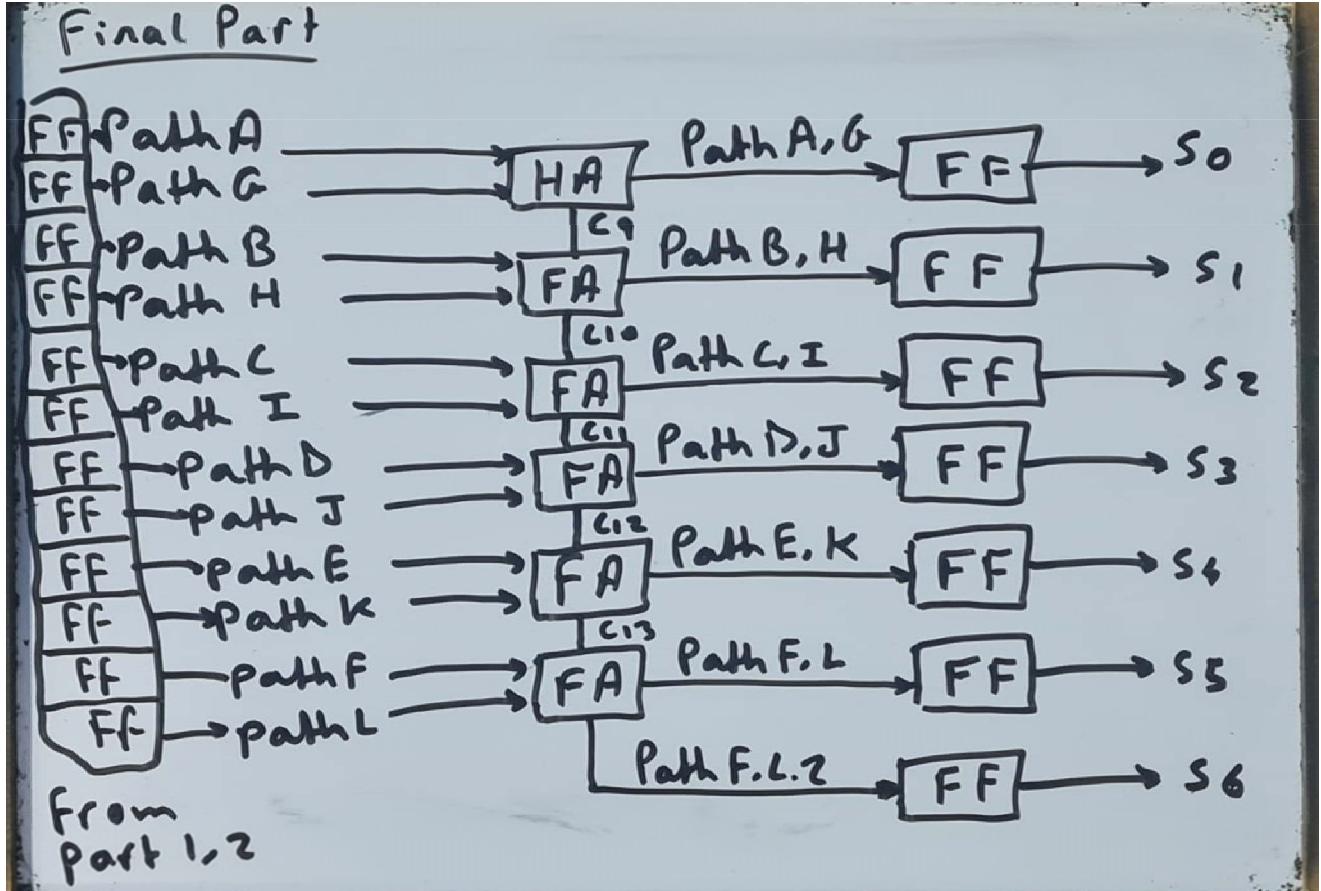
Longest path or critical path

FF->path11->HA->C5->FA->C6->FA->C7->FA->C8->FA->PATH15,20->FF

$$T_{lh} = t_{CQ} + t_{HAcarryHL} + t_{FACarryHL} + t_{FACarryHL} + t_{FACarryHL} + t_{FASumHL} + t_{SU} = 204R_0C_0$$

$$T_{lh} = t_{CQ} + t_{HAcarryLH} + t_{FACarryLH} + t_{FACarryLH} + t_{FACarryLH} + t_{FASumLH} + t_{SU} = 194.75R_0C_0$$

Final part which is part 3



Then we will calculate its path delay calculations, best and worst cases

Worst case:

Longest path or critical path

FF->pathA->HA->C9->FA->C10->FA->C11->FA->C12->FA->C13->FA->PATHF,L->FF

$$T_{lh} = T_{lh} = t_{CQ} + t_{HAcarry} + t_{FAcarry} + t_{FAcarry} + t_{FAcarry} + t_{FAsum} + t_{SU} = 440R_0C_0$$

Best case:

Longest path or critical path

FF->pathA->HA->C9->FA->C10->FA->C11->FA->C12->FA->C13->FA->PATHF,L->FF

$$T_{lh} = t_{CQ} + t_{HAcarryHL} + t_{FAcarryHL} + t_{FAcarryHL} + t_{FAcarryHL} + t_{FAcarryHL} + t_{FAsumHL} + t_{SU}$$

$$= 240R_0C_0$$

$$T_{lh} = t_{CQ} + t_{HAcarryLH} + t_{FAcarryLH} + t_{FAcarryLH} + t_{FAcarryLH} + t_{FAsumLH} + t_{SU}$$

$$= 218.75R_0C_0$$