Credit Hours System

ELCN321

Cairo University

Faculty of Engineering

VLSI

ANALOG PROJECT

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IMPLEMENTATION FOR P-MOS

Date / / Object

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VLSI
Analog project

1) For P-Mos transistors

↳ each transistor is of $\frac{40\,um}{1\,um}$ → each is of width 40 um

∴ we have total width of 120 um (length → 1um)

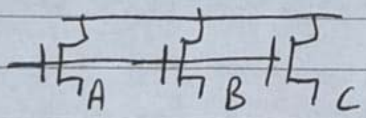
↳ The stack consists of the 3 pMos

we will use K = 12 → we will use 12 number of fingers

∴ the width of the stack is $\frac{120nm}{12} = 10nm$

∴ Assume the name of the 3 transistors are A, B, C

∴ gate size of $\frac{10nm}{1um}$ (poly)



∴ each transistor is of 4 fingers and the size of the finger is $\frac{10nm}{1um}$

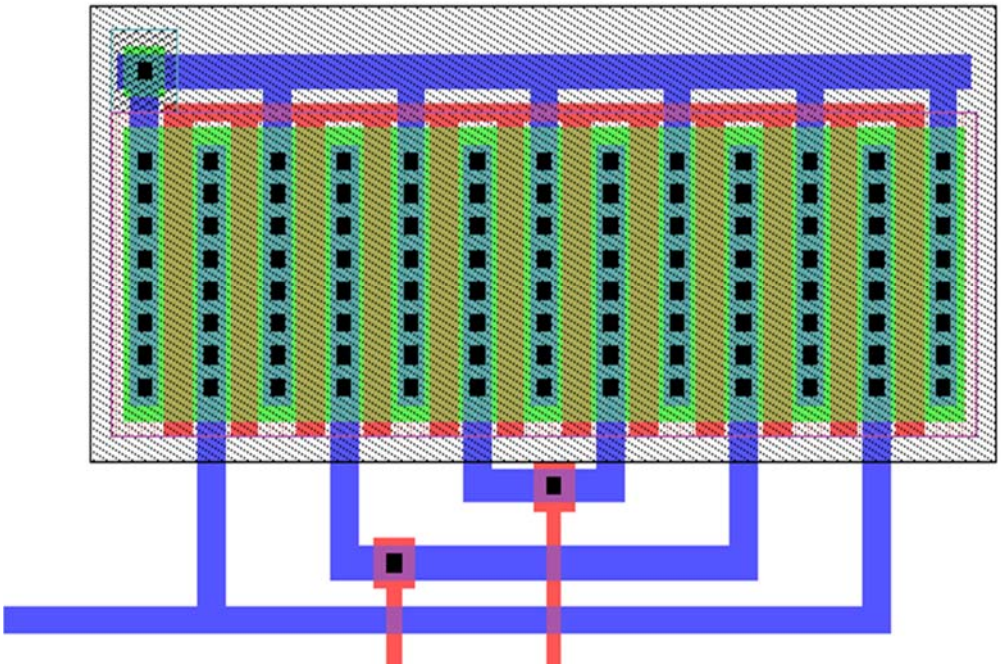
And we will use interdigitation technique for matching

A A B B C C C C B B A A

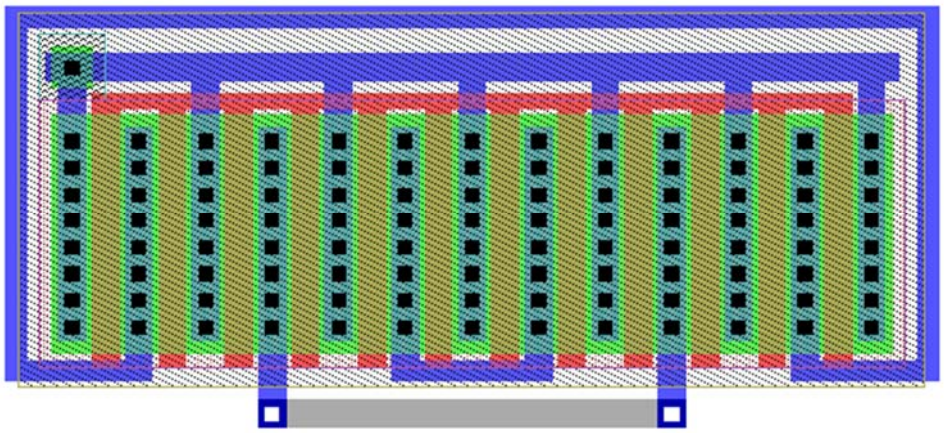
S D S D S D S D S D S D

* All of them have similar source
* All of them have similar gate

We will use first method shown below



Can also be implemented by using metal 2



IMPLEMENTATION FOR RESISTOR

[2] For resistors

⇒ we implemented a unit resistor of 2KΩ and it's of a linear type

∴ we used an N-well resistor with a sheet resistance of 2KΩ/□

↳ instead of using poly type resistor with a sheet resistance of 25Ω/□
↳ it will require very large area in our case

∴ we implement an N-well resistor
↳ 2KΩ (with W and L = 12λ * 12λ)
↳ N-well in our case is used to minimize area

⇒ we will use inter digitation technique for matching

$R_D = 10 \times 2K$
$R_1 = 50 \times 2K$, $R_1 = 50 \times 2K$
$R_L = 100 \times 2K$

} ⇒ stack containing these resistance

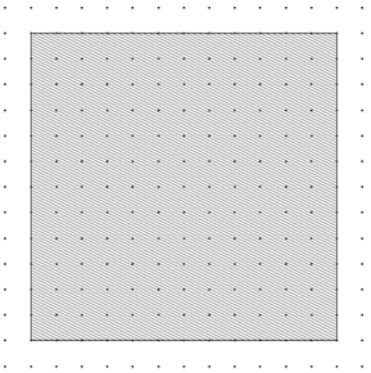
∴ we have a total $210 \times 2K$
∴ we will use 42 finger in our case
∴ $R_D = \frac{10}{210} \times 42 = 2$ finger
$R_1 = \frac{50}{210} \times 42 = 10$ finger
$R_L = \frac{100}{210} \times 42 = 20$ finger

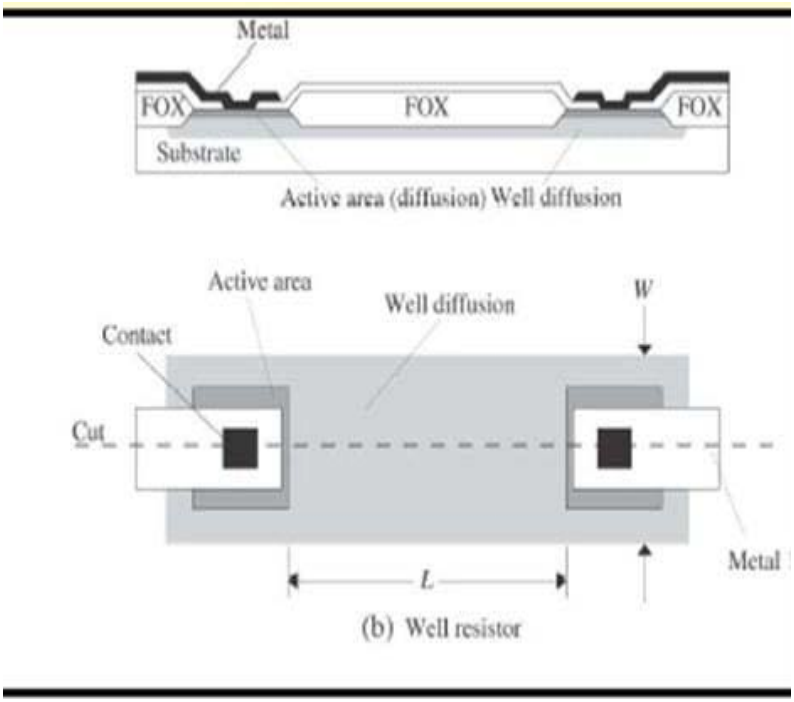
where each finger is made of $5 \times 2K\ \Omega$ //

⇒ $R_D\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L$ →
→ $R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_L\ R_1\ R_D$

Implementation of N-well resistance is shown in the following figure

K.M.S.





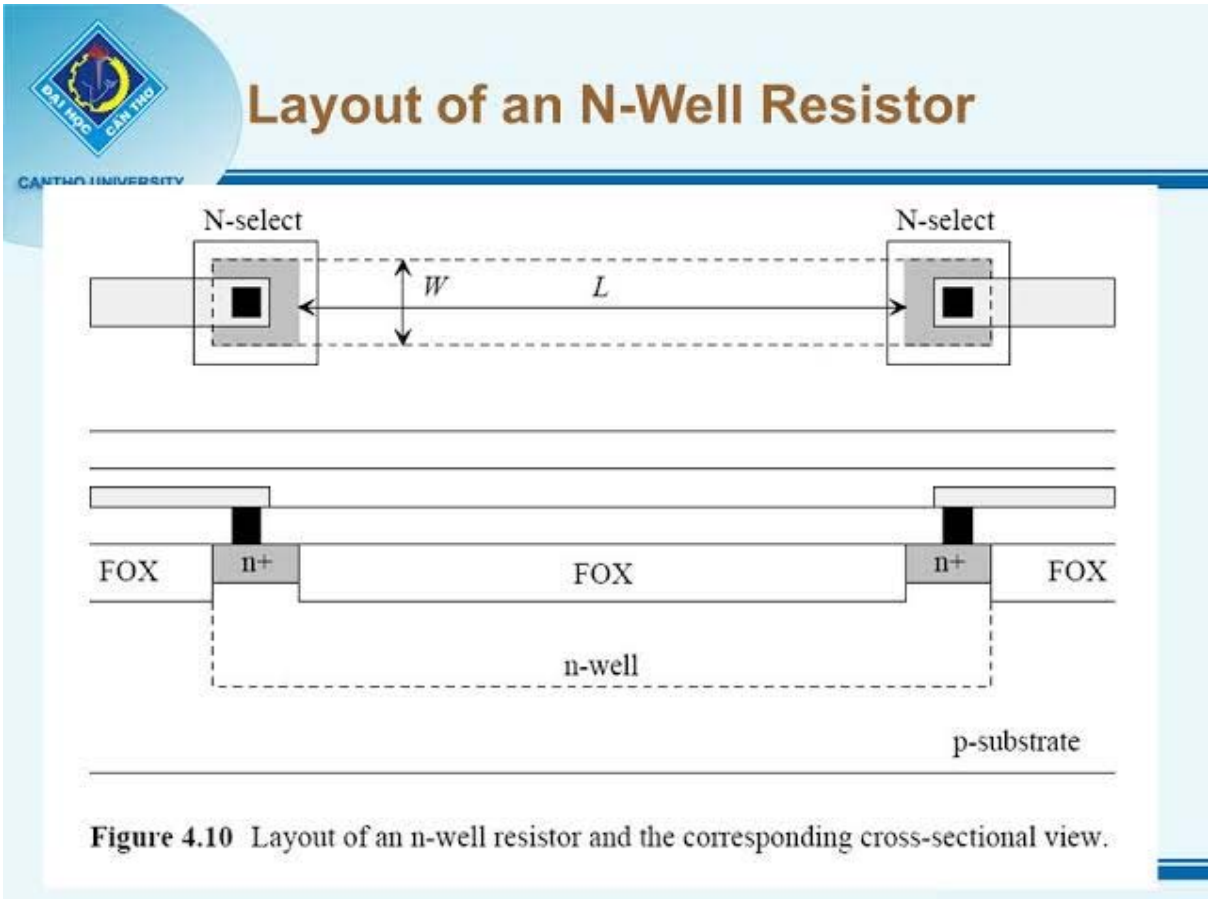
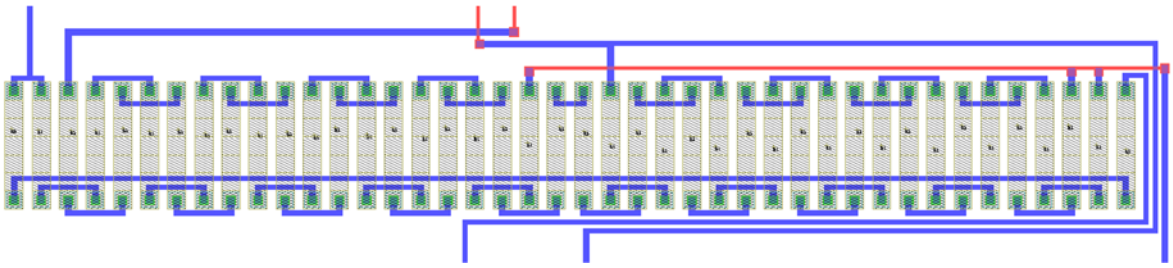


Figure 4.10 Layout of an n-well resistor and the corresponding cross-sectional view.



IMPLEMENTATION FOR N-MOS

[3] for NMOS → we can use fingers to minimize C_{DB} and C_{SB} (parasitic capacitance)

→ we will assume x is of 10nm/1nm similar ratio as for PMOS

↳ ∴ we have a total width of 90nm

∴ we will use 9 fingers

↳ so gate size similar to P-MOS = 10nm / 1um (poly)

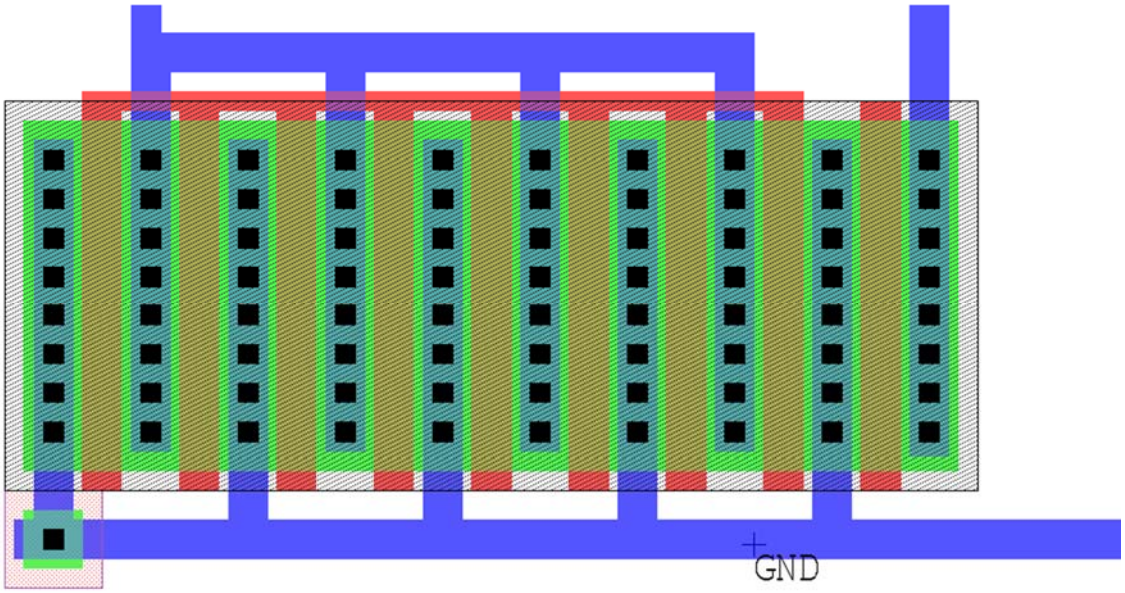
∴ transistor of 8x → we will use 8 fingers

· transistor of 1x → we will use 1 finger

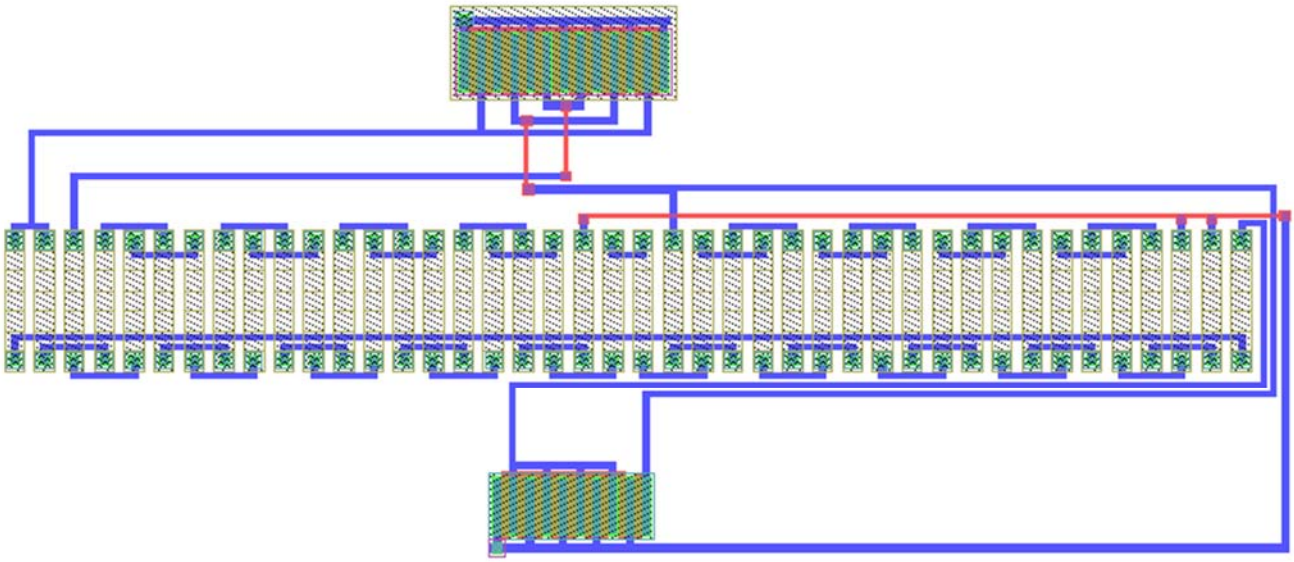
* both have similar source

no matching is required

↳ we only used fingers to reduce capacitance

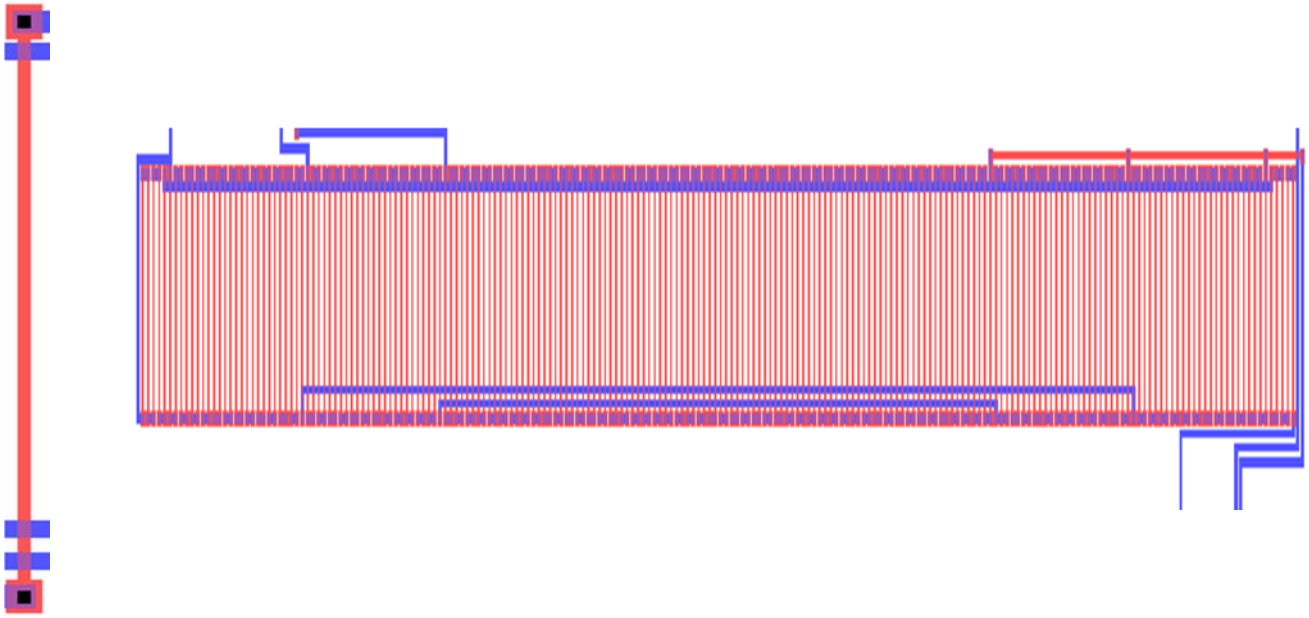


COMPLETE DESIGN:



ANOTHER WAY TO IMPLEMENT A RESISTOR

This is the size of single unit resistor of 2k ohm



Date / / Object

→ we can also implemet resistor using poly but it will result in large area as shown
↳ sheet resistance for poly is 50Ω/□
∴ inorder to implemet 2KΩ resistance we would require 50 units

∴ we will use interdigitation technique for matching
∴ we have a total of 210×2KΩ
↳ we will use 210 fingers
↳ where each finger is of 2KΩ

∴ R_D = 10 finger, R_1 = 50 finger and R_L = 100 finger

will be implemeted as follow:

$R_D(5)$ $R_{1A}(25)$ $R_{1B}(25)$ $R_L(100)$ $R_{1A}(25)$ $R_{1B}(25)$ $R_D(5)$

Complete design for this method