Credit Hours System

ELCN321 VLSI Systems
Cairo University Faculty of Engineering

PROJECT 1

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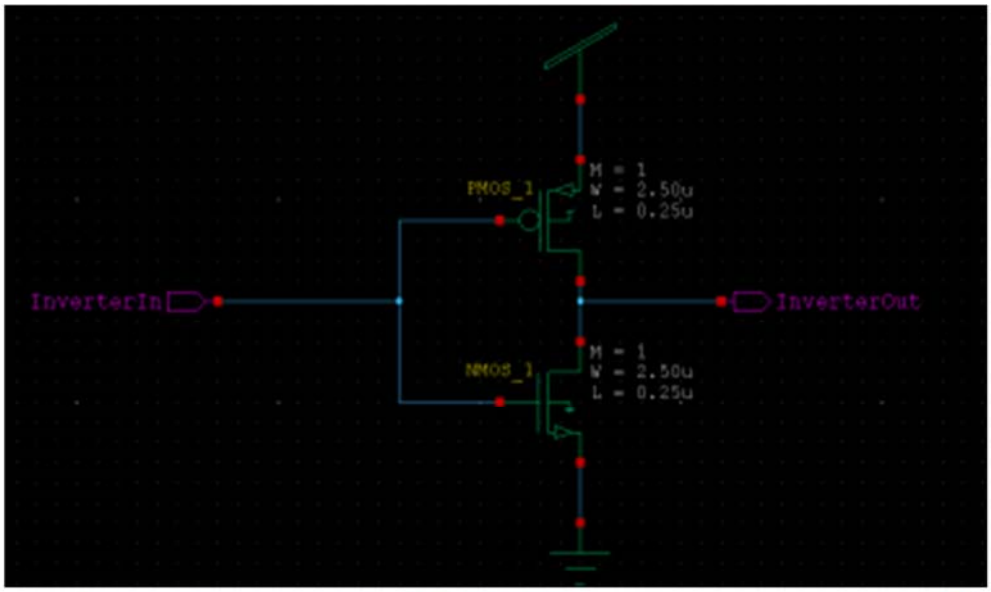
CCEE

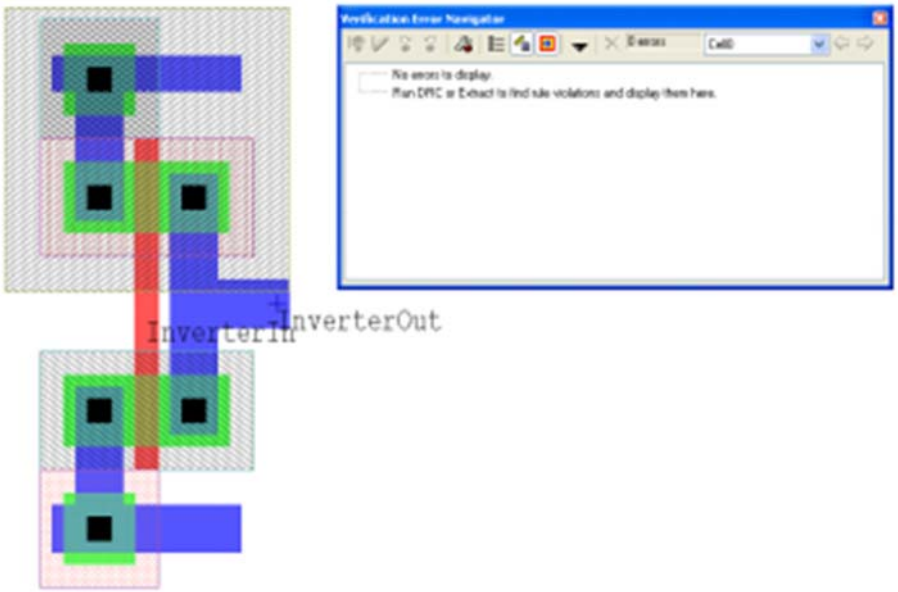
1- Design a FF with the following capabilities:

- Positive Edge CLK
- Asynchronous Preset and Reset signals.

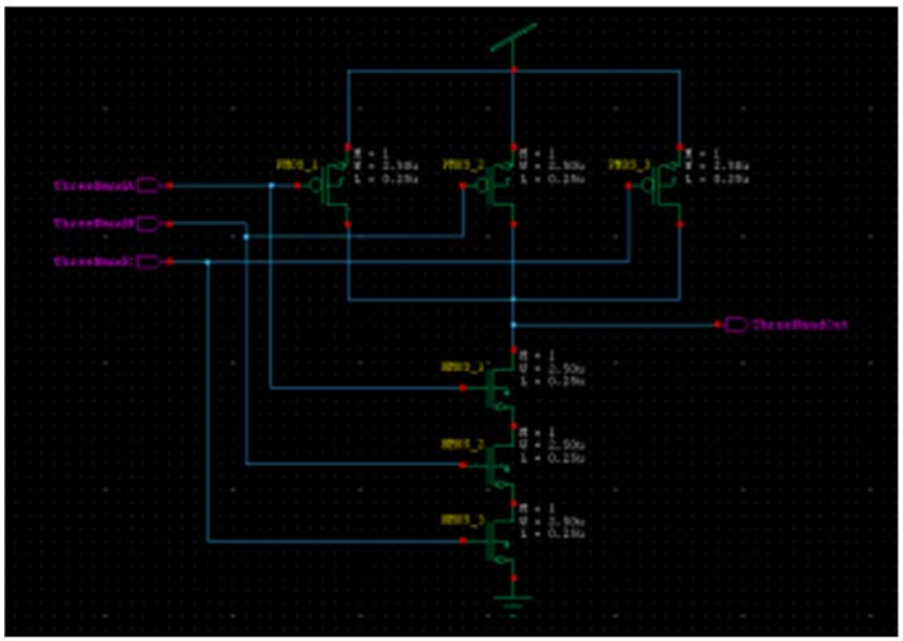
The D-Flip Flop is made of two inverters and six 3-input nand so first we will make the gates

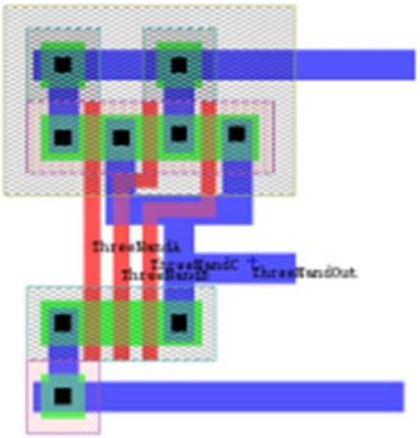
1- Inverter

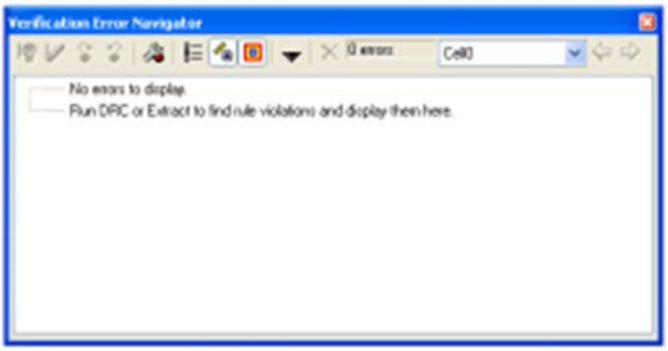




2- 3-input nand







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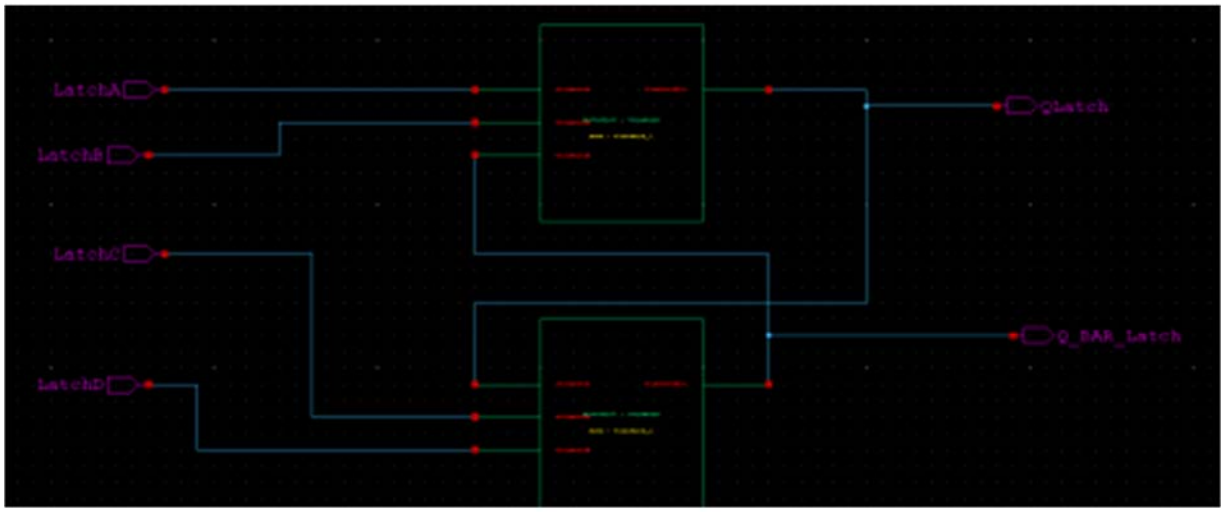
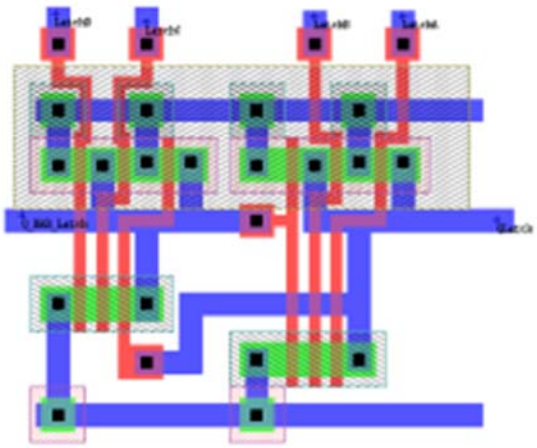
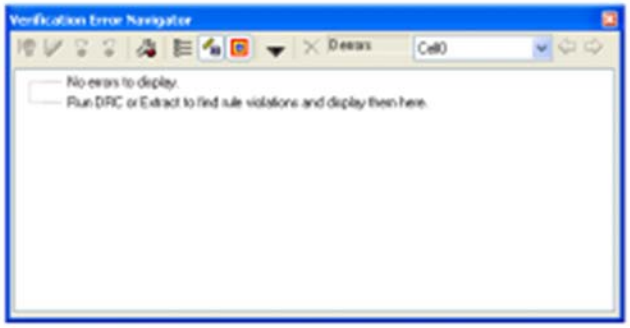
3- Latches

We made a latch from two 3-input nand

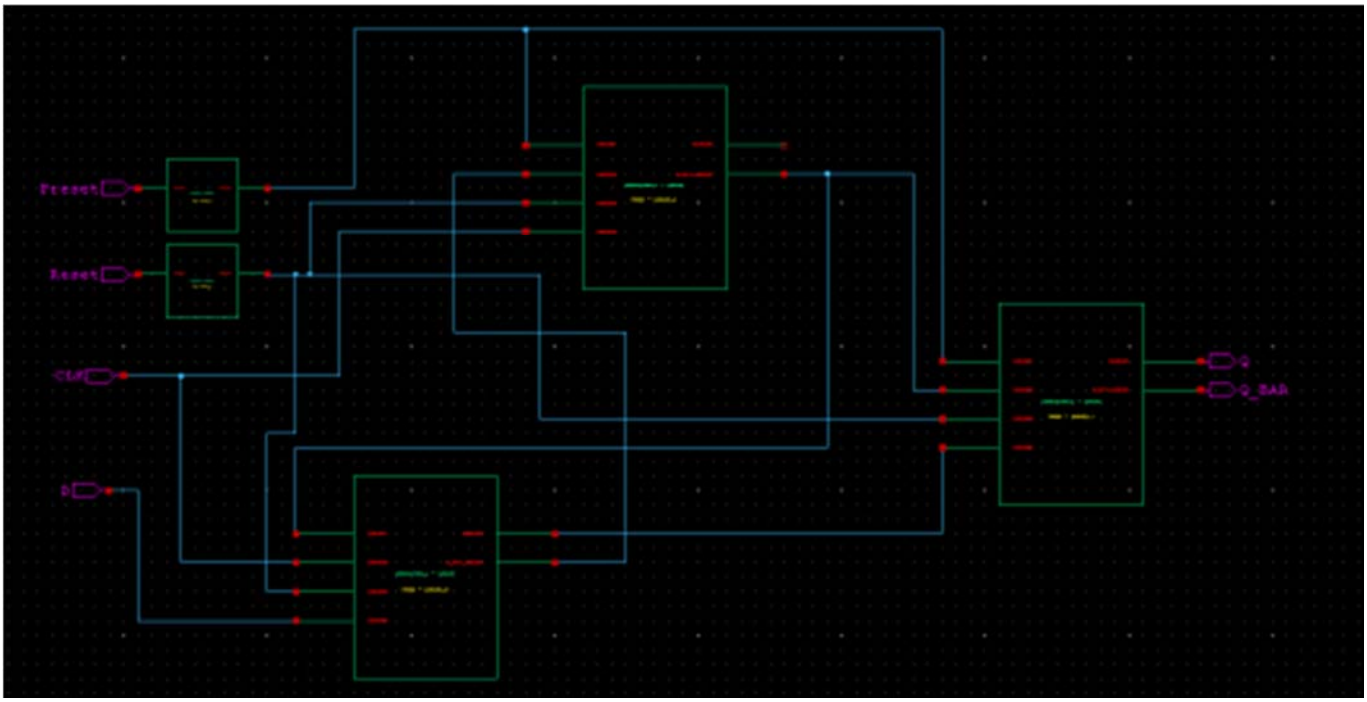




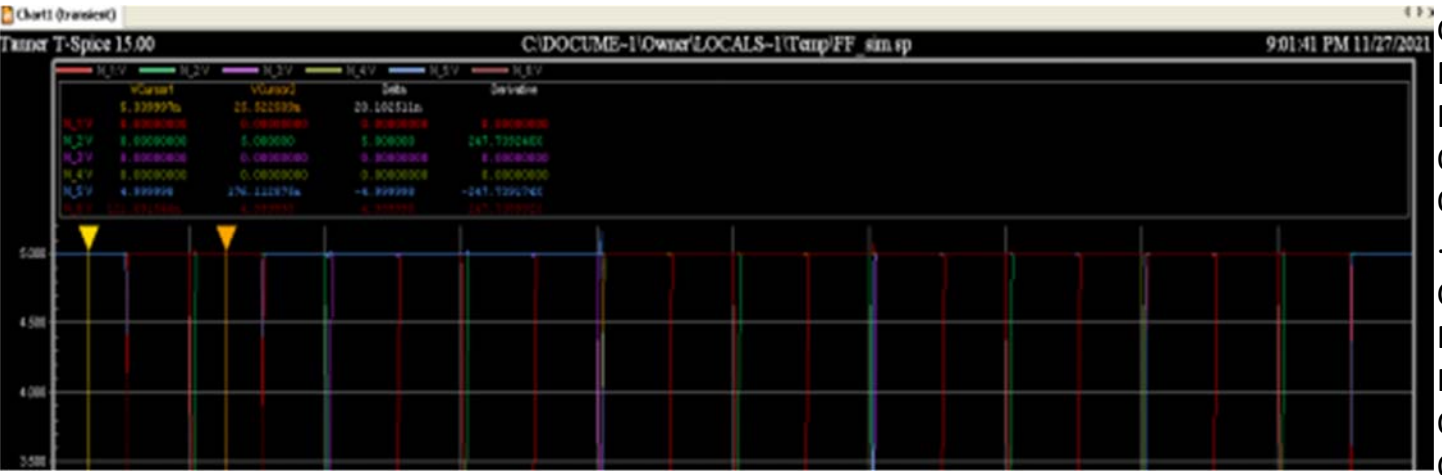


4- Flip flop

We made the flip flop with the two inverters and three latches (six 3-input nand)



2- Create a testbench to test the FF



· D=0, CLK=0, P=0, R=0 -> Q=1, Q'=0

· D=0, CLK=1, P=0, R=0 -> Q=0, Q'=1

D

CLK

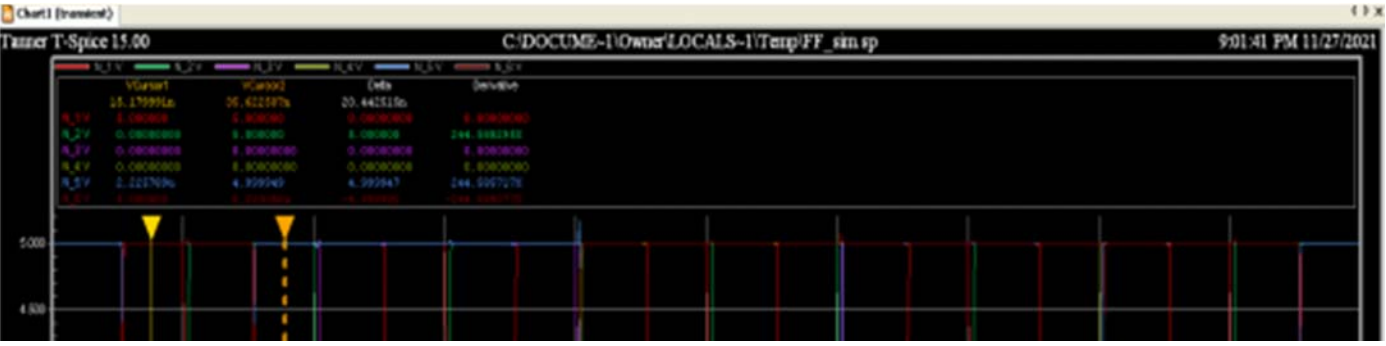
P

R

Q

Q'

· D=1, CLK=0, P=0, R=0 -> Q=0, Q’=1



· D=1, CLK=1, P=0, R=0 -> Q=1, Q’=0

D

CLK

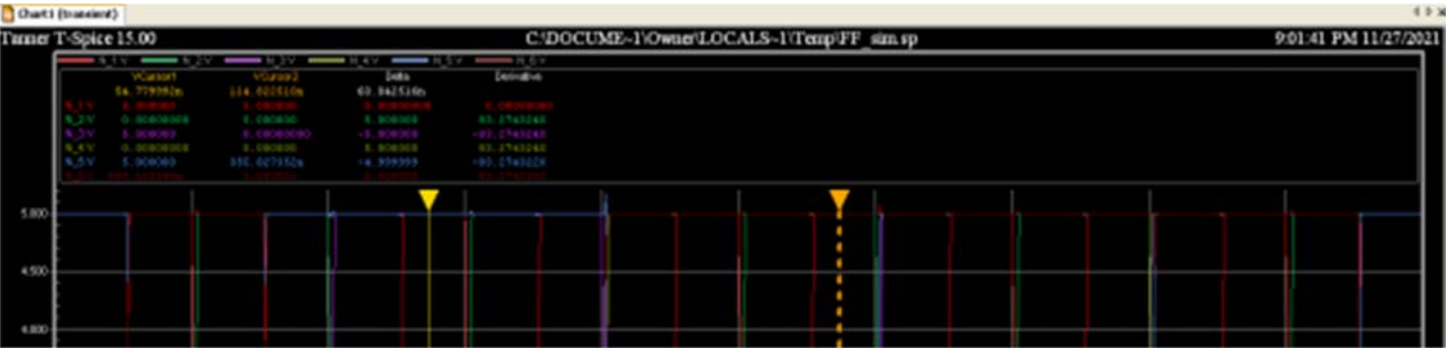
P

R

Q

Q’

· D=1, CLK=0, P=1, R=0 -> Q=1, Q’=0



· D=1, CLK=1, P=0, R=1 -> Q=0, Q’=1

D

CLK

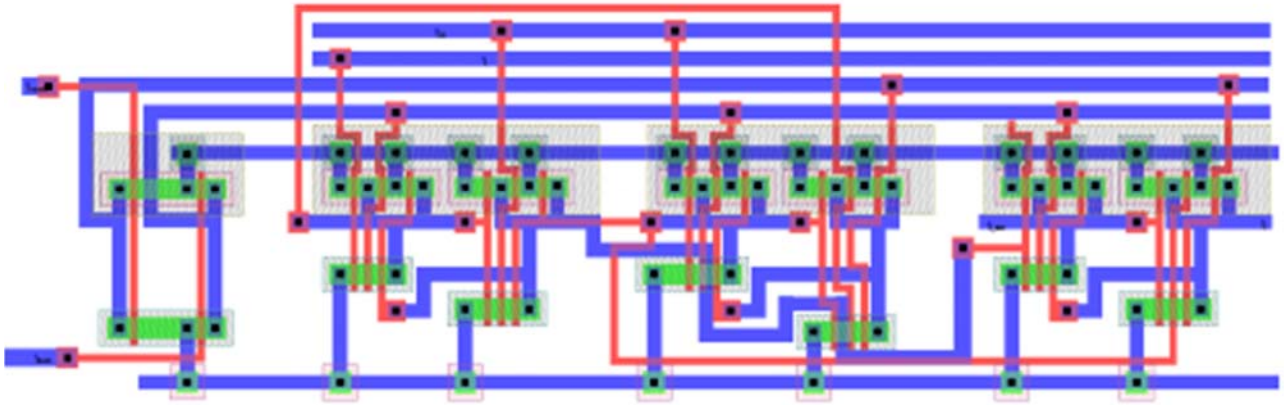
P

R

Q

Q’

3- Layout the cell for a minimum area, use proper □□□□□□, □□□□□□, □□, □□ , □□ and □□ connections to ease top level connections. Make it DRC and LVS clean.



4- Extract the FF and simulate the extracted

version. · D=1, CLK=0, P=0, R=0 -> Q=0, Q’=1

· D=1, CLK=0, P=1, R=0 -> Q=1, Q’=0

The layout gives the same output of the schematic

5- Create top Level schematic of the Serial Interface Bus

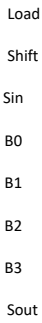
First we created an 8-bit Serial Interface Bus as a building unit

Then we will make the 32-bit SIB with these units

6- Simulate the top level by loading a stream of bits and loading it. Test the “□□□□□□□□□□□□□□□□” signal as well.

We make the simulation on 4-bit SIB first to make the simulation easier and the steps and the results of the 4-bit is the same as 32-bit SIB

Let the steam of bits be 1011.



At first the load registers contain garbage and default = 0 then the CLK began to iterate and the stream of bits enter the shift registers and began to enter the load register when the CLK trigger its positive edge. And the 0 in the stream of bits began to show in the 3rd positive edge of the CLK and it moved to the next register in the following positive edge cycle.

Load

Shift

Sin

B0

B1

B2

B3

Sout

When the default signal is triggered ‘1’ then B0, B2 will be ‘1’ and B1, B3 will be ‘0’

Simulation of 32-bit SIB

7,8- Create a Layout of the top level & Minimize the area.